T-52-33-03

ST62BC003-B
LADR: Low Address Bus Controller:

FEATURES:

- System low address bus latch driver circuit
- Memory address bus latch driver circuit
- Refresh counter circuit
- 14.31818 MHZ video clock oscillator
- 1.5 µm BiCMOS technology
- 68 pin PLCC package

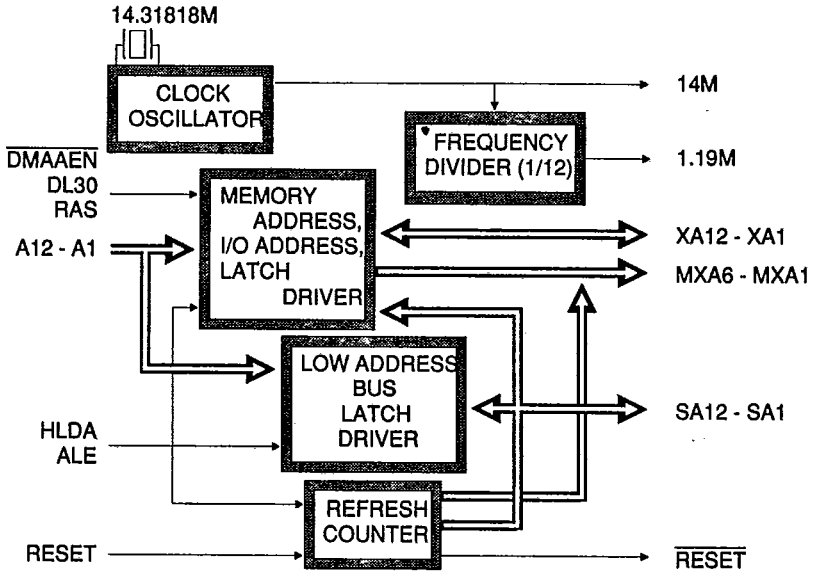
DESCRIPTION:

ST62BC003-B consists of:

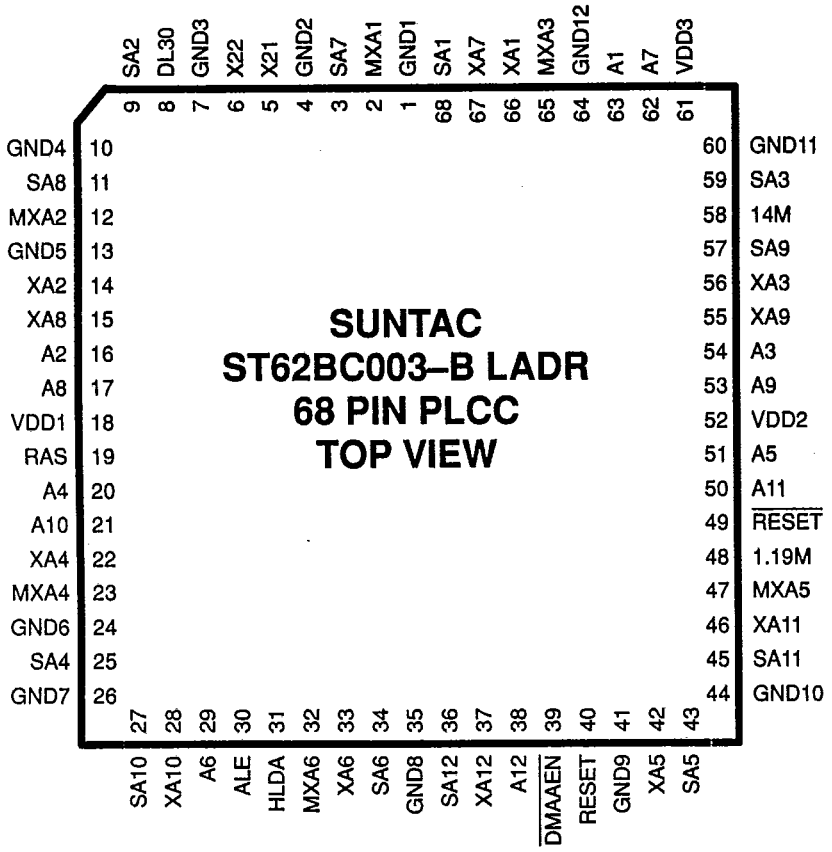
(1) latch drivers which latch and output the low addresses of 80286 CPU to system address bus and memory address bus,
(2) a refresh address counter and
(3) video clock oscillator circuitry.

System address bus and memory address bus are controlled by individual latch timing signal, which enables fast access to system memories, PROM and DRAM during high speed (XTAL-25MHz) memory operation.

ST62BC003-B FUNCTIONAL BLOCK DIAGRAM



ST62BC003-B PIN DIAGRAM



ST62BC003-B
Pin Description

Symbol	Pin No.	Type	Functions
RESET	40	I	Active high input signal to be connected to system reset signal, "RESET".
A1-A12	63, 16 54, 20 51, 29 62, 17 53, 21 50, 38	I	Input terminal to be connected with 80286 address bus, A1-A12.
$\overline{\text{DMAAEN}}$	39	I	Input signal to indicate address signal of 8237 output is valid during DMA.
$\overline{\text{RESET}}$	49	O	Active low output signal of active low, to be connected to system reset signal, "$\overline{\text{RESET}}$".
MXA1-MXA6	12, 2 65, 23 47, 32	O	Address bus for on-board main memory (PROM, DRAM).
SA1-SA12	9, 3 68, 59 43, 25 34, 57 11, 27 45, 36	I/O	Address bus for system address BUS SA1-SA12.
14M	58	O	14MHz clock to be outputted to I/O slot.
HLDA	31	I	Input terminal to be connected with 80286 hold acknowledge signal, "HLDA".
XA1-XA12	66, 14 56, 22 42, 33 67, 15 55, 28 46, 37	I/O	I/O terminal to be connected with address bus for internal I/O devices, XA1-XA12.
DL30	8	I	Input terminal for the multiplexing control of DRAM addresses.

Symbol	Pin No.	Type	Functions
V_{DD}	18, 52 61	I	System power +5V
GND	1,10,26 35, 44 60, 4 7, 13 24,41,64	I	System ground.
1.19M	48	O	1.19MHz clock for programmable interval timer 8254.
X21	5	I	Input terminal to be connected to XTAL14.31818MHz.
X22	6	O	Output terminal to be connected to XTAL14.31818MHz.
RAS	19	I	Input terminal indicating the start of a bus cycle. This signal is active high.
ALE	30	I	Input terminal, connects to "ALE", for address latch enable signal.