



ST62BC002-B

HADR: High Address Bus Decoder

FEATURES:

- Memory address decoder
- 8 modes of system memory size and operation
- Non-adjusting $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ timing signals
- EMS control register
- High address bus driver
- 1.5 μm BiCMOS technology
- 68 pin PLCC package

DESCRIPTION:

ST62BC002-B consists of:

- (1) an address driver circuit for higher address A23-A13 from 80286 CPU to system address bus SA19-SA13, local address bus LA23-LA17, and memory address bus MXA10-7,
- (2) BIOS ROM address decoder,
- (3) D-RAM address decoder,
- (4) higher refresh address counter and
- (5) EMS control register.

Both the 27256 and 27128 can be used for BIOS ROM and 1Mbit, 256Kbit and 64Kbit can be used for system D-RAM.

If 1Mbit memory is used, a maximum of 4MB memory can be furnished on the

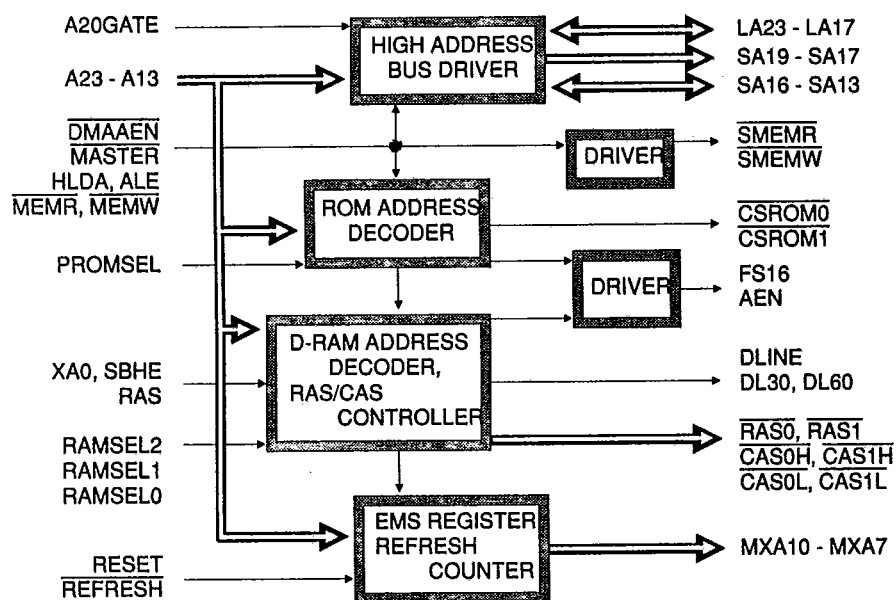
motherboard. This large memory capacity can be effectively used as extended memory or as EMS memory. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals for D-RAM access are generated in ST62BC002-B. It uses an external delay line to set the critical timing and achieve reliable operation.

8 modes of memory operations are available as shown in the "Modes of Memory Operation" table included in this section of this manual.

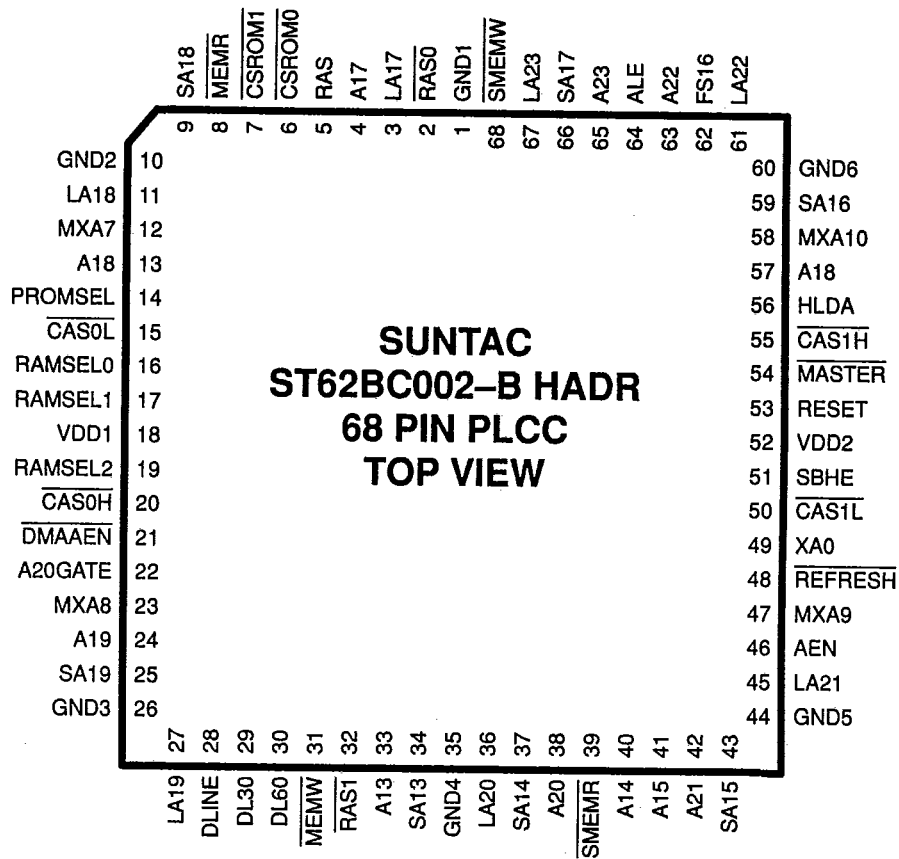
ST62BC002-B contains 6 x 8 bit registers for EMS functions. It holds configuration information such as system memory size, EMS segment start addresses and page numbers.



ST62BC002-B FUNCTIONAL BLOCK DIAGRAM



ST62BC002-B PIN DIAGRAM





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MODES OF MEMORY OPERATION

Mode	RAMSEL			Memory Type		Memory Size	Memory Location
	2	1	0	BANK1	BANK0		
0	L	L	L	NONE	256Kbits	512KB	0-7FFFF
1	L	L	H	64Kbits	256Kbits	640KB	0-9FFFF
2	L	H	L	256Kbits	256Kbits	640KB+384KB	0-9FFFF 100000-15FFFF
3	L	H	H	256Kbits	256Kbits	640KB + EMS (16KB x 24 pages)	0-9FFFF
4	H	L	L	NONE	1Mbits	640KB+1408KB	0-9FFFF 100000-25FFFF
5	H	L	H	NONE	1Mbits	640KB + EMS (16KB x 88 pages)	0-9FFFF
6	H	H	L	1Mbits	1Mbits	640KB + 3456KB	0-9FFFF 100000-45FFFF
7	H	H	H	1Mbits	1Mbits	640KB + EMS (16KB x 216 pages)	0-9FFFF



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Pin Description

Symbol	Pin No.	Type	Functions
LA17-LA23	3, 11, 27 36, 45 61, 67	I/O	I/O terminal, connects to local address bus LA17-LA23.
A13-A23	4, 13, 24 33, 38 40, 41 42, 57 63, 65	I	Input terminal, connects to 80286 address bus A13-A23.
SA17-SA19	66 25, 9	O	Output terminal, connects to system address bus SA17-SA19.
S $\overline{\text{MEMR}}$	39	O	Output signal active when 80286 executes memory cycle in low 1MB address.
MXA7-MXA10	12, 23 47, 58	O	Address bus for on-board main memory (PROM, DRAM).
CSROM0	6	O	Chip select signal for BANK 0 of BIOS ROM.
CSROM1	7	O	Chip select signal for BANK 1 of BIOS ROM.
XA0	49	I	Input terminal, connects to internal I/O address bus, "XA0".
$\overline{\text{MEMR}}$	8	I	Input terminal, connects to " $\overline{\text{MEMR}}$ " signal indicating memory read cycle.
$\overline{\text{MEMW}}$	31	I	Input terminal, connects to " $\overline{\text{MEMW}}$ " signal indicating memory write cycle.
SA13-SA16	34, 37 43, 59	I	System address bus.
RESET	53	I	Input terminal to connect system reset signal "RESET".
MASTER	54	I	Input terminal, connects to I/O slot "MASTER" signal.
HLDA	56	I	Input terminal, connects to 80286 hold acknowledge signal, "HLDA".



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Symbol	Pin No.	Type	Functions
AEN	46	O	Active high output signal indicating address output from DMA controller 8237 to be valid. This signal goes active when "HLDA" is high and "MASTER" is high, too.
REFRESH	48	O	"REFRESH" signal indicating refresh cycle.
FS16	62	O	Output signal connects to "FS16" signal indicating system memory read/write cycle.
DMAAEN	21	I	Input signal indicating address signal of 8237 output to be valid during DMA.
A20GATE	22	I	Input control signal to make address bus A20 active when A20GATE signal is "H".
PROMSEL	14	I	Input signal to select either 27128 or 27256 to be used for BIOS ROM.
RAMSEL0 RAMSEL1 RAMSEL2	16 17 19	I	Input signal to select 4164/41256/411000 to be used for main memory DRAM
DLIN	28	O	Output terminal, connects to input of delay line.
DL30	29	I	Input terminal, connects to delay line 30ns tap.
DL60	30	I	Input terminal, connects to delay line 60ns tap.
CAS1H	55	O	CAS output for higher 9 lines of BANK 1 of main memory DRAM.
CAS1L	50	O	CAS output for lower 9 lines of BANK 1 of main memory DRAM.
CAS0H	20	O	CAS output for higher 9 lines of BANK 0 of main memory DRAM.
CAS0L	15	O	CAS output for lower 9 line of BANK 0 of main memory DRAM.
RAS0	2	O	RAS output for BANK 0.
RAS1	32	O	RAS output for BANK1.
SMEMW	68	O	Active when 80286 executes memory write cycle for low 1MB address
SBHE	51	I	Active low I/O signal indicating SD8-SD15 of system data bus to be valid.

Symbol	Pin No.	Type	Functions
RAS	5	I	Input signal indicating the start of a bus cycle. This signal is active high.
ALE	64	I	Input terminal, connects to "ALE", for address latch enable signal.
VDD	18, 52	...	System power +5V.
GND	1, 35 10, 44 60, 26	...	System ground.