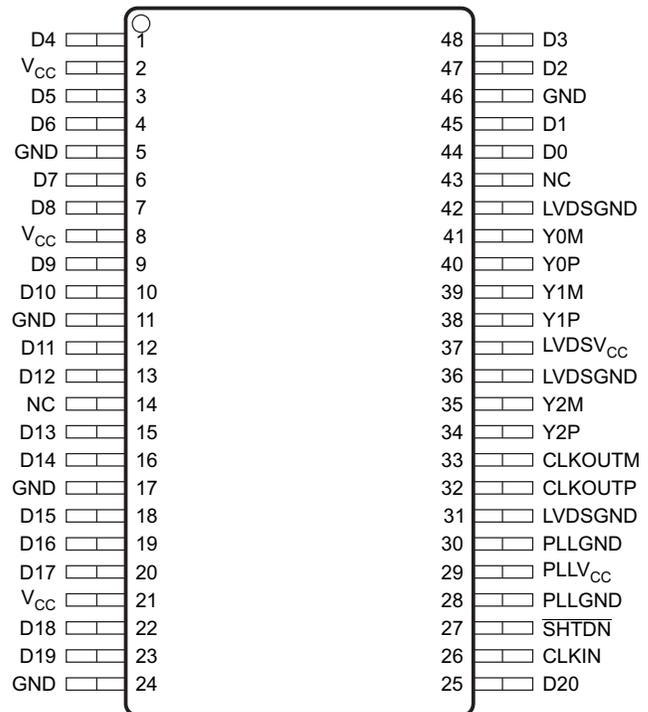# FLATLINK™ TRANSMITTERS

FEATURES

- **21:3 Data Channel Compression at up to 163 Million Bytes per Second Throughput**
- **Suited for SVGA, XGA, or SXGA Data Transmission From Controller to Display With Very Low EMI**
- **21 Data Channels Plus Clock-In Low-Voltage TTL and 3 Data Channels Plus Clock-Out Low-Voltage Differential**
- **Operates From a Single 3.3-V Supply and 250 mW (Typ)**
- **5-V Tolerant Data Inputs**
- **ESD Protection Exceeds 6 kV**
- **SN75LVDS84 Has Falling-Clock Edge-Triggered Inputs**
- **Packaged in Thin Shrink Small-Outline Package (TSSOP) With 20-Mil Terminal Pitch**
- **Consumes Less Than 1 mW When Disabled**
- **Wide Phase-Lock Input Frequency Range:**
  - **31 MHz to 68 MHz**
- **No External Components Required for PLL**
- **Outputs Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard**
- **Improved Replacement for the DS90C561**

DGG PACKAGE
(TOP VIEW)

D4	1		48	D3
V_{CC}	2		47	D2
D5	3		46	GND
D6	4		45	D1
GND	5		44	D0
D7	6		43	NC
D8	7		42	LVDSGND
V_{CC}	8		41	Y0M
D9	9		40	Y0P
D10	10		39	Y1M
GND	11		38	Y1P
D11	12		37	$LVDSV_{CC}$
D12	13		36	LVDSGND
NC	14		35	Y2M
D13	15		34	Y2P
D14	16		33	CLKOUTM
GND	17		32	CLKOUTP
D15	18		31	LVDSGND
D16	19		30	PLLGND
D17	20		29	$PLLV_{CC}$
V_{CC}	21		28	PLLGND
D18	22		27	$\overline{SHTDN}$
D19	23		26	CLKIN
GND	24		25	D20

NC - Not Connected

P0052-02

DESCRIPTION

The SN75LVDS84 FlatLink™ transmitter contains three 7-bit parallel-load serial-out shift registers, a 7× clock synthesizer, and four low-voltage differential signaling (LVDS) line drivers in a single integrated circuit. These functions allow 21 bits of single-ended low-voltage TTL (LVTTL) data to be synchronously transmitted over three balanced-pair conductors for receipt by a compatible receiver, such as the SN75LVDS82 or SN75LVDS86.

When transmitting, data bits D0–D20 are each loaded into registers of the SN75LVDS84 on the falling edge of the input clock signal (CLKIN). The frequency of CLKIN is multiplied seven times and then used to unload the data registers in 7-bit slices and serially. The three serial streams and a phase-locked clock (CLKOUT) are then output to LVDS output drivers. The frequency of CLKOUT is the same as the input clock, CLKIN.

AVAILABLE OPTIONS[1]

LATCHING CLOCK EDGE
FALLING
SN75LVDS84DGG
SN75LVDS84DGGR

(1) The R suffix indicates taped and reeled packaging.

DESCRIPTION (CONTINUED)

The SN75LVDS84 requires no external components and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user(s). The only possible user intervention is the use of the shutdown/clear ($\overline{\text{SHTDN}}$) active-low input to inhibit the clock and shut off the LVDS output drivers for lower power consumption. A low level on this signal clears all internal registers to a low level.

The SN75LVDS84 is characterized for operation over ambient free-air temperatures of 0°C to 70°C.

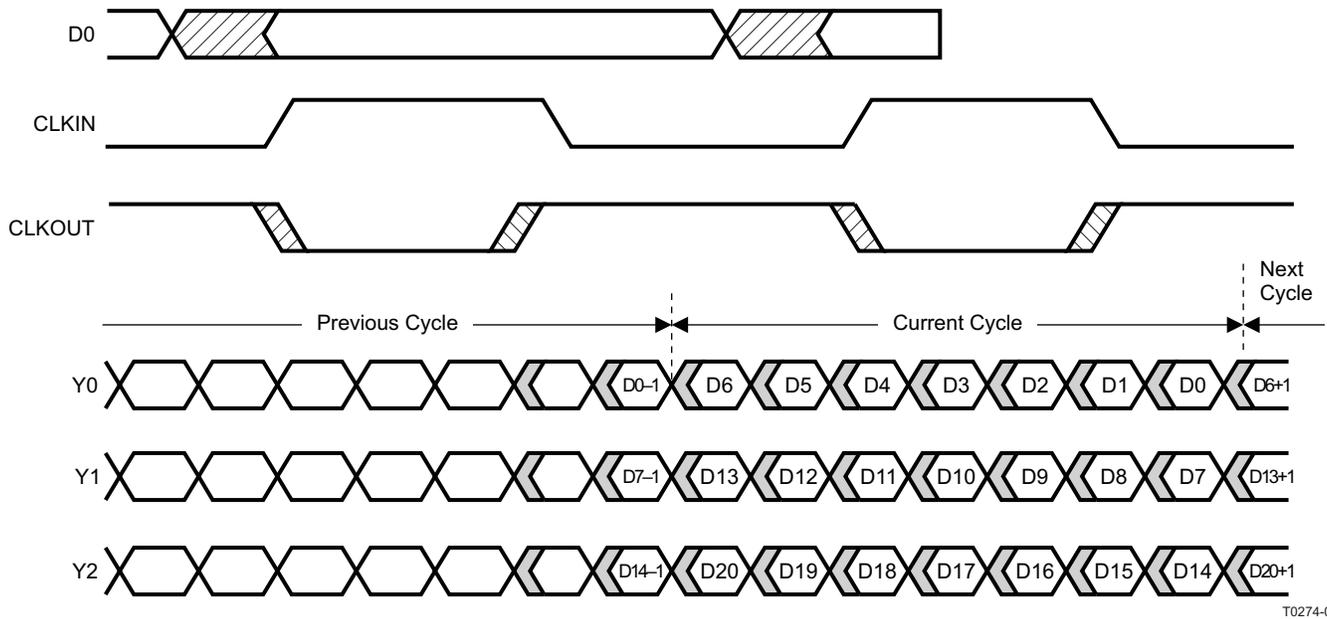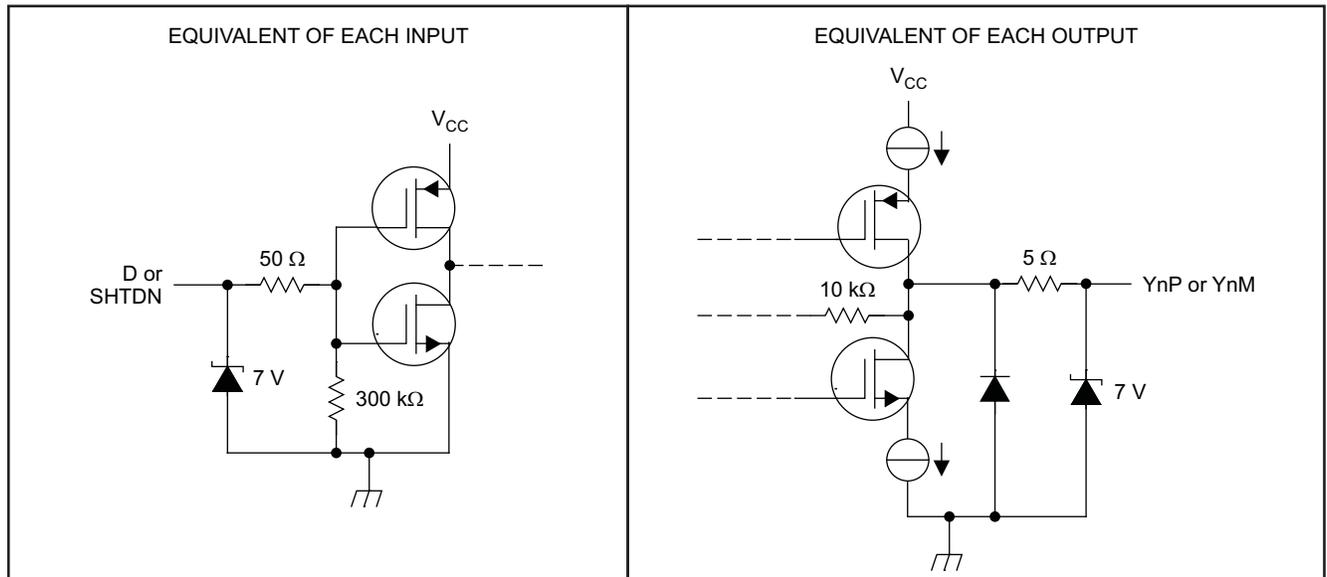## FUNCTIONAL BLOCK DIAGRAM

B0274-01

Product Folder Link(s) :*SN75LVDS84*
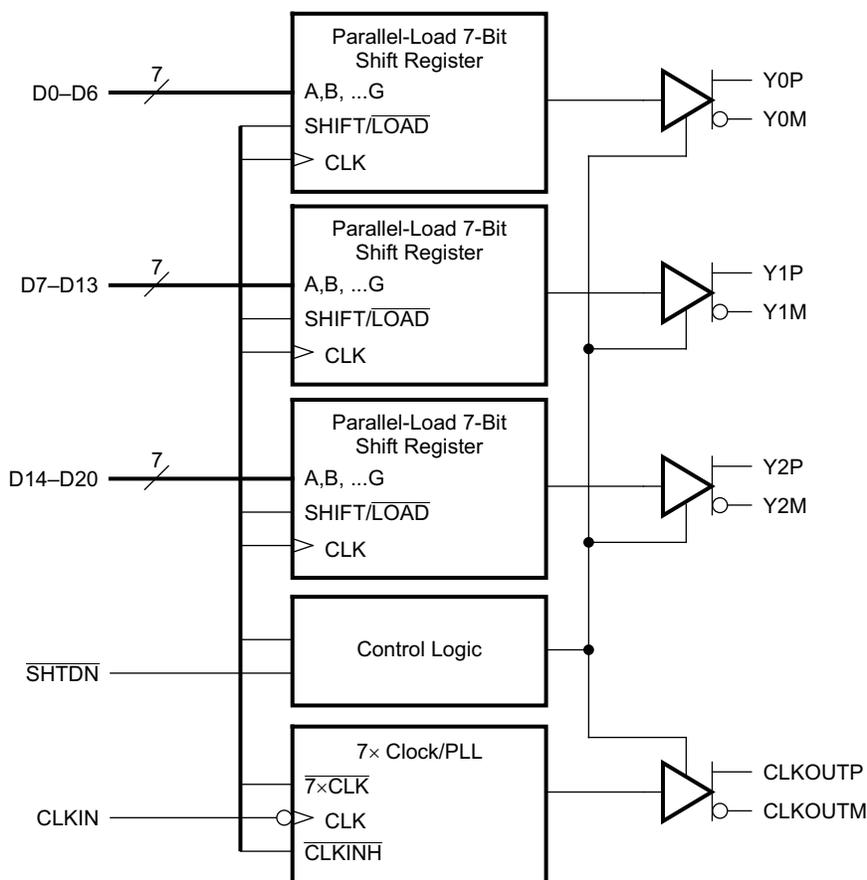
Figure 1. Load and Shift Timing Sequences

SCHEMATICS OF INPUT AND OUTPUT

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) [1]

		VALUE	UNIT
V_{CC}	Supply voltage range[2]	−0.5 to 4	V
V_O	Output voltage range (all terminals)	−0.5 to V_{CC} + 0.5	V
V_I	Input voltage range (all terminals)	−0.5 to 5.5	
	Continuous total power dissipation	See Dissipation Rating Table	
T_{stg}	Storage temperature range	−6 to 150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to the GND terminals.

DISSIPATION RATINGS

PACKAGE	$T_A \leq 25$°C POWER RATING	DERATING FACTOR[1] ABOVE T_A = 25°C	T_A = 70°C POWER RATING
DGG	1316 mW	13.1 mW/°C	726 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
Z_L	Differential load impedance	90		132	Ω
T_A	Operating free-air temperature	0		70	°C

TIMING REQUIREMENTS

	PARAMETER	MIN	TYP	MAX	UNIT
t_c	Input clock period	14.7		32.4	ns
t_w	Pulse duration, high-level input clock	0.4 t_c		0.6 t_c	ns
t_t	Transition time, input signal			5	ns
t_{su}	Setup time, data, D0−D27 valid before CLKIN↓ (See Figure 2)	3			ns
t_h	Hold time, data, D0−D27 valid after CLKIN↓ (See Figure 2)	1.5			ns

Product Folder Link(s) :*SN75LVDS84*

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
V_{IT}	Input threshold voltagee			1.4		V
$|V_{OD}|$	Differential steady-state output voltage magnitude		247		454	mV
$\Delta|V_{OD}|$	Change in the steady-state differential output voltage magnitude between opposite binary states	R_L = 100 Ω, See Figure 3			50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	1.125		1.375	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			80	150	mV
I_{IH}	High-level input current	$V_{IH} = V_{CC}$			20	μA
I_{IL}	Low-level input current	V_{IL} = 0			±10	μA
I_{OS}	Short-circuit output current	$V_{O(Yn)}$ = 0			±24	mA
		V_{OD} = 0			±12	mA
I_{OZ}	High-impedance output current	V_O = 0 to V_{CC}			±10	μA
$I_{CC(AVG)}$	Quiescent supply current (average)	Disabled, all inputs at GND			280	μA
		Enabled, R_L = 100 Ω (4 places), gray-scale pattern (see Figure 4), V_{CC} = 3.3 V, t_c = 15.38 ns		68	80	mA
		Enabled, R_L = 100 Ω, (4 places), worst-case pattern (see Figure 5), t_c = 15.38 ns		75	100	mA
C_I	Input capacitance			3		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
t_{d0}	Delay time, CLKOUT↑ to serial bit position 0	$t_c = 15.38$ ns (±0.2%), |Input clock jitter| < 50 ps[2], See Figure 6	−0.2	0	0.2	ns
t_{d1}	Delay time, CLKOUT↑ to serial bit position 1		$\frac{1}{7}t_C - 0.2$		$\frac{1}{7}t_C + 0.2$	ns
t_{d2}	Delay time, CLKOUT↑ to serial bit position 2		$\frac{2}{7}t_C - 0.2$		$\frac{2}{7}t_C + 0.2$	ns
t_{d3}	Delay time, CLKOUT↑ to serial bit position 3		$\frac{3}{7}t_C - 0.2$		$\frac{3}{7}t_C + 0.2$	ns
t_{d4}	Delay time, CLKOUT↑ to serial bit position 4		$\frac{4}{7}t_C - 0.2$		$\frac{4}{7}t_C + 0.2$	ns
t_{d5}	Delay time, CLKOUT↑ to serial bit position 5		$\frac{5}{7}t_C - 0.2$		$\frac{5}{7}t_C + 0.2$	ns
t_{d6}	Delay time, CLKOUT↑ to serial bit position 6		$\frac{6}{7}t_C - 0.2$		$\frac{6}{7}t_C + 0.2$	ns
$t_{sk(o)}$	Output skew, $t_n - \frac{n}{7}t_C$		−0.2		0.2	ns
t_{d7}	Delay time, CLKIN↓ to CLKOUT↑	$t_c = 15.38$ ns (±0.2%), |Input clock jitter| < 50 ps[2], see Figure 6		4.2		ns
$\Delta t_{c(o)}$	Cycle time, output clock jitter[3]	$t_c = 15.38 + 0.75 \sin(2\pi 500E3t) \pm 0.05$ ns, See Figure 7		±70		ps
		$t_c = 15.38 + 0.75 \sin(2\pi 3E3t) \pm 0.05$ ns, See Figure 7		±187		ps
t_w	Pulse duration, high-level output clock			$\frac{4}{7}t_C$		ns
t_t	Transition time, differential output voltage (t_r or t_f)	See Figure 3	260	700	1500	ps
t_{en}	Enable time, $\overline{\text{SHTDN}}$↑ to phase lock (Yn valid)	See Figure 8		1		ms
t_{dis}	Disable time, $\overline{\text{SHTDN}}$↓ to off state (CLKOUT low)	See Figure 9		250		ns

(1) All typical values are at $V_{CC} = 3.3$ V, $T_A = 25°C$.
(2) |Input clock jitter| is the magnitude of the change in the input clock period.
(3) Output clock jitter is the change in the output clock period from one cycle to the next cycle observed over 15,000 cycles.

Product Folder Link(s) :*SN75LVDS84*

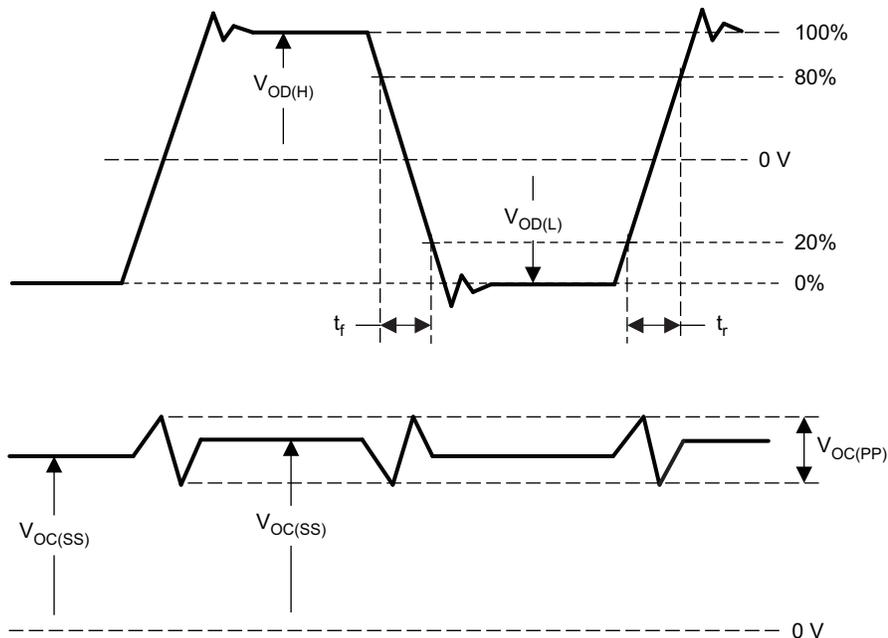## PARAMETER MEASUREMENT INFORMATION
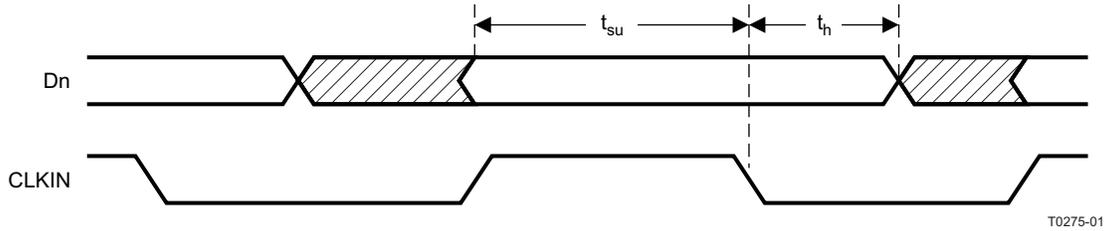
A.   All input timing is defined at 1.4 V on an input signal with a 10%-to-90% rise or fall time of less than 5 ns.

Figure 2. Setup and Hold Time Definition
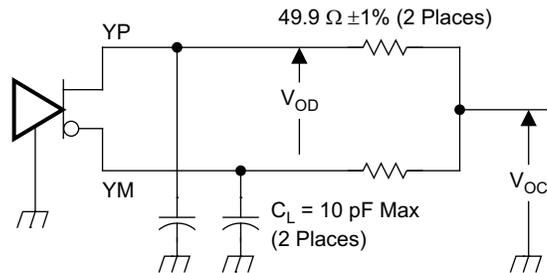
Note: The lumped instrumentation capacitance for any single-ended voltage measurement is less than or equal to 10 pF. When making measurements at YP or YM, the complementary output is similarly loaded.
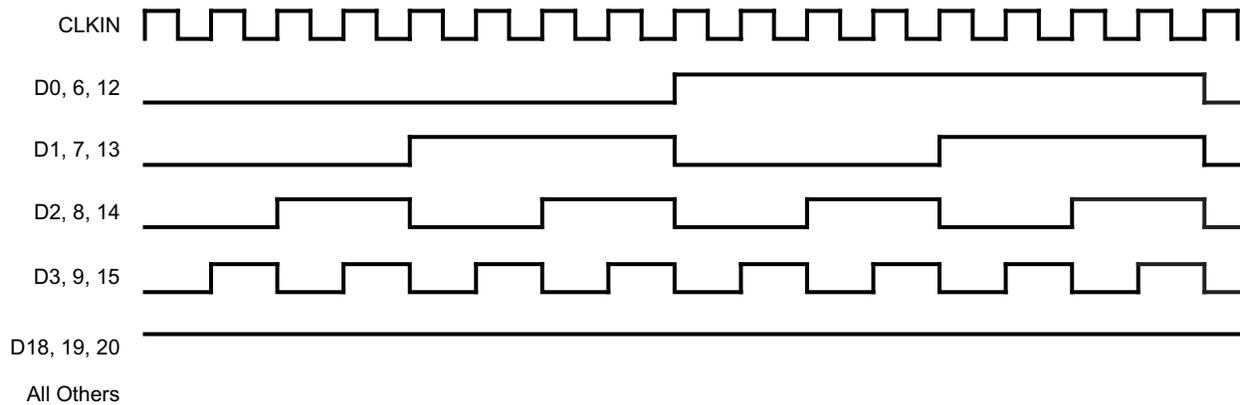
(a) Schematic

(b) Waveforms

Figure 3. Test Load and Voltage Definitions for LVDS Outputs

PARAMETER MEASUREMENT INFORMATION (continued)

CLKIN

D0, 6, 12

D1, 7, 13

D2, 8, 14

D3, 9, 15

D18, 19, 20

All Others

T0276-01

A.   The 16-grayscale test-pattern test device power consumption for a typical display pattern.

B. V_{IH} = 2 V and V_{IL} = 0.8 V

Figure 4. 16-Grayscale Test-Pattern Waveforms

t_c

CLKIN

Even Dn

Odd Dn
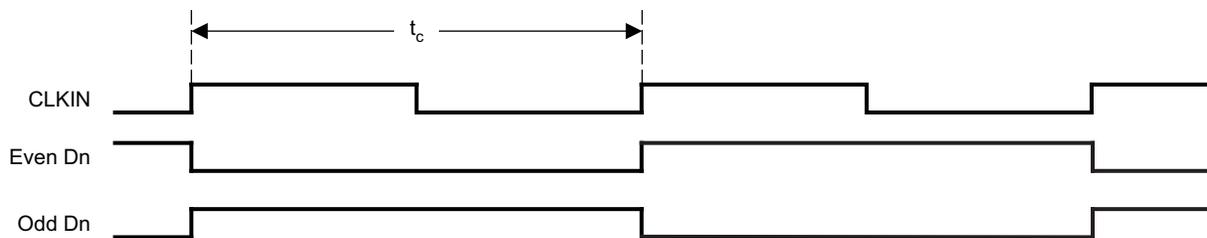
T0277-01

A.   The worst-case test pattern produces nearly the maximum switching frequency for all of the LVDS outputs.

B. V_{IH} = 2 V and V_{IL} = 0.8 V

Figure 5. Worst-Case Test-Pattern Waveforms

Product Folder Link(s) :*SN75LVDS84*

PARAMETER MEASUREMENT INFORMATION (continued)
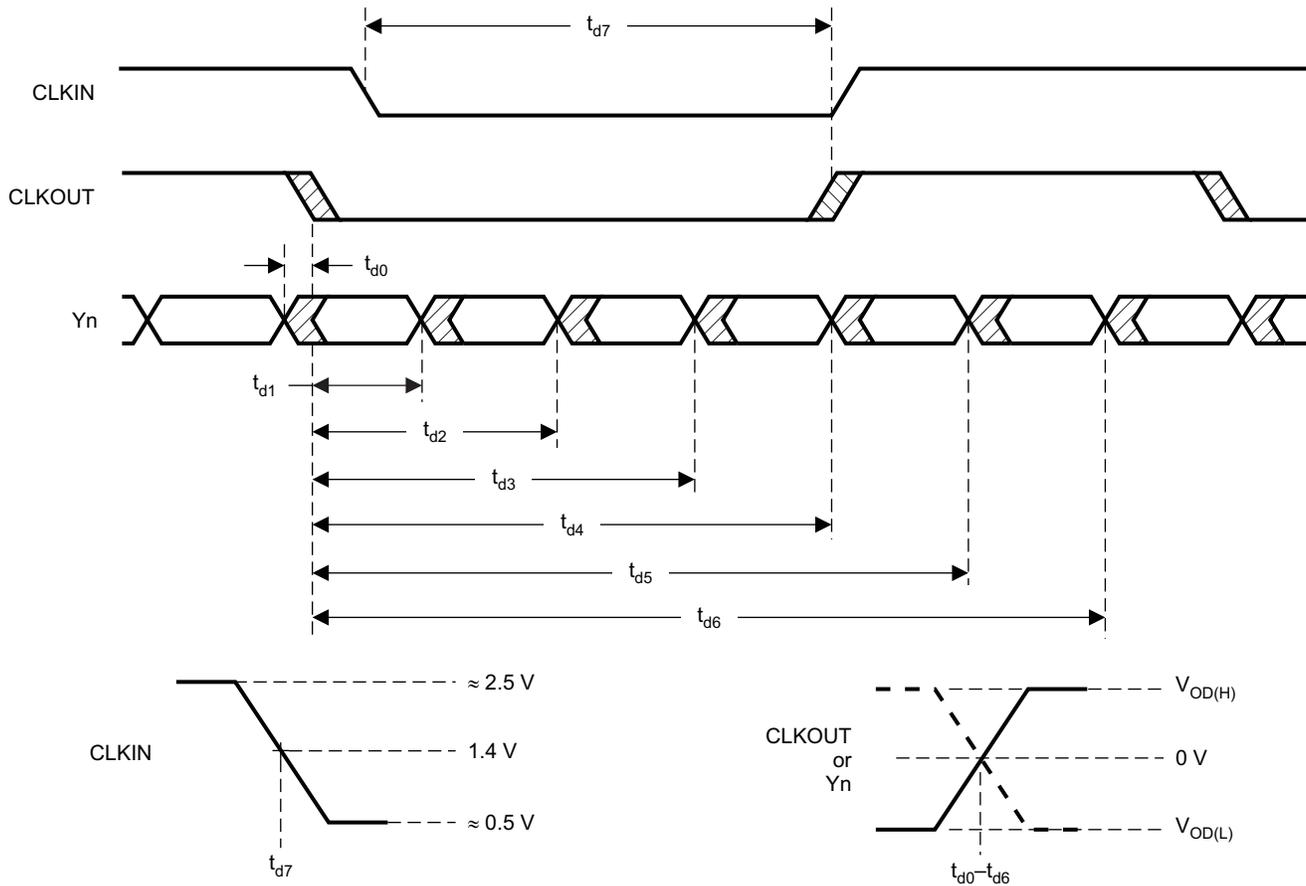
Figure 6. Timing Definitions

V(t) = A sin ($2\pi f_{mod} t$)
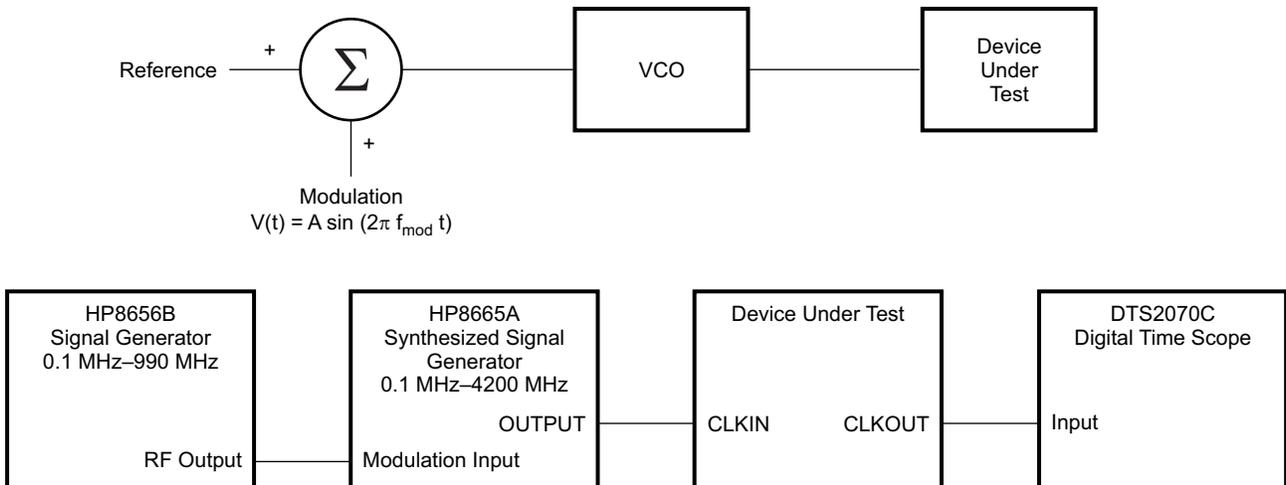
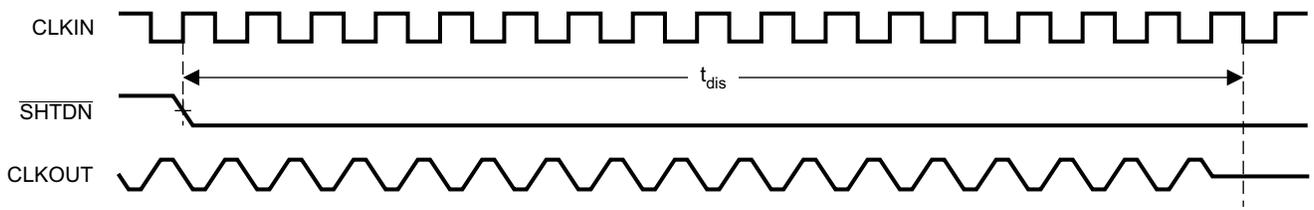**Figure 7. Clock Jitter Test Setup**

TYPICAL CHARACTERISTICS
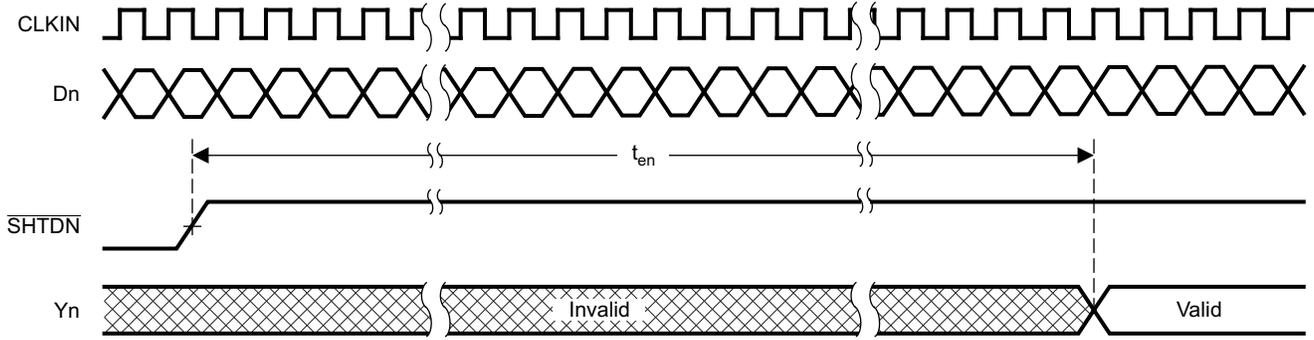
Figure 8. Enable Time Waveforms

Figure 9. Disable Time Waveforms

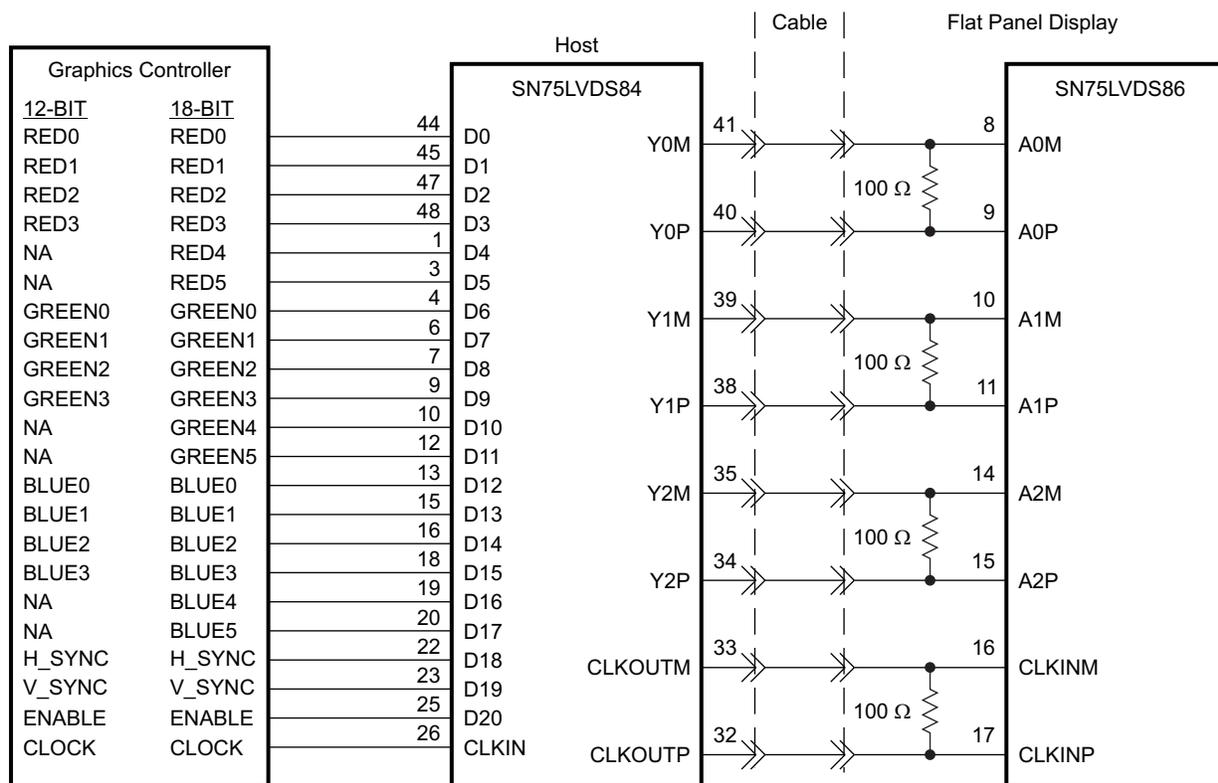**Figure 10.**

Figure 11.

Product Folder Link(s) :*SN75LVDS84*
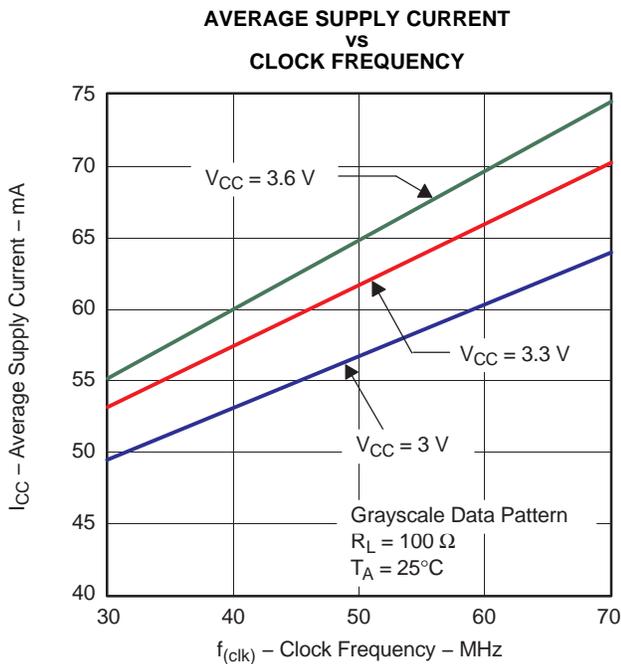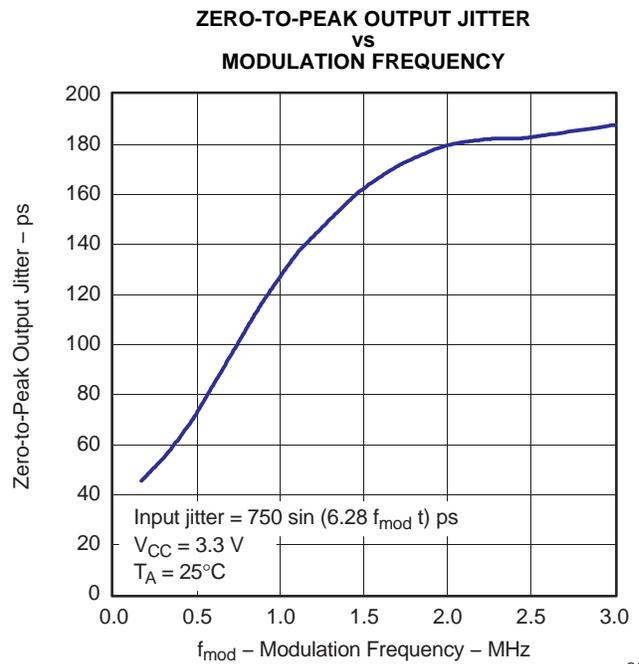
APPLICATION INFORMATION

A. The five 100-Ω terminating resistors are recommended to be 0603 types.

B. NA – not applicable, these unused inputs should be left open.
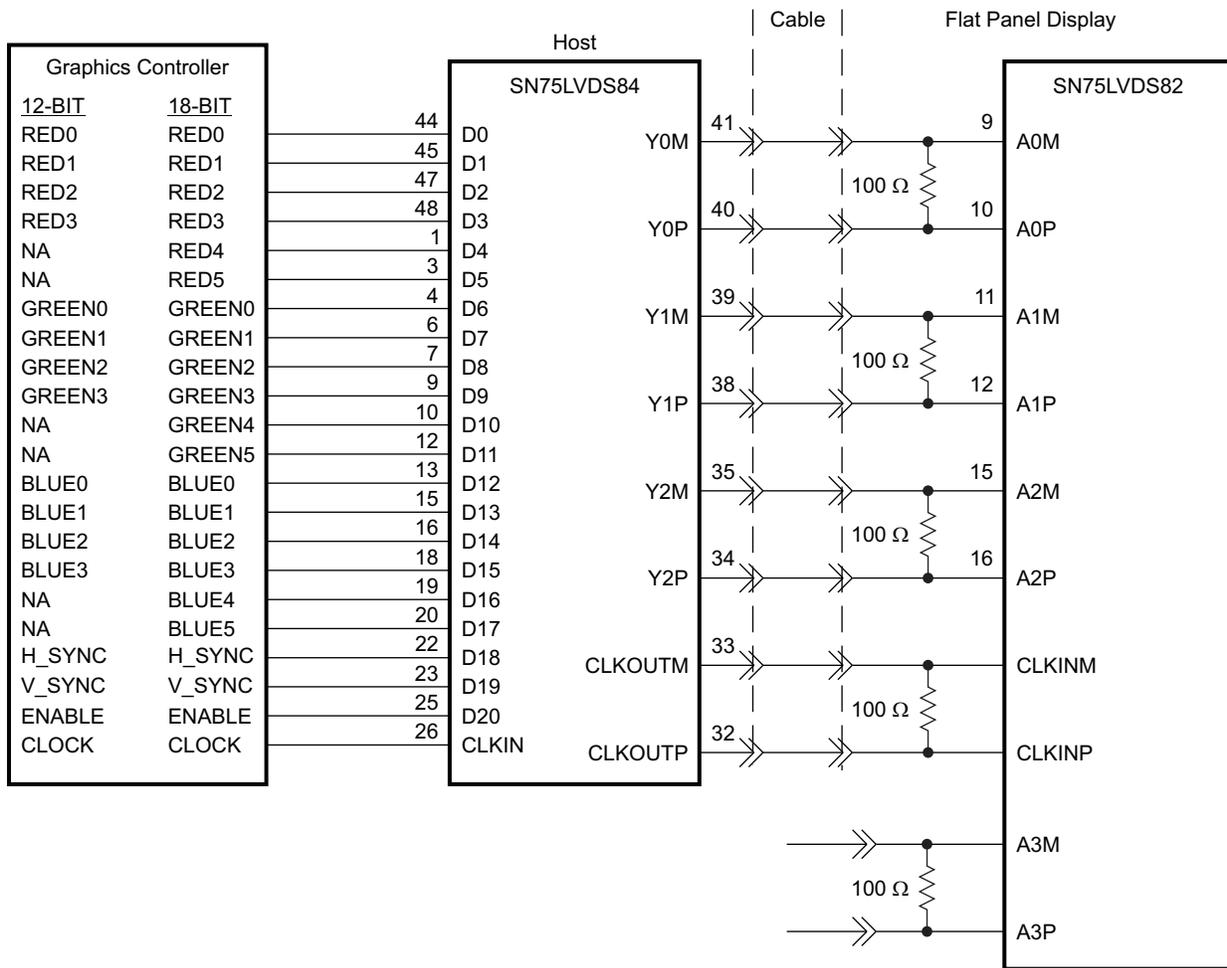
Figure 12. Color Host to LCD Panel Application

B0277-01

A. The four 100-Ω terminating resistors are recommended to be 0603 types.

B. NA – not applicable, these unused inputs should be left open.

Figure 13. 18-Bit Color Host to 24-Bit LCD Display Panel Application
(See the FlatLink Designer's Guide (SLLA012) for more application information.)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75LVDS84DGG	Active	Production	TSSOP (DGG) | 48	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75LVDS84
SN75LVDS84DGG.Z	Active	Production	TSSOP (DGG) | 48	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75LVDS84
SN75LVDS84DGGG4	Active	Production	TSSOP (DGG) | 48	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75LVDS84
SN75LVDS84DGGR	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75LVDS84
SN75LVDS84DGGR.Z	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75LVDS84
SN75LVDS84DGGRG4.Z	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75LVDS84

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
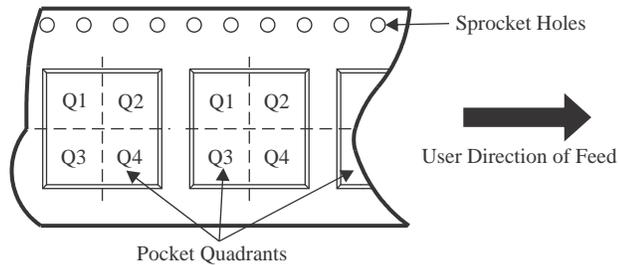
(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LVDS84DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LVDS84DGGR	TSSOP	DGG	48	2000	350.0	350.0	43.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width
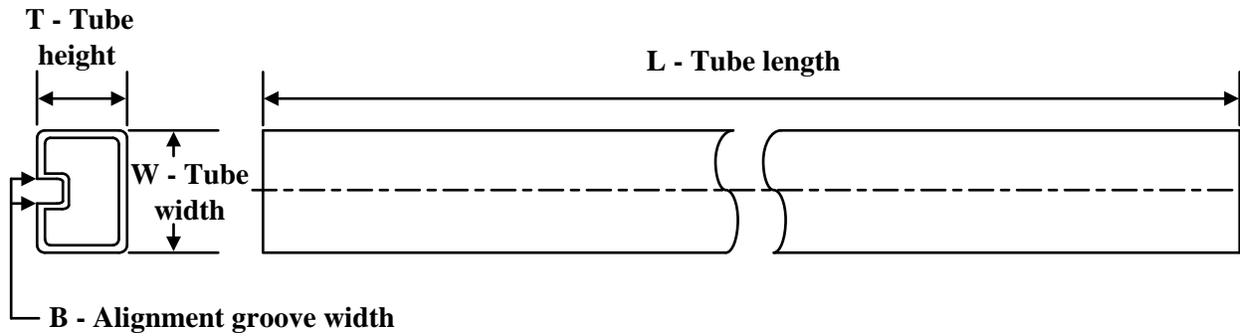
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75LVDS84DGG	DGG	TSSOP	48	40	530	11.89	3600	4.9
SN75LVDS84DGG.Z	DGG	TSSOP	48	40	530	11.89	3600	4.9
SN75LVDS84DGGG4	DGG	TSSOP	48	40	530	11.89	3600	4.9

DGG0048A

SMALL OUTLINE PACKAGE

8.3
7.9 TYP

A

PIN 1 ID
AREA

1

46X 0.5

48

12.6
12.4
NOTE 3

2X
11.5

24

25

B

6.2
6.0

48X 0.27
0.17

⊕ | 0.08Ⓜ | C | A | B

C

SEATING PLANE

⌒ | 0.1 | C

1.2
1.0

(0.15) TYP

SEE DETAIL A

0.25

GAGE PLANE

0° - 8°

0.75
0.50

0.15
0.05

DETAIL A
TYPICAL

4214859/B   11/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

TEXAS
INSTRUMENTS
www.ti.com

LAND PATTERN EXAMPLE
SCALE:6X

48X (1.5)

1

48X (0.3)

46X (0.5)

(R0.05)
TYP

SYMM

SYMM

48

24

25

(7.5)

SOLDER MASK
OPENING

METAL

0.05 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED
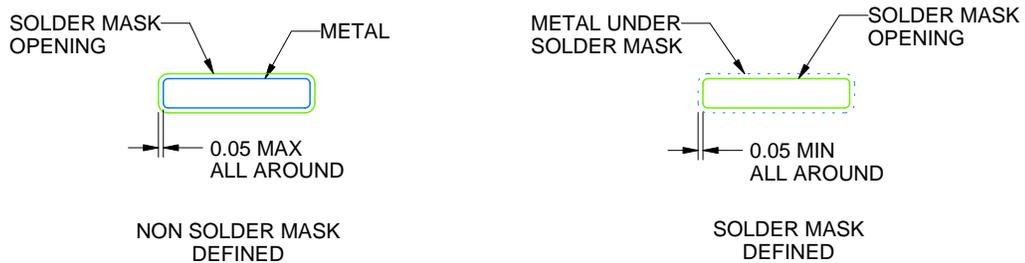
SOLDER MASK DETAILS

4214859/B   11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

48X (1.5)

1

48X (0.3)

46X (0.5)

(R0.05) TYP

SYMM

48

24

25

SYMM

(7.5)
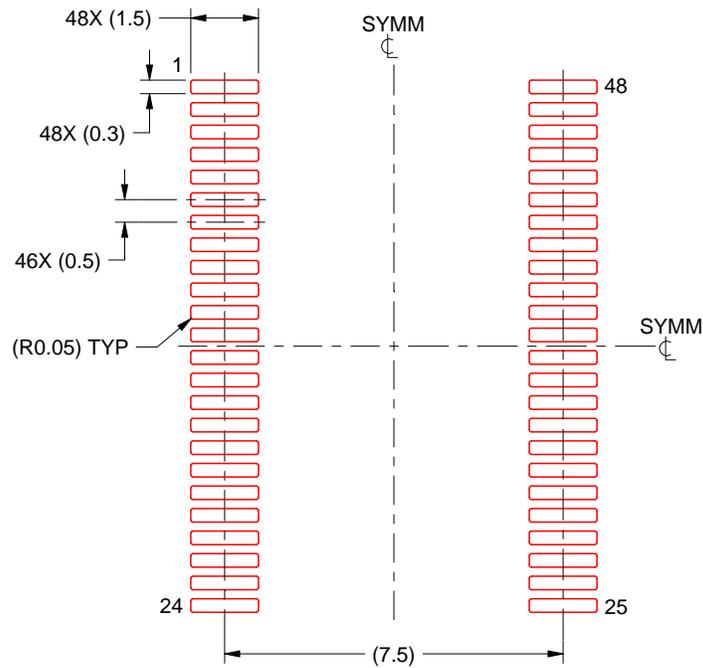
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4214859/B   11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

PINS **	48	56	64
DIM			
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97
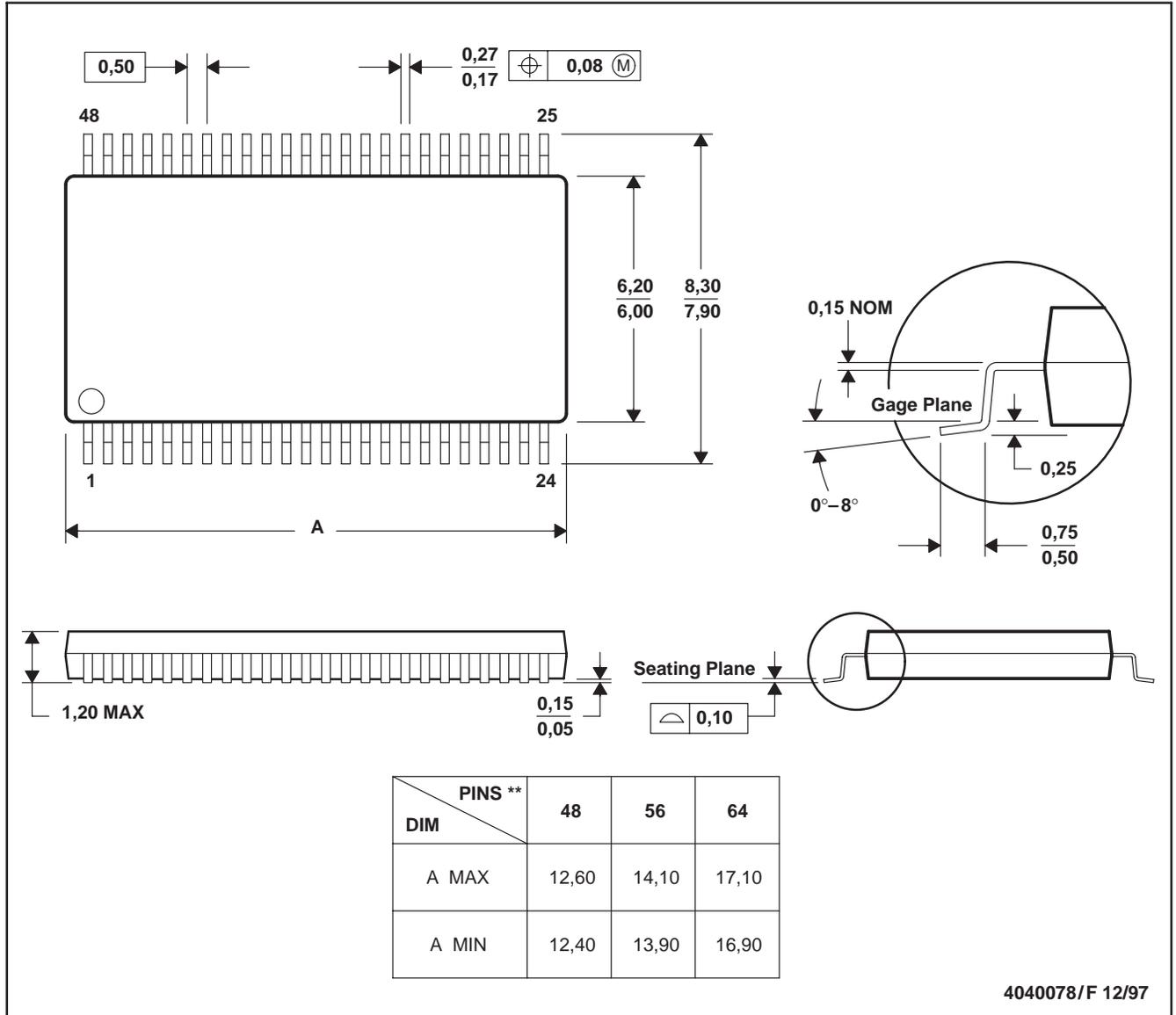
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

![Texas Instruments logo] **TEXAS INSTRUMENTS**

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