LYNX FAMILY

SM718

LynxSE 2D Multimedia Mobile Display Controller Datasheet

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Revision No.	Date	Note
0.1	March 2010	First release

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1. General Description

1.1 Overview

The SM718 is a PCI 2D multimedia mobile display controller device, packaged in a 320-pin BGA. Designed to complement needs for the embedded industry, it provides video and 2D capability. To help reduce system costs, it supports a wide variety of I/O, including analog RGB and digital LCD Panel interfaces, two Zoom Video interfaces, and Pulse Width Modulation (PWM). There are additional GPIO bits that can be used to interface to external devices as well.

The 2D engine includes a front-end color space conversion with 4:1 and 1:8 scaling support. The video engine supports two different video outputs (Dual Monitor), at 8-bit, 16-bit, or 32-bit per pixel and a 3-color hardware cursor per video output. The LCD panel video pipe supports a back-end YUV color space conversion with 4:1 and 1:212 scaling. A Zoom Video (ZV) port is also included to interface to external circuitry for MPEG decode or TV input.

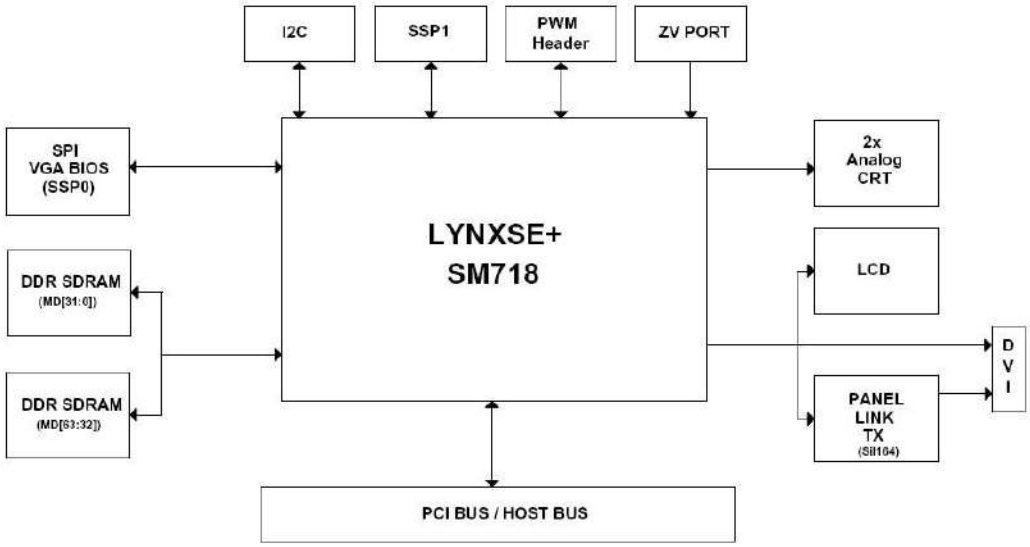


Figure 1: System Block Diagram

1.2 Pins

1.2.1 Pin Descriptions

The following table provides brief description of each BGA ball of the SM718. Signal names with # following are active “LOW” signals, whereas signal names without # following are active “HIGH” signals. Also the following abbreviations are used for Pin Type.

I -Input Signal

O -Output Signal

I/O -Input or Output Signal

Signal Name	Pin Number	Type	Pad	IOL (ma)	Description
Host/PCI Interface (76)					
ACK#	G20	I	CMOS 3.3V	TBD	CPU Bus Acknowledge / PCI Bus Grant.
BE[3:0]	A10, B10, C10, D10	I/O	CMOS 3.3V	TBD	CPU Byte Enable / SDRAM Data Mask.
BREQ#	F20	O	CMOS 3.3V	TBD	CPU Bus Request / PCI Bus Request.
BS#	A9	I	CMOS 3.3V	TBD	SH4 Cycle Start / XScale or NEC CPU Write Enable.
CA[11:1]	B13, C13, D13, A12, B12, C12, D12, A11, B11, C11, D11	I/O	CMOS 3.3V	TBD	CPU Address [11:1] / SDRAM MA.
CA[13:12]	D14, A13	I/O	CMOS 3.3V	TBD	CPU Address [13:12] / SDRAM BA / SDRAM MA.
CA[20:17]	C21, A20, B18, C16	I/O	CMOS 3.3V	TBD	CPU Address [20:17] / PCI C/BE#[3:0] / SDRAM MA.
CA14	E17	I/O	CMOS 3.3V	TBD	CPU Address 14 / PCI CLKRUN# / SDRAM BA / SDRAM MA.
CA15	G19	I/O	CMOS 3.3V	TBD	CPU Address 15 / PCI IDSEL / SDRAM BA / SDRAM MA.
CA16	D18	I/O	CMOS 3.3V	TBD	CPU Address 16 / PCI PAR / SDRAM BA / SDRAM MA.
CA21	A19	I/O	CMOS 3.3V	TBD	CPU Address 21 / PCI DEVSEL# / SDRAM MA.
CA22	C19	I/O	CMOS 3.3V	TBD	CPU Address 22 / PCI STOP# / SDRAM BA / SDRAM MA.
CA23	D19	I/O	CMOS 3.3V	TBD	CPU Address 23 / PCI TRDY# / SDRAM BA / SDRAM MA.
CA24	B19	I/O	CMOS 3.3V	TBD	CPU Address 24 / PCI IRDY# / SDRAM BA.
CA25	E18	I/O	CMOS 3.3V	TBD	CPU Address 25 / PCI FRAME#.
CD[31:0]	E21, J19, E20, J18, D21, H19, D20, H18, C20, G18, B21, F19, A21, F18, B20, E19, C18, A18, D17, B17, C17, A17, D16, B16, A16, D15, B15, C15, A15, C14, A14, B14	I/O	CMOS 3.3V	TBD	CPU Data Bus / PCI AD Bus / SDRAM Data Bus.
CPURD#	C9	I/O	CMOS 3.3V	TBD	XScale or NEC Read Enable.

HCAS#	B8	O	CMOS 3.3V	TBD	SDRAM Column Address select.
HCKE	D8	I/O	CMOS 3.3V	TBD	SDRAM Clock Enable.
HCLK	F21	I/O	CMOS 3.3V	TBD	CPU clock / PCI clock.
HCS#	E14	I	CMOS 3.3V	TBD	SM718 chip select.
HRAS#	C8	O	CMOS 3.3V	TBD	SDRAM Row Address select.
HRDY	A7	O	CMOS 3.3V	TBD	CPU Ready. This signal must be externally pulled-up for SH4. For all other CPUs, this signal must be pulled up.
HWE#	B9	I/O	CMOS 3.3V	TBD	SH4 Write Enable / SDRAM Write Enable.
INTR	K19	O	CMOS 3.3V	TBD	CPU Interrupt / PCI Interrupt.
MCS#[1:0]	D9, A8	O	CMOS 3.3V	TBD	SDRAM Chip Select.
RST#	G21	I	CMOS 3.3V	TBD	SM718 reset.
Power Down Interface (1)					
CLKOFF	F17	I	CMOS 3.3V	TBD	Host Clock Off
Clock Interface (11)					
PLL_AGND	M20, J20	I	0V	--	PLL analog ground
PLL_DGND	K20, L20	I	0V	--	PLL digital ground
PLLPWR_A	H21	I	3.3V	--	PLLA analog power
PLLPWR_DA	J21	I	3.3V	--	PLLA digital power
PLLPWR_BC	N21	I	3.3V	--	PLLB and PLLC analog power
PLLPWR_DBC	M21	I	3.3V	--	PLLB and PLLC digital power
TESTCLK	H20	I	CMOS 3.3V	TBD	For testing purpose
XTALIN	L21	I	CMOS 3.3V	TBD	14.31818MHz crystal input connection
XTALOUT	K21	O	CMOS 3.3V	TBD	14.31818MHz crystal output connection
Test Interface (3)					
TEST[2:0]	Y15, W15, V15	I	CMOS 3.3V	TBD	Test mode selection
Memory Interface (104)					
BA[1:0]	H3, H4	O	CMOS 2.5V	TBD	DDR bank address
CAS#	H2	O	CMOS 2.5V	TBD	DDR column address strobe
CKE	J3	O	CMOS 2.5V	TBD	DDR clock enable
CS#	J4	O	CMOS 2.5V	TBD	DDR chip select
DQM[7:0]	T2, P1, F2, C3, V5, A3, Y1, A6	O	CMOS 2.5V	TBD	DDR data mask
DQS[7:0]	U3, R1, F1, D3, W5, A2, AA1, A5	O	CMOS 2.5V	TBD	DDR data strobe
MA[12:0]	N4, M2, M3, M4, L1, L2, L3, L4, L5, K1, K2, K3, K4	O	CMOS 2.5V	TBD	DDR address bus. MA[12:0] also function as strap pins.
MD[31:0]	AA6, Y6, AA5, Y5, AA4, Y4, W4, V4, B1, A1, B2, B3, C4, B4, A4, B5, AA3, Y3, AA2, Y2, W1, W2, W3, V1, D5, C5, D6, C6, B6, D7, C7, B7	I/O	CMOS 2.5V	TBD	DDR data bus [31:0]

MD[63:32]	V2, V3, U1, U2, U4, U5, T3, T4, R2, R3, R4, P2, P3, P4, N2, N3, G1, G2, G3, G4, E1, E2, F3, F4, D1, D2, C1, C2, E3, E4, D4, E5	I/O	CMOS 2.5V	TBD	DDR data bus [63:32]
MVREF[1:0]	T1, J1	I	1.25V	--	DDR voltage reference
RAS#	H1	O	CMOS 2.5V	TBD	DDR row address strobe
SCK+, SCK-	M1, N1	O	CMOS 2.5V	TBD	DDR differential clock
WE#	J2	O	CMOS 2.5V	TBD	DDR write enable
Flat Panel Interface (31)					
BIAS	V13	O	CMOS 3.3V	TBD	Flat panel voltage bias enable
FP[23:0]	W12, V12, AA11, Y11, W11, V11, AA10, Y10, W10, V10, AA9, Y9, W9, V9, AA8, Y8, W8, V8, AA7, Y7, W7, V7, W6, V6	O	CMOS 3.3V	TBD	Flat panel data bus [23:0]
FP_DISP	V14	O	CMOS 3.3V	TBD	Flat panel display enable
FP_HSYNC	Y13	O	CMOS 3.3V	TBD	Flat panel horizontal sync
FP_VSYNC	Y12	O	CMOS 3.3V	TBD	Flat panel vertical sync
FPCLK	AA12	O	CMOS 3.3V	TBD	Flat panel pixel clock
FPEN	W13	O	CMOS 3.3V	TBD	Flat panel enable
VDEN	W14	O	CMOS 3.3V	TBD	Flat panel VDD enable
CRT0 Interface (6)					
B0	AA14	O	Analog	--	CRT0 blue output
CRT_HSYNC	Y19	O	CMOS 3.3V	TBD	CRT0 horizontal sync
CRT_VSYNC	AA19	O	CMOS 3.3V	TBD	CRT0 vertical sync
G0	AA15	O	Analog	--	CRT0 green output
IREF0	AA18	I	Analog	--	CRT0 IREF output
R0	AA16	O	Analog	--	CRT0 red output
CRT1 Interface (4)					
B1	AA21	O	Analog	--	CRT1 blue output
G1	Y21	O	Analog	--	CRT1 green output
IREF1	U21	I	Analog	--	CRT1 IREF output
R1	W21	O	Analog	--	CRT1 red output
Video Port Interface (3)					
VP_CLK	T21	I	CMOS 3.3V	TBD	Video port clock
VP_HREF	P21	I	CMOS 3.3V	TBD	Video port horizontal reference
VP_VSYNC	R21	I	CMOS 3.3V	TBD	Video port vertical sync
GPIO Interface (32)					
GPIO[7:0]	N20, N19, N18, M19, M18, L19, L18, K18	I/O	CMOS 3.3V	TBD	GPIO[7:0] / Video Port D[7:0]

GPIO[15:8]	T19, T18, R20, R19, R18, P20, P19, P18	I/O	CMOS 3.3V	TBD	GPIO[15:8] / Video Port D[15:8] / FD[31:24]
GPIO16	T20	I/O	CMOS 3.3V	TBD	GPIO16 / CLKIN / FDSCLK1
GPIO[19:17]	U19, U18, U17	I/O	CMOS 3.3V	TBD	GPIO[19:17] / PWM[2:0] / GPIO[19:17] also function as strap pins.
GPIO20	U20	I/O	CMOS 3.3V	TBD	GPIO20 / SSP0 TXD / GPIO20 also functions as a strap pin.
GPIO21	V17	I/O	CMOS 3.3V	TBD	GPIO21 / SSP0 RXD / GPIO21 also functions as a strap pin.
GPIO22	V18	I/O	CMOS 3.3V	TBD	GPIO22 / SSP0 SFOUT
GPIO23	V19	I/O	CMOS 3.3V	TBD	GPIO23 / SSP0 SFIN / GPIO23 also functions as a strap pin.
GPIO24	V20	I/O	CMOS 3.3V	TBD	GPIO24 / SSP0 CLK
GPIO25	W17	I/O	CMOS 3.3V	TBD	GPIO25 / SSP1 TXD / FD32
GPIO26	W18	I/O	CMOS 3.3V	TBD	GPIO26 / SSP1 RXD / FD33
GPIO27	W19	I/O	CMOS 3.3V	TBD	GPIO27 / SSP1 SFOUT / FD34
GPIO28	Y17	I/O	CMOS 3.3V	TBD	GPIO28 / SSP1 SFIN / FD35
GPIO29	Y18	I/O	CMOS 3.3V	TBD	GPIO29 / SSP1 CLK
GPIO30	V16	I/O	CMOS 3.3V	TBD	GPIO30 / I2C SCL
GPIO31	W16	I/O	CMOS 3.3V	TBD	GPIO31 / I2C SDA
Power and Ground (49)					
AVDD0	AA13	I	1.2V	--	DAC0 Analog Power,1.2V
AVDD1	AA20	I	1.2V	--	DAC1 Analog Power,1.2V
AVDD2	AA17	I	3.3V	--	DAC0 Analog Power,3.3V
AVDD3	V21	I	3.3V	--	DAC1 Analog Power,3.3V
AVSS	W20, Y16, Y20, Y14	I	0V	--	DAC Analog Ground
VSS	U14, U10, U6, T17, P5, M17, K5, H17, G5, E16, E11, E7	I	0V	--	Core Ground
GVDD	N17, R17, U16	I	3.3V	--	GPIO Power
HVDD	E8, E10, E15, G17	I	3.3V	--	Host Power
MVDD	F5, L17, M5, U8	I	2.5V	--	DDR Core Power
MVDD2	E9, E13, H5, R5, U11, U15	I	2.5V	--	DDR I/O Power
PVDD	T5, U9, U13	I	3.3V	--	LCD Panel I/O Power
VDD	E6, E12, J5, J17, N5, P17, U7, U12	I	1.2V	--	Core Power
XTALPWR	K17	I	3.3V	--	Crystal Power

Table 1: Pin Description

1.2.2 Package Information

SM718 Pin Diagram for 320 BGA Package

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
A	MD22	DQS2	DQM2	MD17	DQS0	DQM0	HRDY	MCS0#	BS#	BE3	CA4	CA8	CA12	CD1	CD3	CD7	CD10	CD14	CA21	CA19	CD19
B	MD23	MD21	MD20	MD18	MD16	MD3	MD0	HCAS#	HWE#	BE2	CA3	CA7	CA11	CD0	CD5	CD8	CD12	CA18	CA24	CD17	CD21
C	MD37	MD36	DQM4	MD19	MD6	MD4	MD1	HRAS#	CPURD#	BE1	CA2	CA6	CA10	CD2	CD4	CA17	CD11	CD15	CA22	CD23	CA20
D	MD39	MD38	DQS4	MD33	MD7	MD5	MD2	HCKE	MCS1#	BE0	CA1	CA5	CA9	CA13	CD6	CD9	CD13	CA16	CA23	CD25	CD27
E	MD43	MD42	MD35	MD34	MD32	VDD	VSS	HVDD	MVDD2	HVDD	VSS	VDD	MVDD2	HCS#	HVDD	VSS	CA14	CA25	CD16	CD29	CD31
F	DQS5	DQM5	MD41	MD40	MVDD												CLKOFF	CD18	CD20	BREQ#	HCLK
G	MD47	MD46	MD45	MD44	VSS												HVDD	CD22	CA15	ACK#	RST#
H	RAS#	CAS#	BA1	BA0	MVDD2												VSS	CD24	CD26	TESTCLK	PLLPWR_A
J	MVREF0	WE#	CKE	CS#	VDD						TOP VIEW						VDD	CD28	CD30	PLL_AGND	PLLPWR_DA
K	MA3	MA2	MA1	MA0	VSS						320-PIN						XTALPWR	GPIO0	INTR	PLL_DGND	XTALOUT
L	MA8	MA7	MA6	MA5	MA4						19X19 mm						MVDD	GPIO1	GPIO2	PLL_DGND	XTALIN
M	SCK+	MA11	MA10	MA9	MVDD												VSS	GPIO3	GPIO4	PLL_AGND	PLLPWR_DBC
N	SCK-	MD49	MD48	MA12	VDD												GVDD	GPIO5	GPIO6	GPIO7	PLLPWR_BC
P	DQM6	MD52	MD51	MD50	VSS												VDD	GPIO8	GPIO9	GPIO10	VP_HREF
R	DQS6	MD55	MD54	MD53	MVDD2												GVDD	GPIO11	GPIO12	GPIO13	VP_VSYNC
T	MVREF1	DQM7	MD57	MD56	PVDD												VSS	GPIO14	GPIO15	GPIO16	VP_CLK
U	MD61	MD60	DQS7	MD59	MD58	VSS	VDD	MVDD	PVDD	VSS	MVDD2	VDD	PVDD	VSS	MVDD2	GVDD	GPIO17	GPIO18	GPIO19	GPIO20	IREF1
V	MD8	MD63	MD62	MD24	DQM3	FD0	FD2	FD6	FD10	FD14	FD18	FD22	BIAS	FP_DISP	TEST0	GPIO30	GPIO21	GPIO22	GPIO23	GPIO24	AVDD3
W	MD11	MD10	MD9	MD25	DQS3	FD1	FD3	FD7	FD11	FD15	FD19	FD23	FPEN	VDEN	TEST1	GPIO31	GPIO25	GPIO26	GPIO27	AVSS	R1
Y	DQM1	MD12	MD14	MD26	MD28	MD30	FD4	FD8	FD12	FD16	FD20	FP_VSYNC	FP_HSYNC	AVSS	TEST2	AVSS	GPIO28	GPIO29	CRT_HSYNC	AVSS	G1
AA	DQS1	MD13	MD15	MD27	MD29	MD31	FD5	FD9	FD13	FD17	FD21	FPCLK	AVDD0	B0	G0	R0	AVDD2	IREF0	CRT_VSYNC	AVDD1	B1

1.3 Internal Block Description

1.3.1 Host Bus

The SM718 supports two mutually exclusive modes of interfacing with the host CPU. The first option is to configure the SM718 as a memory-mapped device located off the host system's CPU to memory interface. In this case, the SM718 supports a 32-bit interface for commands/status and a 32-bit or 16-bit interface for data transfer. With a typical Marvell PXA250/270 processor interface, this allows for a peak bandwidth of 400 MB/s.

The second configuration option is to use the SM718 as a PCI device on a PCI bus. In this mode, the SM718 supports PCI-1X and 2X for a maximum bus throughput of 250 MB/s.

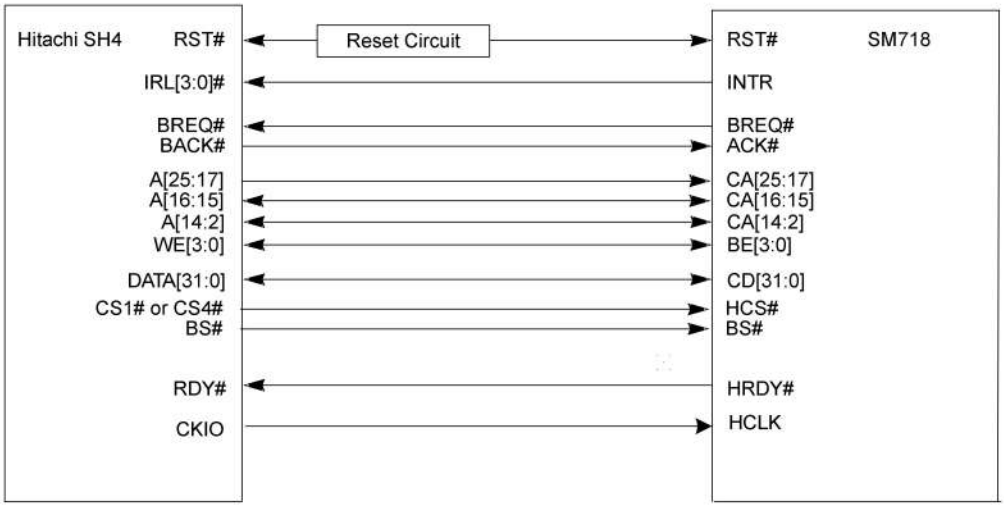
The following sections summarize the interface connections between the SM718 and a host CPU or PCI bus. See the SM718 Host Interface Design Guide for more information on particular CPU type.

Hitachi SH4

When the SM718 is interfaced to the Hitachi SH4 host bus, it can run in host interface's salve mode that acts as Byte Control SRAM mode.

Figure 1-5 shows a typical system-level hookup between the SM718 device and the Hitachi SH4.

Figure 1-5: Hitachi SH4 to the SM718 Bus Interface



Design Notes:

1) In the SM718 Slave mode, the SH4 CPU drives RD/WR# (WE#) for the SM718 and SDRAM. In Bus Master mode, the SM718 drives this line.

2) The SH4 supports up to 64 MB with each chip select. Depending on the memory size and configuration, address [14:12] can be used for the bank address or the memory address. The design shown in Figure 1-5 supports two groups of 64MB memory.

3) The SM718 works as a byte-enable SRAM with the SH4. The SH4 supports byte-enable SRAM only with CS1 or CS4.

4) The SH4 can be programmed for 4-level or 16-level interrupts. The SM718 interrupt output can be connected to one of the 4-level interrupt inputs, depending on the system and software designs. To connect to a 16-level interrupt, an external circuit is required.

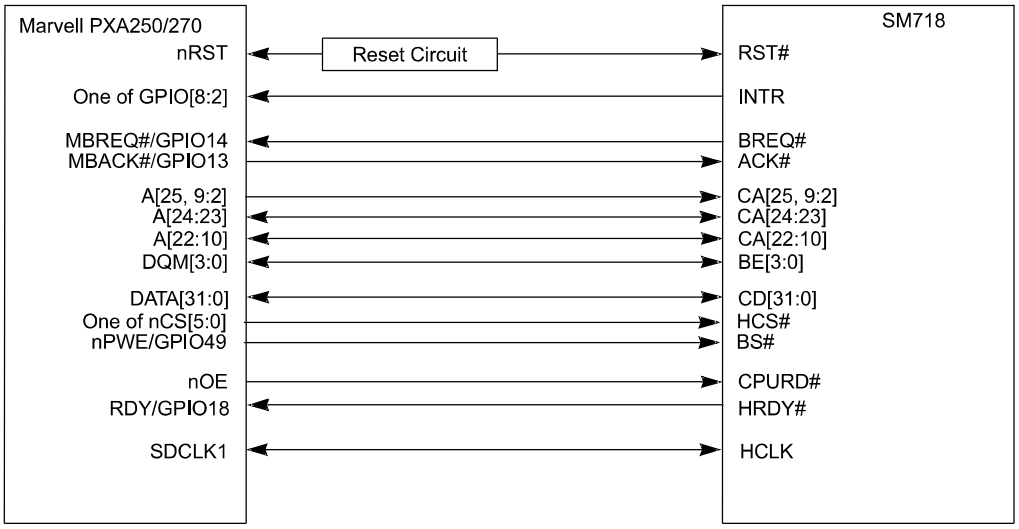
For a discussion of clock buffering, see the SM718 Host Interface Design Guide.

Marvell PXA250/270

When the SM718 is interfaced to the PXA250/270 host bus, it can run in host interface's slave mode as a SRAM-like Variable Latency I/O mode.

Figure 1-6 shows a typical system-level hookup between the SM718 device and the PXA250 or PXA270 processor.

Figure 1-6: Marvell PXA250/270 to the SM718 Bus Interface



Design Notes:

1) The PXA250/270 processor only has one 3-stateable SDRAM CS line. Thus the SM718 can support only one group of SDRAMs in Bus Master mode.

2) According to the PXA250/270 specification, SDRAM must use SDCLK2 or SDCLK1. 3) The variable latency I/O must use either SDCLK0 (synchronous) or no clock. Because the SM718 has to drive the SDRAM clock on the same line, SDCLK1 is used.

4) According to the PXA250/270 specification, the variable latency I/O device can use one of nCS[5:0] as the chip select.

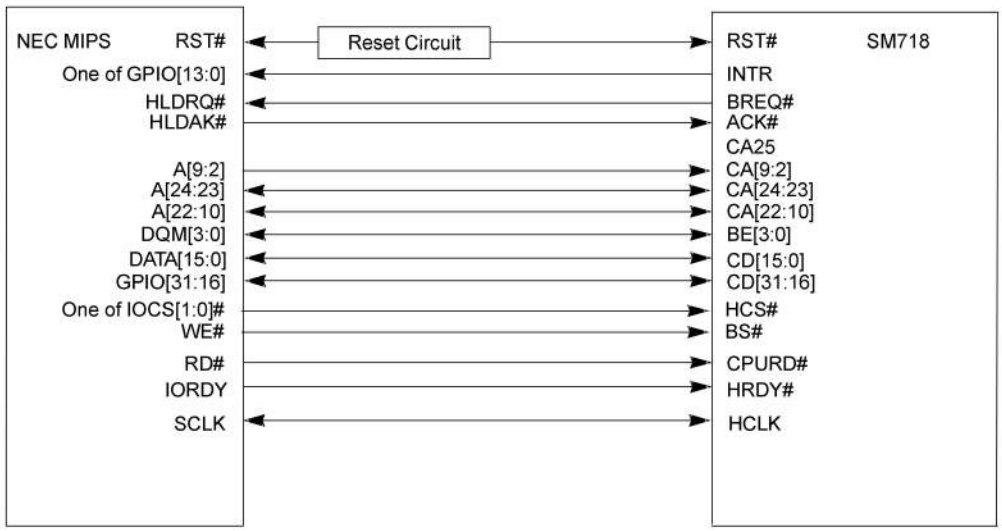
5) The PXA250/270 processor does have a dedicated interrupt input. Use one of GPIO[8:2] and configure the selection as an interrupt via software.

NEC VR4122/4131 MIPS

When the SM718 is interfaced to the NEC VR4122/31 MIPS host bus, it can run in host interface's slave mode as a LCD Controller mode.

Figure 1-7 shows a typical system-level hookup between the SM718 device and the NEC VR4122/31 MIPS processor.

Figure 1-7: NEC MIPS to the SM718 Bus Interface

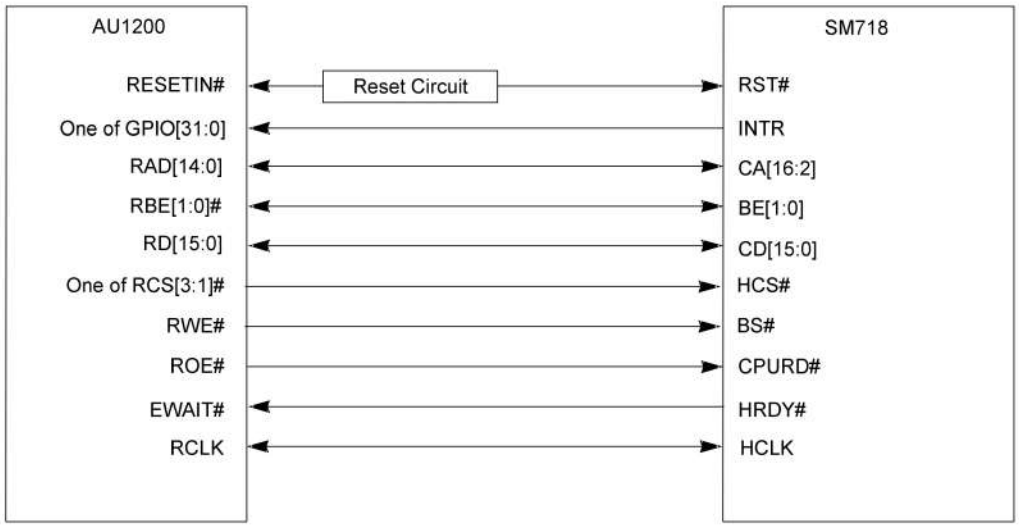


AMD AU1200

When the SM718 is interfaced to the AMD AU1200 16-bit host bus, it can run in host interface's slave mode as Byte Control SRAM mode.

Figure 1-7 shows a typical system-level hookup between the SM718 device and the AMD AU1200 processor.

Figure 1-7: AMD AU1200 to the SM718 Bus Interface



Other 16-bit CPU Host Interface -- TBD

1.3.2 PCI Bus

SM718 provides a glue-less interface to the PCI system bus. The device is fully compliant with PCI. To maximize performance, the Interface Unit also supports burst write and burst read. The Interface Unit decodes I/O read, I/O write, memory read, memory write, memory mapped access, 2D Drawing Engine access, VAG access, and others.

SM718 has an internal HIF (Host Interface) bus, which is designed to transfer data between the PCI Interface Unit and other functional blocks. The PCI Interface Unit controls the HIF bus protocol to effectively deliver I/O and memory cycles to each function block.

Interfacing to PCI Device

This section provides information for interfacing the SM718 to PCI complaint devices. It covers these topics:

- Hardware Connections
- Configuration Header
- Power Supply Considerations
- Board Layout Considerations

Hardware Connections

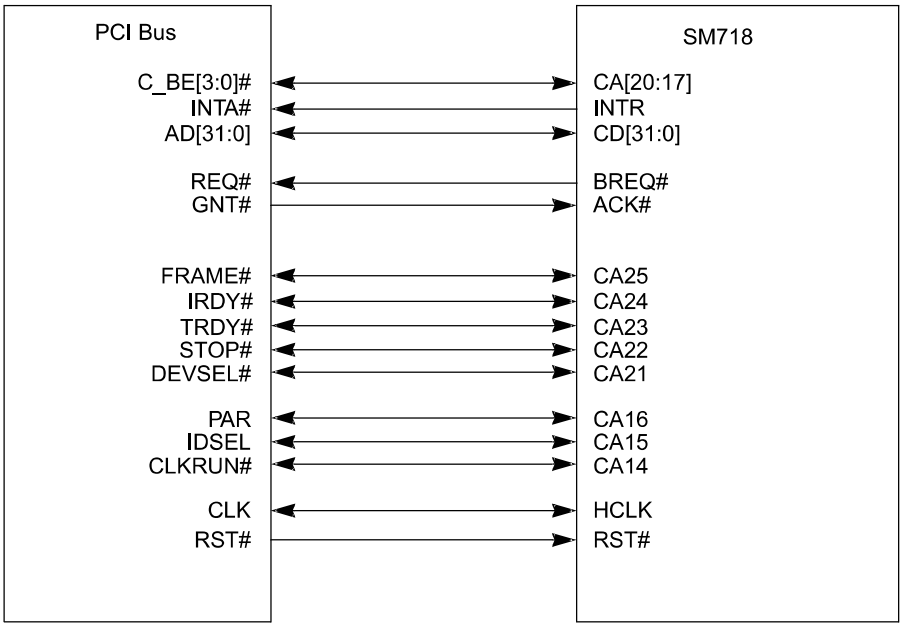


Figure 2: SM718 Connections to PCI Device

Configuration Header

Figure 4 shows the Configuration Space Header.

Address (hex)	Field Definitions			
	31:24	23:16	15:8	7:0
00	Device ID		Vendor ID	
04	Status		Command	
08	Class Code			Revision ID
0C	BIST	Header Type	Master Latency Timer	Cache Line Size
10	Base Address Registers			
14				
18				
1C				
20				
24				
28	Cardbus CIS Pointer			
2C	Subsystem ID		Subsystem Vendor ID	
30	Expansion ROM Base Address			
34	Reserved			Capabilities Pointer
38	Reserved			
3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line

Figure 3: Type 00 PCI Configuration Header Values

Power Supply Considerations

Figure 5 shows the power supply connections to the SM718 in a PCI design.

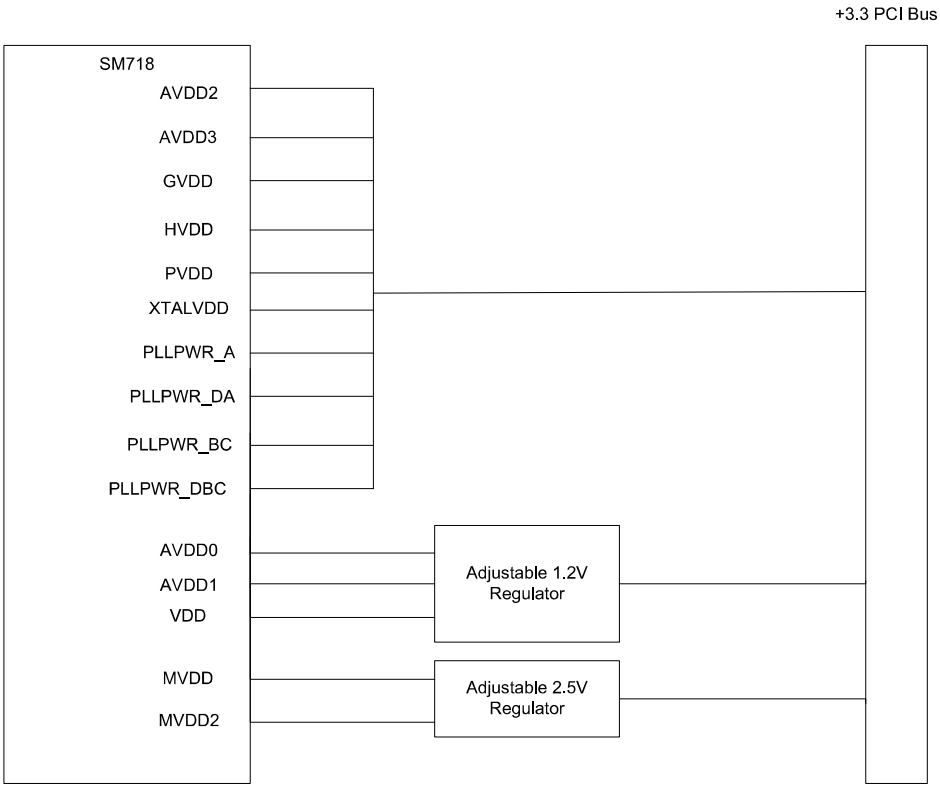


Figure 4: Power Supply Connections for SM718 in PCI Design

Board Layout Considerations

PC Board requirements are as follows:

- The unloaded characteristic impedance of shared PCI signal traces must be controlled to be in the range of 60 to 100 ohms.
- Trace velocity should be between 150 and 190 ps/inch.
- Six layers are required. The rest area must be covered with ground on both sides, top and bottom.

PCI Bus Interface requirements are as follows:

- Set VCC and GND plane. A split power planes is permitted; for this board, 3.3V is the main plane.
- Signal traces must remain entirely over either the 3.3V plane.
- Signals that cross from one domain to the other should be routed on the opposite side of the board.
- If some signal traces are routed on layer 3 or 4, they cannot be overlaid.
- The maximum trace length for all 32-bit interfaces is 1.5 inches.
- Traces must be at least 7 mils wide.
- The length of the PCI clock trace should be 2.5 inches +/- 0.1 inches.

1.3.3 *Display Memory Interface*

The SM718 supports embedded DDR memory or external DDR memory setup. It includes a local memory interface to drive an external local memory of 8 to 64 Mbytes in size. This chapter provides basic information for designing an embedded local memory or an external local memory setup. For detailed timing information, consult the documentation provided by the memory device manufacture.

This chapter contains the following sections:

- Memory Architectures
- Local Memory Interface Signals
- Configuring the Local Memory Interface

Memory Architectures

SM718 supports 16Mbytes of embedded DDR memory that clocked up to 166MHz. The device's embedded memory supports a 32-bit DDR memory interface, so it provides up to 1.3GB/s of memory bandwidth.

SM718 also supports an independent 64-bit external DDR memory interface that supports up to 64Mbytes of external DDR memory. Therefore, with a 64-bit external DDR memory setup, it provides up to 2.6GB/s of memory bandwidth.

Figure 6 shows the three possible memory setups. (A) 32-bit embedded DDR memory, (B) 32-bit external DDR memory, and (C) 64-bit external DDR memory setups.

Figure 5: Memory Setups

Local Memory Interface Signals

Figure 7 shows the connection diagram for a typical DDR memory setup organized as two pieces of 16M x 16 DDR SDRAMs.

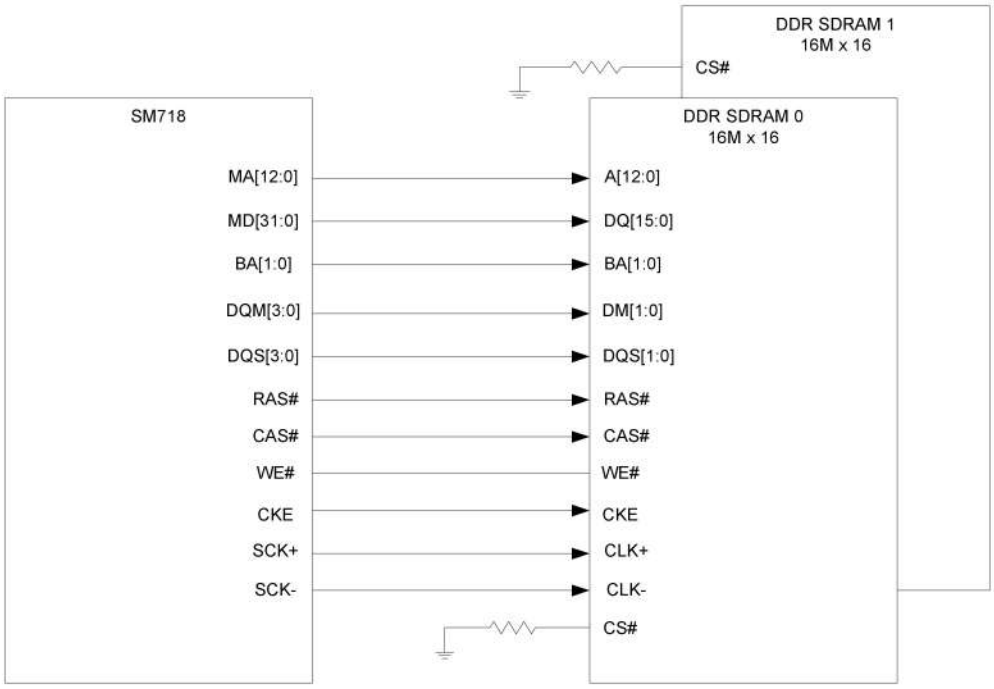


Figure 6: Typical DDR Memory Setup

Configuring the Local Memory Interface

The configuration of the local memory interface can be set through power-on strap pins or using Miscellaneous Control Register MMIO_base + 0x000004. This section discusses the bits and strap-pins that control parameters for the local memory interface.

Memory Size

The SM718 must be configured with the size of local memory. Bits [13:12] of the Miscellaneous Control Register set the size of the local memory as shown in Table 3. The size of the local memory can also be determined by the power-on configuration values of Memory Address pins MA[6:5] as shown in Table 3; however, writing a value to the Miscellaneous Control Register will override the power-on configuration setting.

Miscellaneous Control Register Bit or Memory Address Pin at Power-On		Memory Size in Mbytes
Bit 13 or MA6	Bit 12 or MA5	
0	0	16MB
0	1	32MB
1	0	64MB
1	1	8MB

Table 2: Configuring the Size of Local Memory

Memory Device Architecture

The SM718 must be configured for the physical architecture of the memory devices used in the local memory, including the column size and memory bus width.

Bit [15:14] of the Miscellaneous Control Register set the column size of the local memory as shown in Table 4. The column size can also be determined by power-on configuration values of Memory Address pins MA[8:7] as shown in Table 4; however, writing a value to the Miscellaneous Control Register will override the power-on configuration setting.

Bit 1 of the Miscellaneous Control Register set the width of the memory interface data bus as shown in Table 5. The memory interface data bus width can also be determined by power-on configuration values of Memory Address pins MA1 as shown in Table 5; however, writing a value to the Miscellaneous Control Register will override the power-on configuration setting.

Miscellaneous Control Register Bit or Memory Address Pin at Power-On		Column Size
Bit 15 or MA8	Bit 14 or MA7	
0	0	256 words
0	1	512 words
1	X	1024 words

Table 3: Configuring the Column Size of Local Memory

Miscellaneous Control Register Bit or Memory Address Pin at Power-On	Memory Bus Width
Bit 1 or MA1	
0	32-bit
1	64-bit

Table 4: Configuring the Memory Bus Width

1.3.4 Zoom Video Port

The SM718 includes two Zoom Video (ZV) ports to allow the use of external MPEG decoders for DVD playback, external TV tuners, and other sources. This interface supports the YUV 4:2:2, YUV 4:2:2 with byte swap and RGB 5:6:5 data formats. It also supports ITU656-8 bit.

The standard ZV port uses an 8-bit interface at 72 MHz. However, if desired, an extra 8 bits in the GPIO interface may be used to interface to ICs that only support a 16-bit ZV interface or uses the extra 8 bits for the second ZV port input. The pins used for the ZV interface are designated GPIO pins. See the SM718 MMCC Design Guide for more information.

Note that the ZV input to video display path is as follows: ZV port → capture → frame buffer → video scalar → display. The capture portion supports a 1:1 or 2:1 reducing. In addition, the video scalar allows arbitrary scaling from 1:1 to 4:1 on shrinking and 1:1 to 1:212 on expansion; however, the quality of the expansion is degraded beyond 1:8. This will easily allow 4:3 and 16:9 conversion, full screen PAL, and picture-in-picture.

See Chapter 8 for more information about the ZV Port registers. See the SM718 MMCC Design Guide for more information about interfacing the SM718 to external sources.

1.3.5 2D Engine

The SM718 provides industry-leading 2D acceleration through the combination of an optimized 128-bit 2D drawing engine and a high bandwidth link to local frame memory. The 2D engine also contains a command interpreter (an enhanced DMA engine) that can intelligently fetch operands out of the frame buffer at up to 600MB/s. The command interpreter can conditionally branch to another location in memory, wait for status from another module, etc. as it fetches and interprets commands.

The 2D drawing engine also contains a color space conversion unit. The color space conversion unit allows for direct translation from many YUV formats into RGB. The 2D drawing engine also contains a bi-linear scalar, which supports 4:1 shrink and 1:216 stretch.

As noted previously, the SM718 supports embedded memory in 32-bit modes. With 32 bits of DDR running at 166 MHz, the SM718's DMA engine has 1.2GB/s of memory bandwidth to use for fetching 2D operands and data. This high memory bandwidth allows the 2D engine to run at full speed without costly waits or pipeline stalls from the frame buffer.

The 2D drawing engine understands the following commands:

1. BitBlt (from system/local memory to system/local memory) with 256 raster operations. Pattern is selectable between 8x8 monochrome pattern, 8x8 color pattern or another surface located in either system or local memory.
2. Transparent BitBlt with the same capabilities as the previous command, but only the source or destination can be transparent (either ColorKey or ChromaKey).
3. Alpha BitBlt with a constant alpha value.
4. Rotation BitBlt for any block size. This feature allows high speeds conversion between landscape and portrait display without the need for special software drivers. (90°, 180°, 270°.)
5. YUV to 16-bit/32-bit RGB Blt conversion with 1:216 stretch or 4:1 shrink to provide high speeds video in common format.
6. Auto-wrapping for smooth scrolling support for navigational or other data.
7. Support for tiled memory to optimize performance for 2D operations and rotation.

As noted previously, the 2D Drawing Engine has a 112 MHz clock and a 128-bit wide memory access path.
With 8-bpp colors, the 2D engine can process 2400M pixels/s, and with 16-bpp the 2D engine can process 1200M pixels/s.

See Chapter 4 for more information about the 2D Drawing Engine.

1.3.6 *Video Display Layers*

As shown in Figure 9, the SM718 supports seven layers of display frames (2x hardware cursor, primary graphics, video, video alpha, alpha, and secondary graphics). (See Chapter 5 for more information about the Display Controller.)

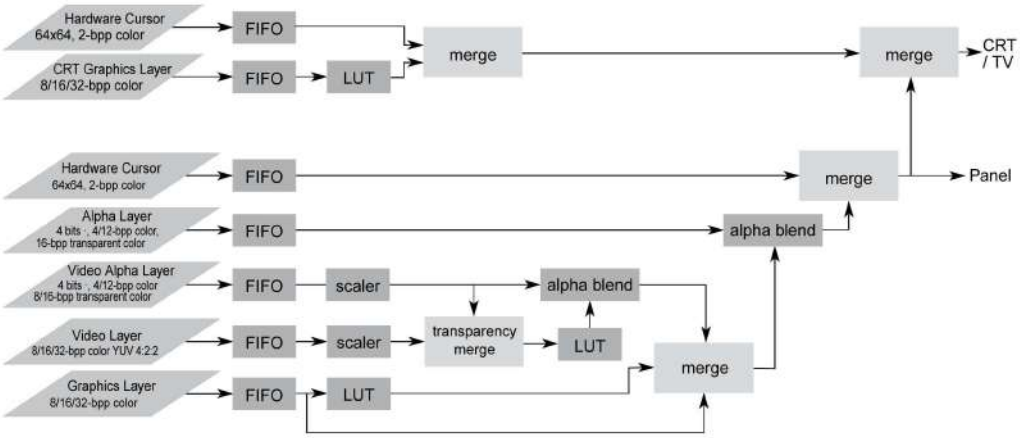


Figure 7: Video Layers and Data Processing

Layer #7: Secondary Hardware Cursor

To display a cursor on the analog output for multi-monitor function.

- One single 64x64 pixel cursor 2-bpp color [1:0] (00 = transparent, 01 = color0, 10 = color1, 11 = color2), is mapped into a 32-bit RGB 8:8:8 color map.

Layer #6: Secondary Graphics

To display text or drawings on the analog output (CRT) for multi-monitor function.

- 8-bpp (index into RGB 8:8:8 lookup table).
- 16-bpp RGB 5:6:5.
- 32-bpp RGB 8:8:8.

Layer #5: Primary Hardware Cursor

To display a cursor on the digital output.

- One single 64x64 pixel cursor 2-bpp color [1:0] (00 = transparent, 01 = color0, 10 = color1, 11 = color2), is mapped into a 32-bit RGB 8:8:8 color map.

Layer #4: Alpha

To alpha-blend and/or color-key an image on top of the Primary Graphics and Video layer outputs.

- 16-bpp (4-bit alpha, 4-bit Red, 4-bit Green, 4-bit Blue) or RGB 5:6:5.
- 16-bit transparency register (with 16-bit RGB 5:6:5 mode); if a color matches the register's value it is transparent.
- 4-bit planar blending register (in 16-bit RGB 5:6:5 mode only) to blend all pixels on the plane (that are non-transparent) to one planar alpha value.

Layer #3: Video Alpha

To alpha-blend and/or color-key an image on top of the Video layer output.

- Supports bi-linear scale up or down.
- 8-bpp (4-bit alpha, 4-bit index color), or 8-bit index (index into RGB 8:8:8 lookup table).
- 16-bpp (4-bit alpha, 4-bit Red, 4-bit Green, 4-bit Blue) or RGB 5:6:5.
- 8-bit transparency register (with 8-bit index), or 16-bit transparency register (with 16-bit RGB 5:6:5 mode); if a color matches the register's value it is transparent.
- 4-bit planar blending register (in 16-bit RGB 5:6:5 mode only) to blend all pixels on the plane (that are non-transparent) to one planar alpha value.

Layer #2: Video

To overlay video image or graphics on top of Primary Graphics layer.

- Supports bi-linear scale up or down.
- 8-bit index (index into RGB 8:8:8 lookup table).
- 16-bpp RGB 5:6:5 or YUV 4:2:2.

Layer #1: Primary Graphics

To display text or drawings on the primary output (LCD panel).

- Support smooth scrolling and auto-wrapping.
- 8-bit index (index into RGB 8:8:8 lookup table).
- 16-bpp RGB 5:6:5.
- 32-bpp RGB 8:8:8.
- 8-bit (with 8-bit index), 16-bit (with 16-bit RGB 5:6:5), or 32-bit (with 32-bit RGB 8:8:8) color key register. If the color value matches the register's value, the color is transparent and the pixel from the Primary Video layer is shown instead.

Terminology

Some definitions of terms used above:

bpp – bits per pixel.

RGB – Red, Green, Blue.

RGB 5:6:5 – 16-bit color mode, where Red has 5 bits, Green has 6 bits, and Blue has 5 bits.

RGB 8:8:8 – 32-bit color mode, where Red has 8 bits, Green has 8 bits, and Blue has 8 bits. The upper 8 bits are unused.

Alpha – A means of blending two layers together. The fundamental equation is (α * c) + (1 - α) * (original pixel), where c is the 4-bit color that points into the 18-bit lookup table. In practical terms, 4-bit alpha blending means that for two given display layers, one layer is dominant (e.g. video layer) and the other layer (e.g. video alpha) has 16 levels of transparency from 100% to 0% that may be applied to the colors in that layer.

LUT – Lookup table; a means to map an 8-bit color index into a 24-bit color space, thus a smaller number of simultaneous colors (8-bit) but with a wide range of colors (24-bit) to choose from.

Display Resolution

The SM718 supports display resolutions up to 1920 x 1440. 16:9 formats in this range (e.g. 800 x 480, 1024 x 600, 1280 x 768, and etc.) are supported. Note that there are trade-offs between the maximum resolution, the number of active video layers, and the frame memory choice.

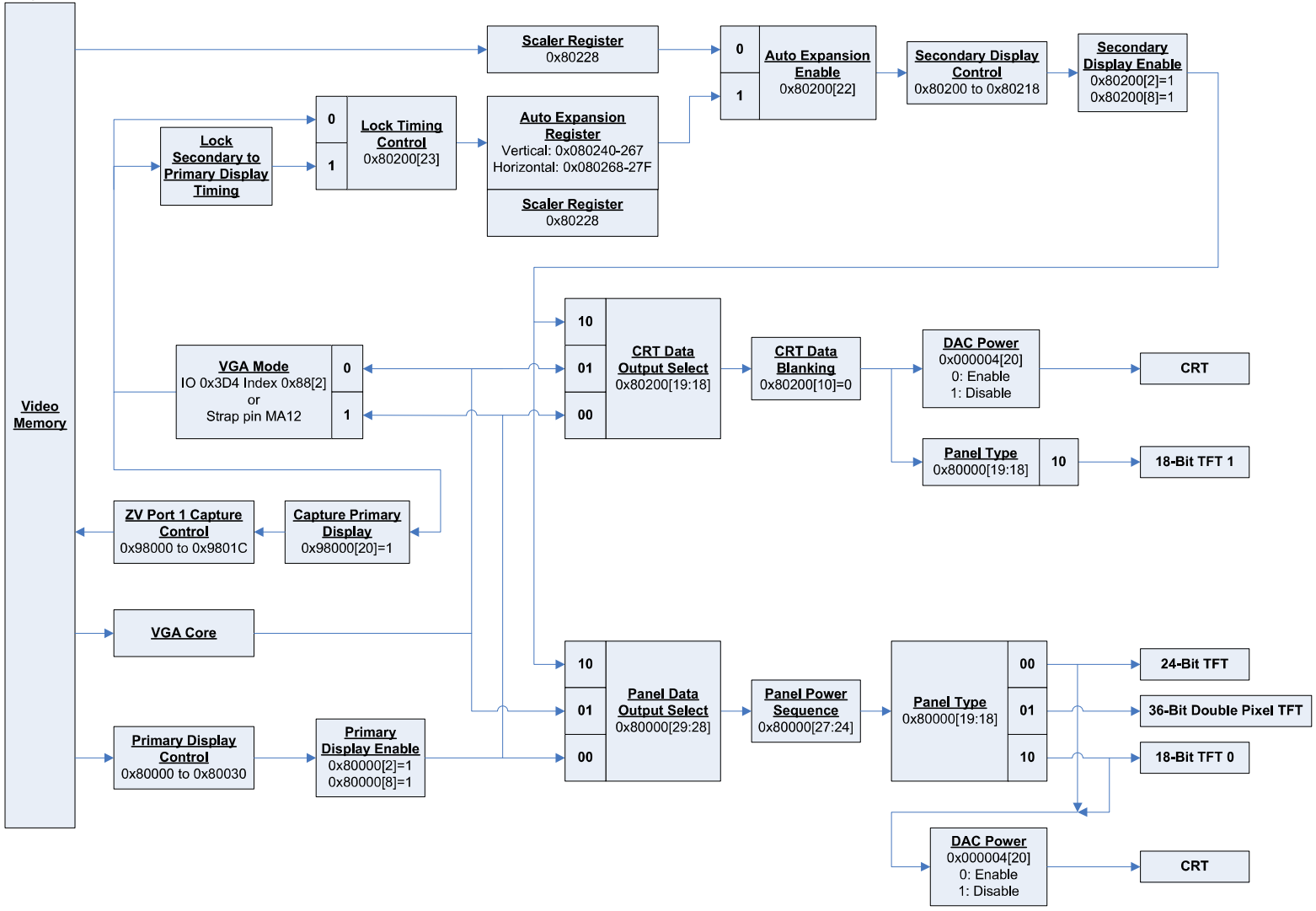
Dual Display

The SM718 supports Dual Display, i.e. two different displays of the same or different resolutions.

As shown in Figure 1-9, only the panel pipe supports the video and alpha planes. However, since these planes fetch data from the frame buffer memory as well, there might not be enough bandwidth to enable the video and alpha planes in Dual Display mode.

In order to display video on the panel pipe in Dual Display mode and on the CRT pipe in any mode, the 2D Engine's Color Space Conversion and Stretching functionality should be used.

The SM718 supports Dual Display in several combinations: CRT, LCD, LCD+CRT, or LCD1+LCD2; the figure below shows the relationship between each display in respect to the frame buffer.



1.3.7 LCD Panel

The SM718 integrates a concurrent video processor to control LCD displays. The SM718 LCD interface can be configured to drive one of the following:

- An 18-bit or 24-bit active matrix (TFT) panel
- An 36-bit (18-bit x 2) active matrix (TFT) panel
- Two independent 18-bit active matrix (TFT) panels

The maximum supported panel size is 1920x1440. Figure 9 shows a typical interface between the SM718 and a 24-bit TFT panel. Note the following with regards to this interface:

1. The timings of VDEN, FPEN, and BIAS are fully controlled by software.
2. The TFT panel does not use Vbias. The BIAS control used here controls the On/Off switch of the backlights. Program its timing so backlight is on after 12V is applied to the inverter.
3. The SM718 provides three PWM signals that can be used to control brightness.

See the SM718 MMCC Design Guide for information about interfacing to LCD displays.

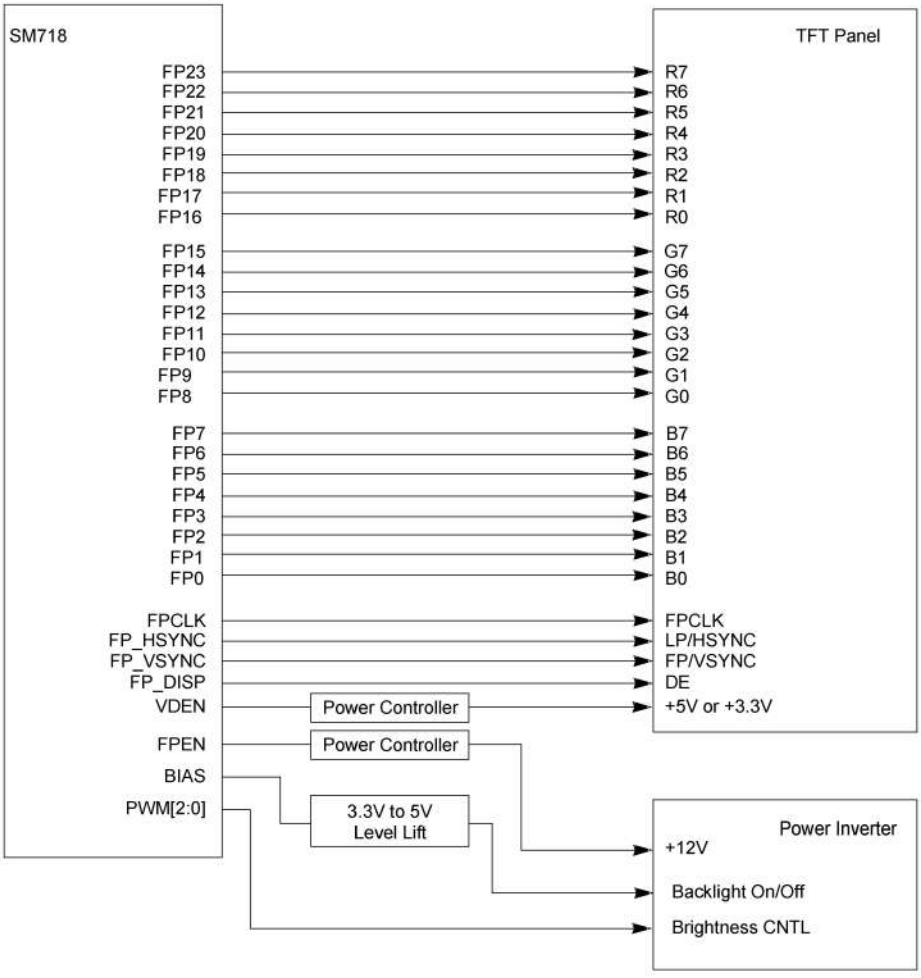


Figure 8: Typical 24-bit TFT Panel Interface

Figure 10 shows a typical interface between the SM718 and two independent 18-bit TFT panels.

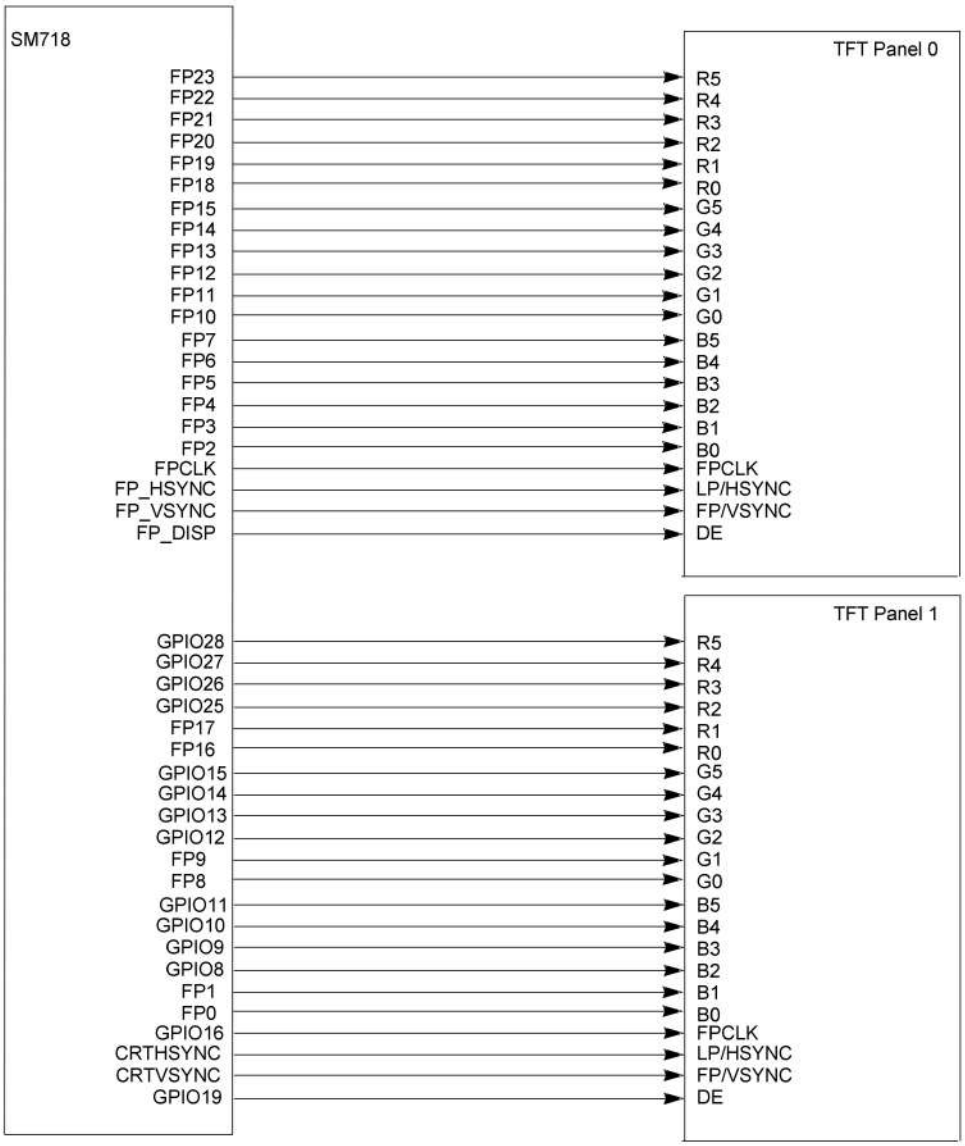


Figure 9: Typical Two 18-bit TFT Panels Interface

Table 2 compares the display data between different TFT modes.

SM718 Pin Name	Single TFT			Dual TFT	
	18-bit	24-bit	18-bit x 2	TFT 0	TFT 1
FPHSYNC	HSYNC	HSYNC	HSYNC	HSYNC	
FPVSYNC	VSYNC	VSYNC	VSYNC	VSYNC	
FPCLK	CLK	CLK	CLK	CLK	
FPDISP	DE	DE	DE	DE	
CRTHSYNC					HSYNC
CRTVSYNC					VSYNC
GPIO16					CLK
GPIO29					DE
GPIO28 (FDATA35)			RB5		R5
GPIO27 (FDATA34)			RB4		R4
GPIO26 (FDATA33)			RB3		R3
GPIO25 (FDATA32)			RB2		R2
GPIO15 (FDATA31)			GB5		G5
GPIO14 (FDATA30)			GB4		G4
GPIO13 (FDATA29)			GB3		G3
GPIO12 (FDATA28)			GB2		G2
GPIO11 (FDATA27)			BB5		B5
GPIO10 (FDATA26)			BB4		B4
GPIO9 (FDATA25)			BB3		B3
GPIO8 (FDATA24)			BB2		B2
FDATA23	R5	R7	RA5	R5	
FDATA22	R4	R6	RA4	R4	
FDATA21	R3	R5	RA3	R3	
FDATA20	R2	R4	RA2	R2	
FDATA19	R1	R3	RA1	R1	
FDATA18	R0	R2	RA0	R0	
FDATA17		R1	RB1		R1
FDATA16		R0	RB0		R0

SM718 Pin Name	Single TFT			Dual TFT	
	18-bit	24-bit	18-bit x 2	TFT 0	TFT 1
FDATA15	G5	G7	GA5	G5	
FDATA14	G4	G6	GA4	G4	
FDATA13	G3	G5	GA3	G3	
FDATA12	G2	G4	GA2	G2	
FDATA11	G1	G3	GA1	G1	
FDATA10	G0	G2	GA0	G0	
FDATA9		G1	GB1		G1
FDATA8		G0	GB0		G0
FDATA7	B5	B7	BA5	B5	
FDATA6	B4	B6	BA4	B4	
FDATA5	B3	B5	BA3	B3	
FDATA4	B2	B4	BA2	B2	
FDATA3	B1	B3	BA1	B1	
FDATA2	B0	B2	BA0	B0	
FDATA1		B1	BB1		B1
FDATA0		B0	BB0		B0

Table 5: Display data between the different TFT modes

1.3.8 Analog RGB (Analog LCD or CRT)

The analog RGB block contains two 24-bit DACs (RGB 8:8:8) to drive two external analog RGB interfaces. The 300 MHz DAC easily supports the maximum resolution of 1920 x 1440. See the SM718 MMCC Demo Board Design Guide for information about interfacing the SM718 to analog RGB devices.

1.3.9 GPIO

The SM718 provides 32 bits of GPIO. The table below shows the layout of these bits.

31	30	29	.....	25	24	.....	20	19	18	17	16	15	.....	8	7	.....	0
I2C		SSP1 or FD[35:32]			SSP0			PWM[2:0]			CLKIN or FDSCLK1	ZV Port[15:8] or FD[31:24]			ZV Port[7:0]		

ZV Port

Most ZV-compatible ICs support an 8-bit wide ZV port. The SM718 includes this functionality using GPIO pins 7:0. However, some ICs may only support a 16-bit ZV interface. To support these ICs, GPIO bits 15:8 may be used to add the extra 8 bits to the ZV interface.

PWM

Three independent PWM outputs are provided for generic use. Each output has its own control register. Two PWMs have each three independently selectable frequencies. The third PWM has three selectable frequency multiples that are synchronized to the Video Sync signal.

1.3.10 Strap Pins

MA[12:0], PWM[2:0], BA[1:0], and SSP0 signals control the power-on configuration for the SM718 according to table below:

Pin Name	Default Strapping	Description
MA1	Pulled-down	Memory Data Bus Width Selection: 0: 32-bit Memory Data Bus. 1: 64-bit Memory Data Bus.
MA2	Pulled-down	DDR Drive Strength Selection: 0: Normal DDR Driver Strength. 1: Low DDR Drive Strength.
MA3	Pulled-down	DDR DLL Selection: 0: DDR DLL Enabled. 1: DDR DLL Disabled.
MA4	Pulled-down	DDR CAS Selection: 0: 2.5 CAS Latency Clocks. 1: 3 CAS Latency Clocks.
MA[6:5]	Pulled-down	Memory Size Selection: 00: 16MB 01: 32MB 10: 64MB 11: 8MB
MA[8:7]	Pulled-down	Memory Column Size Selection: 00: 256 01: 512 1x: 1024

Pin Name	Default Strapping	Description
MA9	Pulled-down	Test Clock Selection: 0: Normal XTAL input. 1: Test Clock input.
MA10	Pulled-down	Reserved (must be 0)
MA11	Pulled-down	C0000 Access Enable: 0: Disable C0000 Access. 1: Enable C0000 Access.
MA12	Pulled-down	VGA Mode Selection: 0: VGA mode. 1: Non-VGA mode.
PWM[2:0]	Pulled-down	Bus Selection: 000: Hitachi SH3/SH4. 001: PCI. 010: Marvell Xscale. 110: NEC MIPS.
SSP0_RXD	Pulled-down	Marvell Xscale Host Clock Input Source: 0: Internal PLL. 1: HCLK pin.
SSP0_SFIN	Pulled-down	Host Data Bus Width: 0: 32-bit. 1: 64-bit.
BA[1:0]	Pulled-down	BIOS Default Panel Size: 00: 640x480. 01: 800x600. 10: 1024x768. 11: 1280x1024.

1.3.11 *DMA Controller*

The SM718 supports a DMA controller that can move data from one memory bus to another. DMA1 is used to transfer data between or within memory buses.

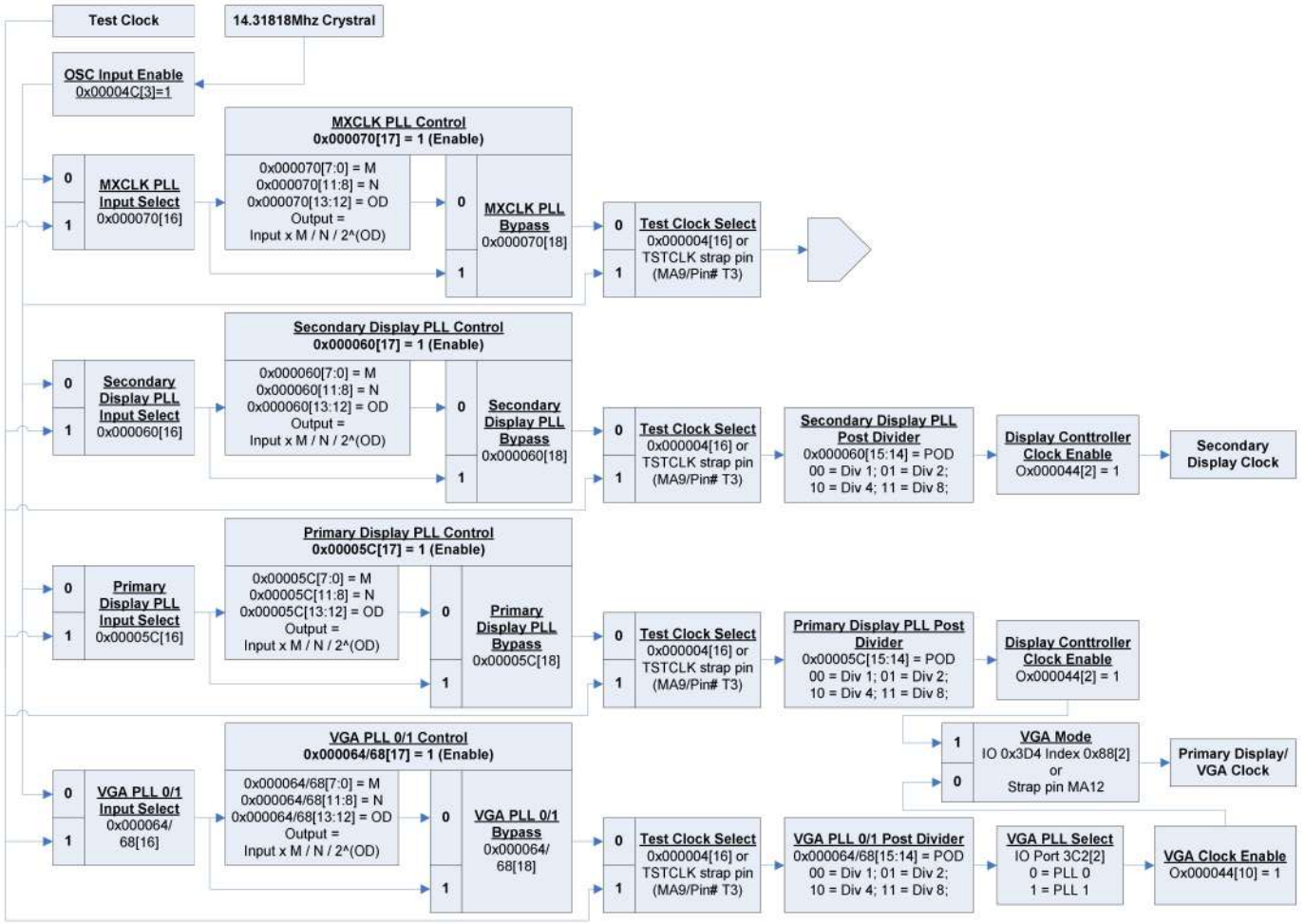
1.3.12 *Interrupt Controller*

Because the SM718 has only one interrupt to the PCI bus, all internal interrupts are shared without priority.

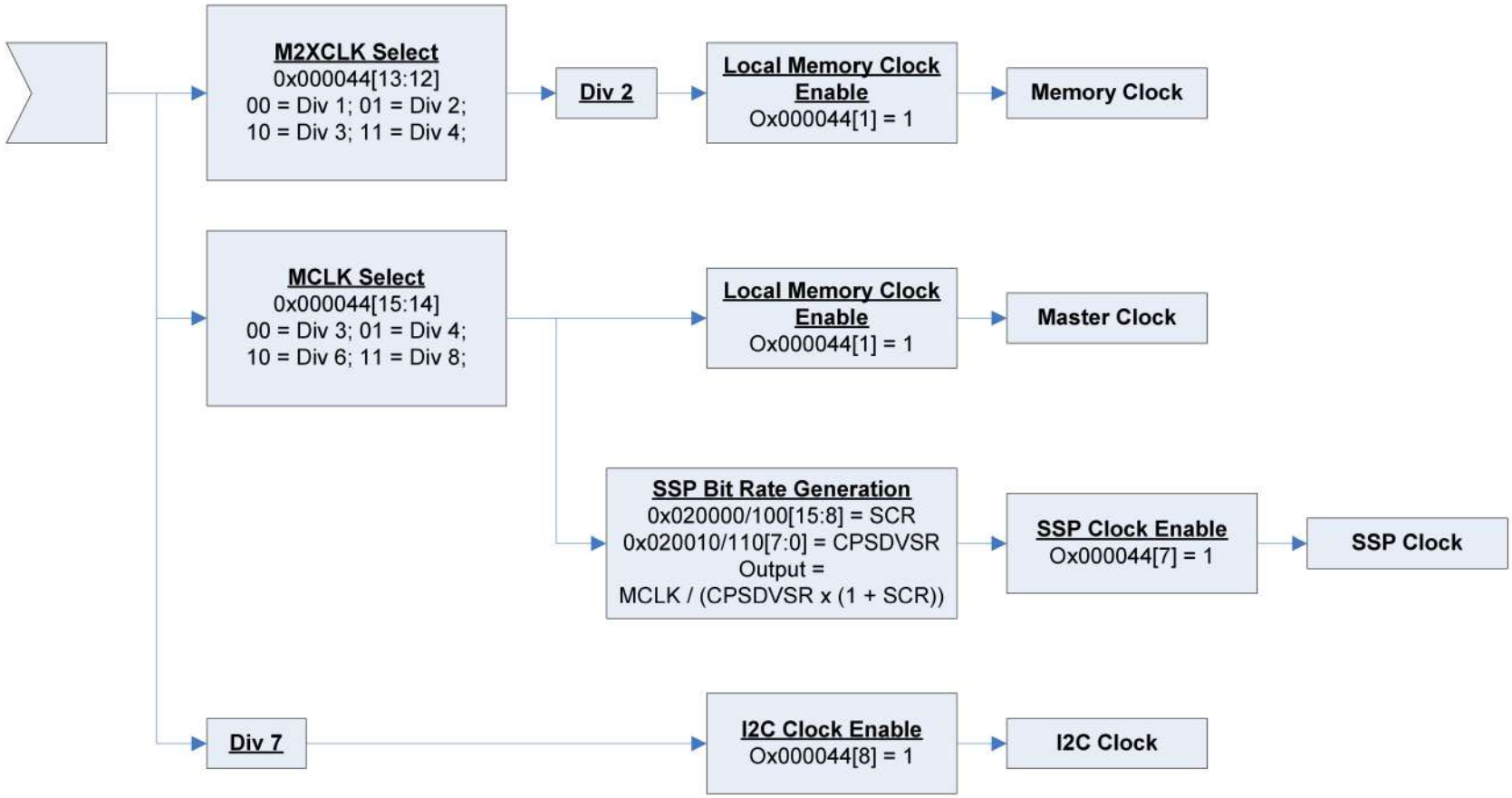
One interrupt status register specifies which module(s) generated the interrupts and the software drivers are responsible for clearing the interrupt at the source. The Host Interrupt remains asserted as long as there is any bit set in the System Interrupt Status register.

1.3.13 Clock Control

The SM718 has one oscillator input and one external clock input. The figure below shows the clock tree for the SM718.



Connecting to the MXCLK PLL Post Divider from the above figure, the figure below shows the detail clock tree for the master clock.



1.3.14 Power Management

Figure 11 shows the possible power states the SM718 supports.

During power-on reset, the SM718 comes up in a predefined state with all I/O turned off, and running the lowest possible clock. The software is responsible for programming the Mode 0 power state to the requested state after power-on and transition into the Mode 0 power state.

The Mode 0 and Mode 1 power states are the same and fully under software control. Whenever the software decides that the SM718 must go into a different state, the software programs the non-active power state and transitions into that state. This way there are an infinite number of power states supported by software and makes power management very flexible.

The Sleep power state puts the SM718 into a sleep mode. In this mode the SDRAM is put into self-refresh mode, and the crystal and PLL circuits are turned off.

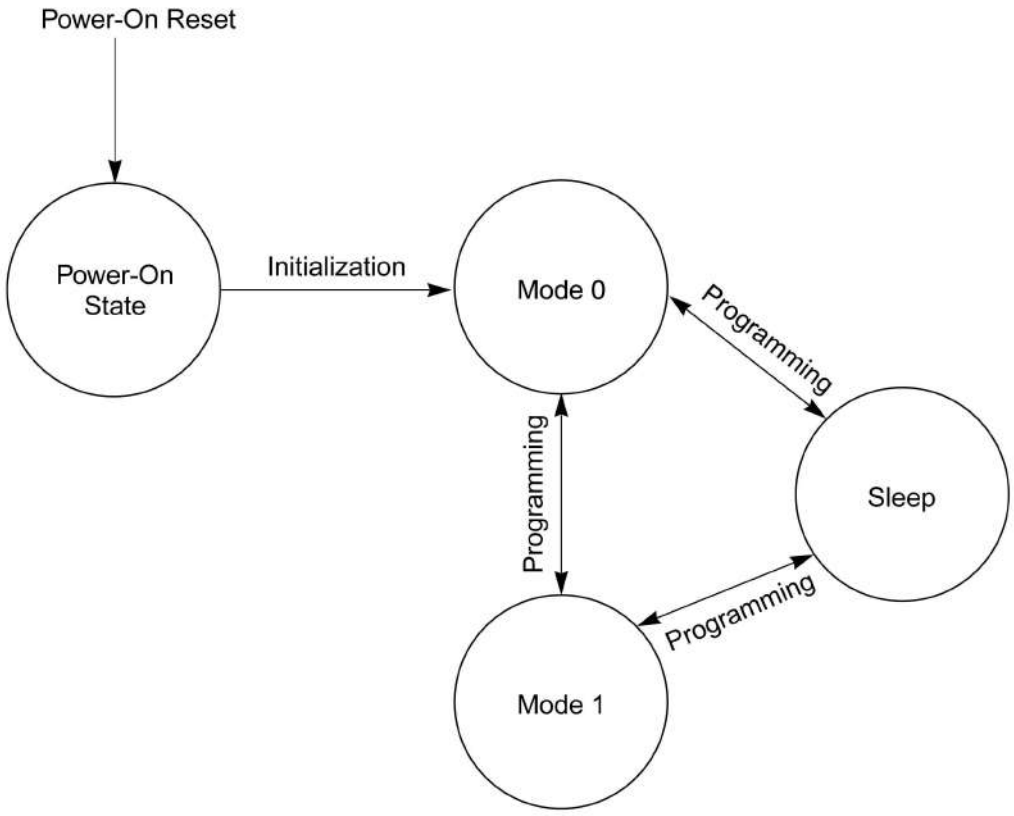


Figure 10: Power State Diagram

Notes: The System Control registers are clocked in the Host clock domain and even shutting off the crystal and PLL circuits does not keep the System Control registers and the host bus from functioning. This way the software is always able to wake up the SM718 from sleep mode.

1.3.15 MMIO Space

The MMIO space contains the SM718 register set and is divided into separate 64kB blocks that hold the registers for each individual functional block of the SM718. If a functional block requires a data port to fill its FIFO, a separate 64kB block is specified for the data port.

Figure 12 shows the MMIO space. Note that the addresses are offsets from the MMIO base address.

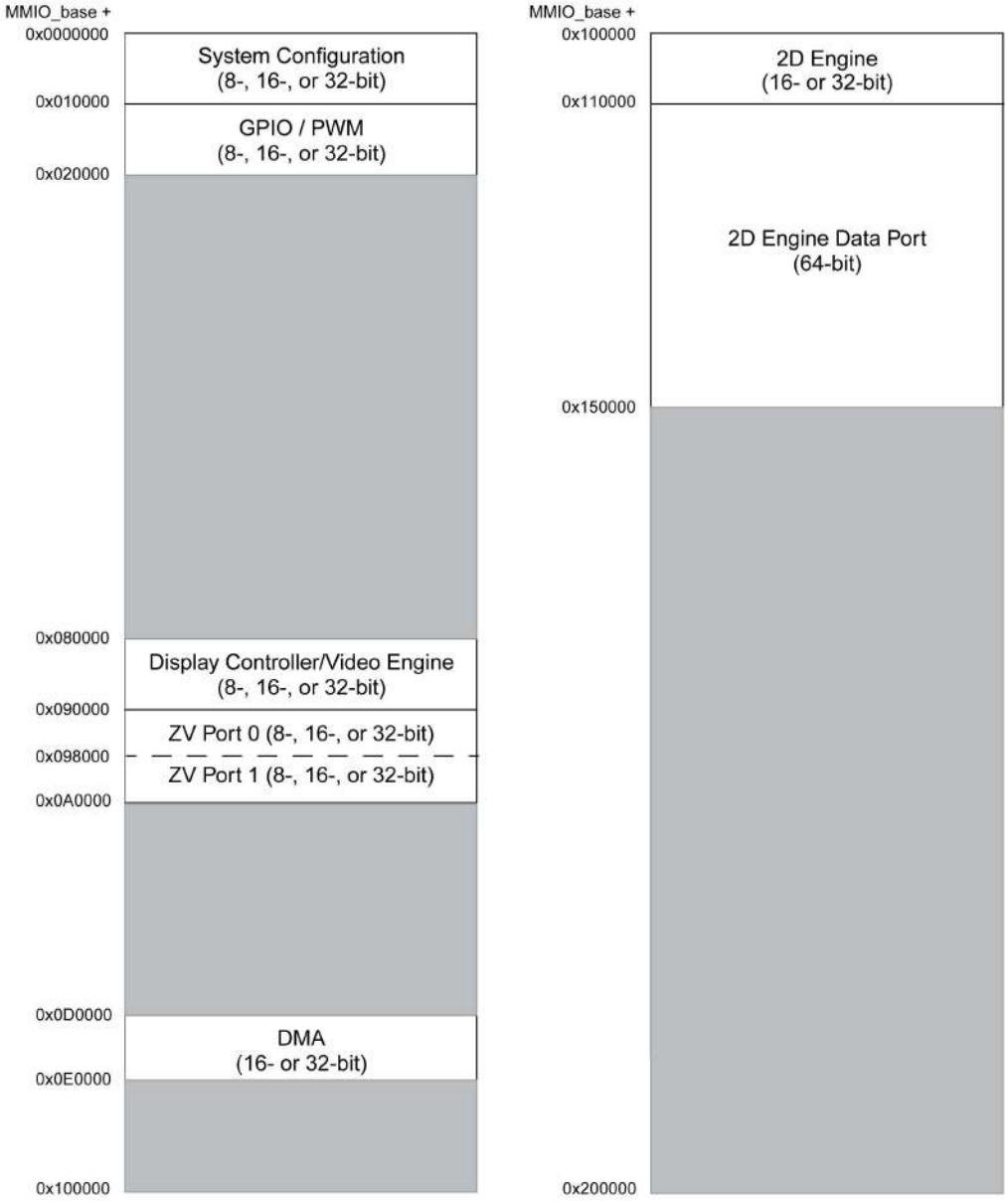


Figure 11: MMIO Space

1.4 Standard VGA

1.4.1 Video BIOS ROM Interface

The Video BIOS contains code for chip power-on initialization, graphics mode setup, and various read/write routines to the frame buffer. The Video BIOS can be burned into a separate video BIOS EPROM (this is the typical case for add-in board design) or be integrated into the system BIOS ROM (this is the typical case for embedded graphics implementation).

More information will be provided later.

1.4.2 Legacy VGA Support

TBA

2. VGA Register

2.1 Functional Overview

The SM718 has Standard VGA Registers and Extended VGA Registers.

2.2 VGA Registers

2.2.1 Register Descriptions

VGA Configuration Register

Read/Write MMIO_base + 0x000088

7	6	5	4	3	2	1	0
A0	Res	BA		Res	VGA	Gra	C0

Bit(s)	Name	Description
7	A0	A0000 Access Enable: 0x88[2] / 0x88[7] / A0000 Access / Usage 0 / 0 / Yes / Boot as primary 0 / 1 / Yes / Unused case 1 / 0 / No / Boot as secondary 1 / 1 / Yes / VESA modes that uses A0000 to access frame buffer.
6	Res	This bit is reserved.
5:4	BA	User Configuration bits configured by BA[1:0]
3	Res	This bit is reserved.
2	VGA	VGA and 0xA0000 access Mode: 0: Use VGA PLL and 0xA0000 access is in planar mode. 1: Use Panel PLL and 0xA0000 access is in linear mode. Note: Power-on configuration through MA[12].
1	Gra	Graphic Mode.
0	C0	C0000 Access Enable: 0: Disable C0000 access. (default) 1: Enable C0000 access. Note: Power-on configuration through MA[11].

2.3 Standard VGA Register

See SM712 for standard VGA registers definition

2.3.1 Extended VGA Registers

MMIO Address Register

Read/Write Address: 3D4, Index: 80

7	6	5	4	3	2	1	0
Addr R/W							

Bit(s)	Name	Description
7:0	Addr	MMIO Address [7:0]

MMIO Address Register

Read/Write Address: 3D4, Index: 81

7	6	5	4	3	2	1	0
Addr R/W							

Bit(s)	Name	Description
7:0	Addr	MMIO Address [15:8]

MMIO Address Register

Read/Write Address: 3D4, Index: 82

7	6	5	4	3	2	1	0
Addr R/W							

Bit(s)	Name	Description
7:0	Addr	MMIO Address [23:16]

MMIO Data 0 Register

Read/Write Address: 3D4, Index: 84

7	6	5	4	3	2	1	0
Data R/W							

Bit(s)	Name	Description
7:0	Data	MMIO Data [7:0]

MMIO Address 1 Register

Read/Write Address: 3D4, Index: 85

7	6	5	4	3	2	1	0
Data R/W							

Bit(s)	Name	Description
7:0	Data	MMIO Data [15:8]

MMIO Address 2 Register

Read/Write Address: 3D4, Index: 86

7	6	5	4	3	2	1	0
Data R/W							

Bit(s)	Name	Description
7:0	Data	MMIO Data [23:16]

MMIO Address 3 Register

Read/Write Address: 3D4, Index: 87

7	6	5	4	3	2	1	0
Data R/W							

Bit(s)	Name	Description
7:0	Data	MMIO Data [31:24]

To write data into MMIO register via IO port, programs MMIO address into MMIO address registers, write high order data into data register 1-3 (index 85-87), write low order data into data register 0 will generate MMIO write cycle.

To read data from MMIO register via IO port, programs MMIO address into MMIO address registers, read the corresponding data register will generate MMIO read cycle.

VGA Configuration Register

Read/Write Address: 3D4, Index: 88

7	6	5	4	3	2	1	0
Res		BA		Res	VGA	Gra	Res

Bit(s)	Name	Description
7:6	Res	These bits are reserved.
5:4	BA	User Configuration bits configured by BA[1:0]
3	Res	This bit is reserved.
2	VGA	VGA and 0xA0000 access Mode. (Power-on configuration through MA[12]) 0: Use VGA PLL and 0xA0000 access is in planar mode. 1: Use Panel PLL and 0xA0000 access is in linear mode.
1	Gra	Graphic Mode. 0: VGA mode. 1: Graphic mode.
0	C0	C0000 Access Enable: 0: Disable C0000 access. (default) 1: Enable C0000 access. Note: Power-on configuration through MA[11].

VGA Base Register

Read/Write Address: 3D4, Index: 89

7	6	5	4	3	2	1	0
VB R/W							

Bit(s)	Name	Description
7:0	VB	VGA Base Address [7:0]

VGA Base Register

Read/Write Address: 3D4, Index: 8A

7	6	5	4	3	2	1	0
VB R/W							

Bit(s)	Name	Description
7:2	Res	These bits are reserved.
1:0	VB	VGA Base Address [9:8]

In VGA mode, a 26-bits Local Memory address is generated by 10 bits (VGA Base Register) + 16 bits VGA Address. In other words, this is a page register to span 64M of frame buffer memory with a 64K address window.

VGA Scratch Data Register

Read/Write Address: 3D4, Index: 8B – 9F

7	6	5	4	3	2	1	0
Data R/W							

Bit(s)	Name	Description
7:0	Data	Scratch Data

3. System Configuration

3.1 Functional Overview

The SM718 has only one interrupt to the host bus. All internal interrupts are shared without priority.

3.2 Register Descriptions

Table 6 shows the System Configuration Register offsets and general functions.

Address Offset from MMIO_base1	Type	Width	Reset Value	Register Name
Configuration 1				
0x000000	R/W	32	0x00A00000	System Control
0x000004	R/W	32	0x01006066	Miscellaneous Control
0x000008	R/W	32	0x1F000000	$GPIO_{31:0}$ Control
0x00000C	R/W	32	0x01765324	Local Memory Arbitration Control
0x000010	R/W	32	0x01765324	PCI Bus Master Memory Arbitration Control
0x000014	R/W	32	0x00000000	Arbitration Control
0x000020	R	32	0x00000000	Raw Interrupt Status
0x000020	W	32	0x00000000	Raw Interrupt Clear
0x000024	R	32	0x00000000	Interrupt Status
0x000028	R/W	32	0x00000000	Interrupt Mask
0x00002C	R/W	32	0x00000000	Debug Control
Power Management				
0x000040	R	32	0x00005FC6	Current Clock Status
0x000044	R/W	32	0x00005FC6	Power Mode 0 Clock Control
0x000048	R/W	32	0x00005FC6	Power Mode 1 Clock Control
0x00004C	R/W	32	0x00000008	Power Mode Control
Configuration 2				
0x000050	R/W	32	0x00000000	PCI Master Base Address
0x000054	R	32	0x071800A0	Device Id
0x000058	R	32	0x00000000	PLL Clock Count
0x00005C	R/W	32	0x00020407	Primary Display PLL Control
0x000060	R/W	32	0x00020A1C	Secondary Display PLL Control
0x000064	R/W	32	0x00020407	VGA PLL 0 Control
0x000068	R/W	32	0x00020408	VGA PLL 1 Control
0x00006C	R/W	32	0x00000000	Scratch Data
0x000070	R/W	32	0x0002045C	MXCLK PLL Control

Table 6: SM718 System Configuration Register Summary

3.2.1 Configuration 1 Register Descriptions

System Control

Read/Write MMIO_base + 0x000000

Power-on Default 0x00A00000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DPMS R/W		Res				PM R/W	Res	2DF	2D	2DMF	CSC	CRT	P	Buf	DMA
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res		Abort R/W	Res				BE	Res				CT R/W	EMT R/W	MT R/W	PT R/W

Bit(s)	Name	Description
31:30	DPMS	31:30 Vertical Sync Horizontal Sync 00 Pulsing Pulsing 01 Pulsing Not pulsing 10 Not pulsing Pulsing 11 Not pulsing Not pulsing
29:26	Res	These bits are reserved.
25	PM	PCI Bus Master Control: 0: Disable. 1: Enable. Note: For DMA to transfer data to/from system memory, this bit has to set to 1.
24	Res	This bit is reserved.
23	2DF	2D Engine FIFO Empty. (Read Only) 0: FIFO not empty. 1: FIFO empty.
22	2D	2D Engine Status. (Read Only) 0: Idle. 1: Busy.
21	2DMF	2D Engine Memory Interface FIFO Empty. (Read Only) 0: FIFO not empty. 1: FIFO empty.
20	CSC	Color Space Conversion Status. (Read Only) 0: Idle. 1: Busy.
19	CRT	CRT VSYNC. (Read Only) 0: Normal. 1: CRT VSYNC.
18	P	Panel VSYNC. (Read Only) 0: Normal. 1: Panel VSYNC.
17	Buf	Current Buffer. (Read Only) 0: Normal. 1: Flip pending.
16	DMA	DMA Status. (Read Only) 0: Idle. 1: Busy.
15:14	Res	These bits are reserved.
13	Abort	Drawing Engine Abort. 0: Normal. 1: Abort 2D engine.

12:9	Res	These bits are reserved.

Bit(s)	Name	Description
8	BE	BAR 2 to BAR 5 Enable. (The count starts with BAR0) 0: Disable BAR 2, 3, 4, and 5 of PCI Config Space. (Default) 1: Enable BAR 2, 3, 4, and 5 of PCI Config Space.
7:4	Res	These bits are reserved.
3	CT	CRT Interface 3-State. 0: Normal. 1: 3-state.
2	EMT	External Memory Interface 3-State. 0: Normal. 1: 3-state.
1	LMT	Local Memory Interface 3-State. 0: Normal. 1: 3-state.
0	PT	Panel Interface 3-State. 0: Normal. 1: 3-state.

Miscellaneous Control

Read/Write MMIO_base + 0x000004

Power-on Default 0x01006066

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				RC	RCtl		II R/W	PLL R/W	Res		DAC R/W	Res			Clk R
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ColSize R/W		Size R/W		tWTR	tWR	tRP	tRFC	tRAS	Rst R/W	RA R/W	CL R/W	DLL R/W	Low	Width R/W	E R/W

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27	RC	Refresh Count. 0: Each refresh is 1 row. 1: Each refresh is 3 rows.
26:25	RCtl	Memory Refresh Control. 00: Refresh every 8x100xMemory Clock. 01: Refresh every 16x100xMemory Clock. 10: Refresh every 32x100xMemory Clock. 11: Refresh every 64x100xMemory Clock.
24	II	Interrupt Inverting. 0: Normal. 1: Inverted.
23	PLL	PLL Clock Count. (This bit is for testing purpose only) 0: Disable. 1: Enable.
22:21	Res	These bits are reserved.
20	DAC	DAC Power Control. 0: Enable. 1: Disable.
19:17	Res	These bits are reserved.
16	Clk	Clock Select. 0: Crystal input. (default) 1: Test clock input. Note: Power-on configuration through strap pin MA9.
15:14	ColSize	DDR SDRAM Column Size. 00: 256 words. 01: 512 words. 1x: 1024 words. Note: Power-on configuration through strap pins MA8 and MA7.
13:12	Size	DDR SDRAM Size. 00: 16MB 01: 32MB 10: 64MB 11: 8MB Note: Power-on configuration through strap pins MA6 and MA5.
11	tWTR	tWTR 0: 2 clocks. (default) 1: 1 clock.
10	tWR	tWR 0: 3 clocks. (default) 1: 2 clocks.
9	tRP	tRP 0: 3 clocks. (default) 1: 4 clocks.
8	tRFC	tRFC 0: 12 clocks. (default)

		1: 14 clocks.
7	tRAS	tRAS 0: 7 clocks. (default) 1: 8 clocks.

Bit(s)	Name	Description
6	Rst	Local Memory Controller Reset. (Software can use this bit for debug when suspecting local memory problem) 0: Reset 1: Normal
5	RA	Local Memory Remain in Active State. (This bit can be used by software to tune performance for video memory) 0: Remain active. 1: Do not remain active.
4	CL	Memory CAS Latency. 0: 2.5 clocks. 1: 3 clocks. Note: Power-on configuration through strap pin MA4.
3	DLL	DDR Delay Lock Loop Control. 0: Enable. 1: Disable. Note: Power-on configuration through strap pin MA3.
2	Low	SDRAM Low Driver Output. 0: Enable 1: Disable Note: Power-on configuration through strap pin MA2.
1	Width	Memory Bus Width. 0: 32bit. 1: 64bit. Note: Power-on configuration through strap pin MA1.
0	E	Embedded Memory Control. (This bit is used to disable embedded local memory) 0: Enable. 1: Disable.

$GPIO_{31:0}$ Control

Read/Write MMIO_base + 0x000008

Power-on Default 0x01F00000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
G_{31} R/W	G_{30} R/W	G_{29} R/W		G_{27} R/W		G_{25} R/W	G_{24} R/W		G_{22} R/W		G_{20} R/W	G_{19} R/W	G_{18} R/W	G_{17} R/W	G_{16} R/W
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
G_{15} R/W	G_{14} R/W	G_{13} R/W	G_{12} R/W	G_{11} R/W	G_{10} R/W	G_{9} R/W	G_{8} R/W	G_{7} R/W	G_{6} R/W	G_{5} R/W	G_{4} R/W	G_{3} R/W	G_{2} R/W	G_{1} R/W	G_{0} R/W

Bit(s)	Name	Description
31	G_{31}	GPIO Pin 31 Control. 0: GPIO. 1: I2C Data.
30	G_{30}	GPIO Pin 30 Control. 0: GPIO. 1: I2C Clock.
29	G_{29}	GPIO Pin 29 Control. 0: GPIO. 1: SSP1 Clock Out.
28	G_{28}	GPIO Pin 28 Control. 0: GPIO. 1: SSP1 Input. (Default)
27	G_{27}	GPIO Pin 27 Control. 0: GPIO. 1: SSP1 Frame Out.
26	G_{26}	GPIO Pin 26 Control. 0: GPIO. 1: SSP1 Input. (Default)
25	G_{25}	GPIO Pin 25 Control. 0: GPIO. 1: SSP1 Transmit.
24	G_{24}	GPIO Pin 24 Control. 0: GPIO. 1: SSP0 Clock Out.
23	G_{23}	GPIO Pin 23 Control. 0: GPIO. 1: SSP0 Input. (Default)
22	G_{22}	GPIO Pin 22 Control. 0: GPIO. 1: SSP0 Frame Out.
21	G_{21}	GPIO Pin 21 Control. 0: GPIO. 1: SSP0 Input. (Default)
20	G_{20}	GPIO Pin 20 Control. 0: GPIO. 1: SSP0 Transmit.
19	G_{19}	GPIO Pin 19 Control. 0: GPIO. 1: PWM2.
18	G_{18}	GPIO Pin 18 Control. 0: GPIO. 1: PWM1.

Bit(s)	Name	Description
17	G17	GPIO Pin 17 Control. 0: GPIO. 1: PWM0.
16	G16	GPIO Pin 16 Control. 0: GPIO or ZV-Port 1 Clock. 1: Test Data[xx].
15	G15	GPIO Pin 15 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
14	G14	GPIO Pin 14 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
13	G13	GPIO Pin 13 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
12	G12	GPIO Pin 12 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
11	G11	GPIO Pin 11 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
10	G10	GPIO Pin 10 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
9	G9	GPIO Pin 9 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
8	G8	GPIO Pin 8 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
7	G7	GPIO Pin 7 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
6	G6	GPIO Pin 6 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
5	G5	GPIO Pin 5 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
4	G4	GPIO Pin 4 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
3	G3	GPIO Pin 3 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
2	G2	GPIO Pin 2 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
1	G1	GPIO Pin 1 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
0	G0	GPIO Pin 0 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].

Local Memory Arbitration Control

Read/Write MMIO_base + 0x00000C

Power-on Default 0x01765324

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res			Int R/W	Res	VGA R/W			Res	DMA R/W			Res	ZVPort1 R/W		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	ZVPort0 R/W			Res	Video R/W			Res	Panel R/W			Res	CRT R/W		

Bit(s)	Name	Description			
31:29	Res	These bits are reserved.			
28	Int	Internal Memory Priority Scheme. 0: Fixed priority. 1: Revolving priority.			
27	Res	This bit is reserved.			
26:24	VGA	VGA FIFO Priority.			
		000	Off	100	Priority 4.
		001	Priority 1 (highest).	101	Priority 5.
		010	Priority 2.	110	Priority 6.
		011	Priority 3.	111	Priority 7 (lowest).
23	Res	This bit is reserved.			
22:20	DMA	DMA FIFO Priority.			
		000	Off	100	Priority 4.
		001	Priority 1 (highest).	101	Priority 5.
		010	Priority 2.	110	Priority 6.
		011	Priority 3.	111	Priority 7 (lowest).
19	Res	This bit is reserved.			
18:16	ZVPort1	ZV Port 1 FIFO Priority.			
		000	Off	100	Priority 4.
		001	Priority 1 (highest).	101	Priority 5.
		010	Priority 2.	110	Priority 6.
		011	Priority 3.	111	Priority 7 (lowest).
15	Res	This bit is reserved.			

<table>
<tr><th>Bit(s)</th><th>Name</th><th colspan="4">Description</th></tr>
<tr><td rowspan="6">14:12</td><td rowspan="6">ZVPort0</td><td colspan="4">ZV Port 0 FIFO Priority.</td></tr>
<tr><td>000</td><td>Off</td><td>100</td><td>Priority 4.</td></tr>
<tr><td>001</td><td>Priority 1 (highest).</td><td>101</td><td>Priority 5.</td></tr>
<tr><td>010</td><td>Priority 2.</td><td>110</td><td>Priority 6.</td></tr>
<tr><td>011</td><td>Priority 3.</td><td>111</td><td>Priority 7 (lowest).</td></tr>
<tr><td></td><td></td><td colspan="4"></td></tr>
<tr><td>11</td><td>Res</td><td colspan="4">This bit is reserved.</td></tr>
<tr><td rowspan="6">10:8</td><td rowspan="6">Video</td><td colspan="4">Video FIFO Priority.</td></tr>
<tr><td>000</td><td>Off</td><td>100</td><td>Priority 4.</td></tr>
<tr><td>001</td><td>Priority 1 (highest).</td><td>101</td><td>Priority 5.</td></tr>
<tr><td>010</td><td>Priority 2.</td><td>110</td><td>Priority 6.</td></tr>
<tr><td>011</td><td>Priority 3.</td><td>111</td><td>Priority 7 (lowest).</td></tr>
<tr><td></td><td></td><td colspan="4"></td></tr>
<tr><td>7</td><td>Res</td><td colspan="4">This bit is reserved.</td></tr>
<tr><td rowspan="6">6:4</td><td rowspan="6">Panel</td><td colspan="4">Panel FIFO Priority.</td></tr>
<tr><td>000</td><td>Off</td><td>100</td><td>Priority 4.</td></tr>
<tr><td>001</td><td>Priority 1 (highest).</td><td>101</td><td>Priority 5.</td></tr>
<tr><td>010</td><td>Priority 2.</td><td>110</td><td>Priority 6.</td></tr>
<tr><td>011</td><td>Priority 3.</td><td>111</td><td>Priority 7 (lowest).</td></tr>
<tr><td></td><td></td><td colspan="4"></td></tr>
<tr><td>3</td><td>Res</td><td colspan="4">This bit is reserved.</td></tr>
<tr><td rowspan="6">2:0</td><td rowspan="6">CRT</td><td colspan="4">CRT FIFO Priority.</td></tr>
<tr><td>000</td><td>Off</td><td>100</td><td>Priority 4.</td></tr>
<tr><td>001</td><td>Priority 1 (highest).</td><td>101</td><td>Priority 5.</td></tr>
<tr><td>010</td><td>Priority 2.</td><td>110</td><td>Priority 6.</td></tr>
<tr><td>011</td><td>Priority 3.</td><td>111</td><td>Priority 7 (lowest).</td></tr>
</table>

PCI Bus Master Memory Arbitration Control

Read/Write MMIO_base + 0x000010

Power-on Default 0x01765324

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res			Ext R/W	Res	VGA R/W			Res	DMA R/W			Res	ZVPort1 R/W		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	ZVPort0 R/W			Res	Video R/W			Res	Panel R/W			Res	CRT R/W		

Bit(s)	Name	Description			
31:29	Res	These bits are reserved.			
28	Ext	External Memory Priority Scheme. 0: Fixed priority. 1: Revolving priority.			
27	Res	This bit is reserved.			
26:24	VGA	VGA FIFO Priority.			
		000	Off	100	Priority 4.
		001	Priority 1 (highest).	101	Priority 5.
		010	Priority 2.	110	Priority 6.
		011	Priority 3.	111	Priority 7 (lowest).
23	Res	This bit is reserved.			
22:20	DMA	DMA FIFO Priority.			
		000	Off	100	Priority 4.
		001	Priority 1 (highest).	101	Priority 5.
		010	Priority 2.	110	Priority 6.
		011	Priority 3.	111	Priority 7 (lowest).
19	Res	This bit is reserved.			
18:16	ZVPort1	ZV Port 1 FIFO Priority.			
		000	Off	100	Priority 4.
		001	Priority 1 (highest).	101	Priority 5.
		010	Priority 2.	110	Priority 6.
		011	Priority 3.	111	Priority 7 (lowest).
15	Res	This bit is reserved.			

<table>
<tr><th>Bit(s)</th><th>Name</th><th colspan="4">Description</th></tr>
<tr><td rowspan="5">14:12</td><td rowspan="5">ZVPort0</td><td colspan="4">ZV Port 0 FIFO Priority.</td></tr>
<tr><td>000</td><td>Off</td><td>100</td><td>Priority 4.</td></tr>
<tr><td>001</td><td>Priority 1 (highest).</td><td>101</td><td>Priority 5.</td></tr>
<tr><td>010</td><td>Priority 2.</td><td>110</td><td>Priority 6.</td></tr>
<tr><td>011</td><td>Priority 3.</td><td>111</td><td>Priority 7 (lowest).</td></tr>
<tr><td>11</td><td>Res</td><td colspan="4">This bit is reserved.</td></tr>
<tr><td rowspan="5">10:8</td><td rowspan="5">Video</td><td colspan="4">Video FIFO Priority.</td></tr>
<tr><td>000</td><td>Off</td><td>100</td><td>Priority 4.</td></tr>
<tr><td>001</td><td>Priority 1 (highest).</td><td>101</td><td>Priority 5.</td></tr>
<tr><td>010</td><td>Priority 2.</td><td>110</td><td>Priority 6.</td></tr>
<tr><td>011</td><td>Priority 3.</td><td>111</td><td>Priority 7 (lowest).</td></tr>
<tr><td>7</td><td>Res</td><td colspan="4">This bit is reserved.</td></tr>
<tr><td rowspan="5">6:4</td><td rowspan="5">Panel</td><td colspan="4">Panel FIFO Priority.</td></tr>
<tr><td>000</td><td>Off</td><td>100</td><td>Priority 4.</td></tr>
<tr><td>001</td><td>Priority 1 (highest).</td><td>101</td><td>Priority 5.</td></tr>
<tr><td>010</td><td>Priority 2.</td><td>110</td><td>Priority 6.</td></tr>
<tr><td>011</td><td>Priority 3.</td><td>111</td><td>Priority 7 (lowest).</td></tr>
<tr><td>3</td><td>Res</td><td colspan="4">This bit is reserved.</td></tr>
<tr><td rowspan="5">2:0</td><td rowspan="5">CRT</td><td colspan="4">CRT FIFO Priority.</td></tr>
<tr><td>000</td><td>Off</td><td>100</td><td>Priority 4.</td></tr>
<tr><td>001</td><td>Priority 1 (highest).</td><td>101</td><td>Priority 5.</td></tr>
<tr><td>010</td><td>Priority 2.</td><td>110</td><td>Priority 6.</td></tr>
<tr><td>011</td><td>Priority 3.</td><td>111</td><td>Priority 7 (lowest).</td></tr>
</table>

Arbitration Control

Read/Write MMIO_base + 0x000014

Power-on Default 0x0000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res			Int R/W	Res					Panel R/W			Res	ZVPort R/W		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	Command R/W			Res	DMA R/W			Res	Video R/W			Res	CRT R/W		

Bit(s)	Name	Description
31:29	Res	These bits are reserved.
28	Int	Internal Memory Priority Scheme. 0: Fixed priority. 1: Revolving priority.
27:23	Res	These bits are reserved.
22:20	Panel	Panel FIFO Priority. 000 Off; 001 Priority 1 (highest).; 010 Priority 2.; 011 Priority 3.; 100 Priority 4.; 101 Priority 5.; 110 Priority 6.; 111 Priority 7 (lowest).
19	Res	This bit is reserved.
18:16	ZVPort	ZV Port FIFO Priority. 000 Off; 001 Priority 1 (highest).; 010 Priority 2.; 011 Priority 3.; 100 Priority 4.; 101 Priority 5.; 110 Priority 6.; 111 Priority 7 (lowest).
15	Res	This bit is reserved.
14:12	Command	Command List Interpreter FIFO Priority. 000 Off; 001 Priority 1 (highest).; 010 Priority 2.; 011 Priority 3.; 100 Priority 4.; 101 Priority 5.; 110 Priority 6.; 111 Priority 7 (lowest).
11	Res	This bit is reserved.
10:8	DMA	DMA FIFO Priority. 000 Off; 001 Priority 1 (highest).; 010 Priority 2.; 011 Priority 3.; 100 Priority 4.; 101 Priority 5.; 110 Priority 6.; 111 Priority 7 (lowest).
7	Res	This bit is reserved.

<table>
<tr><th>Bit(s)</th><th>Name</th><th>Description</th></tr>
<tr><td>6:4</td><td>Video</td><td>Video FIFO Priority.<table>
<tr><td>000</td><td>Off</td><td>100</td><td>Priority 4.</td></tr>
<tr><td>001</td><td>Priority 1 (highest).</td><td>101</td><td>Priority 5.</td></tr>
<tr><td>010</td><td>Priority 2.</td><td>110</td><td>Priority 6.</td></tr>
<tr><td>011</td><td>Priority 3.</td><td>111</td><td>Priority 7 (lowest).</td></tr>
</table></td></tr>
<tr><td>3</td><td>Res</td><td>This bit is reserved.</td></tr>
<tr><td>2:0</td><td>CRT</td><td>CRT FIFO Priority.<table>
<tr><td>000</td><td>Off</td><td>100</td><td>Priority 4.</td></tr>
<tr><td>001</td><td>Priority 1 (highest).</td><td>101</td><td>Priority 5.</td></tr>
<tr><td>010</td><td>Priority 2.</td><td>110</td><td>Priority 6.</td></tr>
<tr><td>011</td><td>Priority 3.</td><td>111</td><td>Priority 7 (lowest).</td></tr>
</table></td></tr>
</table>

Raw Interrupt Status

Read MMIO_base + 0x000020

Power-on Default 0x0000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res											ZV1 R	ZV0 R	CV R	PV R	VV R

Bit(s)	Name	Description
31:5	Res	These bits are reserved.
4	ZV1	ZV Port 1 VSYNC Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
3	ZV0	ZV Port 0 VSYNC Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
2	CV	CRT VSYNC Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
1	PV	Panel VSYNC Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
0	VV	VGA VSYNC Interrupt Status. 0: Interrupt not active. 1: Interrupt active.

Raw Interrupt Clear

Write MMIO_base + 0x000020

Power-on Default 0x0000000

Interrupt bit should be clear by software when the interrupt has been serviced. Writing a zero has no effect. This register can be used to clear interrupts from VGA, Panel, CRT, ZV0, and ZV1. Other features (DMA, for example) have interrupt clear bits in their own functional registers sets.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res											ZV1 W	ZV0 W	CV W	PV W	VV W

Bit(s)	Name	Description
31:5	Res	These bits are reserved.
4	ZV1	ZV Port 1 VSYNC Interrupt Status. 0: No action. 1: Clear interrupt.
3	ZV0	ZV Port 0 VSYNC Interrupt Status. 0: No action. 1: Clear interrupt.
2	CV	CRT VSYNC Interrupt Status. 0: No action. 1: Clear interrupt.
1	PV	Panel VSYNC Interrupt Status. 0: No action. 1: Clear interrupt.
0	VV	VGA VSYNC Interrupt Status. 0: No action. 1: Clear interrupt.

Interrupt Status

Read MMIO_base + 0x000024

Power-on Default 0x0000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
G31 R	G30 R	G29 R	G28 R	G27 R	G26 R	G25 R	Res								
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res			I2C R	PW R	Res	DMA1 R	PCI R	S1 R	S0 R	2D R	ZV1 R	ZV0 R	CV R	PV R	VV R

Bit(s)	Name	Description
31	G31	GPIO Pin 31 Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
30	G30	GPIO Pin 30 Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
29	G29	GPIO Pin 29 Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
28	G28	GPIO Pin 28 Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
27	G27	GPIO Pin 27 Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
26	G26	GPIO Pin 26 Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
25	G25	GPIO Pin 25 Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
24:13	Res	These bits are reserved.
12	I2C	I2C Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
11	PW	PWM Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
10	Res	This bit is reserved.
9	DMA1	DMA 1 Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
8	Res	This bit is reserved.
7	S1	SSP1 Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
6	S0	SSP0 Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
5	2D	2D Engine Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
4	ZV1	ZV-Port 1 Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
3	ZV0	ZV-Port 0 Interrupt Status. 0: Interrupt not active.

1: Interrupt active.

Bit(s)	Name	Description
2	CV	CRT Vertical Sync Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
1	PV	Panel Vertical Sync Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
0	VV	VGA Vertical Sync Interrupt Status. 0: Interrupt not active. 1: Interrupt active.

Interrupt Mask

Read MMIO_base + 0x000028

Power-on Default 0x0000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
G31 R/W	G30 R/W	G29 R/W	G28 R/W	G27 R/W	G26 R/W	G25 R/W	Res								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res			I2C R/W	PW R/W	Res	DMA1 R/W	PCI R/W	S1 R/W	S0 R/W	2D R/W	ZV1 R/W	ZV0 R/W	CV R/W	PV R/W	VV R/W

Bit(s)	Name	Description
31	G31	GPIO Pin 31 Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
30	G30	GPIO Pin 30 Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
29	G29	GPIO Pin 29 Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
28	G28	GPIO Pin 28 Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
27	G27	GPIO Pin 27 Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
26	G26	GPIO Pin 26 Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
25	G25	GPIO Pin 25 Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
24:13	Res	These bits are reserved.
12	I2C	I2C Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
11	PW	PWM Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
10	Res	This bit is reserved.
9	DMA1	DMA 1 Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
8	PCI	PCI Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
7	S1	SSP1 Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
6	S0	SSP0 Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
5	2D	2D Engine Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
4	ZV1	ZV-Port 1 Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.

Bit(s)	Name	Description
3	ZV0	ZV-Port 0 Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
2	CV	CRT Vertical Sync Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
1	PV	Panel Vertical Sync Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
0	VV	VGA Vertical Sync Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.

Debug Control

Read/Write MMIO_base + 0x00002C

Power-on Default 0x0000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res								Module R/W			Partition R/W				

Bit(s)	Name	Description
31:8	Res	These bits are reserved.
7:5	Module	Module Select for Partition.
4:0	Partition	Partition select for Debugging Test Mode. 00000: PCI controller 00001: External memory controller 00010: HIF controller 00100: Display controller 00101: ZV-Port 0 00110: 2D Engine 01000: Internal memory interface 01011: ZV-Port 1 01100: SSP0 01101: SSP1 10101: I2C 11010: Internal memory controller 11011: DMA 11100: Simulation test mode 11110: VGA 0 11111: VGA 1

3.2.2 Power Management Register Descriptions

Current Clock Status

Read MMIO_base + 0x000040

Power-on Default 0x00005FC6

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MR		M2R		Res	VR	PR	I2CR	SR	GR	ZR	CR	2DR	DR	MR	DMAR

Bit(s)	Name	Description
31:16	Res	These bits are reserved.
15:14	M	MCLK Select. (Master clock select, the frequencies are derived from input crystal value of 14.31818MHz) 00: Divided by 3. 01: Divided by 4. (default) 10: Divided by 6. 11: Divided by 8.
13:12	M2	M2XCLK Select. (Memory clock select, the frequencies are derived from input crystal value of 14.3181MHz) 00: Divided by 1. 01: Divided by 2. (default) 10: Divided by 3. 11: Divided by 4.
11	Res	This bit is reserved.
10	V	VGA Clock Control. 0: Disable. 1: Enable.
9	P	PWM Clock Control. 0: Disable. 1: Enable.
8	I2C	I2C Clock Control. 0: Disable. 1: Enable.
7	S	SSP Clock Control. 0: Disable. 1: Enable.
6	G	GPIO Clock Control. 0: Disable. 1: Enable.
5	Z	ZV Port Clock Control. 0: Disable. 1: Enable.
4	C	Color Space Conversion Clock Control. 0: Disable. 1: Enable.
3	2D	2D Engine Clock Control. 0: Disable. 1: Enable.
2	D	Display Controller Clock Control. 0: Disable. 1: Enable.
1	M	Local Memory Controller Clock Control. 0: Disable. 1: Enable.
0	DMA	DMA Clock Control. 0: Disable. 1: Enable.

Power Mode 0 Clock Control

Read/Write MMIO_base + 0x000044

Power-on Default 0x00005FC6

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M R/W		M2 R/W		Res	V R/W	P R/W	I2C R/W	S R/W	G R/W	Z R/W	C R/W	2D R/W	D R/W	M R/W	DMA R/W

Bit(s)	Name	Description
31:16	Res	These bits are reserved.
15:14	M	MCLK Select. 00: Divided by 3. 01: Divided by 4. (default) 10: Divided by 6. 11: Divided by 8.
13:12	M2	M2XCLK Select. 00: Divided by 1. 01: Divided by 2. (default) 10: Divided by 3. 11: Divided by 4.
11	Res	This bit is reserved.
10	V	VGA Clock Control. 0: Disable. 1: Enable.
9	P	PWM Clock Control. 0: Disable. 1: Enable.
8	I2C	I2C Clock Control. 0: Disable. 1: Enable.
7	S	SSP Clock Control. 0: Disable. 1: Enable.
6	G	GPIO Clock Control. 0: Disable. 1: Enable.
5	Z	ZV Port Clock Control. 0: Disable. 1: Enable.
4	C	Color Space Conversion Clock Control. 0: Disable. 1: Enable.
3	2D	2D Engine Clock Control. 0: Disable. 1: Enable.
2	D	Display Controller Clock Control. 0: Disable. 1: Enable.
1	M	Local Memory Controller Clock Control. 0: Disable. 1: Enable.
0	DMA	DMA Clock Control. 0: Disable. 1: Enable.

Power Mode 1 Clock Control

Read/Write MMIO_base + 0x000048

Power-on Default 0x00005FC6

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M R/W		M2 R/W		Res	V R/W	P R/W	I2C R/W	S R/W	G R/W	Z R/W	C R/W	2D R/W	D R/W	M R/W	DMA R/W

Bit(s)	Name	Description
31:16	Res	These bits are reserved.
15:14	M	MCLK Select. 00: Divided by 3. 01: Divided by 4. (default) 10: Divided by 6. 11: Divided by 8.
13:12	M2	M2XCLK Select. 00: Divided by 1. 01: Divided by 2. (default) 10: Divided by 3. 11: Divided by 4.
11	Res	This bit is reserved.
10	V	VGA Clock Control. 0: Disable. 1: Enable.
9	P	PWM Clock Control. 0: Disable. 1: Enable.
8	I2C	I2C Clock Control. 0: Disable. 1: Enable.
7	S	SSP Clock Control. 0: Disable. 1: Enable.
6	G	GPIO Clock Control. 0: Disable. 1: Enable.
5	Z	ZV Port Clock Control. 0: Disable. 1: Enable.
4	C	Color Space Conversion Clock Control. 0: Disable. 1: Enable.
3	2D	2D Engine Clock Control. 0: Disable. 1: Enable.
2	D	Display Controller Clock Control. 0: Disable. 1: Enable.
1	M	Local Memory Controller Clock Control. 0: Disable. 1: Enable.
0	DMA	DMA Clock Control. 0: Disable. 1: Enable.

Power Mode Control

Read/Write MMIO_base + 0x00004C

Power-on Default 0x00000008

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res												O R/W	A R/W	Mode R/W	

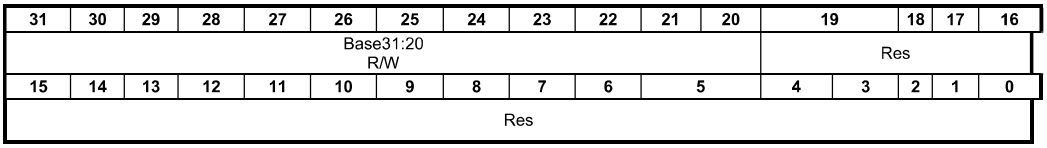
Bit(s)	Name	Description
31:4	Res	These bits are reserved.
3	O	Oscillator Input Control. (Enable or disable crystal input) 0: Disable. 1: Enable. (default)
2	A	ACPI Select. 0: Enable. 1: Disable.
1:0	Mode	Power Mode Select. 00: Power Mode 0. 01: Power Mode 1. 1x: Sleep Mode.

3.2.3 *Configuration 2 Register Descriptions*

PCI Master Base Address

Read/Write MMIO_base + 0x000050

Power-on Default 0x00000000



Bit(s)	Name	Description
31:20	Base31:20	PCI Master Base Address Bits [31:20].
19:0	Res	These bits are reserved.

Device Id

Read MMIO_base + 0x000054

Power-on Default 0x071800A0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DeviceId R															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res								RevisionId R							

Bit(s)	Name	Description
31:16	DeviceId	Device Identification: 0x0718.
15:8	Res	These bits are reserved.
7:0	RevisionId	Revision Identification: 0xA0.

PLL Clock Count

Read MMIO_base + 0x000058

Power-on Default 0x00000000

1	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ClockCount R															

Bit(s)	Name	Description
31:16	Reserved	These bits are reserved.
15:0	ClockCount	Number of clocks since enabling. These clock counts verify if there is a PLL function. (This is for testing purpose only)

Primary Display Control

Read/Write MMIO_base + 0x00005C

Power-on Default 0x00020407

Controlled by Configuration Register (0x3D4, index 88) bit 2 exclusively.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				By R/W				PD R/W				OD R/W			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OD R/W				Res				N R				M R			

Bit(s)	Name	Description
31:19	Res	These bits are reserved.
18	By	PLL Bypass. 0: No bypass. (default) 1: Bypass.
17	PD	PLL Power Down. 0: Power Down. 1: Power On.
16	CS	PLL Clock Select. 0: Crystal input. (default) 1: Test clock input.
15:14	POD	PLL Post Divider. 00: Divided by 1. 01: Divided by 2. 10: Divided by 4. 11: Divided by 8.
13:12	OD	PLL OD. 00: Divided by 1. 01: Divided by 2. 10: Divided by 4. 11: Divided by 8.
11:8	N	PLL N Value.
7:0	M	PLL M Value.

Secondary Display Control

Read/Write MMIO_base + 0x000060

Power-on Default 0x00020A1C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				By R/W				PD R/W				OD R/W			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OD R/W				Res				N R				M R			

Bit(s)	Name	Description
31:19	Res	These bits are reserved.
18	By	PLL Bypass. 0: No bypass. (default) 1: Bypass.
17	PD	PLL Power Down. 0: Power Down. 1: Power On.
16	CS	PLL Clock Select. 0: Crystal input. (default) 1: Test clock input.
15:14	POD	PLL Post Divider. 00: Divided by 1. 01: Divided by 2. 10: Divided by 4. 11: Divided by 8.
13:12	OD	PLL OD. 00: Divided by 1. 01: Divided by 2. 10: Divided by 4. 11: Divided by 8.
11:8	N	PLL N Value.
7:0	M	PLL M Value.

VGA PLL 0 Control

Read/Write MMIO_base + 0x000064

Power-on Default 0x00020407

Controlled by Standard VGA Register 3C2[2] exclusively.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				By R/W				PD R/W				OD R/W			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OD R/W				Res				N R				M R			

Bit(s)	Name	Description
31:19	Res	These bits are reserved.
18	By	PLL Bypass. 0: No bypass. (default) 1: Bypass.
17	PD	PLL Power Down. 0: Power Down. 1: Power On.
16	CS	PLL Clock Select. 0: Crystal input. (default) 1: Test clock input.
15:14	POD	PLL Post Divider. 00: Divided by 1. 01: Divided by 2. 10: Divided by 4. 11: Divided by 8.
13:12	OD	PLL OD. 00: Divided by 1. 01: Divided by 2. 10: Divided by 4. 11: Divided by 8.
11:8	N	PLL N Value.
7:0	M	PLL M Value.

VGA PLL 1 Control

Read/Write MMIO_base + 0x000068

Power-on Default 0x00020408

Controlled by Standard VGA Register 3C2[2] exclusively.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res													By R/W	PD R/W	OD R/W
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OD R/W	Res			N R				M R							

Bit(s)	Name	Description
31:19	Res	These bits are reserved.
18	By	PLL Bypass. 0: No bypass. (default) 1: Bypass.
17	PD	PLL Power Down. 0: Power Down. 1: Power On.
16	CS	PLL Clock Select. 0: Crystal input. (default) 1: Test clock input.
15:14	POD	PLL Post Divider. 00: Divided by 1. 01: Divided by 2. 10: Divided by 4. 11: Divided by 8.
13:12	OD	PLL OD. 00: Divided by 1. 01: Divided by 2. 10: Divided by 4. 11: Divided by 8.
11:8	N	PLL N Value.
7:0	M	PLL M Value.

PLL Notes:

- All PLLs are defaulted to power on after RESET. Software can turn off any PLL not in use for power saving purpose.
- PLL output frequency = 14.31818MHz x M / N (2^OD)

MXCLK PLL Control

Read/Write MMIO_base + 0x000070

Power-on Default 0x0002045C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res													By R/W	PD R/W	OD R/W
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res		OD R/W		N R				M R							

Bit(s)	Name	Description
31:19	Res	These bits are reserved.
18	By	PLL Bypass. 0: No bypass. (default) 1: Bypass.
17	PD	PLL Power Down. 0: Power Down. 1: Power On.
16	CS	PLL Clock Select. 0: Crystal input. (default) 1: Test clock input.
15:14	Res	These bits are reserved.
13:12	OD	PLL OD. 00: Divided by 1. 01: Divided by 2. 10: Divided by 4. 11: Divided by 8.
11:8	N	PLL N Value.
7:0	M	PLL M Value.

Host Control

Read/Write MMIO_base + 0x000074

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Non$ RW														S R
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
16b RW	Xc RW	Res						E RW	SH RW	VR RW	extRDY RW		Bus RW		

Bit(s)	Name	Description
31	Res	This bit is reserved.
30:17	Non$	Non-Cache Addres. Readying this address [Non$, xxxx] does not get data from the previous read. It fetches data directly from memory.
16	S	Current Sleep Status: (read only) 0: Not in sleep mode. 1: In sleep mode. Note: When the SM718 is transitioning back from sleep mode to normal power mode (Mode 0 or 1), the software needs to poll this bit until it becomes “0” before writing any other command to the chip.
15	16b	Host CPU 16bit/32bit Selection: 0: Host CPU 32bit mode. 1: Host CPU 16bit mode. Note: This bit is determined by GPIO23 pin at reset.
14	Xc	Marvell Xscale Clock Input Source Selection: 0: Internal PLL. 1: HCLK pin. Note: This bit is determined by GPIO21 pin at reset.
13:8	Res	These bits are reserved.
7	E	Endian Selection: 0: Little Endian. (default) 1: Big Endian. Note: To program the correct Endianess for the CPU, the CPU should either write 0x00000000 (for little Endian) or 0xFFFFFFFF (for big Endian) into this register before programming any other register on the chip.
6	SH	Hitachi Ready Signal Polarity Selection: 0: For SH series CPU, active low. For strapped SA1110 mode, the SRAM write shared with the SDRAM write. 1: For SH series CPU, active high. For strapped SA1110 mode, the SRAM write is separated from the SDRAM write. Note: This bit is determined by GPIO20 pins at reset.
5	VR	NEC Memory Map Selection: 0: MMIO located at 30MB (0x1E00000). 1: MMIO located at 62MB (0x3E00000).
4:3	extRDY	Extended RDY signal for SH4 system: 00: One clock wide. 01: Two clocks wide. 1X: CS control.
2:0	Bus	Host Bus Type Selection: 000: Hitachi SH3/SH4. 001: PCI. 010: Marvell Xscale. 110: NEC. Note: These bits are determined by GPIO[19:17] pins at reset.

System Memory Control

Read/Write MMIO_base + 0x000078

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res								Ex RW				Burst RW			CL RW
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Hold RW			Col RW		Size RW			APX RW	WPX RW	BX RW	RX RW	Delay RW			BL RW

Bit(s)	Name	Description
31:24	Res	These bits are reserved.
23:20	Ex	Extend the bus holding when the SM718 is a host bus master to access system SDRAM. The extension period starts to count down when the SM718 gets an asserted bus acknowledge signal from the CPU.

Bits	Extension	Bits	Extension
0000	No Extension	1000	128 HCLKs
0001	16 HCLKs	1001	144 HCLKs
0010	32 HCLKs	1010	160 HCLKs
0011	48 HCLKs	1011	176 HCLKs
0100	64 HCLKs	1100	192 HCLKs
0101	80 HCLKs	1101	208 HCLKs
0110	96 HCLKs	1110	224 HCLKs
0111	112 HCLKs	1111	240 HCLKs

19:17	Burst	System Memory Burst Length Selection: 000: 1 word. (default) 001: 2 words. 010: 4 words. 011: 8 words.
16	CL	System Memory CAS Latency Selection: 0: 2 clocks. (default) 1: 3 clocks.
15:13	Hold	Bus Hold Time Selection: 000: Hold bus until command FIFO is empty. (default) 001: Hold bus for 8 transactions. 010: Hold bus for 16 transactions. 011: Hold bus for 24 transactions. 100: Hold bus for 32 transactions.
12:11	Col	System Memory Column Size Selection: 00: 1024 words. 01: 512 words. 10: 256 words. (default)
10:8	Size	System Memory Size Selection: 000: 2MB. 001: 4MB. 100: 64MB. 101: 32MB. 110: 16MB.
7	APX	System Memory Active to Pre-charge Delay: 0: 6 clocks. 1: 7 clocks. (default)
6	WPX	System Memory Write to Pre-charge Delay: 0: 2 clocks. (default) 1: 1 clock.
5	BX	System Memory Bank Selection: 0: 4 banks. (default) 1: 2 banks.
4	RX	System Memory Reset Selection: 0: Reset. 1: Normal. (default)

3:1	Delay	Delay time to latch read data from external SDRAM controller: 000: No delay. (default) 001: Delay ½ ns. 010: Delay 1ns 011: Delay 1 ½ ns. 100: Delay 2ns. 101: Delay 2 ½ ns.
0	BL	CPU Master Burst Length Select: 0: Burst of 8. (default) 1: Burst of 1.

Scratch Data

Read/Write MMIO_base + 0x00006C

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Data R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data R/W															

Bit(s)	Name	Description
31:0	Data	Scratch Data.

4. PCI Configuration Space

4.1 Register Descriptions

The PCI specification defines the configuration space for auto-configuration (plug-and-play), and device and memory relocation.

Table 8 summarizes the PCI Configuration Space Registers.

Address	Type	Width	Reset Value	Register Name
0x00	R	32	0x0718126F	CSR00: Vendor ID and Device ID
0x04	R/W	32	0x02300000	CSR04: Command and Status
0x08	R	32	0x380000C0	CSR08: Revision ID and Class Code
0x0D	R	8	0x00	CSR0C: Latency Timer
0x10	R/W	32	0x00000000	CSR10: Linear Frame Buffer Base Address Register
0x14	R/W	32	0x00000000	CSR14: Base Address Register for Memory Map Address
0x18	R/W	32	0x00000000	CSR18: 64K VGA 0xA0000/0xB0000 Base Address
0x1C	R/W	32	0x00000000	CSR1C: 32K VGA 0xB8000 Base Address
0x20	R/W	32	0x00000000	CSR20: VGA I/O Ports 0x3Cx Base Address
0x24	R/W	32	0x00000000	CSR24: VGA I/O Ports 0x3Dx/0x3Bx Base Address
0x2C	R	32	0x00000000	CSR2C: Subsystem ID and Subsystem Vendor ID
0x30	R/W	32	0x00000000	CSR30: Expansion ROM Base Address
0x34	R	32	0x00000040	CSR34: Power Down Capability Pointer
0x3C	R/W	32	0x00000000	CSR3C: Interrupt Pin and Interrupt Line
0x40	R	32	0x06010001	CSR40: Power Down Capability Register
0x44	R/W	32	0x00000000	CSR44: Power Down Capability Data

Table 7: PCI Configuration Space Register Summary

Figure 24 lists the registers available in the PCI Configuration register space.

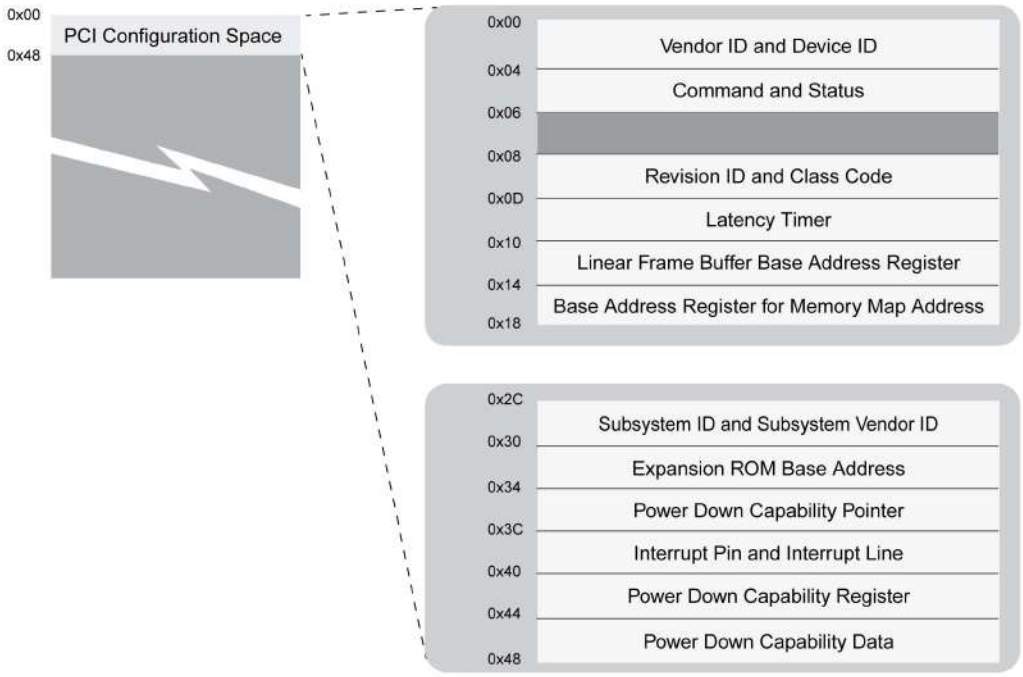


Figure 12: PCI Configuration Register Space

CSR00: Vendor ID and Device ID

Read Address 0x00

Power-on Default 0x0718126F

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Device ID R															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Vendor ID R															

This register specifies the device and vendor IDs.

Bit(s)	Name	Description
31:16	Device ID	These bits are hardwired to 0x0718 to identify the SM718 device.
15:0	Vendor ID	These bits are hardwired to 0x126F to identify the vendor as Silicon Motion®, Inc.

CSR04: Command and Status

Read/Write Address 0x04

Power-on Default 0x02300000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DPE R	Res		DTA R	Res	DEVSEL R		Res			66C R	NCD R	Res			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res										PSE R/W	MWR R/W	Res	PBM R/W	MS R/W	IO R

This register controls which types of PCI command cycles are supported by the SM718.

Notes: Reserved bits are read only.

Bit(s)	Name	Description
31	DPE	Data Parity Error Detected. 0: Correct. 1: Error detected.
30:29	Res	These bits are reserved.
28	DTA	Received Target Abort. 0: Correct. 1: Abort detected
27	Res	This bit is reserved.
26:25	DEVSEL	Timing Select Medium.
24:22	Res	These bits are reserved.
21	66C	66 MHz Capable.
20	NCD	New Capability Definition.
19:6	Res	This bit is reserved.
5	PSE	Palette Snooping Enable. 0: Disable. 1: Enable.
4	MWR	Memory Write and Invalidate Enable. 0: Disable. 1: Enable.
3	Res	This bit is reserved.
2	PBM	PCI Bus Master Enable.
1	MS	Memory Space Access Enable. 0: Disable. 1: Enable.
0	IO	I/O Space Access Enable. 0: Disable.

CSR08: Revision ID and Class Code

Read Address 0x08

Power-on Default 0x038000C0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Base Class Code R								Subclass Code R							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register Level Programming Interface R								Revision ID R							

This register specifies the silicon revision ID and the Class Code that the silicon supports.

Bit(s)	Name	Description
31:24	Base	Class Code 0x03 = For Video Controller
23:16	Subclass	Code 0x80 = Other Display Controller
15:8	Register	Level Programming Interface 0x00 = Hardwired setting
7:0	Revision ID	0xA0 = SM718

CSR0C: Latency Timer

Read Address 0x0D

Power-on Default 0x00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LT R								Reserved							

This register specifies the latency timer that the SM718 supports for burst master mode.

Bit(s)	Name	Description
31:16	Reserved	These bits are reserved.
15:8	LT	Latency Timer. The default for this field is 0x00.
7:0	Reserved	These bits are reserved.

CSR10: Linear Frame Buffer Base Address Register

Read/Write Address 0x10

Power-on Default 0x0000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Linear Addressing Memory Base R/W/R											Linear Frame Buffer Base Address R				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Linear Frame Buffer Base Address R															MB R

This register specifies the PCI configuration space for address relocation.

Notes: Reserved bits are read only.

Bit(s)	Name	Description
31:21	Linear Address Memory Base Address	Memory segment allocated within 64 MB boundary. • If 2 MB: **Bits 26:21** = FBA (Read/Write) • If 4 MB: **Bits 26:22** = FBA (Read/Write) **Bit 21** = 0b • If 8 MB: **Bits 26:23** = FBA (Read/Write) **Bits 22:21** = 00b (Read Only) • If 16 MB: **Bits 26:24** = FBA (Read/Write) **Bits 23:21** = 000b (Read Only) • If 32 MB: **Bit 26** = FBA (Read/Write) **Bits 24:21** = 0000b (Read Only) • If 64 MB: **Bit 26** = FBA (Read/Write) **Bits 25:21** = 00000b (Read Only)
20:1	Linear Frame Buffer Base Address	The default for this read-only field is 0x000000.
0	MB	Memory Base Read. The default for this bit is 0.

CSR14: Base Address Register for Memory Map Address

Read/Write Address 0x14

Power-on Default 0x0000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Memory Map Address Base Address R/W/R											Memory Map Address Base Address R				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Memory Map Address Base Address R															MB R

This register specifies the PCI configuration space for address relocation.

Notes: Reserved bits are read only.

Bit(s)	Name	Description
31:21	FBA	Memory Map Address Base Address. • If One Endian: **Bits [31:21]** = FBA (Read/Write) • If Big and Small Endian: **Bit [31:22]** = FBA (Read/Write) **Bit [21]** = 0b (Read Only)
20:1	ABA	Memory Map Address Base Address. The default for this read-only field is 0x000000.
0	MB	Memory Base. The default for this read-only bit is 0.

CSR18: 64K VGA 0xA0000/0xB0000 Base Address

Read/Write Address 0x18

Power-on Default 0x0000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
64K VGA BAR R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
64K VGA BAR R/W															

Bit(s)	Name	Description
31:0	64K VGA BAR	Memory segment allocated for 64K access of legacy VGA 0xA0000 or 0xB0000 memory area.

CSR1C: 32K VGA 0xB8000 Base Address

Read/Write Address 0x1C

Power-on Default 0x0000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
32K VGA BAR R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
32K VGA BAR R/W															

Bit(s)	Name	Description
31:0	32K VGA BAR	Memory segment allocated for 32K access of legacy VGA 0xB8000 memory area.

CSR20: VGA I/O Ports 0x3Cx Base Address

Read/Write Address 0x20

Power-on Default 0x0000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VGA 3Cx BAR R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VGA 3Cx BAR R/W															

Bit(s)	Name	Description
31:0	VGA 3Cx BAR	Memory segment allocated for 16 bytes access of legacy VGA I/O ports 0x3Cx memory area.

CSR24: VGA I/O Ports 0x3Dx/0x3Bx Base Address

Read/Write Address 0x24

Power-on Default 0x0000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VGA 3D/Bx BAR R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VGA 3D/Bx BAR R/W															

Bit(s)	Name	Description
31:0	VGA 3D/Bx BAR	Memory segment allocated for 16 bytes access of legacy VGA I/O ports 0x3Dx or 0x3Bx memory area.

CSR2C: Subsystem ID and Subsystem Vendor ID

Read Address 0x2C

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Subsystem ID R															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Subsystem Vendor ID R															

This register specifies both the Subsystem device ID and the Subsystem Vendor ID.

Bit(s)	Name	Description
31:16	Subsystem ID	This System ID is written by the system BIOS during POST.
15:0	Subsystem Vendor ID	This field contains the Subsystem Vendor ID.

CSR30: Expansion ROM Base Address

Read/Write Address 0x30

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ROM Base Address R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															BIOS R/W

This register specifies the expansion ROM base address.

Notes: Reserved bits are read only.

Bit(s)	Name	Description
31:16	ROM Base Address	Memory segment allocated for BIOS ROM in 64KB boundary [15:0].
15:1	Reserved	These bits are reserved.
0	BIOS Address Decode Enable	This bit is valid only if memory space access is enabled (CSR04 bit 1 = 1). 0: Disable. 1: Enable.

CSR34: Power Down Capability Pointer

Read Address 0x34

Power-on Default 0x00000040

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Power Down Capability Pointer															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Power Down Capability Pointer															

This register contains the address where PCI power down management registers are located.

Bit(s)	Name	Description
31:0	Power Down Capability Pointer	The Capability pointer contains the address where the PCI Power Down Management Register is located.

CSR3C: Interrupt Pin and Interrupt Line

Read/Write Address 0x3C

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Interrupt Pin R								Interrupt Line R/W							

This register specifies the PCI interrupt pin and interrupt line.

Bit(s)	Name	Description
31:16	Reserved	These bits are reserved.
15:8	Interrupt Pin	
7:0	Interrupt Line	

CSR40: Power Down Capability Register

Read Address 0x40

Power-on Default 0x06010001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PCI Power Down Management Capability (0x0601) R															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Next Capability Pointer Link List R								PCI Power Down Mgmt Capability (0x01) R							

This register contains the address for PCI power-down management capabilities.

Bit(s)	Name	Description
31:16	PCI Power Down Management Capability	Offset 2. This field is hardwired to 0x0601.
15:8	No More Extra Capability Pointer	This field is hardwired to 0x00.
7:0	PCI Power Down Management Capability ID	Offset 0. This field is hardwired to 0x01.

CSR44: Power Down Capability Data

Read/Write Address 0x44

Power-on Default 0x00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Data R								Reserved							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PCI Power Down Mgmt Control/Status R/W														PDS R/W	

This register contains the address for PCI power-down management Control, Status and Data.

Bit(s)	Name	Description
31:24	Data	Offset 7. This data field is read-only.
23:16	Reserved	Offset 6.
15:2	PCI Power Down Management Control/Status	Offset 4.
1:0	PDS	Power Down Management Control and Status. 00: Power Down Management State D0. 01: Power Down Management State D1. 10: Power Down Management State D2. 11: Power Down Management State D3.

5. Drawing Engine

5.1 Functional Overview

The SM718's Drawing Engine is designed to accelerate Microsoft's DirectDraw and Direct3D applications. The engine contains a 3-operand ALU with 256 raster operations, source and destination FIFOs, as well as a host data FIFO. The drawing engine pipeline allows single cycle operations and runs at the memory clock speed.

The Drawing Engine includes several key functions to achieve the high GUI performance. The device supports color expansion with packed mono font, color pattern fill, host BLT, stretch BLT, short stroke, line draw, and others. Dedicated pathways are designed to transfer data between the host interface (HIF) bus and the Drawing Engine, and memory interface (MIF) bus and the Drawing Engine. In addition, the Drawing Engine supports rotation BIBLT for any block size, and automatic self activate rotation BLIT. This feature allows conversion between landscape and portrait display without the need for special software drivers.

5.2 Programmer's Model

The Drawing Engine supports various drawing functions, including Bresenham line draw, short stroke line draw, BITBLT, rectangle fill, HOSTBLT, Rotation Blit, and others. Hardware clipping is supported by 4 registers, DPR2C-DPR32, which define a rectangular clipping area.

The drawing engine supports two types of addressing formats for its source and destination locations. In XY addressing mode, the location is specified in X-Y coordinates, where the upper left corner of the screen is defined to be (0,0). In linear addressing mode, the location is specified based on its position in the display memory sequentially from the first pixel of the visible data. The addressing mode is set by the Addressing field of the 2D Stretch & Format register. The Command field of the 2D Control register selects other drawing functions, for example, Bresenham line draw, host write and short stroke.

5.3 Register Descriptions

All Drawing Engine control registers can be accessed via memory mapping. The address is at DP_Base + XXXh, where DP_Base is at PCI graphics base address + 4MB + 32K. Figure 25 shows how this 64kB region in the MMIO space is laid out. It controls the Drawing Engine registers.

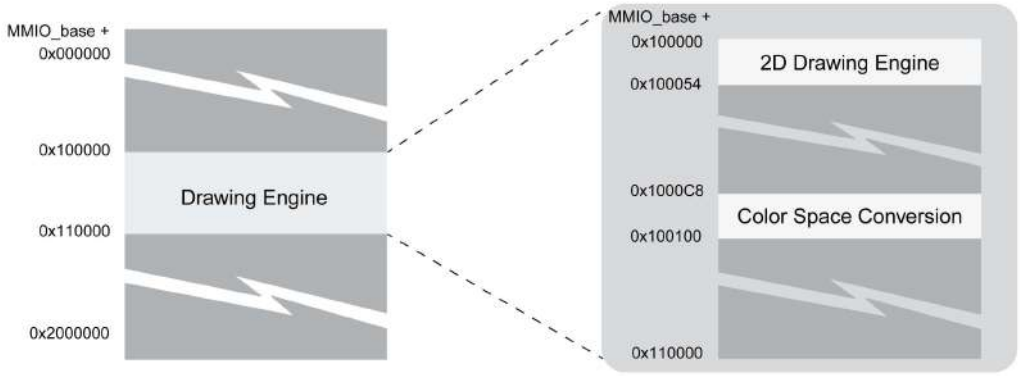


Figure 13: Bus Signal Level

Table 9 summarizes the Drawing Engine registers.

Offset from MMIO_base[1]	Type	Width	Reset Value	Register Name
0x100000	R/W	32	0x00000000	2D Source
0x100004	R/W	32	0x00000000	2D Destination
0x100008	R/W	32	0x00000000	2D Dimension
0x10000C	R/W	32	0x00000000	2D Control
0x100010	R/W	32	0x00000000	2D Pitch
0x100014	R/W	32	0x00000000	2D Foreground
0x100018	R/W	32	0x00000000	2D Background
0x10001C	R/W	32	0x00000000	2D Stretch & Format
0x100020	R/W	32	0x00000000	2D Color Compare
0x100024	R/W	32	0x00000000	2D Color Compare Mask
0x100028	R/W	32	0x00000000	2D Mask
0x10002C	R/W	32	0x00000000	2D Clip TL
0x100030	R/W	32	0x00000000	2D Clip BR
0x100034	R/W	32	0x00000000	2D Mono Pattern Low
0x100038	R/W	32	0x00000000	2D Mono Pattern High
0x10003C	R/W	32	0x00000000	2D Window Width

Offset from MMIO_base[1]	Type	Width	Reset Value	Register Name
0x100040	R/W	32	0x00000000	2D Source Base
0x100044	R/W	32	0x00000000	2D Destination Base
0x100048	R/W	32	0x00000000	2D Alpha
0x10004C	R/W	32	0x00000000	2D Wrap
0x100050	R/W	32	0x00000000	2D Status
0x1000C8	R/W	32	0x00000000	CSC Source Base
0x1000CC	R/W	32	0x00000000	CSC Constants
0x1000D0	R/W	32	0x00000000	CSC Source X
0x1000D4	R/W	32	0x00000000	CSC Source Y
0x1000D8	R/W	32	0x00000000	CSC U Source Base in YUV420
0x1000DC	R/W	32	0x00000000	CSC V Source Base in YUV420
0x1000E0	R/W	32	0x00000000	CSC Source Dimension
0x1000E4	R/W	32	0x00000000	CSC Source Pitch
0x1000E8	R/W	32	0x00000000	CSC Destination
0x1000EC	R/W	32	0x00000000	CSC Destination Dimension
0x1000F0	R/W	32	0x00000000	CSC Destination Pitch
0x1000F4	R/W	32	0x00000000	CSC Scale Factor
0x1000F8	R/W	32	0x00000000	CSC Destination Base
0x1000FC	R/W	32	0x00000000	CSC Control

Table 8: Drawing Engine Register Summary

1. Refer to Table 5 on page 27 for MMIO_base values depending on the CPU.

5.3.1 2D Drawing Engine Registers

The 2D Drawing Engine register space is shown in Figure 26.

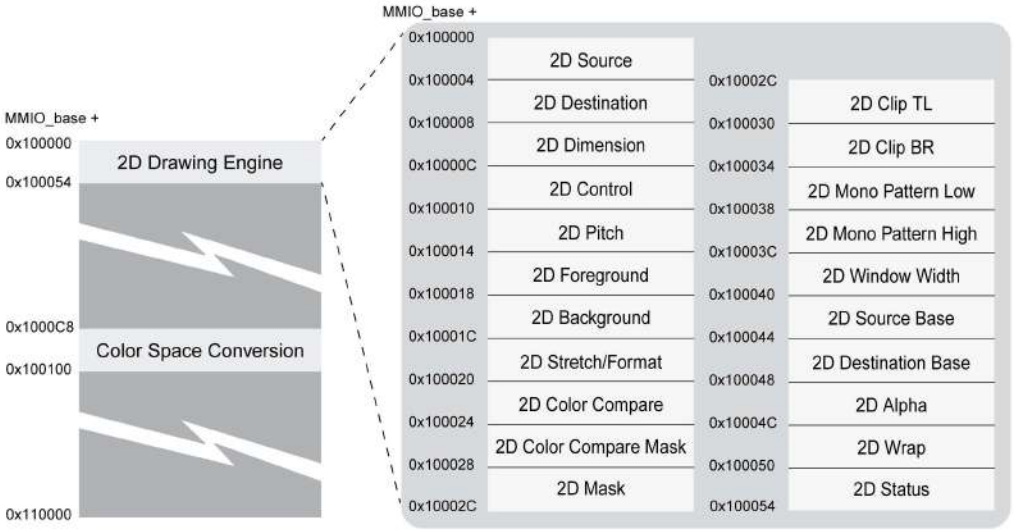


Figure 14: 2D Drawing Register Space

2D Source

Read/Write MMIO_base + 0x100000

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
W R/W	Res	X_K1 R/W													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Y_K2 R/W															

Bit(s)	Name	Description
31	W	Wrap Control. 0: Disable. 1: Enable.
30	Res	This bit is reserved.
29:16	X_K1	In XY addressing mode, the 12-bit X-coordinate of source (bits 27:16). In linear addressing mode, the lower 12-bits of the source address (bits 27:16). In host write mode, the 5-bit mono source for alignment (bits 20:16) In Bresenham line drawing mode, the 14-bit K1 constant for line drawing (bits 29:16): K1 = 2 * min(|dx|, |dy|).
15:0	Y_K2	In XY addressing mode, the 12-bit Y-coordinate of source (bits 11:0). In linear addressing mode, the higher 12-bits of the source address (bits 11:0). In host write mode, this field is not used. In Bresenham line drawing mode, the 14-bit K2 constant for line drawing (bits 13:0): K2 = 2 * (min(|dx|, |dy|) – max(|dx|, |dy|).

2D Destination

Read/Write MMIO_base + 0x100004

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
W R/W	Reserved		X R/W												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Y R/W															

Bit(s)	Name	Description
31	W	Wrap Control. 0: Disable. 1: Enable.
30:29	Reserved	These bits are reserved.
28:16	X	In XY addressing mode, the 12-bit X-coordinate of source (bits 27:16). In linear addressing mode, the lower 12-bits of the source address (bits 27:16). In Bresenham mode, the vector X start address (bits 27:16).
15:0	Y	In XY addressing mode, the 12-bit Y-coordinate of source (bits 11:0). In linear addressing mode, the higher 12-bits of the source address (bits 11:0). In Bresenham mode, the vector Y start address (bits 11:0)

2D Dimension

Read/Write MMIO_base + 0x100008

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			X_VL R/W												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Y_ET R/W															

Bit(s)	Name	Description
31:29	Reserved	These bits are reserved.
28:16	X_VL	In XY addressing mode, the X dimension in pixels. In Bresenham mode, the vector length. In short stroke mode, horizontal length
15:0	Y_ET	In XY addressing mode, the Y dimension in pixels. In Bresenham mode, the vector error term given by: ET = 2 * min(|dx|, |dy|) – max(|dx|, |dy|) if start X > end X, or ET = 2 * min(|dx|, |dy|) – max(|dx|, |dy|) – 1 if start X <= end X. In short stroke mode, the non-horizontal length.

2D Control

Read/Write MMIO_base + 0x10000C

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	P R/W	U R/W	Q R/W	D R/W	M R/W	X R/W	Y R/W	St R/W	H R/W	LP R/W	Command R/W				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R R/W	R2 R/W	Mono R/W		RR R/W	TM R/W	TS R/W	T R/W	ROP R/W							

Bit(s)	Name	Description
31	S	Drawing Engine Status. 0: Stop. 1: Start.
30	P	Pattern Select. 0: Monochrome. 1: Color.
29	U	Update Destination X after Operation Control. 0: Disable. 1: Enable.
28	Q	Quick Start Control. Quick start will start the drawing engine after the X field in the 2D Dimension register has been written to. 0: Disable. 1: Enable.
27	D	Direction Control for Operation. 0: Left to right. 1: Right to left.
26	M	Major Axis for Line Drawing. 0: X axis. 1: Y axis.
25	X	X Step Control for Line Drawing. 0: Positive. 1: Negative.
24	Y	Y Step Control for Line Drawing. 0: Positive. 1: Negative.
23	St	Stretch in Y Direction Control. 0: Disable. 1: Enable.
22	H	Host BitBlt Select. 0: Color. 1: Monochrome.
21	LP	Draw Last Pixel Control for Line Drawing. 0: Don't draw last pixel. 1: Draw last pixel.
20:16	Command	Command Code. 00000 BitBlt; 00001 Rectangle Fill; 00010 De-Tile; 00011 Trapezoid Fill; 00100 Alpha Blend; 00101 RLE Strip; 00110 Short Stroke; 00111 Line Draw; 01000 Host Write; 01001 Host Read; 01010 Host Write bottom-to-top; 01011 Rotate; 01100 Font; 01111 Texture Load

Bit(s)	Name	Description
15	R	ROP Control. 0: ROP3. 1: ROP2.
14	R2	ROP2 Control. 0: ROP2 source is bitmap. 1: ROP2 source is pattern.
13:12	Mono	Monochrome Data Pack Control. 00: Not packed. 01: Packed at 8-bit. 10: Packed at 16-bit.
11	RR	Repeat Rotation Control. Only valid when Command is 01011 (Rotate). When enabled, the drawing engine is started again at every vertical sync. 0: Disable. 1: Enable.
10	TM	Transparency Match Select. 0: Matching pixel is opaque. 1: Matching pixel is transparent.
9	TS	Transparency Select. 0: Transparency is controlled by source. 1: Transparency is controlled by destination.
8	T	Transparency Control. 0: Disabled. 1: Enabled.
7:0	ROP	ROP2 or ROP3 code (see tables below).

Binary Raster Operations (ROP2)

Each raster-operation code represents a Boolean operation in which the values of the pixels in the selected pen and the destination bitmap are combined. The operands used in these operations are:

- P = selected pen
- D = destination bitmap

		Bit[2:0]							
		0	1	2	3	4	5	6	7
Bit 3	0	0	~(D+S)	D*~S	~S	~D*S	~D	D^S	(~D*S)
	1	D*S	(~D^S)	D	D+~S	S	~D+S	D+S	1

Ternary Raster Operations (ROP3)

Each raster-operation code represents a Boolean operation in which the values of the pixels in the source, the selected brush, and the destination are combined.
The operands and operands are:

- D = destination bitmap
- P = selected brush (pattern)
- S = source bitmap
- a = bitwise AND
- n = bitwise NOT (inverse)
- o = bitwise OR
- x = bitwise XOR (exclusive OR)

All Boolean operations are presented in reverse Polish notation. For example, the following operation replaces the pixel values in the destination bitmap with a combination of the pixel values of the source and brush:

PSo = (P+S)

The following operation combines the values of the pixels in the source and brush with the pixel values of the destination bitmap (there are alternative spellings of the same function, so although a particular spelling may not be in the list, an equivalent form would be):

DPSoo = (P+S) + D

The SM718 supports all the 256 operations. However, the pattern must be monochrome.

Table 10 lists all the possible ROP3 operations.

bit [3:0]	Bits [7:4] 0	1	2	3	4	5	6	7
0	0	PDSona	DPSnaa	PSna	PSDnaa	PDna	PDSxa	PDSana
1	DPSoon	DSon	SDPxon	SDPnaon	DPSxon	DSPnaon	DSPDSaoxxn	SSDxPDxaxn
2	DPSona	SDPxnon	DSna	SDPSoox	SDxPDxa	DPSDaox	DSPDoax	SDPSxox
3	PSon	SDPaon	SPDnaon	Sn	SPDSanaxn	SPDSxaxn	SDPnox	SDPnoan
4	SDPona	DPSxnon	SPxDSxa	SPDSaox	SDna	DPSonon	SDPSoax	DSPDxox
5	DPon	DPSaon	PDSPanaxn	SPDSxnox	DPSnaon	Dn	DSPnox	DSPnoan
6	PDSxnon	PSDPSanaxx	SDPSaox	SDPox	DSPDaox	DPSox	DSx	SDPSnaox
7	PDSaon	SSPxDSxaxn	SDPSxnox	SDPoan	PSDPxaxn	DPSoan	SDPSonox	DSan
8	SDPnaa	SPxPDxa	DPSxa	PSDPoax	SDPxa	PDSPoax	DSPDSonoxxn	PDSax
9	PDSxon	SDPSanaxn	PSDPSaoxxn	SPDnox	PDSPDaoxxn	DPSnox	PDSxxn	DSPDSoaxxn
A	DPna	PDSPaox	DPSana	SPDSxox	DPSDoax	DPx	DPSax	DPSDnoax
B	PSDnaon	SDPSxaxn	SSPxPDxaxn	SPDnoan	PDSnox	DPSDonox	PSDPSoaxxn	SDPxnan
C	SPna	PSDPaox	SPDSoax	PSx	SDPana	DPSDxox	SDPax	SPDSnoax
D	PDSnaon	DSPDxaxn	PSDnox	SPDSonox	SSPxDSxoxn	DPSnoan	PDSPDoaxxn	DPSxnan
E	PDSonon	PDSox	PSDPxox	SPDSnaox	PDSPxox	DPSDnaox	SDPSnoax	SPxDSxo
F	Pn	PDSoan	PSDnoan	PSan	PDSnoan	DPan	PDSxnan	DPSaan

bit [3:0]	Bits [7:4] 8	9	A	B	C	D	E	F
0	DPSaa	PDSxna	DPa	PDSnoa	PSa	PSDnoa	PDSoa	P
1	SPxDSxon	SDPSnoaxn	PDSPnaoxn	PDSPxoxn	SPDSnaoxn	PSDPxoxn	PDSoxn	PDSono
2	DPSxna	DPSDPoaxx	DPSnoa	SSPxDSxox	SPDSonoxn	PDSnax	DSPDxax	PDSnao
3	SPDSnoaxn	SPDaxn	DPSDxoxn	SDPanan	PSxn	SPDSoaxn	PSDPaoxn	PSno
4	SDPxna	PSDPSoaxx	PDSPonoxn	PSDnax	SPDnoa	SSPxPDxax	SDPSxax	PSDnao
5	PDSPnoaxn	DPSaxn	PDxn	DPSDoaxn	SPDSxoxn	DPSanan	PDSPaoxn	PDno
6	DSPDSoaxx	DPSxx	DSPnax	DPSDPaoxx	SDPnax	PSDPSaoxx	SDPSanax	PDSxo
7	PDSaxn	PSDPSonoxx	PDSPoaxn	SDPxan	PSDPoaxn	DPSxan	SPxPDxan	PDSano
8	DSa	SDPSonoxn	DPSoa	PSDPxax	SDPoa	PDSPxax	SSPxDSxax	PDSao
9	SDPSnaoxn	DSxn	DPSoxn	DSPDaoxn	SPDoxn	SDPSaoxn	DSPDSanaxxn	PDSxno
A	DSPnoa	DPSnax	D	DPSnao	DPSDxax	DPSDanax	DPSao	DPo
B	DSPDxoxn	SDPSoaxn	DPSono	DSno	SPDSaoxn	SPxDSxan	DPSxno	DPSnoo
C	SDPnoa	SPDnax	SPDSxax	SPDSanax	S	SPDnao	SDPao	PSo
D	SDPSxoxn	DSPDoaxn	DPSDaoxn	SDxPDxan	SDPono	SDno	SDPxno	PSDnoo
E	SSDxPDxax	DSPDSaoxx	DSPnao	DPSxo	SDPnao	SDPxo	DSo	DPSoo
F	PDSanan	PDSxan	DPno	DPSano	SPno	SDPano	SDPnoo	1

Table 9: ROP3 Operations

Rotate Command

For the Rotate command, the X and Y bits determine the rotation angle. For the Short Stroke command, the D, M, X, and Y bits determine the direction of the vector.

X	Y	Rotation Direction
0	0	0 degrees
0	1	270 degrees
1	0	90 degrees
1	1	180 degrees

D	M	X	Y	Vector Direction
0	0	0	0	225 degrees
0	0	0	1	135 degrees
0	0	1	0	315 degrees
0	0	1	1	45 degrees
0	1	0	0	270 degrees
0	1	0	1	90 degrees
1	0	0	0	180 degrees
1	0	1	0	0 degrees

2D Pitch

Read/Write MMIO_base + 0x100010

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			Destination R/W												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			Source R/W												

Bit(s)	Name	Description
31:29	Reserved	These bits are reserved.
28:16	Destination	Pitch of destination specified in pixels.
15:13	Reserved	These bits are reserved.
12:0	Source	Pitch of source specified in pixels.

2D Foreground

Read/Write MMIO_base + 0x100014

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Foreground R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Foreground R/W															

Bit(s)	Name	Description
31:0	Foreground	Bits Per Pixel: Foreground Color 8: Index color. 16: RGB565 color. 32: RGBx888 color.

2D Background

Read/Write MMIO_base + 0x100018

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Background R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Background R/W															

Bit(s)	Name	Description
31:0	Background	Bits Per Pixel: Background Color 8: Index color. 16: RGB565 color. 32: RGBx888 color.

In monochrome transparency, the Background must be programmed with the invert of the Foreground pixels in the 2D Foreground register.

2D Stretch & Format

Read/Write MMIO_base + 0x10001C

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	XY R/W	Y R/W			Res	X R/W			Res	Format R/W		Addressing R/W			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				Height R/W											

Bit(s)	Name	Description
31	Res	This bit is reserved.
30	XY	Pattern XY Select. 0: Only use X and Y fields in linear mode. 1: Use X and Y fields in XY mode.
29:27	Y	Pattern Y Origin. This field is only valid in linear mode (Addressing = 1111) or when XY is enabled.
26	Res	This bit is reserved.
25:23	X	Pattern X Origin. This field is only valid in linear mode (Addressing = 1111) or when XY is enabled.
22	Res	This bit is reserved.
21:20	Format	Pixel Format. 00: 8-bits per pixel. 01: 16-bits per pixel. 10: 32-bits per pixel.
19:16	Addressing	Addressing Mode. 0000: XY mode. 1111: Linear mode.
15:12	Res	These bits are reserved.
11:0	Height.	Source height when stretch is enabled.

2D Color Compare

Read/Write MMIO_base + 0x100020

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								Color R/W							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Color R/W															

Bit(s)	Name	Description
31:24	Reserved	These bits are reserved.
23:0	Color	Bits Per Pixel / Color Compare 8 / Index color. 16 / RGB565 color. 32 / RGB888 color.

In monochrome transparency, the Color must be programmed with the same value as the Foreground pixels in the 2D Foreground register.

2D Color Compare Mask

Read/Write MMIO_base + 0x100024

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								Mask R/W							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mask R/W															

Bit(s)	Name	Description
31:24	Reserved	These bits are reserved.
23:0	Mask	Mask Bits for Color Compare. 0: Color compare always matches. 1: Color compare only matches when bits are equal.

2D Mask

Read/Write MMIO_base + 0x100028

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Byte R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit R/W															

Bit(s)	Name	Description
31:16	Byte	Byte mask for each of the 16 bytes on the 128-bit memory bus. 0: Disable write. 1: Enable write.
15:0	Bit	Bit mask for 8- and 16-bits per pixel modes. 0: Disable write. 1: Enable write.

2D Clip TL

Read/Write MMIO_base + 0x10002C

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Top R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		E R/W	S R/W	Left R/W											

Bit(s)	Name	Description
31:16	Top	Top Coordinate of Clipping Rectangle.
15:14	Reserved	These bits are reserved.
13	E	Clipping Control. 0: Disable. 1: Enable.
12	S	Clipping Select Control. 0: Write outside clipping rectangle disabled. 1: Write inside clipping rectangle disabled.
11:0	Left	Left Coordinate of Clipping Rectangle.

2D Clip BR

Read/Write MMIO_base + 0x100030

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bottom R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			Right R/W												

Bit(s)	Name	Description
31:16	Bottom	Bottom Coordinate of Clipping Rectangle.
15:13	Reserved	These bits are reserved.
12:0	Right	Right Coordinate of Clipping Rectangle.

2D Mono Pattern Low

Read/Write MMIO_base + 0x100034

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Pattern R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Pattern R/W															

Bit(s)	Name	Description
31:0	Pattern	Bits [31:0] of monochrome pattern.

2D Mono Pattern High

Read/Write MMIO_base + 0x100038

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Pattern R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Pattern R/W															

Bit(s)	Name	Description
31:0	Pattern	Bits [63:32] of monochrome pattern.

2D Window Width

Read/Write MMIO_base + 0x10003C

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			Destination R/W												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			Source R/W												

Bit(s)	Name	Description
31:29	Reserved	These bits are reserved.
28:16	Destination	Width of destination window specified in pixels.
15:13	Reserved	These bits are reserved.
12:0	Source	Width of source window specified in pixels.

2D Source Base

Read/Write MMIO_base + 0x100040

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				Ext R/W	CS R/W	Address R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address R/W												0000			

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:4	Address	Memory address of source window with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

2D Destination Base

Read/Write MMIO_base + 0x100044

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				Ext R/W	CS R/W	Address R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address R/W												0000			

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:4	Address	Memory address of destination window with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

2D Alpha

Read/Write MMIO_base + 0x100048

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								Alpha R/W							

Bit(s)	Name	Description
31:8	Reserved	These bits are reserved.
7:0	Alpha	Alpha Value for Alpha Blend.

2D Wrap – Width and Height

Read/Write MMIO_base + 0x10004C

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Width R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Height R/W															

Bit(s)	Name	Description
31:16	Width	Horizontal pitch (H_Pitch) in pixels.
15:0	Height	Vertical pitch (V_Pitch) in lines.

2D Status

Read/Write MMIO_base + 0x100050

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														CSC R/W	2D R/W

Bit(s)	Name	Description
31:2	Reserved	These bits are reserved.
1	CSC	Color Space Conversion Interrupt Status. Write a 0 into this field to clear the interrupt status. 0: CSC not active or job not done. 1: CSC interrupt.
0	2D	2D Engine Interrupt Status. Write a 0 into this field to clear the interrupt status. 0: 2D not active or job not done. 1: 2D interrupt.

5.3.2 *Color Space Conversion Registers*

The Color Space Conversion register space is shown in Figure 27.

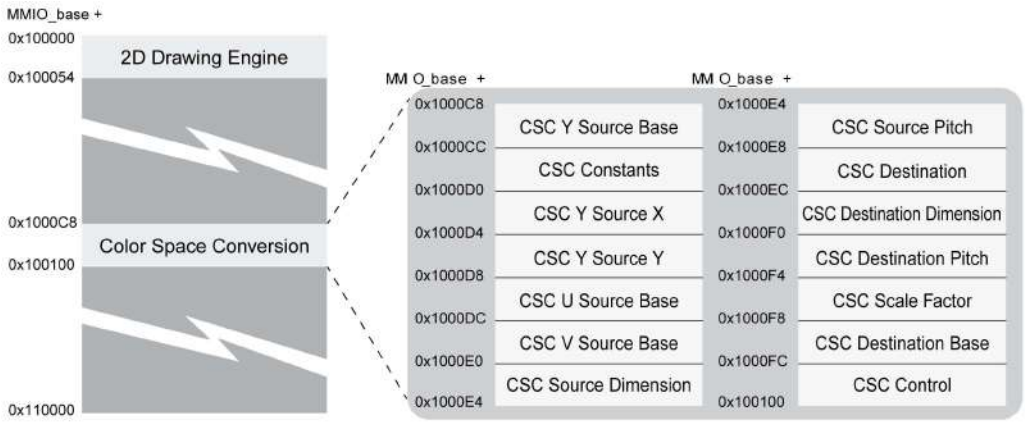


Figure 15: Color Space Conversion Register Space

CSC Source Base (Y Source Base in YUV420)

Read/Write MMIO_base + 0x1000C8

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				Ext R/W	CS R/W	Address R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address R/W												0000			

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:4	Address	Memory Address of Source Base with 128-bit Alignment. Memory Address of Y Source Base in YUV420 with 128-bit Alignment.
3:0	0000	These bits are hardwired to zeros.

CSC Constants

Read/Write MMIO_base + 0x1000CC

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Y R/W								R R/W							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
G R/W								B R/W							

Bit(s)	Name	Description
31:24	Y	Y Conversion Constant (luminosity).
23:16	R	Red Conversion Constant.
15:8	G	Green Conversion Constant.
7:0	B	B Blue Conversion Constant.

CSC Source X

Read/Write MMIO_base + 0x1000D0

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				X_I R/W											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X_F R/W													Reserved		

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27:16	X_I	Integer Part of Starting X-coordinate of Source.
15:3	X_F	Fractional Part of Starting X-coordinate of Source.
2:0	Reserved	These bits are reserved.

CSC Source Y

Read/Write MMIO_base + 0x1000D4

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				Y_I R/W											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Y_F R/W													Reserved		

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27:16	Y_I	Integer Part of Starting Y-coordinate of Source.
15:3	Y_F	Fractional Part of Starting Y-coordinate of Source.
2:0	Reserved	These bits are reserved.

CSC U Source Base in YUV420

Read/Write MMIO_base + 0x1000D8

Power-on Default 0x00000000

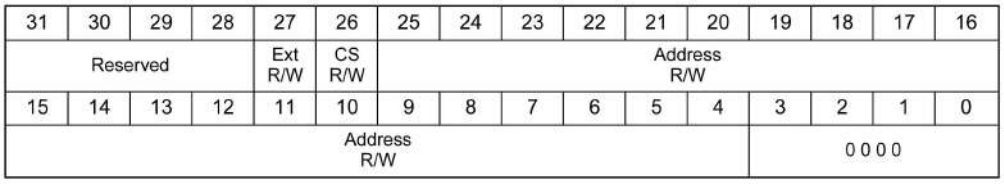
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				Ext R/W	CS R/W	Address R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address R/W												0000			

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:4	Address	Memory Address of U Source Base in YUV420 with 128-bit Alignment.
3:0	0000	These bits are hardwired to zeros.

CSC V Source Base in YUV420

Read/Write MMIO_base + 0x1000DC

Power-on Default 0x00000000

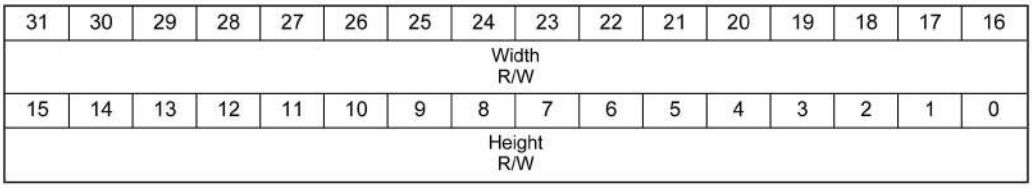


Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27	Ext	Ext Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:4	Address	Memory Address of V Source Base in YUV420 with 128-bit Alignment.
3:0	0000	These bits are hardwired to zeros.

CSC Source Dimension

Read/Write MMIO_base + 0x1000E0

Power-on Default 0x00000000



Bit(s)	Name	Description
31:16	Width	Width of Source in Pixels.
15:0	Height	Height of Source in Lines.

CSC Source Pitch

Read/Write MMIO_base + 0x1000E4

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Y R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UV R/W															

Bit(s)	Name	Description
31:16	Y	Pitch of Source specified in bytes ÷ 16. Pitch of Y Source in YUV420 specified in bytes ÷ 16.
15:0	UV	Pitch of U or V Source in YUV420 specified in bytes ÷ 16.

CSC Destination

Read/Write MMIO_base + 0x1000E8

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
W R/W	Reserved			X R/W											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				Y R/W											

Bit(s)	Name	Description
31	W	Wrap Control. 0: Disable. 1: Enable.
30:28	Reserved	These bits are reserved.
27:16	X	X-coordinate of Destination.
15:12	Reserved	These bits are reserved.
11:0	Y	Y-coordinate of Destination.

CSC Destination Dimension

Read/Write MMIO_base + 0x1000EC

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Width R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Height R/W															

Bit(s)	Name	Description
31:16	Width	Width of Destination in Pixels.
15:0	Height	Height of Destination in Lines.

CSC Destination Pitch

Read/Write MMIO_base + 0x1000F0

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
X R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Y R/W															

Bit(s)	Name	Description
31:16	X	Horizontal Pitch of Destination specified in Bytes ÷ 16.
15:0	Y	Vertical Pitch of Destination specified in Lines.

CSC Scale Factor

Read/Write MMIO_base + 0x1000F4

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
X R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Y R/W															

Bit(s)	Name	Description
31:16	X	Horizontal scale factor specified in 3.13 format. Scale factor = $2^{13} * (Width_S - 1) / (Width_D - 1)$.
15:0	Y	Vertical scale factor specified in 3.13 format. Scale factor = $2^{13} * (Height_S - 1) / (Height_D - 1)$.

CSC Destination Base

Read/Write MMIO_base + 0x1000F8

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				Ext R/W	CS R/W	Address R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address R/W												0000			

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:4	Address	Memory Address of Destination Window with 128-bit Alignment.
3:0	0000	These bits are hardwired to zeros.

CSC Control

Read/Write MMIO_base + 0x1000FC

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	$Format_S$ R/W			$Format_D$ R/W		H R/W	V R/W	B R/W	Reserved						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit(s)	Name	Description
31	S	Color Space Conversion Control. 0: Stop. 1: Start.
30:28	$Format_S$	Source Pixel Format. 000 YUV422 / 100 Reserved 001 Reserved / 101 Reserved 010 YUV420 / 110 RGB565 011 Reserved / 111 RGB888
27:26	$Format_D$	Destination Pixel Format. 00: RGB565. 01: RGBx888.
25	H	Horizontal Linear Filter Control. 0: Disable. 1: Enable.
24	V	Vertical Linear Filter Control. 0: Disable. 1: Enable.
23	B	Byte Order for YUV422. 0 YUYV 1 UYVY
22:0	Reserved	These bits are reserved.

6. Display Controller

6.1 Programmer's Model

The SM718 integrates a concurrent video processor to control LCD display. Some of the features are:

- Background graphic supports from 4-bit index color, 8-bit index color, 16-bit direct color, and 32-bit direct color.
  Background graphic can be programmed to pan to the left/right and to up/down automatically according to number of VSYNC.
- Support 1 independent video surface using hardware scaling for any size of video windows at any location of the screen display and using hardware YUV to RGB color space conversion.
- Support 1 Alpha blend surface at any location of the screen display. It can use as hardware cursor or popup icon or sub picture for the video. Data format is 4-bit alpha and 4-bit color.
- The LCD module manages data flow and generate timing to select LCD display. It provides support for 18-bit, 24-bit, 36-bit panels up to 1920x1440.

The Video Processor Control Registers specify the control registers for Video Processor. The Video Processor Control Registers can only be accessed through memory-mapping.

6.2 Register Descriptions

Table 11 summarizes the Display Controller registers.

Offset from MMIO_base[1]	Type	Width	Reset Value[2]	Register Name
Primary Graphics Control				
0x080000	R/W	32	0x00010000	Primary Display Control
0x080004	R/W	32	Undefined	Primary Display Panning Control
0x080008	R/W	32	Undefined	Primary Display Color Key
0x08000C	R/W	32	Undefined	Primary Display FB Address
0x080010	R/W	32	Undefined	Primary Display FB Offset/Window Width
0x080014	R/W	32	Undefined	Primary Display FB Width
0x080018	R/W	32	Undefined	Primary Display FB Height
0x08001C	R/W	32	Undefined	Primary Display Plane TL Location
0x080020	R/W	32	Undefined	Primary Display Plane BR Location
0x080024	R/W	32	Undefined	Primary Display Horizontal Total
0x080028	R/W	32	Undefined	Primary Display Horizontal Sync
0x08002C	R/W	32	Undefined	Primary Display Vertical Total
0x080030	R/W	32	Undefined	Primary Display Vertical Sync
0x080034	R	32	0b0000.0000.0000.0000. 0000.0XXX.XXXX.XXXX	Primary Display Current Line
Video Control				
0x080040	R/W	32	0b0000.0000.0000.0001. X000.0000.0000.0000	Video Display Control
0x080044	R/W	32	Undefined	Video FB 0 Address
0x080048	R/W	32	Undefined	Video FB Width
0x08004C	R/W	32	Undefined	Video FB 0 Last Address
0x080050	R/W	32	Undefined	Video Plane TL Location
0x080054	R/W	32	Undefined	Video Plane BR Location
0x080058	R/W	32	0x00000000	Video Scale
0x08005C	R/W	32	0x00000000	Video Initial Scale
0x080060	R/W	32	0x00EDEDED	Video YUV Constants
0x080064	R/W	32	Undefined	Video FB 1 Address
0x080068	R/W	32	Undefined	Video FB 1 Last Address

Offset from MMIO_base[1]	Type	Width	Reset Value[2]	Register Name
Video Alpha Control				
0x080080	R/W	32	0x00000000	Video Alpha Display Control
0x080084	R/W	32	Undefined	Video Alpha FB Address
0x080088	R/W	32	Undefined	Video Alpha FB Offset/Window Width
0x08008C	R/W	32	Undefined	Video Alpha FB Last Address
0x080090	R/W	32	Undefined	Video Alpha Plane TL Location
0x080094	R/W	32	Undefined	Video Alpha Plane BR Location
0x080098	R/W	32	0x00000000	Video Alpha Scale
0x08009C	R/W	32	0x00000000	Video Alpha Initial Scale
0x0800A0	R/W	32	Undefined	Video Alpha Chroma Key
0x0800A4 – 0x0800C0	R/W	32	Undefined	Video Alpha Color Lookup
Primary Display Cursor Control				
0x0800F0	R/W	32	Undefined	Primary Display HWC Address
0x0800F4	R/W	32	Undefined	Primary Display HWC Location
0x0800F8	R/W	32	Undefined	Primary Display HWC Color 1 & 2
0x0800FC	R/W	32	Undefined	Primary Display HWC Color 3
0x080100	R/W	32	0x00010000	Alpha Display Control
0x080104	R/W	32	Undefined	Alpha FB Address
0x080108	R/W	32	Undefined	Alpha FB Offset/Window Width
0x08010C	R/W	32	Undefined	Alpha Plane TL Location
0x080110	R/W	32	Undefined	Alpha Plane BR Location
0x080114	R/W	32	Undefined	Alpha Chroma Key
0x080118 – 0x080134	R/W	32	Undefined	Alpha Color Lookup
Secondary Graphics Control				
0x080200	R/W	32	0x00010000	Secondary Display Control
0x080204	R/W	32	Undefined	Secondary Display FB Address
0x080208	R/W	32	Undefined	Secondary Display FB Offset/Window Width
0x08020C	R/W	32	Undefined	Secondary Display Horizontal Total
0x080210	R/W	32	Undefined	Secondary Display Horizontal Sync
0x080214	R/W	32	Undefined	Secondary Display Vertical Total

Offset from MMIO_base[1]	Type	Width	Reset Value[2]	Register Name
0x080218	R/W	32	Undefined	Secondary Display Vertical Sync
0x08021C	R/W	32	Undefined	Secondary Display Signature Analyzer
0x080220	R	32	0b0000.0000.0000.0000. 0000.0XXX.XXXX.XXXX	Secondary Display Current Line
0x080224	R/W	32	0b0000.0000.XXXX.XXXX. XXXX.XXXX.XXXX.XXXX	Secondary Display Monitor Detect
Secondary Display Cursor Control				
0x080230	R/W	32	Undefined	Secondary Display HWC Address
0x080234	R/W	32	Undefined	Secondary Display HWC Location
0x080238	R/W	32	Undefined	Secondary Display HWC Color 1 & 2
0x08023C	R/W	32	Undefined	Secondary Display HWC Color 3
Palette RAM				
0x080400 – 0x0807FC	R/W	32	Undefined	Primary Display Palette RAM
0x080800 – 0x080BFC	R/W	32	Undefined	Video Palette RAM
0x080C00 – 0x080FFC	R/W	32	Undefined	Secondary Display Palette RAM

Table 10: Display Controller Register Summary

1. Refer to Table 17 on page 27 for MMIO_base values depending on the CPU.
2. In the reset values, “X” indicates don’t care.

Figure 28 shows how this 64kB region in the MMIO space is laid out. It controls the backend of the display controller as shown in Figure 29.

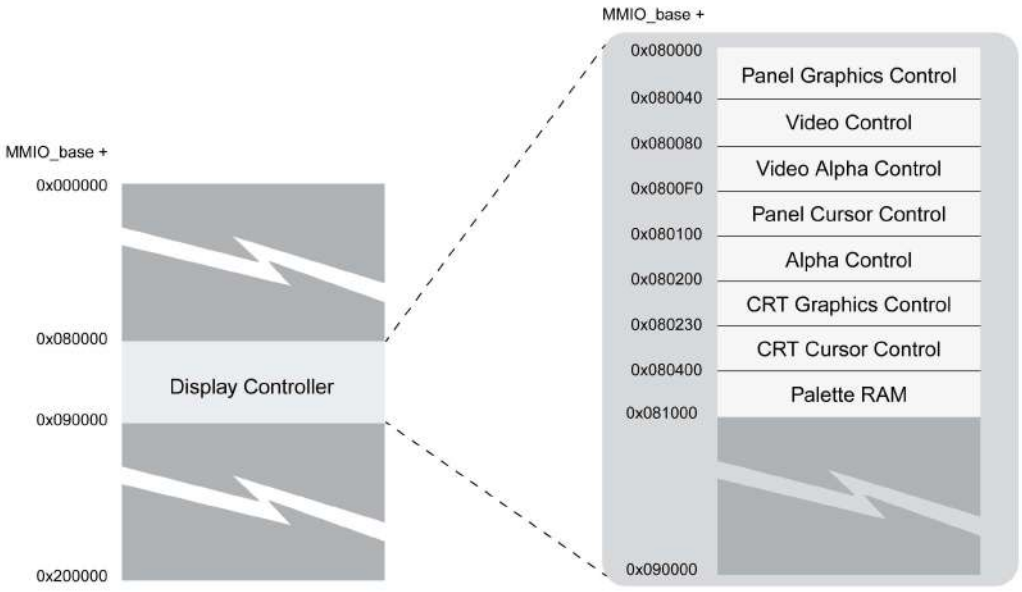


Figure 16: Display Controller Register Space

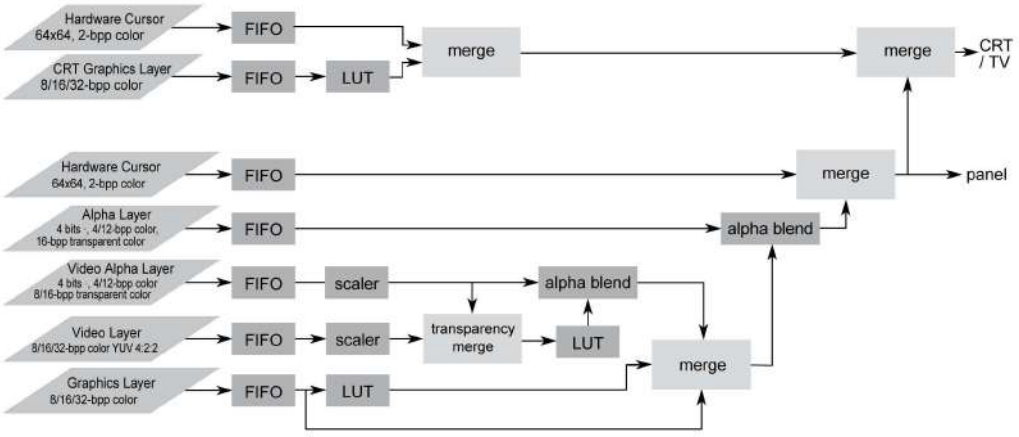


Figure 17: Video Layers

6.2.1 *Primary Graphics Control Registers*

Figure 30 shows the layout of the Primary Graphics Control registers.

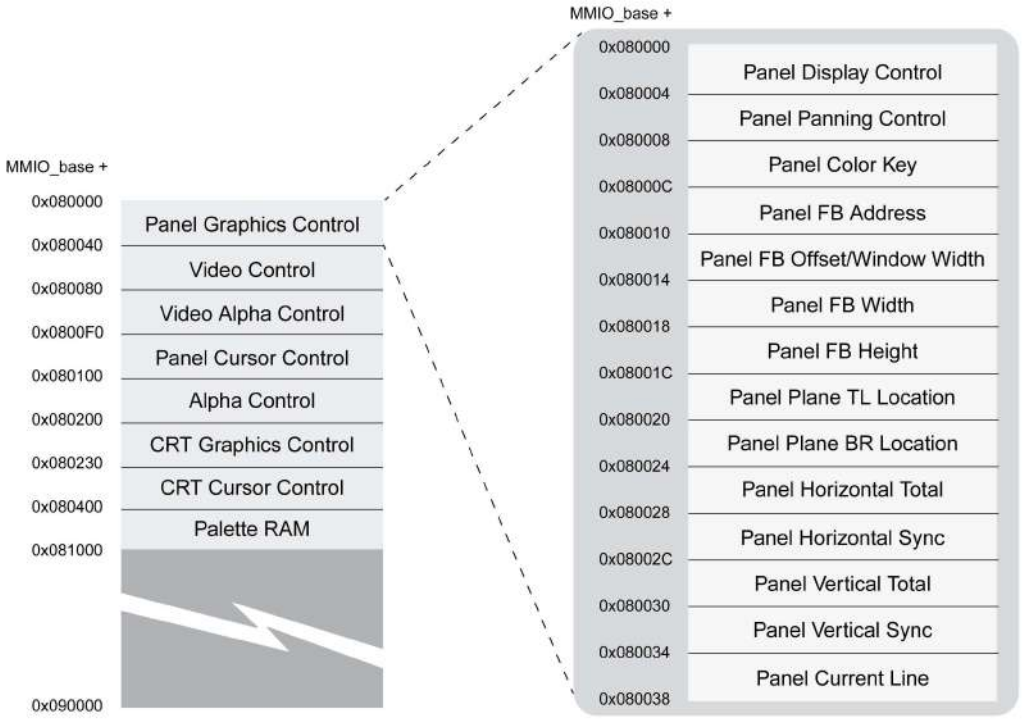


Figure 18: Primary Graphics Control Register Space

To understand video windowing, please refer to Figure 31. Here a window is created inside a much large frame buffer. That window is then being displayed on the panel as the Primary Graphics Plane.

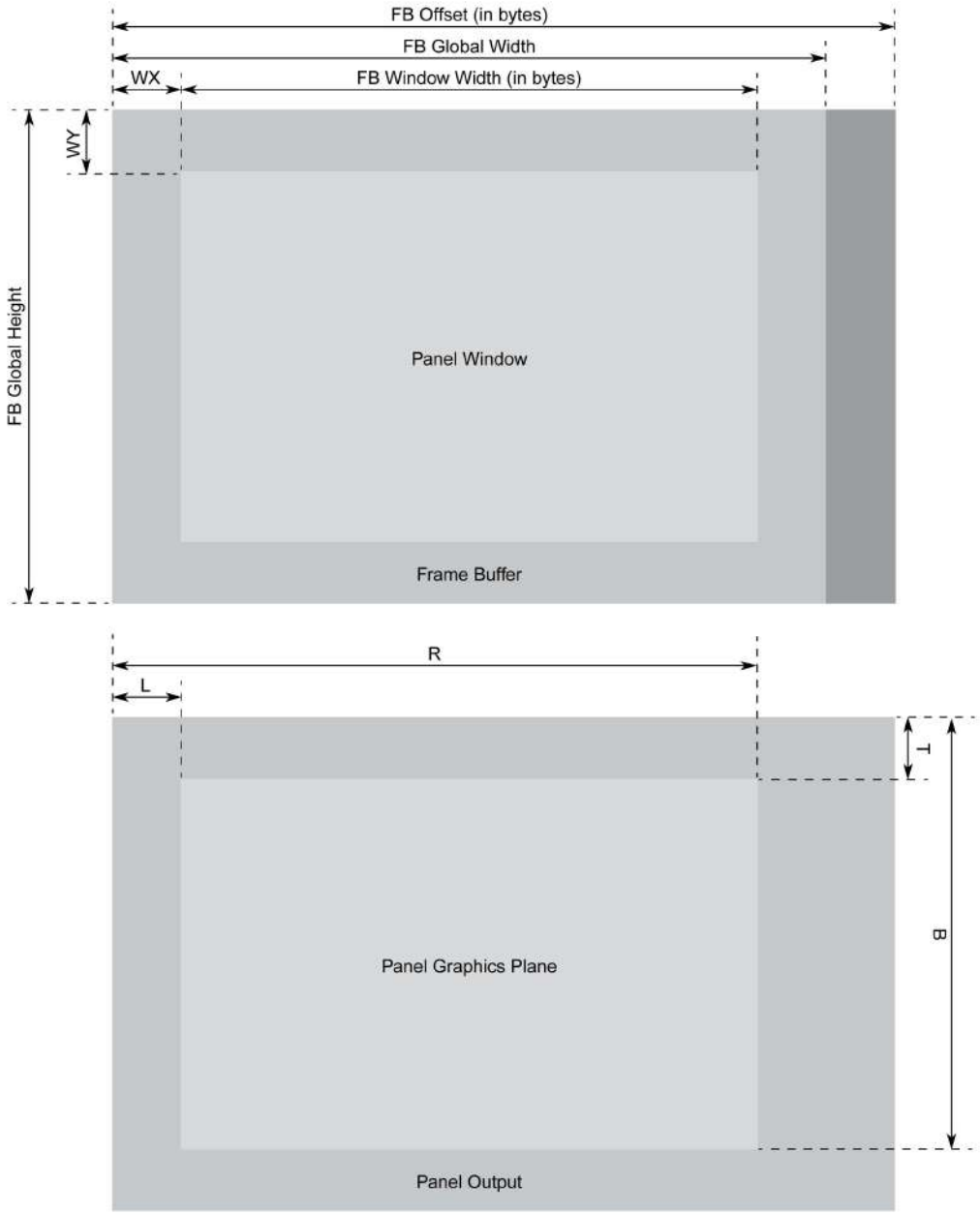


Figure 19: Video Windowing

Primary Display Control

Read/Write MMIO_base + 0x080000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res		Sel R/W		En R/W	Bias R/W	Data R/W	VDD R/W	Res				DD R/W	DP R/w	FIFO R/W	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	CP R/W	VSP R/W	HSP R/W	V R/W	CAPT R/W	CK R/W	TE R/W	VPD R/W	VP R/W	HPD R/W	HP R/W	γ R/W	E R/W	Format R/W	

Bit(s)	Name	Description
31:30	Res	These bits are reserved.
29:28	Sel	Panel Data Select. 00: Panel Data. 01: VGA Data. 10: Secondary Display Data. 11: Reserved.
27	En	FPEN Control. 0: Drive low. 1: Drive high.
26	Bias	Control VBIASEN Output Pin. 0: Driven low. 1: Driven high.
25	Data	Panel Control Signals and Data Lines Enable. 0: Disable panel control signals and data lines. 1: Enable panel control signals and data lines.
24	VDD	Control FPVDDEN Output Pin. 0: Driven low. 1: Driven high.
23:20	Res	These bits are reserved.
19	DD	Dual Digital Display Output. 0: Disable. 1: Enable.
18	DP	Double Pixel Output. 0: Disable. 1: Enable.
17:16	FIFO	Panel Data FIFO Request Level. When the FIFO empty level reaches the level specified, a FIFO read request will be generated. 00: 1 or more entries empty. 01: 3 or more entries empty. 10: 7 or more entries empty. 11: 11 or more entries empty.
15	Res	This bit is reserved.
14	CP	Clock Phase Select. 0: Clock active high. 1: Clock active low.
13	VSP	Vertical Sync Pulse Phase Select. 0: Vertical sync pulse active high. 1: Vertical sync pulse active low.
12	HSP	Horizontal Sync Pulse Phase Select. 0: Horizontal sync pulse active high. 1: Horizontal sync pulse active low.

Bit(s)	Name	Description
11	V	VSYNC
10	CAPT	Enabel Capture Timing (Frame Lock). 0: Disable capture timing. 1: Lock panel timing to ZV Port 0 timing.
9	CK	Enable Color Key. 0: Disable color key. 1: Enable color key.
8	TE	Enable Panel Timing. 0: Disable panel timing. 1: Enable panel timing.
7	VPD	Vertical Panning Direction. 0: Panning down. 1: Panning up.
6	VP	Enable Automatic Vertical Panning. 0: Disable. 1: Enable.
5	HPD	Horizontal Panning Direction. 0: Pan to the right. 1: Pan to the left.
4	HP	Enable Automatic Horizontal Panning. 0: Disable. 1: Enable.
3	γ	Enable Gamma Control. Gamma control can only be enabled in RGB 5:6:5 and RGB 8:8:8 modes. 0: Disable. 1: Enable.
2	E	Primary Graphics Plane Enable. 0: Disable Primary graphics plane. 1: Enable Primary graphics plane. Note: This bit has delayed update until the next VSYNC after change of value, and bit 8 of this register must be set to 1 for a VSYNC to happen.
1:0	Format	Primary Graphics Plane Format. 00: 8-bit indexed mode. 01: 16-bit RGB 5:6:5 mode. 10: 32-bit RGB 8:8:8 mode. 11: Reserved.

Primary Display Panning Control

Read/Write MMIO_base + 0x080004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VPan R/W								Res		VWait R/W					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HPan R/W								Res		HWait R/W					

Bit(s)	Name	Description
31:24	VPan	Number of lines to pan vertically.
23:22	Res	These bits are reserved.
21:16	VWait	Number of vertical sync pulses for each vertical pan.
15:8	HPan	Number of pixels to pan horizontally.
7:6	Res	These bits are reserved.
5:0	HWait	Number of horizontal sync pulses for each horizontal pan.

Primary Display Color Key

Read/Write MMIO_base + 0x080008

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mask R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value R/W															

Bit(s)	Name	Description
31:16	Mask	Color key mask for video window plane.
15:0	Value	Color key value for video window plane.

Primary Display FB Address

Read/Write MMIO_base + 0x08000C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Res			Ext R/W	Res	Address R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address R/W												0 0 0 0			

Bit(s)	Name	Description
31	S	Status Bit. 0: No flip pending. 1: Flip pending.
30:28	Res	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: PCI Bus Master memory.
26	Res	This bit is reserved.
25:4	Address	Memory address of frame buffer for the Primary graphics plane with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Primary Display FB Offset/Window Width

Read/Write MMIO_base + 0x080010

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res		FB Window Width R/W										0 0 0 0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res		FB Offset R/W										0 0 0 0			

Bit(s)	Name	Description
31:30	Res	These bits are reserved.
29:20	FB Window Width	Number of bytes per line of the frame buffer window specified in 128-bit aligned bytes.
19:16	0000	These bits are hardwired to zeros.
15:14	Res	These bits are reserved.
13:4	FB Offset	Number of 128-bit aligned bytes per line of the FB graphics plane.
3:0	0000	These bits are hardwired to zeros.

Primary Display FB Width

Read/Write MMIO_base + 0x080014

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				FB Global Width R/W											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				WX R/W											

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27:16	FB Global Width	Width of FB graphics window specified in pixels (see Figure 5-4).
15:12	Res	These bits are reserved.
11:0	WX	Starting x-coordinate of Primary graphics window specified in pixels.

Primary Display FB Height

Read/Write MMIO_base + 0x080018

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				FB Global Height R/W											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				WY R/W											

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27:16	FB GLobal Height	Height of FB graphics window specified in lines.
15:12	Res	These bits are reserved.
11:0	WY	Starting y-coordinate of Primary graphics window specified in lines.

Primary Display Plane TL Location

Read/Write MMIO_base + 0x08001C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res					T R/W										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res					L R/W										

Bit(s)	Name	Description
31:27	Res	These bits are reserved.
26:16	T	Top location of the Primary Display graphics plane specified in lines.
15:11	Res	These bits are reserved.
10:0	L	Left location of the Primary Display graphics plane specified in pixels.

Primary Display Plane BR Location

Read/Write MMIO_base + 0x080020

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res					B R/W										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res					R R/W										

Bit(s)	Name	Description
31:27	Res	These bits are reserved.
26:16	B	Bottom location of the Primary Display graphics plane specified in lines.
15:11	Res	These bits are reserved.
10:0	R	Right location of the Primary Display graphics plane specified in pixels.

Primary Display Horizontal Total

Read/Write MMIO_base + 0x080024

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				HT R/W											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				HDE R/W											

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27:16	HT	Primary Display horizontal total specified as number of pixels - 1.
15:12	Res	These bits are reserved.
11:0	HDE	Primary Display horizontal display end specified as number of pixels - 1.

Primary Display Horizontal Sync

Read/Write MMIO_base + 0x080028

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res								HSW R/W							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				HS R/W											

Bit(s)	Name	Description
31:24	Res	These bits are reserved.
23:16	HSW	Primary Display horizontal sync width specified in pixels.
15:12	Res	These bits are reserved.
11:0	HS	Primary Display horizontal sync start specified as pixel number - 1.

Primary Display Vertical Total

Read/Write MMIO_base + 0x08002C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res					VT R/W										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res					VDE R/W										

Bit(s)	Name	Description
31:27	Res	These bits are reserved.
26:16	VT	Primary Display vertical total specified as number of lines - 1.
15:11	Res	These bits are reserved.
10:0	VDE	Primary Display vertical display end specified as number of lines - 1.

Primary Display Vertical Sync

Read/Write MMIO_base + 0x080030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res										VSH R/W					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res					VS R/W										

Bit(s)	Name	Description
31:22	Res	These bits are reserved.
21:16	VSH	Primary Display vertical sync height specified in lines.
15:11	Res	These bits are reserved.
10:0	VS	Primary Display vertical sync start specified as line number - 1.

Primary Display Current Line

Read MMIO_base + 0x080034

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res					Line R										

Bit(s)	Name	Description
31:11	Res	These bits are reserved.
10:0	Line	Primary Display current line being fetched.

6.2.2 *Video Control Registers*

Figure 32 shows the layout of the Video Control registers.

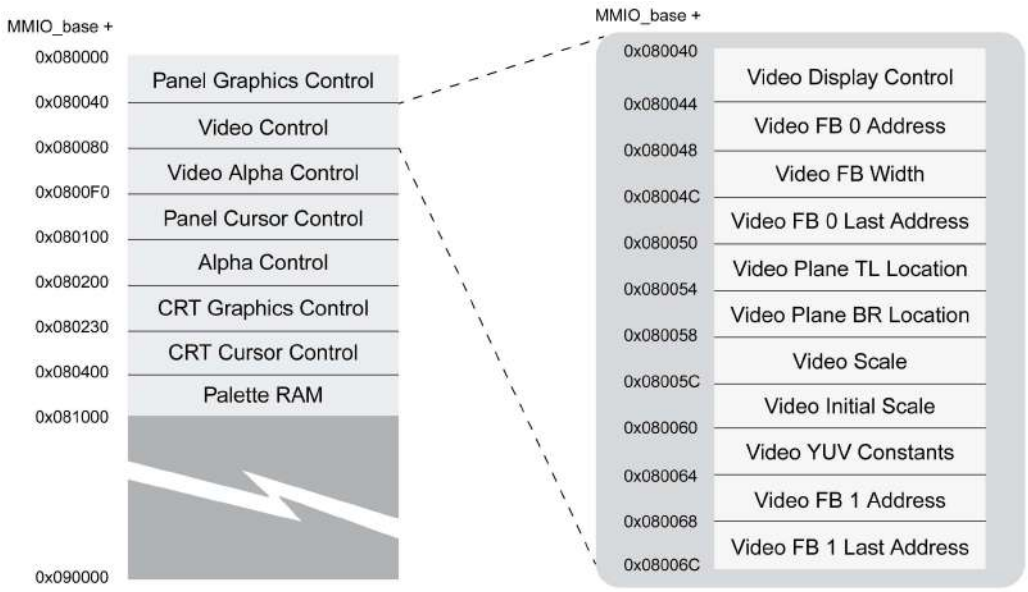


Figure 20: Video Control Register Space

Video Display Control

Read/Write MMIO_base + 0x080040

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res													LineBuf R/W	FIFO R/W	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Buf R	CB R/W	DB R/W	BS R/W	VS R/W	HS R/W	VI R/W	HI R/W	Pixel R/W				γ R/W	E R/W	Format R/W	

Bit(s)	Name	Description
31:19	Res	These bits are reserved.
18	LineBuf	Line Buffer. 0: Disable. 1: Enable. Note: Use it for vertical stretch only. Do not use it for vertical shrinking.
17:16	FIFO	Video Data FIFO Request Level. When the FIFO empty level reaches the level specified, a FIFO read request will be generated. 00: 1 or more entries empty. 01: 3 or more entries empty. 10: 7 or more entries empty. 11: 11 or more entries empty.
15	Buf	Current Video Frame Buffer Used. This bit is read-only. 0: Buffer 0. 1: Buffer 1.
14	CB	Use Capture Frame Buffer as Video Frame Buffer. 0: Disable. 1: Enable.
13	DB	Enable Double Buffering. 0: Disable.

		1: Enable.
12	BS	Enable Byte Swapping for YUV Data. 0: Disable (YUYV). 1: Enable (UYVY).
11	VS	Force Vertical Scale Factor to ½. 0: Disable. 1: Enable.
10	HS	Force Horizontal Scale Factor to ½. 0: Disable. 1: Enable.

Bit(s)	Name	Description
9	VI	Enable Vertical Interpolation. 0: Disable. 1: Enable.
8	HI	Enable Horizontal Interpolation. 0: Disable. 1: Enable.
7:4	Pixel	Starting Pixel Number for Smooth Pixel Panning.
3	Res	This bit is reserved.
2	E	Video Plane Enable. 0: Disable video plane. 1: Enable video plane.
1:0	Format	Video Plane Format. 00: reserved. 01: 16-bit RGB 5:6:5 mode. 10: reserved. 11: 16-bit YUYV mode.

1. All display devices have an inherent non-linearity so that the intensity of the output is not linearly proportional to the input signal over the full range of input values. The gamma control helps to correct this nonlinearity.

Video FB 0 Address

Read/Write MMIO_base + 0x080044

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Reserved			Ext R/W	CS R/W					Address R/W					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					Address R/W								0 0 0 0		

Bit(s)	Name	Description
31	S	Status Bit. 0: No flip pending. 1: Flip pending.
30:28	Res	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: PCI Bus Master memory.
26	Res	This bit is reserved.
25:4	Address	Memory address of frame buffer 0 for the video plane with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Video FB Width

Read/Write MMIO_base + 0x080048

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		Width R/W										0 0 0 0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		Offset R/W										0 0 0 0			

Bit(s)	Name	Description
31:30	Reserved	These bits are reserved.
29:20	Width	Number of bytes per line of the video plane specified in 128-bit aligned bytes.
19:16	0000	These bits are hardwired to zeros.
15:14	Reserved	These bits are reserved.
13:4	Offset	Number of 128-bit aligned bytes per line of the video plane.
3:0	0000	These bits are hardwired to zeros.

Video FB 0 Last Address

Read/Write MMIO_base + 0x08004C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				Ext R/W	CS R/W	Address R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address R/W												0 0 0 0			

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27	Ext	Memory Selection. 0: Internal memory. 1: External memory.
26	Res	This bit is reserved.
25:4	Address	Memory address of last byte of frame buffer 0 for the video plane with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Video Plane TL Location

Read/Write MMIO_base + 0x080050

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					T R/W										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					L R/W										

Bit(s)	Name	Description
31:27	Reserved	These bits are reserved.
26:16	T	Top location of the video plane specified in lines.
15:11	Reserved	These bits are reserved.
10:0	L	Left location of the video plane specified in pixels.

Video Plane BR Location

Read/Write MMIO_base + 0x080054

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					B R/W										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					R R/W										

Bit(s)	Name	Description
31:27	Reserved	These bits are reserved.
26:16	B	Bottom location of the video plane specified in lines.
15:11	Reserved	These bits are reserved.
10:0	R	Right location of the video plane specified in pixels.

Video Scale

Read/Write MMIO_base + 0x080058

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VS R/W	Reserved			VScale R/W											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HS R/W	Reserved			HScale R/W											

Bit(s)	Name	Description
31	VS	Select Vertical Video Scaling. 0: Video expands vertically. 1: Video shrinks vertically.
30:28	Reserved	These bits are reserved.
27:16	VScale	Vertical Video Scale Factor. For expansion: VScale = ($height_{src}$ / $height_{dest}$) * 2_{12}. For shrinking: VScale = ($height_{dest}$ / $height_{src}$) * 2_{12}.
15	HS	Select Horizontal Video Scaling. 0: Video expands horizontally. 1: Video shrinks horizontally.
14:12	Reserved	These bits are reserved.
11:0	HScale	Horizontal Video Scale Factor. For expansion: HScale = ($width_{src}$ / $width_{dest}$) * 2_{12}. For shrinking: HScale = ($width_{dest}$ / $width_{src}$) *2_{12}.

Scaling example: To expand (magnify) the horizontal scale by a factor of 3:

1 Set HS = 0.

2 Calculate the scaling factor: (widthsrc / widthdest) * 212 = (1/3) * 212

3 Set HScale. In this example, HScale = 0101 0101 0101 b or 555h.

To shrink the horizontal scale by a factor of 3:

1 Set HS = 1.

2 Calculate the scaling factor: (widthdest / widthsrc) * 212 = ((1/3/)1) * 212 = 1/3 * 212

3. Set HScale. Note that the HScale setting is the same for shrinking by 1/3 as it is for magnifying by a factor of 3, only the setting of HS differs

Video Initial Scale

Read/Write MMIO_base + 0x08005C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				VScale1 R/W											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				VScale0 R/W											

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27:16	VS	Initial vertical scale factor for video buffer.
15:12	Reserved	These bits are reserved.
11:0	HS	Initial horizontal scale factor for video buffer.

Video YUV Constants

Read/Write MMIO_base + 0x080060

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Y R/W								R R/W							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
G R/W								B R/W							

Bit(s)	Name	Description
31:24	Y	Y Adjustment.
23:16	R	Red Conversion Constant.
15:8	G	Green Conversion Constant.
7:0	B	Blue Conversion Constant.

Video FB 1 Address

Read/Write MMIO_base + 0x080064

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Reserved			Ext R/W	CS R/W R/W	Address									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address R/W												0 0 0 0			

Bit(s)	Name	Description
31	S	Status Bit. 0: No flip pending. 1: Flip pending.
30:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: PCI Bus Master memory.
26	Res	This bit is reserved.
25:4	Address	Memory address of frame buffer 1 for the video plane with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Video FB 1 Last Address

Read/Write MMIO_base + 0x080068

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				Ext R/W	CS R/W	Address R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address R/W												0 0 0 0			

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: PCI Bus Master memory.
26	Res	This bit is reserved.
25:4	Address	Memory address of last byte of frame buffer 1 for the video plane with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Video FB Edge Control

Read/Write MMIO_base + 0x080074

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res							ED R/W	Re							
15	**14**	**13**	**12**	**11**	**10**		**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res							EV R/W									

Bit(s)	Name	Description
31:25	Res	These bits are reserved.
24	ED	Edge Detection Selection: 0: Disable. (default) 1: Enable. Note: It must be used with Line Buffer enable in register 0x80040[18]=1.
23:10	Res	These bits are reserved.
9:0	EV	Edge value.

6.2.3 *Video Alpha Control Registers*

Figure 33 shows the layout of the Video Alpha Control registers.

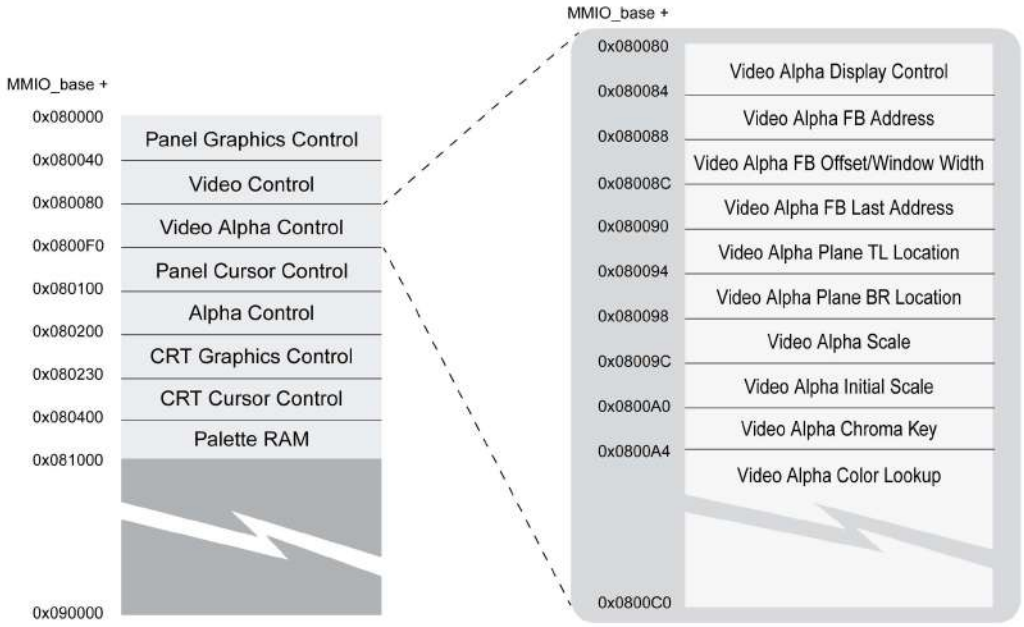


Figure 21: Video Alpha Control Register Space

Video Alpha Display Control

Read/Write MMIO_base + 0x080080

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			Sel R/W	Alpha R/W				Reserved						FIFO R/W	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				VS R/W	HS R/W	VI R/W	HI R/W	Pixel R/W				CK R/W	E R/W	Format R/W	

Bit(s)	Name	Description
31:29	Reserved	These bits are reserved.
28	Sel	Alpha Select. 0: Use per-pixel alpha values. 1: Use alpha value specified in *Alpha*.
27:24	Alpha	Video Alpha Plane Alpha Value. This field is only valid when the *Sel* bit is 1.
23:18	Reserved	These bits are reserved.
17:16	FIFO	Video Alpha Data FIFO Request Level. When the FIFO empty level reaches the level specified, a FIFO read request will be generated. 00: 1 or more entries empty. 01: 3 or more entries empty. 10: 7 or more entries empty. 11: 11 or more entries empty.
15:12	Reserved	These bits are reserved.
11	VS	Force Vertical Scale Factor to ½. 0: Disable. 1: Enable.
10	HS	Force Horizontal Scale Factor to ½. 0: Disable. 1: Enable.
9	VI	Enable Vertical Interpolation. 0: Disable. 1: Enable.
8	HI	Enable Horizontal Interpolation. 0: Disable. 1: Enable.
7:4	Pixel	Starting Pixel Number for Smooth Pixel Panning.
3	CK	Enable Chroma Key. 0: Disable. 1: Enable.
2	E	Video Alpha Plane Enable. 0: Disable video plane. 1: Enable video plane.
1:0	Format	Video Alpha Plane Format. 00: 8-bit indexed mode. 01: 16-bit RGB 5:6:5 mode. 10: 8-bit indexed αI 4:4 mode. 11: 16-bit αRGB 4:4:4:4 mode.

Video Alpha FB Address

Read/Write MMIO_base + 0x080084

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Reserved			Ext R/W	CS R/W	Address R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address R/W												0 0 0 0			

Bit(s)	Name	Description
31	S	Status Bit. 0: No flip pending. 1: Flip pending.
30:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: PCI Bus Master memory.
26	Res	This bit is reserved.
25:4	Address	Memory address of frame buffer for the video alpha plane with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Video Alpha FB Offset/Window Width

Read/Write MMIO_base + 0x080088

31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
Reserved		Window Width R/W											0 0 0 0			
15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
Reserved		FB Offset R/W											0 0 0 0			

Bit(s)	Name	Description
31:30	Reserved	These bits are reserved.
29:20	Window Width	Number of bytes per line of the video alpha window specified in 128-bit aligned bytes.
19:16	0000	These bits are hardwired to zeros.
15:14	Reserved	These bits are reserved.
13:4	FB Offset	Number of 128-bit aligned bytes per line of the video alpha FB.
3:0	0000	These bits are hardwired to zeros.

Video Alpha FB Last Address

Read/Write MMIO_base + 0x08008C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved			Ext R/W	CS R/W	Address R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address R/W												0 0 0 0			

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: PCI Bus Master memory.
26	Res	This bit is reserved.
25:4	Address	Memory address of last byte of frame buffer for the video alpha plane with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Video Alpha Plane TL Location

Read/Write MMIO_base + 0x080090

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					Top R/W										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					Left R/W										

Bit(s)	Name	Description
31:27	Reserved	These bits are reserved.
26:16	Top	Top location of the video alpha plane specified in lines.
15:11	Reserved	These bits are reserved.
10:0	Left	Left location of the video alpha plane specified in pixels.

Video Alpha Plane BR Location

Read/Write MMIO_base + 0x080094

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					Bottom R/W										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					Right R/W										

Bit(s)	Name	Description
31:27	Reserved	These bits are reserved.
26:16	Bottom	Bottom location of the video alpha plane specified in lines.
15:11	Reserved	These bits are reserved.
10:0	Right	Right location of the video alpha plane specified in pixels.

Video Alpha Scale

Read/Write MMIO_base + 0x080098

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VS R/W	Reserved			VScale R/W											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HS R/W	Reserved			HScale R/W											

Bit(s)	Name	Description
31	VS	Select Vertical Video Scaling. 0: Video expands vertically. 1: Video shrinks vertically.
30:28	Reserved	These bits are reserved.
27:16	VScale	Vertical Video Scale Factor. For expansion: VScale = $height_{src}$ / $height_{dest}$ * 2_{12}. For shrinking: VScale = $height_{dest}$ / $height_{src}$ * 2_{12}.
15	HS	Select Horizontal Video Scaling. 0: Video expands horizontally. 1: Video shrinks horizontally.
14:12	Reserved	These bits are reserved.
11:0	HScale	Horizontal Video Scale Factor. For expansion: HScale = $width_{src}$ / $width_{dest}$ * 2_{12}. For shrinking: HScale = $width_{dest}$ / $width_{src}$ * 2_{12}.

Video Alpha Initial Scale

Read/Write MMIO_base + 0x08009C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				VS R/W											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				HS R/W											

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27:16	VS	Initial Vertical Scale Factor.
15:12	Res	These bits are reserved.
11:0	HS	Initial Horizontal Scale Factor.

Video Alpha Chroma Key

Read/Write MMIO_base + 0x0800A0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mask R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value R/W															

Bit(s)	Name	Description
31:16	Mask	Chroma Key Mask for Video Alpha Plane. 0: Compare respective bit. 1: Do not compare respective bit.
15:0	Value	Chroma Key Value for Video Alpha Plane.

Video Alpha Color Lookup

Read/Write MMIO_base + 0x0800A4-0x0800C0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Lookup1 R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Lookup0 R/W															

Bit(s)	Name	Description
31:16	$Lookup_1$	Alpha RGB 5:6:5 color lookup value for 4-bit indexed color 1.
15:0	$Lookup_0$	Alpha RGB 5:6:5 color lookup value for 4-bit indexed color 0.

There are 8 Video Alpha Color Lookup registers, each containing two RGB 5:6:5 color lookup values for each of the 16 4-bit indexed colors.

6.2.4 *Primary Display Cursor Control Registers*

Figure 34 shows the layout of the Primary Display Cursor Control registers.

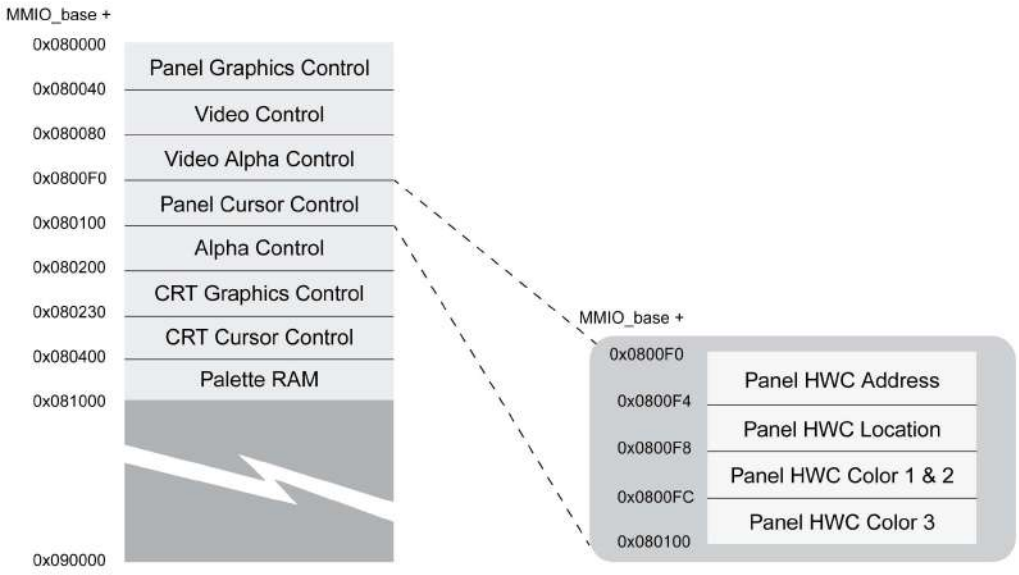


Figure 22: Primary Display Cursor Control Register Space

Primary Display HWC Address

Read/Write MMIO_base + 0x0800F0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E R/W	Reserved			Ext R/W	CS R/W	Address R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address R/W												0 0 0 0			

Bit(s)	Name	Description
31	E	Enable Primary Display Hardware Cursor. 0: Disable. 1: Enable.
30:28	Res	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: PCI Bus Master memory.
26	Res	This bit is reserved.
25:4	Address	Memory address of Primary Display hardware cursor with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Primary Display HWC Location

Read/Write MMIO_base + 0x0800F4

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				T R/W	Y R/W										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				L R/W	X R/W										

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27	T	Top Boundary Select. 0: Primary Display hardware cursor is within screen top boundary. 1: Primary Display hardware cursor is partially outside screen top boundary.
26:16	Y	Primary Display Hardware Cursor Y Position.
15:12	Reserved	These bits are reserved.
11	L	Left Boundary Select. 0: Primary Display hardware cursor is within screen left boundary. 1: Primary Display hardware cursor is partially outside screen left boundary.
10:0	X	Primary Display Hardware Cursor X Position.

Primary Display HWC Color 1 & 2

Read/Write MMIO_base + 0x0800F8

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Color2 R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Color1 R/W															

Bit(s)	Name	Description
31:16	Color2	Primary Display hardware cursor color 2 in RGB 5:6:5.
15:0	Color1	Primary Display hardware cursor color 1 in RGB 5:6:5.

Primary Display HWC Color 3

Read/Write MMIO_base + 0x0800FC

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Color3 R/W															

Bit(s)	Name	Description
31:16	Reserved	These bits are reserved.
15:0	Color3	Primary Display hardware cursor color 3 in RGB 5:6:5.

6.2.5 *Alpha Control Registers*

Figure 35 shows the layout of the Alpha Control registers.

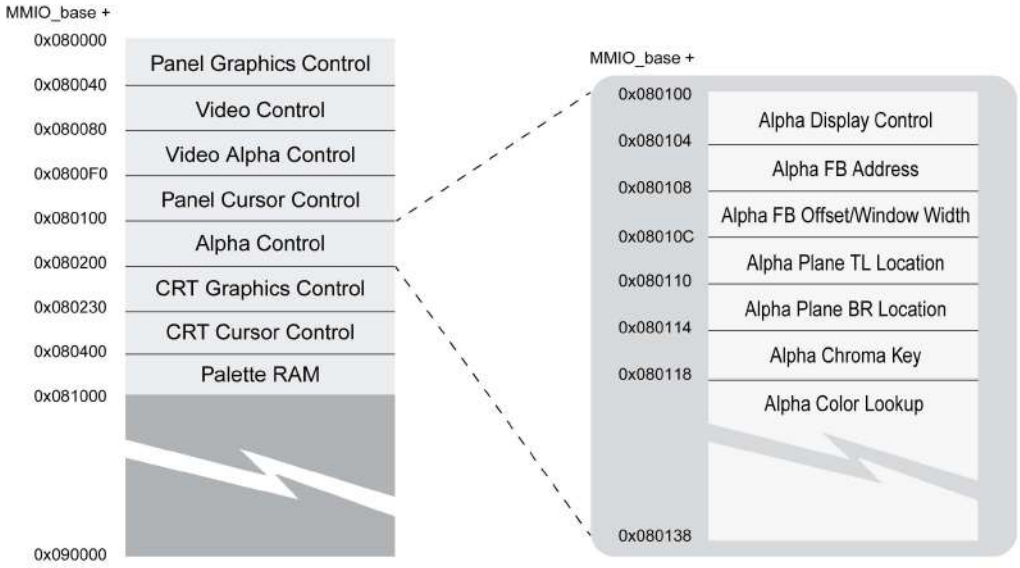


Figure 23: Alpha Control Register Space

Alpha Display Control

Read/Write MMIO_base + 0x080100

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			Sel R/W	Alpha R/W				Reserved						FIFO R/W	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								Pixel R/W				CK R/W	E R/W	Format R/W	

Bit(s)	Name	Description
31:29	Reserved	These bits are reserved.
28	Sel	Alpha Select. 0: Use per-pixel alpha values. 1: Use alpha value specified in *Alpha*.
27:24	Alpha	Alpha Plane Alpha Value. This field is only valid when the *Sel* bit is 1.
23:18	Reserved	These bits are reserved.
17:16	FIFO	Video Data FIFO Request Level. When the FIFO empty level reaches the level specified, a FIFO read request will be generated. 00: 1 or more entries empty. 01: 3 or more entries empty. 10: 7 or more entries empty. 11: 11 or more entries empty.
15:8	Reserved	These bits are reserved.
7:4	Pixel	Starting Pixel Number for Smooth Pixel Panning.
3	CK	Enable Chroma Key. 0: Disable chroma key. 1: Enable chroma key.
2	E	Alpha Plane Enable. 0: Disable alpha plane. 1: Enable alpha plane.
1:0	Format	Alpha Plane Format. 00: reserved. 01: 16-bit RGB 5:6:5 mode. 10: 8-bit indexed αI 4:4 mode. 11: 16-bit αRGB 4:4:4:4 mode.

Alpha FB Address

Read/Write MMIO_base + 0x080104

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Reserved			Ext R/W	CS R/W	Address R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address R/W												0 0 0 0			

Bit(s)	Name	Description
31	S	Status Bit. 0: No flip pending. 1: Flip pending.
30:28	Res	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: PCI Bus Master memory.
26	Res	This bit is reserved.
25:4	Address	Memory address of frame buffer for the alpha plane with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Alpha FB Offset/Window Width

Read/Write MMIO_base + 0x080108

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		Window Width R/W										0 0 0 0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		FB Offset R/W										0 0 0 0			

Bit(s)	Name	Description
31:30	Reserved	These bits are reserved.
29:20	Window Width	Number of bytes per line of the alpha window specified in 128-bit aligned bytes.
19:16	0000	These bits are hardwired to zeros.
15:14	Reserved	These bits are reserved.
13:4	FB Offset	Number of 128-bit aligned bytes per line of the alpha FB.
3:0	0000	These bits are hardwired to zeros.

Alpha Plane TL Location

Read/Write MMIO_base + 0x08010C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					Top R/W										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					Left R/W										

Bit(s)	Name	Description
31:27	Reserved	These bits are reserved.
26:16	Top	Top location of the alpha plane specified in lines.
15:11	Reserved	These bits are reserved.
10:0	Left	Left location of the alpha plane specified in pixels.

Alpha Plane BR Location

Read/Write MMIO_base + 0x080110

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					Bottom R/W										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					Right R/W										

Bit(s)	Name	Description
31:27	Reserved	These bits are reserved.
26:16	Bottom	Bottom location of the alpha plane specified in lines.
15:11	Reserved	These bits are reserved.
10:0	Right	Right location of the alpha plane specified in pixels.

Alpha Chroma Key

Read/Write MMIO_base + 0x080114

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mask R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value R/W															

Bit(s)	Name	Description
31:16	Mask	Chroma Key Mask for Alpha Plane. 0: Compare respective bit. 1: Do not compare respective bit.
15:0	Value	Chroma Key Value for Alpha Plane.

Alpha Color Lookup

Read/Write MMIO_base + 0x080118-0x080134

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Lookup1 R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Lookup0 R/W															

Bit(s)	Name	Description
31:16	Lookup1	Alpha RGB 5:6:5 color lookup value for 4-bit indexed color 1.
15:0	Lookup0	Alpha RGB 5:6:5 color lookup value for 4-bit indexed color 0.

There are 8 Alpha Color Lookup registers, each containing two RGB 5:6:5 color lookup values for each of the 16 4-bit indexed colors.

6.2.6 *Secondary Display Graphics Control Registers*

Figure 36 shows the layout of the Secondary Display Graphics Control registers.

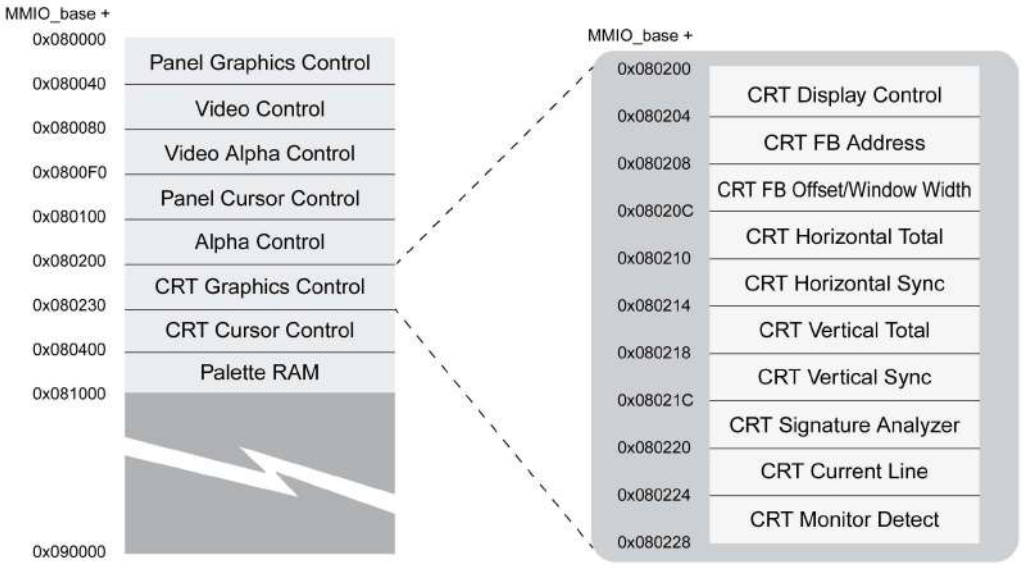


Figure 24: Secondary Display Graphics Control Register Space

Secondary Display Control

Read/Write MMIO_base + 0x080200

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					VDS	Res	HAC	Lock	Exp	VI	HI	Sel		FIFO R/W	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	CP R/W	VSP R/W	HSP R/W	VS R	B R/W	Sel R/W	TE R/W	Pixel R/W				γ R/W	E R/W	Format R/W	

Bit(s)	Name	Description
31:27	Res	These bits are reserved.
26	VDS	VGA Data Shift. (Color data shift from lower 6-bit to 8-bit) 0: Enable. 1: Disable.
25	Res	This bit is reserved.
24	HAC	Enable Horizontal Auto-Centering. 0: Disable. 1: Enable.
23	Lock	Enable Capture Timing (Frame Lock). 0: Disable capture timing. 1: Lock panel timing to CRT timing.
22	Exp	Enable Auto Expansion. 0 Disable. 1: Enable.
21	VI	Enable Vertical Interpolation. 0: Disable. 1: Enable.
20	HI	Enable Horizontal Interpolation. 0: Disable. 1: Enable.
19:18	Sel	Secondary Display Data Select. 00: Panel Data. 01: VGA Data. 10: CRT Data. 11: reserved.
17:16	FIFO	Secondary Display Data FIFO Request Level. When the FIFO empty level reaches the level specified, a FIFO read request will be generated. 00: 1 or more entries empty. 01: 3 or more entries empty. 10: 7 or more entries empty. 11: 11 or more entries empty.
15	Res	This bit is reserved.
14	CP	CRT Clock Phase Select. 0: CRT clock active high. 1: CRT clock active low.
13	VSP	Vertical Sync Pulse Phase Select. 0: Vertical sync pulse active high. 1: Vertical sync pulse active low.
12	HSP	Horizontal Sync Pulse Phase Select. 0: Horizontal sync pulse active high. 1: Horizontal sync pulse active low.
11	VS	Vertical Sync. This bit is read only.
10	B	CRT Data Blanking. 0: CRT will show pixels. 1: CRT will be blank.
9	Res	This bit is reserved.

Bit(s)	Name	Description
8	TE	Enable CRT Timing. 0: Disable CRT timing. 1: Enable CRT timing.
7:4	Pixel	Starting Pixel Number for Smooth Pixel Panning.
3	γ	Enable Gamma Control. Gamma control can be enabled only in RGB 5:6:5 and RGB 8:8:8 modes. 0: Disable gamma control. 1: Enable gamma control.
2	E	Secondary Display Graphics Plane Enable. 0: Disable Secondary Display Graphics plane. 1: Enable Secondary Display Graphics plane. Note: This bit has delayed update until the next VSYNC after change of value, and bit 8 of this register must be set to 1 for a VSYNC to happen.
1:0	Format	Secondary Display Graphics Plane Format. 00: 8-bit indexed mode. 01: 16-bit RGB 5:6:5 mode. 10: 32-bit RGB 8:8:8 mode. 11: reserved.

Secondary Display FB Address

Read/Write MMIO_base + 0x080204

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Reserved			Ext R/W	CS R/W	Address R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address R/W												0 0 0 0			

Bit(s)	Name	Description
31	S	Status Bit. 0: No flip pending. 1: Flip pending.
30:28	Res	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: PCI Bus Master memory.
26	Res	This bit is reserved.
25:4	Address	Memory address of the frame buffer for the Secondary Display graphics plane with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Secondary Display FB Offset/Window Width

Read/Write MMIO_base + 0x080208

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		Window Width R/W										0 0 0 0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		FB Offset R/W										0 0 0 0			

Bit(s)	Name	Description
31:30	Reserved	These bits are reserved.
29:20	Window Width	Number of bytes per line of the Secondary Display graphics window specified in 128-bit aligned bytes.
19:16	0000	These bits are hardwired to zeros.
15:14	Reserved	These bits are reserved.
13:4	FB Offset	Number of 128-bit aligned bytes per line of the Secondary Display graphics FB.
3:0	0000	These bits are hardwired to zeros.

Secondary Display Horizontal Total

Read/Write MMIO_base + 0x08020C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				HT R/W											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				HDE R/W											

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27:16	HT	Secondary Display horizontal total specified as number of pixels – 1.
15:12	Reserved	These bits are reserved.
11:0	HDE	Secondary Display horizontal display end specified as number of pixels – 1.

Secondary Display Horizontal Sync

Read/Write MMIO_base + 0x080210

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								HSW R/W							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				HS R/W											

Bit(s)	Name	Description
31:24	Reserved	These bits are reserved.
23:16	HSW	Secondary Display horizontal sync width specified in pixels.
15:12	Reserved	These bits are reserved.
11:0	HS	Secondary Display horizontal sync start specified as pixel number - 1.

Secondary Display Vertical Total

Read/Write MMIO_base + 0x080214

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					VT R/W										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					VDE R/W										

Bit(s)	Name	Description
31:27	Reserved	These bits are reserved.
26:16	VT	Secondary Display vertical total specified as number of lines – 1.
15:11	Reserved	These bits are reserved.
10:0	VDE	Secondary Display vertical display end specified as number of lines – 1.

Secondary Display Vertical Sync

Read/Write MMIO_base + 0x080218

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										VSH R/W					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					VS R/W										

Bit(s)	Name	Description
31:22	Reserved	These bits are reserved.
21:16	VSH	Secondary Display vertical sync height specified in lines.
15:11	Reserved	These bits are reserved.
10:0	VS	Secondary Display vertical sync start specified as line number - 1.

Secondary Display Signature Analyzer

Read/Write MMIO_base + 0x08021C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Status R															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												E R/W	R R/W	Sel R/W	

Bit(s)	Name	Description
31:16	Status	Analyzer Signature. This field is read-only.
15:4	Reserved	These bits are reserved.
3	E	Enable Signature Analyzer. 0: Disable. 1: Enable.
2	R	Reset Signature Analyzer. 0: Normal. 1: Reset.
1:0	Sel	Source Select for Signature Analyzer. 00: Red color. 01: Green color. 10: Blue color. 11: reserved.

Secondary Display Current Line

Read MMIO_base + 0x080220

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					Line R										

Bit(s)	Name	Description
31:11	Reserved	These bits are reserved.
10:0	Line	Secondary Display Current Line Being Fetched.

CRT Monitor Detect

Read/Write MMIO_base + 0x080224

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						MDET R	E R/W	Data R							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data R															

Bit(s)	Name	Description
31:26	Reserved	These bits are reserved.
25	MDET	Monitor Detect Read Back. 0: All R, G, and B voltages are less than or equal to 0.325 V. 1: All R, G, and B voltages are greater than 0.325 V.
24	E	Monitor Detect Enable. 0: Disable. 1: Enable.
23:0	Data	Monitor Detect Data in RGB 8:8:8. This field is read-only.

Secondary Display Scaler Register

Read/Write MMIO_base + 0x080228

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				VSF											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				HSF											

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27:16	VSF	Vertical Scale Factor.
15:12	Reserved	These bits are reserved.
11:0	HSF	Horizontal Scale Factor.

6.2.7 *Secondary Display Cursor Control Registers*

Figure 37 shows the layout of the Secondary Display Cursor Control registers.

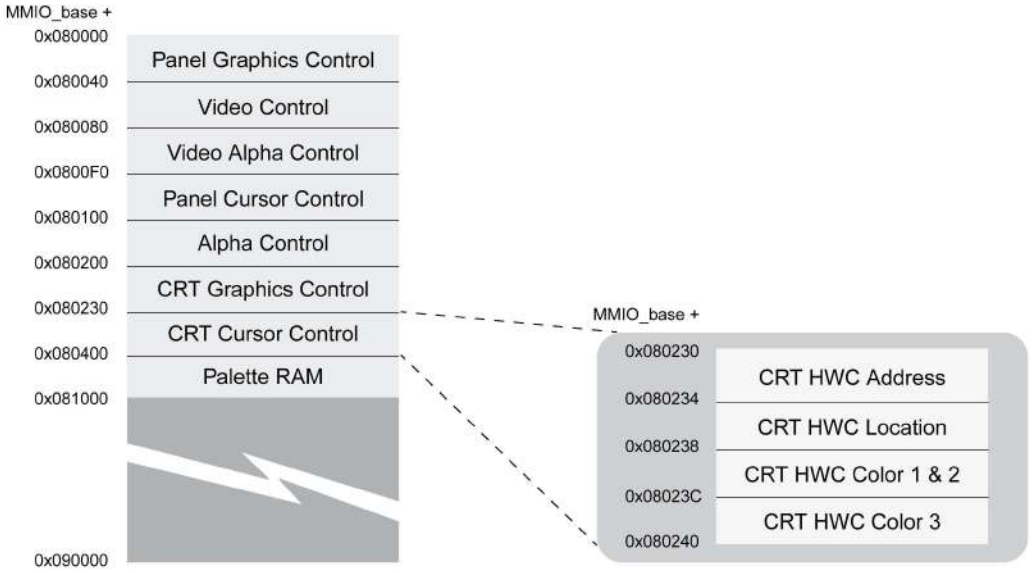


Figure 25: Secondary Display Cursor Control Register Space

Secondary Display HWC Address

Read/Write MMIO_base + 0x080230

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E R/W	Reserved			Ext R/W	CS R/W	Address R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address R/W												0 0 0 0			

Bit(s)	Name	Description
31	E	Enable Secondary Display Hardware Cursor. 0: Disable. 1: Enable.
30:28	Res	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: PCI Bus Master memory.
26	Res	This bit is reserved.
25:4	Address	Memory address of Secondary Display hardware cursor with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Secondary Display HWC Location

Read/Write MMIO_base + 0x080234

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				T R/W	Y R/W										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				L R/W	X R/W										

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27	T	Top Boundary Select. 0: Secondary Display hardware cursor is within screen top boundary. 1: Secondary Display hardware cursor is partially outside screen top boundary.
26:16	Y	Secondary Display Hardware Cursor Y Position.
15:12	Reserved	These bits are reserved.
11	L	Left Boundary Select. 0: Secondary Display hardware cursor is within screen left boundary. 1: Secondary Display hardware cursor is partially outside screen left boundary.
10:0	X	Secondary Display Hardware Cursor X Position.

Secondary Display HWC Color 1 & 2

Read/Write MMIO_base + 0x080238

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Color2 R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Color1 R/W															

Bit(s)	Name	Description
31:16	Color2	Secondary Display Hardware Cursor Color 2 in RGB 5:6:5.
15:0	Color1	Secondary Display Hardware Cursor Color 1 in RGB 5:6:5.

Secondary Display HWC Color 3

Read/Write MMIO_base + 0x08023C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Color3 R/W															

Bit(s)	Name	Description
31:16	Reserved	These bits are reserved.
15:0	Color3	Secondary Display Hardware Cursor Color 3 in RGB 5:6:5.

6.2.8 *Palette RAM Registers*

Figure 38 shows the layout of the Palette RAM registers.

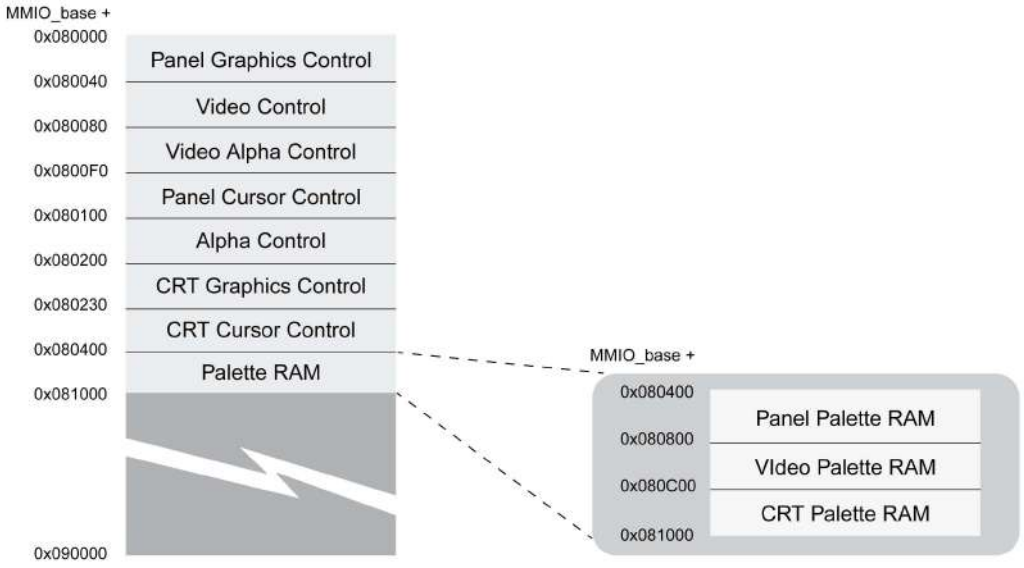


Figure 26: Palette RAM Register Space

Vertical Auto Expansion

Read/Write MMIO_base + 0x080240-0x080267

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res								Comp							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Line				VS											

Bit(s)	Name	Description
31:24	Res	These bits are reserved. (must be 0)
23:16	Comp	Line Compare with Vertical Display End VGA mode: 3D4_01[7:0] Non-VGA mode: 0x8002C[10:3]
15:12	Line	Number of Line Before Secondary Display Horizontal Total to Start Panel Display. This will lock panel timing to Secondary Display timing. This also allows enough data in the line buffer to start graphic display from the line buffer.
11:0	VS	Vertical Scale Factor.

Horizontal Auto Expansion

Read/Write MMIO_base + 0x080268-0x08027F

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ACH								Comp							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Line				HS											

Bit(s)	Name	Description
31:24	ACH	Auto-Centering Horizontal Centering. (0x080268 to 0x08027C)
23:16	Comp	Line Compare with Horizontal Display End VGA mode: 3D4_12[7:0] Non-VGA mode: 0x80024[10:3]
15:12	Res	These bits are reserved.
11:0	HS	Horizontal Scale Factor.

Centering TL Location

Read/Write MMIO_base + 0x080280-0x080282

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					T R/W										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					L R/W										

Bit(s)	Name	Description
31:27	Reserved	These bits are reserved.
26:16	T	Top location of the centering specified in lines.
15:11	Reserved	These bits are reserved.
10:0	L	Left location of the centering specified in pixels.

Centering BR Location

Read/Write MMIO_base + 0x080284-0x080286

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					B R/W										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					R R/W										

Bit(s)	Name	Description
31:27	Reserved	These bits are reserved.
26:16	B	Bottom location of the centering specified in lines.
15:11	Reserved	These bits are reserved.
10:0	R	Right location of the centering specified in pixels.

Primary Display Palette RAM

Read/Write MMIO_base + 0x080400-0x0807FC

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								Red R/W							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Green R/W								Blue R/W							

Bit(s)	Name	Description
31:24	Reserved	These bits are reserved.
23:16	Red	For indexed color modes: 8-bit red color value. For 16- and 32-bit color modes: 8-bit red alpha value.
15:8	Green	For indexed color modes: 8-bit green color value. For 16- and 32-bit color modes: 8-bit green alpha value.
7:0	Blue	For indexed color modes: 8-bit blue color value. For 16- and 32-bit color modes: 8-bit blue alpha value.

There are 256 Primary Display Palette RAM registers, each containing a 24-bit RGB 8:8:8 color value.

Secondary Display Palette RAM

Read/Write MMIO_base + 0x080C00-0x080FFC

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								Red R/W							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Green R/W								Blue R/W							

Bit(s)	Name	Description
31:24	Reserved	These bits are reserved.
23:16	Red	For indexed color modes: 8-bit red color value. For 16- and 32-bit color modes: 8-bit red alpha value.
15:8	Green	For indexed color modes: 8-bit green color value. For 16- and 32-bit color modes: 8-bit green alpha value.
7:0	Blue	For indexed color modes: 8-bit blue color value. For 16- and 32-bit color modes: 8-bit blue alpha value.

There are 256 Video Palette RAM registers, each containing a 24-bit RGB 8:8:8 color value.

7. GPIO

7.1 Functional Overview

7.1.1 GPIO Interface

The GPIO peripheral includes the following registers:

- Data register
- Data Direction register
- Interrupt Setup register
- Interrupt Status register
- Interrupt Reset register

7.2 Programmer's Model

The base address of the GPIO is not fixed, and can be different for any particular system implementation.

However, the offset of any particular register from the base address is fixed.

The following locations are reserved and must not be used during normal operation:

- Locations at offsets 0x424 to 0xFCC are reserved for possible future extensions and test purposes
- Locations at offsets +0xFDO to +0xFDC are reserved for future ID expansion.

Figure 40 shows how this 64kB region in the MMIO space is laid out. It controls the GPIO registers.

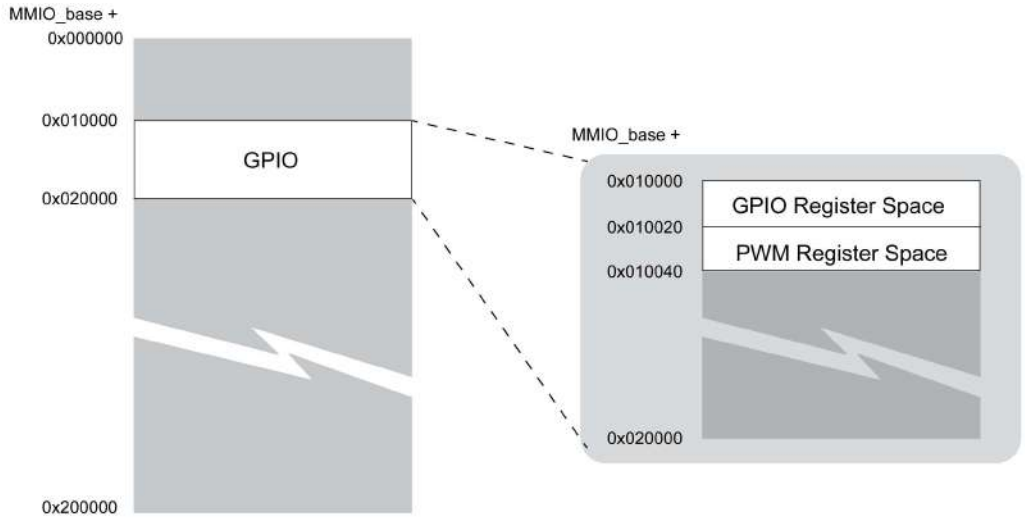


Figure 27: GPIO Register Space

The following sections define each region in more detail.

7.3 Register Descriptions

The GPIO registers are shown in Table 14.

Address	Type	Width	Reset Value	Register Name
0x010000	R/W	32	0x00000000	GPIO Data Low
0x010004	R/W	32	0x00000000	GPIO Data High
0x010008	R/W	32	0x00000000	GPIO Data Direction Low
0x01000C	R/W	32	0x00000000	GPIO Data Direction High
0x010010	R/W	32	0x00000000	GPIO Interrupt Setup
0x010014	R	32	0x00000000	GPIO Interrupt Status
0x010014	W	32	0x00000000	GPIO Interrupt Reset

Table 11: GPIO Register Summary

1. Refer to Table 5 on page 27 for MMIO_base values depending on the CPU.

7.3.1 GPIO Register Descriptions

The GPIO registers are described in this section.

The GPIO registers control the GPIO pins. There are seven GPIO registers, two of which share the same address for interrupt status/reset. Figure 41 defines the register layout for the GPIO registers.

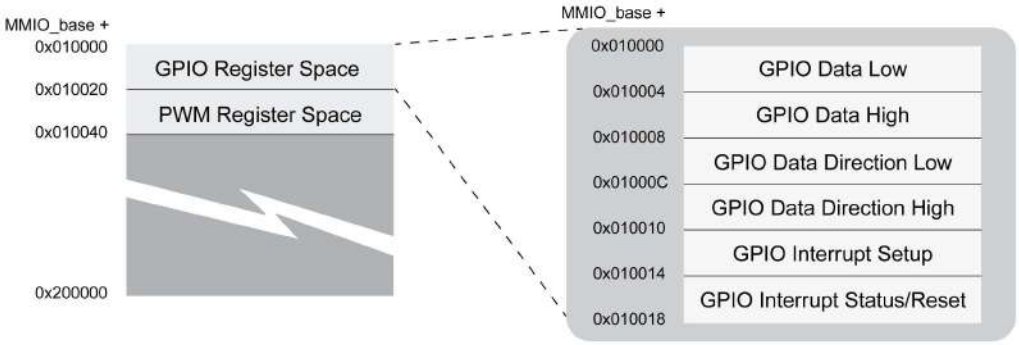


Figure 28: GPIO Register Space

GPIO Data Low

Read/Write Address 0x010000

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
$Data_{31:16}$ R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$Data_{15:0}$ R/W															

Bit(s)	Name	Description
31:0	$Data_{31:0}$	The values in the $Data_{31:0}$ bits reflect the value on the $GPIO_{31:0}$ pins.

This register reflects the value on a GPIO pin. If it is programmed as an input, the value of the GPIO pin is transferred to the corresponding bit in this register. If it is programmed as an output, the value of the bit is transferred to the corresponding GPIO pin.

GPIO Data High

Read/Write Address 0x010004

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
$Data_{63:48}$ R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$Data_{47:32}$ R/W															

Bit(s)	Name	Description
31:0	$Data_{63:32}$	The values in the $Data_{63:32}$ bits reflect the value on the $GPIO_{63:32}$ pins.

This register reflects the value on a GPIO pin. If it is programmed as an input, the value of the GPIO pin is transferred to the corresponding bit in this register. If it is programmed as an output, the value of the bit is transferred to the corresponding GPIO pin.

GPIO Data Direction Low

Read/Write Address 0x010008

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
$Direction_{31:16}$ R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$Direction_{15:0}$ R/W															

Bit(s)	Name	Description
31:0	$Direction_{31:0}$	This register defines whether a GPIO pin is programmed as in input or as an output. 0: Input. 1: Output.

GPIO Data Direction High

Read/Write Address 0x01000C

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
$Direction_{63:48}$ R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$Direction_{47:32}$ R/W															

Bit(s)	Name	Description
31:0	$Direction_{63:32}$	This register defines whether a GPIO pin is programmed as in input or as an output. 0: Input. 1: Output.

GPIO Interrupt Setup

Read/Write Address 0x010010

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved									$Trigger_{54:48}$ R/W						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	$Active_{54:48}$ R/W							Res	$Enable_{54:48}$ R/W						

Bit(s)	Name	Description
31:23	Reserved	These bits are reserved.
22:16	$Trigger_{54:48}$	Triggering Type. 0: Edge triggered. 1: Level triggered.
15	Res	This bit is reserved.
14:8	$Active_{54:48}$	Active State. 0: Active low or falling edge. 1: Active high or rising edge.
7	Res	This bit is reserved.
6:0	$Enable_{54:48}$	This register defines whether GPIO54:48 pins are programmed as regular input/output pins or as interrupt input pins. It also defines the interrupt type. 0: Regular GPIO Input/Output. 1: GPIO Interrupt.

GPIO Interrupt Status

Read Address 0x010014

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved									$Status_{54:48}$ R/W						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit(s)	Name	Description
31:23	Reserved	These bits are reserved.
22:16	$Status_{54:48}$	This read/only register reflects the status of the interrupt pins. When an external interrupt happens on a GPIO interrupt pin, the status bit will be set to “1” until the software resets the interrupt by writing to the GPIO Interrupt Status. 0: Interrupt inactive. 1: Interrupt active.
15:0	Reserved	These bits are reserved.

GPIO Interrupt Reset

Write Address 0x010014

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved									$Reset_{54:48}$ W						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit(s)	Name	Description
31:23	Reserved	These bits are reserved.
22:16	$Reset_{54:48}$	This field resets the GPIO interrupt. 0: No action. 1: Reset interrupt.
15:0	Reserved	These bits are reserved.

SPI 0 Control 0

Read/Write MMIO_base + 0x020n00 Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCR R/W								Ph R/W	Pol R/W	Format R/W		DataSize R/W			

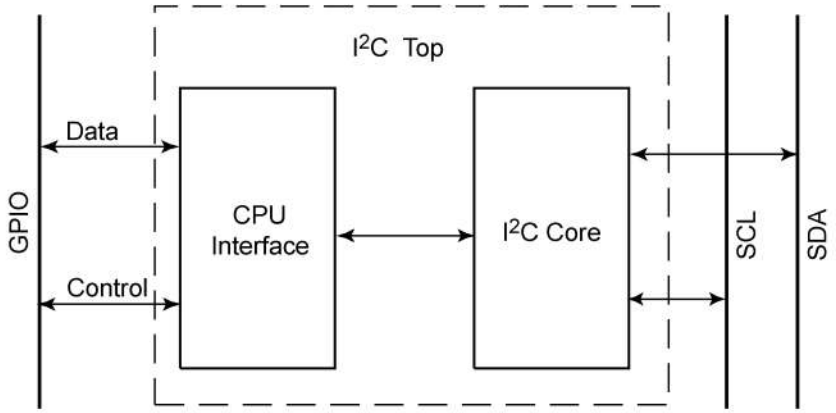
Bit(s)	Name	Description
31:16	Reserved	These bits are reserved.
15:8	SCR	Serial Clock Rate. The clock rate is calculated as follows: where CPSDVSR is an even value from 2 to 254, programmed via the Clock Prescale register. FSSPCLK CPSDVSR 1 + SCR( )×
7	Ph	SCLKOUT Phase for Motorola SPI Frame.
6	Pol	SCLKOUT Polarity for Motorola SPI Frame. 0: Rising edge. 1: Falling edge.
5:4	Format	Frame Format. 00: Motorola SPI frame format. 01: Texas Instruments serial frame format. 10: National Microwire frame format. 11: Reserved
3:0	DataSize	Data Size Select. 0000: Reserved 0001: Reserved 0010: Reserved 0011: 4-bit 0100: 5-bit 0101: 6-bit 0110: 7-bit 0111: 8-bit 1000: 9-bit 1001: 10-bit 1010: 11-bit 1011: 12-bit 1100: 13-bit 1011: 14-bit 1110: 15-bit 1111: 16-bit

8. I2C Interface

8.1 Functional Overview

The SM718 supports one I2C interface. The interface is in Master mode with 7-bit addressing. It supports speeds up to 400 kbps (Fast mode).

Figure 8-1 shows a simplified block diagram of the I2C interface.



8.2 Register Descriptions

The I2C registers are shown below :

Address	Type	Width	Reset Value	Register Name
0x010040	R/W	8	0x00	I2C Byte Count
0x010041	R/W	8	0x00	I2C Control
0x010042	R	8	0x00	I2C Status
0x010042	W	8	0x00	I2C Reset
0x010043	R/W	8	0x00	I2C Slave Address
0x010044 to 0x010053	R/W	8	0x00	I2C Data

Table 12: I2C Register Summary

I2C Byte Count

Read/Write MMIO_base + 0x010040

Power-on Default 0x00

7	6	5	4	3	2	1	0
Res				Count R/W			

Bit(s)	Name	Description
7:4	Res	These bits are reserved.
3:0	Count	Byte count -1.

I2C Control

Read/Write MMIO_base + 0x010041

Power-on Default 0x00

7	6	5	4	3	2	1	0
Res	Repeat R/W	IntAck R/W	Int R/W	Res	Status R/W	Mode R/W	E R/W

Bit(s)	Name	Description
7	Res	This bit is reserved.
6	Repeat	Repeated Start Enable: 0: Disable. 1: Enable.
5	IntAck	Interrupt Acknowledge: 0: Not acknowledge. 1: Acknowledge.
4	Int	Interrupt Enable: 0: Disable. 1: Enable.
3	Res	This bit is reserved.
2	Status	Start/Stop Status: 0: Stop. 1: Start.
1	Mode	Bus Speed Mode Selection: 0: Standard mode (100kbps). 1: Fast mode (400kbps).
0	E	Controller Enable: 0: Disable. 1: Enable.

I2C Status

Read MMIO_base + 0x010042

Power-on Default 0x00

7	6	5	4	3	2	1	0
Res				Comp R	Err R	Ack R	Busy R

Bit(s)	Name	Description
7:4	Res	These bits are reserved.
3	Comp	Whole Transfer Competed Status: 0: Transfer in progress. 1: Transfer completed.
2	Err	Bus Error Status: 0: Normal. 1: Error.
1	Ack	Slave Acknowledge Received Status: 0: Not received. 1: Received.
0	Busy	Bus Busy: 0: Idle. 1: Busy.

I2C Reset

Write MMIO_base + 0x010042

Power-on Default 0x00

7	6	5	4	3	2	1	0
Res					Err W	Res	

Bit(s)	Name	Description
7:3	Res	These bits are reserved.
2	Err	Bus Error Reset: 0: Clear. 1: Reserved.
1:0	Res	These bits are reserved.

I2C Slave Address

Read/Write MMIO_base + 0x010043

Power-on Default 0x00

7	6	5	4	3	2	1	0
Addr R/W							RW R/W

Bit(s)	Name	Description
7:1	Addr	7-bit Slave Address.
0	RW	Read/Write Selection: 0: Write. 1: Read.

I2C Data

Read/Write MMIO_base + 0x010044 to 0x010053

Power-on Default 0x00

7	6	5	4	3	2	1	0
Data R/W							

Bit(s)	Name	Description
7:0	Data	There are 16 I2C Data registers that hold the data to be written to or read from the I2C Slave. These registers can be accessed in 8-bit, 16-bit, or 32-bit mode for very fast FIFO transfer.

9. ZV Port

9.1 Functional Overview

This section covers the ZV Port and the Video Capture Unit.

9.1.1 ZV Port Overview

Incoming video data from the ZV Port can be interlaced or non-interlaced and YUV or RGB format. By disabling the video capture function, the ZV Port can be configured in output mode. In output mode, the ZV Port can send video data and 18-bit graphics in RGB format.

9.1.2 Video Capture Unit Overview

The Video Capture Unit captures incoming video data from the ZV Port and then stores the data into the frame buffer. The Video Capture Unit maintains display quality and balances the capture rate. Its key features are:

- 2-to-1 reduction for horizontal and vertical frame size
- YUV 4:2:2, YUV 4:2:2 with byte swapping, and RGB 5:6:5
- Interlaced data and non-interlaced data capture
- Single buffer and double buffer capture
- Cropping

The SM718 uses the Video Processor block to display captured data on the display (LCD, TV, or CRT). The Video Window displays the captured data. The Video Processor does the stretching, color interpolation, YUV-to-RGB conversion, and color key functions.

9.2 Programmer's Model

Figure 43 shows how this 64kB region in the MMIO space is laid out. It controls the ZV Port capture registers.

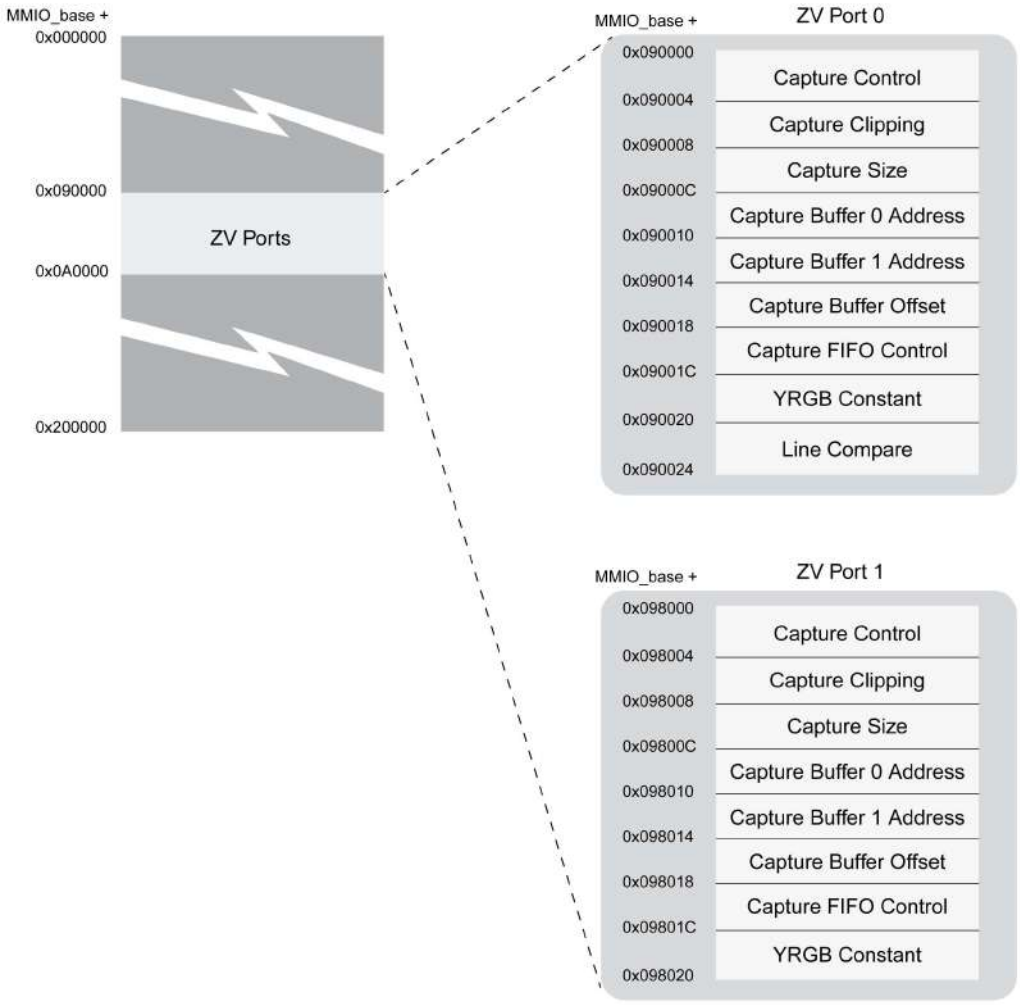


Figure 29: ZV Port Register Space

9.3 Register Descriptions

9.3.1 *ZV Port 0 Registers*

The ZV Port 0 registers are shown in Table 15.

Offset from MMIO_base[1]	Type	Width	Reset Value[2]	Register Name
0x090000	R/W	32	0b0000.XXXX.0000.0000. 0000.0000.0000.0000	Capture Control
0x090004	R/W	32	Undefined	Capture Clipping
0x090008	R/W	32	Undefined	Capture Size
0x09000C	R/W	32	Undefined	Capture Buffer 0 Address
0x090010	R/W	32	Undefined	Capture Buffer 1 Address
0x090014	R/W	32	Undefined	Capture Buffer Offset
0x090018	R/W	32	0x00000004	Capture FIFO Control
0x09001C	R/W	32	0x00EDEDED	YRGB Constant
0x090020	R/W	32	0x00000000	Line Compare

Table 13: Port 0 Register Summary

1. Refer to Table 5 on page 27 for MMIO_base values depending on the CPU.
2. In the reset values, “X” indicates don’t care.

Capture Control

Read/Write MMIO_base + 0x090000

Power-on Default 0b0000.XXXX.0000.0000.0000.0000.0000.0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				F R	I R	CB R	VSS R	Reserved				ADJ R/W	HA R/W	VS R/W	HS R/W
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FD R/W	VP R/W	HP R/W	CP R/W	UVS R/W	BS R/W	CS R/W	CF R/W	FS R/W	W R/W	B R/W	DB R/W	CC R/W	RGB R/W	656 R/W	E R/W

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27	F	Field Input Status. This bit is read-only. o: Even field. 1: Odd field.
26	I	Interlace Status. This bit is read-only. 0: Non-interlaced. 1: Interlaced.
25	CB	Current Buffer Status. This bit is read-only. 0: Capturing data into buffer 0. 1: Capturing data into buffer 1.
24	VSS	Vertical Sync Status. This bit is read-only. 0: VSync pulse is inactive. 1: VSync pulse is active.
23:20	Reserved	These bits are reserved.
19	ADJ	Delay HREF. 0: Do not delay HREF. 1: Delay HREF by one clock.
18	HA	Enable Horizontal Averaging. 0: Disable. 1: Enable.
17	VS	Enable 2÷1 Vertical Shrink. 0: Disable. 1: Enable.
16	HS	Enable 2÷1 Horizontal Shrink. 0: Disable. 1: Enable.
15	FD	Field Detect Method. 0: Rising edge of VSync. 1: Falling edge of VSync.
14	VP	Select VSync Phase. 0: Active high. 1: Active low.
13	HP	Select HRef Phase. 0: Active high. 1: Active low.
12	CP	Select Input Clock Polarity. 0: Active high. 1: Active low.
11	UVS	Enable UV Swap. 0: Disable. 1: Enable.
10	BS	Enable Byte Swap. 0: Disable. 1: Enable.
9	CS	Capture Size. 0: 16-bit. 1: 8-bit.

Bit(s)	Name	Description
8	CF	Capture Format. 0: YUV. 1: RGB.
7	FS	Enable Field Swap. 0: Disable. 1: Enable.
6	W	Enable Interlaced Data Capturing in Weave. 0: Disable. 1: Enable.
5	B	Enable Interlaced Data Capturing in Bob. 0: Disable. 1: Enable.
4	DB	Enable Double Buffering. 0: Disable. 1: Enable.
3	CC	Select Capture Control. 0: Continuous capture. 1: Conditional capture by using the S bit.
2	RGB	Enable YUV to RGB Color Conversion. 0: Disable. 1:Enable.
1	66	Enable 8-bit ITU-656 Input. 0: Disable. 1: Enable.
0	E	Enable Capture. 0: Disable. 1: Enable.

Capture Clipping

Read/Write MMIO_base + 0x090004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						EYClip R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						XClip R/W									

Bit(s)	Name	Description
31:26	Reserved	These bits are reserved.
25:16	EYClip	Number of lines to skip after VSync for even field.
15:10	Reserved	These bits are reserved.
9:0	XClip.	Number of pixels to skip after HRef.

Capture Size

Read/Write MMIO_base + 0x090008

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					Height R/W										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					Width R/W										

Bit(s)	Name	Description
31:27	Reserved	These bits are reserved.
26:16	Height	Number of lines to capture.
15:11	Reserved	These bits are reserved.
10:0	Width	Number of pixels to capture.

Capture Buffer 0 Address

Read/Write MMIO_base + 0x09000C

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Reserved			Ext R/W	CS R/W	Memory Address R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Memory Address R/W												0000			

Bit(s)	Name	Description
31	S	Status Bit. 0: Flip not pending. 1: Flip pending.
30:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: External memory.
26	CS	Chip Select for External Memory. 0: CS0 of external memory. 1: CS1 of external memory.
25:4	Memory Address	Memory address of capture buffer 0 with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Capture Buffer 1 Address

Read/Write MMIO_base + 0x090010

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Reserved			Ext R/W	CS R/W	Memory Address R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Memory Address R/W												0000			

Bit(s)	Name	Description
31	S	Status Bit. 0: Flip not pending. 1: Flip pending.
30:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: External memory.
26	CS	Chip Select for External Memory. 0: CS0 of external memory. 1: CS1 of external memory.
25:4	Memory Address	Memory address of capture buffer 1 with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Capture Buffer Offset

Read/Write MMIO_base + 0x090014

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						OYClip									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Offset R/W												0000			

Bit(s)	Name	Description
31:26	Reserved	These bits are reserved.
25:16	OYClip	Number of lines to skip after VSync for odd field.
15:4	Offset	Number of 128-bit aligned bytes per line of the capture buffer.
3:0	0000	These bits are hardwired to zeros.

Capture FIFO Control

Read/Write MMIO_base + 0x090018

Power-on Default 0x00000004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													FIFO R/W		

Bit(s)	Name	Description
31:3	Reserved	These bits are reserved.
2:0	FIFO	FIFO Request Level. When the FIFO empty level reaches the level specified, a FIFO read request will be generated. 000: 2 or more empty. 001: 3 or more empty. 010: 4 or more empty. 011: 5 or more empty. 100: 6 or more empty. 101: 8 or more empty. 110: 10 or more empty. 111: 12 or more empty.

YRGB Constant

Read/Write MMIO_base + 0x09001C

Power-on Default 0x00EDEDED

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Y R/W								R R/W							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
G R/W								B R/W							

Bit(s)	Name	Description
31:24	Y	Y Adjustment.
23:16	R	Red Conversion Constant.
15:8	G	Green Conversion Constant.
7:0	B	B Blue Conversion Constant.

Line Compare

Read/Write MMIO_base + 0x090020

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					L-COMP R/W										

Bit(s)	Name	Description
31:11	Reserved	These bits are reserved.
10:0	L-COMP	Line Compare. The current line number is used to trigger the Primary Display display.

9.3.2 *ZV Port 1 Registers*

The ZV Port 1 registers are shown in Table 16.

Offset from MMIO_base[1]	Type	Width	Reset Value[2]	Register Name
0x098000	R/W	32	0b0000.XXXX.0000.0000. 0000.0000.0000.0000	Capture Control
0x098004	R/W	32	Undefined	Capture Clipping
0x098008	R/W	32	Undefined	Capture Size
0x09800C	R/W	32	Undefined	Capture Buffer 0 Address
0x098010	R/W	32	Undefined	Capture Buffer 1 Address
0x098014	R/W	32	Undefined	Capture Buffer Offset
0x098018	R/W	32	0x00000004	Capture FIFO Control
0x09801C	R/W	32	0x00EDEDED	YRGB Constant

Table 14: ZV Port 1 Register Summary

Capture Control

Read/Write MMIO_base + 0x098000

Power-on Default 0b0000.XXXX.0000.0000.0000.0000.0000.0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				F R	I R	CB R	VSS R	Reserved			Panel R/W	ADJ R/W	HA R/W	VS R/W	HS R/W
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FD R/W	VP R/W	HP R/W	CP R/W	UVS R/W	BS R/W	CS R/W	CF R/W	FS R/W	W R/W	B R/W	DB R/W	CC R/W	RGB R/W	656 R/W	E R/W

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27	F	Field Input Status. This bit is read-only. o: Even field. 1: Odd field.
26	I	Interlace Status. This bit is read-only. 0: Non-interlaced. 1: Interlaced.
25	CB	Current Buffer Status. This bit is read-only. 0: Capturing data into buffer 0. 1: Capturing data into buffer 1.
24	VSS	Vertical Sync Status. This bit is read-only. 0: VSync pulse is inactive. 1: VSync pulse is active.
23:21	Reserved	These bits are reserved.
20	Panel	Enable Capture Panel Output. 0: Disable. 1: Enable.
19	ADJ	Delay HREF. 0: Do not delay HREF. 1: Delay HREF by one clock.
18	HA	Enable Horizontal Averaging. 0: Disable. 1: Enable.
17	VS	Enable 2÷1 Vertical Shrink. 0: Disable. 1: Enable.
16	HS	Enable 2÷1 Horizontal Shrink. 0: Disable. 1: Enable.
15	FD	Field Detect Method. 0: Rising edge of VSync. 1: Falling edge of VSync.
14	VP	Select VSync Phase. 0: Active high. 1: Active low.
13	HP	Select HRef Phase. 0: Active high. 1: Active low.
12	CP	Select Input Clock Polarity. 0: Active high. 1: Active low.
11	UVS	Enable UV Swap. 0: Disable. 1: Enable.
10	BS	Enable Byte Swap. 0: Disable. 1: Enable.

Bit(s)	Name	Description
9	CS	Capture Size. 0: 16-bit. 1: 8-bit.
8	CF	Capture Format. 0: YUV. 1: RGB.
7	FS	Enable Field Swap. 0: Disable. 1: Enable.
6	W	Enable Interlaced Data Capturing in Weave. 0: Disable. 1: Enable.
5	B	Enable Interlaced Data Capturing in Bob. 0: Disable. 1: Enable.
4	DB	Enable Double Buffering. 0: Disable. 1: Enable.
3	CC	Select Capture Control. 0: Continuous capture. 1: Conditional capture by using the S bit.
2	RGB	Enable YUV to RGB Color Conversion. 0: Disable. 1:Enable.
1	656	Enable 8-bit ITU-656 Input. 0: Disable. 1: Enable.
0	E	Enable Capture. 0: Disable. 1: Enable.

Capture Clipping

Read/Write MMIO_base + 0x098004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						EYClip R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						XClip R/W									

Bit(s)	Name	Description
31:26	Reserved	These bits are reserved.
25:16	EYClip	Number of lines to skip after VSync for even field.
15:10	Reserved	These bits are reserved.
9:0	XClip.	Number of pixels to skip after HRef.

Capture Size

Read/Write MMIO_base + 0x098008

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					Height R/W										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					Width R/W										

Bit(s)	Name	Description
31:27	Reserved	These bits are reserved.
26:16	Height	Number of lines to capture.
15:11	Reserved	These bits are reserved.
10:0	Width	Number of pixels to capture.

Capture Buffer 0 Address

Read/Write MMIO_base + 0x09800C

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Reserved			Ext R/W	CS R/W	Memory Address R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Memory Address R/W												0000			

Bit(s)	Name	Description
31	S	Status Bit. 0: Flip not pending. 1: Flip pending.
30:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: External memory.
26	CS	Chip Select for External Memory. 0: CS0 of external memory. 1: CS1 of external memory
25:4	Memory Address	Memory address of capture buffer 0 with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Capture Buffer 1 Address

Read/Write MMIO_base + 0x098010

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Reserved			Ext R/W	CS R/W	Memory Address R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Memory Address R/W												0000			

Bit(s)	Name	Description
31	S	Status Bit. 0: Flip not pending. 1: Flip pending.
30:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: External memory.
26	CS	Chip Select for External Memory. 0: CS0 of external memory. 1: CS1 of external memory.
25:4	Memory Address	Memory address of capture buffer 1 with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Capture Buffer Offset

Read/Write MMIO_base + 0x098014

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						OYClip									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Offset R/W												0000			

Bit(s)	Name	Description
31:26	Reserved	These bits are reserved.
25:16	OYClip	Number of lines to skip after VSync for odd field.
15:4	Offset	Number of 128-bit aligned bytes per line of the capture buffer.
3:0	0000	These bits are hardwired to zeros.

Capture FIFO Control

Read/Write MMIO_base + 0x098018

Power-on Default 0x00000004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													FIFO R/W		

Bit(s)	Name	Description
31:3	Reserved	These bits are reserved.
2:0	FIFO	FIFO Request Level. When the FIFO empty level reaches the level specified, a FIFO read request will be generated. 000: 2 or more empty. 001: 3 or more empty. 010: 4 or more empty. 011: 5 or more empty. 100: 6 or more empty. 101: 8 or more empty. 110: 10 or more empty. 111: 12 or more empty.

YRGB Constant

Read/Write MMIO_base + 0x09801C

Power-on Default 0x00EDEDED

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Y R/W								R R/W							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
G R/W								B R/W							

Bit(s)	Name	Description
31:24	Y	Y Adjustment.
23:16	R	Red Conversion Constant.
15:8	G	Green Conversion Constant.
7:0	B	B Blue Conversion Constant.

10. DMA Controller (DMAC)

10.1 Functional Overview

In the SM718, the Display Controller, Command Interpreter, Draw Engine, and DMA can access system memory through the on-chip system memory controller (see Figure 44).

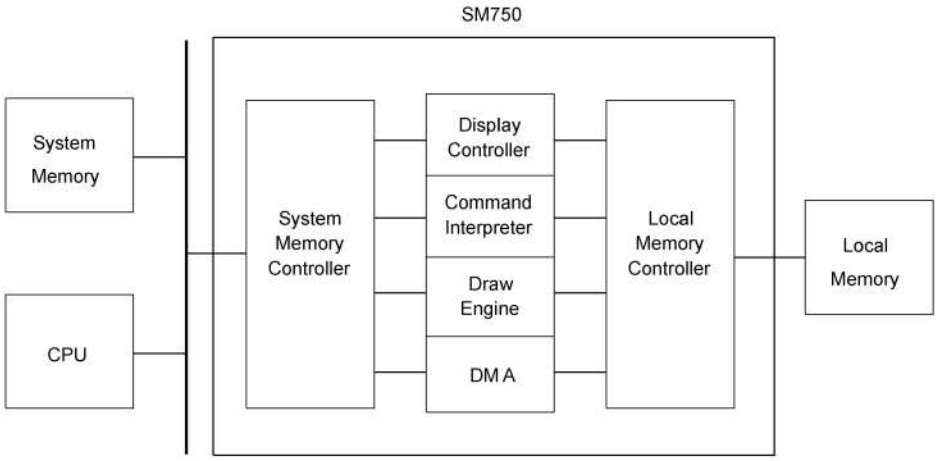


Figure 30: SM718 Functional Block Connections to Memory Controllers

The DMA channel within the SM718 handles memory data transfers, thus offloading the CPU. The DMA channel moves data between internal and system memory.

- DMA1 – Moves data between system memory and local memory (see Figure 45)
  There are four ways to transfer data in DMA1:
  - System memory to system memory
  - System memory to local memory
  - Local memory to system memory
  - Local memory to local memory

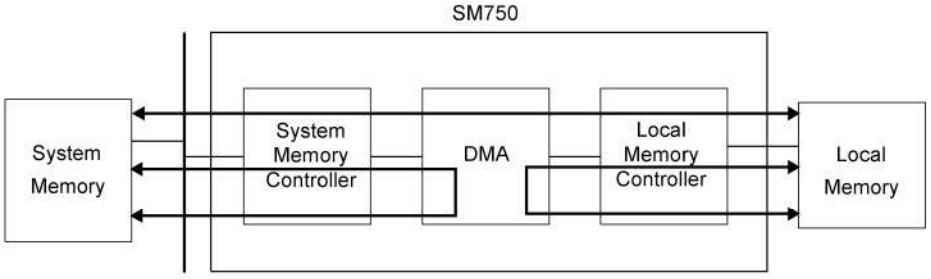
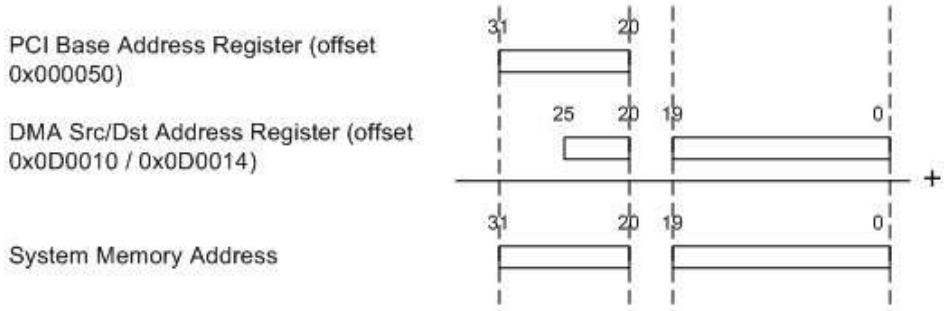


Figure 31: DMA Channel 1

System Memory Addressing Mechanism

When DMA uses bus master to access system memory, it uses the following decoding method:

SM718 DMA Addressing Method



10.2 Register Descriptions

Figure 46 shows how this 64kB region in the MMIO space is laid out. It controls the DMA registers.

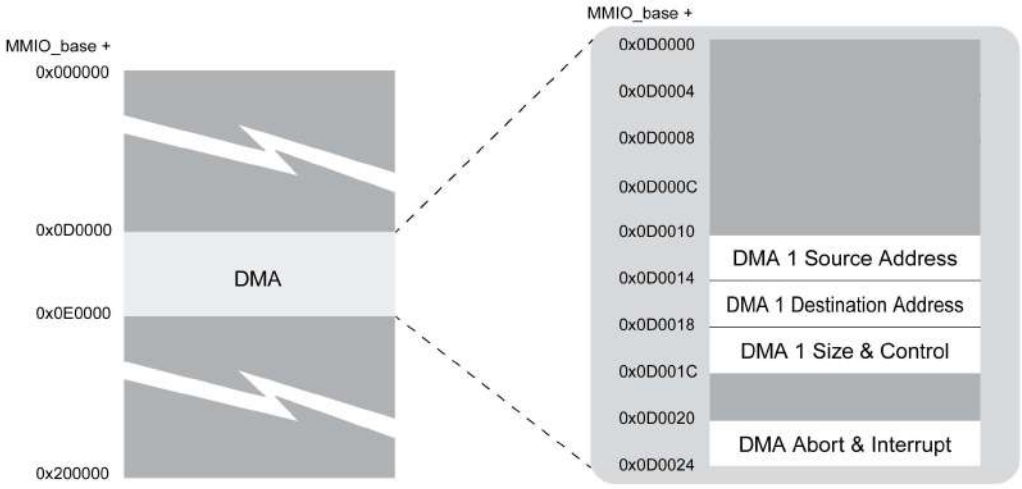


Figure 32: DMA Register Space

Table 17 shows the DMA Controller registers.

Offset from MMIO_base[1]	Type	Width	Reset Value	Register Name
0x0D0010	R/W	32	0x00000000	DMA 1 Source Address
0x0D0014	R/W	32	0x00000000	DMA 1 Destination Address
0x0D0018	R/W	32	0x00000000	DMA 1 Size & Control
0x0D0020	R/W	32	0x00000000	DMA Abort & Interrupt

Table 15: DMA Controller Register Summary

1. Refer to Table 5 on page 27 for MMIO_base values depending on the CPU.

DMA 1 Source Address

Read/Write MMIO_base + 0x0D0010

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				Ext R/W	CS R/W	Memory Address R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Memory Address R/W														0	0

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:2	Memory Address	Memory address with 32-bit alignment.
1:0	00	00 These bits are hardwired to zeros.

DMA 1 Destination Address

Read/Write MMIO_base + 0x0D0014

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				Ext R/W	CS R/W	Memory Address R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Memory Address R/W														0	0

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:2	Memory Address	Memory address with 32-bit alignment.
1:0	00	00 These bits are hardwired to zeros.

DMA 1 Size & Control

Read/Write MMIO_base + 0x0D0018

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Act R/W	Reserved							Size R/W							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Size R/W														0	0

Bit(s)	Name	Description
31	Act	DMA Channel 1 Activation. The Act bit will be cleared to "0" by the hardware when the DMA is finished. 0: Idle. 1: Activate DMA channel 1.
30:24	Reserved	These bits are reserved.
23:2	Size	Number of 32-bit aligned bytes to transfer (up to 16MB).
1:0	00	These bits are hardwired to zeros.

DMA Abort & Interrupt

Read/Write MMIO_base + 0x0D0020

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										$Abort_{1:0}$ R/W		Reserved		$Int_{1:0}$ R/W	

Bit(s)	Name	Description
31:6	Reserved	These bits are reserved.
5:4	$Abort_{1:0}$	Enable or Abort DMA Channel. Aborting will reset the corresponding DMA controller. For normal operation, the Abort bits should be set to "0". 0: Enable corresponding DMA channel. 1: Abort corresponding DMA channel.
3:2	Reserved	These bits are reserved.
1:0	$Int_{1:0}$	Interrupt Status Bit. The Int bit should be cleared to "0" by software when the interrupt has been serviced. Writing a "1" has no effect. 0: DMA is not active or still busy – no interrupt. 1: DMA is finished – interrupt.

11. PWM Specification

11.1 Functional Overview

The Pulse Width Modulation (PWM) module is a simple counter that can pulse with programmable pulse widths. The pulse optionally can be tied to the PWM interrupt signal to generate a periodic interrupt for timing or watchdog support. The input clock is the peripheral clock at 96 MHz. The output pulse starts high.

he following subsections provide some different samples of PWM usage.

11.1.1 Delay Counter with Interrupt

Any of the three available PWM circuits can be programmed to perform a single shot delay. Once the delay is finished, an interrupt is triggered. The required delay is assumed to be 20 ms.

The values for the PWM n register are calculated as follows:

- Delay * clock = 20 ms * 96 MHz = 1,920,000
- A 50% duty cycle means 960,000 clocks are LOW and 960,000 clocks are HIGH
- The shift to a 12-bit value is done by dividing by 2^8: (3,750 – 1) clocks LOW and (3,750 – 1) clocks HIGH
- The value for the PWM n register is: 0xEA5EA585

11.1.2 Internal Timer with Interrupt

Any of the three available PWM circuits can be programmed to act as a periodic timer to support a clock. The periodic timer generates an interrupt after each cycle. The required periodic interval is assumed to be 1 s. For this example, there is a 30/70% duty cycle.

The values for the PWM n register are calculated as follows:

- Delay * clock = 1 s * 96 MHz = 96,000,000
- A 30% duty cycle means 28,800,000 clocks are LOW and 67,200,000 clocks are HIGH
- The shift to a 12-bit value is done by dividing by 2^{15}: (879 – 1) clocks LOW and (2,051 – 1) clocks HIGH
- The value for the PWM n register is: 0x80236EF5

11.1.3 External Pulse

In this example, the PWM is programmed for an external pulse with a frequency of 44.1 kHz and a duty cycle of 15%.

The values for the PWM n register are calculated as follows:

- Delay * clock = (1 / 44.1 kHz) * 96 MHz = 2,177
- A 15% duty cycle means (327 – 1) clocks are LOW and (1,850 – 1) clocks are HIGH
- The value for the PWM n register is: 0x73914601

11.2 Register Descriptions

The PWM registers are shown in Table 18.

Offset from MMIO_base[1]	Type	Width	Reset Value	Register Name
0x010020	R/W	32	0x00000000	PWM 0
0x010024	R/W	32	0x00000000	PWM 1
0x010028	R/W	32	0x00000000	PWM 2

Table 16: PWM Register Summary

The PWM registers control the three PWM pins. It contains three registers, one for each PWM pin. Figure 47 defines the register layout for the PWM registers.

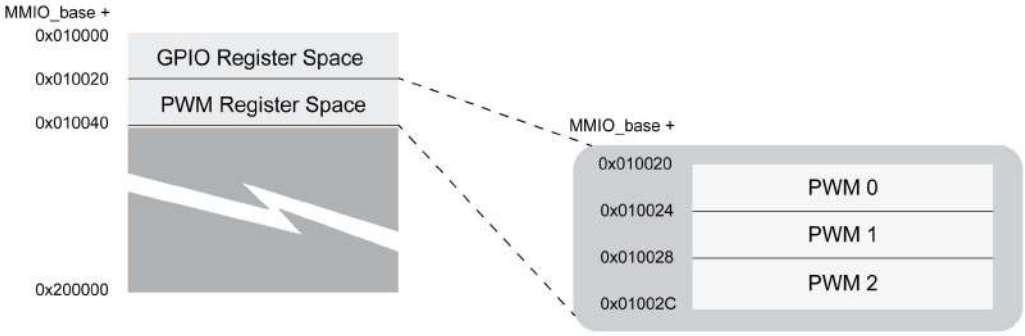


Figure 33: PWM Register Space

PWM 0

Read/Write Address 0x010020

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
High Counter R/W												Low Counter R/W			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Low Counter R/W								Clock Divide R/W				IP R/W	I R/W	Res	E R/W

Bit(s)	Name	Description
31:20	High Counter	Number of clocks – 1 the PWM should remain high before switching to low.
19:8	Low Counter	Number of clocks – 1 the PWM should remain low before switching to high.
7:4	Clock Divide	Select divisor for 96MHz input clock.
3	IP	PWM Interrupt Pending. In order to clear a pending interrupt, write a "1" in the IP bit. 0: No interrupt pending. 1: Interrupt pending.
2	I	Enable or Disable PWM Interrupt. 0: Disable PWM interrupt. 1: Enable PWM interrupt whenever a single cycle is completed.
1	Res	This bit is reserved.
0	E	Enable or Disable the PWM. 0: Disabled. 1: Enabled.

0000	÷ 1	96MHz	1000	÷ 256	375kHz
0001	÷ 2	48MHz	1001	÷ 512	187.5kHz
0010	÷ 4	24MHz	1010	÷ 1,024	93.75kHz
0011	÷ 8	12MHz	1011	÷ 2,048	46.875kHz
0100	÷ 16	6MHz	1100	÷ 4,096	23.438kHz
0101	÷ 32	3MHz	1101	÷ 8,192	11.719kHz
0110	÷ 64	1.5MHz	1110	÷ 16,384	5.859kHz
0111	÷ 128	750kHz	1111	÷ 32,768	2.93kHz

PWM 1

Read/Write Address 0x010024

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
High Counter R/W												Low Counter R/W			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Low Counter R/W								Clock Divide R/W				IP	I	Res	E

Bit(s)	Name	Description
31:20	High Counter	Number of clocks – 1 the PWM should remain high before switching to low.
19:8	Low Counter	Number of clocks – 1 the PWM should remain low before switching to high.
7:4	Clock Divide	Select divisor for 96MHz input clock. 0000 ÷ 1 96MHz; 1000 ÷ 256 375kHz 0001 ÷ 2 48MHz; 1001 ÷ 512 187.5kHz 0010 ÷ 4 24MHz; 1010 ÷ 1,024 93.75kHz 0011 ÷ 8 12MHz; 1011 ÷ 2,048 46.875kHz 0100 ÷ 16 6MHz; 1100 ÷ 4,096 23.438kHz 0101 ÷ 32 3MHz; 1101 ÷ 8,192 11.719kHz 0110 ÷ 64 1.5MHz; 1110 ÷ 16,384 5.859kHz 0111 ÷ 128 750kHz; 1111 ÷ 32,768 2.93kHz
3	IP	PWM Interrupt Pending. In order to clear a pending interrupt, write a “1” in the IP bit. 0: No interrupt pending. 1: Interrupt pending.
2	I	Enable or Disable PWM Interrupt. 0: Disable PWM interrupt. 1: Enable PWM interrupt whenever a single cycle is completed.
1	Res	This bit is reserved.
0	E	0 E Enable or Disable the PWM. 0: Disabled. 1: Enabled.

PWM 2

Read/Write Address 0x010028

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
High Counter R/W												Low Counter R/W			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Low Counter R/W								Clock Divide R/W				IP R/W	I R/W	Res	E R/W

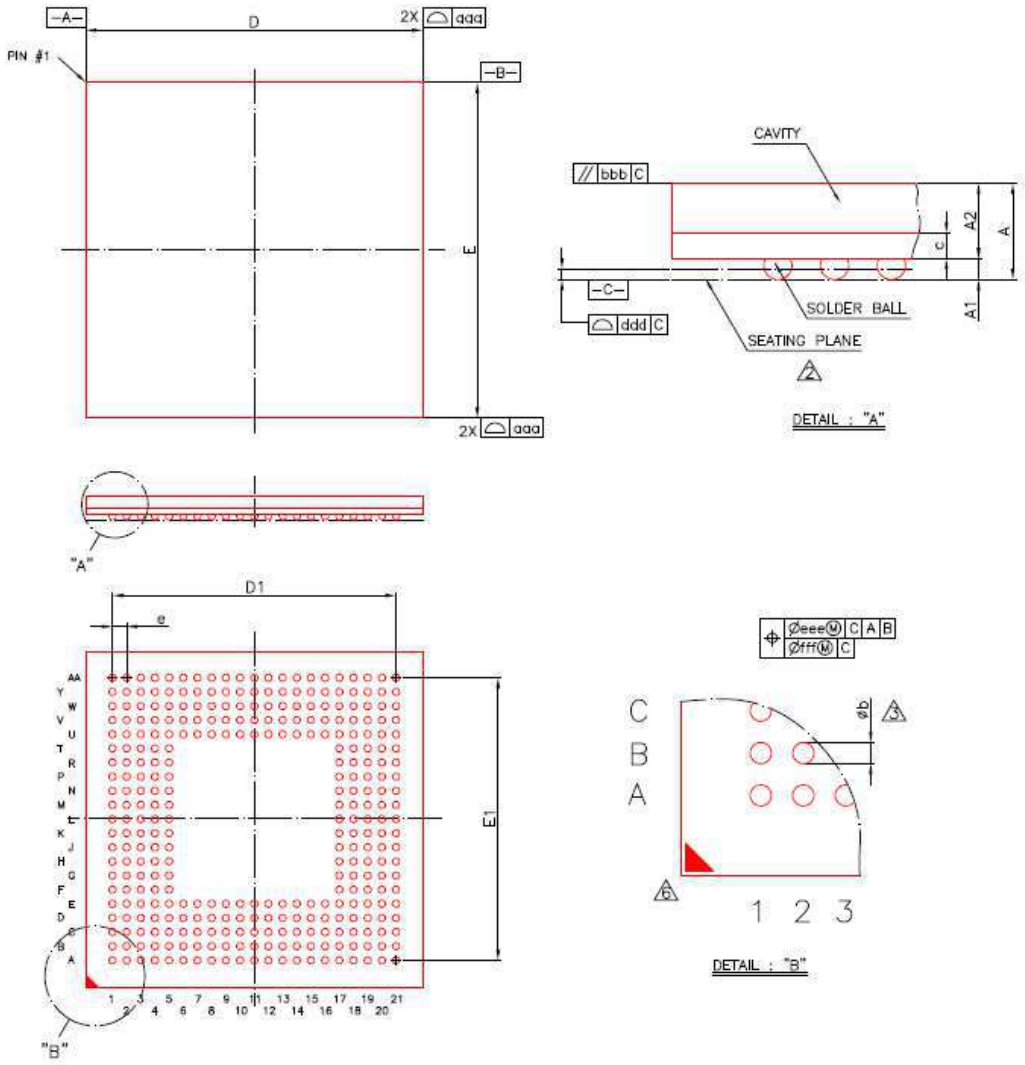
Bit(s)	Name	Description
31:20	High Counter	Number of clocks – 1 the PWM should remain high before switching to low.
19:8	Low Counter	Number of clocks – 1 the PWM should remain low before switching to high.
7:4	Clock Divide	Select divisor for 96MHz input clock.
3	IP	PWM Interrupt Pending. In order to clear a pending interrupt, write a “1” in the IP bit. 0: No interrupt pending. 1: Interrupt pending.
2	I	Enable or Disable PWM Interrupt. 0: Disable PWM interrupt. 1: Enable PWM interrupt whenever a single cycle is completed.
1	Res	This bit is reserved.
0	E	Enable or Disable the PWM. 0: Disabled. 1: Enabled.

0000	÷ 1	96MHz	1000	÷ 256	375kHz
0001	÷ 2	48MHz	1001	÷ 512	187.5kHz
0010	÷ 4	24MHz	1010	÷ 1,024	93.75kHz
0011	÷ 8	12MHz	1011	÷ 2,048	46.875kHz
0100	÷ 16	6MHz	1100	÷ 4,096	23.438kHz
0101	÷ 32	3MHz	1101	÷ 8,192	11.719kHz
0110	÷ 64	1.5MHz	1110	÷ 16,384	5.859kHz
0111	÷ 128	750kHz	1111	÷ 32,768	2.93kHz

12. Packaging Information

12.1 Packaging

The SM718 is available in a 320-pin BGA package. The total package size is 19mm x 19mm.



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.46	---	---	0.057
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	1.01	1.06	1.11	0.040	0.042	0.044
b	0.35	0.40	0.45	0.014	0.016	0.018
c	0.32	0.36	0.40	0.013	0.014	0.016
D	18.90	19.00	19.10	0.744	0.748	0.752
E	18.90	19.00	19.10	0.744	0.748	0.752
D1	---	16.00	---	---	0.630	---
E1	---	16.00	---	---	0.630	---
e	---	0.80	---	---	0.031	---
aaa	0.15			0.006		
bbb	0.20			0.008		
ddd	0.20			0.008		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	21/21			21/21		

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. REFERENCE DOCUMENT : JEDEC MO-205.
6. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .
7. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd

13. Specifications

13.1 Soldering Profile

Figure 50 shows the soldering profile for the SM718 device. This profile is designed for use with Sn63 or Sn62 (tin measurements in the PCB) and can serve as a general guideline in establishing a reflow profile.

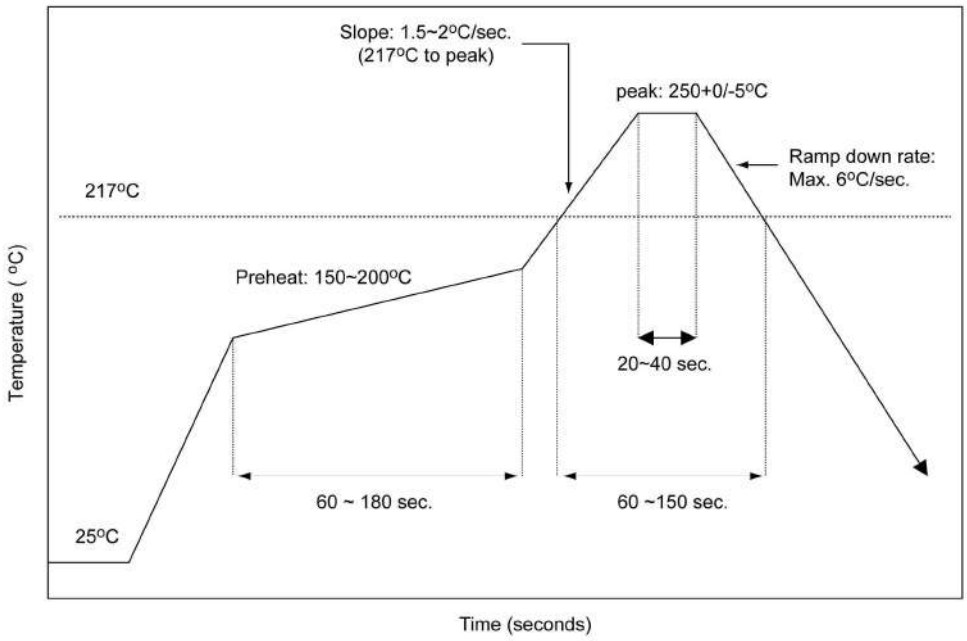


Figure 34: Temperature Profile

The reflow profile is defined as follows:

- Average ramp-up rate (217℃ to peak): 1.5~2℃/seco nd
- Preheat (150~200℃): 60~180 seconds
- Temperature maintained above 217℃: 60~150 seconds
- Time within 5℃ of actual peak temperature: 20 ~ 4 0 seconds
- Peak temperature: 250+0/-5℃
- Ramp-down rate: 6℃/second max.
- Time 25℃ to peak temperature: 8 minutes max.
- Cycle interval: 5 minutes

13.2 DC Characteristics

Parameter	MIN.	TYP.	MAX.	Units
Operation Temperature	0		75	degrees C
VDDI/O1 with respect to VSS	3.125	3.3	3.465	V
VDD core with respect to VSS	1.1.14	1.2	1.26	V
Voltage on I/O pins with respect to VSS	-0.5		VDD + 5%	V

1. VDD I/O refers to AVDD, GVDD, HVDD, PVDD, XTALPWR.

Table 17: Recommend Operating Condition

Parameter	MAX.	Unites
VDDI/O1 with respect to VSS	3.3 +/- 5%	V
VDD core with respect to VSS	1.2 +/- 5%	V
ESD Rating(Human Body) , all signal pins	> 2000	V
ESD Rating(Human Body), all VDD pins (AVDD,PVDD,VDD)	> 1500	V
Voltage on I/O pins with respect to VSS	-0.5V to VDD + 5%	V

1. VDD I/O refers to AVDD, GVDD, HVDD, PVDD, XTALPWR.

Table 18: Absolute Rating

Symbol	Parameter	Min	Max	Units
V_{IL}	Input Low Voltage	-0.3	0.8	V
V_{IH}	Input High Voltage	2.4	5.5	V
V_{OL}	Output Low Voltage	–	0.4	V
V_{OH}	Output High Voltage	2.8	VDD + 0.5	V
I_{OZL}	Output 3-State Current	–	10	µA
I_{OZH}	Output 3-State Current	–	10	µA
I_{OZL} (pull up pins)	Output 3-State Current	-130	-10	µA
I_{OZH} (pull up pins)	Output 3-State Current	–	10	µA
I_{OZL} (pull down pins)	Output 3-State Current	–	10	µA

I_{OZH} (pull down pins)	Output 3-State Current	10	130	µA
C_{IN}	Input Capacitance	–	7	pF
C_{OUT}	Output Capacitance	–	7	pF

Table 19: DC Characteristics

13.3 AC Timing

This section provides the AC timing waveforms and parameters:

- "PCI and Host Timing"
- "Display Controller Timing"
- "ZV Port Timing"
- "Local DDR Timing"

13.3.1 PCI and Host Timing

PCI Interface Timing

Figure 18-2 shows the PCI clock and its timing parameters. Table 18-3 provides the values for the PCI clock timing parameters shown in Figure 18-2.

Figure 18-2: PCI Clock Timing

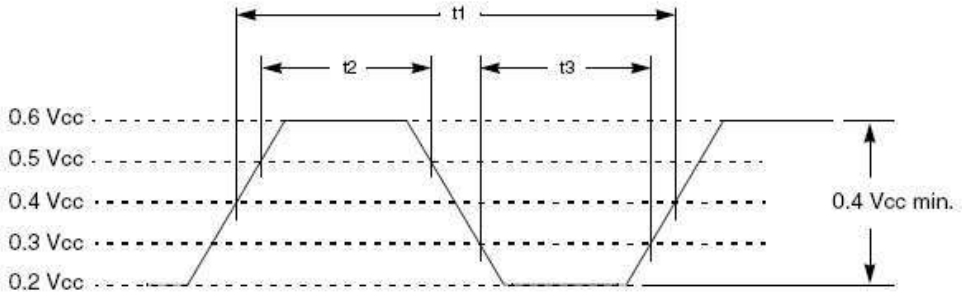


Table 18-3: PCI Clock Timing Parameters

Sym	Parameter	66 MHz		33 MHz		Unit
		Min	Max	Min	Max	
t1	CLK cycle time	15	30	30		ns
t2	CLK high time	6		11		ns
t3	CLK low time	6		11		ns
–	CLK skew rate	1.5	4	1	4	V/ns

Figure 18-3 and Figure 18-4 show the PCI outputs and inputs, respectively, and their relationship to the PCI clock. Table 18-4 provides the values for the timing parameters shown in the two figures.

Figure 18-3: PCI Clock to Output Timing

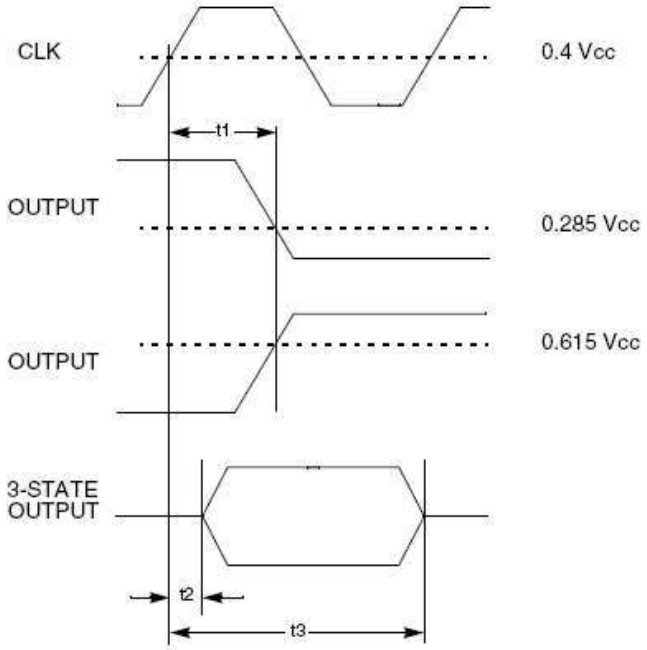


Figure 18-4: PCI Clock to Input Timing

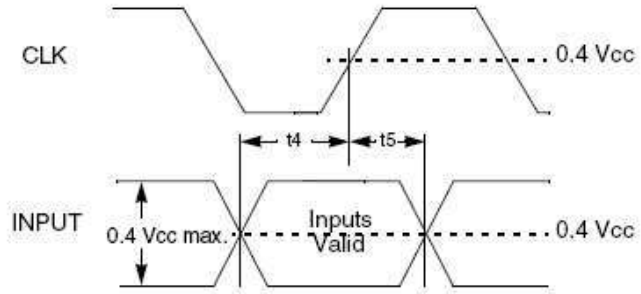


Table 18-4: PCI I/O Timing Parameters

Sym	Parameter	66 MHz		33 MHz		Unit
		Min	Max	Min	Max	
t1	CLK to signal valid delay	2	6	2	11(12)[1]	ns
t2	Float to active delay	2		2		ns
t3	Active to float delay		14		28	ns
t4	Input setup time to CLK	3(5)		7(10.12)		ns
t5	Input hold time from CLK	0		0		ns

1. Values shown in parentheses are for point-to-point signals.

Figure 18-5 shows the remaining timing PCI bus waveforms. Table 18-5 provides the values for the timing parameters shown in Figure 18-5.

Figure 18-5: PCI Bus Timing Diagram

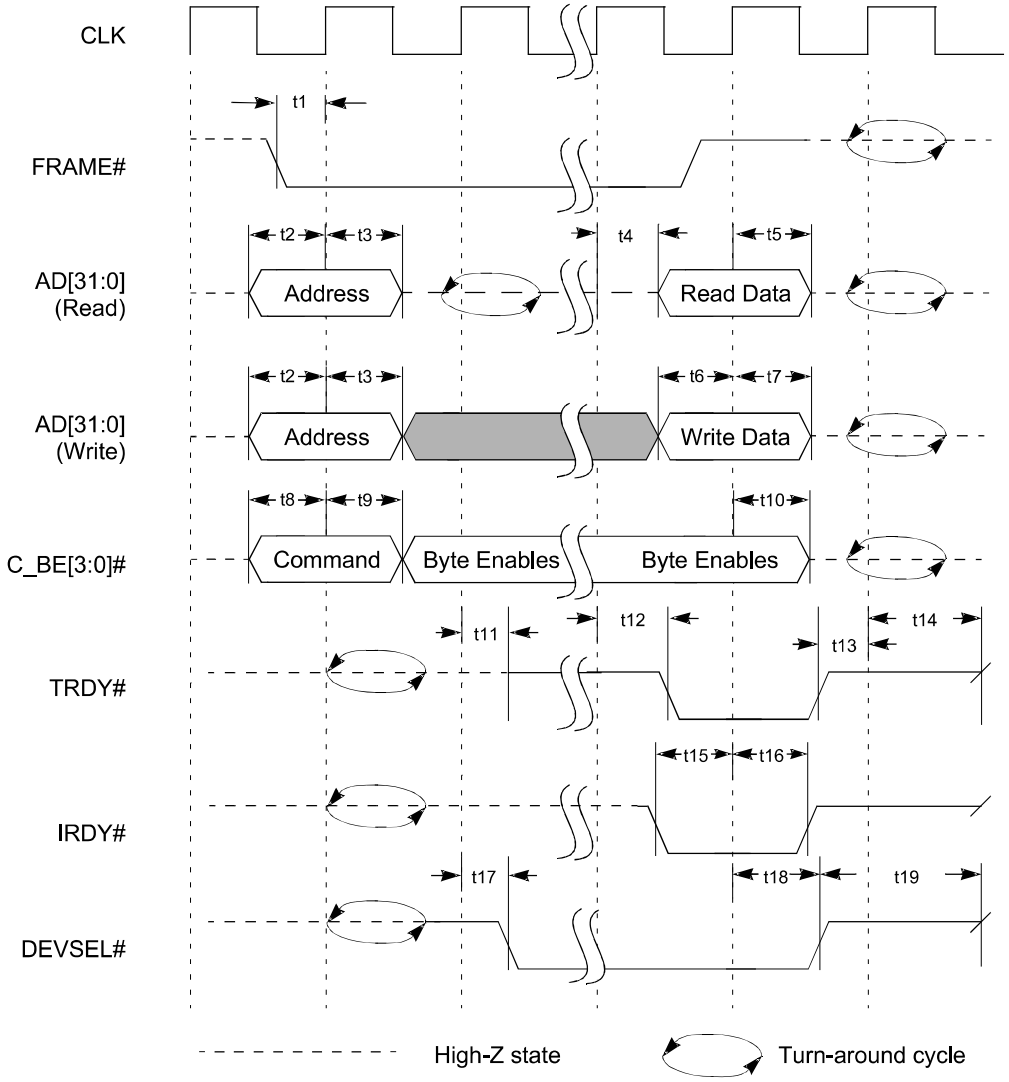


Table 18-5: PCI Bus Timing Parameters (33 MHz)

Symbol	Parameter	Min	Max	Unit
t1	FRAME# setup to CLK	7	-	ns
t2	AD[31:0] (address) setup to CLK	7	-	ns
t3	AD[31:0] (address) hold from CLK	0	-	ns
t4	AD[31:0] (Read Data) valid from CLK	2	11	ns
t5	AD[31:0] (Read Data) hold from CLK	0	-	ns
t6	AD[31:0] (Write Data) setup to CLK	7	-	ns
t7	AD[31:0] (Write Data) hold from CLK	0	-	ns
t8	C/BE[3:0]# (Command) setup to CLK	7	-	ns
t9	C/BE[3:0]# (Command) hold from CLK	0	-	ns
t10	C/BE[3:0]# (Byte Enable) hold from CLK	0	-	ns
t11	TRDY High-Z to High from CLK	2	-	ns
t12	TRDY# active from CLK	2	11	ns
t13	TRDY# inactive from CLK	2	11	ns
t14	TRDY# High before High-Z	1T	-	CLK
t15	IRDY# setup to CLK	7	-	ns
t16	IRDY# hold from CLK	0	-	ns
t17	DEVSEL# active from CLK	2	11	ns
t18	DEVSEL# inactive from CLK	2	11	ns
t19	DEVSEL# High before High-Z	1T	-	CLK

Marvell PXA250/270 Host

Figure 18-6 shows the timing waveforms for Marvell PXA250/270 System DRAM operations. Figure 18-7 shows the timing waveforms for Marvell PXA250/270 read operations. Figure 18-8 shows the timing waveforms for Marvell PXA250/270 write operations. Table 18-6 lists the AC timing values for the parameters shown in the three Marvell PXA250/270 figures.

Figure 18-6: Marvell PXA250/270 System DRAM (Master) Timing

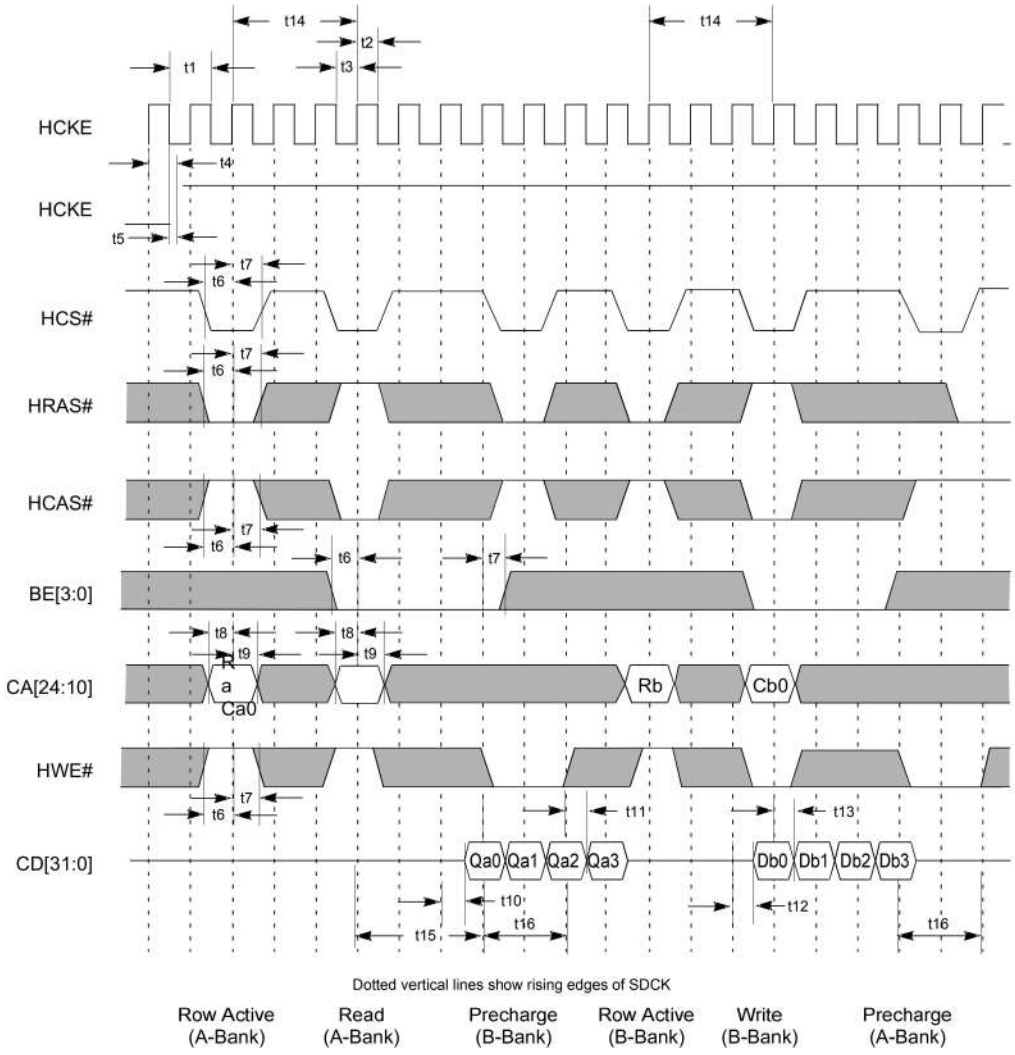


Figure 18-7: Marvell PXA250/270 Read Timing

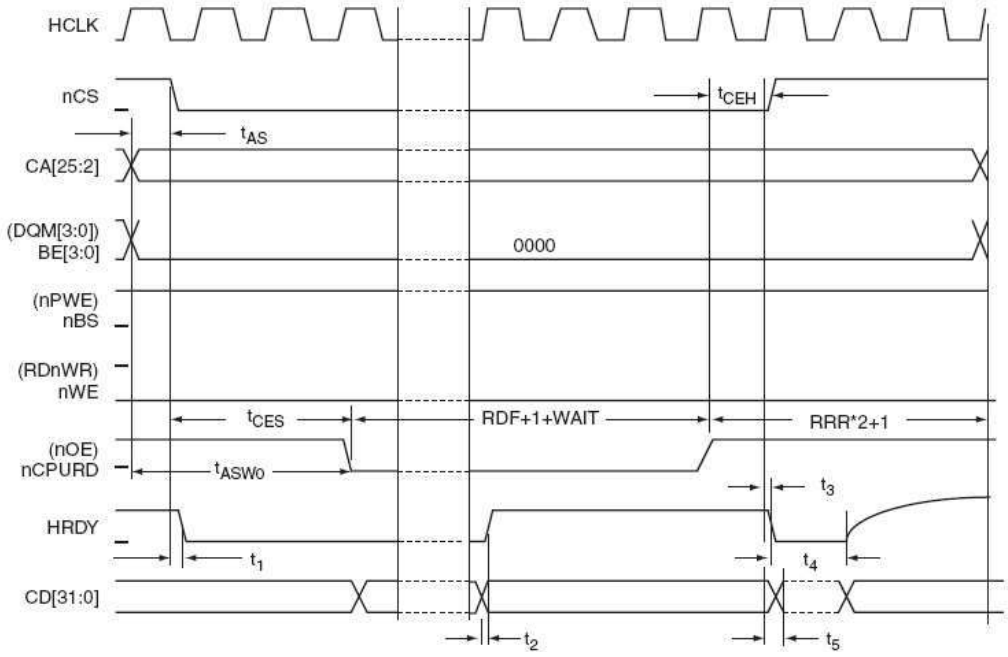


Figure 18-8: Marvell PXA250/270 Write Timing

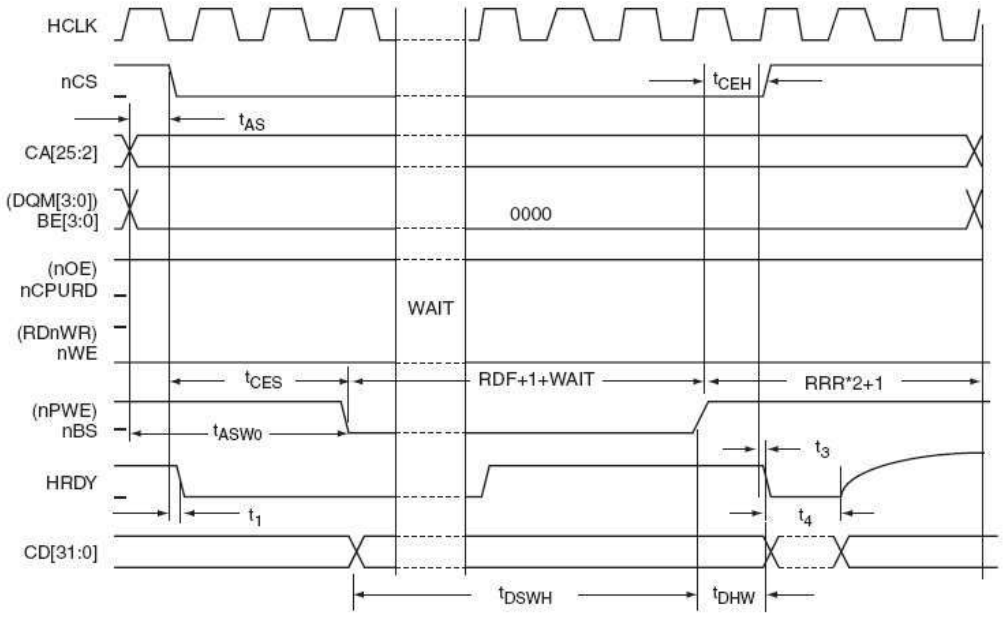


Table 18-6: Marvell PXA250/270 Timing Parameters

Symbol	Parameter	Min	Max	Units
XScale SDRAM Timing				
t1	HCLK cycle time	12		ns
t2	HCLK high time	4		ns
t3	HCLK low time	4		ns
t4	HCKE hold time	3.5		ns
t5	HCKE setup time	3.5		ns
t6	Command setup time	3.5		ns
t7	Command hold time	3.5		ns
t8	Address setup time	3.5		ns
t9	Address hold time	2.5		ns
t10	Access time from HCLK		t1 - 2	ns
t11	CD Out hold time from HCLK	4		ns
t12	CD In setup time from HCLK	3.5		ns
t13	CD In hold time from HCLK	3.5		ns
t14	Active to READ, WRITE delay (Row Active)	3* t1		ns
t15	READ Latency	3* t1 or 2* t1[1]		ns
t16	Write recovery time (Precharge)	2* t1		ns

Table 18-7: Marvell PXA250/270 Read Timing Specification

Parameter	Timing Descriptions	Control Side	Specified[1]
tAS	Address Setup to nCS	CPU	1 MCLK
tCES	nCS Setup to nOE or nPWE asserted (Low)	CPU	2 MCLKs
tASRW0	Address Setup to nOE or nPWE asserted (Low)	CPU	3 MCLKs
tCEH	nCS Held Asserted After nOE or nPWE Deasserted	CPU	1 MCLK
tAH	Address Hold After nOE or nPWE Deasserted	CPU	RDF+2 MCLKs min.
t1	From nCS Asserted to HRDY Driven	SM502	4 ns max.
t2	Data Setup to HRDY Rise	SM502	1 ns min.
t3	HRDY Deasserted Delay	SM502	4 ns max.
t4	HRDY Driven Low After nCS Deasserted	SM502	1 HCLK
t5	Data Hold After HRDY Deasserted	SM502	1 ns min.

Table 18-6: Marvell PXA250/270 Write Timing Specification

Parameter	Timing Descriptions	Control Side	Specified[1]
tAS	Address Setup to nCS	CPU	1 MCLK
tCES	nCS Setup to nOE or nPWE Asserted (Low)	CPU	2 MCLKs
tASRW0	Address Setup to nOE or nPWE Asserted (Low)	CPU	3 MCLKs
tDSWH	Write Data Setup to nPWE Deasserted (High)	CPU	RDF+2 MCLKs min.
tDHW	Data Hold After nPWE Deasserted (High)	CPU	1 MCLK
tCEH	nCS Held Asserted After nOE or nPWE Deasserted	CPU	1 MCLK
tAH	Address Hold After nOE or nPWE Deasserted	CPU	RDN+1 MCLK
t1	From nCS Asserted to HRDY Driven	SM502	4 ns max.
t3	HRDY Deasserted Delay	SM502	4 ns max.
t4	HRDY Driven Low After nCS Deasserted	SM502	1 HCLK

Hitachi SH4 Host

Figure 18-9 shows the timing waveforms for SH4 System DRAM operations. Figure 18-10 shows the timing waveforms for SH4 read operations. Figure 18-11 shows the timing waveforms for SH4 write operations. Table 18-7 lists the AC timing values for the parameters shown in the three SH4 figures.

Figure 18-9: SH4 System DRAM (Master) Timing

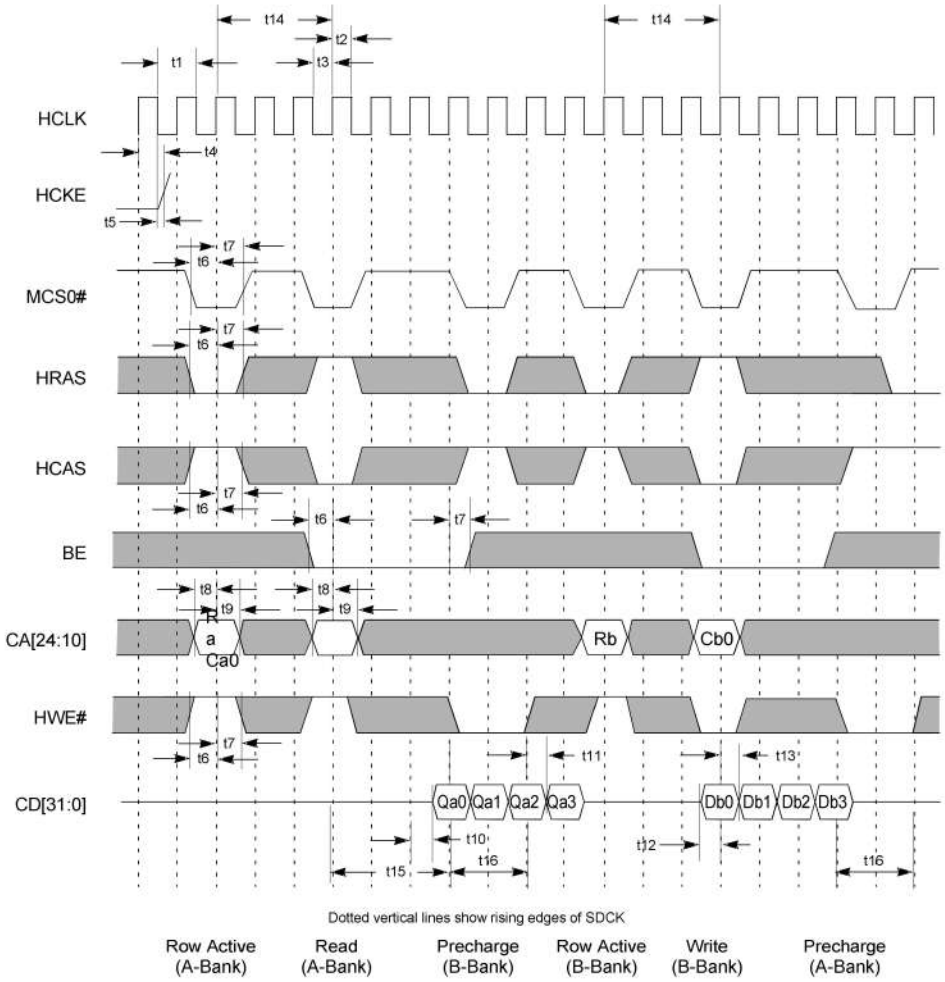


Figure 18-10: SH4 Read/Write Timing

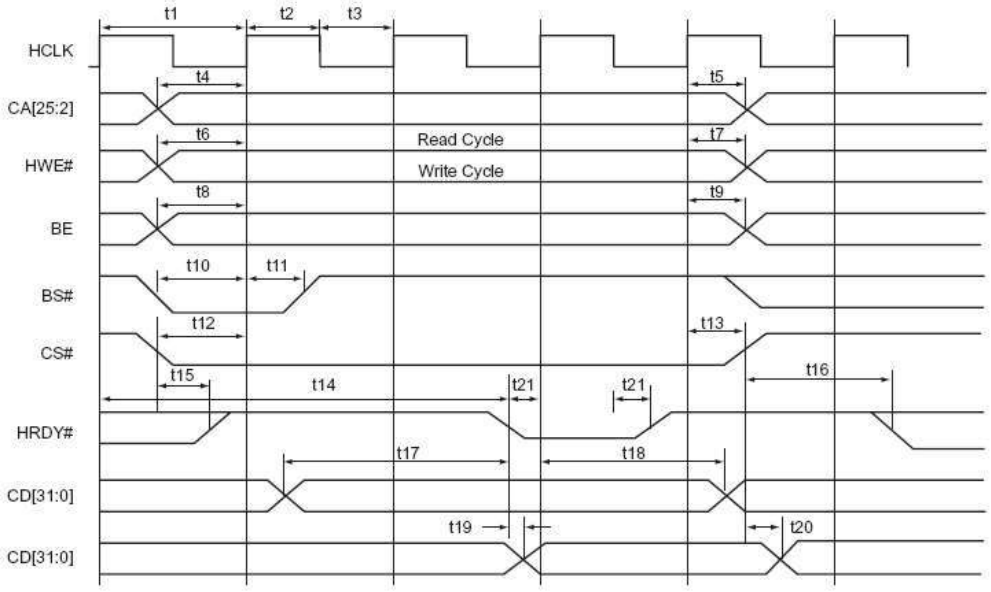


Table 18-19: SH4 Timing Parameters

Symbol	Parameter	Min	Max	Units
SH4 SDRAM Timing				
t1	HCLK Cycle Time	12		ns
t2	HCLK High Time	4		ns
t3	HCLK Low Time	4		ns
t4	HCKE hold time	3.5		ns
t5	HCKE setup time	3.5		ns
t6	Command setup time		6	ns
t7	Command hold time		2	ns
t8	Address/BA setup time	3.5		ns
t9	Address/BA hold time	2.5		ns
t10	Access time from SDCK		t1 - 2	ns
t11	Data Out hold time from HCLK	4		ns
t12	Data In setup time from HCLK	3.5		ns
t13	Data In hold time from HCLK	3.5		ns
t14	Active to READ, WRITE delay (Row Active)	3* t1		ns
t15	READ Latency	3* t1 or 2* t11		ns

t16	Write recovery time (Precharge)	2* t1		ns
SH4 Read Timing				
t17	Ready setup time		6	ns
t18	Ready hold time		2	ns
t19	Read hold time		2	ns
t20	Data valid delay time		4	ns
SH4 Write Timing				
t21	Ready setup time		6	ns
t22	Ready hold time		2	ns

Table 18-10: SH4 Read/Write Timing Parameters

Symbol	Parameter	Min	Max	Units
SH4 SDRAM Timing				
t1	HCLK cycle time	12		ns
t2	HCLK high time	4[1]		ns
t3	HCLK low time	4[1]		ns
t4, t6, t8, t12	Command setup time	4		ns
t5, t7, t9, t13	Command hold time	0		ns
t10	BS# setup time	4		ns
t11	BS# hold time	3		ns
t14	Earliest Ready	24[2,3]		ns
t15	Falling edge of CS# to Ready driven	2	12[3]	ns
t16	Rising edge of CS# to Ready 3-stated		12[3]	ns
t17	Data setup time (write cycle)	4		ns
t18	Data hold time (write cycle)	4		ns
t19	Data delay time from falling edge of Ready (read cycle)	0[4]	4[4]	ns
t20	Data hold time from rising edge of CS# or a new BS# (read cycle)	0	4	ns
t21	Falling edge of HCLK to Ready delay	1	4	ns

1. This timing is based on a 12ns HCLK cycle time.
2. This timing is based on a 12ns HCLK cycle time. If HCLK is faster than 12ns, t14 should be 2xHCLK, and t15 and t16 should be 1xHCLK.
3. Data is driven at the same time as Ready with a maximum delay of 4ns.

Figure 18-12: NEC System DRAM (Master) Timing

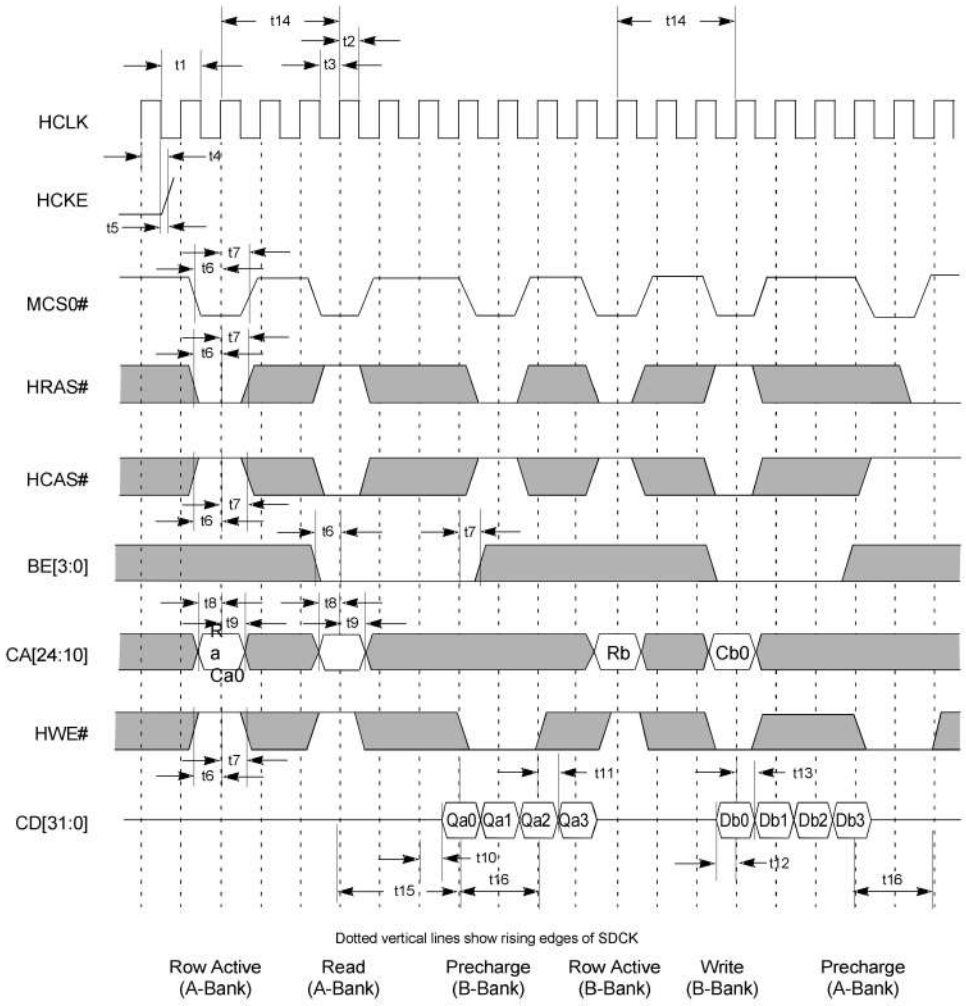


Figure 18-13: NEC DRAM (Slave) Timing

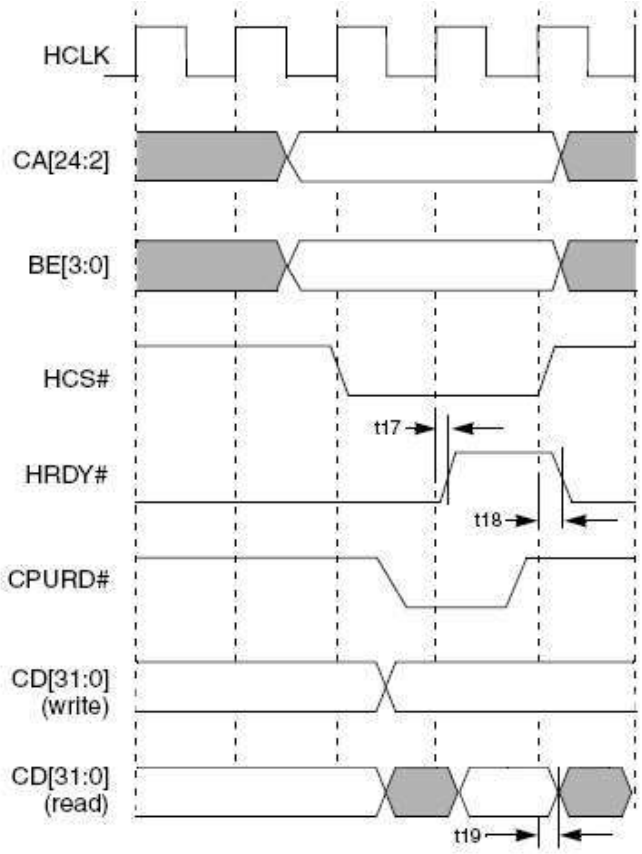


Table 18-8: NEC MIPS Timing Parameters Table 18-8: NEC MIPS Timing Parameters

Symbol	Parameter	Min	Max	Units
NEC SDRAM Master Timing				
t1	HCLK Cycle Time	12		ns
t2	HCLK High Time	4		ns
t3	HCLK Low Time	4		ns
t4	HCKE hold time	3.5		ns
t5	HCKE setup time	3.5		ns
t6	Command setup time		6	ns
t7	Command hold time		2	ns
t8	Address/BA setup time	3.5		ns
t9	Address/BA hold time	2.5		ns
t10	Access time from HCLK		t1 - 2	ns
t11	Data Out hold time from HCLK	4		ns
t12	Data In setup time from HCLK	3.5		ns
t13	Data In hold time from HCLK	3.5		ns
t14	Active to READ, WRITE delay (Row Active)	3* t1		ns
t15	READ Latency	3* t1 or 2*		ns

		t11		
t16	Write recovery time (Precharge)	2* t1		ns
NEC DRAM Slave Timing				
t17	Ready latency		4	ns
t18	Ready hold time		2	ns
t19	Data hold time		2	ns

13.3.2 Display Controller Timing

Color TFT Interface

Figure 62 shows the timing waveforms for the FP and FP_DISP signals. Figure 63 shows the timing waveforms for the FP_HSYNC and FP_VSYNC signals. Table 32 lists the AC timing values for the parameters shown in the two figures.

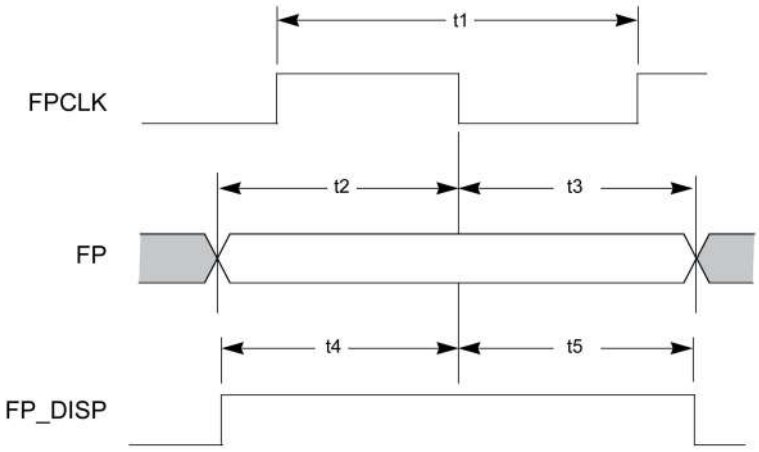
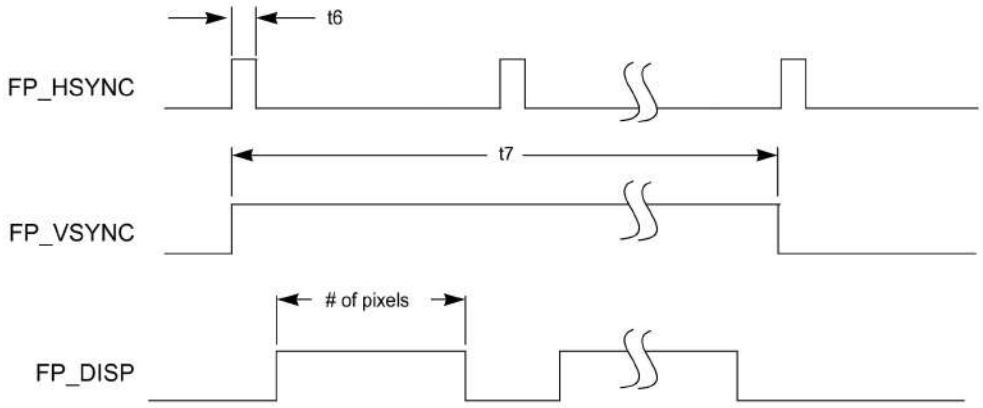


Figure 35: FP and FP_DISP Timing



Note: Number of pixels is programmed in the Panel Horizontal Total register, bits [11:0] (see "Panel Horizontal Total" on page 5-15).

Figure 36: FHSYNC and FVSYNC Timing

Symbol	Parameter	Min	Max	Unit
t1	TFT FPCLK cycle time	12		ns
t2	FP setup to FPCLK falling edge	0.5*T[1] – 2		ns
t3	FP hold from FPCLK falling edge	0.5*T – 2		ns
t4	FP_DISP setup to FPCLK falling edge	0.5*T – 2		ns
t5	FP_DISP hold from FPCLK falling edge	0.5*T – 2		ns
T6	FP_HSYNC pulse width	8	16	T
t7	FP_VSYNC pulse width	1		FP_HSYNC

Table 20: Color TFT Interface Timing Parameters

1. T is pixel clock rate on LCD.

13.3.3 ZV Port Timing

Figure 64 depicts the relationship amongst the ZV Port signals. Table 33 shows the AC parameters associated with the ZV Port signals when the ZV Port custom interface is in use at 50 MHz.

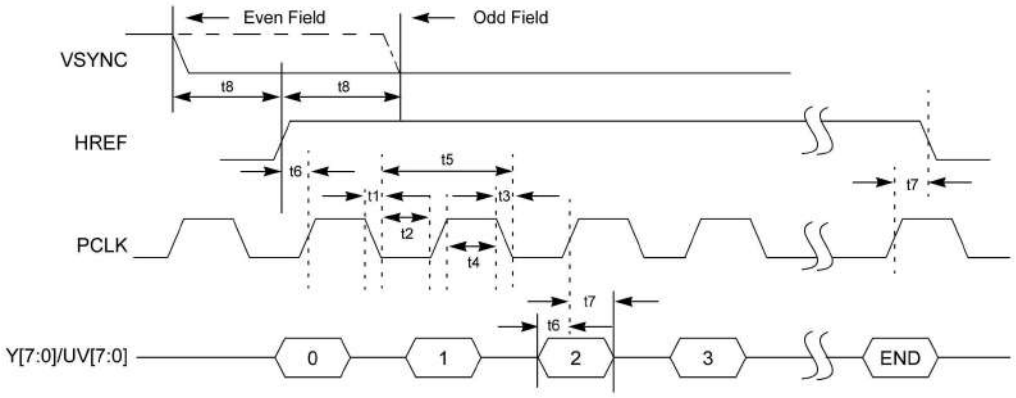


Figure 37: ZV Port Timing

Symbol	Parameter	Min	Max	Unit
t1	PCLK fall time	2		ns
t2	PCLK low time	7		ns
t3	PCLK rise time	2		ns
t4	PCLK high time	7		ns
t5	PCLK cycle time	20		ns
t6	Y[7:0] / UV[7:0] / HREF setup time	10		ns
t7	Y[7:0] / UV[7:0] / HREF hold time	3		T
t8	VSYNC setup / hold time to HREF	30		ns

Table 21: ZV Port Timing Parameters

Notes: All video signals have minimum rise and fall times of 4 ns and maximum rise and fall times of 8 ns. Non-interlaced data asserts VSYNC at the Odd Field timing.

13.3.4 Local DDR Timing

TBA