



FEATURES

- Complete 2400 bps modem conforming to V.22 bis
- Compatible with CCITT V.22 bis, V.22, V.21 and Bell 212A and 103 standards
- Integrated DTMF/Guard Tone Generators, call progress monitor
- All loopback diagnostics
- Programmable audio port

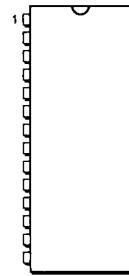
GENERAL DESCRIPTION

The SC11006 is a complete 2400 bps modem IC containing all modem functions except the adaptive equalizer. It is used in conjunction with an external controller such as the Sierra SC11019 (for parallel bus applications), the SC11020 (for RS-232 applications), the SC11022 (for either configuration or ROMless microcontroller such as the Sierra SC11011, 11021, 11061 or 11091 to implement a 2400 bps full duplex intelligent modem, compatible with the CCITT V.22bis recommen-

ation. The controller performs all modem control and handshaking functions as well as the adaptive equalization.

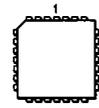
The SC11006 operates in 2400 bps QPSK/QAM and 1200 bps PSK as well as 0 to 300 baud FSK modes, compatible with Bell 103 and 212A as well as CCITT V.21, V.22 and V.22bis standards. When used with the SC11019 or SC11020 controllers, the SC11006 becomes an intelligent modem controlled by the industry

28-PIN DIP PACKAGE



SC11006CN

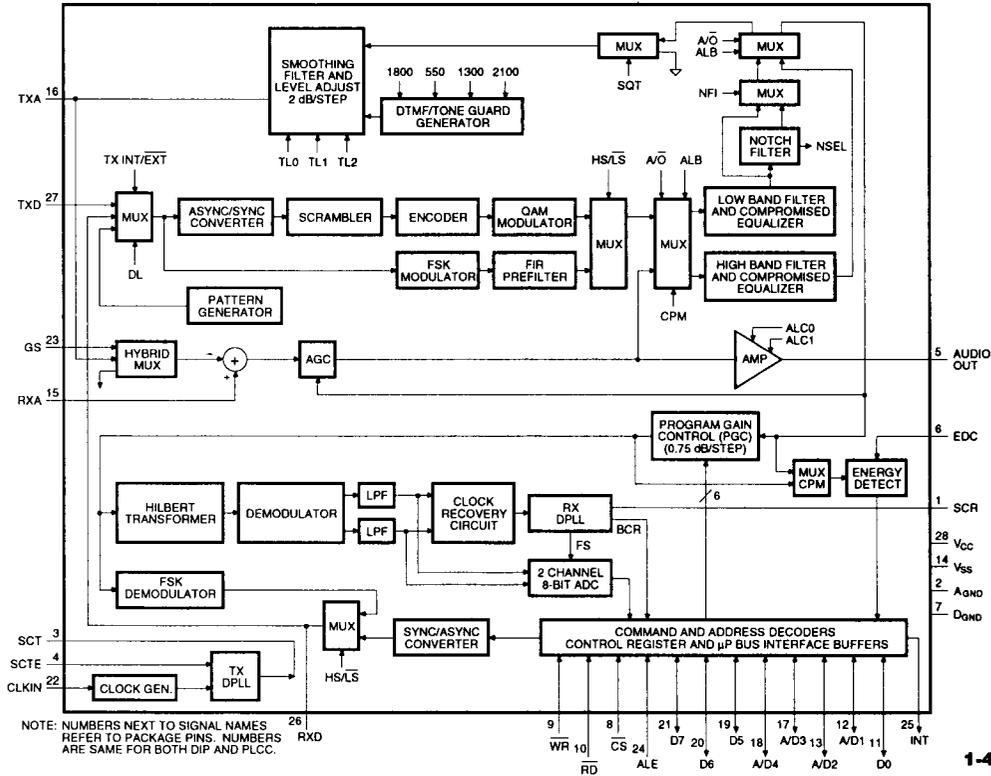
28-PIN PLCC PACKAGE



SC11006CV

standard "AT" command set. The interface between the SC11006 modem and controller is a standard microcontroller interface that easily connects to the SC22201 (128 by 8) EE memory for permanent storage of configuration settings and phone numbers.

BLOCK DIAGRAM



SC11006 2400 Bit Per Second Modem Analog Peripheral



FUNCTIONAL DESCRIPTION OF THE SC11006 MODEM

The SC11006 includes:

- Full transmitter consisting of
 - Async to Sync converter
 - Scrambler
 - Data encoder
 - 75% square root of raised cosine pulse shaper
 - Quadrature modulator
 - FSK (Bell 103 and CCITT V.21) modulator
 - Hybrid
- High band and low band filters
- High band and low band compromise equalizers
- V.22 notch filter (selectable at 550 or 1800 Hz)
- Transmit smoothing filter
- Programmable attenuator for transmit level adjust
- DTMF, 550 Hz, 1300 Hz, 1800 Hz, and 2100 Hz tone generator
- Transmit clock circuit for synchronous operation (slave, external, and internal modes)
- Pattern generator for generating fixed digital patterns in handshaking mode
- Receive section consisting of
 - 64-step programmable gain controller (PGC)
 - Energy detector at the output of the PGC
 - Hilbert transformer
 - Quadrature demodulator (free running carrier) with low pass filters
 - Baud timing recovery circuit (sampling clock of 600 Hz)
 - FSK demodulator
 - Sync to Async converter
- 8-bit analog to digital converter (ADC)
- Control and Status registers
- 8-bit microprocessor interface with interrupt and multiplexed address/data lines
- Audio output with level adjust

Transmitter

Since data terminals and computers may not have the timing accuracy required for 2400/1200 bps transmission (0.01%), timing correction on the incoming data

stream must be made. The async/sync converter accepts asynchronous serial data clocked at a rate between 2400/1200 Hz $\pm 2.3\%$, -2.5% . It outputs serial data at a fixed rate of 2400/1200 Hz $\pm 0.01\%$ derived from the master clock oscillator. To compensate for the input and output rate differences, a stop bit is either deleted or inserted when necessary. If the input data rate is slower than the output data rate, a stop bit is inserted. If the input data rate is faster than the output data rate, a stop bit is deleted. The output of the async/sync converter is applied to the scrambler.

The scrambler is a 17-bit shift register clocked at 2400/1200 Hz. Outputs from the 14th and 17th stages are exclusive OR'd and further exclusive OR'd with the input data. The resultant data is applied to the D input of the shift register. Outputs from the first four/two stages of the shift register form the quad/dibit that is applied to the QAM/QPSK modulator. The purpose of the scrambler is to randomize data so that the energy of the modulated carrier is spread over the band of interest—either the high band, centered at 2400 Hz, or the low band, centered at 1200 Hz. In the 2400 bps mode, the modem actually sends four bits at a time, called a quadbit. The actual rate of transmission for a quadbit is 600 baud. This is the optimum rate of transmission over the general switched telephone network for a full duplex FDM (frequency division multiplexing) modem because band limit filters in the central office cut off at about 3000 Hz.

In the 2400 bps data rate, the data to be transmitted is divided into groups of four consecutive bits (quadbits). The first two bits of the quadbit are encoded as a phase quadrant change relative to the quadrant occupied by the preceding signal element. The last two bits

define one of the four signaling elements associated with the new quadrant.

In the 1200 bps data rate, the data stream is divided into groups of two consecutive bits (dibits). The dibits are used to determine the phase quadrant change relative to the quadrant occupied by the preceding signal element. The resulting signaling elements from the inphase (I) and quadrature (Q) channels are passed through base-band filters with a square root of raised cosine shape. The filtered signals subsequently modulate sine and cosine carriers, and add to form the QAM/QPSK signal. The wave-shaped signal is then passed through either the low-band or high-band filter, depending upon originate or answer mode selection.

For low speed operation, the FSK modulator is used. It produces one of four precision frequencies, depending upon originate or answer mode selection and the 1 (mark) or 0 (space) level of the transmit data. Different frequencies are used for V.21 and 212A modes. The frequencies are produced from the master clock oscillator using programmable dividers. The dividers respond quickly to data changes, introducing negligible bit jitter while maintaining phase coherence. The output of the FSK modulator is applied to the appropriate filter when the low speed mode of the operation is selected.

The filter section consists of low-band (1200 Hz) and high-band (2400 Hz) filters, half-channel compromise amplitude and group delay equalizers for both bands, smoothing filters for both bands, and multiplexers for routing of the transmit and receive signals through the appropriate band filters. For CCITT V.22 bis applications, a notch filter is included that can be programmed for either 550 Hz or 1800 Hz. In the call progress

monitor mode, the low-band filter is scaled down by a factor of 2.5 to center it over a frequency range of 300 to 660 Hz. Thus, during call establishment in the originate mode, call progress tones can be monitored through the scaled low-band filter and the modem answer tone or voice can be monitored through the unscaled high-band filter.

The low-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 1200 Hz. In the originate mode, this filter is used in the transmit direction; in the answer mode, it is used in the receive direction. When analog loopback is used in the originate mode, this filter, together with the low-band delay equalizer, is in the test loop.

The low-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the low-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band.

The high-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 2400 Hz. In the answer mode, this filter is used in the transmit direction; in the originate mode, it is used in the receive direction. When analog loopback is used in the answer mode, this filter, together with the high-band delay equalizer, will be in the test loop.

The high-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the high-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band. The transmit smoothing filter is a second-order low-pass switched-capacitor filter that adds the modem transmit signal to the V.22 guard tones. It also provides a

2 dB per step programmable gain function to set the output level.

Receiver

The receiver section consists of an energy detector, programmable gain control (PGC), part of the QAM/QPSK demodulator, FSK demodulator, 8-bit ADC and sync/asynch converter.

The received signal is routed through the appropriate band-pass filter and applied to the energy detector and PGC circuit. The energy detector provides detection within 17 to 24 msec. It is set to turn on when the signal exceeds -43 dBm and turn off when the signal falls below -48 dBm measured at the chip. A 2 dB minimum hysteresis is provided between the turn on and turn off levels. In call progress mode, the energy detector is connected to the output of the PGC to allow detection level adjustment.

The output of the receive filter is applied to the programmable gain control. This circuit has a wide overall range of 47.25 dB and provides 64 steps of 0.75 dB/step. The PGC gain is controlled by the external processor. It also provides auto-zeroing to minimize the output DC offset voltage.

The QAM/QPSK demodulator uses a coherent demodulation technique. Output of the programmable gain control (PGC) is applied to a Hilbert transformer that produces an in-phase and 90° out of phase component. These components are then demodulated to baseband in a mixer stage where individual components are multiplied by a free-running carrier. The baseband components are low-pass filtered to produce I and Q (Inphase and Quadrature) channel outputs. The I and Q channel outputs are both filtered by 300 Hz band-pass filters. Then they are rectified, summed and passed through a band-pass filter giving a 600 Hz

signal. This signal is applied to a digital phase lock loop (DPLL) to produce a baud rate clock. Using the recovered clock signal, the I and Q channels are sampled and digitized into 8-bit samples by the ADC. Each channel (I and Q) is sampled twice during a baud period, once at the middle and once at the end of the baud period, allowing T/2 or T sampling operation. The external processor is interrupted once every baud period (1.667 msec). The processor should read the I and Q samples (within 100 μ s from the time interrupt is issued), and perform adaptive equalization, carrier phase tracking, data decoding, and data descrambling. One quad/dibit is transferred from the SC11006 during each baud period.

In the asynchronous mode, data received from the processor is applied to the sync/asynch converter to reconstruct the originally transmitted asynchronous data. For data which had stop bits deleted at the transmitter (overspeed data), these stop bits are re-inserted. Underspeed data is passed essentially unchanged. The sync/asynch converter has two modes of operation. In the basic signaling mode, the buffer can accept an overspeed which corresponds to one missing stop bit in eight characters. The length of the start and data elements will be the same, and the stop bit will be reduced by 12.5%. In the extended-signaling range, the buffer can accept one missing stop bit in four characters and the stop bits will be reduced by 25% to allow for overspeed in the transmitting terminal. Output of the sync/asynch converter, along with the output of the FSK demodulator, is applied to a multiplexer. The multiplexer selects the appropriate output, depending on the operating speed and output data received on the RXD pin.

For low-speed operation, the FSK demodulator is used. The output of

the PGC amplifier is passed through a zero crossing detector and applied to a counter that is reset on zero crossings. The counter is designed to cycle at a rate 4 times faster than the carrier signal. The counter output is low-pass filtered and hard limited to generate FSK data.

To improve the performance of the receiver at low signal levels, while maintaining a wide amplitude range, a 1-bit AGC circuit is placed prior to the band-pass filter. The decision thresholds of this AGC are controlled by the AGCVT bit. When AGCVT = 1, the thresholds will be 6 dB further apart than when AGCVT = 0, so that the probability of gain change will be reduced. The status of the AGC gain is available through the AGCO bit. AGC will have 8 dB more gain when AGCO = 1. Status of AGCO should be monitored at every baud timing and when it makes a transition (causing a gain-hit) the PGC's gain should be modified accordingly to prevent divergence of the adaptive equalizer.

Hybrid

The signal on the phone line is the sum of the transmit and receive signals. The hybrid subtracts the transmitted signal from the signal on the line to form the received signal. It is important to match the hybrid impedance as closely as possible to the telephone line to produce only the received signal. When the internal hybrid is used, by turning the "Hybrid" code on through the interface, this matching is provided by an external resistor connected between the TXA and RXA pins on the SC11006. The filter section provides sufficient attenuation of the out-of-band signals to eliminate leftover transmit signals from the received signal. The hybrid also acts as a first order low-pass antialiasing filter. The

hybrid can be deactivated by the controller.

The SC11006 internal hybrid is intended to simplify the phone line interface. The internal hybrid can compensate for the loss in the line coupling transformer used in the DAA. By tying the GS pin to V_{SS} , ground, or V_{CC} , compensation levels of 0, +2, +3 dB, respectively, are provided.

With a higher loss transformer, some degradation in performance at lower signal levels will occur. Specifically, the bit error rate, when operating at receive signal levels below -40 dBm in the presence of noise, will be higher. The energy detect on/off levels measured at the line will also be different from those specified at the chip. An external hybrid circuit, shown in Figure 2, can be used to overcome these losses and achieve maximum performance. In this case, the internal hybrid must be turned off by setting bit 6 of the TXCR register to 0.

The external hybrid circuit uses two operational amplifiers, one in the transmit path and the other in the receive path. The SC11006 internal transmit stage provides a gain of 6 dB over the transmit signal level desired at the line. Under ideal conditions, with no loss in the transformer and perfect line matching, the signal level at the line will then be the desired value. In practice, however, there is impedance mismatch and a loss in the coupling transformer. Therefore, it may be desired to provide a gain in the transmit and receive paths to overcome the loss. The receive gain (G_R) and transmit gain (G_T) are set by the ratios of resistors R2, R1 and R6, R5 respectively (Figure 2).

The circuit can be analyzed as follows:

$$V_R = -\frac{R_2}{R_1}(V_{TR}) + \left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_4}{R_3+R_4}\right)V_Y$$

$$V_Y = -\frac{R_6}{R_5}V_X$$

If R6/R5 is chosen to equal the loss in the transformer, it can be assumed that V_Y is twice as high as V_{TX} (transmit portion of the total line signal). Since $V_{TR} = V_{TX} + V_{RX}$ and $V_Y = 2V_{TX}$

$$V_R = -\frac{R_2}{R_1}(V_{TX} + V_{RX}) + \left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_4}{R_3+R_4}\right)2V_{TX}$$

$$= -\frac{R_2}{R_1}V_{RX} + \left[\left(1 + \frac{R_2}{R_1}\right)\left(\frac{2R_4}{R_3+R_4}\right) - \frac{R_2}{R_1}\right]V_{TX}$$

To eliminate any transmit signal from appearing at the received signal input, the second term in the above equation must be set to zero, giving:

$$\left(1 + \frac{R_2}{R_1}\right)\left(\frac{2R_4}{R_3+R_4}\right) - \frac{R_2}{R_1}$$

Solving for R3/R4:

$$\frac{R_3}{R_4} = 1 + \frac{2R_1}{R_2}$$

Additionally,

$$G_R = \frac{R_2}{R_1} \text{ and } G_T = \frac{R_6}{R_5}$$

These equations can be solved to select component values that meet the desired requirements. For example, if the transmit and receive loss in the coupling transformer is 2.5 dB, then:

$$\frac{R_2}{R_1} = \text{INV Log} \left(\frac{G_{\text{RdB}}}{20} \right) = \text{INV Log} \left(\frac{2.5}{20} \right) = 1.333$$

$$\text{Similarly, } \frac{R_6}{R_5} = 1.333 \text{ and } \frac{R_3}{R_4} = 2.5$$

Some typical values are:

$$R_1=20\text{K}\Omega, R_2=27\text{K}\Omega, R_3=13\text{K}\Omega, R_4=5.1\text{K}\Omega, R_5=20\text{K}\Omega, \text{ and } R_6=27\text{K}\Omega$$

It should be noted that the transmit amplifier is only needed to overcome the loss in line coupling. It can be eliminated since the transmit signal level specification is typically stated as a maximum. Amplifier B, resistors R5 and R6, and capacitor C1 can be eliminated, and point X can be connected to point Y in the circuit of Figure 2 to achieve a more cost effective external hybrid arrangement.

The SC11006 with the internal hybrid may also be used on a 4-wire system where the transmit and receive signals are kept separate. In this mode, the "Hybrid" code must be turned off. The transmit signal is connected to a 600 Ω line transformer through a 600 Ω resistor.

Tone Generator

The tone generator section consists of a DTMF generator, V.22 guard-tone, and 1300 and 2100 Hz tone generators. The DTMF generator produces all of the tones corresponding to digits 0 through 9 and A, B, C, D, *, and # keys. The V.22 guard-tone generator produces either 550 Hz or 1800 Hz. Selection of either the 550 Hz or 1800 Hz tone will cascade the corresponding

notch filter with the low-band filter. The tones are selected by applying appropriate codes through the tone control register. Before a tone can be generated, tone mode must be selected. Facility is also provided to generate single tones corresponding to 1300 and 2100 Hz and the individual rows or columns of the DTMF signal.

Audio Output Stage

A programmable attenuator that can drive a load impedance of 50K Ohms is provided to allow monitoring of the received line signal through an external speaker. The attenuator is connected to the output of the hybrid. Four levels of attenuation—no attenuation, 6 dB

attenuation, 12 dB attenuation, and squelch are provided through the ALC1 and ALC0 audio output level control codes. Output of the attenuator is available on the audio output pin where an external audio amplifier (LM386 type) can be connected to drive a low impedance speaker. The output can directly drive a high impedance transducer, but the volume level will be low.

Clock Input

CLKIN (Pin 22) of the SC11006 should be connected to a 9.8304 MHz clock source with an accuracy of $\pm 0.01\%$. Alternatively, a 12.288 MHz clock can be used if the CLKSEL bit in the MCRB control register is set.

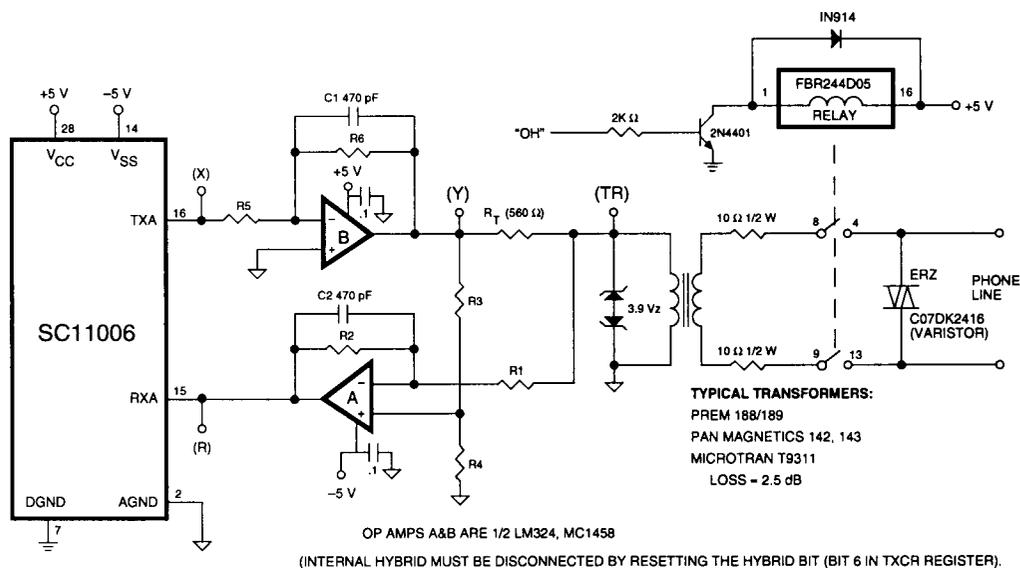


Figure 2. Using an External Hybrid with the SC11006

FUNCTIONAL DESCRIPTION OF THE SC11019, SC11020 SC11021, SC11022 AND SC11023 CONTROLLERS

The SC11019 modem controller, implemented in Sierra's 1.5 micron CMOS process, was designed specifically to handle all of the modem control functions, as well as the interface to a system bus. Besides including a 16-bit microprocessor, 16K by 8 bytes of ROM and 128 by 8 bytes of RAM, it also contains the functionality of an 16C450 UART, greatly simplifying the interface to a parallel system bus, such as the one used in IBM's PC. In fact, a complete, Hayes compatible modem for the PC consists of the SC11019 controller, the SC110024 modem and the DAA. All of the popular communications software written for the PC will work with the SC11006/SC11019 set.

Another version of the controller, the SC11020, is intended for RS-232 applications. It contains the same processor, memory, and UART as the SC11019 and has the same interface to the modem chip. The difference is that the UART is turned around so that the serial data from the RS-232 port is converted to parallel data handled by the internal processor. Pins are provided for connecting the familiar switches and indicator lamps found on most stand-alone modems, although the switches and lamps are not needed for operation—all of the switch settings can be done through software.

The controller receives an 8-bit signal sample from the SC11006 and performs adaptive equalization, carrier phase recovery, data decode, and descrambling. SC11019 and SC11020 have identical silicon but are bonded differently in the 44 pin package. Each controller can be configured as an SC11019 or SC11020 by the software. The controller is designed by using a 16-bit 2900 processor to perform the digital signal processing and the control functions. Its instruction set is a subset of the Intel 8096 instruction set, but operates faster than the 8096.

The SC11020 provides a standard 5V logic level interface—RS-232 drivers are required to interface to the port. Like the SC11019, the SC11020 comes programmed with the Hayes "AT" command set, and when used with the SC11006 modem, emulates a Hayes-type stand-alone modem. The SC11019 and SC11024 emulate a Hayes-type IBM PC plug-in card modem.

But the chip set is by no means limited to implementing a Hayes-type smart modem. Sierra is in the custom IC business and both chips were designed with this in mind. For example, only about 15K bytes of the SC11019's ROM is used for the handshaking and smart modem code, leaving 1K bytes for additional features that a customer may specify. And since the controller is ROM programmable, any command set, not just the Hayes "AT" set, can be implemented.

Both the SC11019 and SC11020 are available in two pinout options. They are 48 pin DIP, and 44 pin PLCC.

Please refer to the SC11019 series data sheet for complete details on controller features and performance characteristics.

The SC11021 is a ROMless version of the SC11019 & 20. It is available in a 68 pin PLCC and operates with up to 24K external ROM. It can be configured for either serial or parallel operation.

A fourth version, SC11022, is available in 48 pin DIP and 68 pin PLCC. This version can be configured as either a serial or a parallel modem and comes in the 68 pin package. It can also address up to 24K external ROM.

The SC11022 includes 16K ROM programmed with the same code as SC11019 and SC11020.

Both the controllers require +5 V power supply. Besides the interface for the SC11006 modem, the SC11019 controller has an eight-bit data port, three address lines, a chip select input, an interrupt line, and the DOST and DIST control lines found in the 16C450 UART. It also has control lines for ring indication, the off-hook relay, and a data/voice relay; these lines connect to the DAA.

In the SC11020, the eight-bit port becomes the switch input lines, and the address, chip select, INTO, DIST and DOST lines become the lines for the RS-232 interface, and modem status. These lines are also used to drive the LEDs. Internally, all of these lines are treated as programmable I/O ports under software control—so the main difference between the SC11019 and SC11020 is the ROM code. The SC11020 also contains the same modem and DAA interface lines as the SC11019.

The interface to the SC11006 is via an 8-bit address/data bus and the control lines for read and write. The same interface is used for access to an electrical erasable random access memory (SC22201). There are six clock multiplexed address/data bus cycles. A ready signal is provided for the interface to a high speed PC-AT type bus cycle. For the 68 pin packages, there are 15 extra address lines and chip selects for external ROM and external RAM interfaces. An EA pin is also available for selection of internal ROM or external ROM.

The SC11019 and SC11020 are truly ASIC controllers—they are designed to control a modem or other peripheral that operates at a moderately slow data rate up to 2400 bits per second. What's unique about the SC11019, for example, is that it allows a slow peripheral to interface to a high speed bus without making the main processor add unnecessary wait states.

This is done through the UART interface and the on-chip registers which look somewhat like dual port registers. The main processor can write to and read from them at will, while the on-chip controller can do the same. The controller was designed this way because most communications software has to have unrestrained access to the UART registers. To make the SC11019 compatible with this software, the registers were included.

The internal processor monitors the registers to determine the mode of operation—command mode or data mode; at power-up, it is automatically put in the command mode and it looks for instructions. Once carrier is detected, it goes into the data mode, and stays there until an escape sequence is entered, just like a Hayes-type modem. The escape sequence is three + signs—+++—in the default mode, but it can be changed in the software.

The actual processor contains a 16-bit data path and can execute 54 instructions with three different addressing modes: direct, indirect, and immediate. There is 16K by 8 of ROM on the chip for program storage.

To the system bus, the SC11019 looks and acts like a 16C450 UART. Communications software written for this UART will work with the SC11019 and SC11020. The Sierra chip set is truly a Hayes-type modem in two chips.

THE SC11006 & SC11019/SC11020 SYSTEM

The only external components required by the SC11006 are a 600 Ohm line matching resistor and a 1.0 μ F capacitor from the EDC pin to ground. That's all! If it is desired to drive a speaker to monitor the line, an amplifier like the LM386 can be added, but the output provided on the SC11024 can directly drive a high impedance (50 k Ω) ear-phone-type transducer.

The SC11006 modem's CLKIN pin line is driven by the SC11019 CKOUT line at 9.8304 MHz. The SC11019 interfaces directly to an IBM PC bus. The only external parts may be an 8 input NAND gate for COM1 and COM2 decoding inside the PC. A ready signal is provided to control the IOCHRDY pin on the bus to allow operation with higher speed computers (AT, XT TURBO, etc.)

For tone dialing, the controller sends a code to the modem chip which in turn puts out the called for DTMF tone on the line via the on-chip DTMF generator. For pulse

dialing, the controller pulses the OH (off-hook) relay. Both dialing modes work with the built-in call progress algorithm so they won't start dialing until a dial tone is detected.

All modems require a DAA. A DAA or data access arrangement is a piece of equipment required by the FCC to connect anything to the general switched telephone network. It consists of an isolation transformer, typically 600 Ω to 600 Ω ; a relay for disconnecting the modem from the line; a ring detector, typically an optoisolator; and high voltage surge protectors. The DAA has to be FCC registered and this can be done by one of many consultants and labs around the country. The fee is typically \$2,000 and it takes several weeks. Another alternative is to buy a DAA, supplied by several manufacturers.

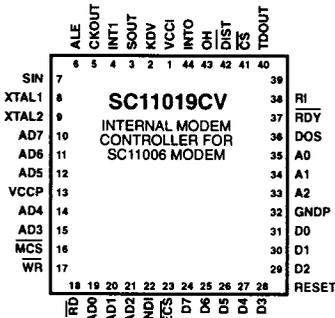
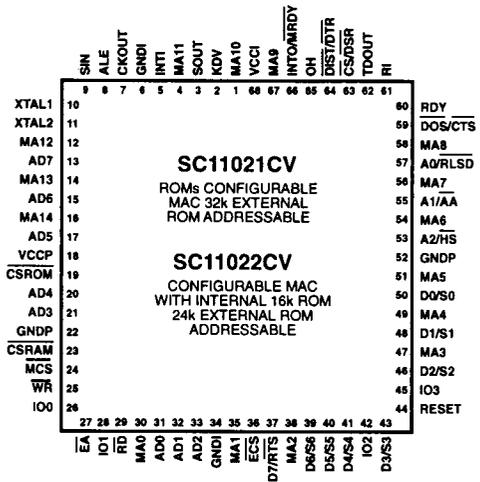
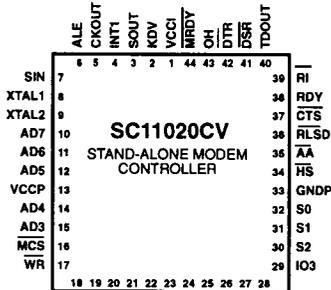
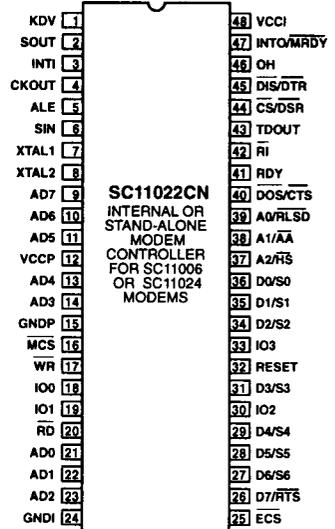
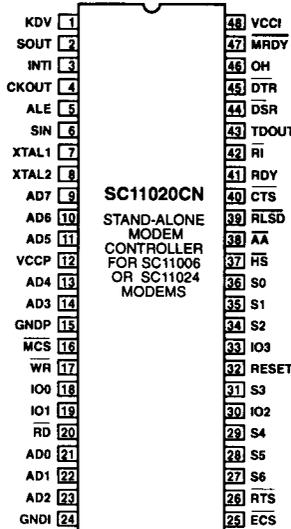
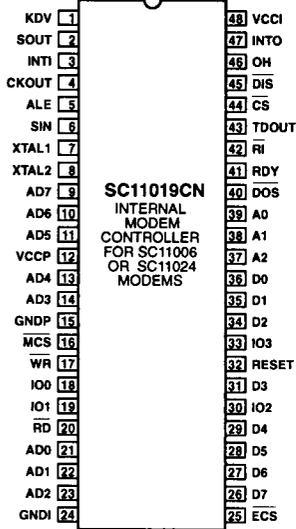
V.22bis is a CCITT specification that calls for 2400 bit per second, full or half duplex data transmis-

sion with a fallback mode of 1200 bps. It is not 2400 baud; the spec calls for transmission of quadsbits—4 bits per baud so the 2400 bps transmission takes place at 600 baud. The same is true for V.22—it is 1200 bps or 600 baud. V.22 does not call for a 300 baud fallback; there is a CCITT standard for 300 bps and that's V.21.

V.22 and V.22bis also call for guard tones to be sent along with the data. In most of Europe the tone is 1800 Hz except in Sweden where 550 Hz is used. The SC11006 modem has the 550 Hz and 1800 Hz tone generators built in as well as the 550 and 1800 Hz notch filter to remove the guard tone in the receiver.

All modems require a Hybrid; a term used to describe a circuit, passive or active, that takes the separate transmit and receive signals and combines them to go over the phone line. In the SC11006, this is done with op amps. The hybrid can be disabled so an external hybrid can be used, if desired.

CONNECTION DIAGRAM FOR CONTROLLERS



PIN DESCRIPTIONS

PIN NO.	PIN NAME	DESCRIPTION
1	SCR	Synchronous Clock Receive (Data set source); Output; TTL ; Used only in bit synchronous mode; Recovered by the Receiver Phase Locked Loop from the far end modem. Data on RXD is valid at the rising edge of this clock.
2	AGND	Analog Ground.
3	SCT	Synchronous Clock Transmit (Data set source); Output; TTL ; Used only in bit synchronous mode; Generated internally by the SC11006 Clock Generator; Rate = 1200 Hz \pm 0.01% or 2400 Hz \pm 0.01%.
4	SCTE	Synchronous Clock Transmit External (DTE source); Input; TTL ; Used only in bit synchronous mode; Data on TXD line is latched by the SC11006 at the rising edge of this clock. Clock rate = 1200 Hz \pm 0.01% or 2400 Hz \pm 0.01%.
5	AUDIO	Audio output; The hybrid output is passed through a programmable attenuator and fed to this analog pin. Four different levels can be attained by controlling bit 0 and bit 1 of the AUDIO register as specified under AUDIO register description.
6	EDC	Capacitor for energy detect; A 1.0 μ F capacitor should be connected between this pin and AGND.
7	DGND	Digital ground
8	\overline{CS}	Chip Select; Input; TTL ; Active low.
9	\overline{WR}	Write; Input; TTL ; Normally high; Data on AD7-AD0 is written into the SC11006 registers at the rising edge of this pulse.
10	\overline{RD}	Read; Input; TTL ; Normally high; Data on AD7-AD0 is to be read by the processor at the rising edge of this pulse.
12,13,17,18	AD1-AD4	Multiplexed address/data bus (8-bits); Input/Output; TTL ; A/D4-A/D1 (4-bits) are used for multiplexed addressing of internal registers.
14	V _{SS}	-5 V Supply
15	RXA	Receive analog; Input
16	TXA	Transmit analog; Output
11,19-21	D0, D5-D7	Bits 0, 5, 6 and 7 are don't cares as far as address is concerned.
22	CLKIN	Clock input; 9.8304 MHz or 12.288 MHz clock input from the controller.
23	GS	Gain Select to compensate for loss in line coupling transformer. When left open or tied to V _{SS} , the compensation is 0 dB; connected to ground, +2 dB compensation is provided; and when tied to V _{CC} , the compensation is +3 dB.
24	ALE	Address Latch Enable; Input; TTL ; The address on A/D4-A/D1 is latched into the SC11006 Address decoder at the falling edge of this normally low pulse.
25	INT	Interrupt; Output; TTL ; Normally low; A short (13 μ s typical) positive pulse is generated after all A to D conversions are completed.
26	RXD	Received Data; Output; TTL
27	TXD	Transmit Data; Input; TTL
28	V _{CC}	+5 V supply

REGISTERS

There are twelve 8-bit registers interfacing to the microprocessor bus. Five of these registers can only be read by the processor (called READ registers) and

the remaining seven can be written into by the processor (called CONTROL registers). Bit 1 of the "Tone" register can be read and written by the

processor, Table 1 shows the address and bit assignments for these registers.

A chip select pin is provided for multi-peripheral addressing by the processor.

Table 1. READ Registers

ADDRESS BITS				NAME	BIT NUMBER							
A4	A3	A2	A1		7	6	5	4	3	2	1	0
0	0	0	0	Q1	Q17	Q16	Q15	Q14	Q13	Q12	Q11	Q10
0	0	0	1	I1	I17	I16	I15	I14	I13	I12	I11	I10
0	0	1	0	Q2	Q27	Q26	Q25	Q24	Q23	Q22	Q21	Q20
0	0	1	1	I2	I27	I26	I25	I24	I23	I22	I21	I20
0	1	0	0	Status	X	X	X	AGCO	PA	PR	FSKD	ED
0	1	X	1	Unused								
0	1	1	X	Unused								

STATUS Register: Address (A4-A1) = 0100

BIT NUMBER	BIT NAME	DESCRIPTION
Bits 7-5	Unused	
Bit 4	AGCO	Status of internal 1-bit AGC. When this bit is set, RXA signal is amplified by 8 dB before entering the bandpass filters.
Bit 3	PA	This bit is set whenever the clock recovery DPLL advances one step (skips a count) to lock. It is cleared only when STATUS register is read.
Bit 2	PR	This bit is set whenever the clock recovery DPLL retards one step (adds an extra count) to lock. It is cleared only when STATUS register is read.
Bit 1	FSKD	Received FSK data. FSKD = 1 when mark is received.
Bit 0	ED	Energy detect circuit output. ED = 1 when energy detected.

Note 1: When DPLL neither advances nor retards, then PA = PR = 0.

Note 2: When reading unused bits, the corresponding bus lines will not be driven by the SC11024 and will be floating.

Table 1a. READ Registers

Q1 Register:	Stores midbaud inphase sample output of ADC.
I1 Register:	Stores midbaud quadrature sample output of ADC.
Q2 Register:	Stores endbaud inphase sample output of ADC.
I2 Register:	Stores endbaud quadrature sample output of ADC.

Note: All samples are represented in two's complement form.

Table 2. CONTROL Registers

ADDRESS BITS				NAME	BIT NUMBER							
A4	A3	A2	A1		7	6	5	4	3	2	1	0
1	0	0	0	TXCR	X	HYBRID	TXSEL2	TXSEL1	TXSEL0	SQT	BR1	BR0
1	0	0	1	MCRA	X	LCK/INT	RNGX	SYNC	WLS1	WLS0	A/O	RXMRK
1	0	1	0	MCRB	X	X	CLKSEL	CPM	ALB	TL2	TL1	TL0
1	0	1	1	TONE	X	HNDSHK	TONEON	DTMF	D3	D2	D1	D0
1	1	0	0	PGCR	X	AGCVT	G5	G4	G3	G2	G1	G0
1	1	0	1	DATA	X	PLLJAM	PLLFRZ	PLLFAST	RD3	RD2	RD1	RD0
1	1	1	0	AUDIO	X	DISS	PGCZ	TST2	TST1	TST0	ALC1	ALC0
1	1	1	1					UNUSED				

CONTROL REGISTERS

Transmit Control Register (TXCR): Address (A4-A1) = 1000

(Note: When writing into these registers, the bus lines corresponding to the unused bits are ignored by the SC11006.)

BIT NUMBER	BIT NAME	DESCRIPTION
------------	----------	-------------

Bit 7 Unused

Bit 6 HYBRID When set, the transmitter output (TXA) is connected to the inverting input of the receive buffer to allow the use of the on-chip hybrid circuit for 2 to 4 wire conversion.

Bit 5 TXSEL2 and Bit 4 TXSEL1 and Bit 3 TXSEL0 Transmit Select bits. These 3 bits determine the data transmitted by the transmitter according to the following table:

TXSEL2	TXSEL1	TXSEL0	TRANSMITTED DATA
0	0	0	External data sent by DTE.
0	0	1	Unscrambled S1 (Note 1).
0	1	0	Unscrambled Space.
0	1	1	Unscrambled Mark.
1	0	0	Scrambled RX. Digital loop back mode (Note 2).
1	0	1	Scrambled Reversals (Notes 3 and 4).
1	1	0	Scrambled Space (Note 4).
1	1	1	Scrambled Mark (Note 4).

Note 1: S1 is a pattern of 0011 transmitted at 1200 bps rate regardless of BR1. If in FSK mode (BR0 = 1), then reversals are sent. This pattern cannot be sent at 2400 bps rate.

Note 2: In this mode, the received data, after being descrambled, is sent back to the scrambler. The modem will automatically go to the Synchronous mode with Slave timing.

Note 3: Reversals are continuous streams of 01.

Note 4: When in FSK mode (BR0 = 1), TXSEL2 is ignored since scrambling is not applicable.

Bit 2 SQT When this bit is set, the transmitter is squelched by connecting the output of MUX1 (see the block diagram) to analog ground.

Bit 1 BR1 and Bit 0 BR0 Bit Rate Selection bits based on the following table:

BR1	BR0	BIT RATE
0	0	2400 bps V.22 bis
1	0	1200 bps V.22/212A
0	1	0-300 bps Bell 103
1	1	0-300 bps CCITT V.21



CONTROL REGISTERS (Cont.)

Mode Control Register A (MCRA): Address (A4-A1) = 1001

BIT NUMBER	BIT NAME	DESCRIPTION															
Bit 7	unused																
Bit 6	LCK/INTB	Determines the clock source for the transmitter. When this bit is set, the clock source is externally provided on SCTE (pin 4), and when cleared, it is internally generated (SCT). This bit can select the clock source independent of Sync/Async mode selection (see below). When in Digital Loop-Back mode, the clock source will be forced to the Slave mode (SCR).															
Bit 5	RNGX	Range extender for the receiver Sync/Async converter. When set, the receiver Sync/Async can insert up to one stop bit per four (8, 9, 10 or 11-bit) characters to compensate for a far end DTE being up to 2.3% over speed. The transmitter Async/Sync always handles this overspeed condition regardless of this bit's condition.															
Bit 4	SYNC	When set, operate in bit synchronous mode; when clear, operate in character asynchronous mode. When in Digital Loop-Back mode, the SC11006 will be forced to the Synchronous mode.															
Bit 3	WLS1	Word length select bits in asynchronous mode, according to the following table:															
Bit 2	WLS0																
<table border="1"> <thead> <tr> <th>WLS1</th> <th>WLS0</th> <th>NUMBER OF BITS PER CHARACTER</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>8</td> </tr> <tr> <td>1</td> <td>1</td> <td>9</td> </tr> <tr> <td>0</td> <td>0</td> <td>10</td> </tr> <tr> <td>0</td> <td>1</td> <td>11</td> </tr> </tbody> </table>			WLS1	WLS0	NUMBER OF BITS PER CHARACTER	1	0	8	1	1	9	0	0	10	0	1	11
WLS1	WLS0	NUMBER OF BITS PER CHARACTER															
1	0	8															
1	1	9															
0	0	10															
0	1	11															
Bit 1	A/ \bar{O}	When set, operate in answer mode; when clear, operate in originate mode.															
Bit 0	RXMARK	When set, the RXD pin is clamped to the high logical level.															

Mode Control Register B (MCRB): Address (A4-A1) = 1010

BIT NUMBER	BIT NAME	DESCRIPTION																																				
Bit 7	unused																																					
Bit 6	unused																																					
Bit 5	CLKSEL	This bit must be set when CLKIN = 12.288 MHz, and clear when CLKIN = 9.8304 MHz.																																				
Bit 4	CPM	Call progress monitor mode. When set, the receive path can be connected to the high band filter to detect answer tone (ALB=0) or to the low band filter scaled down 2.5 times (ALB=1) to listen for the call progress tones during auto dialing.																																				
Bit 3	ALB	Analog Loop Back. When set, the transmitter output (TXA) is connected to the receive path, bypassing the receive filter.																																				
Bit 2	TL2	Transmit level adjust bits based on the following table:																																				
Bit 1	TL1																																					
Bit 0	TL0																																					
<table border="1"> <thead> <tr> <th>TL2</th> <th>TL1</th> <th>TL0</th> <th>TRANSMIT LEVEL AT TXA PIN</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0 dBm</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>-2 dBm</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>-4 dBm</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>-6 dBm</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>-8 dBm</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>-10 dBm</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>-12 dBm</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>-14 dBm</td> </tr> </tbody> </table>			TL2	TL1	TL0	TRANSMIT LEVEL AT TXA PIN	0	0	0	0 dBm	0	0	1	-2 dBm	0	1	0	-4 dBm	0	1	1	-6 dBm	1	0	0	-8 dBm	1	0	1	-10 dBm	1	1	0	-12 dBm	1	1	1	-14 dBm
TL2	TL1	TL0	TRANSMIT LEVEL AT TXA PIN																																			
0	0	0	0 dBm																																			
0	0	1	-2 dBm																																			
0	1	0	-4 dBm																																			
0	1	1	-6 dBm																																			
1	0	0	-8 dBm																																			
1	0	1	-10 dBm																																			
1	1	0	-12 dBm																																			
1	1	1	-14 dBm																																			

CONTROL REGISTERS (Cont.)

TONE Register: Address (A4-A1) = 1011

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	HNDSHK	This bit is set only during handshaking sequence. When set, both FSK and PSK/QAM demodulators are enabled. When cleared, FSK demodulator is disabled when in high speed mode.
Bit 5	TONEON	When set, the output of the tone generator appears at TXA. When cleared, the output of the tone generator is squelched.
Bit 4	DTMF*	When set, the DTMF generator is turned on. When cleared, the DTMF generator is turned off, but other tones can be generated.
Bits 3-0	D3-D0	Specify the desired tone (see the following table):

DTMF	D3	D2	D1	D0	DIGIT DIALED	TONE OUTPUT	FREQUENCIES (HZ)
1	0	0	0	0	0	941	1336
1	0	0	0	1	1	697	1209
1	0	0	1	0	2	697	1336
1	0	0	1	1	3	697	1477
1	0	1	0	0	4	770	1209
1	0	1	0	1	5	770	1336
1	0	1	1	0	6	770	1477
1	0	1	1	1	7	852	1209
1	1	0	0	0	8	852	1336
1	1	0	0	1	9	852	1477
1	1	0	1	0	*	941	1209
1	1	0	1	1	(A)	697	1633
1	1	1	0	0	(B)	770	1633
1	1	1	0	1	(C)	852	1633
1	1	1	1	0	#	941	1477
1	1	1	1	1	(D)	941	1633
0	0	0	0	0		No tone; tone generator turned off	
0	0	0	0	1		550	
0	0	0	1	0		1800	
0	0	0	1	1		2100	
0	0	1	0	0		1300	
0	0	1	0	1		No tone; tone generator turned off	
0	0	1	1	x		No tone; tone generator turned off	
0	1	x	x	x		No tone; tone generator turned off	

Note: TONEON must also be set to generate DTMF signals.

Programmable Gain Controller Register (PGCR): Address (A4-A1) = 1100

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	AGCVT	When set, prevents gain hit due to AGC's gain step. This bit must be set during the handshaking after detecting the four point constellation and before switching to 16-way decision making.
Bits 5-0	G5-G0	Control the gain of the PGC within a range from -10 to +37.5 dB in 0.75 dB steps. (See the following table):



CONTROL REGISTERS (Cont.)

G5	G4	G3	G2	G1	G0	PGC GAIN (dB)
0	0	0	0	0	0	-10.0
0	0	0	0	0	1	-9.25
0	0	0	0	1	0	-8.5
0	0	0	1	0	0	-7.0
0	0	1	0	0	0	-4.0
0	1	0	0	0	0	+2.0
1	0	0	0	0	0	+14.0
1	1	1	1	1	1	+37.25

Note: Signal level is adjusted (before entering the filter) by an internal AGC with +12 dB or 0 dB gain, plus a fixed gain of 5 dB.

DATA Register: Address (A4-A1) = 1101

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	PLLJAM	When this bit is set, the DPLL will be reset by the next rising edge of the received baud clock. This bit must remain high for at least one baud period. It should be cleared by the processor to end the jamming mode. PLLFRZ (see below) overrides PLLJAM when both are enabled.
Bit 5	PLLFRZ	Phase locked loop freeze. When this bit is set, the DPLL begins to run freely regardless of the received baud clock. To re-enable the DPLL locking, the bit must be cleared by the processor. PLLFRZ overrides PLLJAM when both are enabled.
Bit 4	PLLFST	When set, the DPLL operates in "fast" locking mode. In this mode, the DPLL is updated on every baud period by 13 μ s steps. When this bit is cleared (default mode), the DPLL operates in "normal" locking mode and is updated once every 8 baud periods by 6.5 μ s steps.
Bit 3-0	RD3-RD0	Four-bit Received Data. Used only in high speed (1200 or 2400 bps) mode, they are descrambled by the processor and shifted out by the SC11006. Sync to Async is also done by the SC11006, when in the asynchronous mode. RD0 is the first bit appearing on the RXD pin, followed by RD1, RD2 and RD3. In the 1200 bps mode, only RD0 and RD1 are shifted out during one baud period.

AUDIO Register: Address (A4-A1) = 1110

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	DISS	When this bit is set, the scrambler is disabled, when cleared, it is enabled. Transmit select bits (TXSEL0-2) override this bit when in "transmit internal mode".
Bit 5	PGCZ	When set, the output of the PGC is grounded. DC offset of the demodulator can be stored and canceled by the controller.
Bit 4-2	TEST	Test bits used for factory testing. For normal chip operation, these bits must be cleared.
Bit 1	ALC1	Audio level control bit 1.
Bit 0	ALC0	Audio level control bit 0. These two bits are used to control the audio level at AUDIO pin according to the following table:

ALC1	ALC0	AUDIO ATTENUATION (dB)
0	0	Audio off
0	1	12
1	0	6
1	1	0 (no attenuation)

Note: The audio signal may be amplified by 12 dB by the line receiver AGC before being fed to the audio attenuator.

SYNCHRONOUS OPERATION

Transmitter Timing

Case 1—SC11006 Provides the Timing to the Data Terminal Equipment (DTE). See Figure 3.

If the DTE can lock to an external clock, then all that needs to be done is to put the SC11006 in the synchronous mode. This provides a 2400/1200 Hz clock on the SCT pin that can be used as a clock source for the DTE. The Transmit Phase-Locked-Loop (TX PLL) of the SC11006 will be in free-running mode.

Case 2—SC11006 Should Lock Its Transmit Timing to the Clock Source Provided by the DTE.

In this case, after selecting synchronous mode, also select "Locked" mode.

The TX PLL of SC11006 will then synchronize itself to the clock provided on its "SCTE" pin.

Case 3—Slave mode. The Transmit Timing is slaved to the receiver

recovered clock. Select synchronous mode and connect SCTE to SCR.

In either case, the SC11006 will sample the data on the rising edge of the clock.

Receiver Timing

In synchronous mode, the recovered clock will be provided on the SCR pin and the transitions of RXD will be on the falling edges of this clock. Data is valid on the rising edge of the clock.

SYNCHRONOUS MODE CHART

Transmitter Timing

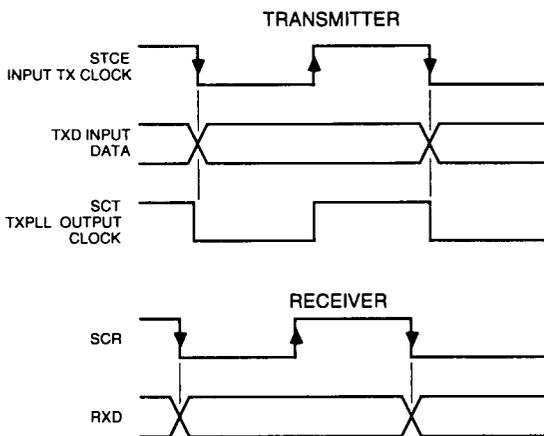


Figure 3. SC11006 Synchronous Mode Timing Diagrams.

SC11006 SPECIFICATIONS**Absolute Maximum Ratings (Notes 1–3)**

Supply Voltage, V_{CC}	6 V
Supply Voltage, V_{SS}	-6 V
DC Input Voltage (Analog Signals)	$V_{SS}-0.6$ to $V_{CC}+0.6$ V
DC Input Voltage (Digital Signals)	$V_{SS}-0.6$ to $V_{CC}+0.6$ V
Storage Temperature Range	-65 to 150°C
Power Dissipation (Note 3)	500 mW
Lead Temperature (Soldering 10 Sec.)	300°C

- Notes: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
 2. Unless otherwise specified, all voltages are referenced to ground.
 3. Power dissipation temperature derating—Plastic package: -12 mW/C from 65°C to 85°C.

Operating Conditions

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0		70	°C
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
V_{SS}	Negative Supply Voltage		-4.5	-5.0	-5.5	V
GND	Ground			0		V
F_C	Clock Frequency	CLKSEL = 0	9.8295	9.8304	9.8313	MHz
		CLKSEL = 1	12.2868	12.288	12.2892	MHz
T_R, T_F	Input Rise or Fall Time	All digital inputs except CLKIN			500	ns
T_R, T_F	Input Rise or Fall Time	CLKIN			20	ns

DC Electrical Characteristics ($T_A = 0$ TO 70°C , $V_{CC} = +5\text{ V} \pm 10\%$, $V_{SS} = -5\text{ V} \pm 10\%$)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Quiescent Current	Normal		18	35	mA
I_{SS}	Quiescent Current			18	35	mA
V_{IH}	High Level Input Voltage; Digital pins		2.4			V
V_{IL}	Low Level Input Voltage; Digital pins				0.8	V
V_{OH}	High Level Output ($I_{OH} = 0.5\text{ mA}$)		2.4			V
V_{OL}	Low Level Output ($I_{OL} = 1.6\text{ mA}$)				0.6	V
VXTA	Maximum Peak Output Level on TXA pin	$V_{CC} = +5\text{ V}$ $V_{SS} = -5\text{ V}$	± 3			V

- Notes: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
 2. Unless otherwise specified, all voltages are referenced to ground.
 3. Power dissipation temperature derating—Plastic package: -12 mW/C from 65°C to 85°C.

SC11006 SPECIFICATIONS (Cont.)

PROCESSOR BUS TIMING

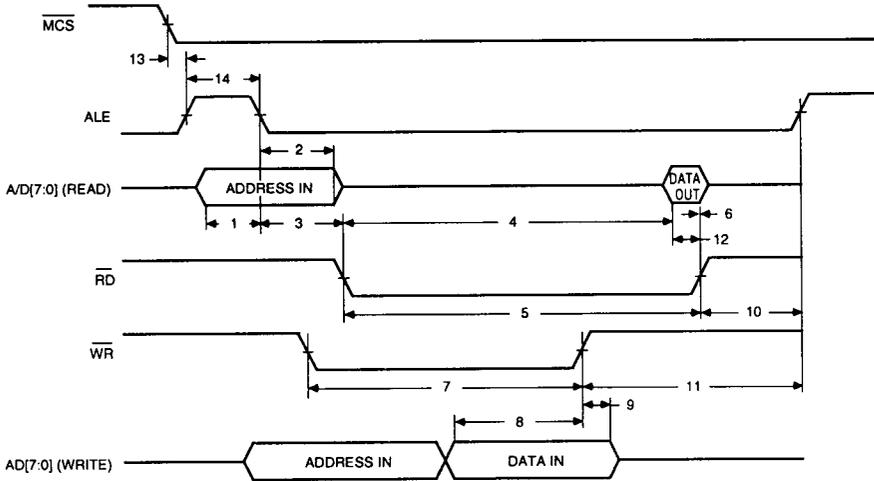


Figure 4.

When the controller is reading or writing to the SC11006, the address must be valid at least 30 ns before ALE goes low and stay valid 40 ns or more.

When the controller is writing, data must be valid at least 40 ns before WR goes false and stay valid until at least 0 ns after WR goes false.

When reading from the MAP, data is valid a maximum of 185 ns after RD goes true and stays valid at least until 0 ns after RD goes false.

AC Electrical Characteristics

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	TAVEL	Address Valid to ALE low		30			ns
2	THAD	Hold address after ALE low		40			ns
3	TALRD	Delay from ALE low to RD low		45			ns
4	TDVRL	Data valid after RD low				180	ns
5	TRD	Read pulse width		200			ns
6	TDHRD	Data hold after RD high		0			ns
7	TWR	Write pulse width		150			ns
8	TDVWR	Data setup before WR high		70			ns
9	TDHWR	Data hold after WR high		15			ns
10	TRHLH	End of read to next ALE		55			ns
11	TWHLH	End of write to next ALE		120			ns
12	TDVRH	Data valid set-up to RD high		15			ns
13	TMCAL	MCS low to ALE high		10			ns
14	TALE	ALE Pulse width		40			ns

SC11006 SPECIFICATIONS (Cont.)

Modem Transmit Signals—Hz (Assume 9.8304 Crystal)

PARAMETER	CONDITIONS	NOM.	ACT.	UNITS
FSK Mod/Demod Frequencies				
Bell 103				
Answer Mark		2225	2226	Hz
Answer Space		2025	2024.4	Hz
Originate Mark		1270	1269.4	Hz
Originate Space		1070	1070.4	Hz

CCITT V.21				
Answer Mark		1650	1649.4	Hz
Answer Space		1850	1850.6	Hz
Originate Mark		980	978.34	Hz
Originate Space		1180	1181.53	Hz

Call progress monitor mode:		MIN	TYP	MAX	
Center frequency	ALB = 1		480		Hz
Detect level (ED high) measured at RXA		-43			dBm
Reject level (ED low) measured at RXA				-48	dBm
Hysteresis measured at RXA		2			dB
Delay time (ED low to high)	EDC = 1.0 μ F	10	15	24	ms
Hold time (ED high to low)	EDC = 1.0 μ F	10	15	24	ms

DTMF Generator (Note 1)

PARAMETER	NOMINAL FREQUENCY	ALLOWABLE ERROR*	ACTUAL ERROR
Row 1	697 Hz	$\pm 1\%$	-0.23%
Row 2	770 Hz	$\pm 1\%$	-0.01%
Row 3	852 Hz	$\pm 1\%$	-0.12%
Row 4	941 Hz	$\pm 1\%$	-0.39%
Column 1	1209 Hz	$\pm 1\%$	-0.35%
Column 2	1336 Hz	$\pm 1\%$	-0.93%
Column 3	1477 Hz	$\pm 1\%$	-0.48%
Column 4	1633 Hz	$\pm 1\%$	-0.91%
Guard Tones	550 Hz	± 20 Hz	-2 Hz
	1800 Hz	± 20 Hz	-2 Hz
Calling Tone	1300 Hz		-6 Hz
Answer Tone	2100 Hz		-12 Hz

* CCITT Specifications

SC11006 SPECIFICATIONS (Cont.)

SC11006

DTMF Generator (Cont.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Second Harmonic Distortion	VCC = +5 V VSS = -5 V		-40		dB
Row Output Level			0		dBm
Column Output Level			2		dBm
550 Hz Guard Tone	TL2 = TL1 = TL0 = 0		-3		dB (Note 2)
1800 Hz Guard Tone	Measured at TXA Pin		-6		dB (Note 2)
1300 Hz Calling Tone			0		dB
2100 Hz Answer Tone			0		dB
Transmit level measured at TXA	Load = 1200 Ohms TL2 = TL1 = TL0 = 0 Squelched		0	-50	dBm dBm

Notes: 1: This assumes a clock of exactly 9.8304 MHz.

2: These levels are referenced to the TX signal level. When guard tones are added, the TXA level is adjusted to maintain a constant level on the line. For 1800 Hz, the adjustment is -0.97 dB; for 550 Hz, the adjustment is -1.76 dB, per the CCITT specification.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Mode	EDC = 1.0 μ F; measured at RXA PGC = 0				
Energy detect level (ED low to high)				-43	dBm
Loss of energy detect level (ED low to high)		-48			dBm
Hysteresis		2	3		dB

Programmable Gain Controller (PGC)

Gain step size			0.75		dB
Dynamic range			47.25		dB
Response time (from change in PGC register to output of A to D converter)			1.0		ms

Filter Characteristics

Crosstalk rejection			70		dB
Power supply rejection			0		dB
DPLL Response times JAM or FRZ			20		μ s
Fast			200		μ s

1

APPLICATIONS INFORMATION

Applications

The SC11006 with an external control microprocessor, a telephone line interface and a suitable computer interface, can implement a complete 2400 bps modem for many applications with a minimum of components and cost. Figure 7 shows the common portion of such a modem using the SC11006 with a telephone line interface. Sierra's SC22101, 128 byte E² memory is used to store default parameters and often used phone numbers. The SC11019/20/21/22 controllers also support a serial E² memory as an alternative. Figures 6 and 7 show the stand-alone and PC bus integral modems implemented with Sierra's SC11019/20 controllers. Figure 8 shows the connections for an internal ROM special purpose controller using the SC11021. Figure 9 shows an RS-232C serial interface for implementing a stand-alone modem. Figure 10 shows a parallel bus interface for implementing an internal modem for an IBM PC/XT/AT compatible computer when used with Sierra's SC11019 controller shown in Figure 6, while Figure 13 shows the interface required for implementing the same internal modem when used with the controller shown in Figure 12. Figure 11 shows a power supply

schematic for a stand-alone modem application.

Various modem configurations can be realized by combining schematics shown in Figures 5 thru 13.

A Hayes compatible stand-alone smart modem (Fig. 5) can be implemented by combining Figures 7, 8, 9 and 11.

The internal version for an IBM PC/XT/AT compatible (Fig. 6) can be implemented using Figures 7, 8 and 10.

An Alternative to the controller of Figure 8 is shown in Figures 12 and 13.

For performance evaluation, the circuit shown in Figure 14 can be used to obtain the receiver constellation. Quality of the signal processing performed by the modem can thus be visualized by observing the constellation for various line conditions and signal to noise ratios.

Power Supply Decoupling and Circuit Layout Consideration

For optimum performance at low received signal levels with low s/n ratios, it is important to use the

recommended power supply decoupling circuit as shown in Figure 7.

Small inductors in series with the supplies help suppress RFI as well as improve the power supply noise rejection capability of the SC11006. A 10Ω, 1/4 W resistor in place of, or in series with, the inductor in the SC11006 power leads has been found to be helpful in computer based products where the power supplies are particularly noisy.

The 10 μF capacitors should be a tantalum type while the 0.1 μF capacitors should have good high frequency rejection characteristics—monolithic ceramic types are recommended. It is important to locate the decoupling capacitors as close to the actual power supply pins of the SC11006 as possible. It is also recommended that the analog ground and digital ground buses be routed separately and connected at the common ground point of the power supply. Avoid routing digital traces through the analog area.

Ferrite beads on the ±5 V input to the circuit board should also be considered, both from a modem performance standpoint, as well as an aid in reducing RF radiation from the phone lines.

Note: Crystal oscillator: The controller requires a parallel resonant 19.6608 MHz crystal designed with CL = 18 pF and tolerance of ± .01% (such as Saronix NYP196-18). With this crystal, use 27 pF to ground from XTAL1 (Pin 10) and XTAL2 (Pin 11). Clock frequency measured at CKOUT (Pin 7) must be within ±0.005% of 9.8304 MHz.

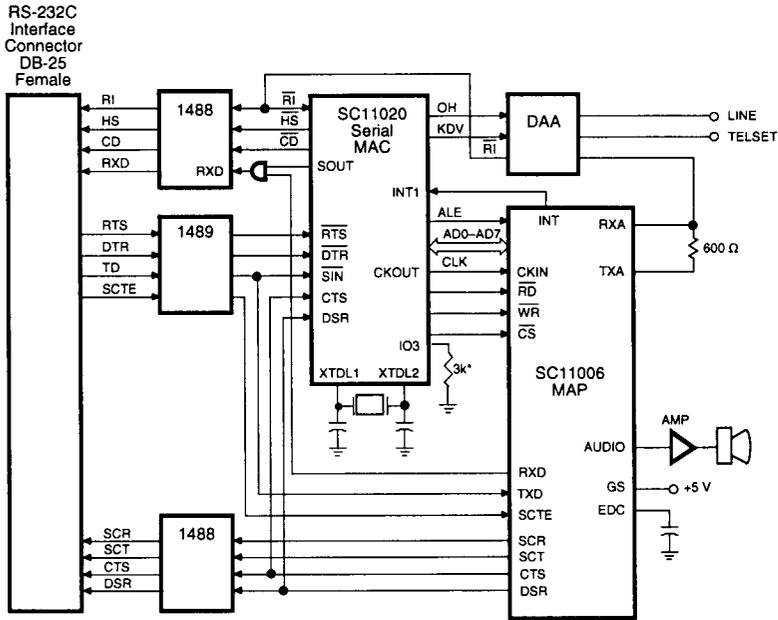


Figure 5. V22 bis Standalone Intelligent Modem with Internal ROM.

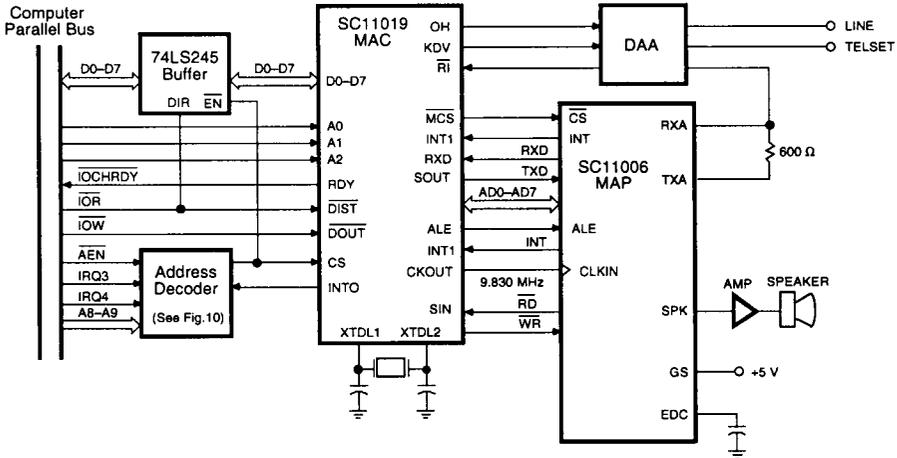
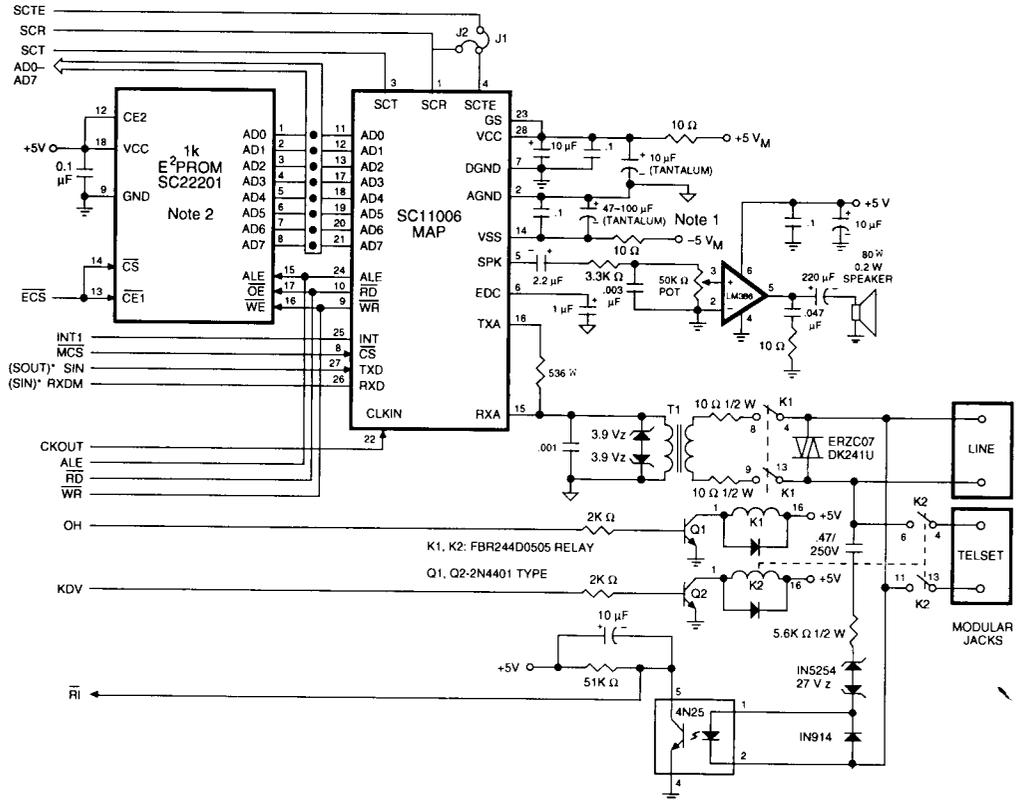


Figure 6. Internal Smart Modem for PC Bus Applications with internal ROM.



APPLICATIONS INFORMATION (Cont.)



Note 1: Connect analog ground directly to common of the power supply filter capacitor.

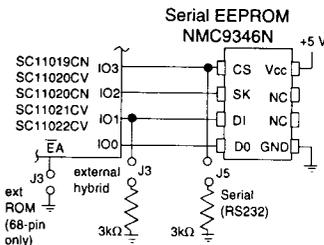
Note 2: A serial E²PROM may be substituted when using the SC11019, SC11020, SC11021 or SC11022 Modem Advanced Controller (48 and 68 pin versions), or SC11020 44 pin version.

Note 3: For external clocking of the transmitter, install J1 and set bit 6 of the MCRA; omit J2. For slave clocking of the transmitter, install J2 and set bit 6 of the MCRA; omit J1. For normal operation, omit J1 and J2, and clear bit 6 of the MCRA.

*When used in the configuration as a parallel modem (Figure 6), connect Pin 27 of SC11006 to SOUT pin of controller and connect Pin 26 of SC11006 to SIN pin of controller.

Figure 7. Common Portion of 2400 BPS Modem.

CONFIGURATIONS FOR SC11019CN, 20CN, 20CV, 22CV BIG MACS



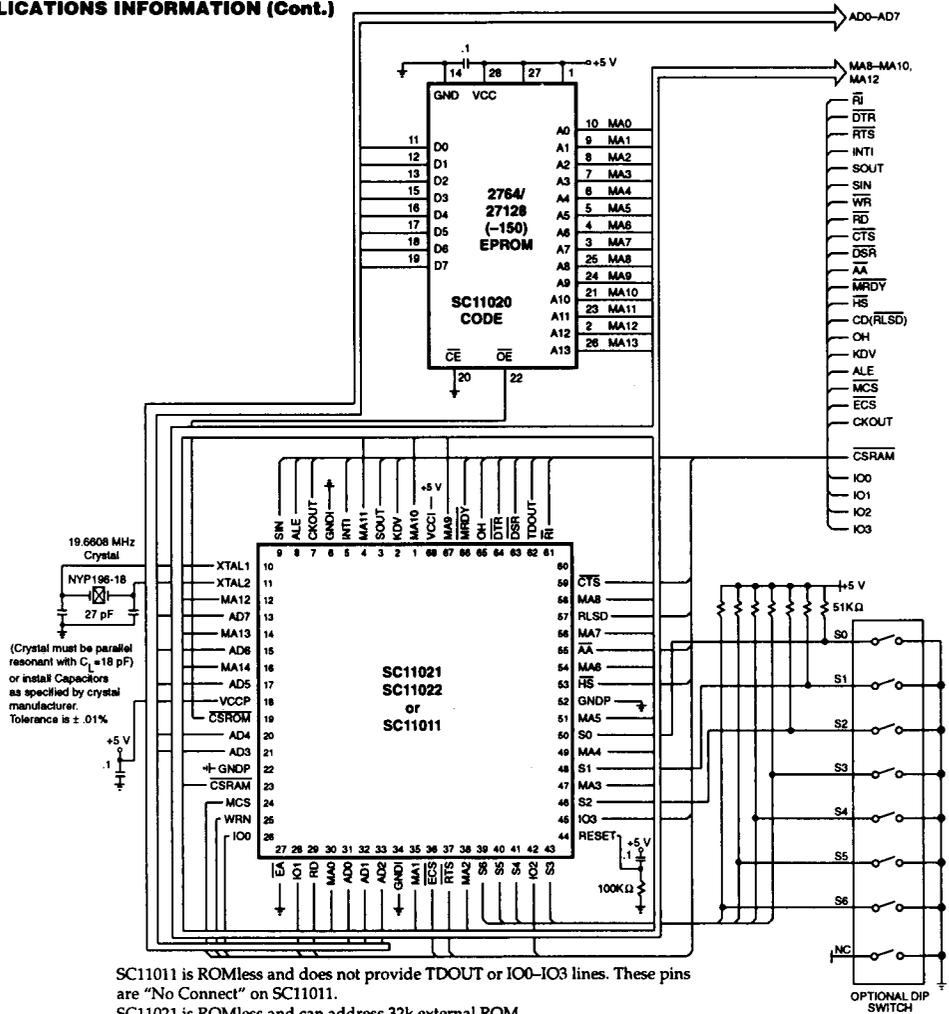
All models listed above can operate with either serial or multiplexed EEPROMs for configuration and number storage. The internal ROM program automatically determines which kind of EEPROM is connected and adapts accordingly.

Note that the SC11022 pin configuration matches that of the SC11011 controller except five new pins are used that were formerly not connected. Four of these are the I/O pins described above. One is the TDOUT pin which

will be used in later versions for V.23 signalling.

When substituting SC11022 for SC11011 it is only necessary to open the EA pin and remove the external EPROM. Connect the jumpers as shown if required to operate with external hybrid or in serial mode.

Three of the four I/O pins on the specified models of the internal ROMed MAC are programmed to set the configuration at power-up or reset. Internal weak pull-up resistors will set the



SC11011 is ROMless and does not provide TDOUT or IO0-IO3 lines. These pins are "No Connect" on SC11011.
 SC11021 is ROMless and can address 32k external ROM.
 SC11022 has 16k internal ROM and can address 24k external ROM.
 Consult controller data sheet for programming information.

Figure 8. Special Purpose Control Processor for Stand-Alone or Parallel Applications.

default configuration to internal hybrid, and Parallel mode if there is no external pull-down.

External pull-down resistors must be added to select other options as indicated in the table. The I/O drivers will overcome these pull-up or pull-down resistors in normal operation to operate the serial EEPROM. The I/O pins may be directly grounded if the serial EEPROM is not used.

In the 44-pin version of SC11019, the I/O pins are not externally available.

APPLICATIONS INFORMATION (Cont.)

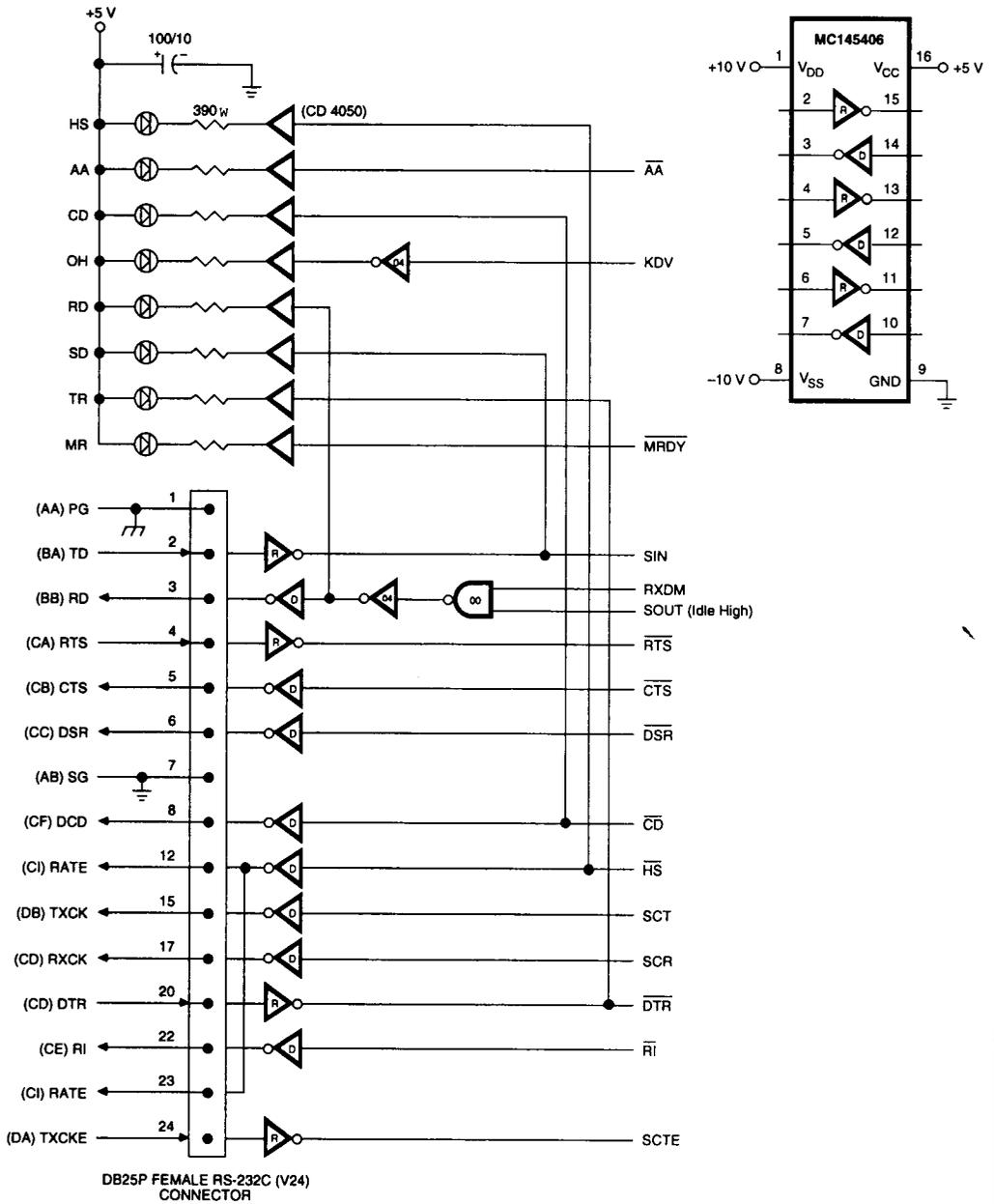


Figure 9. RS-232C Interface for Stand-Alone Modem Application.

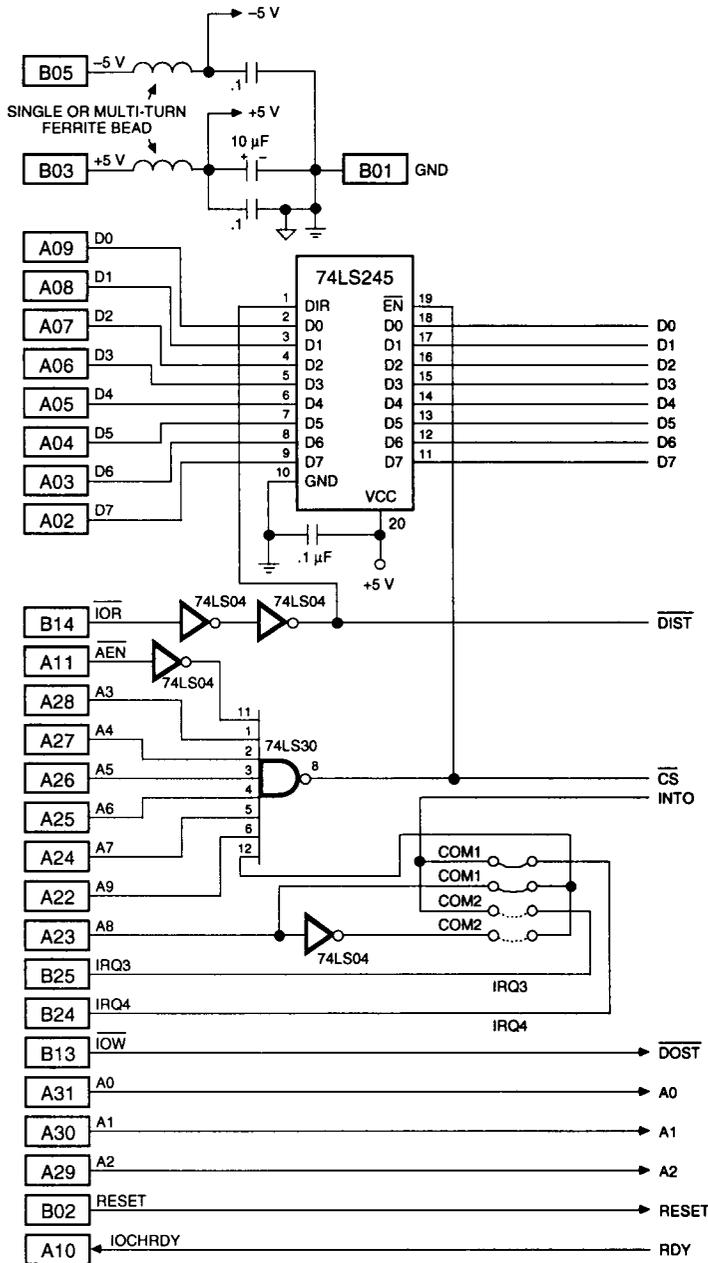


Figure 10. IBM PC/XT/AT Compatible Computer Bus Interface for SC11019 Controller of Figure 7.



APPLICATIONS INFORMATION (Cont.)

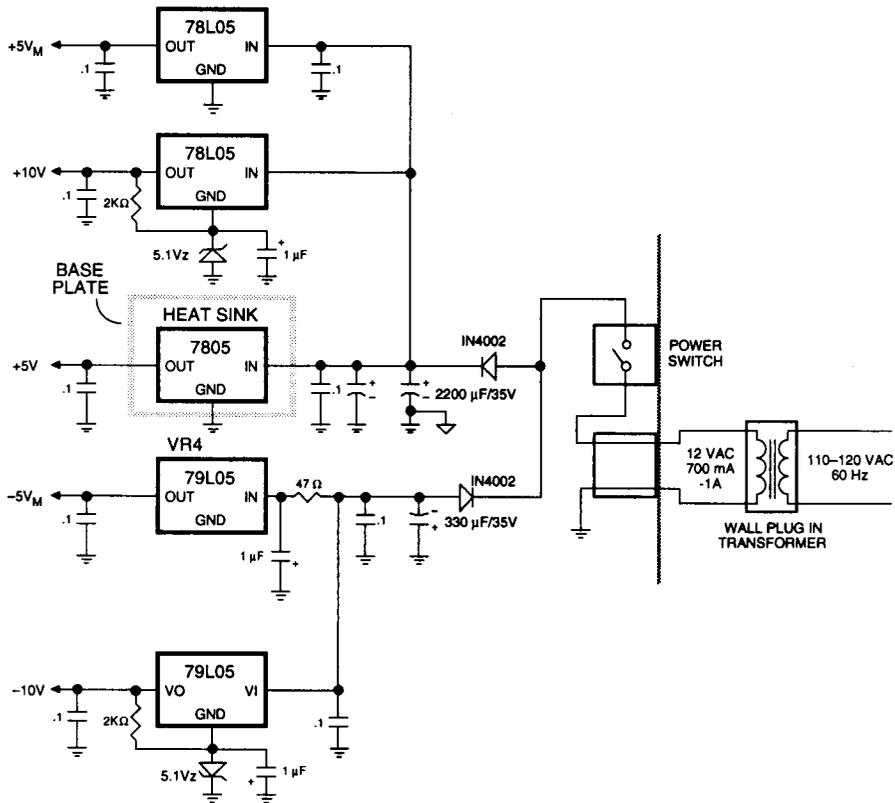


Figure 11. A Typical Power Supply for Stand-Alone Modem Application.

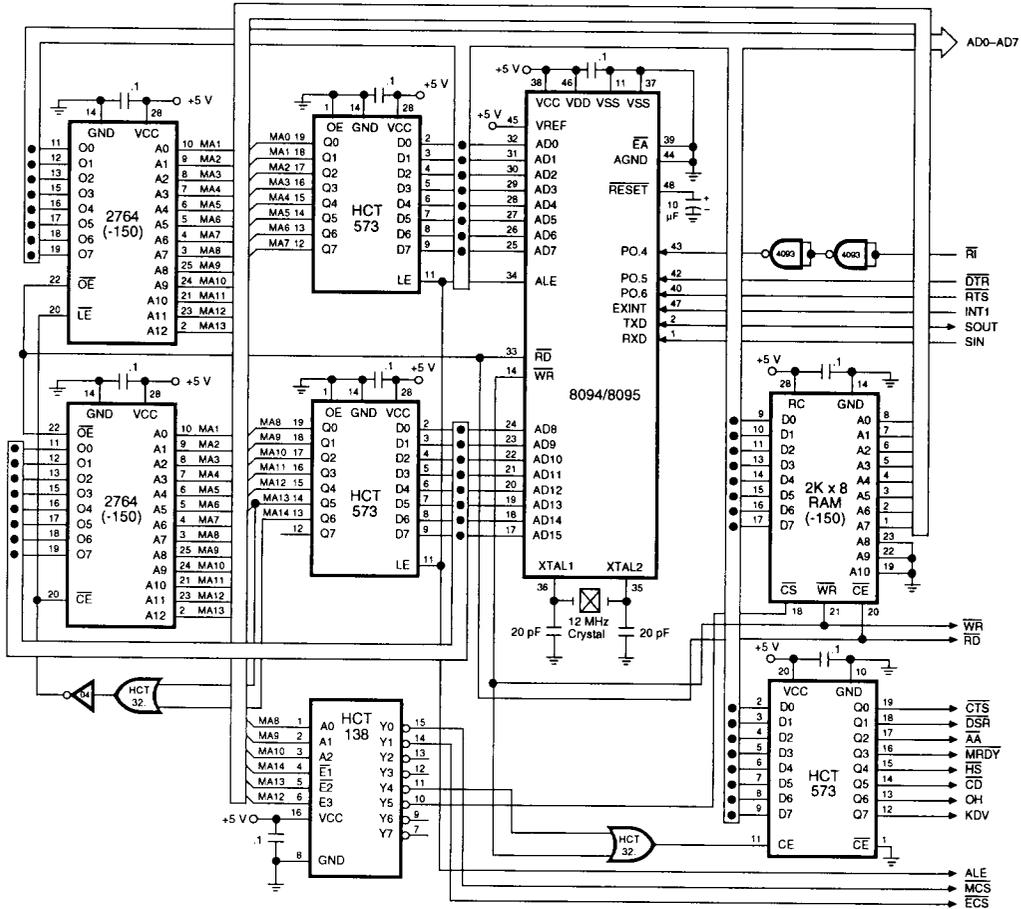


Figure 12. Control Processor Using 8095



APPLICATIONS INFORMATION (Cont.)

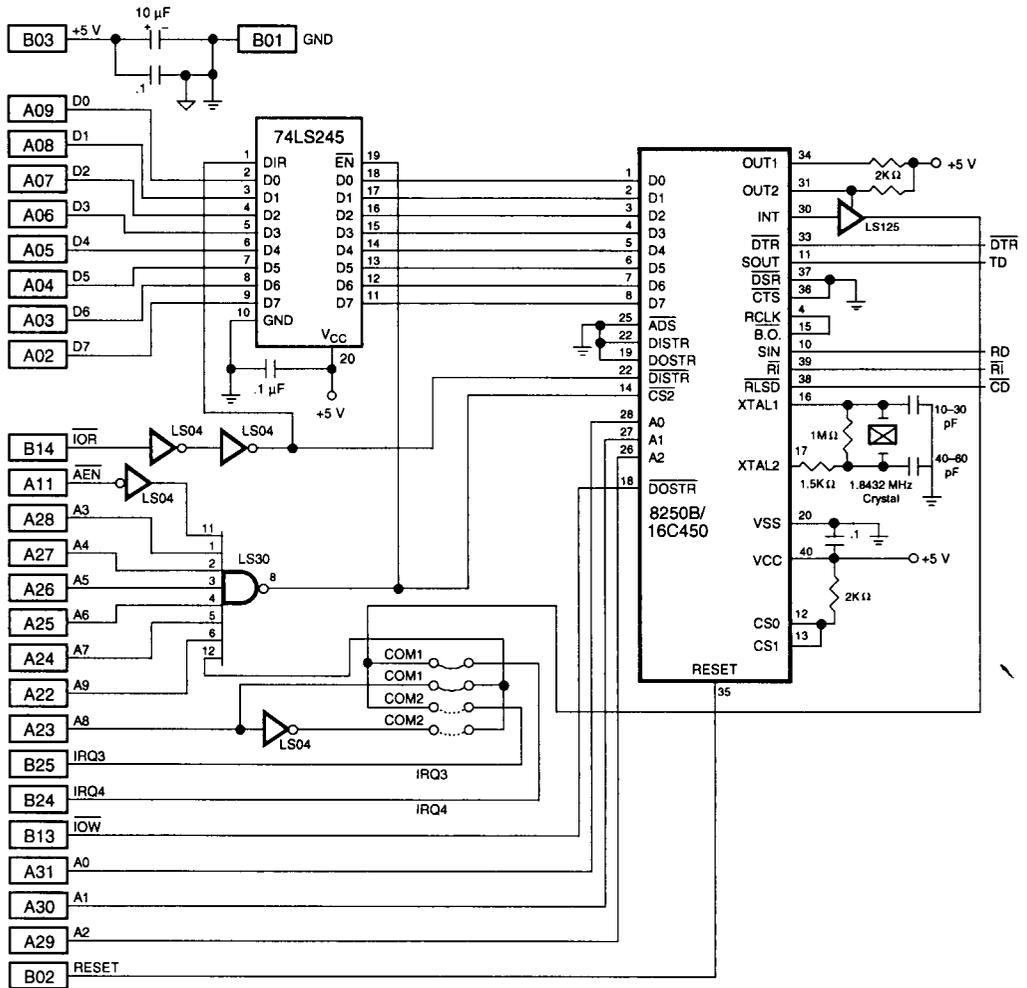
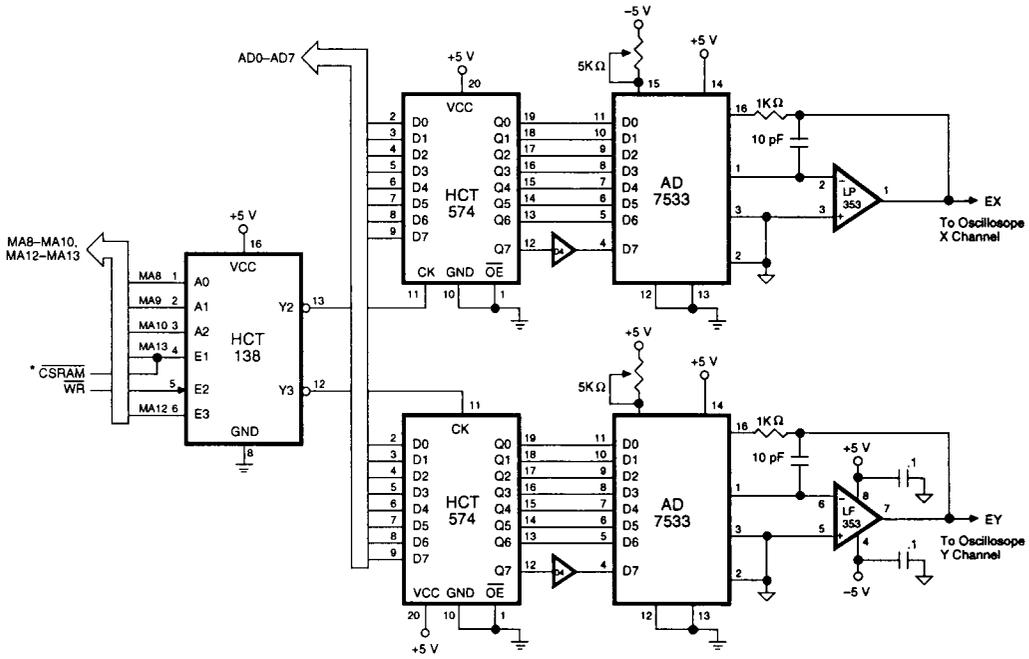


Figure 13. IBM PC/XT/AT Compatible Computer Bus Interface for 8095 Controller of Figure 12.



*IF THE SC11019, SC11020 FAMILY IS USED, CONNECT $\overline{\text{CSRAM}}$, IF AN 8096 IS USED, CONNECT MA13.

Figure 14. Test Circuit to Generate "Eye Pattern".

