

POWER MANAGEMENT
Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

| Parameter | Symbol | Maximum | Units |
|--|---------------|-------------|-------|
| VCC to AGND | V_{IN} | -0.3 to +7 | V |
| PGNDH, PGNDL to AGND | | ±1 | V |
| BSTH to PGNDH, BSTL to PGNDL | | -0.3 to +15 | V |
| DH to PGNDH, DL to PGNDL (Note2) | | -1 to +15 | V |
| Operating Temperature Range | T_A | 0 to +70 | °C |
| Junction Temperature Range | T_J | 0 to +125 | °C |
| Storage Temperature Range | T_{STG} | -65 to +150 | °C |
| Lead Temperature (Soldering) 10 Sec. | T_{LEAD} | 300 | °C |
| Thermal Resistance Junction to Ambient | θ_{JA} | 80 | °C/W |
| Thermal Impedance Junction to Case | θ_{JC} | 25 | °C/W |

Electrical Characteristics

Unless specified: $V_{CC} = 4.75V$ to $5.25V$; $GND = P_{GND} = 0V$; $V_{OSENSE} = V_O$; $0mV < (CS+ - CS-) < 60mV$; $LDOV = 11.4V$ to $12.6V$; $T_A = 0$ to $70^\circ C$

| Parameter | Conditions | Min | Typ | Max | Units |
|------------------------------|--|--------------------------|------|------------|--------------|
| Switching Section | | | | | |
| Output Voltage | $I_O = 2A$ in Application Circuit | See Output Voltage Table | | | |
| Supply Voltage | VCC | 4.5 | | 7 | V |
| Supply Current | VCC = 5.0V | | 8 | 15 | mA |
| Load Regulation | $I_O = 0.8A$ to $24A$ | | 1 | | % |
| Line Regulation | | | +0.5 | | % |
| Current Limit Voltage | | 55 | 70 | 85 | mV |
| Oscillator Frequency | | 170 | 200 | 230 | kHz |
| Oscillator Max Duty Cycle | | 90 | 95 | | % |
| Peak DH Sink/Source Current | BSTH - DH = 4.5V, DH - PGNDH = 3.3V DH - PGNDH = 1.5V | 2 1 100 | | | A A mA |
| Peak DL Sink/Source Current | BSTL - DL = 4.5V, DL - PGNDL = 3.3V DL - PGNDL = 1.5V | 2 1 100 | | | A A mA |
| Gain (A_{OL}) | VOSENSE to V_O | | 35 | | dB |
| VID Source Current | VIDx ≤ 2.4V | 1 | 10 | | uA |
| VID Leakage | VIDx = 3.3V VIDx = 0V | | | ±10 100 | μA μA |
| Power good threshold voltage | | 88 | | 112 | % |
| Dead Time | | 40 | 100 | | ns |

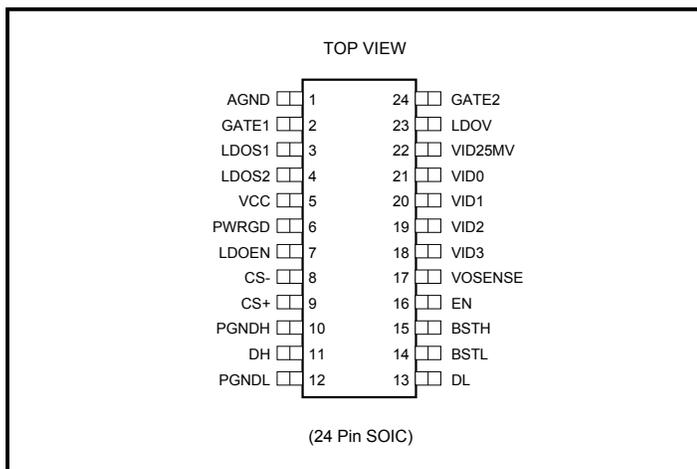
POWER MANAGEMENT
Electrical Characteristics (Cont.)

Unless specified: $V_{CC} = 4.75V$ to $5.25V$; $GND = P_{GND} = 0V$; $V_{OSENSE} = V_O$; $0mV < (CS+ - CS-) < 60mV$; $LDOV = 11.4V$ to $12.6V$; $T_A = 0$ to $70^\circ C$

| Parameter | Conditions | Min | Typ | Max | Units |
|--|---------------------------------|-------|--------------|-------------|--------------------|
| Linear Sections | | | | | |
| Quiescent Current | LDOV = 12V | | | 5 | mA |
| Output Voltage LDO1 | | 2.487 | 2.525 | 2.563 | V |
| Output Voltage LDO2 | | 1.231 | 1.250 | 1.269 | V |
| Gain (A_{OL}) | LDOS (1,2) to GATE (1,2) | | 90 | | dB |
| Load Regulation | $I_o = 0$ to 8A | | | 0.3 | % |
| Line Regulation | | | | 0.3 | % |
| Output Impedance | VGATE = 6.5V | | 1 | 1.5 | k Ω |
| LDOV Undervoltage Lockout | | 6.5 | 8.0 | 10 | V |
| LDOEN Threshold | | 1.3 | | 1.9 | V |
| LDOEN Sink Current | LDOEN = 3.3V LDOEN = 0V | | 0.01 -200 | 1.0 -300 | μA μA |
| Overcurrent Trip Voltage | % of V_o set point | 20 | 40 | 60 | % |
| Power-up Output Short Circuit Immunity | | 1 | 5 | 60 | ms |
| Output Short Circuit Glitch Immunity | | 0.5 | 4 | 30 | ms |
| Gate Pulldown Impedance | GATE (1,2) -AGND; VCC+BST=0V | 80 | 300 | 750 | k Ω |
| VOSENSE Impedance | | 10 | | | k Ω |

Notes:

- (1) This device is ESD sensitive. Use of standard ESD handling precautions is required.
- (2) See Gate Resistor Selection recommendations.

POWER MANAGEMENT
Pin Configuration

Ordering Information

| Device ⁽¹⁾ | Package | Linear Voltage | Temp Range (T _j) |
|----------------------------|---------|----------------|------------------------------|
| SC1189SWTR | SO-24 | 1.25V/2.5V | 0° to 125°C |
| SC1189SWTRT ⁽²⁾ | | | |

Notes:

(1) Only available in tape and reel packaging. A reel contains 1000 devices.

(2) Lead free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

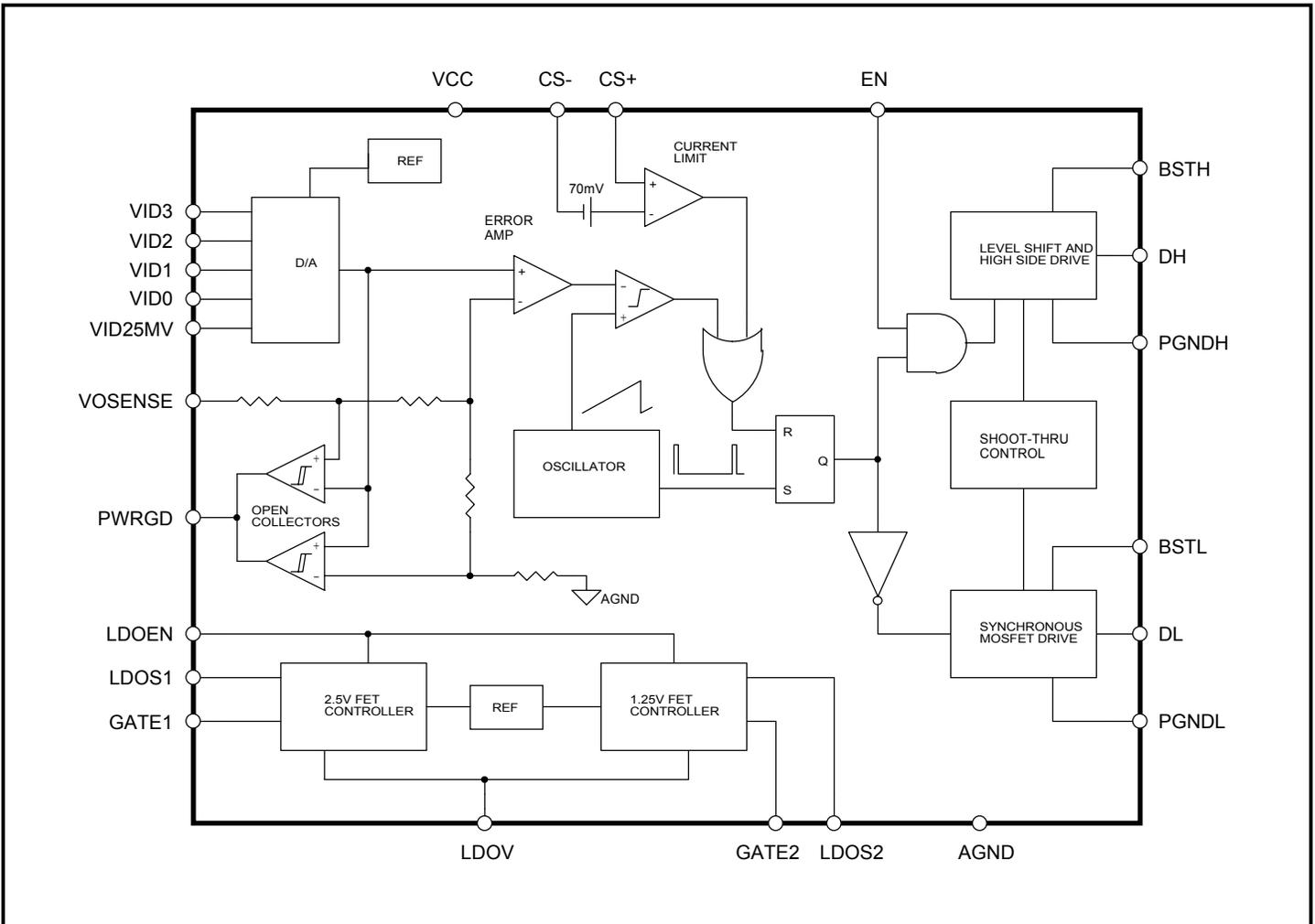
| Pin # | Pin Name | Pin Function |
|-------|------------------------|---|
| 1 | AGND | Small Signal Analog and Digital Ground |
| 2 | GATE1 | Gate Drive Output LDO1 |
| 3 | LDOS1 | Sense Input for LDO1 |
| 4 | LDOS2 | Sense Input for LDO2 |
| 5 | VCC | Input Voltage |
| 6 | PWRGD | Power Good Output, pulls low if VCC_CORE is outside valid range |
| 7 | LDOEN | LDO Supply Monitor. |
| 8 | CS- | Current Sense Input (negative) |
| 9 | CS+ | Current Sense Input (positive) |
| 10 | PGNDH | Power Ground for High Side Switch |
| 11 | DH | High Side Driver Output |
| 12 | PGNDL | Power Ground for Low Side Switch |
| 13 | DL | Low Side Driver Output |
| 14 | BSTL | Supply for Low Side Driver |
| 15 | BSTH | Supply for High Side Driver |
| 16 | EN ⁽¹⁾ | Logic low shuts down the converter, High or open for normal operation |
| 17 | VOSENSE | Top end of internal feedback chain. |
| 18 | VID3 ⁽¹⁾ | Programming Input (MSB) |
| 19 | VID2 ⁽¹⁾ | Programming Input |
| 20 | VID1 ⁽¹⁾ | Programming Input |
| 21 | VID0 ⁽¹⁾ | Programming Input |
| 22 | VID25MV ⁽¹⁾ | Programming Input (LSB) |
| 23 | LDOV | +12V for LDO section |
| 24 | GATE2 | Gate Drive Output LDO2 |

Note:

(1) All logic level inputs and outputs are open collector TTL compatible.

POWER MANAGEMENT

Block Diagram



POWER MANAGEMENT
Applications Information - Output Voltage Table

 Unless specified: 4.75V < VCC < 5.25V; GND = PGND = 0V; VOSENSE = V_O; 0mV < (CS+ - CS-) < 60mV; = 0°C < T_j < 85°C

| Parameter | Conditions | VID | | Min | Typ | Max | Units |
|-------------------------------|--|------|------|-------|-------|-------|-------|
| | | 25MV | 3210 | | | | |
| Output Voltage ⁽¹⁾ | I _O = 2A in Application circuit | 0 | 0100 | 1.034 | 1.050 | 1.066 | V |
| | | 1 | 0100 | 1.059 | 1.075 | 1.091 | |
| | | 0 | 0011 | 1.084 | 1.100 | 1.117 | |
| | | 1 | 0011 | 1.108 | 1.125 | 1.142 | |
| | | 0 | 0010 | 1.133 | 1.150 | 1.167 | |
| | | 1 | 0010 | 1.157 | 1.175 | 1.193 | |
| | | 0 | 0001 | 1.182 | 1.200 | 1.218 | |
| | | 1 | 0001 | 1.207 | 1.225 | 1.243 | |
| | | 0 | 0000 | 1.231 | 1.250 | 1.269 | |
| | | 1 | 0000 | 1.256 | 1.275 | 1.294 | |
| | | 0 | 1111 | 1.281 | 1.300 | 1.320 | |
| | | 1 | 1111 | 1.305 | 1.325 | 1.345 | |
| | | 0 | 1110 | 1.330 | 1.350 | 1.370 | |
| | | 1 | 1110 | 1.354 | 1.375 | 1.396 | |
| | | 0 | 1101 | 1.379 | 1.400 | 1.421 | |
| | | 1 | 1101 | 1.404 | 1.425 | 1.446 | |
| | | 0 | 1100 | 1.428 | 1.450 | 1.472 | |
| | | 1 | 1100 | 1.453 | 1.475 | 1.497 | |
| | | 0 | 1011 | 1.478 | 1.500 | 1.523 | |
| | | 1 | 1011 | 1.502 | 1.525 | 1.548 | |
| | | 0 | 1010 | 1.527 | 1.550 | 1.573 | |
| | | 1 | 1010 | 1.551 | 1.575 | 1.599 | |
| | | 0 | 1001 | 1.584 | 1.600 | 1.616 | |
| | | 1 | 1001 | 1.609 | 1.625 | 1.641 | |
| | | 0 | 1000 | 1.634 | 1.650 | 1.667 | |
| | | 1 | 1000 | 1.658 | 1.675 | 1.692 | |
| | | 0 | 0111 | 1.683 | 1.700 | 1.717 | |
| | | 1 | 0111 | 1.708 | 1.725 | 1.742 | |
| | | 0 | 0110 | 1.733 | 1.750 | 1.768 | |
| | | 1 | 0110 | 1.757 | 1.775 | 1.793 | |
| | | 0 | 0101 | 1.782 | 1.800 | 1.818 | |
| | | 1 | 0101 | 1.798 | 1.825 | 1.852 | |

Note 1: VID[3:0] correspond to legacy VRM8.4 voltage levels for 1.3V to 1.8V

POWER MANAGEMENT

Layout Guidelines

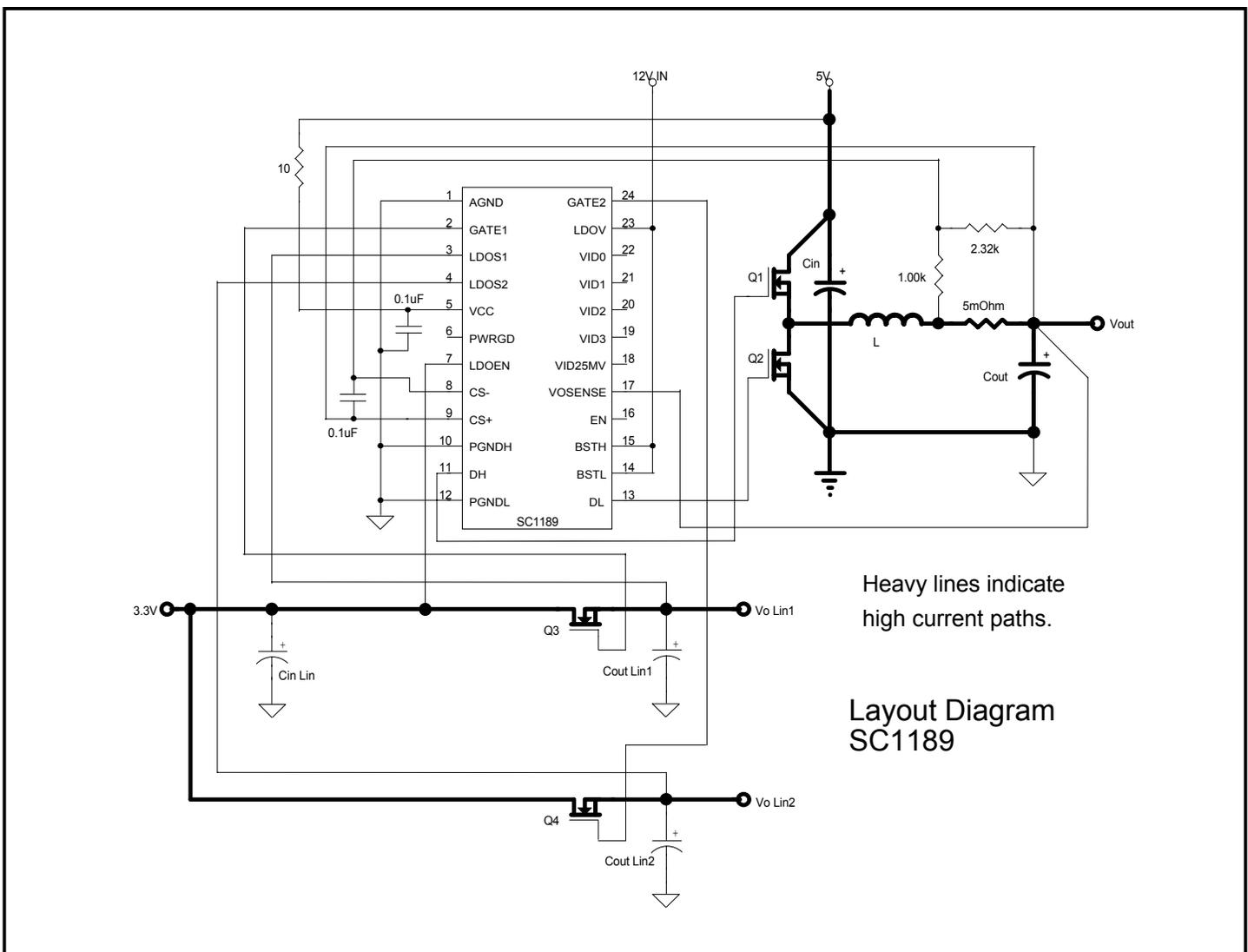
Careful attention to layout requirements are necessary for successful implementation of the SC1189 PWM controller. High currents switching at 200kHz are present in the application and their effect on ground plane voltage differentials must be understood and minimized.

1). The high power parts of the circuit should be laid out first. A ground plane should be used, the number and position of ground plane interruptions should be such as to not unnecessarily compromise ground plane integrity. Isolated or semi-isolated areas of the ground plane may be deliberately introduced to constrain ground currents to particular areas, for example the input capacitor and bottom FET ground.

2). The loop formed by the Input Capacitor(s) (Cin), the Top FET (Q1) and the Bottom FET (Q2) must be kept as small as possible. This loop contains all the high current, fast

transition switching. Connections should be as wide and as short as possible to minimize loop inductance. Minimizing this loop area will a) reduce EMI, b) lower ground injection currents, resulting in electrically “cleaner” grounds for the rest of the system and c) minimize source ringing, resulting in more reliable gate switching signals.

3). The connection between the junction of Q1, Q2 and the output inductor should be a wide trace or copper region. It should be as short as practical. Since this connection has fast voltage transitions, keeping this connection short will minimize EMI. The connection between the output inductor and the sense resistor should be a wide trace or copper area, there are no fast voltage or current transitions in this connection and length is not so important, however adding unnecessary impedance will reduce efficiency.



Heavy lines indicate high current paths.

Layout Diagram SC1189

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Layout Guidelines (Cont.)

4) The Output Capacitor(s) (Cout) should be located as close to the load as possible, fast transient load currents are supplied by Cout only, and connections between Cout and the load must be short, wide copper areas to minimize inductance and resistance.

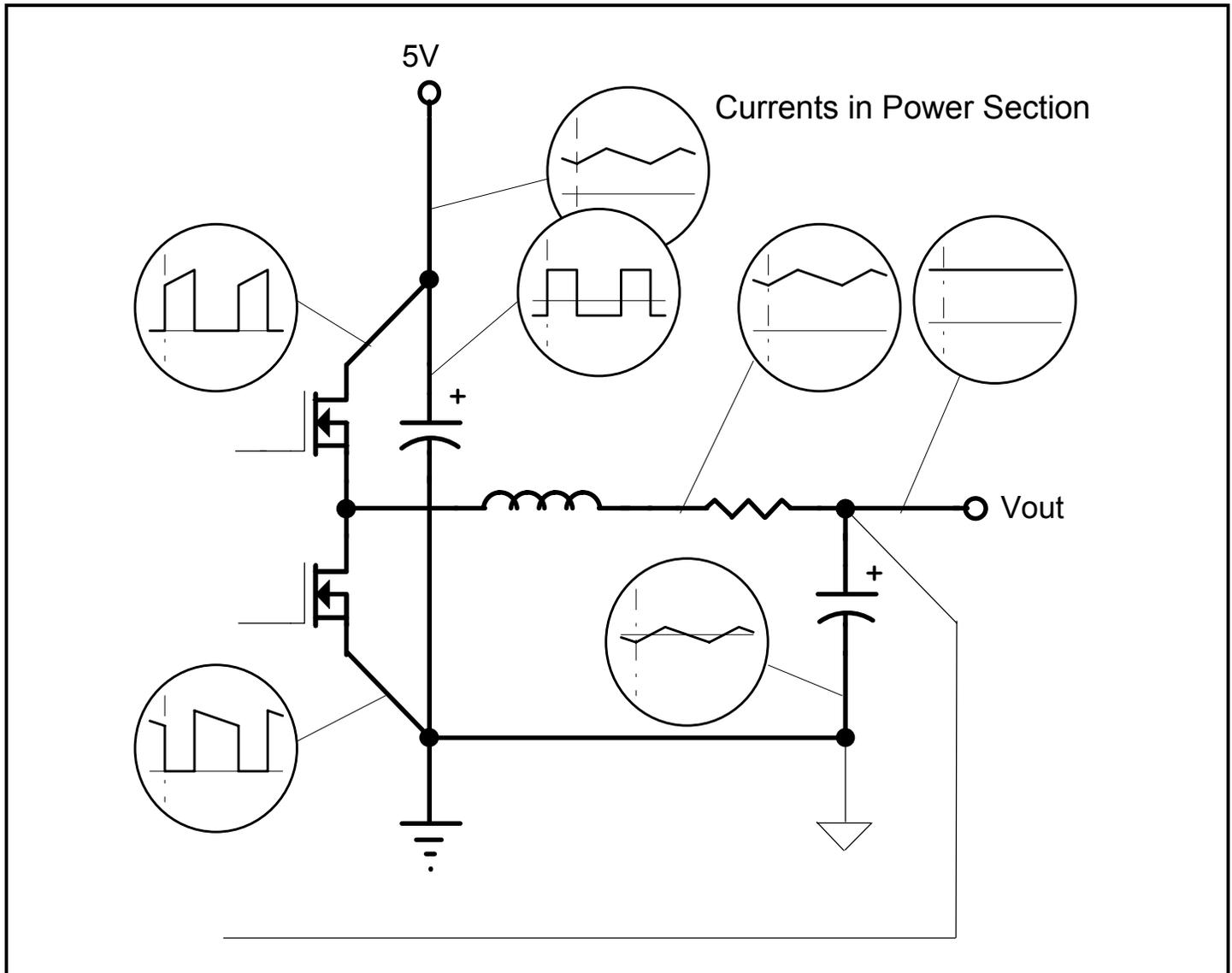
5) The SC1189 is best placed over a quiet ground plane area, avoid pulse currents in the Cin, Q1, Q2 loop flowing in this area. PGNDH and PGNDL should be returned to the ground plane close to the package. The AGND pin should be connected to the ground side of (one of) the output capacitor(s). If this is not possible, the AGND pin may be connected to the ground path between the Output Capacitor(s) and the Cin, Q1, Q2 loop. Under no circumstances should AGND be returned to a ground inside the

Cin, Q1, Q2 loop.

6) Vcc for the SC1189 should be supplied from the 5V supply through a 10Ω resistor, the Vcc pin should be decoupled directly to AGND by a 0.1μF ceramic capacitor, trace lengths should be as short as possible.

7) The Current Sense resistor and the divider across it should form as small a loop as possible, the traces running back to CS+ and CS- on the SC1189 should run parallel and close to each other. The 0.1μF capacitor should be mounted as close to the CS+ and CS- pins as possible.

8) Ideally, the grounds for the two LDO sections should be returned to the ground side of (one of) the output capacitor(s).



POWER MANAGEMENT
Component Selection
SWITCHING SECTION

OUTPUT CAPACITORS - Selection begins with the most critical component. Because of fast transient load current requirements in modern microprocessor core supplies, the output capacitors must supply all transient load current requirements until the current in the output inductor ramps up to the new level. Output capacitor ESR is therefore one of the most important criteria. The maximum ESR can be simply calculated from:

$$R_{ESR} \leq \frac{V_t}{I_t}$$

Where

V_t = Maximum transient voltage excursion

I_t = Transient current step

For example, to meet a 100mV transient limit with a 10A load step, the output capacitor ESR must be less than 10mΩ. To meet this kind of ESR level, there are three available capacitor technologies.

| Technology | Each Cap. | | Qty. Rqd. | Total | |
|------------------|-----------|-------------|--------------|-----------|-------------|
| | C (μF) | ESR (mΩ) | | C (μF) | ESR (mΩ) |
| Low ESR Tantalum | 330 | 60 | 6 | 2000 | 10 |
| OS-CON | 330 | 25 | 3 | 990 | 8.3 |
| Low ESR Aluminum | 1500 | 44 | 5 | 7500 | 8.3 |

The choice of which to use is simply a cost/performance issue, with Low ESR Aluminum being the cheapest, but taking up the most space.

INDUCTOR - Having decided on a suitable type and value of output capacitor, the maximum allowable value of inductor can be calculated. Too large an inductor will produce a slow current ramp rate and will cause the output capacitor to supply more of the transient load current for longer - leading to an output voltage sag below the ESR excursion calculated above.

The maximum inductor value may be calculated from:

$$L \leq \frac{R_{ESR} \cdot C}{I_t} \cdot V_A$$

where V_A is the lesser of V_O or $(V_{IN} - V_O)$

The calculated maximum inductor value assumes 100%

and 0% duty cycle capability, so some allowance must be made. Choosing an inductor value of 50 to 75% of the calculated maximum will guarantee that the inductor current will ramp fast enough to reduce the voltage dropped across the ESR at a faster rate than the capacitor sags, hence ensuring a good recovery from transient with no additional excursions.

We must also be concerned with ripple current in the output inductor and a general rule of thumb has been to allow 10% of maximum output current as ripple current. Note that most of the output voltage ripple is produced by the inductor ripple current flowing in the output capacitor ESR. Ripple current can be calculated from:

$$I_{LRIFFLE} = \frac{V_{IN}}{4 \cdot L \cdot f_{OSC}}$$

Ripple current allowance will define the minimum permitted inductor value.

POWER FETS - The FETs are chosen based on several criteria, with probably the most important being power dissipation and power handling capability.

TOP FET - The power dissipation in the top FET is a combination of conduction losses, switching losses and bottom FET body diode recovery losses.

a) Conduction losses are simply calculated as:

$$P_{COND} = I_O^2 \cdot R_{DS(on)} \cdot \delta$$

where

$$\delta = \text{duty cycle} \approx \frac{V_O}{V_{IN}}$$

b) Switching losses can be estimated by assuming a switching time, if we assume 100ns then:

$$P_{SW} = I_O \cdot V_{IN} \cdot 10^{-2}$$

or more generally,

$$P_{SW} = \frac{I_O \cdot V_{IN} \cdot (t_r + t_f) \cdot f_{OSC}}{4}$$

c) Body diode recovery losses are more difficult to estimate, but to a first approximation, it is reasonable to assume that the stored charge on the bottom FET body diode will be moved through the top FET as it starts to turn on. The resulting power dissipation in the top FET will be:

$$P_{RR} = Q_{RR} \cdot V_{IN} \cdot f_{OSC}$$

To a first order approximation, it is convenient to only con-

POWER MANAGEMENT
Component Selection (Cont.)

sider conduction losses to determine FET suitability. For a 5V in; 2.8V out at 14.2A requirement, typical FET losses would be:

Using 1.5X Room temp $R_{DS(on)}$ to allow for temperature rise.

| FET type | $R_{DS(on)}$ (mΩ) | P_D (W) | Package |
|----------|-------------------|-----------|--------------------|
| IRL34025 | 15 | 1.69 | D ² Pak |
| IRL2203 | 10.5 | 1.19 | D ² Pak |
| Si4410 | 20 | 2.26 | S0-8 |

BOTTOM FET - Bottom FET losses are almost entirely due to conduction. The body diode is forced into conduction at the beginning and end of the bottom switch conduction period, so when the FET turns on and off, there is very little voltage across it, resulting in low switching losses. Conduction losses for the FET can be determined by:

$$P_{COND} = I_O^2 \cdot R_{DS(on)} \cdot (1 - \delta)$$

For the example above:

| FET type | $R_{DS(on)}$ (mΩ) | P_D (W) | Package |
|----------|-------------------|-----------|--------------------|
| IRL34025 | 15 | 1.33 | D ² Pak |
| IRL2203 | 10.5 | 0.93 | D ² Pak |
| Si4410 | 20 | 1.77 | S0-8 |

Each of the package types has a characteristic thermal impedance. For the surface mount packages on double sided FR4, 2 oz printed circuit board material, thermal impedances of 40°C/W for the D²PAK and 80°C/W for the S0-8 are readily achievable. The corresponding temperature rise is detailed below:

| FET type | Temperature Rise (°C) | |
|----------|-----------------------|------------|
| | Top FET | Bottom FET |
| IRL34025 | 67.6 | 53.2 |
| IRL2203 | 47.6 | 37.2 |
| Si4410 | 180.8 | 141.6 |

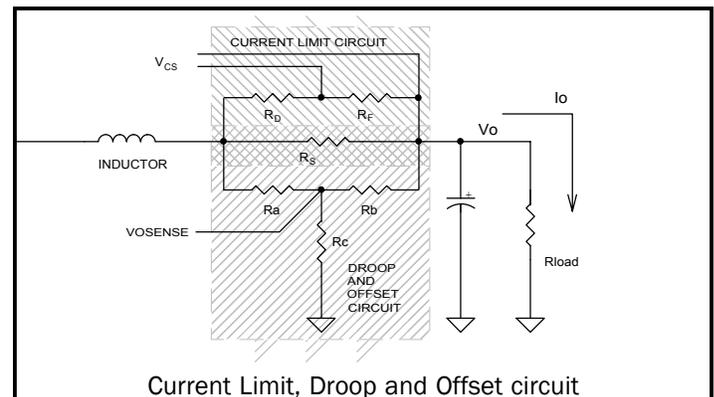
It is apparent that single S0-8 Si4410 are not adequate for this application, but by using parallel pairs in each position, power dissipation will be approximately halved and temperature rise reduced by a factor of 4.

INPUT CAPACITORS - since the RMS ripple current in the input capacitors may be as high as 50% of the output current, suitable capacitors must be chosen accordingly. Also, during fast load transients, there may be restrictions on input di/dt. These restrictions require useable energy storage within the converter circuitry, either as extra output capacitance or, more usually, additional input capacitors. Choosing low ESR input capacitors will help maximize ripple rating for a given size.

GATE RESISTOR SELECTION - The gate resistors for the top and bottom switching FETs limit the peak gate current and hence control the transition time. It is important to control the off time transition of the top FET, it should be fast to limit switching losses, but not so fast as to cause excessive phase node oscillation below ground as this can lead to current injection in the IC substrate and erratic behaviour or latchup. The actual value should be determined in the application, with the final layout and FETs.

CURRENT SENSE, LIMIT, DROOP AND OFFSET

The converter is protected and it's loadline shaped by the signals generated from the sense resistor and associated components.



Current Limit is given by

$$I_{OLIM} = V_{CS} \cdot (R_D + R_F) / (R_S \cdot R_F)$$

At no load the output voltage is given by:

$$V_O = V_{O(nom)} \cdot (1 + (R_A \cdot R_B) / (R_C \cdot (R_A + R_B)))$$

so the offset is:

$$V_{OS} = V_{O(nom)} \cdot 1000 \cdot (R_A \cdot R_B) / (R_C \cdot (R_A + R_B))$$

and the droop is calculated as:

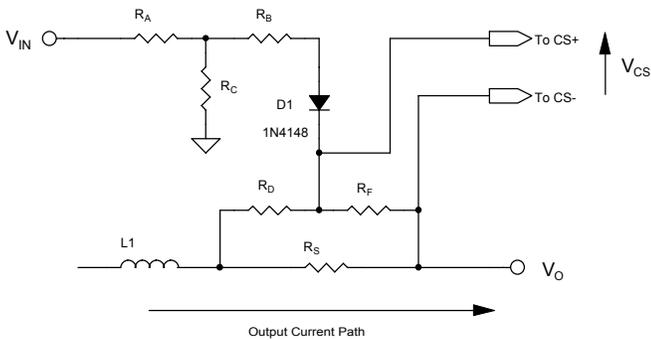
$$V_D = I_O \cdot R_S \cdot R_B / (R_A + R_B)$$

where R_S is in mΩ, V_{OS} and V_D in mV

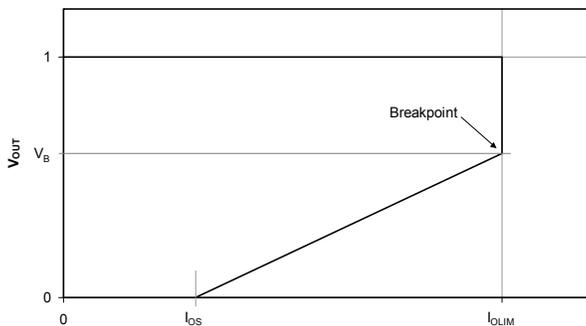
For a full design procedure for droop and offset, see Application Note AN97-9, "Using Droop and Vout Offset for improved transient response".

FOLDBACK CURRENT LIMITING

The SC1189 implements a “Hard Current Limit” overcurrent protection for the switching supply output. In a short circuit condition, this will lead to higher than normal power dissipation in the bottom side FETs. If this is problematic, foldback current limiting can be easily and inexpensively implemented to drastically reduce dissipation during output short circuit



Foldback current limit components



Foldback current limit characteristics

For a complete design procedure for foldback current limiting see Application Note AN01-2, “Foldback Current Limit”. An abbreviated procedure is given below.

1) Choose values for I_{OLIM} and R_S and calculate the ratio

$$\frac{R_F}{R_D + R_F} = \frac{V_{CS}}{I_{OLIM} \cdot R_S}$$

If this ratio > 1 , the value of R_S or I_{OLIM} must be increased. Then let $R_F = 1k\Omega$ and calculate R_D .

2) Choose a short circuit current (I_{OS}) and calculate M , do not be too aggressive with M , a value between 2 and 3 should be sufficient. Choosing too low a value for I_{OS} will result in a high value for M and may cause startup problems due to insufficient current.

$$M = \frac{I_{OLIM}}{I_{OS}}$$

3) Choose V_B and calculate R_B

$$R_B = \frac{M \cdot V_B \cdot R_D \cdot R_F}{(M - 1) V_{CS} (R_D + R_F)}$$

4) Calculate the ratio of the input divider

$$\frac{R_C}{(R_A + R_C)} = \frac{V_B + V_{CS} + V_F}{V_{IN}}$$

where V_F = Forward Voltage drop of diode ($\approx 0.6V$)

Choose $R_C < R_B / 10$ and calculate R_A

SHORT CIRCUIT PROTECTION - LINEARS

The Short circuit feature on the linear controllers is implemented by using the $R_{ds(on)}$ of the FETs. As output current increases, the regulation loop maintains the output voltage by turning the FET on more and more. Eventually, as the $R_{ds(on)}$ limit is reached, the FET will be unable to turn on more fully, and output voltage will start to fall. When the output voltage falls to approximately 50% of nominal, the LDO controller is latched off, setting output voltage to 0. Power must be cycled to reset the latch.

To prevent false latching due to capacitor inrush currents or low supply rails, the current limit latch is initially disabled. It is enabled at a preset time (nominally 2mS) after both the LDOV and LDOEN rails rise above their lockout points.

To be most effective, the linear FET $R_{ds(on)}$ should not be selected artificially low, the FET should be chosen so that, at maximum required current, it is almost fully turned on.

If, for example, a linear supply of 1.5V at 4A is required from a $3.3V \pm 5\%$ rail, max allowable $R_{ds(on)}$ would be.

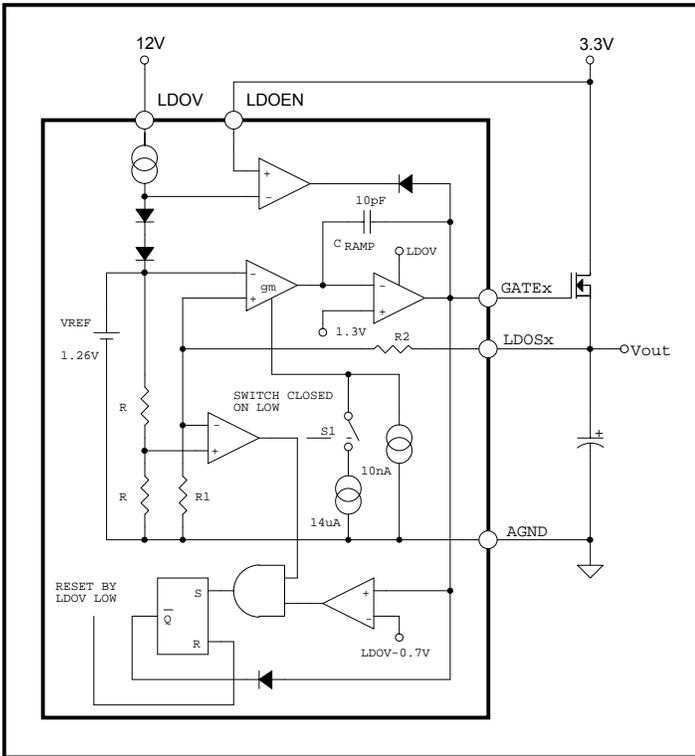
$$R_{ds(on)max} = (0.95 * 3.3 - 1.5) / 4 \approx 400m\Omega$$

To allow for temperature effects 200m Ω would be a suitable room temperature maximum, allowing a peak short circuit current of approximately 15A for a short time before shutdown.

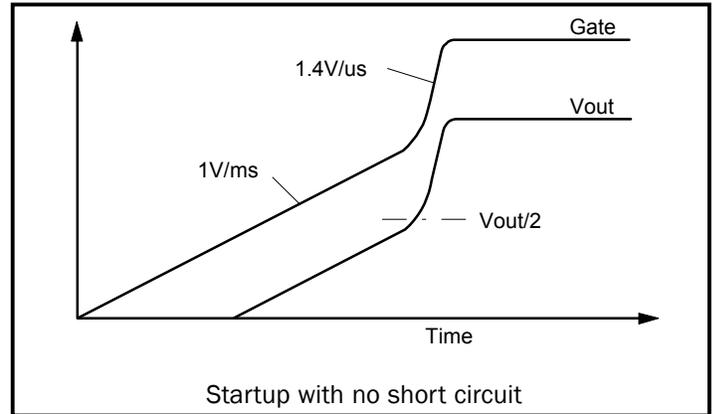
POWER MANAGEMENT

Theory of Operation (Linear OCP)

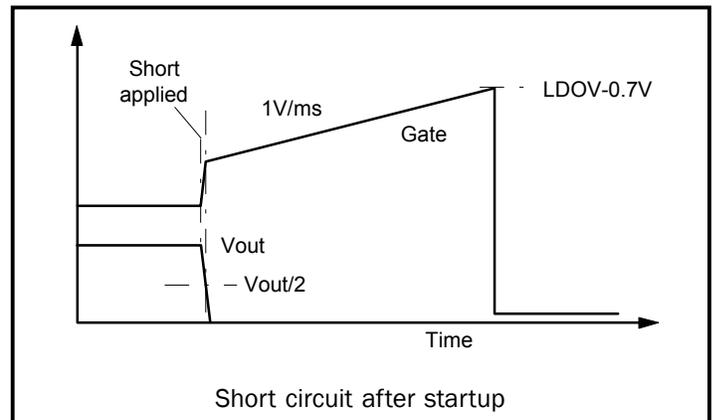
The Linear controllers in the SC1189 have built in Overcurrent Protection (OCP). An overcurrent is assumed to have occurred when the external FET is turned fully on and the output current is $R_{DS(ON)}$ limited, this is detected by the gate voltage going very high while the output voltage is below approximately 40% of it's setpoint. To allow for capacitor charging and very short overcurrent durations, the gate voltage is ramped very slowly upwards whenever the output voltage is below the OCP threshold. To guarantee that the LDO output voltage is capable of reaching it's setpoint, the gate drive is disabled until both LDOV Undervoltage Lockout (UVLO) and LDOEN Threshold values are exceeded, ensuring that there is sufficient gate drive capability and sufficient LDO input voltage capability. A block diagram of one LDO controller is shown below.



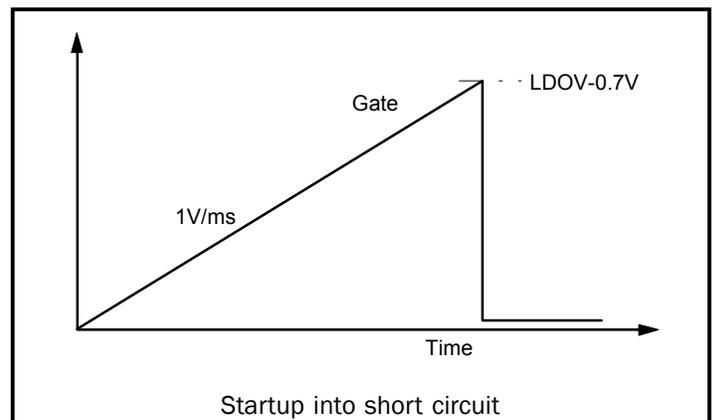
During a normal start-up, once LDOV and LDOEN have reached their thresholds, the GATEx pin is released and C_{RAMP} is charged by 10nA causing the GATEx voltage to ramp at $10nA/10pF = 1V/ms$. Once the GATEx output has ramped to the external FET threshold, Vout starts to ramp up, following GATEx. When Vout reaches the OCP threshold, approximately 40% of setpoint, switch S1 is closed and GATEx ramps up at a much faster rate, followed by Vout, until Vout reaches setpoint and the loop settles into steady state regulation.



If at some later time, a short circuit is applied to the output, the GATEx voltage will ramp up quickly as Vout falls to try and maintain regulation. Once Vout has fallen to the OCP threshold, switch S1 will open and the gate will continue ramping at the 1V/ms rate. If the short is not removed before the GATEx output reaches approximately LDOV - 0.7V, the GATEx pin will be latched low, disabling the LDO

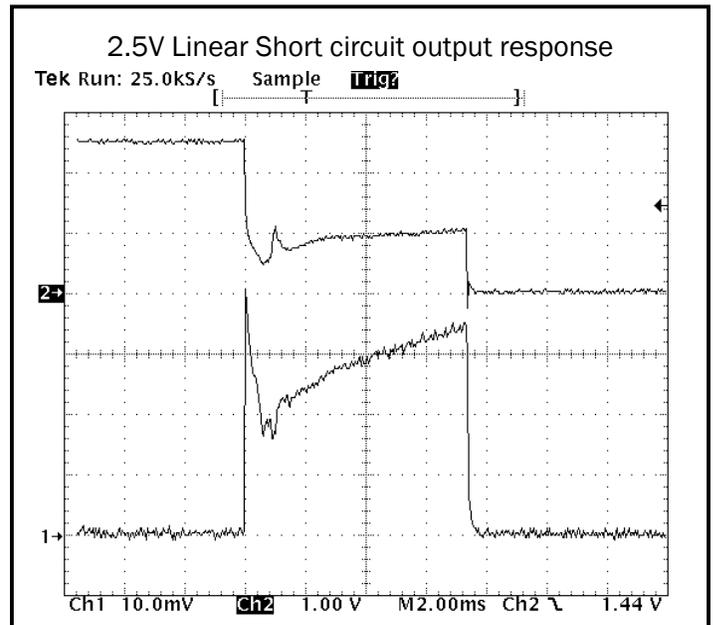
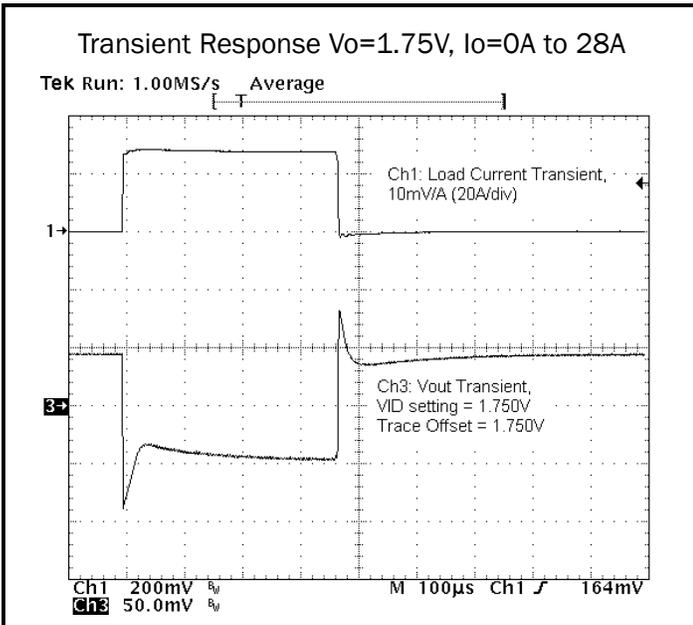
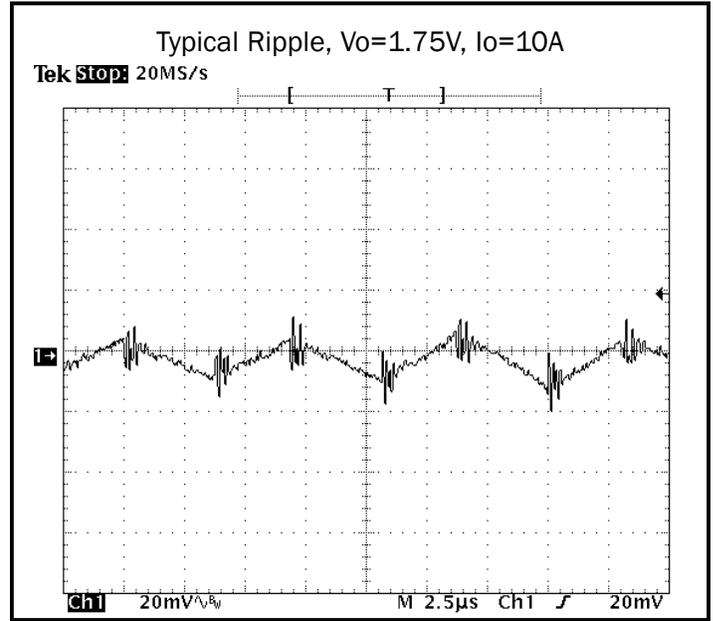
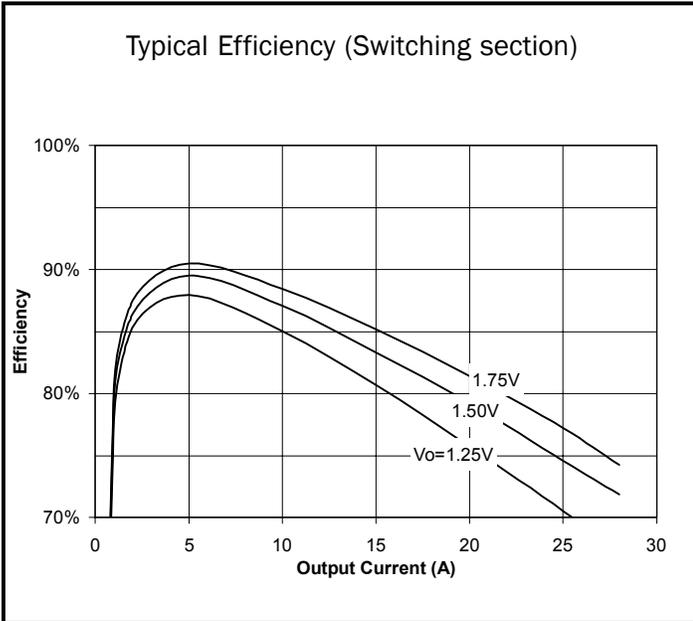


If the LDO tries to start into a short, the gate ramps at the 1V/ms rate to LDOV - 0.7V, where the GATEx pin will be latched low.



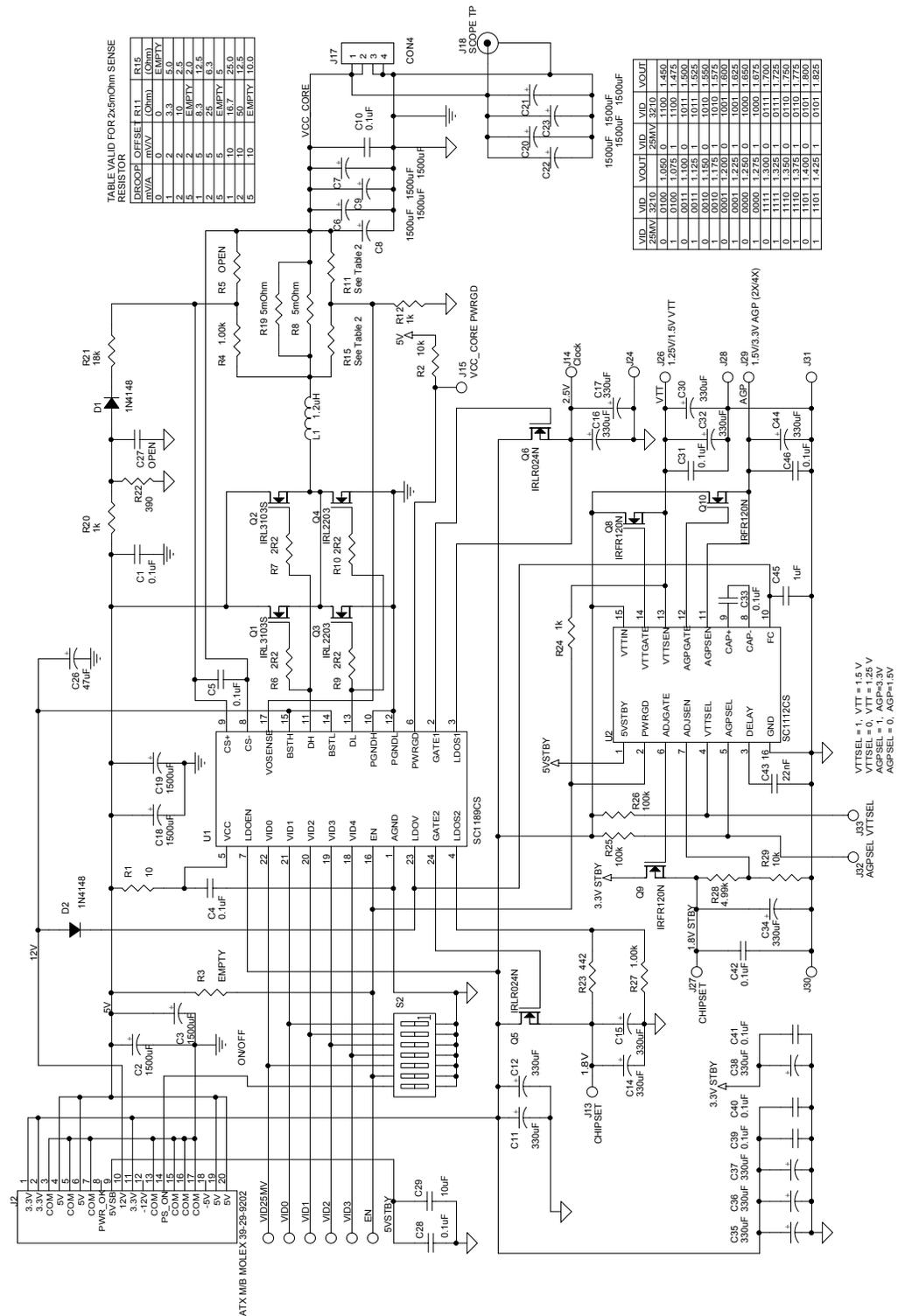
POWER MANAGEMENT

Typical Characteristics



POWER MANAGEMENT

Typical Application Circuit

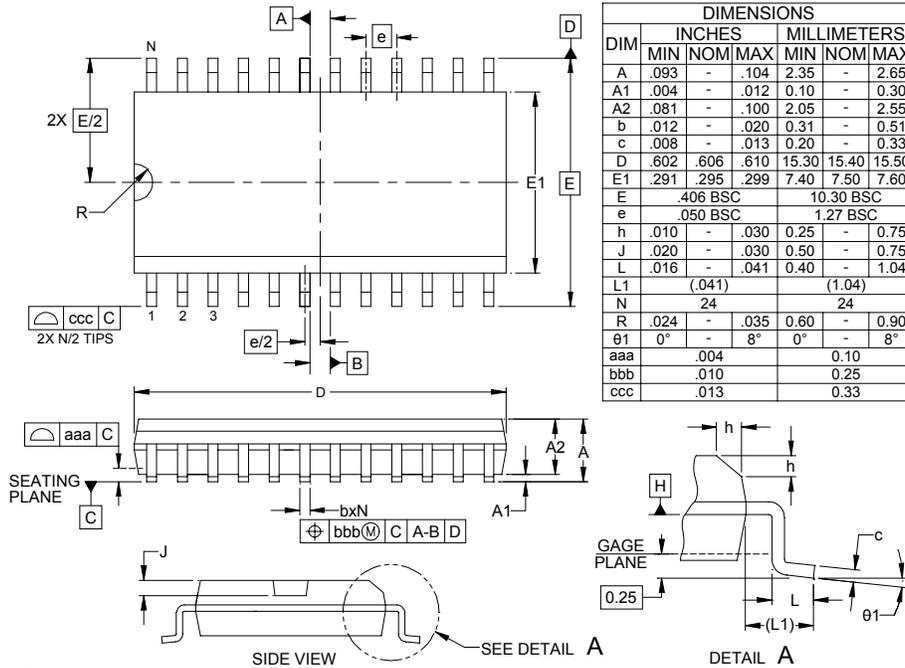


POWER MANAGEMENT
Evaluation Board Bill of Materials

| Item | Qty. | Reference | Value | Notes |
|------|------|--|-----------|-----------------------------------|
| 1 | 12 | C1, C4, C5, C10, C28, C31, C33, C39, C40, C41, C42, C46 | 0.1uF | |
| 2 | 12 | C2, C3, C6, C7, C8, C9, C18, C19, C20, C21, C22, C23 | 1500uF | Low ESR Sanyo MV-GX or equivalent |
| 3 | 14 | C11, C12, C14, C15, C16, C17, C30, C32, C34, C35, C36, C37, C38, C44 | 330uF | |
| 4 | 1 | C26 | 47uF | |
| 6 | 1 | C29 | 10uF | |
| 7 | 1 | C43 | 22nF | |
| 8 | 1 | C45 | 1uF | |
| 9 | 2 | D1, D2 | 1N4148 | |
| 10 | 1 | J2 | ATX M/B | MOLEX 39-29-9202 |
| 6 | 1 | L1 | 1.2uH | Panasonic PCC-S1 |
| 7 | 2 | Q1, Q2 | IRLR3103S | |
| 8 | 2 | Q3, Q4 | IRL2203 | |
| 9 | 2 | Q5, Q6 | IRLR024N | |
| 25 | 3 | Q8, Q9, Q10 | IRFR120N | |
| 10 | 1 | R1 | 10 | |
| 11 | 2 | R2, R29 | 10k | |
| 29 | 2 | R4, R27 | 1.00k | |
| 13 | 4 | R6, R7, R9, R10 | 2R2 | |
| 14 | 2 | R8, R19 | 5mOhm | IRC OAR1 |
| 15 | 2 | R11, R15 | See Table | |
| 12 | 3 | R12, R20, R24 | 1k | |
| 16 | 1 | R21 | 18k | |
| 17 | 1 | R22 | 390 | |
| 36 | 1 | R23 | 442 | |
| 37 | 2 | R26, R25 | 100k | |
| 38 | 1 | R28 | 4.99k | |
| 18 | 1 | U1 | SC1189CS | SEMTECH |
| 41 | 1 | U2 | SC1112CS | SEMTECH |

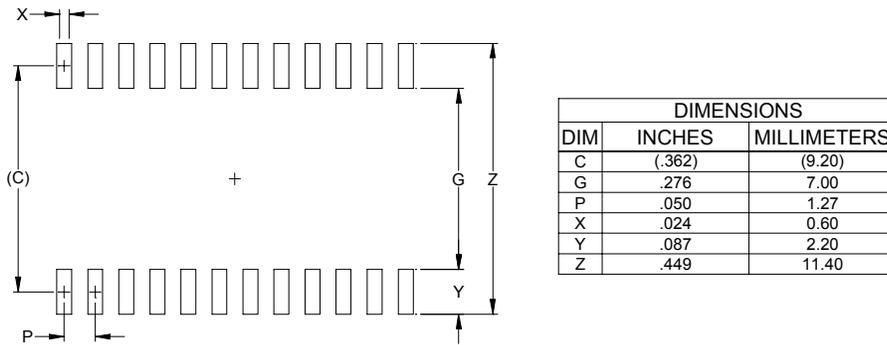
POWER MANAGEMENT

Outline Drawing - SO-24



- NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
 2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
 3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
 4. REFERENCE JEDEC STD MS-013, VARIATION AD.

Land Pattern - SO-24



- NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
 2. REFERENCE IPC-SM-782A, RLP NO. 307A.

Contact Information

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