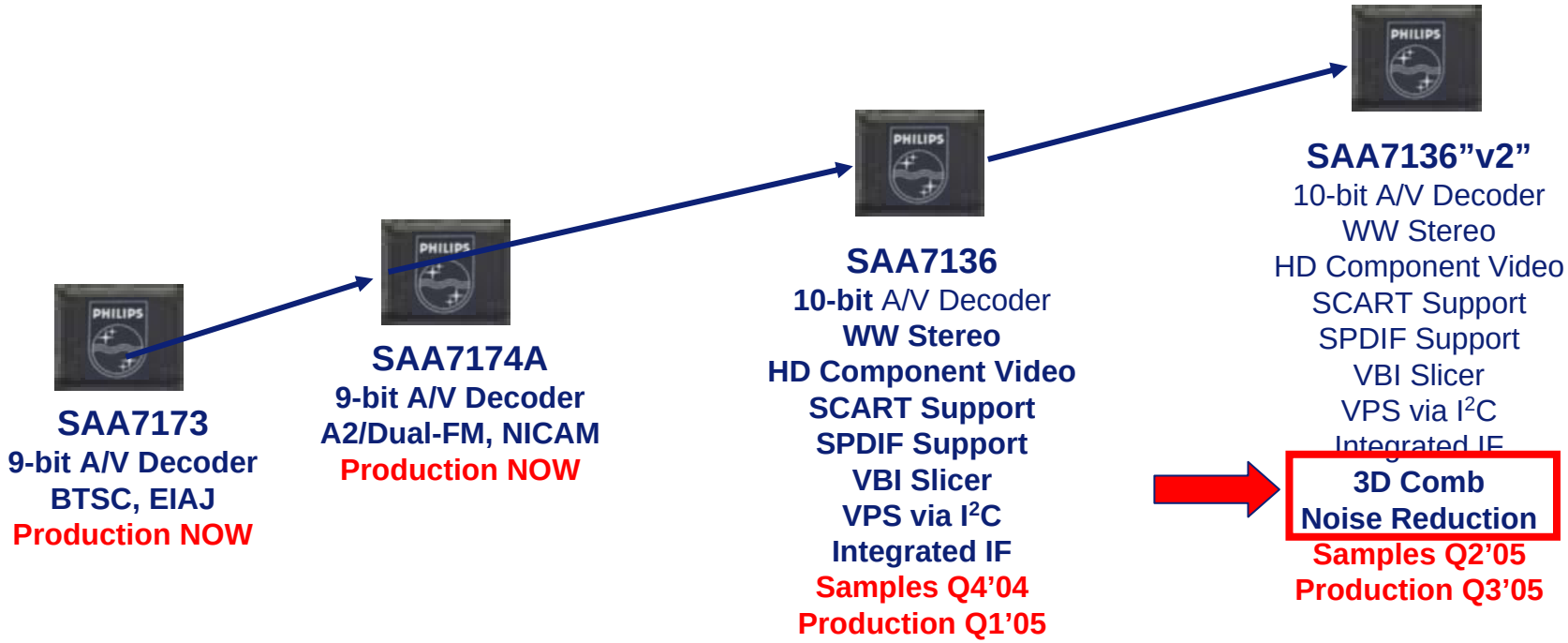
PHILIPS

Digital Video Decoder Solutions SAA7136

Business Line Display Processing
Digital Video Front Ends

September 2004

Philips Semiconductors
AV Decoder roadmap



SAA7136 Block diagram

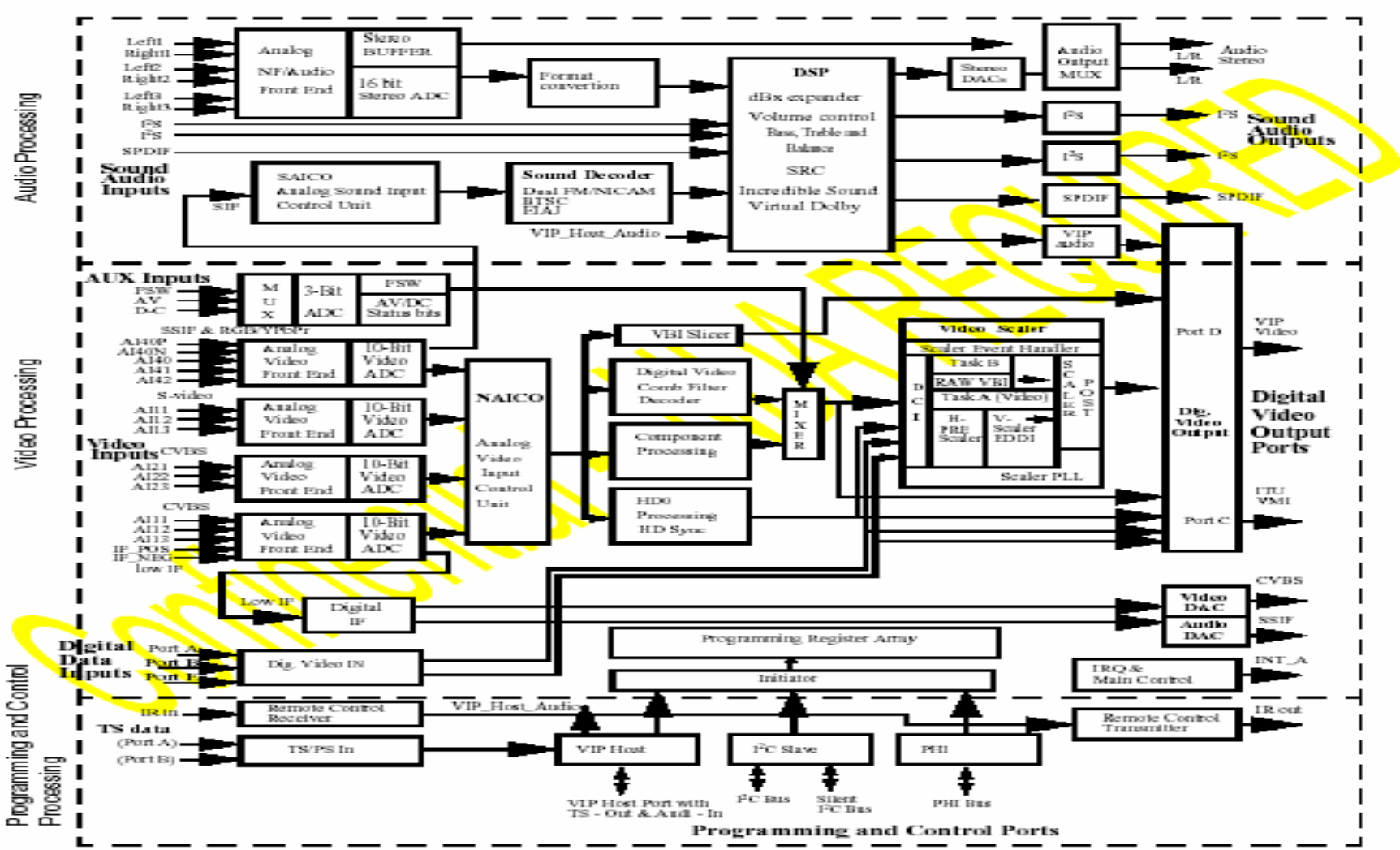


Fig.2 System Block Diagram of SAA7136

SAA7136 Analog Video Acquisition

- Fourteen analog inputs, allowing for multiple combinations of
  - CVBS
  - S-Video
  - RGB or Y-Pb-Br progressive or interlace able to handle standard definition signals as well as HD0
  - Low-IF from a Philips silicon tuner (TDA827x) or direct IF from Philips Can tuner (TD1316AL)
- RGB or Y-Pb-Br component input according to
  - 480i and 576i (Standard definition, interlaced)
  - 480p and 576 (HD0, double scan rate) at two-fold over sampling (54 MHz)
- Software controlled gain adjustment for RGB and Y-Pb-Br component inputs
- Four trilevel input pins for 2 fully equipped SCART applications
- Six trilevel input pins for 2 fully equipped D-Terminal applications
- Seamless Fast Blanking between CVBS input and synchronous RGB-SCART input
- Four video processing channels with automatic signal clamping and signal amplifying adjustment to a high quality 10 bit CMOS Analog-to-Digital converters results in a four-fold ITU 656 over sampled (54 MHz) video signal
- Automatic gain control (AGC) for the selected CVBS or S-Video channel, or manually adjustable gain for all video signal types
- Two buffered analog outputs providing CVBS / S-Video signal selected from any input
- Differential analog CVBS and SSIF (Second Sound IF) outputs from the integrated digital video IF demodulator
- Optional digitizing of VGA (640 x 480) computer graphics with H- and V- sync (supports only 60 Hz vertical sync)

SAA7136 Digital IF Demodulator

- Worldwide multi standard analog TV IF (Intermediate Frequency) demodulator (M/N, B/G/H, D/K, I, L/L')
- FM Radio pre-processing, internal selectivity for FM stereo application
- Especially adapted to the Philips low IF silicon tuner TDA817x without external SAW-filter
- Optional direct IF demodulation (IF at 38.9 MHz) possible (e.g. Philips TD 1316 AL)
- Alignment-free application
- Noise shaped IF AGC output signal
- Easy programming of IF processing by TV or FM Radio standard selection

SAA7136 Video signal processing & decoding

- Luminance and chrominance signal processing for
- – PAL BGDHIN, Combination-PAL N, PAL M, NTSC M, NTSC-Japan, NTSC 4.43, SECAM
- High performance super-adaptive NTSC/PAL comb filter for 2-dimensional chrominance/luminance separation for
- - increased Luminance and Chrominance Bandwidth for all NTSC- and PAL- standards
- - reduced cross color and cross luminance artifacts, even with critical colour pattern
- Automatic detection of any supported color standard
- High quality RGB and Y-Pb-Br component processing for standard TV and progressive TV
- Optional reduced resolution for Y-Pb-Br component processing of High Definition TV (1080i and 720p) sources
- Automatic detection of any supported video standard, including 480p, 576p, 720p and 1080i
- Automatic detection of signals from consumer grade sources (e.g.VTRs)
- Versatile Brightness-Contrast-Saturation (BCS) adjustment for CVBS/s-Video and RGB and Y-Pb-Br component processing
- Easy discrimination between CVBS and Y/C signals
- Digital PLL for synchronization and clock generation from all standards and non-standard video sources, e.g. consumer grade VTR
- Detection of copy protected input signals according to the Macrovision TM (1) standard, indicating level of protection, including progressive signals 480p and 576p
- On-chip line-locked clock generation according to
  - ITU601(standard definition) or SMPTE 293M /ITU-RBT.1358 (HD0)

SAA7136 Video scaler

- Horizontal and Vertical Down-Scaling and Up-Scaling to randomly sized windows
- Horizontal Up-Down Scaling
  - linear horizontal scaling ration down to 1/512 and up to 1024 limited by transfer data rates
  - horizontal INTERGER prescaler with N = 1 to 63, (range 1 to 1/128)
  - horizontal VPD (Variable Phase Delay) final scaler for down scale 1/7.999 to zoom up by factor 1024
- Vertical Up-Down Scaling
  - linear phase accurate vertical scaling ration down to 64 (6 in high quality) and up to 1024 limited by transfer data rates
  - two separate 4-tap programmable polyphase filters for luminance (Y) and chrominance (U or V) data streams optimized for STV and HDTV
  - edge guided 2-tap interpolation (EDGI) scale algorithm for areas with detected edges
  - edge detector controlled mixing of 4-tap polyphase interpolator results and EDGI results enabled a maximum of performance with a minimize scale artefacts
- Two separated tasks processing pipes for active video (task A) and raw vbi (task B) regions
- Linear zooming of free programmable picture fragment
- Programmable panorama scaling
- Versatile Brightness-Contrast-Saturation (BCS) adjustment for scaled video outputs
- Optional dynamic Contrast Improvement (DCI) via programmable look up table
- Optional intra-field de-interlacing (EDGI)
- Optional Colour Transient Improvement (CTI)
- Optional RGB matrix and a programmable gamma correction

SAA7136 Advanced signal processing

- Support for letter Box detection (Black Bar detection) via histogram evaluation
- Approximate noise level estimation of video input signal
- Status register and configurable status change output (interrupt) to minimise software overhead
- Support for RMS noise level estimation via histogram evaluation

SAA7136 Vertical Blanking Interval (VBI) slicing

- Versatile VBI-data slicer (slicer, clock regeneration and data byte synchronization) for all common text and data services
  - WST525/WST625, Gemstar2x R(1)& Gemstar1xR(2)/VPS, VITC525/VITC625, CC525/CC625, WSS 525 (CGMS)
  - WSS625, CGMS-A (line 41) of 480p (HD0), CGMS (line 41) of 576p (HD0), US NABTS/ Euro Teletext (FC), Moji
- Sliced VBI-data can be transferred as ANC data on the digital Video output ports (C or D) or on the parallel host port
- I2C read-back access to following VBI data standards
  - Close Caption (CC525 and CC625), CGMS (WSS525), WSS625, Gemstar1x and Gemstar2x, VPS
- Optionally, raw data with dedicated gain and offset adjustment is available for software decoding

SAA7136 Digital Video Interfaces

- A digital Video input port of 32 pins useable for maximum clock rates up to 75 MHz
  - two independent Standard TV (ITU 656, VMI) 8 or 10 Bit input streams
  - one Standard TV/HDTV 16 bit input stream and one TS (Transport stream)
  - one Standard TV/HDTV 20 bit input stream
  - one Standard TV/HDTV 24 bit (RGB) input stream
  - two TS and one STV (ITU 656) 8bit stream
- ·Select able Video input streaming standards
  - STV/HDTV video in ITU-656 representation, either 8 (10) or 16 (20) bit format Y-CB-CR 4:2:2
  - STV/HDTV video in VMI representation, either 8 (10) or 16 (20) bit format
  - optionally, STV/HDTV 24 Bit (RGB) input stream converted to YUV422 via internal programmable RGB/YUV Matrix
  - Parallel (8bit) and serial MPEG transport (TS) and program streams (PS), optional unstructured data.
- A digital Video output port of 25 pins useable for maximum clock rates up to 75 MHz
  - two independent Standard TV (ITU 656, VMI) 8 or 10 bit output streams
  - one Standard TV/HDTV 16 bit output stream
  - one Standard TV/HDTV 20 bit output stream
  - optionally, one Standard TV/HDTV 24 Bit (RGB) output stream
- Select able Video output streaming standards
  - STV/HDTV video in ITU-656 representation, either 8 (10) or 16 (20) bit format Y-CB-CR 4:2:2, optional with included
- sliced VBI data and/or Audio data
  - VIP 2.0 compatible video port including sound as ancillary data and VBI raw data
  - STV/HDTV video in VMI representation, either 8 (10) or 16 (20) bit format
  - optionally, STV/HDTV 24 bit (RGB) output stream via internal programmable YUV/RGB Matrix
- 1 serial input port for infrared transceivers supported RC5 and RC6 tansmission standards
- 1 serial output port for infrared transmitter adjustable to all common tansmission standards

SAA7136 Analog Audio acquisition

- Four inputs of analog SSIF (Second Sound IF)
  - One differential SSIF signal input connectable to internal dig. IF via simple post filter, or
  - One single ended SSIF signal inputs connectable to conventional tuners (TV and FM)
- Sound processing channels with automatic signal clamping and signal amplifying adjustment to a high quality 10 Bit
- CMOS Analog-to-Digital converter with 24.576 MHz sample frequency
- Three analog audio baseband inputs with two serial Sigma-Delta 16 bit High Resolution Audio ADC
- Two analog stereo baseband outputs with two Filter Stream Stereo D/A-converters
- Integrated analog audio pass-through (Support for analog audio loop back cable to sound card)

SAA7136 TV Sound Decoder

- All standards TV-stereo/mono-sound decoder:
  - BTSC, EIAJ, NICAM, FM A2, AM
  - dbx-TV Noise Reduction decoding for BTSC systems
- FM radio stereo decoding
- Automatic sound standard detection
- Automatic dematrixing (stereo, dual)

SAA7136 Digital Audio Interfaces

- Audio up streaming input via VIP Host port data bus
- Audio down streaming output as embedded ANC data into the VIP Video data stream (VIP video bus)
- One S/PDIF input and one 24bit S/PDIF output (according to IEC 60958-3, TTL compliant only) with 32, 44.1 or 48 kHz
- One direct pass-through from the S/PDIF input to VIP video port, e. g. for encoded audio data
- One direct pass-through from the VIP Host bus to the S/PDIF output, e. g. for encoded audio data
- Two I2S-bus inputs and two 24bit I2S-bus outputs for up to 4 channels with 32, 44.1 or 48 kHz
- Input of external audio reference clock of 256fs or 384 fs
- Output of audio output master clock (512 ´ fs, 256 ´ fs or 128 ´ fs selectable).
- Audio output sampling clock can be locked to video frame rate (constant number of audio samples per frame)

SAA7136 Audio feature processing

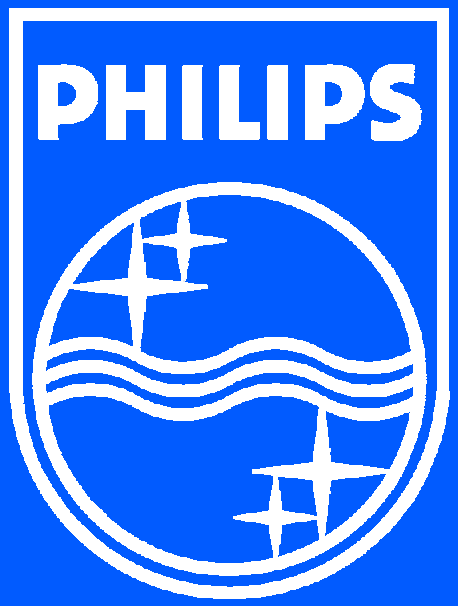
- Two stereo sample-rate converters (SRCs) from 32, 44.1 or 48 kHz to 32, 44.1 or 48 kHz
- Volume, balance, bass and treble control
- Incredible Mono, Incredible Stereo
- Dolby ProLogic
- Virtual Dolby Surround
- Automatic Volume Levelling (AVL)
- Optional generation of a frame locked audio master clock to support a constant number of audio clocks per video field

SAA7136 Programming Ports

- VIP 2.0 complaint host port
  - VIP slave support VIP 2 extensions
  - Support fast access to programming register (up to 50 MHz)
  - Supports standard 2-bit, 4 bit and 8 bit data interface
  - High speed FIFO downstream port for transport streams (48 Mbit/sec)
  - Medium speed FIFO up stream port for audio (2Mbit/sec)
  - Interrupt signal via INT_A output from up to 29 select able important internal signal processing statuses
- PHI, Parallel Host port Interface. Byte oriented programming interface for fast access of modern micro controller in future oriented PVR application.
  - Fast alternative to I2C based general control
  - Support fast access to programming register (up to 8 MHz)
  - Supports 8 bit data interface
  - Data read from VBI slicer (FIFO) for Teletext decoding
  - IRQ register support
- I2C Interface. It is the common way to program and control TV decoder inside of TV consumer application
  - support register access with 100 kHz and 400 kHz bit rate
  - I2C master useable via VIP and PHI port to program additional system devices like Tuner, MPEG Encoder and decoder
  - I2C slave, useable to support a programming interface for application systems with limiting controller performance
  - 2nd ‘silent’ I2C port to support noise sensitive devices

SAA7136 General features

- Only a single Crystal of 24.576MHz or 32.11MHz is required for all standards
- CMOS 3.3 V (input/output) and 1.8V (core) device; I2C pins and INT_A pin (interrupt enable flag) are 5V tolerant
- Software controlled power saving stand-by modes
- Boundary Scan Test circuit complies to the IEEE Std. 1149.b1 -1994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