Datasheet

SAA7115
CVIP2

PAL/NTSC/SECAM Video Decoder with Adaptive PAL/NTSC Comb Filter, High Performance Scaler, I2C Sliced Data Readback and SQ Pixel Output

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PHILIPS

CONTENTS

1 DOCUMENT INFO. . . . 6
1.1 Revision History . . . 6
2 FEATURES . . . 6
2.1 Video Acquisition . . . 6
2.2 Combfilter Video Decoder . . . 6
2.3 Video Scaler . . . 7
2.4 VBI Data Slicer . . . 7
2.5 Clock Generation . . . 8
2.6 General Features . . . 8
2.7 Summary SAA7114 versus SAA7115 . . . 9
3 GENERAL DESCRIPTION . . . 10
4 QUICK REFERENCE DATA . . . 11
5 ORDERING INFORMATION . . . 11
6 BLOCK DIAGRAM . . . 12
7 PINNING . . . 13
7.1 Pinning List and Pinning Diagram . . . 13
7.2 Pin Configurations . . . 19
7.3 SAA7115 Pin Strapping . . . 20
8 FUNCTIONAL DESCRIPTION . . . 21
8.1 Decoder . . . 21
8.1.1 Analog input processing . . . 21
8.1.1.1 Clamping . . . 23
8.1.1.2 Gain control . . . 23
8.1.2 Chrominance and luminance processing . . . 28
8.1.2.1 Chrominance path . . . 28
8.1.2.2 Luminance path . . . 32
8.1.2.3 Brightness Contrast Saturation (BCS) control and decoder output levels . . . 38
8.1.3 Synchronization . . . 39
8.1.4 Clock generation circuit . . . 39
8.1.5 Power-on reset and Chip Enable (CE) input . . . 41
8.2 Output Formatter . . . 43
8.3 Scaler . . . 49
8.3.1 Acquisition control and task handling (subaddresses 80H, 90H, 91H, 94H to 9FH and C4H to CFH) 50
8.3.1.1 Input field processing . . . 50
8.3.1.2 Task handling . . . 51
8.3.1.3 Output field processing . . . 52
8.3.2 Horizontal scaling . . . 55
8.3.2.1 Horizontal prescaler (subaddresses A0H to A7H and D0H to D7H) . . . 55
8.3.2.2 Horizontal fine scaling (variable phase delay filter; subaddresses A8H to AFH and D8H to DFH)60
8.3.3 Vertical scaling . . . 60
8.3.3.1 Line FIFO buffer (subaddresses 91H, B4H and C1H, E4H) . . . 60
8.3.3.2 Vertical scaler (subaddresses B0H to BFH and E0H to EFH) . . . 61
8.3.3.3 Use of the vertical phase offsets . . . 61
8.4 VBI-data decoder and capture (subaddresses 40H to 7FH) . . . 65
8.4.1 VBI Data Slicer . . . 65
8.4.2 I2C Readback of sliced VBI data . . . 67

8.4.3 Sliced VBI Data Output at the I-Port . . . 68
8.4.3.1 Euro WST, US WST and NABTS Data . . . 68
8.4.3.2 WSS 625 Data . . . 68
8.4.3.3 WSS 525 Data . . . 68
8.4.3.4 VPS Data . . . 68
8.4.3.5 Closed Caption . . . 68
8.4.3.6 Moji Data . . . 68
8.4.3.7 VITC Data . . . 69
8.4.3.8 Open Data Types . . . 69
8.5 Image port output interface (subaddresses 84H to 87H) . . . 70
8.5.1 Scaler output formatter (subaddresses 93H and C3H) . . . 71
8.5.2 Video FIFO (subaddress 86H) . . . 71
8.5.3 Text FIFO . . . 72
8.5.4 Video / text arbitration and Data packing (subaddress 86H) . . . 72
8.5.4.1 VBI insertion in SAV/EAV mode (bit SLDOM[3] = ‘1’) . . . 72
8.5.4.2 Data Packing (bit IMPAK (86H) and programming of the pulse generator via addr. F5H to FBH)73
8.5.5 Data stream coding and reference signal generation (subaddresses 84H, 85H and 93H) . . . 73
8.6 Scaler Backend clock generation (subaddresses 30H to 3FH) . . . 79
8.6.1 Square Pixel Clock Generation . . . 80
8.6.1.1 The second PLL (PLL2) . . . 80
8.7 Audio clock generation (subaddresses 30H to 3FH) . . . 82
8.7.1 Audio clock generation without analog PLL (CGC2) enhancement . . . 82
8.7.1.1 Master audio clock . . . 82
8.7.1.2 Signals ASCLK and ALRCLK . . . 83
8.7.2 Audio clock generation with analog PLL (CGC2) support . . . 84
8.7.3 Other control signals for audio clock generation . . . 89
9 INPUT/OUTPUT INTERFACES AND PORTS . . . 90
9.1 Analog terminals . . . 90
9.2 Audio clock signals . . . 90
9.3 Clock and real-time synchronization signals . . . 91
9.4 Video expansion port (X-port) . . . 92
9.4.1 X-port configured as output . . . 94
9.4.2 X-port configured as input . . . 96
9.5 Image port (I-port) . . . 96
9.6 Host port for 16-bit extension of video data I/O (H-port) . . . 98
9.7 Basic input and output timing diagrams I-port and X-port . . . 99
9.7.1 I-port output timing . . . 99
9.7.2 X-port input timing . . . 99
10 BOUNDARY SCAN TEST . . . 104
10.1 Initialization of boundary scan circuit . . . 104
10.2 Device identification codes . . . 104
11 LIMITING VALUES . . . 106
12 THERMAL CHARACTERISTICS . . . 106
13 CHARACTERISTICS . . . 107
14 APPLICATION INFORMATION . . . 114
15 DEVICE PROGRAMMING OVERVIEW . . . 116
15.1 I2C-bus description . . . 116
15.2 Register Overview . . . 117
16 DETAILED DESCRIPTION OF THE CONTROL REGISTERS . . . 127

16.1 Chip Version / Ident Register . . . 127
16.1.1 Chip Version . . . 127
16.1.2 Chip ID . . . 127
16.2 Programming Register Decoder . . . 128
16.2.1 Subaddress 01 Analog Input Control 0, Increment Delay . . . 128
16.2.2 Subaddress 02 Analog Input Control 1 . . . 129
16.2.3 Subaddress 03 Analog Input Control 2 . . . 132
16.2.4 Subaddress 04 Analog Input Control 3 . . . 133
16.2.5 Subaddress 05 Analog Input Control 4 . . . 133
16.2.6 Subaddress 06 Horizontal Sync Start . . . 133
16.2.7 Subaddress 07 Horizontal Sync Stop . . . 134
16.2.8 Subaddress 08 Sync Control . . . 135
16.2.9 Subaddress 09 Luminance control . . . 136
16.2.10 Subaddress 0A Decoder Brightness . . . 137
16.2.11 Subaddress 0B Decoder Contrast . . . 137
16.2.12 Subaddress 0C Decoder Saturation . . . 137
16.2.13 Subaddress 0D Chrominance Hue . . . 138
16.2.14 Subaddress 0E Chrominance Control 1 . . . 139
16.2.15 Subaddress 0F Chrominance Gain Control . . . 143
16.2.16 Subaddress 10 Chrominance/Luminance Control 2 . . . 144
16.2.17 Subaddress 11 Mode / Delay Control . . . 145
16.2.18 Subaddress 12 RTS0/1 Output Control . . . 146
16.2.19 Subaddress 13 and 1B RT / X-port Output Control . . . 148
16.2.20 Subaddress 14 Analog / ADC / Auto/ Compatibility Control . . . 149
16.2.21 Subaddress 15, 17VGATE Start . . . 151
16.2.22 Subaddress 16, 17 VGATE Stop . . . 151
16.2.23 Subaddress 17 Misc./VGATE-MSB's . . . 152
16.2.24 Subaddress 18 Raw data Gain Control . . . 153
16.2.25 Subaddress 19 Raw data Offset Control . . . 153
16.2.26 Subaddress 1A Color Killer Level Control . . . 154
16.2.27 Subaddress 1B Misc. Chroma Control . . . 154
16.2.28 Subaddress 1C Enhanced Combfilter Control 1 . . . 155
16.2.29 Subaddress 1D Enhanced Combfilter Control 2 . . . 156
16.2.30 Subaddresses 1E, 1F Status Bytes Video Decoder (read-only register) . . . 157
16.3 Programming Register Audio Clock Generation . . . 158
16.3.1 Subaddresses 30 to 32 AMCLK Cycles per Field . . . 158
16.3.2 Subaddresses 34 to 36 AMCLK Nominal Increment . . . 158
16.3.3 Subaddress 38 Ratio AMXCLK to ASCLK . . . 158
16.3.4 Subaddress 39 Ratio ASCLK to ALRCLK . . . 158
16.3.5 Subaddress 3A Audio Clock Control . . . 159
16.4 Programming Register VBI data slicer . . . 160
16.4.1 Subaddress 40 Basic Slicer Settings . . . 160
16.4.2 Subaddress 41 to 57 Line Control Register . . . 162
16.4.3 Subaddress 58 Programmable Framing Code . . . 162
16.4.4 Subaddress 59 Horizontal Offset . . . 163
16.4.5 Subaddress 5A Vertical Offset . . . 163
16.4.6 Subaddress 5B Field Offset, MSB's H/V-Offsets . . . 163
16.4.7 Subaddress 5D: SLDOM Codes . . . 165
16.4.8 Subaddress 5E SDID codes . . . 166
16.4.9 Subaddress 5E (read-only register) . . . 166
16.4.10 Subaddress 66 to 7F I2C Readback of decoded VBI Data (read-only register) . . . 167
16.4.10.1 Subaddress 66 to 6A I2C Readback of Closed Caption Data (CC525 and CC625) (read-only register)167
16.4.10.2 Subaddress 6B to 71 I2C Readback of Closed Caption Data (WSS525 and WSS625)

(read-only register)168
16.4.10.3 Subaddress 72 to 76 I2C Readback of Gemstar1x Data (read-only register) 169
16.4.10.4 Subaddress 77 to 7F I2C Readback of Gemstar2x Data (read-only register) 170
16.5 Programming Register - Interfaces and Scaler Part 171
16.5.1 Subaddress 80: Global Settings 171
16.5.2 Subaddress 83 to 87: Global Interface Configurations 173
16.5.3 Subaddress 88: Sleep and Power save control 180
16.5.4 Subaddress 8F (read-only register): status information scaler part 181
16.5.5 Subaddress 90: event handler control 181
16.5.6 Subaddress 91 to 93: scaler input and I-port output configuration 182
16.5.7 Subaddress 94 to 9B: Scaler Input Acquisition Window Definition 185
16.5.8 Subaddress 9C to 9F: Scaler Output Window Definition 187
16.5.9 Subaddress A0 to A2: Prescaling and FIR filtering 188
16.5.10 Subaddress A4 to A6: Brightness, Contrast and Saturation Control 190
16.5.11 Subaddress A8 to AE: Horizontal Phase Scaling 191
16.5.12 Subaddress B0 to BF: Vertical Scaling Control 192
16.6 Programming Register - second PLL (PLL2) and Pulse Generator 194
16.6.1 Subaddress F0 to F5 and FF: second PLL (PLL2) Programming Parameters 194
16.6.2 Subaddress F6 to FB: Pulse Generator Programming 198
17 PROGRAMMING START SET-UP 201
17.1 Decoder part 201
17.2 Audio clock generation part 206
17.3 Data slicer and data type control part 207
17.4 Scaler and interfaces 208
17.4.1 Examples 209
17.5 PLL2 and pulse generator control part 212
18 PACKAGE OUTLINE 214

1 DOCUMENT INFO

1.1 Revision History

VERSION NO	REVISION DATE	DESCRIPTION OF STATUS	BY
0.5	5 Oct 2001	Initial Version	H. Lambers
0.51	9 Oct 2001	Fixed LCBW recommended setting	H. Lambers
0.52	9 Oct 2001	VBSL setting changed, scaler and PLL2 examples , sect. 16.4 and 16.5 updated	A. Mittelberg
0.6	10 Oct 2001	Added application examples	H. Lambers
0.65	18 Oct 2001	Status at CQS	H. Lambers
0.66	19 Oct 2001	Minor updates	H. Lambers
0.67	23 Oct 2001	Fixed application example drawing	H. Lambers

2 FEATURES

2.1 Video Acquisition

- Six analog inputs, internal analog source selectors, (e.g.: 6x CVBS or(2 x YC and 2 CVBS) or (1 x YC and 4xCVBS)
- Two built in analog anti-alias filters
- Two improved 9 Bit CMOS analog-to-digital converter in differential CMOS style at two-fold ITU-656 oversampling (27MHz)
- Fully programmable static gain or automatic gain control (AGC) for the selected CVBS or Y/C channel
- Automatic Clamp Control (ACC) for CVBS, Y and C
- Switchable white Peak Control · Two 9-bit Video CMOS AD Converters, digitized CVBS or Y/C
- signals are available on the expansion port (X-port)
- Requires only one crystal (32.11 MHz or 24.576 MHz) for all standards
- Independent Gain and Offset - adjustment for raw data path

2.2 Combfilter Video Decoder

- Digital PLL for Synchronization and Clock Generation from all Standards and Non Standard Video Sources e.g. consumer grade VTR
- Automatic detection of 50/60Hz field frequency, and automatic recognition of all common broadcast standards
- Enhanced Horizontal and vertical Sync Detection
- Luminance and chrominance signal processing for
  - PAL BGDHIN,
  - Combination-PAL N,
  - PAL M,
  - NTSC M,
  - NTSC-Japan,
  - NTSC 4.43 and
  - SECAM (50 Hz / 60 Hz)
- PAL delay line for correcting PAL phase errors

- Improved 2/4-line comb filter for two dimensional chrominance/luminance-separation operating with adaptive combfilter parameters.
  - Increased Luminance and Chrominance Bandwidth for all PAL and NTSC-standards
  - Reduced cross colour and cross luminance artefacts
- Independent Brightness Contrast Saturation (BCS) - adjustment for decoder-part
- User programmable sharpness control
- Detection of Copy protected input signals:
  - according to Macrovision standard
  - indicating the level of protection
- Automatic TV/VCR detection
- 10 bit wide video output at combfilter video decoder
- X-port video output either as:
  - Noise shaped 8 bit ITU-656 video or
  - Full 10 bit ITU-656 interface (DC-performance 9 Bit)

2.3 Video Scaler

- Horizontal and Vertical Down-Scaling and Up-Scaling to randomly sized windows
- Horizontal and Vertical Scaling range: variable zoom to 1/64 (icon) (Note: H and V zoom are restricted by the transfer data rates)
- Vertical Scaling with Linear Phase Interpolation and Accumulating Filter for Anti-Aliasing (6 bit phase accuracy)
- Conversion to Square Pixel format
- Generation of a video output stream with improved synchronisation grid at the I-Port
- Two independent programming sets for scaler part, to define two "ranges" per field or sequences over frames
- Fieldwise switching between Decoder-part and Expansion port (X-port) input
- Brightness, contrast and saturation controls for scaled outputs

2.4 VBI Data Slicer

- Versatile VBI-data decoder, slicer, clock regeneration and byte synchronization, e.g. for:
  - WST525 / WST625 (CCST)
  - VPS
  - US / European Close Caption (CC),
  - WSS525 (CGMS), WSS625,
  - US NABTS
  - VITC 525 / VITC 625
  - GEMSTAR 1x
  - GEMSTAR 2x
  - Moji
- I^2C Readback of the following decoded data types:
  - US Close Caption (CC)
  - European Close Caption (CC)

- WSS525 (CGMS)
- WSS625 (CGMS)
- GEMSTAR 1x
- GEMSTAR 2x

2.5 Clock Generation

- On-Chip Line Locked Clock Generation according ITU601
- Generation of a frame locked Audio Master Clock to support a constant number of audio clocks per video field.
- Second onboard analog PLL to be used for:
  - On-Chip Line Locked Square Pixel Clock Generation for PAL and NTSC Square Pixel Video Output or
  - optionally Generation of a low jitter frame locked Audio Clock from the Audio Master Clock through reuse of the analog Square Pixel PLL. Supported audio clock frequencies are 256*fs, 384*fs and 512*fs (fs = 32 KHz, 44.1 KHz or 48 KHz).

2.6 General Features

- CMOS 3.3 V device with 5 V tolerant digital inputs and I/O ports
- Programming via serial I^2C-bus, full read-back ability by an external controller, bit rate up to 400 kbit/s
- Software controlled power saving stand-by modes
- Boundary Scan Test circuit complies to the IEEE Std. 1149.b1 -1994

2.7 Summary SAA7114 versus SAA7115

Table 1 SAA7114 versus SAA7115

ISSUE	SAA7114	SAA7115
Pin compatibility	reference pinning	pin-compatible to SAA7114
Analog Frontend	2 x 9 bit A/D- converters	2 x Low Noise 9 bit A/D- converters
	13.5 MHz CCIR sampling	27 MHz CCIR 2x-oversampling
	Standard White-Peak Control watching raw data	Standard White-Peak Control watching raw data plus baseband luminance data
Combfilter Decoder	4 lines adaptive comb filter	Improved 4 lines adaptive comb filter (reduced artifacts)
	Manual TV/VCR switching	Automatic TV/VCR detection
	Semi-automatic color standard detection	Fully-automatic color standard detection
	Regular SECAM 50 Hz	Regular SECAM 50 Hz and SECAM 60 Hz (Vietnam)
	Color overflow detection	Automatic color reducer (avoids color limitation with low burst)
	Safe lock for VCR feature modes	Extended safe lock for VCR feature modes
	Fast frame lock (ca. 2 fields)	Ultra-fast frame lock (almost 1 field)
Macrovision Detection	‘Pseudo Sync.’Macrovision Detection only	Comprehensive Macrovision Detection: - ‘Pseudo Sync.’ detection and/or - Split Burst detection (Type 2 / Type 3)
Scaled Video Output	Generation of embedded ITU-656 auxiliary codes at the I-Port video output	Generation of embedded ITU-656 auxiliary codes at the I-Port video output with improved synchronization raster for VCR signals
Clock Generation	Scaling to Square Pixel Data representation	Scaling to Square Pixel Data representation with extra integrated clock-PLL (PLL2, CGC2) to generate physical Square Pixel Clock signal of 29.5 MHz (PAL) or 24.5454 MHz (NTSC).
	Field- locked audio clock (constant number of clock cycles per field)	Frame- locked audio clock (constant number of clock cycles per frame), optionally through analog PLL (CGC2)
VBI Data Slicing and Output	Versatile VBI- data slicer	Versatile VBI- data slicer, incl. CGMS (Line 20 NTSC) and GemStar 2x (EPG)
	Output of sliced data embedded into I-Port output stream	Output of sliced data embedded into I-Port output stream and optionally per I2C register readback for CC, CGMS, Gemstar1x and Gemstar2x,

3 GENERAL DESCRIPTION

The SAA7115 is a video capture device for various applications ranging from small screen products like e.g. digital settop boxes, personal video recording applications to big screen devices like e.g. LCD projectors due to it's improved combfilter performance and 10 bit video output capabilities.

The SAA7115 is a combination of a two channel analog preprocessing circuit including Source-Selection, Anti-Aliasing Filter and A/D-converter, an Automatic Clamp and Gain Control, two Clock Generation Circuits (CGC1, CGC2), a Digital Multi Standard Decoder containing two-dimensional chrominance/luminance separation by an improved adaptive comb filter and a high performance scaler, including variable horizontal and vertical up and down scaling and a Brightness- Contrast- Saturation- Control circuit.

The decoder is based on the principle of line-locked clock decoding and is able to decode the colour of PAL, SECAM and NTSC signals into ITU-601 compatible colour component values. The SAA7115 accepts as analog inputs CVBS or S-Video (Y-C) from TV or VCR sources, including weak and distorted signals.

The expansion port (X-port) for digital video (bi-directional half duplex, D1 compatible) can be used either to output unscaled video using 10 bit or 8 bit dithered resolution or to connect to other external digital video sources for reuse of the SAA7115 scaler features.

The enhanced image port (I-port) of the 7115 supports 8 (16) bit wide output data with auxiliary reference data for interfacing to e.g. VGA controllers, settop box applications etc. It is also possible to output video in Square Pixel formats accompanied by a square pixel clock of the appropriate frequency.

In parallel SAA7115 incorporates also provisions for capturing the serially coded data in the vertical blanking interval (VBI-data) of several standards. Three basic options are available to transfer the VBI data to other devices:

- capturing raw video samples, after interpolation to the required output data rate, using the scaler and transferring the data to a device connected to the I-port,
- slicing the VBI data using the build in VBI data slicer (data recovery unit) and transferring the data to a device connected to the I-port
- slicing the VBI data using the build in VBI data slicer and reading out the sliced data via the I^2C bus (for several slow VBI data type standards only)

SAA7115 incorporates also a frame locked audio clock generation. This function ensures that there is always the same number of audio samples associated with a frame, or a set of fields. This prevents the loss of sychronisation between video and audio, during capture or playback. Furthermore the second analog onboard PLL optionally can be used to enhance this audio clock to a low jitter frame locked audio clock.

The SAA7115 is controlled via I^2C-bus (full write / read capability for all programming registers, bit rate up to 400 kbits/s)

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DDx}	digital supply voltage	3.0	3.3	3.6	V
V_{DDCx}	digital supply voltage range core	3.0	3.3	3.6	V
V_{DDA}	analog supply voltage range	3.1	3.3	3.5	V
T_{amb}	ambient temperature range	0	-	70	°C
P_{A+D}	analog and digital power consumption (1)	-	t.b.d.	-	W

1. Power consumption is measured in CVBS-input mode (only one ADC active) and 8 bit image port output mode, expansion port is tristated

5 ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7115	100	LQFP100	Plastic	SOT407-CD5

6 BLOCK DIAGRAM

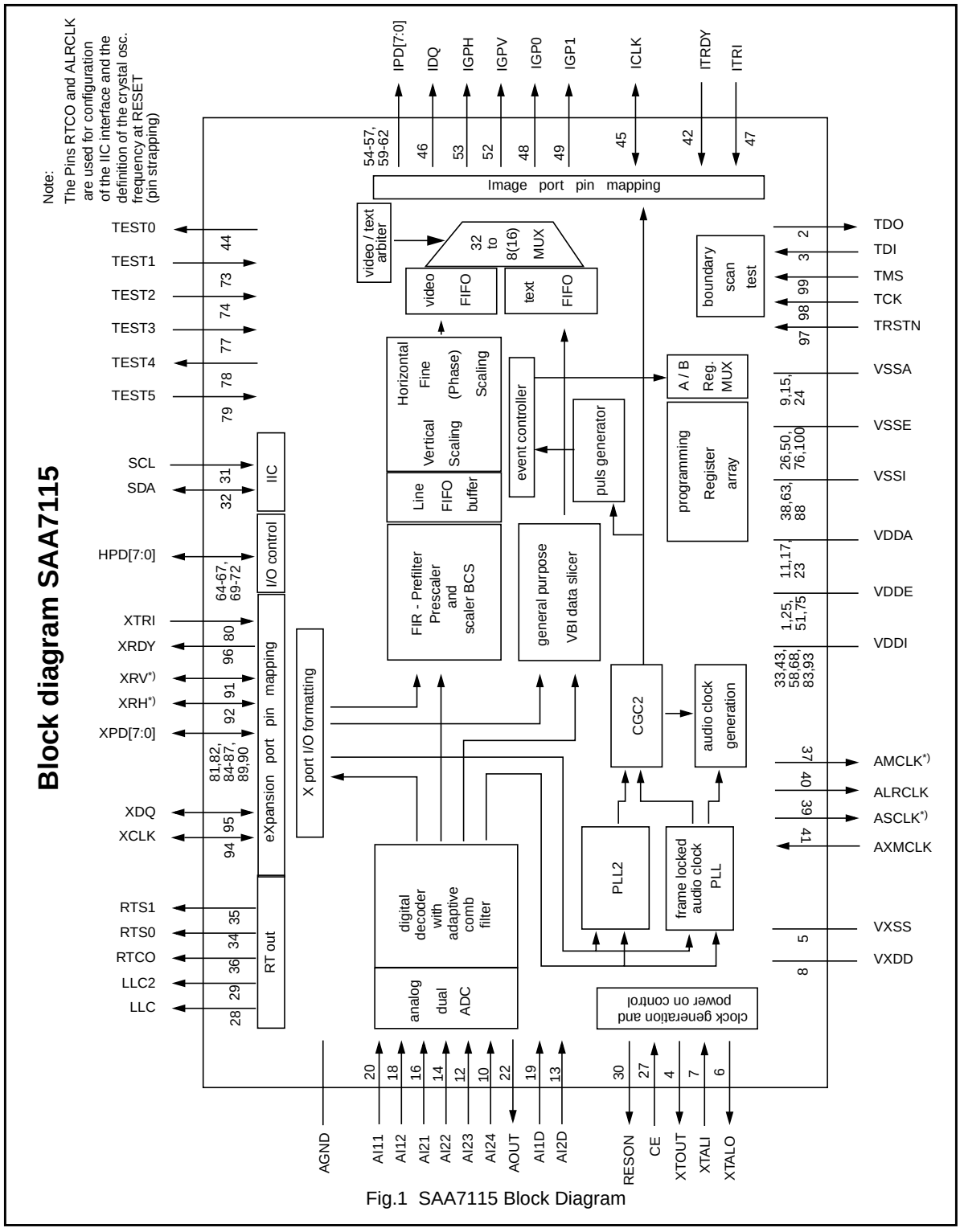


Fig.1 SAA7115 Block Diagram

7 PINNING

7.1 Pinning List and Pinning Diagram

Table 2 Pinning List SAA7115

SYMBOL	PIN	I/O/P	DESCRIPTION
V_{DDE}	1	P	digital supply voltage 3.3 V (external pad supply)
TDO	2	O	Test Data Output for Boundary Scan Test (2)
TDI	3	I	Test Data Input for Boundary Scan Test (with internal pull-up)(2)
XTOUT	4	O	crystal oscillator output signal, auxiliary signal
V_{XSS}	5	P	ground pin for crystal oscillator
XTALO	6	O	24.576 (32.11) MHz crystal oscillator output; not connected if XTALI is driven by an external single-ended oscillator.
XTALI	7	I	Input terminal for 24.576 (32.11) MHz crystal oscillator or connection of external oscillator with TTL compatible square wave clock signal.
V_{XDD}	8	P	supply voltage pin of crystal oscillator
V_{SSA2}	9	P	ground for analog inputs AI2x
AI24	10	I	analog input 24
V_{DDA2}	11	P	analog supply voltage for analog inputs AI2x (3.3V)
AI23	12	I	analog input 23
AI2D	13	I	differential input for ADC channel 2 (pins AI24, AI23, AI22, AI21)
AI22	14	I	analog input 22
V_{SSA1}	15	P	ground for analog inputs AI1x
AI21	16	I	analog input 21
V_{DDA1}	17	P	analog supply voltage for analog inputs AI1x (3.3V)
AI12	18	I	analog input 12
AI1D	19	I	differential input for ADC channel 1 (pins AI12, AI11)
AI11	20	I	analog input 11
AGND	21	P	analog ground connection
AOUT	22	O	Analog test output (do not connect)
V_{DDA0}	23	P	analog positive supply voltage for both internal CGC (Clock Generation Circuit) (3.3V)
V_{SSA0}	24	P	analog ground for internal CGC

SYMBOL	PIN	I/O/P	DESCRIPTION
V_{DDE}	25	P	digital supply voltage 3.3 V (external pad supply)
V_{SSE}	26	P	digital ground (external pad supply)
CE	27	I	Chip Enable or RESET input (with internal pull up)
LLC	28	O	line-locked system clock output (27 MHz nominal), for backward compatibility, do not use for new applications
LLC2	29	O	line locked clock/2 output (13.5 MHz nominal) for backward compatibility, do not use for new applications
RESON	30	O	RESet Output Not signal
SCL	31	I (/O)	IIC serial clock line (with inactive output path)
SDA	32	I/O	IIC serial data line
V_{DDI}	33	P	digital supply voltage 3.3 V internal core supply)
RTS0	34	O	real time status or sync information, controlled by subaddr. “11h and 12h”
RTS1	35	O	real time status or sync information, controlled by subaddr. “11h and 12h”
RTCO	36	(I/) O	Real Time Control Output: contains information about actual system clock frequency, field rate, odd/even sequence, decoder status, subcarrier phase and frequency and PAL sequence (according to RTC level 3.1, refer to external document “RTC Functional Specification” for details), can be strapped to supply via a 3.3 kOhm resistor to change the default IIC-wr-addresses from 42/43 (internal pull down) to 40/41.
AMCLK	37	O	audio master clock output
V_{SSI}	38	P	digital ground (internal core supply)
ASCLK	39	O	audio serial clock output
ALRCLK	40	(I/) O	audio left/right clock output, Can be strapped to supply via a 3.3 kOhm resistor indicate that the default 24.576 MHz crystal (internal pull down) has been replaced by a 32.11 MHz crystal.
AMXCLK	41	I	audio master external clock input (typing error corrected)
ITRDY	42	I	target ready input, image port (with internal pull up)
V_{DDI}	43	P	digital supply voltage 3.3 V (internal core supply)
TEST0	44	O	do not connect, reserved for future extensions and for **Testing:** scan output
ICLK	45	I/O	clock output signal for image-port, LCLK of LPB image port mode, or optional asynchron. backend clock input
IDQ	46	O	output data qualifier for image port *(optional: gated clock output)*

SYMBOL	PIN	I/O/P	DESCRIPTION
ITRI	47	I (/O)	image-port output control signal, effects all I-port pins incl. ICLK, enable and active polarity is under software control (bits IPE in subaddr. “87”) output path used for **Testing**: scan output
IGP0	48	O	general purpose output signal 0; image-port (controlled by subaddr. “84”,”85”)
IGP1	49	O	general purpose output signal 1; image-port (controlled by subaddr. “84”,”85”), same functions as IGP0
V_{SSE}	50	P	digital ground (external pad supply)
V_{DDE}	51	P	digital supply voltage 3.3 V (external pad supply)
IGPV	52	O	multi purpose vertical reference output signal; image-port (controlled by subaddr. “84”,”85”)
IGPH	53	O	multi purpose horizontal reference output signal; image-port (controlled by subaddr. “84”,”85”)
IPD7	54	O	image port data output
IPD6	55	O	
IPD5	56	O	
IPD4	57	O	
V_{DDI}	58	P	digital supply voltage 3.3 V (internal core supply)
IPD3	59	O	image port data output
IPD2	60	O	
IPD1	61	O	
IPD0	62	O	
V_{SSI}	63	P	digital ground (internal core supply)
HPD7	64	I/O	Host port data I/O, carries UV chrominance information in 16 bit video I/O modes
HPD6	65	I/O	
HPD5	66	I/O	
HPD4	67	I/O	
V_{DDI}	68	P	digital supply voltage 3.3 V (internal core supply)
HPD3	69	I/O	Host port data I/O, carries UV chrominance information in 16 bit video I/O modes
HPD2	70	I/O	
HPD1	71	I/O	
HPD0	72	I/O	
TEST1	73	I	do not connect, reserved for future extensions and for **Testing:** scan input

SYMBOL	PIN	I/O/P	DESCRIPTION
TEST2	74	I	do not connect, reserved for future extensions and for **Testing:** scan input
V_{DDE}	75	P	digital supply voltage 3.3 V (external pad supply)
V_{SSE}	76	P	digital ground (external pad supply)
TEST3	77	I	do not connect, reserved for future extensions and for **Testing:** scan input
TEST4	78	O	do not connect, reserved for future extensions and for **Testing:** scan output
TEST5	79	I	do not connect, reserved for future extensions and for **Testing:** scan input
XTRI	80	I	X-port output control signal, effects all X-port pins (XPD[7:0], XRH, XRV, XDQ and XCLK) enable and active polarity is under software control (bits XPE in subaddr. “83”)
XPD7 XPD6	81 82	I/O I/O	expansion-port data: In eight bit video output mode: these signal represent the video bits 7 to 6. In ten bit video output mode: these signal represent the video bits 9 to 8.
V_{DDI}	83	P	digital supply voltage 3.3 V (internal core supply)
XPD5 XPD4 XPD3 XPD2	84 85 86 87	I/O I/O I/O I/O	expansion-port data: In eight bit video output mode: these signal represent the video bits 5 to 2. In ten bit video output mode: these signal represent the video bits 7 to 4.
V_{SSI}	88	P	digital ground (internal core supply)
XPD1 XPD0	89 90	I/O I/O	expansion-port data: In eight bit video output mode: these signal represent the video bits 1 to 0. In ten bit video output mode: these signal represent the video bits 3 to 2.
XRV	91	I/O	vertical reference I/O expansion-port: In ten bit video output mode: this signal represents the video bit 0.
XRH	92	I/O	horizontal reference I/O expansion-port: In ten bit video output mode: this signal represents the video bit 1.
V_{DDI}	93	P	digital supply voltage 3.3 V (internal core supply)
XCLK	94	I/O	clock I/O expansion port
XDQ	95	I/O	data qualifier I/O expansion port
XRDY	96	O	task flag or read signal from scaler, controlled by XRQT (subaddr. 83H)
TRSTN	97	I	Test ReSeT Not for Boundary Scan Test (with internal pull-up); for board design without Boundary Scan connect TRSTN to ‘ground’(1)

SYMBOL	PIN	I/O/P	DESCRIPTION
TCK	98	I	Test Clock for Boundary Scan Test (with internal pull-up)(2)
TMS	99	I	Test Mode Select for Boundary Scan Test or Scan Test (with internal pull-up)(2)
V_{SSE}	100	P	digital ground (external pad supply)

Notes

1. This pin provides easy initialization of BST circuitry. TRSTN can be used to force the TAP (Test Access Port) controller to the Test-Logic-Reset state (normal operation) at once
2. According to the IEEE1149.b1-1994 standard the pads TDI and TMS are input pads with a internal pull-up transistor and TDO a tri-state output pad. TCK, TRSTN are also build with internal pull_up

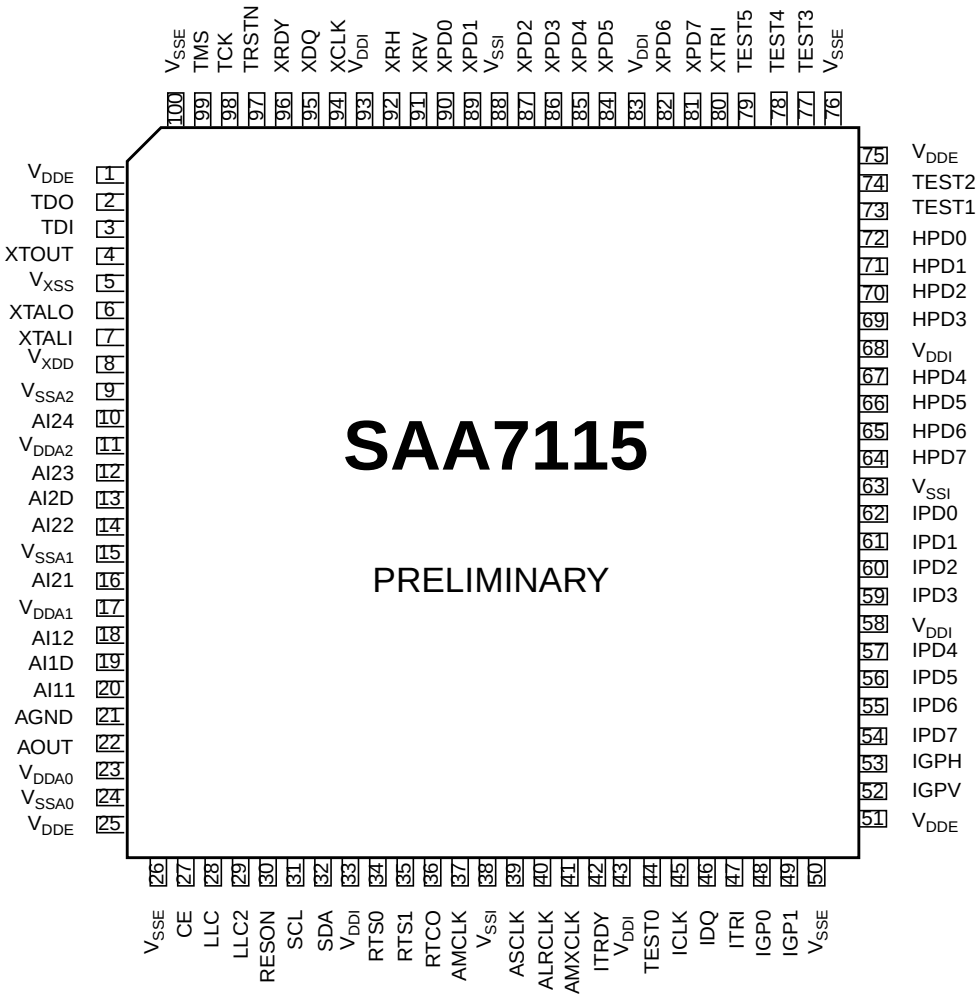


Fig.2 Pinning of the SAA7115

7.2 Pin Configurations

Table 3 Pin Configurations

pin no	pin name	8 bit input modes	16 bit input modes	alternative input functions	8 bit output modes	16 bit output modes	alternative output functions	I/O configuration prog. bits
81,82 84-87 89,90	XPD7...0	D1 data input	Y data input		D1 decoder output [7:0]			XCODE[92[3]] XPE[83[1:0]] + pin XTRI OFTS[1B[4], 13[2:0]]
					D1 decoder output [9:2] 10-bit mode			XCODE[92[3]] XPE[83[1:0]] + pin XTRI OFTS[1B[4], 13[2:0]]
94	XCLK	clock input		gated clock input	decoder clock output			XPE[83[1:0]} + pin XTRI XPCK[83[5:4]] XCKS[92[0]],
95	XDQ	data qualifier input			data quali-fier output (HREF &&VREF gate)			XDQ[92[1]] XPE[83[1:0]] + pin XTRI
96	XRDY	input ready output		active task A/B flag				XRQT[83[2]] XPE[83[1:0]] + pin XTRI
92	XRH	H-ref. input			decoder H-ref output			XDH[92[2]] XPE[83[1:0]] + pin XTRI
					D1 decoder output [1] 10-bit mode			XDH[92[2]] XPE[83[1:0]] + pin XTRI OFTS[1B[4], 13[2:0]]
80	XRV	V-ref. input			decoder V-ref output			XDV[92[5:4]] XPE[83[1:0]] + pin XTRI
					D1 decoder output [0] 10-bit mode			XDV[92[5:4]] XPE[83[1:0]] + pin XTRI OFTS[1B[4], 13[2:0]]
80	XTRI	output enable input						XPE[83[1:0]]
64-67 69-72	HPD7...0		UV data input			UV scaler output		ICODE[93[7]] ISWP[85[7:6]] ICKS[80[3:2]] IPE[87[1:0]] + pin ITRI
54-57 59-62	IPD7...0				D1 scaler output	Y scaler-output		ICODE[93[7]] ISWP[85[7:6]] ICKS[80[3:2]] IPE[87[1:0]] + pin ITRI
45	ICLK				clock output		clock input	ICKS[80[1:0]] IPE[87[1:0]] + pin ITRI ICKS[80[3:2]]
46	IDQ				data quali-fier output		gated clock out-put	ICKS[80[3:2]] IDQP[85[0]] IPE [87[1:0]] + pin ITRI
42	ITRDY				target ready input			

pin no	pin name	8 bit input modes	16 bit input modes	alternative input functions	8 bit output modes	16 bit output modes	alternative output functions	I/O configuration prog. bits
53	IGPH				H-gate out-put		extended H-gate, H- pulses	IDH[84[1:0]] IRHP[85[1]] IPE[87[1:0]] + pin ITRI
52	IGPV				V-gate output		V-sync, V-pulses	IDV[84[3:2]] IRVP[85[2]] IPE[87[1:0]] + pin ITRI
49	IGP1				general pur-pose			IDG1[86[5],84[7:6]] IG1P[85[4]] IPE [87[1:0]] + pin ITRI
48	IGP0				general pur-pose			IDG0[86[4],84[5:4]] IG0P[85[3]] IPE[87[1:0]] + pin ITRI
47	ITRI				output ena-ble input			

7.3 SAA7115 Pin Strapping

Table 4 SAA7115 Pin Strapping

pin no	pin name	function
36	RTCO	operates as IICSA pin, “0” = SA 42/43 hex (default), “1” = SA 40/41 hex
40	ALRCLK	0 = 24.576 MHz crystal (default) 1 = 32.110 MHz crystal

Note

1. Pin strapping is done by connecting the pin to supply via a 4.7 kOhm resistor. During the power up reset sequence the corresponding pins are switched to input-mode to read the strapping level. For the default setting no strapping resistor is necessary (internal pull down)

8 FUNCTIONAL DESCRIPTION

8.1 Decoder

8.1.1 ANALOG INPUT PROCESSING

The SAA7115 offers six analog signal inputs, two analog main channels with source switch, clamp circuit, analog amplifier, anti-alias filter and video 9-bit CMOS ADC with a Decimation Filter (DF); see Figs 4 and 7.

The anti-alias filters are adapted to the line-locked clock frequency via a filter control circuit. The characteristic is shown in Fig.3. During the vertical blanking period gain and clamping control are frozen.

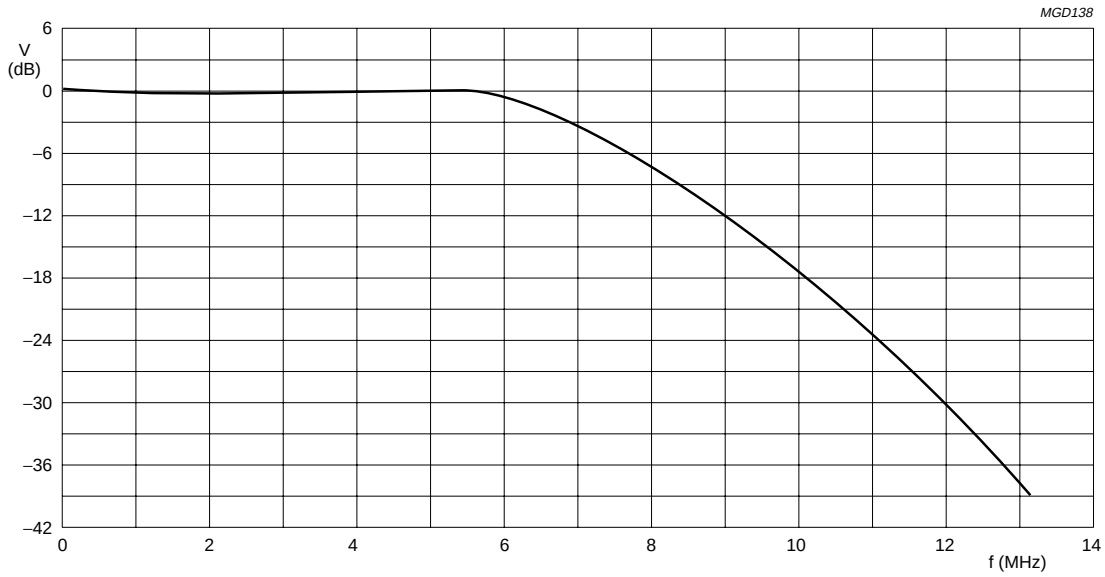


Fig.3 Anti-alias filter.

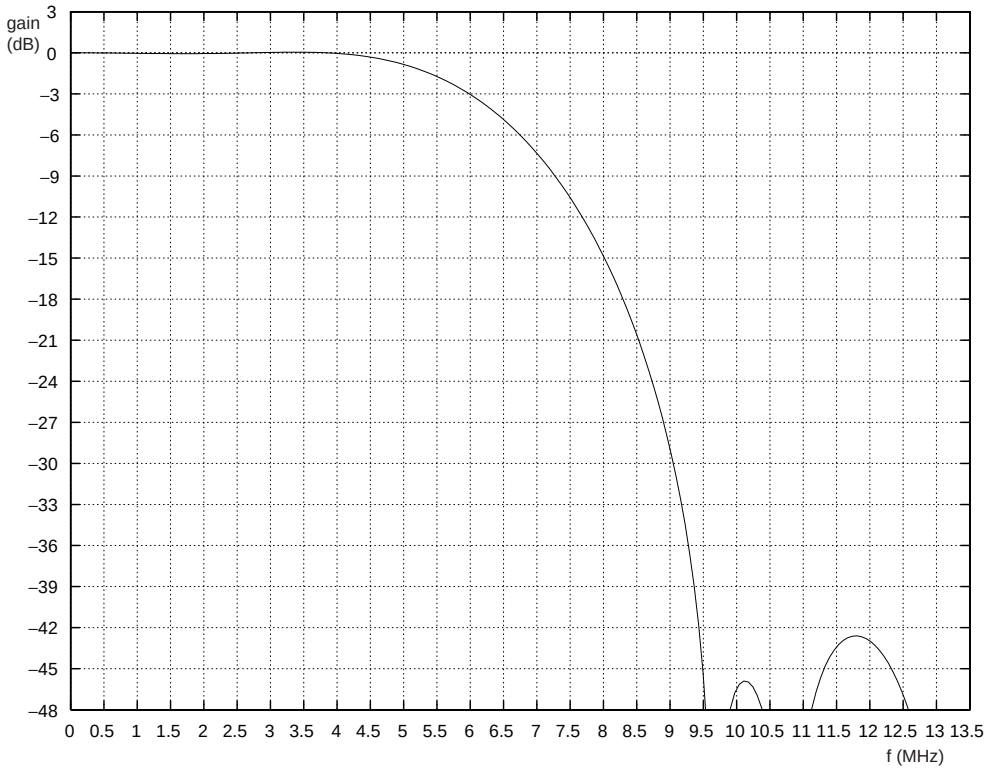


Fig.4 Decimation filter.

8.1.1.1 Clamping

The clamp control circuit controls the correct clamping of the analog input signals. The coupling capacitor is also used to store and filter the clamping voltage. An internal digital clamp comparator generates the information with respect to clamp-up or clamp-down. The clamping levels for the two ADC channels are fixed for luminance (120), chrominance (256) and for component inputs as component Y (32), components P_B and P_R (256). The clamping time is defined by the internally generated HCL pulse on the back porch of the video signal.

8.1.1.2 Gain control

The gain control circuit receives (via the I^2C-bus) the static gain levels for the two analog amplifiers or controls one of these amplifiers automatically via a built-in Automatic Gain Control (AGC) as part of the Analog Input Control (AICO).

The AGC (automatic gain control for luminance) is used to amplify a CVBS or Y signal to the required signal amplitude, matched to the ADCs input voltage range. The AGC active time is the sync bottom of the video signal and is defined by the internally generated HSY pulse.

Signal (white) peak control limits the gain at signal overshoots. The flow charts (see Figs 8 and 9) show more details of the AGC. The influence of supply voltage variation within the specified range is automatically eliminated by clamp and automatic gain control.

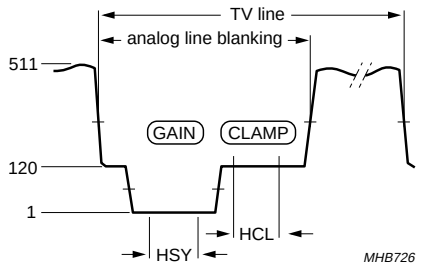


Fig.5 Analog line with clamp (HCL) and gain range (HSY).

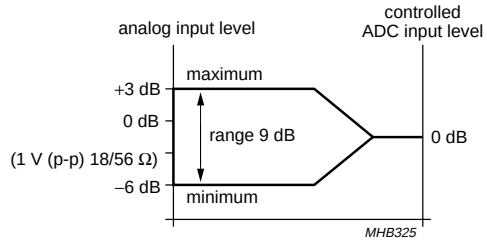


Fig.6 Automatic gain range.

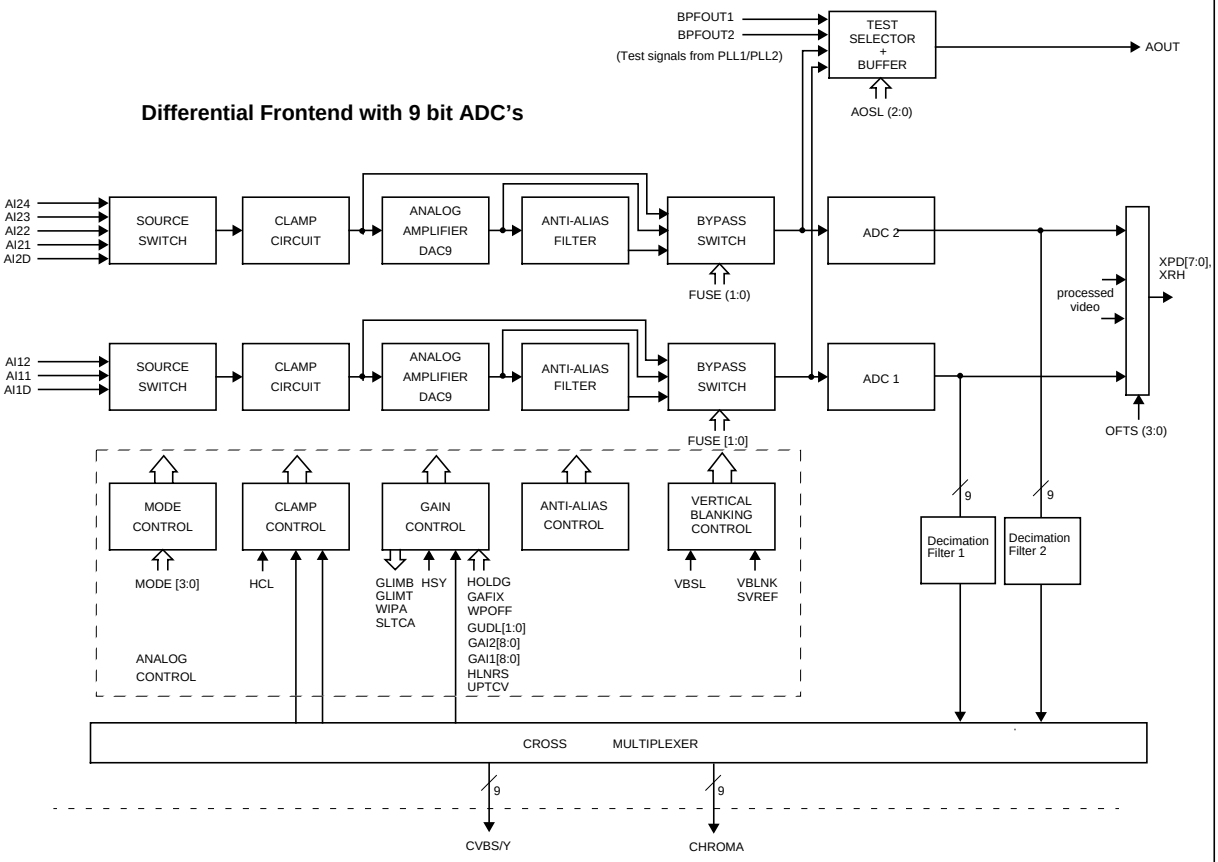
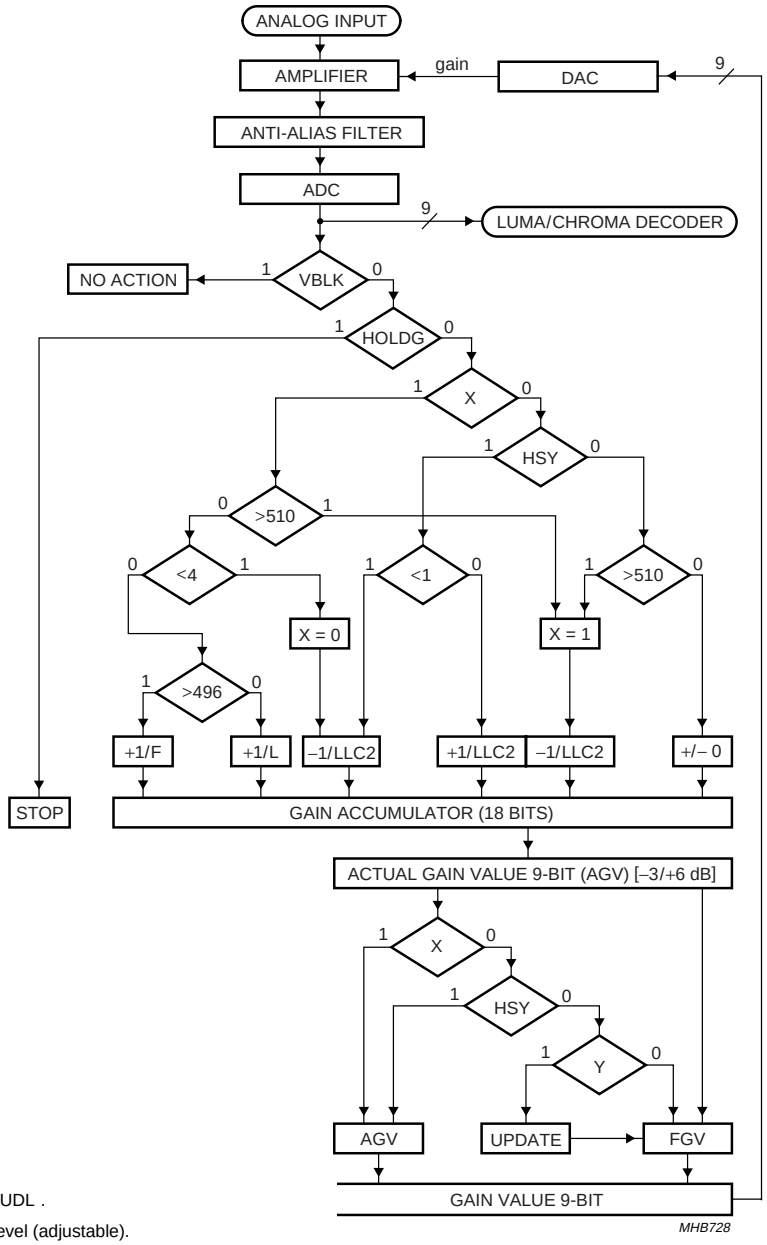


Fig.7 Analog input processing using the SAA7115 as differential front-end with 9-bit ADC.



X = system variable.

$Y = |AGV - FGV| > GUDL$.

GUDL = gain update level (adjustable).

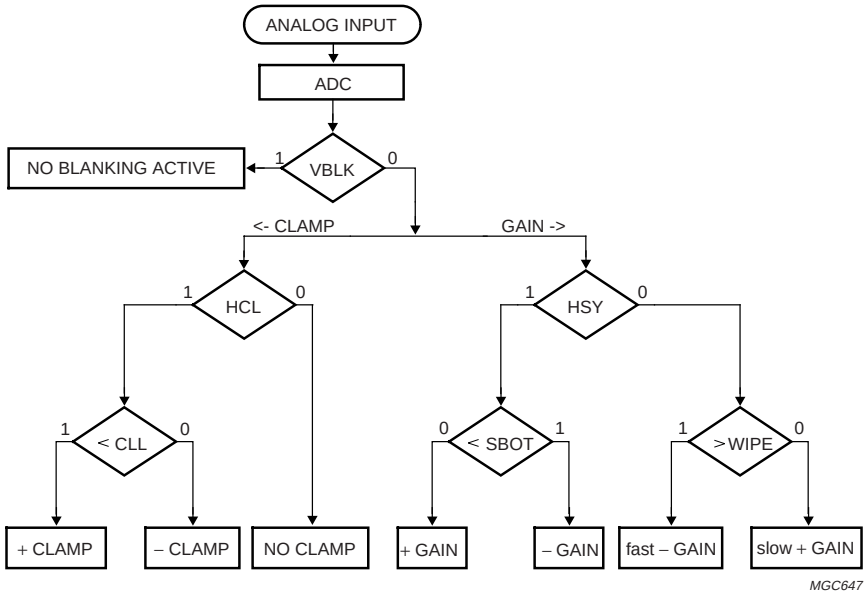
VBLK = vertical blanking pulse.

HSY = horizontal sync pulse.

AGV = actual gain value.

FGV = frozen gain value.

Fig.8 Gain flow chart.



WIPE = white peak level (510).
SBOT = sync bottom level (1).
CLL = clamp level [120 for CVBS, Y(C), S; 256 for C(Y), P_B-P_R; 32 for RGB, Y].
HSY = horizontal sync pulse.
HCL = horizontal clamp pulse.

Fig.9 Clamp and gain flow chart.

8.1.2 CHROMINANCE AND LUMINANCE PROCESSING

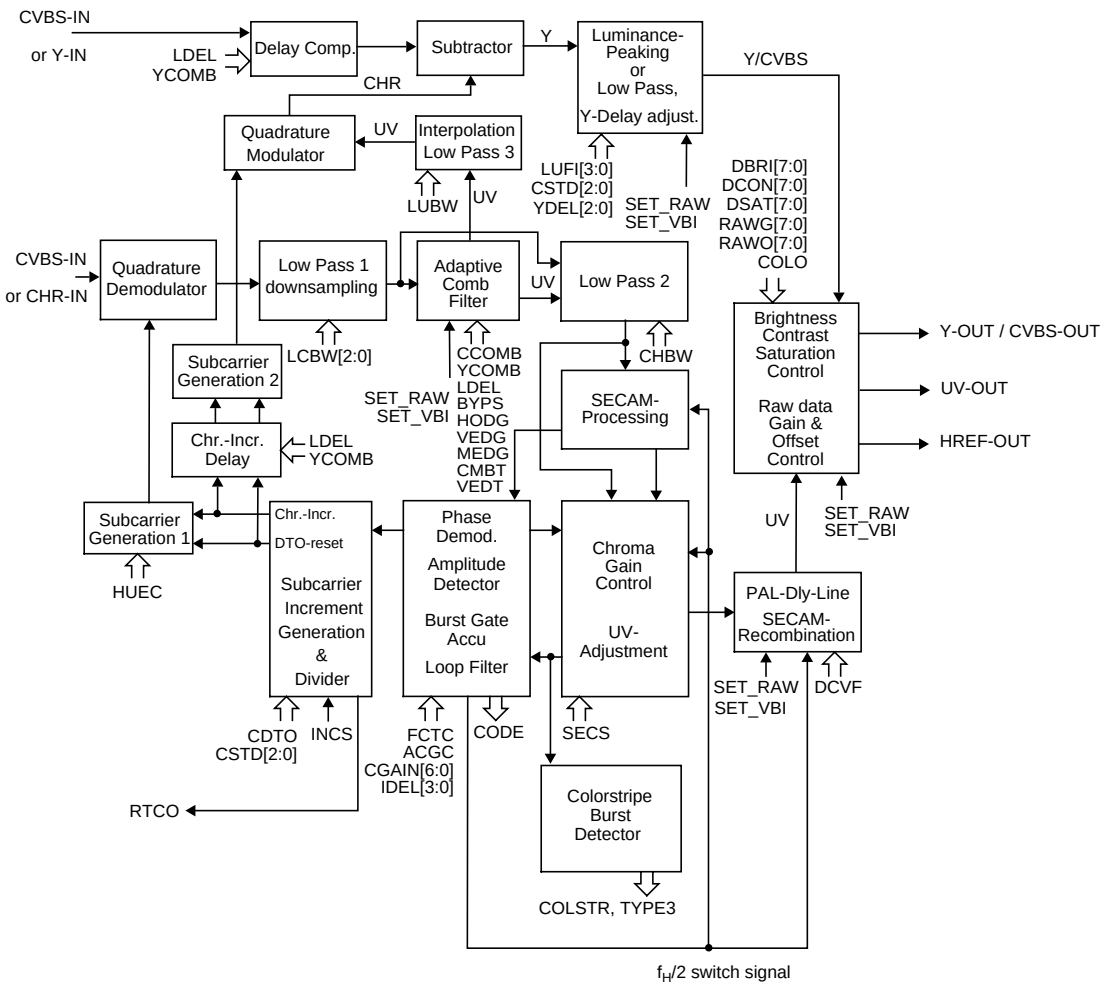


Fig.10 Chrominance and luminance processing.

8.1.2.1 Chrominance path

The 9-bit CVBS or chrominance input signal is fed to the input of a quadrature demodulator, where it is multiplied by two time-multiplexed subcarrier signals from the subcarrier generation block 1 (0° and 90° phase relationship to the demodulator axis). The frequency is dependent on the chosen colour standard.

The time-multiplexed output signals of the multipliers are low-pass filtered (low-pass 1). Eight characteristics are programmable via LCWB3 to LCWB0 to achieve the desired bandwidth for the colour difference signals (PAL, NTSC) or the 0° and 90° FM signals (SECAM).

The chrominance low-pass 1 characteristic also influences the grade of cross-luminance reduction during horizontal colour transients (large chrominance bandwidth means strong suppression of cross-luminance). If the Y-comb filter is disabled by YCOMB = 0 the filter influences directly the width of the chrominance notch within the luminance path (a large chrominance bandwidth means wide chrominance notch resulting in a lower luminance bandwidth).

The low-pass filtered signals are fed to the adaptive comb filter block. The chrominance components are separated from the luminance via a two line vertical stage (four lines for PAL standards) and a decision logic and mixing stage between the filtered and the non-filtered output signals. The decision logic can be fine adjusted by the control signals HODG, VEDG, MEDG, VEDT and CMBT. This block is bypassed for SECAM signals. The comb filter logic can be enabled independently for the succeeding luminance and chrominance processing by YCOMB (subaddress 09H, bit 6) and/or CCOMB (subaddress 0EH, bit 0). It is always bypassed during VBI or raw data lines programmable by the LCRn registers (subaddresses 41H to 57H); see Section 8.4.

The separated C_B-C_R components are further processed by a second filter stage (low-pass 2) to modify the chrominance bandwidth without influencing the luminance path. It's characteristic is controlled by CHBW (subaddress 10H, bit 3). For the complete transfer characteristic of low-passes 1 and 2 see Figs 11 and 12.

The SECAM processing (bypassed for QAM standards) contains the following blocks:

- Baseband 'bell' filters to reconstruct the amplitude and phase equalized 0° and 90° FM signals
- Phase demodulator and differentiator (FM-demodulation)
- De-emphasis filter to compensate the pre-emphasized input signal, including frequency offset compensation (DB or DR white carrier values are subtracted from the signal, controlled by the SECAM switch signal).

The succeeding chrominance gain control block amplifies or attenuates the C_B-C_R signal according to the required ITU 601/656 levels. It is controlled by the output signal from the amplitude detection circuit within the burst processing block.

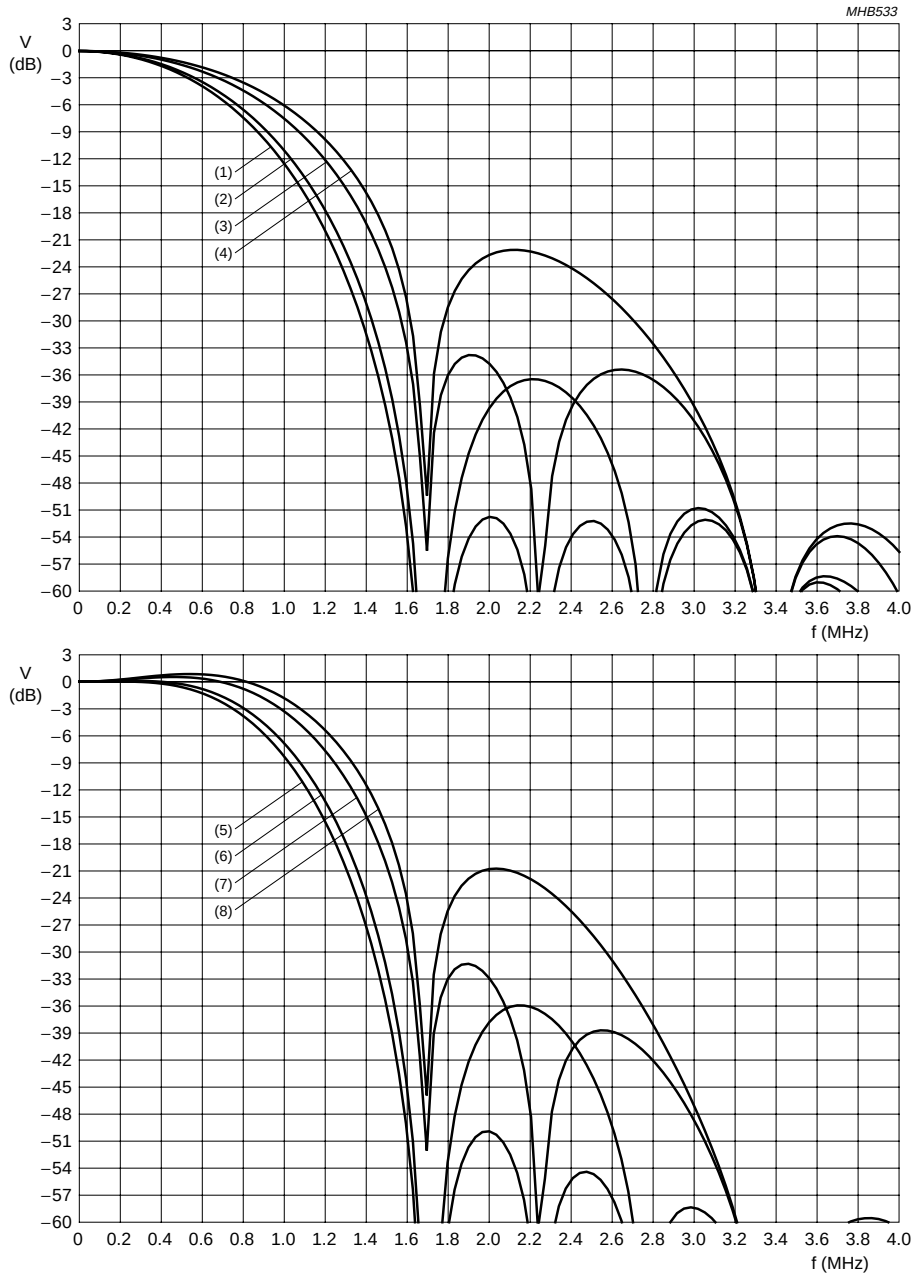
The burst processing block provides the feedback loop of the chrominance PLL and contains the following:

- Burst gate accumulator
- Colour identification and colour killer
- Comparison nominal/actual burst amplitude (PAL/NTSC standards only)
- Loop filter chrominance gain control (PAL/NTSC standards only)
- Loop filter chrominance PLL (only active for PAL/NTSC standards)
- PAL/SECAM sequence detection, H/2-switch generation.

The increment generation circuit produces the Discrete Time Oscillator (DTO) increment for both subcarrier generation blocks. It contains a division by the increment of the line-locked clock generator to create a stable phase-locked sine signal under all conditions (e.g. for non-standard signals).

The PAL delay line block eliminates crosstalk between the chrominance channels in accordance with the PAL standard requirements. For NTSC colour standards the delay line can be used as an additional vertical filter. If desired, it can be switched off by DCVF = 1. It is always disabled during VBI or raw data lines programmable by the LCRn registers (subaddresses 41H to 57H); see Section 8.4. The embedded line delay is also used for SECAM recombination (cross-over switches).

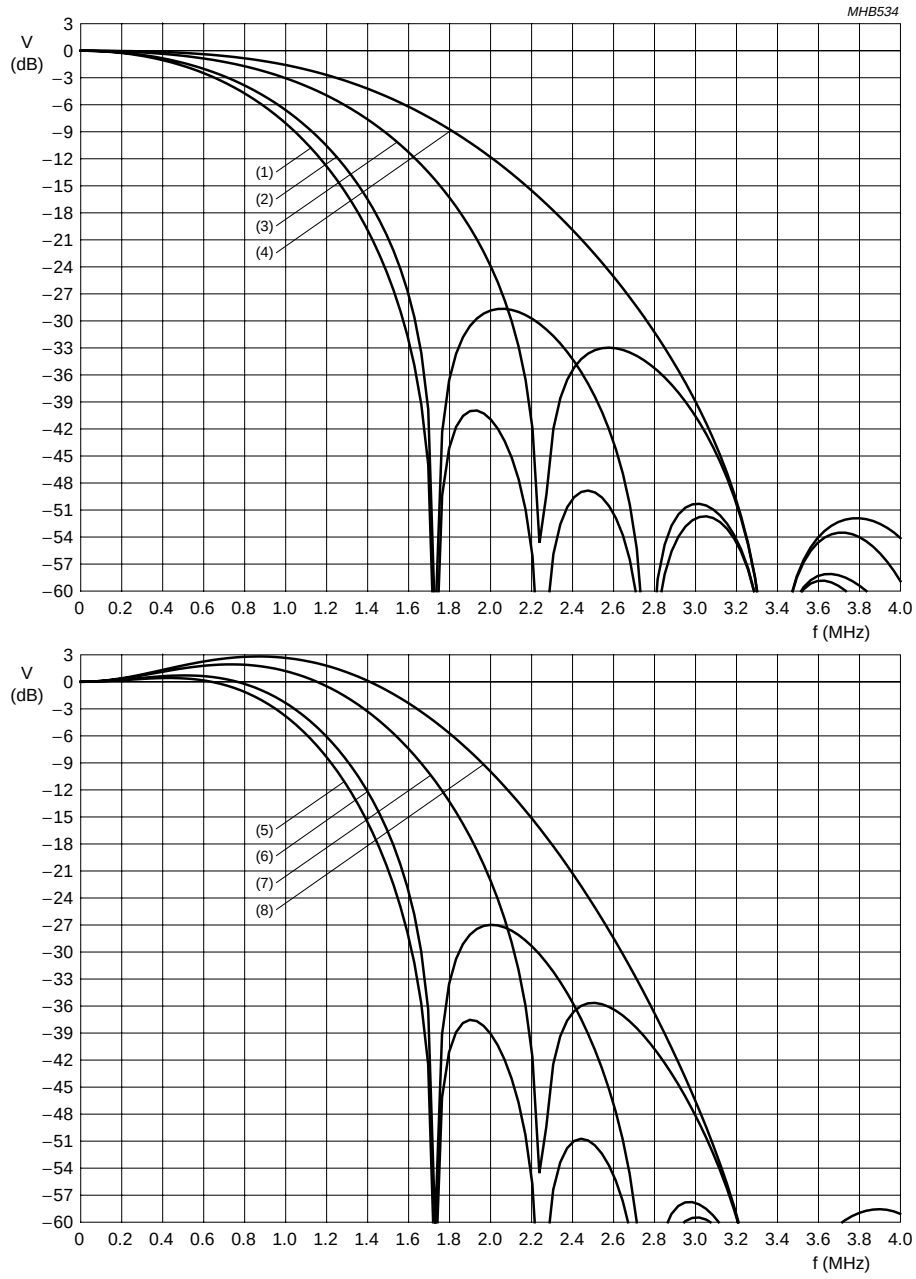
The colorstripe burst detector detects partly or fully phase inverted burst according to the Macrovision standard. The protection level is reported by the status flags COLSTR and TYPE3.



(1) LCBW[2:0] = 000.
(2) LCBW[2:0] = 010.
(3) LCBW[2:0] = 100.
(4) LCBW[2:0] = 110.

(5) LCBW[2:0] = 001.
(6) LCBW[2:0] = 011.
(7) LCBW[2:0] = 101.
(8) LCBW[2:0] = 111.

Fig.11 Transfer characteristics of the chrominance low-pass at CHBW = 0.



(1) LCBW[2:0] = 000.
(2) LCBW[2:0] = 010.
(3) LCBW[2:0] = 100.
(4) LCBW[2:0] = 110.

(5) LCBW[2:0] = 001.
(6) LCBW[2:0] = 011.
(7) LCBW[2:0] = 101.
(8) LCBW[2:0] = 111.

Fig.12 Transfer characteristics of the chrominance low-pass at CHBW = 1.

8.1.2.2 Luminance path

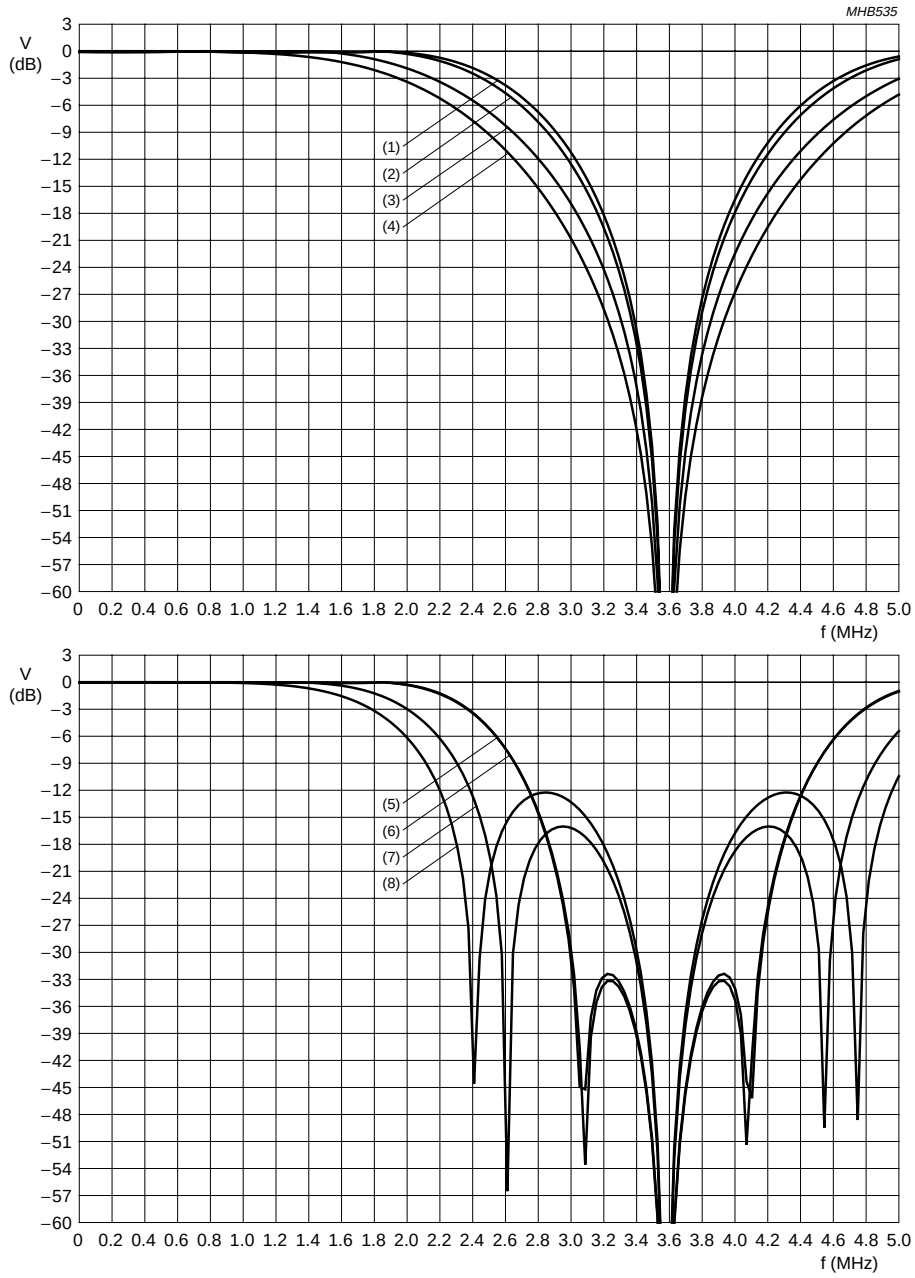
The rejection of the chrominance components within the 9-bit CVBS or Y input signal is achieved by subtracting the remodulated chrominance signal from the CVBS input.

The comb filtered C_B-C_R components are interpolated (upsampled) by the low-pass 3 block. It's characteristic is controlled by LUBW (subaddress 09H, bit 4) to modify the width of the chrominance 'notch' without influencing the chrominance path. The programmable frequency characteristics available, in conjunction with the LCBW2 to LCBW0 settings, can be seen in Figs 13 to 16. It should be noted that these frequency curves are only valid for Y-comb disabled filter mode (YCOMB = 0). In comb filter mode the frequency response is flat. The centre frequency of the notch is automatically adapted to the chosen colour standard.

The interpolated C_B-C_R samples are multiplied by two time-multiplexed subcarrier signals from the subcarrier generation block 2. This second DTO is locked to the first subcarrier generator by an increment delay circuit matched to the processing delay, which is different for PAL and NTSC standards according to the chosen comb filter algorithm. The two modulated signals are finally added to build the remodulated chrominance signal.

The frequency characteristic of the separated luminance signal can be further modified by the succeeding luminance filter block. It can be configured as peaking (resolution enhancement) or low-pass block by LUFI3 to LUFI0 (subaddress 09H, bits 3 to 0). The 16 resulting frequency characteristics can be seen in Fig.17. The LUFI3 to LUFI0 settings can be used as a user programmable sharpness control.

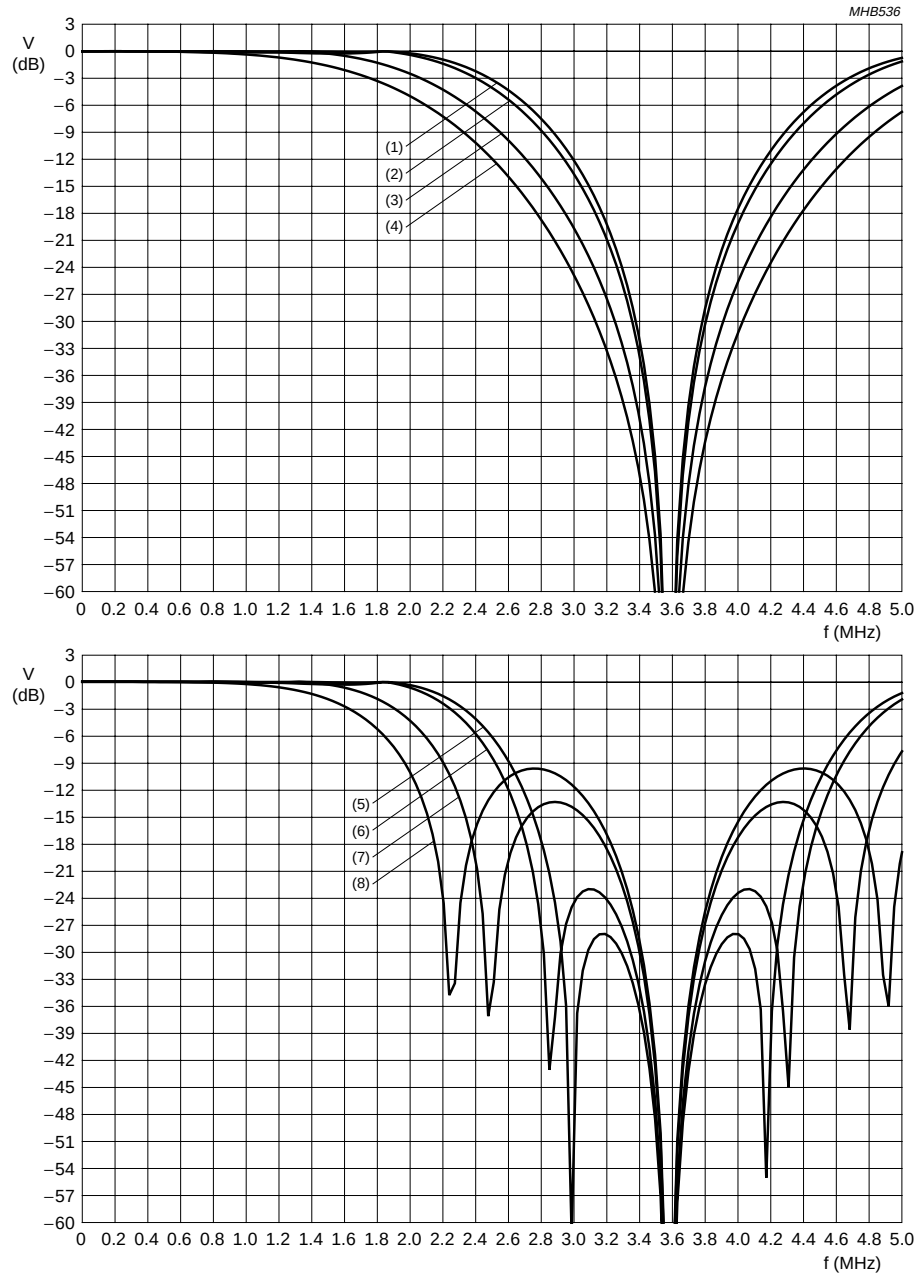
The luminance filter block also contains the adjustable Y-delay part; programmable by YDEL2 to YDEL0 (subaddress 11H, bits 2 to 0).



(1) LCBW[2:0] = 000.
(2) LCBW[2:0] = 010.
(3) LCBW[2:0] = 100.
(4) LCBW[2:0] = 110.

(5) LCBW[2:0] = 001.
(6) LCBW[2:0] = 011.
(7) LCBW[2:0] = 101.
(8) LCBW[2:0] = 111.

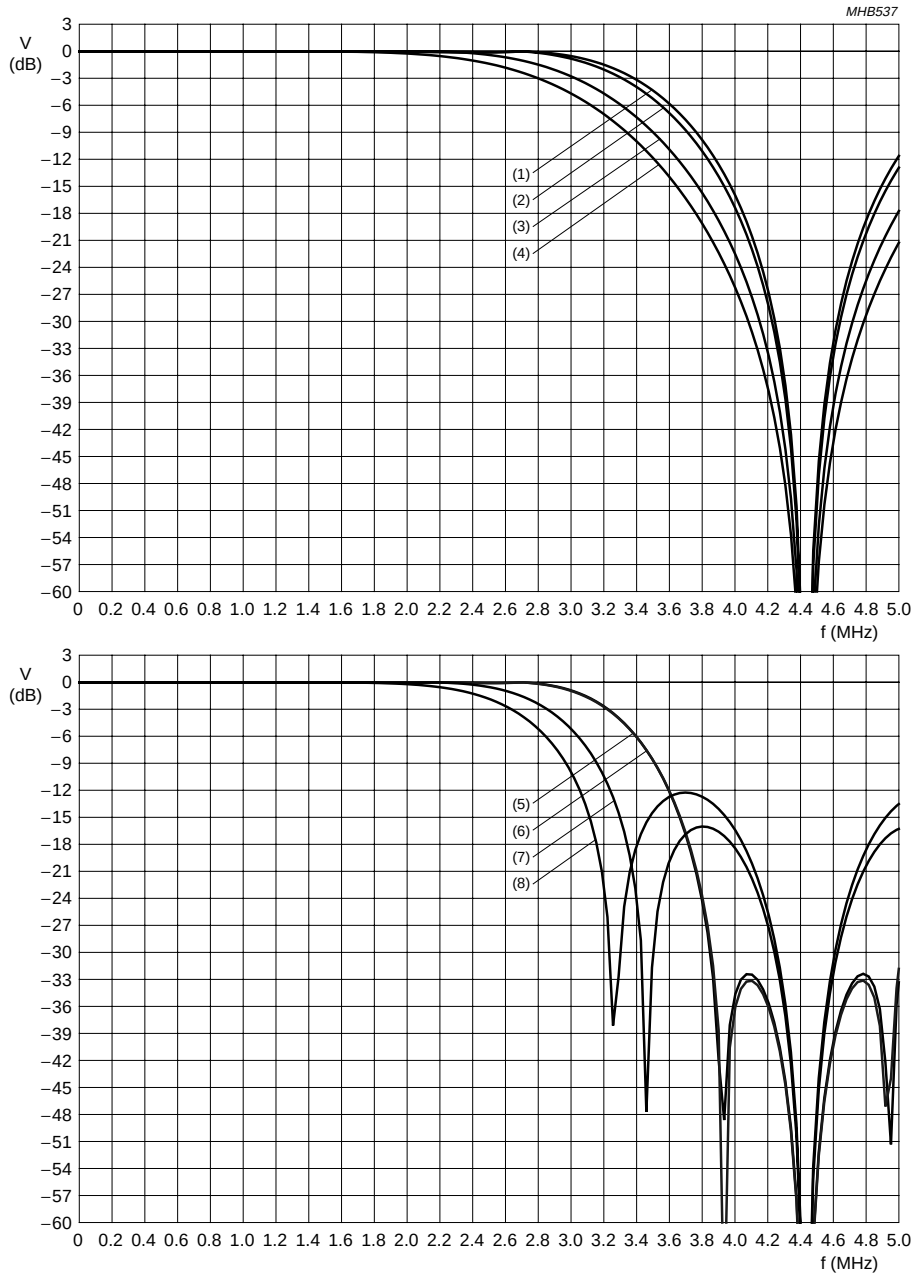
Fig.13 Transfer characteristics of the luminance notch filter in 3.58 MHz mode (Y-comb filter disabled) at LUBW = 0.



(1) LCBW[2:0] = 000
(2) LCBW[2:0] = 010
(3) LCBW[2:0] = 100
(4) LCBW[2:0] = 110

(5) LCBW[2:0] = 001
(6) LCBW[2:0] = 011
(7) LCBW[2:0] = 101
(8) LCBW[2:0] = 111

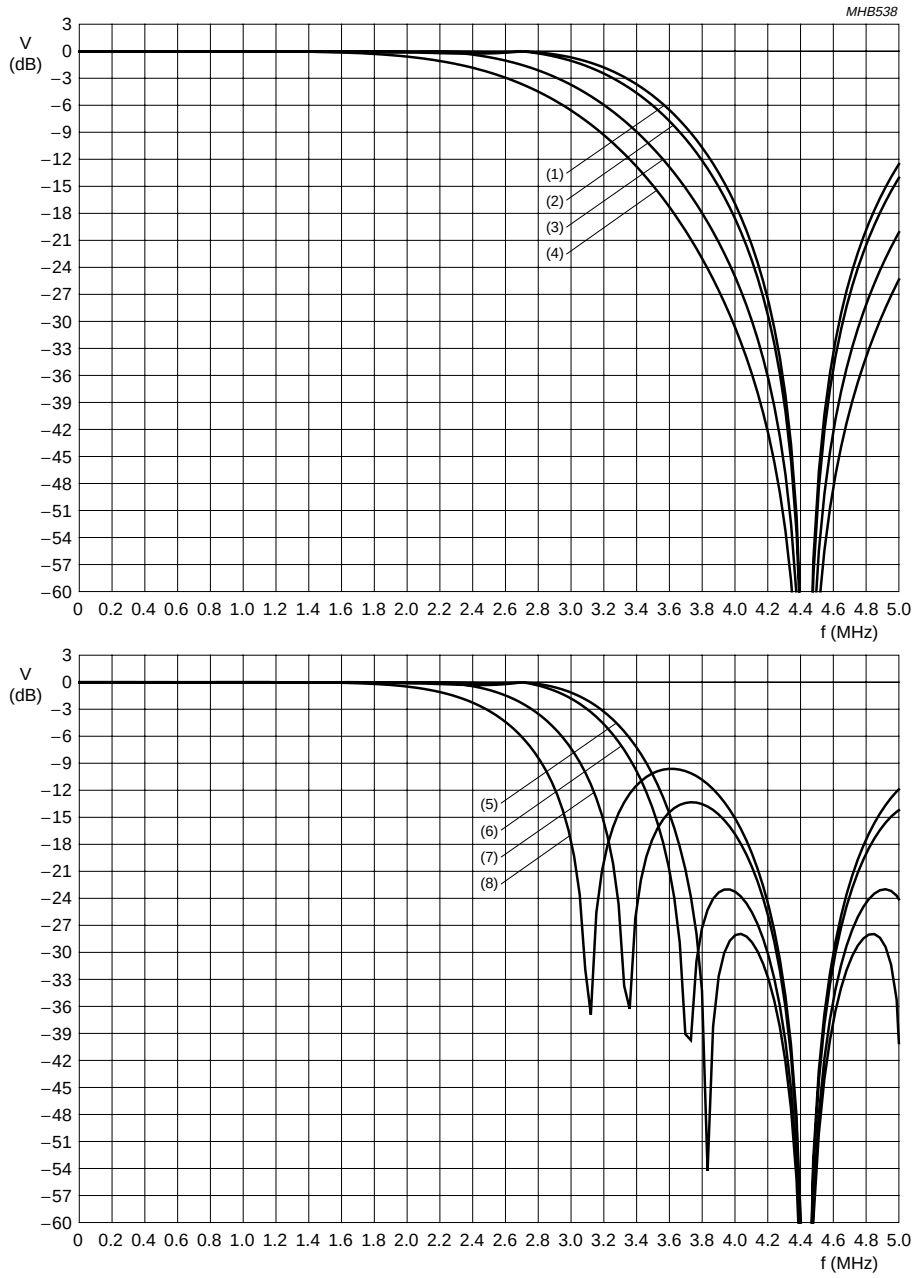
Fig.14 Transfer characteristics of the luminance notch filter in 3.58 MHz mode (Y-comb filter disabled) at LUBW = 1.



(1) LCBW[2:0] = 000.
(2) LCBW[2:0] = 010.
(3) LCBW[2:0] = 100.
(4) LCBW[2:0] = 110.

(5) LCBW[2:0] = 001.
(6) LCBW[2:0] = 011.
(7) LCBW[2:0] = 101.
(8) LCBW[2:0] = 111.

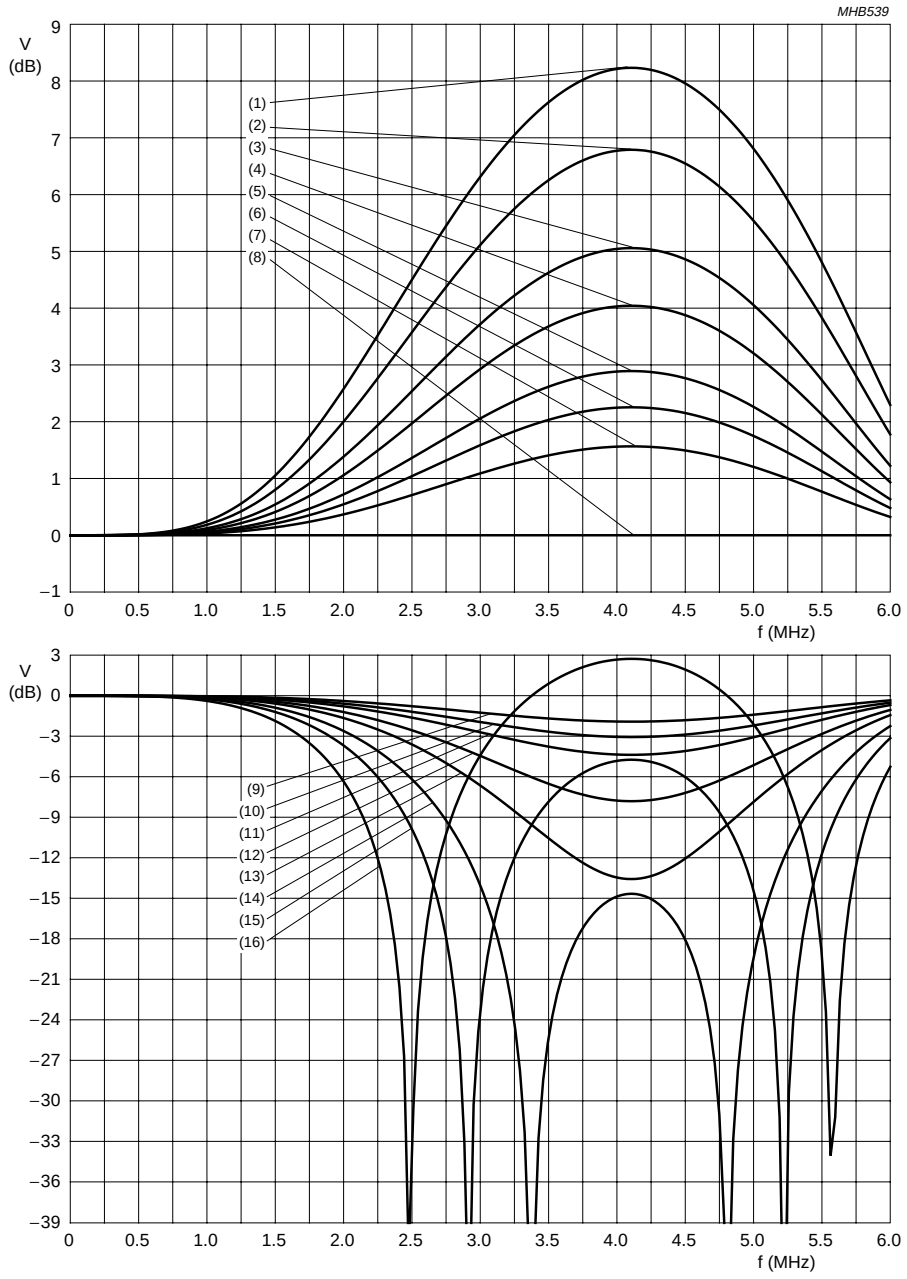
Fig.15 Transfer characteristics of the luminance notch filter in 4.43 MHz mode (Y-comb filter disabled) at LUBW = 0.



(1) LCBW[2:0] = 000.
(2) LCBW[2:0] = 010.
(3) LCBW[2:0] = 100.
(4) LCBW[2:0] = 110.

(5) LCBW[2:0] = 001.
(6) LCBW[2:0] = 011.
(7) LCBW[2:0] = 101.
(8) LCBW[2:0] = 111.

Fig.16 Transfer characteristics of the luminance notch filter in 4.43 MHz mode (Y-comb filter disabled) at LUBW = 1.



(1) LUFI[3:0] = 0001.
(2) LUFI[3:0] = 0010.
(3) LUFI[3:0] = 0011.
(4) LUFI[3:0] = 0100.
(5) LUFI[3:0] = 0101.
(6) LUFI[3:0] = 0110.
(7) LUFI[3:0] = 0111.
(8) LUFI[3:0] = 0000.

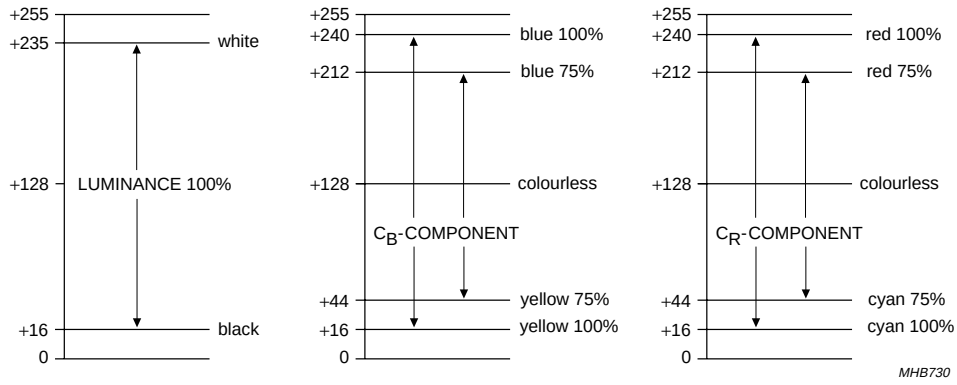
(9) LUFI[3:0] = 1000.
(10) LUFI[3:0] = 1001.
(11) LUFI[3:0] = 1010.
(12) LUFI[3:0] = 1011.
(13) LUFI[3:0] = 1100.
(14) LUFI[3:0] = 1101.
(15) LUFI[3:0] = 1110.
(16) LUFI[3:0] = 1111.

Fig.17 Transfer characteristics of the luminance peaking/low-pass filter (sharpness).

8.1.2.3 Brightness Contrast Saturation (BCS) control and decoder output levels

The resulting Y (CVBS) and C_B-C_R signals are fed to the BCS block, which contains the following functions:

- Chrominance saturation control by DSAT7 to DSAT0
- Luminance contrast and brightness control by DCON7 to DCON0 and DBRI7 to DBRI0
- Raw data (CVBS) gain and offset adjustment by RAWG7 to RAWG0 and RAWO7 to RAWO0
- Limiting Y-C_B-C_R or CVBS to the values 1 (minimum) and 254 (maximum) to fulfil *"ITU Recommendation 601/656"*.



a. Y output range. b. C_B output range. c. C_R output range.

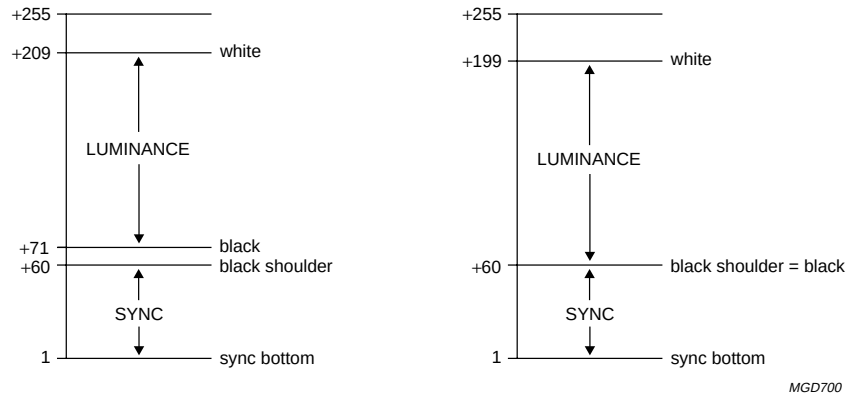
"ITU Recommendation 601/656" digital levels with default BCS (decoder) settings DCON[7:0] = 44H, DBRI[7:0] = 80H and DSAT[7:0] = 40H. Equations for modification to the Y-C_B-C_R levels via BCS control I^2C-bus bytes DBRI, DCON and DSAT.

Luminance: $Y_{OUT} = Int\left[\frac{DCON}{68} \times (Y - 128)\right] + DBRI$

Chrominance: $(C_R C_B)_{OUT} = Int\left[\frac{DSAT}{64} \times (C_R, C_B - 128)\right] + 128$

It should be noted that the resulting levels are limited to 1 to 254 in accordance with *"ITU Recommendation 601/656"*.

Fig.18 Y-C_B-C_R range for scaler input and X-port output.



a. Sources containing 7.5 IRE black level offset (e.g. NTSC M).

b. Sources not containing black level offset.

CVBS levels with default settings RAWG[7:0] = 64 and RAWO[7:0] = 128.
Equation for modification of the raw data levels via bytes RAWG and RAWO:

$$CVBS_{OUT} = Int\left[\frac{RAWG}{64} \times (CVBS_{nom} - 128)\right] + RAWO$$

It should be noted that the resulting levels are limited to 1 to 254 in accordance with "*ITU Recommendation 601/656*".

Fig.19 CVBS (raw data) range for scaler input, data slicer and X-port output.

8.1.3 SYNCHRONIZATION

The prefiltered luminance signal is fed to the synchronization stage. Its bandwidth is further reduced to 1 MHz in a low-pass filter. The sync pulses are sliced and fed to the phase detectors where they are compared with the sub-divided clock frequency. The resulting output signal is applied to the loop filter to accumulate all phase deviations. Internal signals (e.g. HCL and HSY) are generated in accordance with analog front-end requirements. The loop filter signal drives an oscillator to generate the line frequency control signal LFCO; see Fig.20.

The detection of 'pseudo syncs' as part of the macrovision copy protection standard is also achieved within the synchronization circuit.

The result is reported as flag COPRO within the decoder status byte at subaddress 1FH.

8.1.4 CLOCK GENERATION CIRCUIT

The internal CGC generates all clock signals required for the video input processor.

The internal signal LFCO is a digital-to-analog converted signal provided by the horizontal PLL. It is the multiple of the line frequency:

6.75 MHz = 429 $\times$ f_H (50 Hz), or

6.75 MHz = 432 $\times$ f_H (60 Hz).

The LFCO signal is multiplied by a factor of 2 and 4 in the internal PLL circuit (including phase detector, loop filtering, VCO and frequency divider) to obtain the output clock signals. The rectangular output clocks have a 50% duty factor.

Table 5 Decoder clock frequencies

CLOCK	FREQUENCY (MHz)
XTALO	24.576 OR 32.110
LLC	27
LLC2	13.5
LLC4 (INTERNAL)	6.75
LLC8 (VIRTUAL)	3.375

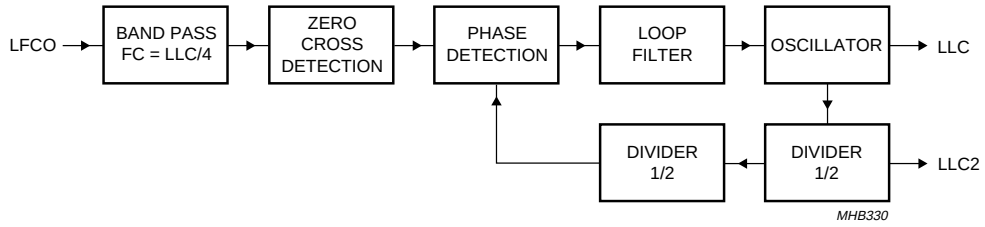


Fig.20 Block diagram of the clock generation circuit.

8.1.5 Power-on reset and Chip Enable (CE) input

A missing clock, insufficient digital or analog V_{DDA0} supply voltages (below 2.8 V) will start the reset sequence; all outputs are forced to 3-state (see Fig.21). The indicator output $\overline{RES}$ is LOW for approximately 128 LLC after the internal reset and can be applied to reset other circuits of the digital TV system.

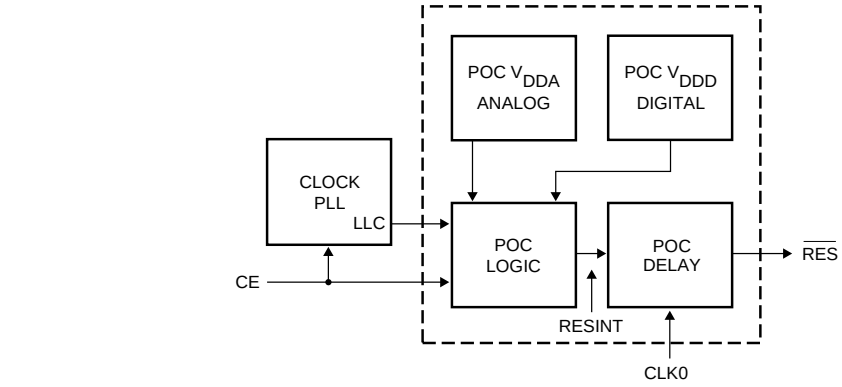
It is possible to force a reset by pulling the Chip Enable pin (CE) to ground. After the rising edge of CE and sufficient power supply voltage, the outputs LLC, LLC2 and SDA return from 3-state to active, while the other signals have to be activated via programming.

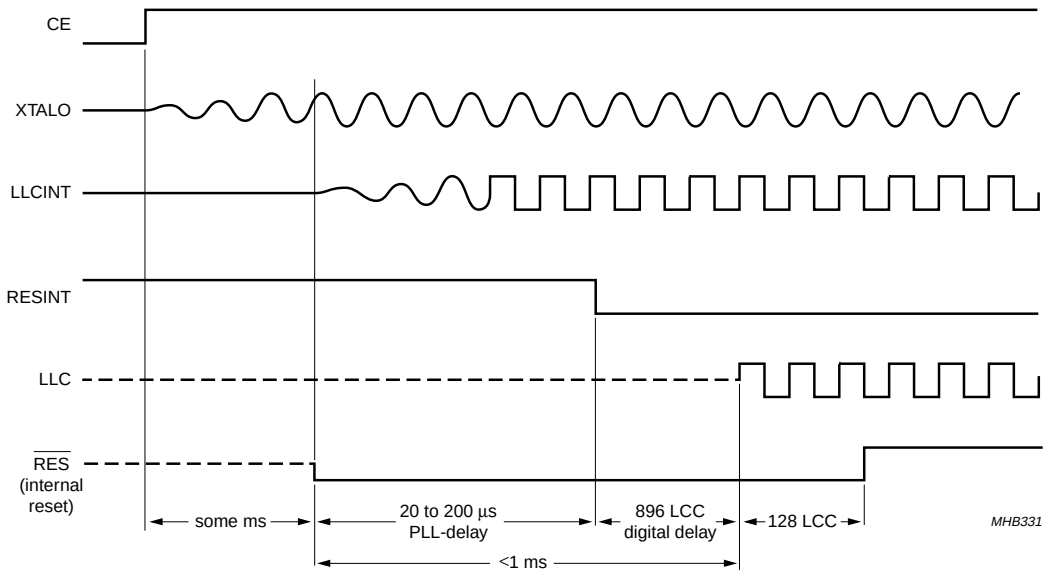
However, some external devices require an active clock during reset to avoid hang up. For these applications it is possible to activate both the I-port and/or the X-port outputs by pulling the ITRI- and/or XTRI inputs to logic 1 by an external pull up resistor (4.7 kΩ).

In detail: Pulling ITRI to 1 activates the outputs ICLK, IPD[7:0], IDQ, IGPH, IGPV, IGP0 and IGP1; pulling XTRI to 1 activates the outputs XCLK, XPD[7:0], XDQ, XRH and XRV. During reset both ICLK and XCLCK deliver the LLC-clock (27 MHz) generated by the internal decoder PLL.

If ITRI and/or XTRI are not connected, an internal pull up resistor takes care that these pins remain in 3-state.

In any case it is possible to force these ports to 3-state by setting XPE[1:0] and/or IPE[1:0] to 00.





POC = Power-on Control.
CE = chip enable input.
XTALO = crystal oscillator output.
LLCINT = internal system clock.
RESINT = internal reset.
LLC = line-locked clock output, occurs also on pins XCLK and/or ICLK if enabled via pull up resistor on XTRI and/or ITRI.
$\overline{RES}$ = reset output.

Fig.21 Power-on control circuit.

8.2 Output Formatter

The Output Formatter of the decoder part contains the ITU 656 8 bit / 10 bit formatter for the expansion port (X-Port) data output (XPD[7:0], XRH, XRV) including the selection of the reference signals for the RT port (RTCO, RTS0 and RTS1) and the expansion port (XRH, XRV and XDQ) (for a detailed description see Section 9.4.1) as well as the control circuitry for the signals needed for the internal paths to the scaler and data slicer part.

This control circuitry requests decoded video data (Y-C_B-C_R 4 : 2 : 2) or raw data from the combfilter decoder output to be provided to expansion port (X-Port) output, to the scaler input and to the VBI data slicer input. This data request is user controlled by the line control registers LCR2 to LCR24 (see also Chapter 16; subaddresses 41H to 57H).

Each of the registers LCR2 to LCR23 defines a data type to be decoded in the associated line; i.e.: the VBI data type can be set independently for each of the lines. Therefore LCR2 to LCR23 refer to line numbers. The selection in LCR24 values is valid for the rest of the corresponding field. The upper nibble of each of the 23 LCR registers contains the value for field 1 (odd), the lower nibble for field 2 (even). The relationship between LCR values and line numbers can be adjusted via VOFF8 to VOFF0, located in subaddresses 5BH (bit 4) and 5AH (bits 7 to 0), FOFF subaddress 5BH (bit D7) and VEP subaddress 5BH (bit D5). The recommended values are VOFF[8:0] = 03H for 50 Hz sources (with FOFF = 0) and VOFF[8:0] = 06H for 60 Hz sources (with FOFF = 1), to accommodate line number conventions as used for PAL, SECAM and NTSC standards; see Tables 7 to 10.
N**ote**: The line counting scheme for 60 Hz standards, with VOFF = 0x06, as mentioned in Fig.23, table 7 and table 8, leads the VBI slicer to take the old field ID as reference for it's field processing. For consistent ID interpretation the VOFF value need to be set to 0x03.

Table 6 Data formats at decoder output

Data type		**60Hz / 525 Lines VBI Data Standards**		**50Hz / 625 Lines VBI Data Standards**	
No.	**binary**	**DESCRIPTION**	**Decoder output data format**	**DESCRIPTION**	**Decoder output data format**
0	0000	do not acquire (active video)	Y-C_B-C_R 4:2:2	do not acquire (active video)	Y-C_B-C_R 4:2:2
1	0001	US Teletext (WST525)	raw data	Euro Teletext (WST625)	raw data
2	0010	NABTS	raw data	Euro Teletext with progammable Framing Code	raw data
3	0011	Moji	raw data	reserved	reserved
4	0100	US Closed Caption (CC525)	raw data	Euro Closed Caption (CC625)	raw data
5	0101	CGMS (WSS525)	raw data	Euro Wide Screen Signalling (WSS625)	raw data
6	0110	VITC525	raw data	VITC625	raw data
7	0111	Gemstar2x	raw data	VPS	raw data
8	1000	Gemstar1x	raw data	reserved	reserved
9	1001	reserved	reserved	reserved	reserved
10	1010	Open1 (5 MHz)	raw data	Open1 (5 MHz)	raw data
11	1011	Open2 (5,7272 MHz)	raw data	Open2 (5,7272 MHz)	raw data
12	1100	reserved	reserved	reserved	reserved
13	1101	do not acquire (RAW)	raw data	do not acquire (RAW)	raw data
14	1110	do not acquire (Test)	reserved	do not acquire (Test)	reserved
15	1111	do not acquire (active video)	Y-C_B-C_R 4:2:2	do not acquire (active video)	Y-C_B-C_R 4:2:2

The adjustment of the slicer processing, the adjustment of video output data via the expansion port (X-Port) and the adjustment of video data transferred to the scaler relative to the input signal source is defined by the programming

registers 59h to 5BH, There are programmable offsets in the horizontal and vertical direction available: parameters HOFF[10:0] 5BH[2:0] 59H[7:0], VOFF[8:0] 5BH[4] 5AH[7:0], FOFF[5BH[7]] and VEP[5BH[5]]). I.e. these control registers are defining the decoder data output format - active video, raw samples (optionally a test line), which is delivered from combfilter video decoder output to the expansion port output, the scaler and the VBI Data Slicer.

Table 7 Relationship of LCR to line numbers in 525 lines/60 Hz systems (part 1)

Vertical line offset, VOFF[8:0] = 06H,resp. 03H (subaddresses 5BH[4] and 5AH[7:0]); horizontal pixel offset, HOFF[10:0] = 347H (subaddresses 5BH[2:0] and 59H[7:0]); FOFF = 1 (subaddress 5BH[7]), VEP = 0 (subaddress 5BH[5])

LINE NUMBER (1ST FIELD)	**521**	**522**	**523**	**524**	**525**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
	ACTIVE VIDEO					**EQUALIZATION PULSES**			**SERRATION PULSES**			**EQUALIZATION PULSES**		
LINE NUMBER (2ND FIELD)	**259**	**260**	**261**	**262**	**263**	**264**	**265**	**266**	**267**	**268**	**269**	**270**	**271**	**272**
	ACTIVE VIDEO					**EQUALIZATION PULSES**			**SERRATION PULSES**			**EQUALIZATION PULSES**		
LCR VOFF = 06H	**24**						**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
LCR VOFF = 03H	**24**									**2**	**3**	**4**	**5**	**6**

Table 8 Relationship of LCR to line numbers in 525 lines/60 Hz systems (part 2)

Vertical line offset, VOFF[8:0] = 06H,resp. 03H (subaddresses 5BH[4] and 5AH[7:0]); horizontal pixel offset, HOFF[10:0] = 347H (subaddresses 5BH[2:0] and 59H[7:0]); FOFF = 1 (subaddress 5BH[7]), VEP = 0 (subaddress 5BH[5])

LINE NUMBER (1ST FIELD)	**10**	**11**	**12**		**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**
	NOMINAL VBI-LINES F1								**ACTIVE VIDEO**						
LINE NUMBER (2ND FIELD)	**273**	**274**	**275**		**281**	**282**	**283**	**284**	**285**	**286**	**287**	**288**	**289**	**290**	**291**
	NOMINAL VBI-LINES F2								**ACTIVE VIDEO**						
LCR VOFF = 06H	**13**	**14**	**15**		**18**	**19**	**20**	**21**	**22**	**23**	**24**				
LCR VOFF = 03H	**7**	**8**	**9**		**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	

Table 9 Relationship of LCR to line numbers in 625 lines/50 Hz systems (part 1)

Vertical line offset, VOFF[8:0] = 03H (subaddresses 5BH[4] and 5AH[7:0]); horizontal pixel offset, HOFF[10:0] = 347H (subaddresses 5BH[2:0] and 59H[7:0]); FOFF = 0 (subaddress 5BH[7]), VEP = 0 (subaddress 5BH[5])

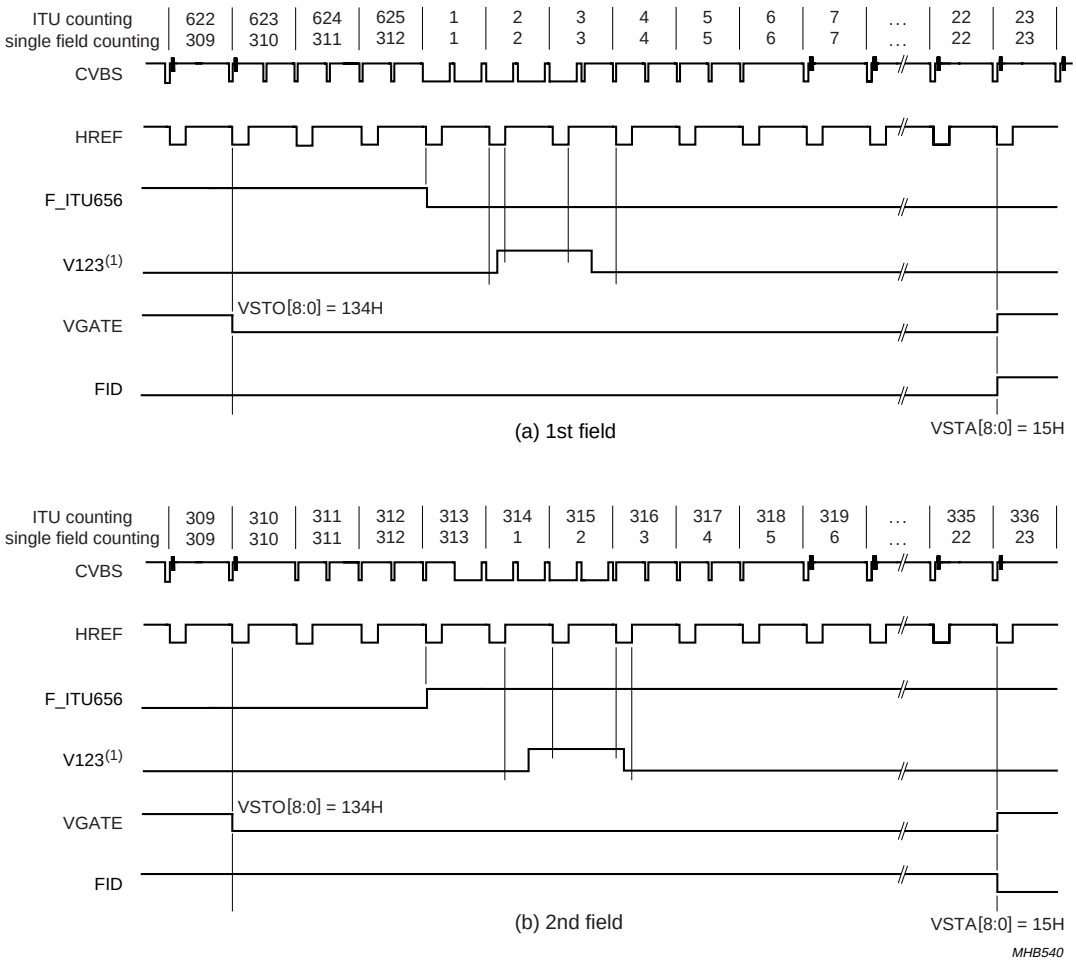
LINE NUMBER (1ST FIELD)	**621**	**622**	**623**	**624**	**625**	**1**	**2**	**3**	**4**	**5**
	ACTIVE VIDEO		**EQUALIZATION PULSES**			**SERRATION PULSES**		**EQUALIZATION PULSES**		
LINE NUMBER (2ND FIELD)	**309**	**310**	**311**	**312**	**313**	**314**	**315**	**316**	**317**	**318**
	ACTIVE VIDEO		**EQUALIZATION PULSES**		**SERRATION PULSES**			**EQUALIZATION PULSES**		
LCR	**24**						**2**	**3**	**4**	**5**

Table 10 Relationship of LCR to line numbers in 625 lines/50 Hz systems (part 2)

Vertical line offset, VOFF[8:0] = 03H (subaddresses 5BH[4] and 5AH[7:0]); horizontal pixel offset, HOFF[10:0] = 347H (subaddresses 5BH[2:0] and 59H[7:0]); FOFF = 0 (subaddress 5BH[7]), VEP = 0 (subaddress 5BH[5])

LINE NUMBER (1ST FIELD)	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**
	NOMINAL VBI-LINES F1																		**ACTIVE VIDEO**	
LINE NUMBER (2ND FIELD)	**319**	**320**	**321**	**322**	**323**	**324**	**325**	**326**	**327**	**328**	**329**	**330**	**331**	**332**	**333**	**334**	**335**	**336**	**337**	**338**
	NOMINAL VBI-LINES F2																	**ACTIVE VIDEO**		
LCR	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	

The relationship of these programming values to the input signal and the recommended values is outlined in table 7 to table 10.



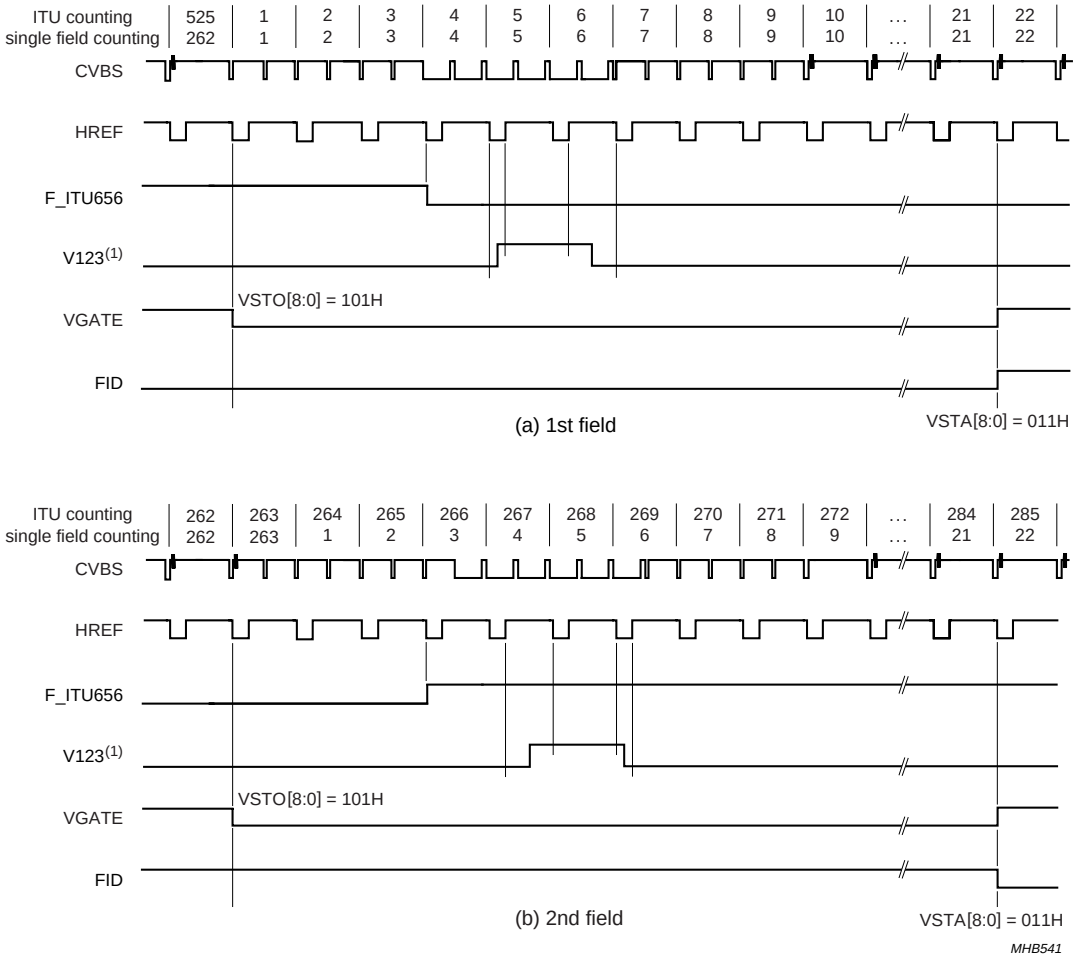
(1) The inactive going edge of the V123 signal indicates whether the field is odd or even. If HREF is active during the falling edge of V123, the field is ODD (field 1). If HREF is inactive during the falling edge of V123, the field is EVEN. The specific position of the slope is dependent on the internal processing delay and may change a few clock cycles from version to version.

The control signals listed above are available on pins RTS0, RTS1, XRH and XRV according to the following table:

NAME	RTS0	RTS1	XRH	XRV
HREF	**X**	**X**	**X**	–
F_ITU656	–	–	–	**X**
V123	**X**	**X**	–	**X**
VGATE	**X**	**X**	–	–
FID	**X**	**X**	–	–

For further information see Section 16.2: Tables 69, 70 and 71.

Fig.22 Vertical timing diagram for 50 Hz/625 line systems.



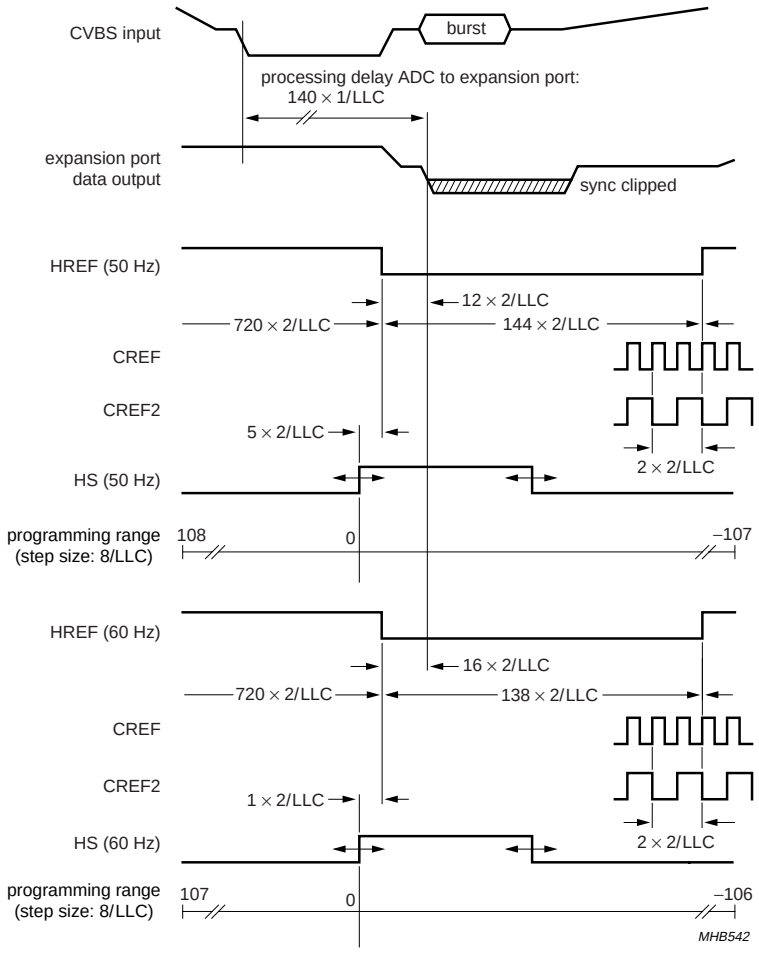
(1) The inactive going edge of the V123 signal indicates whether the field is odd or even. If HREF is active during the falling edge of V123, the field is ODD (field 1). If HREF is inactive during the falling edge of V123, the field is EVEN. The specific position of the slope is dependent on the internal processing delay and may change a few clock cycles from version to version.

The control signals listed above are available on pins RTS0, RTS1, XRH and XRV according to the following table:

NAME	RTS0	RTS1	XRH	XRV
HREF	**X**	**X**	**X**	–
F_ITU656	–	–	–	**X**
V123	**X**	**X**	–	**X**
VGATE	**X**	**X**	–	–
FID	**X**	**X**	–	–

For further information see Section 16.2: Tables 69, 70 and 71.

Fig.23 Vertical timing diagram for 60 Hz/525 line systems.



The signals HREF, HS, CREF2 and CREF are available on pins RTS0 and/or RTS1. Their polarity can be inverted via RTP0 and/or RTP1 (see Section 16.2: Tables 69, 70 and 71)

The signals HREF and HS are available on pin XRH (see Section 16.2 Table 72).

Fig.24 Horizontal timing diagram (50/60 Hz).

8.3 Scaler

The high performance video scaler in the SAA7115 has the following major blocks:

- Acquisition control (horizontal and vertical timer) and task handling (the region/field/frame based processing)
- Prescaler, for horizontal down-scaling by an integer factor, combined with appropriate band limiting filters, especially anti-aliasing for CIF format
- Brightness, saturation, contrast control to adjust scale dependent amplification
- Line buffer, with asynchronous read and write, to support vertical up-scaling (e.g. for videophone application, converting 240 into 288 lines, Y-C_B-C_R 4 : 2 : 2)
- Vertical scaling, with phase accurate Linear Phase Interpolation (LPI) for zoom and downscale, or phase accurate Accumulation Mode (ACM) for large downscaling ratios and better alias suppression
- Variable Phase Delay (VPD), operates as horizontal phase accurate interpolation for arbitrary non-integer scaling ratios, supporting conversion between square and rectangular pixel sampling
- Output formatter for scaled Y-C_B-C_R 4 : 2 : 2, Y-C_B-C_R 4 : 1 : 1 and Y only (format also for raw data)
- FIFO, 32-bit wide, with 64 pixel capacity in Y-C_B-C_R formats
- Output interface, 8 or 16-bit (only if extended by H-port) data pins wide, synchronous or asynchronous operation, with stream events on discrete pins, or coded in the data stream.

The overall H and V zooming (HV_zoom) is restricted by the input/output data rate relationships. With a safety margin of 2% for running in and running out,

the maximum HV_zoom is equal to: $0.98 \times \frac{T_input_field - T_v_blanking}{in_pixel \times in_lines \times out_cycle_per_pix \times T_out_clk}$

For example:

1. Input from decoder: 50 Hz, 720 pixel, 288 lines, 16-bit data at 13.5 MHz data rate, 1 cycle per pixel; output: 8-bit data at 27 MHz, 2 cycles per pixel;

   the maximum HV_zoom is about: $0.98 \times \frac{20\ ms - 24 \times 64\ \mu s}{720 \times 288 \times 2 \times 37\ ns} = 1.18$

2. Input from X-port: 60 Hz, 720 pixel, 240 lines, 8-bit data at 27 MHz data rate (ITU 656), 2 cycles per pixel; output via I + H-port: 16-bit data at 27 MHz clock, 1 cycle per pixel;

   the maximum HV_zoom is about: $0.98 \times \frac{16.666\ ms - 22 \times 64\ \mu s}{720 \times 240 \times 1 \times 37\ ns} = 2.34$

The data flow in the scaler is controlled by internal data valid and data request flags (internal handshake signalling) between the sub-blocks, as the scaling process itself is discontinuous and dynamical. Therefore the entire scaler acts as a pipeline buffer. Depending on the actually programmed scaling parameters the effective buffer can exceed to an entire line. This allows vertical upscaling, more flexible video stream timing at the image port, discontinuous transfers and handshake. The access/bandwidth requirements to the VGA frame buffer are reduced significantly.

The video scaler receives its input signal from the video decoder or from the expansion port (X-port). It gets 16-bit Y-C_B-C_R 4 : 2 : 2 input data at a continuous rate of 13.5 MHz from the decoder. Discontinuous data stream can be accepted from the expansion port (X-port), normally 8-bit wide ITU 656 like Y-C_B-C_R data, accompanied by a pixel qualifier on XDQ.

The input data stream is sorted into two data paths, one for luminance (or raw samples) and one for time multiplexed chrominance C_B and C_R samples. An Y-C_B-C_R 4 : 1 : 1 input format from the X-port is converted to 4 : 2 : 2 for the horizontal prescaling and vertical filter scaling operation.

The scaler operation is defined by two programming pages A and B, representing two different tasks, that can be applied field alternating or to define two regions in a field (e.g. with different scaling range, factors and signal source during odd and even fields).

Each programming page contains control:

- For signal source selection and formats
- For task handling and trigger conditions
- For input and output acquisition window definition
- For H-prescaler, V-scaler and H-phase scaling.

Raw VBI-data is handled as specific input format and needs its own programming page (equals own task).

In VBI pass through operation the processing of prescaler and vertical scaling has to be set to no-processing, however, the horizontal fine scaling VPD can be activated. Upscaling (oversampling, zooming), free of frequency folding, up to a factor of 3.5 can be achieved, as required by some software data slicing algorithms.

These raw samples are transported through the image port as valid data and can be output as Y only format. Also this Y only lines can be framed by SAV and EAV codes.

8.3.1 Acquisition control and task handling (subaddresses 80H, 90H, 91H, 94H to 9FH and C4H to CFH)

The acquisition control receives horizontal and vertical synchronization signals from the decoder section or from the X-port. The acquisition window is generated via pixel and line counters at the appropriate places in the data path. From X-port only qualified pixels and lines (lines with qualified pixel) are counted.

The acquisition window parameters are as follows:

- Signal source selection regarding input video stream and formats from the decoder, or from X-port (programming bits SCSRC[1:0] 91H[5:4] and FSC[2:0] 91H[2:0])

  Remark: The input of raw VBI-data from the internal decoder need to be controlled via the decoder output formatter and the LCR registers (see Section 8.2)
- Vertical offset defined in lines of the video source, parameter YO[11:0] 99H[3:0] 98H[7:0]
- Vertical length defined in lines of the video source, parameter YS[11:0] 9BH[3:0] 9AH[7:0]
- Vertical length defined in number of target lines, as a result of vertical scaling, parameter YD[11:0] 9FH[3:0] 9EH[7:0]
- Horizontal offset defined in number of pixels of the video source, parameter XO[11:0] 95H[3:0] 94H[7:0]
- Horizontal length defined in number of pixels of the video source, parameter XS[11:0] 97H[3:0] 96H[7:0]
- Horizontal destination size, defined in target pixels after fine scaling, parameter XD[11:0] 9DH[3:0] 9CH[7:0].

The source start offset (XO11 to XO0 and YO11 to YO0) opens the acquisition window, and the target size (XD11 to XD0, YD11 to YD0) closes the window, but the window is cut vertically, if there are less output lines than expected. The trigger events for the pixel and line counts are the horizontal and vertical reference edges as defined in subaddress 92H.

The task handling is controlled by subaddress 80H and 90H (see Section 8.3.1.2).
To support instable non standard input signals, different operational modes are implemented (bits CMOD and FMOD).

8.3.1.1 Input field processing

The scaler directly gets a corresponding field ID information from the SAA7115 decoder path.
If switched to the X-port, the trigger event for the field sequence detection from external signals (X-port) are defined in subaddress 92H. From the X-port the state of the scalers H-reference signal at the time of the V-reference edge is taken as field sequence identifier FID. For example, if the falling edge of the XRV input signal is the reference and the state of XRH input is logic 0 at that time, the detected field ID is logic 0.

The bits XFDV[92H[7]] and XFDH[92H[6]] define the detection event and state of the flag from the X-port. For the default setting of XFDV and XFDH at ‘00’ the state of the H-input at the falling edge of the V-input is taken.

The FID flag is used to determine whether the first or second field of a frame is going to be processed within the scaler and it is used as trigger condition for the task handling (see bits STRC[1:0] 90H[1:0]).

According to ITU 656, when FID is at logic 0 means first field of a frame. To ease the application, the polarities of the detection results on the X-port signals and the internal decoder ID can be changed via XFDH.

As the V-sync from the decoder path has a half line timing (due to the interlaced video signal), but the scaler processing only knows about full lines, during 1st fields from the decoder the line count of the scaler possibly shifts by one line, compared to the 2nd field. This can be compensated for by switching the V-trigger event, as defined by XDV0, to the opposite V-sync edge or by using the vertical scalers phase offsets. The vertical timing of the decoder can be seen in Figs 22 and 23.

As the H and V reference events inside the ITU 656 data stream (from X-port) and the real-time reference signals from the decoder path are processed differently, the trigger events for the input acquisition also have to be programmed differently.

Table 11 Processing trigger and start

DESCRIPTION	XDV1 92H[5]	XDV0 92H[4]	XDH 92H[2]
Internal decoder: The processing triggers at the reference edge of the V123 pulse (see Figs 22 (50 Hz) and 23 (60 Hz)), and starts earliest with the rising edge of the decoder HREF at line number:			
falling edge: 4/7 (50/60 Hz, 1st field), resp. 3/6 (50/60 Hz, 2nd field) (decoder count)	0	1	0
rising edge: 2/5 (50/60 Hz, 1st field), resp. 2/5 (50/60 Hz, 2nd field) (decoder count)	0	0	0
External ITU 656 stream: The processing starts earliest with SAV at line number 23 (50 Hz system), respectively line 20 (60 Hz system) (according to ITU 656 count)	0	0	0

8.3.1.2 Task handling

The task handler controls the switching between the two programming register sets. The main function is controlled by subaddresses 90H and C0H.
The operational modes of the task handler are controlled by the bits CMOD[80H[7]] and FMOD[9bH[7]].

A task is enabled via the global control bits TEA[80H[4]] and TEB[80H[5]].
The handler is then triggered by events, which can be defined for each register set.

In case of a programming error the task handling and the complete scaler can be reset to the initial states by setting the software reset bit SWRST[88H[5]] to logic 0. Especially if the programming registers, related acquisition window and scale are reprogrammed while a task is active, a software reset **MUST** be performed after programming.

Contrary to the disabling/enabling of a task, which is evaluated at the end of a running task, when SWRST is at logic 0 it sets the internal state machines directly to their idle states.

The basic operation of the task handler is strongly orientated on the window definitions, which means, if a starting point (in terms of XO and YO values) is missed, or the window definition (especially in terms of the (YO + YS) value) is larger than the input field, the operation is inhibited or incoming video fields are skipped.
To better support non standard input signals and signal sources with varying field lengths (like a VCR in fast forward/rewind mode), there are now some different operational modes implemented for the task handling.

Field Mode (bit FMOD [9BH[7]])
This is a task specific bit (for flexibility reasons), but normally both tasks should be programmed to the same value.
If the FMOD bit is set to ‘1’ the YO and YS parameters change the meaning.
YO defines the start line and YS the end line (instead of the window length) for the scalers processing window.
Additionally the trigger conditions of the task handler are changed.

In ‘field mode’ the vertical trigger event gets higher priority than the vertical window definition.
The processing is normally started at line number YO and ends at line number YS, but
- if a vertical trigger occurs, before the line number YS is reached, the field processing is terminated and the next task is checked
- if the actual line count at V-trigger is between the YO and the YS value, the task processing is started, also if the line number YO is missed.

Continuous Mode (bit CMOD [80H[7]])
Applications, which do not use the vertical scaling, may take advantage from the ‘continuous processing mode’. In this mode a task is started via the SWRST bit and the task enable bits TEA or TEB. The horizontal window definition keeps it’s meaning, but YO and YS are ignored. The vertical blanking scheme is defined by the selected V-sync (see bits V_EAV). Once started, the vertical retrigger pulses from the input are ignored and SWRST at ‘0’ is needed to stop the task processing.

Start, Repeat and Skip
The start condition for the handler is defined by bits STRC[1:0] 90H[1:0] and means: start immediately, wait for next V-sync, next FID at logic 0 or next FID at logic 1. The FID is evaluated, if the vertical and horizontal offsets are reached.

When RPTSK[90H[2]] is at logic 1 the actual running task is repeated (under the defined trigger conditions), before handing control over to the alternate task.

To support field rate reduction, the handler is also enabled to skip fields (bits FSKP[2:0] 90H[5:3]) before executing the task. A TOGGLE flag is generated (used for the correct output field processing), which changes state at the beginning of a task, every time a task is activated. Examples are given in Section 8.3.1.3.

Remarks:

- **To activate a task the start condition must be fulfilled and, in case of FMOD = 0, the acquisition window offsets must be reached**.

  For example, in case of ‘start immediately’, and two regions are defined for one field, the offset of the lower region must be greater than (offset + length) the upper region, if not, the actual counted H and V position at the end of the upper task is beyond the programmed offsets and the processing will ‘wait for next V’.
- **Basically the trigger conditions are checked, when a task is activated**. It is important to realize, that they are not checked while a task is inactive. So you can not trigger to next logic 0 or logic 1 with overlapping offset and active video ranges between the tasks (e.g. task A STRC[2:0] = 2, YO[11:0] = 310 and task B STRC[2:0] = 3, YO[11:0] = 310 results in output field rate of $50/3$ Hz).
- **After power-on or software reset (via SWRST[88H[5]]) task B gets priority over task A**.

8.3.1.3 Output field processing

As a reference for the output field processing, two signals are available for the back-end hardware.

These signals are the input field ID from the scaler source and a TOOGLE flag, which shows that an active task is used an odd (1, 3, 5...) or even (2, 4, 6...) number of times. Using a single or both tasks and reducing the field or frame rate with the task handling functionality, the TOGGLE information can be used, to reconstruct an interlaced scaled picture at a reduced frame rate. The TOGGLE flag isn’t synchronized to the input field detection, as it is only dependent on the interpretation of this information by the external hardware, whether the output of the scaler is processed correctly (see Section 8.3.3).

With OFIDC = 0, the scalers input field ID is available as output field ID on bit D6 of SAV and EAV, respectively on pin IGP0 (IGP1), if FID output is selected.

When OFIDC[90H[6]] = 1, the TOGGLE information is available as output field ID on bit D6 of SAV and EAV, respectively on pin IGP0 (IGP1), if FID output is selected.

Additionally the bit D7 of SAV and EAV can be defined via CONLH[90H[7]]. CONLH[90H[7]] = 0 (default) sets D7 to logic 1, a logic 1 inverts the SAV/EAV bit D7. So it is possible to mark the output of the both tasks by different SAV/EAV codes. This bit can also be seen as ‘task flag’ on the pins IGP0 (IGP1), if TASK output is selected.

Table 12 Examples for field processing

SUBJECT	EXAMPLE 1[1]			EXAMPLE 2[2][3]				EXAMPLE 3[2][4][5]						EXAMPLE 4[2][4][6]					
FIELD SEQUENCE FRAME/FIELD	**1/1**	**1/2**	**2/1**	**1/1**	**1/2**	**2/1**	**2/2**	**1/1**	**1/2**	**2/1**	**2/2**	**3/1**	**3/2**	**1/1**	**1/2**	**2/1**	**2/2**	**3/1**	**3/2**
Processed by task	A	A	A	B	A	B	A	B	B	A	B	B	A	B	B	A	B	B	A
State of detected ITU 656 FID	0	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
TOGGLE flag	1	0	1	1	1	0	0	1	0	1	1	0	0	0[7]	1	1	1[7]	0	0
Bit D6 of SAV/EAV byte	0	1	0	0	1	0	1	1	0	1	1	0	0	0[7]	1	1	1[7]	0	0
Required sequence conversion at the vertical scaler[8]	UP ↓ UP	LO ↓ LO	UP ↓ UP	UP ↓ UP	LO ↓ LO	UP ↓ UP	LO ↓ LO	UP ↓ LO	LO ↓ UP	UP ↓ LO	LO ↓ LO	UP ↓ UP	LO ↓ UP	UP ↓ UP	LO ↓ LO	UP ↓ LO	LO ↓ LO	UP ↓ UP	LO ↓ UP
Output[9]	O	O	O	O	O	O	O	O	O	O	O	O	O	NO	O	O	NO	O	O

Notes

1. Single task every field; OFIDC = 0; subaddress 90H at 40H; TEB[80H[5]] = 0.
2. Tasks are used to scale to different output windows, priority on task B after SWRST.
3. Both tasks at $^1/_2$ frame rate; OFIDC = 0; subaddresses 90H at 43H and C0H at 42H.
4. In examples 3 and 4 OFIDC = 1, thus the association between input FID and tasks may be flipped, dependent on which time the SWRST is deasserted.
5. Task B at $^2/_3$ frame rate constructed from neighbouring motion phases; task A at $^1/_3$ frame rate of equidistant motion phases; subaddresses 90H at 41H and C0H at 45H.
6. Task A and B at $^1/_3$ frame rate of equidistant motion phases; subaddresses 90H at 41H and C0H at 49H.
7. Due to no data output for this field, the state of the prior field is hold.
8. It is assumed that input/output FID = 0 (= upper lines); UP = upper lines; LO = lower lines.
9. O = data output; NO = no output.

8.3.2 HORIZONTAL SCALING

The overall horizontal required scaling factor has to be split into a binary and a rational value according to the equation:

With $\text{H-scale ratio} = \frac{\text{output pixel}}{\text{input pixel}}$ there is

$$\text{H-scale ratio} = \frac{1}{\text{XPSC[5:0]}} \times \frac{1024}{\text{XSCY[12:0]}}$$

where the parameter of prescaler XPSC[5:0] = 1 to 63
and the parameter of VPD phase interpolation XSCY[12:0] = 300 to 8191 (0 to 299 are only theoretical values).
For example, $1/3.5$ is to split in $1/4 \times 1.14286$. The binary factor is processed by the prescaler, the arbitrary non-integer ratio is achieved via the variable phase delay VPD circuitry, called horizontal fine scaling. The latter calculates horizontally interpolated new samples with a 6-bit phase accuracy, which relates to less than 1 ns jitter for regular sampling scheme. Prescaler and fine scaler create the horizontal scaler of the SAA71157115.

Using the accumulation length function of the prescaler (XACL[5:0] A1H[5:0]), application and destination dependent (e.g. scale for display or for a compression machine), a compromise between visible bandwidth and alias suppression can be determined.

8.3.2.1 Horizontal prescaler (subaddresses A0H to A7H and D0H to D7H)

The prescaling function consists of an FIR anti-alias filter stage and an integer prescaler, which creates an adaptive prescale dependent low-pass filter to balance sharpness and aliasing effects.

The FIR prefilter stage implements different low-pass characteristics to reduce alias for downscales in the range of 1 to $1/2$. A CIF optimized filter is built-in, which reduces artefacts for CIF output formats (to be used in combination with the prescaler set to $1/2$ scale); see Table 13.
Fade-in and fade-out of the filters is achieved by copying an original source sample each as first and last pixel after prescaling.

Figs 25 and 26 show the frequency characteristics of the selectable FIR filters.

Table 13 FIR prefilter functions

PFUV[1:0] A2H[7:6] PFY[1:0] A2H[5:4]	LUMINANCE FILTER COEFFICIENTS	CHROMINANCE COEFFICIENTS
00	bypassed	bypassed
01	1 2 1	1 2 1
10	–1 1 1.75 4.5 1.75 1 –1	3 8 10 8 3
11	1 2 2 2 1	1 2 2 2 1

The function of the prescaler is defined by:

- An integer prescaling ratio XPSC[5:0] A0H[5:0] (equals 1 to 63), which covers the integer downscale range 1 to $1/63$
- An averaging sequence length XACL[5:0] A1H[5:0] (equals 0 to 63); range 1 to 64
- A DC gain renormalization XDCG[2:0] A2H[2:0]; 1 down to $1/128$
- The bit XC2_1[A2H[3]], which defines the weighting of the incoming pixels during the averaging process:
  - XC2_1 = 0 ⇒ 1 + 1...+ 1 +1
  - XC2_1 = 1 ⇒ 1 + 2...+ 2 +1

The prescaler creates a prescale dependent FIR low-pass, with up to (64 + 7) filter taps. The parameter XACL[5:0] can be used to vary the low-pass characteristic for a given integer prescale of $1/\text{XPSC[5:0]}$. The user can therewith decide between signal bandwidth (sharpness impression) and alias.

Remark: Due to bandwidth considerations XPSC[5:0] and XACL[5:0] can be chosen different to the mentioned equations or Table 14, as the H-phase scaling is able to scale in the range from zooming up by factor 3 to downscale by a factor of $^{1024}/_{8191}$.

Equation for XPSC[5:0] calculation is: XPSC[5:0] = lower integer of $\frac{Npix_in}{Npix_out}$

where,

the range is 1 to 63 (**value 0 is not allowed**);

Npix_in = number of input pixel, and

Npix_out = number of desired output pixel over the complete horizontal scaler.

The use of the prescaler results in a XACL[5:0] and XC2_1 dependent gain amplification.
The amplification can be calculated according to the equation:

DC gain = (XC2_1 + 1) $\times$ XACL[5:0] + (1 – XC2_1).

It is recommended to use sequence lengths and weights, which results in a DC gain amplification of 2^N, as these amplitudes can be renormalized by the XDCG[2:0] controlled $\frac{1}{2^N}$ shifter of the prescaler.

Other amplifications have to be normalized by using the following BCS control circuitry according to the equation:

CONT[7:0] = SATN[7:0] = lower integer of $\frac{2^{XDCG[2:0]}}{DC\ gain \times 64}$

Where: $2^{XDCG[2:0]} \geq$ DC gain

In these cases the prescaler has to be set to an overall gain of ≤1, e.g. for an accumulation sequence of ‘1 + 1 + 1’ (XACL[5:0] = 2 and XC2_1 = 0), XDCG[2:0] must be set to ‘010’, this equals $^1/_4$ and the BCS has to amplify the signal to $^4/_3$ (SATN[7:0] and CONT[7:0] value = lower integer of $^4/_3 \times 64$).

The use of XACL[5:0] is XPSC[5:0] dependent. XACL[5:0] must be < 2 $\times$ XPSC[5:0].

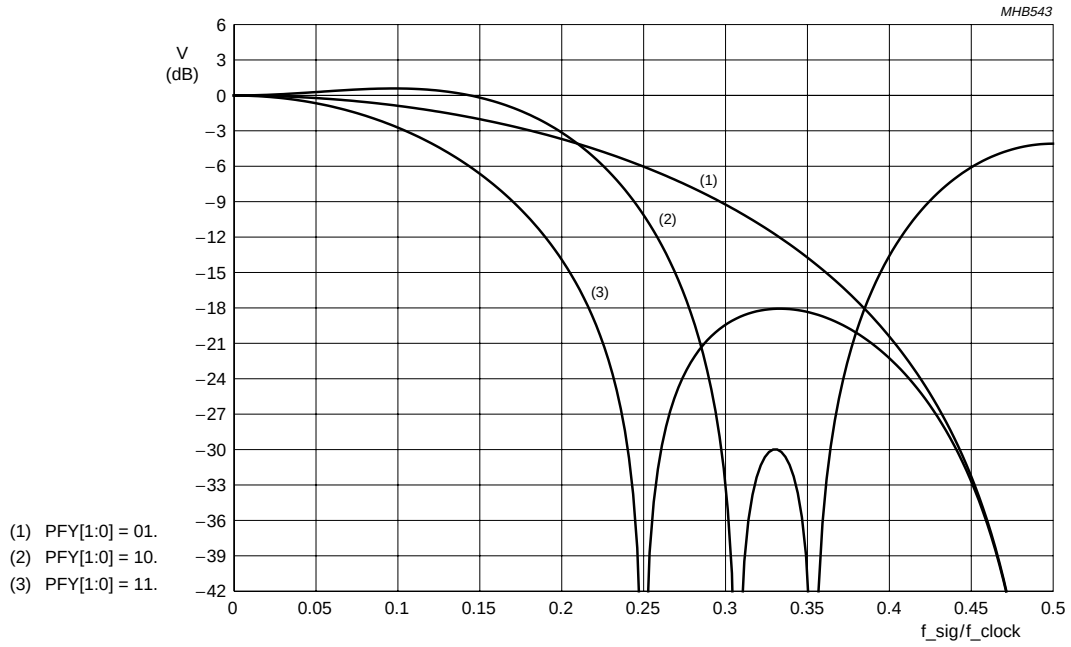
XACL[5:0] can be used to find a compromise between bandwidth (sharpness) and alias effects.

Figs 27 and 28 show some resulting frequency characteristics of the prescaler.

Table 14 shows the recommended prescaler programming. Other programming settings, than given in Table 14, may result in better alias suppression, but the resulting DC gain amplification needs to be compensated by the BCS control

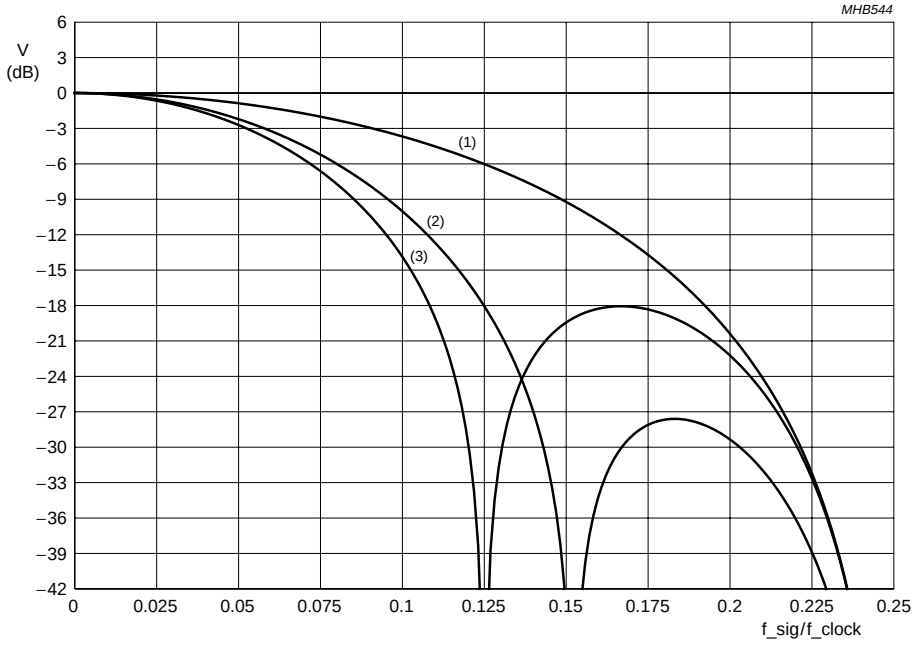
For example, if XACL[5:0] = 5, XC2_1 = 1, then the DC gain = 10 and the required XDCG[2:0] = 4.

The horizontal source acquisition timing and the prescaling ratio is identical for both the luminance path and chrominance path, but the FIR filter settings can be defined differently in the two channels.



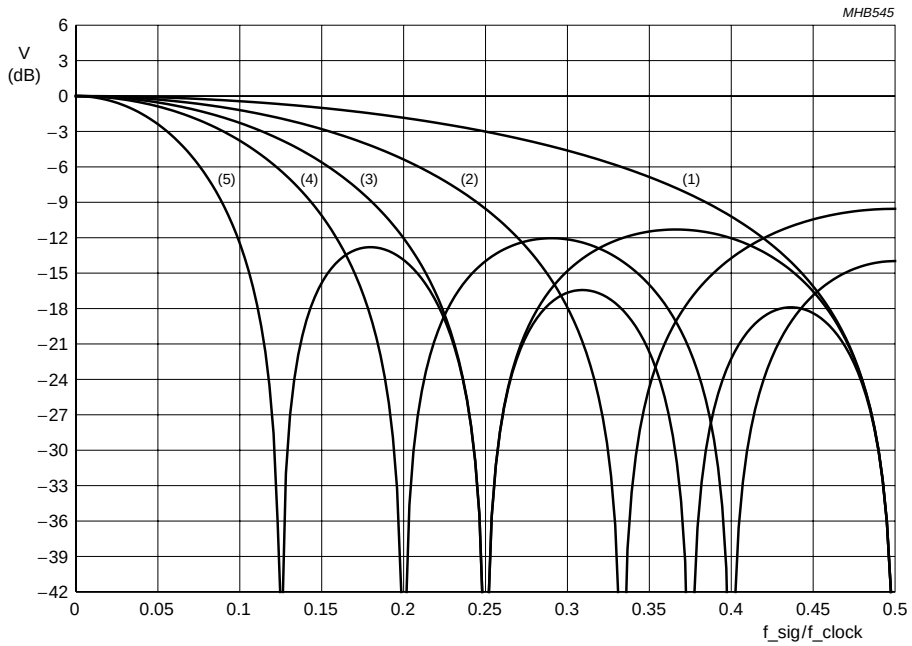
(1) PFY[1:0] = 01.
(2) PFY[1:0] = 10.
(3) PFY[1:0] = 11.

Fig.25 Luminance prefilter characteristic.



(1) PFUV[1:0] = 01.
(2) PFUV[1:0] = 10.
(3) PFUV[1:0] = 11.

Fig.26 Chrominance prefilter characteristic.

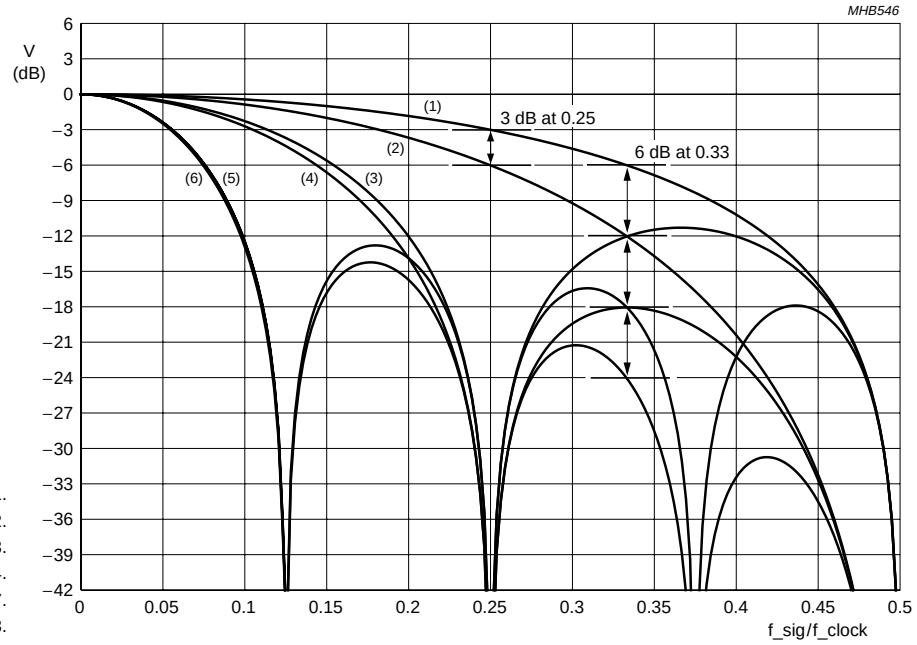


XC2_1 = 0; Zero's at

$$f = n \times \frac{1}{XACL + 1}$$

with XACL = (1), (2), (3), (4) or (5)

Fig.27 Examples for prescaler filter characteristics: effect of increasing XACL[5:0].



(1) XC2_1 = 0 and XACL[5:0] = 1.
(2) XC2_1 = 1 and XACL[5:0] = 2.
(3) XC2_1 = 0 and XACL[5:0] = 3.
(4) XC2_1 = 1 and XACL[5:0] = 4.
(5) XC2_1 = 0 and XACL[5:0] = 7.
(6) XC2_1 = 1 and XACL[5:0] = 8.

Fig.28 Examples for prescaler filter characteristics: setting XC2_1 =1.

Table 14 XACL[5:0] example of usage

PRESCALE RATIO	XPSC [5:0]	RECOMMENDED VALUES						FIR PREFILTER PFY (P_B-P_R)
		FOR LOWER BANDWIDTH REQUIREMENTS			FOR HIGHER BANDWIDTH REQUIREMENTS			
		XACL[5:0]	XC2_1	XDCG[2:0]	XACL[5:0]	XC2_1	XDCG[2:0]	
1	1	0	0	0	0	0	0	0 to 2
1/2	2	2	1	2	1	0	1	0 to 2
		(1 2 1) × 1/4(1)			(1 1) × 1/2(1)			
1/3	3	4	1	3	3	0	2	2
		(1 2 2 2 1) × 1/8(1)			(1 1 1 1) × 1/4(1)			
1/4	4	7	0	3	4	1	3	2
		(1 1 1 1 1 1 1 1) × 1/8(1)			(1 2 2 2 1) × 1/8(1)			
1/5	5	8	1	4	7	0	3	2
		(1 2 2 2 2 2 2 2 1) × 1/16(1)			(1 1 1 1 1 1 1 1) × 1/8(1)			
1/6	6	8	1	4	7	0	3	3
		(1 2 2 2 2 2 2 2 1) × 1/16(1)			(1 1 1 1 1 1 1 1) × 1/8(1)			
1/7	7	8	1	4	7	0	3	3
		(1 2 2 2 2 2 2 2 1) × 1/16(1)			(1 1 1 1 1 1 1 1) × 1/8(1)			
1/8	8	15	0	4	8	1	4	3
		(1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1) × 1/16(1)			(1 2 2 2 2 2 2 2 1) × 1/16(1)			
1/9	9	15	0	4	8	1	4	3
		(1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1) × 1/16(1)			(1 2 2 2 2 2 2 2 1) × 1/16(1)			
1/10	10	16	1	5	8	1	4	3
		(1 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 1) × 1/32(1)			(1 2 2 2 2 2 2 2 1) × 1/16(1)			
1/13	13	16	1	5	16	1	5	3
1/15	15	31	0	5	16	1	5	3
1/16	16	32	1	6	16	1	5	3
1/19	19	32	1	6	32	1	6	3
1/31	31	32	1	6	32	1	6	3
1/32	32	63	1	7	32	1	6	3
1/35	35	63	1	7	63	1	7	3

Note

1. Resulting FIR function.

8.3.2.2 Horizontal fine scaling (variable phase delay filter; subaddresses A8H to AFH and D8H to DFH)

The horizontal fine scaling (VPD) should operate at scaling ratios between $^1/_2$ and 2 (0.8 and 1.6), but can also be used for direct scaling in the range from $^1/_{7.999}$ to (theoretical) zoom 3.5 (restriction due to the internal data path architecture), without prescaler.

In combination with the prescaler a compromise between sharpness impression and alias can be found, which is signal source and application dependent.

For the luminance channel a filter structure with 10 taps is implemented, and for the chrominance a filter with 4 taps.

Luminance and chrominance scale increments (XSCY[12:0] A9H[4:0]A8H[7:0] and XSCC[12:0] ADH[4:0]ACH[7:0]) are defined independently, but must be set in a 2 : 1 relationship in the actual data path implementation. The phase offsets XPHY[7:0] AAH[7:0] and XPHC[7:0] AEH[7:0] can be used to shift the sample phases slightly. XPHY[7:0] and XPHC[7:0] covers the phase offset range 7.999T to $^1/_{32}$T. The phase offsets should also be programmed in a 2 : 1 ratio.

The underlying phase controlling DTO has a 13-bit resolution.

According to the equations $XSCY[12:0] = 1024 \times \frac{Npix_in}{XPSC[5:0]} \times \frac{1}{Npix_out}$ and $XSCC[12:0] = \frac{XSCY[12:0]}{2}$

the VPD covers the scale range from 0.125 to zoom 3.5. VPD acts equivalent to a polyphase filter with 64 possible phases. In combination with the prescaler, it is possible to get very accurate samples from a highly anti-aliased integer downscaled input picture.

8.3.3 VERTICAL SCALING

The vertical scaler of the SAA7115 consists of a line FIFO buffer for line repetition and the vertical scaler block, which implements the vertical scaling on the input data stream in 2 different operational modes from theoretical zoom by 64 down to icon size $^1/_{64}$. The vertical scaler is located between the BCS and horizontal fine scaler, so that the BCS can be used to compensate the DC gain amplification of the ACM mode (see Section 8.3.3.2) as the internal RAMs are only 8-bit wide.

8.3.3.1 Line FIFO buffer (subaddresses 91H, B4H and C1H, E4H)

The line FIFO buffer is a dual ported RAM structure for 768 pixels, with asynchronous write and read access. The line buffer can be used for various functions, but not all functions may be available simultaneously.

The line buffer can buffer a complete unscaled active video line or more than one shorter lines (only for non-mirror mode), for selective repetition for vertical zoom-up.

For zooming up 240 lines to 288 lines e.g., every fourth line is requested (read) twice from the vertical scaling circuitry for calculation.

For conversion of a 4 : 2 : 0 or 4 : 1 : 0 input sampling scheme (MPEG, video phone, Indeo YUV-9) to ITU like sampling scheme 4 : 2 : 2, the chrominance line buffer is read twice or four times, before being refilled again by the source. It has to be preserved by means of the input acquisition window definition, so that the processing starts with a line containing luminance and chrominance information for 4 : 2 : 0 and 4 : 1 : 0 input. The bits FSC[2:1] 91H[2:1] define the distance between the Y/C lines. In the case of 4 : 2 : 2 and 4 : 1 : 1 FSC2 and FSC1 have to be set to ‘00’.

The line buffer can also be used for mirroring, i.e. for flipping the image left to right, for the vanity picture in video phone applications (bit YMIR[B4H[4]]). In mirror mode only one active prescaled line can be held in the FIFO at a time.

The line buffer can be utilized as an excessive pipeline buffer for discontinuous and variable rate transfer conditions at the expansion port or image port.

Remark to 4 : X : 0 input from X-port: These input streams need to look like regular 4:2:2 input and are formatted to the internal 16 bit YUV format. At it’s input port the line fifo only ignores 1 of 2, resp. 3 of 4 chrominance lines, where FSC defines the skipping sequence.

8.3.3.2 Vertical scaler (subaddresses B0H to BFH and E0H to EFH)

Vertical scaling of any ratio from 64 (theoretical zoom) to $^{1}/_{63}$ (icon) can be applied.

The vertical scaling block consists of another line delay, and the vertical filter structure, that can operate in two different modes; Linear Phase Interpolation (LPI) and accumulation (ACM) mode. These are controlled by YMODE[B4H[0]]:

- **LPI mode**: In LPI mode (YMODE = 0) two neighbouring lines of the source video stream are added together, but weighted by factors corresponding to the vertical position (phase) of the target output line relative to the source lines. This linear interpolation has a 6-bit phase resolution, which equals 64 intra line phases. It interpolates between two consecutive input lines only. LPI mode should be applied for scaling ratios around 1 (down to $^{1}/_{2}$), **it must be applied for vertical zooming**.
- **ACM mode**: The vertical Accumulation (ACM) mode (YMODE = 1) represents a vertical averaging window over multiple lines, sliding over the field. This mode also generates phase correct output lines. The averaging window length corresponds to the scaling ratio, resulting in an adaptive vertical low-pass effect, to greatly reduce aliasing artefacts. ACM can be applied for downscales only from ratio 1 down to $^{1}/_{64}$. ACM results in a scale dependent **DC gain amplification**, which has to be precorrected by the BCS control of the scaler part.

The phase and scale controlling DTO calculates in 16-bit resolution, controlled by parameters YSCY[15:0] B1H[7:0] B0H[7:0] and YSCC[15:0] B3H[7:0] B2H[7:0], continuously over the entire filed. A start offset can be applied to the phase processing by means of the parameters YPY3[7:0] to YPY0[7:0] in BFH[7:0] to BCH[7:0] and YPC3[7:0] to YPC0[7:0] in BBH[7:0] to B8H[7:0]. The start phase covers the range of $^{255}/_{32}$ to $^{1}/_{32}$ lines offset.

By programming appropriate, opposite, vertical start phase values (subaddresses B8H to BFH and E8H to EFH) depending on odd/even field ID of the source video stream and A/B-page cycle, frame ID conversion and field rate conversion are supported (i.e. de-interlacing, re-interlacing).

Figs 29 and 30 and Tables 15 and 16 describe the use of the offsets.

Remark: The vertical start phase, as well as scaling ratio are defined independently for luminance and chrominance channel, but must be set to the same values in the actual implementation for accurate 4 : 2 : 2 output processing.

The vertical processing communicates on its input side with the line FIFO buffer. The scale related equations are:

- Scaling increment calculation for ACM and LPI mode, downscale and zoom:

  YSCY[15:0] and YSCC[15:0] = lower integer of $\left(1024 \times \frac{\text{Nline_in}}{\text{Nline_out}}\right)$

- BCS value to compensate DC gain in ACM mode (contrast and saturation have to be set):

  CONT[7:0] A5H[7:0] respectively SATN[7:0] A6H[7:0] = lower integer of $\left(\frac{\text{Nline_out}}{\text{Nline_in}} \times 64\right)$,

  or = lower integer of $\left(\frac{1024}{\text{YSCY[15:0]}} \times 64\right)$

8.3.3.3 Use of the vertical phase offsets

As described in Section 8.3.1.3, the scaler processing may run randomly over the interlaced input sequence (see parameters STRC[1:0], FSKP[2:0] and RPTSK). Additionally the interpretation and timing between ITU 656 field ID and real-time detection by means of the state of H-sync at the falling edge of V-sync may result in different field ID interpretation.

A vertically scaled interlaced output also gets a larger vertical sampling phase error, if the interlaced input fields are processed, without regard to the actual scale at the starting point of operation (see Fig.29).

For correct interlaced processing the vertical scaler must be used with respect to the interlace properties of the input signal and, if required, for conversion of the field sequences.

Four events should be considered, they are illustrated in Fig.30.

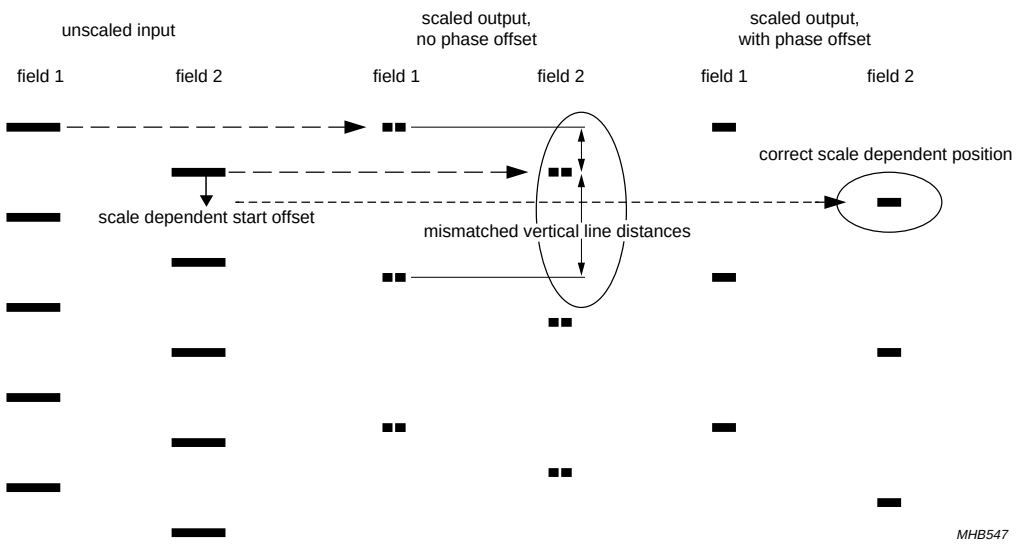
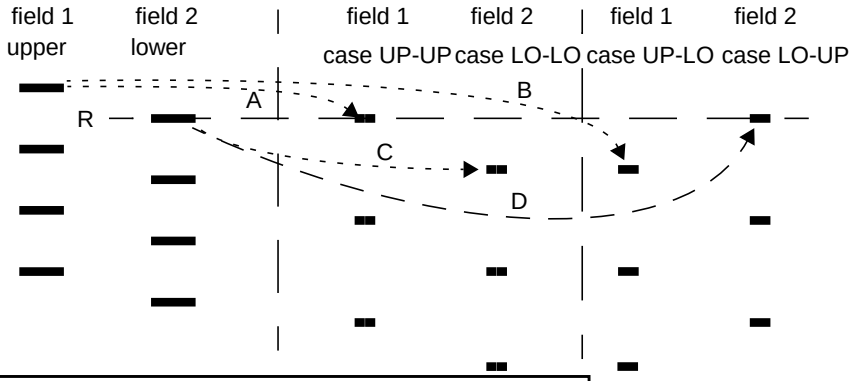


Fig.29 Basic problem of interlaced vertical scaling (example: downscale $^{3}/_{5}$).

Example: interlace vertical scaling down to 3 / 5, with field conversion



Note: Offset = 1024 / 32 = 32 = 1 line shift

R = reference position for upper output field
A = 1/2 input line shift = 16
B = 1/2 input line shift +1/2 scale increment = YSCY/64 + 16
C = 1/2 scale increment= YSCY / 64
D = no offset = 0

Fig.30 Derivation of the phase related equations

In Tables 15 and 16 PHO is a usable common phase offset.

It should be noted that the equations of Fig.30 produce an interpolated output, also for the unscaled case, as the geometrical reference position (R) for all conversions is the position of the first line of the lower field (see Table 15).

If there is no need for UP-LO and LO-UP conversion and the input field ID is the reference for the back-end operation, then it is UP-LO = UP-UP and LO-UP = LO-LO and the $\frac{1}{2}$ line phase shift (PHO + 16) can be skipped.
This case is listed in Table 16.

The SAA7115 supports 4 phase offset registers per task and component (luminance and chrominance). The value of 20H represents a phase shift of one line.

The registers are assigned to the following events; e.g. subaddresses B8H to BBH:

- B8H: 00 = input field ID 0, task status bit 0 (toggle status, see Section 8.3.1.3)
- B9H: 01 = input field ID 0, task status bit 1
- BAH: 10 = input field ID 1, task status bit 0
- BBH: 11 = input field ID 1, task status bit 1.

Depending on the input signal (interlaced or non-interlaced) and the task processing 50 Hz or field reduced processing with one or two tasks (see examples in Section 8.3.1.3), other combinations may also be possible, but the basic equations are the same.

Table 15 Examples for vertical phase offset usage: global equations (referring to reference position R)

INPUT FIELD UNDER PROCESSING	OUTPUT FIELD INTERPRETATION	USED ABBREVIATION	EQUATION FOR PHASE OFFSET CALCULATION (DECIMAL VALUES)
Upper input lines	upper output lines	UP-UP	PHO + 16
Upper input lines	lower output lines	UP-LO	$PHO + \frac{YSCY[15:0]}{64} + 16$
Lower input lines	upper output lines	LO-UP	PHO
Lower input lines	lower output lines	LO-LO	$PHO + \frac{YSCY[15:0]}{64}$

Table 16 Vertical phase offset usage; assignment of the phase offsets for OFIDC[90[6]] = 0, scaler input field ID as output ID

assumed backend interprets output field ID at “0” as upper output lines			
detected input field ID	**task status bit**	**vertical phase offset**	**equation to be used (values)**
0 = upper lines	0	YPY(C)0	UP-UP (PHO)
0 = upper lines	1	YPY(C)1	UP-UP (PHO)
1 = lower lines	0	YPY(C)2	LO-LO (PHO + YSCY / 64 - 16)
1 = lower lines	1	YPY(C)3	LO-LO (PHO + YSCY / 64 - 16)

Notes

1. referring to the upper input field as reference position, a value of 16 is to be substracted from the global equations of table 15.

Table 17 Vertical phase offset usage: Assignment of the phase offsets for OFIDC[90[6]] = 1

detected input field ID	task status bit	vertical phase offset	backend interprets output field ID “0” as upper lines; equation to be used	backend interprets output field ID “1” as upper lines; equation to be used
0 = upper lines	0	YPY(C)0	UP-UP	UP-LO
0 = upper lines	1	YPY(C)1	UP-LO	UP-UP
1 = lower lines	0	YPY(C)2	LO-UP	LO-LO
1 = lower lines	1	YPY(C)3	LO-LO	LO-UP

8.4 VBI-data decoder and capture (subaddresses 40H to 7FH)

The SAA7115 contains a versatile VBI-data decoder and the option of reading back sliced VBI data for low bitrate standards.

8.4.1 VBI Data Slicer

The circuitry recovers the actual clock phase during the clock run-in period, slices the data bits with the selected data rate, and groups them into bytes. The result is buffered into a dedicated VBI-data FIFO with a capacity of 2×56 bytes (2×14 Dwords).

The VBI data slicing is controlled by the programming registers 40H to 5DH. Register 40H and 58H are controlling the slicing process itself. The Line Control Registers (LCR registers) 41H to 57H are defining the data type (VBI data standard) to be decoded. The data type is specified on a line by line basis for the lines two to 23 separately for even and odd field and depends additionally on the detected video standard (i.e. whether the incoming video is a 50Hz / 625 lines or 60Hz / 525 lines signal).

The definition for line control register LCR24 is valid for the rest of the corresponding field, normally no text data (video data) should be selected there (LCR24_[7:0] = FFH) to stop the activity of the VBI-data slicer during active video.
The supported VBI-data standards are shown in Table 18 for 60Hz / 525 lines signals and 19 for 50Hz / 625 lines signals.

Table 18 60Hz / 525 Lines VBI Data types supported by the data slicer block

Data type		**60Hz / 525 Lines VBI Data Standards**					
No.	**binary**	**DESCRIPTION**	**Data rate (Mbits/s)**	**FRAMING CODE**	**FRAMING CODE WINDOW**	**Hamming check**	**Decoder output data format**
0	0000	do not acquire (active video)	-	-	-	-	Y-C_B-C_R 4:2:2
1	0001	US Teletext (WST525)	5.7272	0x27	WST525	always	raw data
2	0010	NABTS	5.7272	programmable	NABTS	optional	raw data
3	0011	Moji	5.7272	programmable (1)	MOJI	-	raw data
4	0100	US Closed Caption (CC525, Line21)	0.503	001 binary	CC525	-	raw data
5	0101	US Wide Screen Signalling (WSS525, CGMS)	0.447443	10 binary	WSS525	-	raw data
6	0110	VITC525	1.7898	10 binary	VITC525	-	raw data
7	0111	Gemstar2x	1.007	0x4ED	4ED H	-	raw data
8	1000	Gemstar1x	0.503	001 binary		-	raw data
9	1001	reserved	-	-	-	-	reserved
10	1010	Open1 (5 MHz)	5	programmable	8-16us	-	raw data
11	1011	Open2 (5,7272 MHz)	5.7272	programmable	8-16us	-	raw data
12	1100	reserved	-	-	-	-	reserved
13	1101	do not acquire (RAW)	-	-	-	-	raw data
14	1110	do not acquire (Test)	-	-	-	-	reserved
15	1111	do not acquire (active video)	-	-	-	-	Y-C_B-C_R 4:2:2

1. should be set to 0x47 for Moji

Table 19 50Hz / 625 Lines VBI Data types supported by the data slicer block

Data type		50Hz / 625 Lines VBI Data Standards					
No.	**binary**	**DESCRIPTION**	**Data rate (Mbits/s)**	**FRAMING CODE**	**FRAMING CODE WINDOW**	**Hamming check**	**Decoder output data format**
0	0000	do not acquire (active video)	-	-	-	-	Y-C_B-C_R 4:2:2
1	0001	European Teletext (WST625), Chinese Teletext (CCST625)	6.9375	0x27	WST625	always	raw data
2	0010	Euro Teletext with progammable Framing Code	6.9375	programmable	gen_text	optional	raw data
3	0011	reserved	-	-	-	-	raw data
4	0100	Euro Closed Caption (CC625)	0.500	001 binary	CC625	-	raw data
5	0101	Euro Wide Screen Signalling (WSS625)	5	0x1E3C1F	WSS625	-	raw data
6	0110	VITC625	1.8125	10 binary	VITC625	-	raw data
7	0111	VPS	5	0x9951	VPS	-	raw data
8	1000	reserved	-	-	-	-	raw data
9	1001	reserved	-	-	-	-	reserved
10	1010	Open1 (5 MHz)	5	programmable	8-16us	-	raw data
11	1011	Open2 (5,7272 MHz)	5.7272	programmable	8-16us	-	raw data
12	1100	reserved	-	-	-	-	reserved
13	1101	do not acquire (RAW)	-	-	-	-	raw data
14	1110	do not acquire (Test)	-	-	-	-	reserved
15	1111	do not acquire (active video)	-	-	-	-	Y-C_B-C_R 4:2:2

The adjustment of the slicer processing to the input signal source is defined by the programming registers 59h to 5BH, There are programmable offsets in the horizontal and vertical direction available: parameters HOFF[10:0] 5BH[2:0] 59H[7:0], VOFF[8:0] 5BH[4] 5AH[7:0], FOFF[5BH[7]] and VEP[5BH[5]]).

Contrary to the scaler counting scheme, the slicer offsets define the position of the H and V trigger events related to the processed video field. The trigger events are the falling edge of HREF and the falling or rising edge of V123 (defined by VEP[5BH[5]]) from the decoder processing part.

Note:
The field ID, used for the slicers data packing, is taken at the internal pixel ‘1’ and line ‘1’ position. Hence for correct line counting according ITU656 and for 60 Hz input signals (see Fig.23), the old value of the field ID is taken as ID reference. This has effect on the I2C read back registers, on the LCR table, the LCR controlled field ID generation and the internal header information of the slicers output stream.
For consistent ID interpretation, the vertical offset parameter VOFF for NTSC has to be set to 0x03. For this case the LCR table covers the range from line 5 to 27 and line 21 corresponds to LCR18.

The relationship of these programming values to the input signal and the recommended values is outlined in table 7 to table 10.

The register SLDMOD[4:0] 5DH[4:0] defines the Slicer Data Output Mode at the I-Port of the SAA7115.
This register enables the VBI output and defines the mode of data insertion into the I-port data stream.

Status Information can be read form register 5EH.

8.4.2 I²C Readback of sliced VBI data

The I²C Readback unit offers readback for the following VBI data standards via the I²C bus (subaddresses 66H 7FH):

- 60Hz / 525 lines VBI data standards
  - US Closed Caption (CC525):
    1 byte header + 2 x 2 bytes payload
  - Copy Generation Management System (CGMS, US Wide Screen Signalling (WSS525)):
    1 byte header + 2 x 3 bytes payload
  - Gemstar1x:
    1 byte header + 2 x 2 bytes payload
  - Gemstar2x:
    1 byte header + 2 x 4 bytes payload
- 50Hz / 625 lines VBI data standards
  - European Closed Caption (CC625):
    1 byte header + 2 x 2 bytes payload
  - European Wide Screen Signalling (WSS625, majority decoded and be-phase decoded):
    1 byte header + 2 x 2 bytes payload

For each VBI data standard the amount of data of one frame (one line per field) and a one byte header can be stored. The I2C Readback registers for Wide Screen Signalling and Closed Caption are shared for 60Hz / 525 lines VBI data standards and 50Hz / 625 lines VBI data standards. In case of decoding WSS625 this data is sore to the same registers than decoded WSS525 data with the third payload byte of each line left unconsidered.

The one byte header delivers decoding error status and the current update status separately for each field as well as a free running 4 bit field counter as reference information, to be able to detect multiple read data or loss of data (refer to table 20)

Table 20 Structure of the I²C readback header

BIT	HEADER DESCRIPTION
7	data of odd field (field_id = 0) is incomplete, i.e. not updated since last read, if set.
6	one or more data bytes of odd field (field_id = 0) are erroneous (data valid signal became inactive), if set.
5	data of even field (field_id = 1) is incomplete. i.e. not updated since last read, if set.
4	one or more data bytes of even field (field_id = 1) are erroneous (data valid signal became inactive), if set.
3:1	field_count (counts up, field identifier represents the LSB)

The I2C Readback unit guarantees consistency between header information and sliced data using internal mirror-registers for the sliced data, which updated at the same time the header is accessed for reading via the I²C bus. I.e. The I²C Readback header must be always accessed before getting the latest data. In case the sliced data has been read already or is being updated at the time the header is accessed for reading, this will be signalled in the header bits 7 and 5 for each field separately.

Additionally to the read access to the header the data coming from VBI data slicer is copied into one of the mirror registers only, if the following additional conditions are satisfied:

- The data type as set in the LCR register must equal to the one of the sampled data.
- The data must be indicated as valid data.
- The maximum number of data bytes per line (CC, WSS625, Gemstar1x:2, CGMS:3, Gemstar2x: 4) is not exceeded

If there is less data in a line than expected for the appropriate data type, this is marked as an error inside the header. If there is more data in a line, this does not lead to an error, and the additional data bytes are neglected.

8.4.3 Sliced VBI Data Output at the I-Port

The following sections are describing the sliced VBI payload data output at the I-Port. Chapter 8.5 describes the output modes for VBI data at the I-Port.

8.4.3.1 Euro WST, US WST and NABTS Data

Euro WST, US WST and NABTS Data are stored in transmission order; first received bit becomes LSB of byte in payload.

8.4.3.2 WSS 625 Data

Each payload byte contains are a group of 6 bits (LSB aligned) representing a single symbol (a WSS625 bit) bi-phase coded and then oversampled at 3 times the baud rate. To decode the individual bits, it is usual to take a majority decision on each group of 3 bits (majority of 0s or 1s), then compare the first and second three-bit groups to do bi-phase decoding.

8.4.3.3 WSS 525 Data

The received data contains 20 bits including 6 bits of CRC code; all 20 bits are packed into 3 bytes (LSB aligned in byte 3) and written to the packet with the first received bit becoming LSB of the first payload byte. CRC checking is performed on the received data (indicated in in the MSB of byte 3; set to ‘0’ in case of no errors). Unused bytes are set to zero.

8.4.3.4 VPS Data

Each pair of two consecutive bits in a payload data byte is a single symbol, biphase coded. 01 represents a 1 symbol,10 represents a 0 symbol. 00 and 11 are biphase errors. The data can be decoded in minimum processor time by using a look-up table (256 bytes) using the received data as index, which gives the correct decoded biphase data in the ls 4 bits of each byte and 4 corresponding error flags; e.g.: a stored byte with hex value 0x1B (binary 00.01.10.11) would be decoded as 1001.0100 (i.e.: the middle two pairs 01 and 10 decode correctly to 1 and 0, but the outer two pairs 00 and 11 are errors).

8.4.3.5 Closed Caption

Closed Caption is stored in transmission order - first received bit becomes LSB of the first payload byte.

8.4.3.6 Moji Data

The Moji Data Line contains 272 bits, made up of a 14-bit prefix, 22 Information Data bytes (176 bits) and an 82-bit Parity Check. The captured bits are constructed into bytes, LSB first, in transmission order, but the first payload byte of the packet contains only 6 bits of trans-mitted data in bits 2 -7. Bit 2 corresponds to the first transmitted bit; bits 1 and 0 are filled with zeros.

This is done in order to align the Information Data bytes to byte boundaries in the constructed data packet. It also means that the last data byte in the packet contains only 2 transmitted bits (in positions 0 - 1) - the remaining 6 bits are undefined and should be ignored.

8.4.3.7 VITC Data

The VITC data line in both 625- and 525-line video formats contains 90 bits, which can be divided into nine 10-bit groups. The first two bits of each group are defined as Synchronising Bits, and consist of a fixed 1 followed by a fixed 0 . These Synchronising Bits are **excluded** from the data packet constructed by the VBI Slicer, leaving exactly nine 8-bit bytes of useful data. The payload bytes are presented in transmission order, with the LSB of each corresponding to the first transmit-ted bit.

Note that this behaviour is different from the VBI Data Slicer of the predecessors of the SAA7115 that supported the VITC data types.

8.4.3.8 Open Data Types

The Open data types are provided primarily to allow capture of low bitrate data types that are not specifically supported by the Data Capture Unit, by oversampling the transmitted data and leaving software to extract the individual bytes.

Acquisition starts when a match is found for the programmable framing code; bytes are then captured, LSB first, in transmission order at the specified bit-rate. The search window for the framing code is open between approximately 8 and 16ms into the line, referenced to the falling edge of the H-Sync pulse. The number of bytes captured in the open data types depends on when in this period the framing code match is found: the maximum numbers of bytes to be received are 38 Data Bytes for Open1 and 43 Bytes for Open2.They are the maximum assuming earliest possible detection of the framing code. If the framing code is detected any later, fewer bytes may be captured; also, data capture may extend into the region of the following line, in which case the last few data bytes in the packet will be meaningless. It is left up to the software to process the appropriate amount of data from the packet, as defined by the application for which the open data type is being used.

8.5 Image port output interface (subaddresses 84H to 87H)

The output interface consists of a FIFO for video and for sliced text data, an arbitration circuit, which controls the mixed transfer of video and sliced text data over the I-port and a decoding and multiplexing unit, which generates the 8 or 16-bit wide output data stream and the accompanied reference and supporting information.

The clock for the output interface can be derived from an internal clock (decoder or X-port), from the second internal PLL set (PLL2 and CGC2) or an externally provided clock which is appropriate for e.g. VGA and frame buffer. The clock can be up to 33 MHz.

The scaler provides the following video related timing reference events (signals), which are available on pins as defined by subaddresses 84H and 85H:

- Output field ID
- Start and end of vertical active video range
- Start and end of active video line
- Data qualifier or gated clock
- Actually activated programming page (if CONLH is used)
- Threshold controlled FIFO filling flags (empty, full, filled)
- Sliced data marker.

The data stream at the scaler output is accompanied by a data valid flag (or data qualifier) or is transported using a gated clock. The discontinuous output data after the scaling process can be output as they occur or the data may be packed to continuous output lines by means of a trigger mechanism, which is controlled by a separate pulse generator (see addresses F5H to FBH).
Clock cycles with invalid data on the I-port data bus (including the HPD pins in 16-bit output mode) are handled in two different ways (controlled by INS80 86H[7]). As before, invalid cycles may be marked with 00H, but additionally a blanking value insertion (80H and 10H) as required by ITU656 is now implemented.

The output interface also arbitrates the transfer between scaled video data and sliced text data over the I-port output. The bits SLDOM (5DH) and VITX (86H) are used to control the arbitration.

As a further operation the serialization of the internal 32-bit Dwords to 8-bit or optional 16-bit output, as well as the insertion of the extended ITU 656 codes (SAV/EAV for video data, ANC or SAV/EAV codes for sliced text data) are done here.

For handshake with the VGA controller, or other memory or bus interface circuitry, programmable FIFO flags are provided (see Section 8.5.2).

8.5.1 SCALER OUTPUT FORMATTER (SUBADDRESSES 93H AND C3H)

The output formatter organizes the packing into the output FIFO. The following formats are available: Y-C_B-C_R 4 : 2 : 2, Y-C_B-C_R 4 : 1 : 1, Y-C_B-C_R 4 : 2 : 0, Y-C_B-C_R 4 : 1 : 0, Y only (e.g. for raw samples). The formatting is controlled by FSI[2:0] 93H[2:0], FOI[1:0] 93H[4:3] and FYSK[93H[5]].

The data formats are defined on Dwords, or multiples, and are similar to the video formats as recommended for PCI multimedia applications, but planar formats are not supported.

FSI[2:0] defines the horizontal packing of the data, FOI[1:0] defines how many Y only lines are expected, before a Y/C line will be formatted. If FYSK is set to logic 0 preceding Y only lines will be skipped, and the output will always start with a Y/C line.

Additionally the output formatter limits the amplitude range of the video data (controlled by ILLV[85H[5]]); see Table 23.

Table 21 Byte stream for different output formats

OUTPUT FORMAT	BYTE SEQUENCE FOR 8-BIT OUTPUT MODES													
Y-CB-CR 4 : 2 : 2	CB0	Y0	CR0	Y1	CB2	Y2	CR2	Y3	CB4	Y4	CR4	Y5	CB6	Y6
Y-CB-CR 4 : 1 : 1	CB0	Y0	CR0	Y1	CB4	Y2	CR4	Y3	Y4	Y5	Y6	Y7	CB8	Y8
Y only	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9	Y10	Y11	Y12	Y13

Table 22 Explanation to Table 21

NAME	EXPLANATION
CBn	CB (B – Y) colour difference component, pixel number n = 0, 2, 4 to 718
Yn	Y (luminance) component, pixel number n = 0, 1, 2, 3 to 719
CRn	CR (R – Y) colour difference component, pixel number n = 0, 2, 4 to 718

Table 23 Limiting range on I-port

LIMIT STEP ILLV[85H[5]]	VALID RANGE		SUPPRESSED CODES (HEXADECIMAL VALUE)	
	DECIMAL VALUE	HEXADECIMAL VALUE	LOWER RANGE	UPPER RANGE
0	1 to 254	01 to FE	00	FF
1	8 to 247	08 to F7	00 to 07	F8 to FF

8.5.2 VIDEO FIFO (SUBADDRESS 86H)

The video FIFO at the scaler output contains 32 Dwords. That corresponds to 64 pixels in 16-bit Y-C_B-C_R 4 : 2 : 2 format. But as the entire scaler can act as a pipeline buffer, the actual available buffer capacity for the image port is much higher, and can exceed beyond a video line.

The video FIFO provides 4 internal flags, reporting to what extent the FIFO is actually filled.

These are:

- The FIFO Almost Empty (FAE) flag
- The FIFO Combined Flag (FCF) or FIFO filled, which is set at almost full level and reset, with hysteresis, only after the level crosses below the almost empty mark
- The FIFO Almost Full (FAF) flag
- The FIFO Overflow (FOVL) flag.

The trigger levels for FAE and FAF are programmable by FFL[1:0] 86H[3:2] (16, 24, 28, full) and FEL[1:0] 86H[1:0] (16, 8, 4, empty).

The state of this flag can be seen on the pins IGP0 or IGP1. The pin mapping is defined by subaddresses 84H and 85H (see Section 9.5).

8.5.3 TEXT FIFO

The data of the internal VBI-data slicer is collected in the text FIFO before the transmission over the I-port is requested (normally before the video window starts). It is partitioned into two FIFO sections. A complete line is filled into the FIFO before a data transfer is requested. So normally, one line of text data is ready for transfer, while the next text line is collected. Thus sliced text data is delivered as a block of qualified data, without any qualification gaps in the byte stream of the I-port.

The decoded VBI-data is collected in the dedicated VBI-data FIFO. After capture of a line is completed, the FIFO can be streamed through the image port, preceded by a header, telling line number and standard.

The VBI-data period can be signalled via the sliced data flag on pin IGP0 or IGP1. The decoded VBI-data is lead by the ITU ancillary data header (SLDOM[4:0] 5DH[5:0] at value > 0H and <8H) or by SAV/EAV codes (SLDOM[4:0] 5DH[5:0] at value > 0H and bit D3 = 1). Similar to the global data qualifier on pin IDQ, the sliced data flag frames the transfer of sliced VBI data from the first to the last byte and can be taken to distinguish video from sliced VBI data.

The decoded VBI-data are presented in two different data formats, controlled by bit D0 of SLDOM[4:0].

- SLDOM[0] = 1: values 00H and FFH will be recoded to even parity values 03H and FCH
- SLDOM[0] = 0: values 00H and FFH may occur in the data stream as detected.

8.5.4 VIDEO / TEXT ARBITRATION AND DATA PACKING (SUBADDRESS 86H)

Sliced text data and scaled video data are transferred over the same bus, the I-port. The mixed transfer is controlled by an arbitration circuit and the SLDOM programming.

If the video data are output for the whole field (also during vertical blanking) and the video FIFO does not need to buffer any output pixel, the text data is inserted after the end of a scaled video line, normally during the horizontal blanking interval of the video.

8.5.4.1 VBI insertion in SAV/EAV mode (bit SLDOM[3] = ‘1’)

VBI insertion in SAV/EAV mode (bit SLDOM[3] = ‘1’):
Especially for external devices, which do not recognize the ANC framing of the sliced VBI data and which need to use the SAV/EAV framing, there are now different levels of VBI/video data insertion implemented.
This functionality is controlled by SLDOM [5DH].
Levels of sliced data insertion:
1. SLDOM[4] = 0: video and sliced data, according SLDOM[1], in parallel, VBI data after EAV sequence of a video line
2. SLDOM[4] = 1: sliced data, according SLDOM[1], video output is skipped for these lines

Note:
1.the insertion after EAV and the skipping is only done, if the scaler region overlaps with the LCR defined VBI region.

8.5.4.2 Data Packing (bit IMPAK (86H) and programming of the pulse generator via addr. F5H to FBH)

To make use of the synthesized line locked PLL2 clock and to enable the use of the scaler for a wider application range, it is now possible to retain the output data of the scaler, until a scaled line can be output as a continuous data package. This is done via internal trigger pulses, one for each type of scaler output data (video from page A or B or sliced VBI data). The parameters PGHAPS (video page A), PGHBPS (video page B) and PGHCPS (sliced VBI data) are defining the delay related to the rising edge of the decoders HREF or of the synthesized HREF (generated by the internal pulse generator, see addr. F5H and F6H). The delay is counted in clock cycles and as a rough estimate for the internal buffering level you can take the following equation for the video data streaming.
With
num_buf_pix = number of buffered pixel,
num_buf_lifo = number of pixel buffered in the internal line FIFO
num_buf_fifo = number of pixel buffered in the output FIFO
h_blanking = number of clock cycles during horizontal blanking = 288 (PAL), 276 (NTSC)
sc_run_in = number of clock cycles for scaler running in = about 72 clock cycles for unscaled video

num_buf_pix is about ~= (PGHAPS - h_blanking - sc_run_in) / 2 = num_buf_lifo + num_buf_fifo
Where
num_buf_lifo = 0 for num_buf_pix =< 64 and the maximum value of num_buf_lifo = 768dec
num_buf_fifo = 64 for num_buf_pix > 64

For unscaled video a level around 1/2 of the buffer capacity (num_buf_lifo + num_buf_fifo = 832dec) is recommended. This leads to a PGHAPS value of about ~= 2 x 416 + h_blanking + sc_run_in = 1192 (PAL case)
for the unscaled case.
To be able to align the EAV sequences for different scales and regions, PGHBPS of page B is a separate parameter. The number of bytes per line and region defines, whether PGHBPS is to be programmed differently to PGHAPS.

If all data types are to be mixed and a fixed SAV/EAV pattern is needed, the VBI slicer has to become the timing master for the data packing. To avoid timing shifts in the EAV pattern, the latest point of text line completion defines the earliest packing timing. This is about 48 clocks before rising edge of the decoders HREF. The slicer data need to be shifted to a position later than this point. The latest point in time is defined by the internal video skipping procedure (SLDOM[4] ='1'). Therefore the end of a video line (EAV) need to have a distance of (number of pixels per line) of clock cycles from the mentioned point of text line completion.
Considering the PLL behaviour and for correct video skipping, the recommendation for this situation and EAV alignment for 720 pixel per line and PAL (=1728) is:
1728 - (48+56) - 720 - 1448 = -544 = 1184 >= PGHCPS >= 1728 - (48-20) = 1700
PGHAPS = PGHCPS - num_bytes_per_video_line + num_bytes_per_VBI_package = e.g. 1700 - 1448 + 56 = 308dec

For other clock rates than 27 MHz, the mentioned values need to be scaled according to the clock relations, e.g. 24.545454 MHz would give
1560 - 94 - 640 - 1288 = -462 = 1098 >= PGHCPS >= 1560 - 25 = 1535
PGHAPS = e.g. 500 - 1288 + 51 = -737 = 823dec

8.5.5 Data stream coding and reference signal generation (subaddresses 84H, 85H and 93H)

As H and V reference signals are logic 1, active gate signals are generated, which frame the transfer of the valid output data. As an alternative to the gates, H and V trigger pulses are generated on the rising edges of the gates.

Due to the dynamic FIFO behaviour of the complete scaler path, the output signal timing has no fixed timing relationship to the real-time input video stream. So fixed propagation delays, in terms of clock cycles, related to the analog input cannot be defined.

The data stream is accompanied by a data qualifier. ITU 656 like codes need to be activated by means of the bit ICODE set to '1'.

The behaviour during non qualified clock cycles is defined by the bit INS80 [93H[6]].
With INS80 = '0' the interface behaves like SAA7118/7114 and invalid data cycles are marked with code 00H.

For INS80 ='1' the behaviour changes and inside the scalers output line (scaler H-gate on IGPH = '1'), the data are hold during IDQ ='0'. Outside the scalers output, in the remaining horizontal blanking interval, blanking values are inserted.

As a further option, it is possible to provide the scaler with an external gating signal on pin ITRDY. Thereby making it possible to hold the data output for a certain time and to get valid output data in bursts of a guaranteed length.

The sketched reference signals and events can be mapped to the I-port output pins IDQ, IGPH, IGPV, IGP0 and IGP1. For flexible use the polarities of all the outputs can be modified. The default polarity for the qualifier and reference signals is logic 1 (active).

Table 24 shows the relevant and supported SAV and EAV coding, the figures 34, 33, 35, 36 show some basic pulse diagrams.

Table 24 SAV/EAV codes on I-port

EVENT DESCRIPTION	SAV/EAV CODES ON I-PORT(1) (HEX)				COMMENT
	MSB(2) OF SAV/EAV BYTE = 0		MSB(2) OF SAV/EAV BYTE = 1		
	FIELD ID = 0	FIELD ID = 1	FIELD ID = 0	FIELD ID = 1	
Next pixel is FIRST pixel of any active line	0E	49	80	C7	HREF = active; VREF = active
Previous pixel was LAST pixel of any active line, but not the last	13	54	9D	DA	HREF = inactive; VREF = active
Next pixel is FIRST pixel of any V-blanking line	25	62	AB	EC	HREF = active; VREF = inactive
Previous pixel was LAST pixel of the last active line or of any V-blanking line	38	7F	B6	F1	HREF = inactive; VREF = inactive
No valid data, don't capture and don't increment pointer	00 (only for INS80 = '0')				IDQ pin inactive

Notes

1. The leading byte sequence is: FFH-00H-00H.
2. The MSB of the SAV/EAV code byte is controlled by:
   a) Scaler output data: task A ⇒ MSB = $\overline{\text{CONLH}}$[90H[7]]; task B ⇒ MSB = $\overline{\text{CONLH}}$[C0H[7]].
   b) VBI-data slicer output data: SLDOM[2] = '1' ⇒ MSB = 1; SLDOM[2] = '0'⇒ MSB = 0.

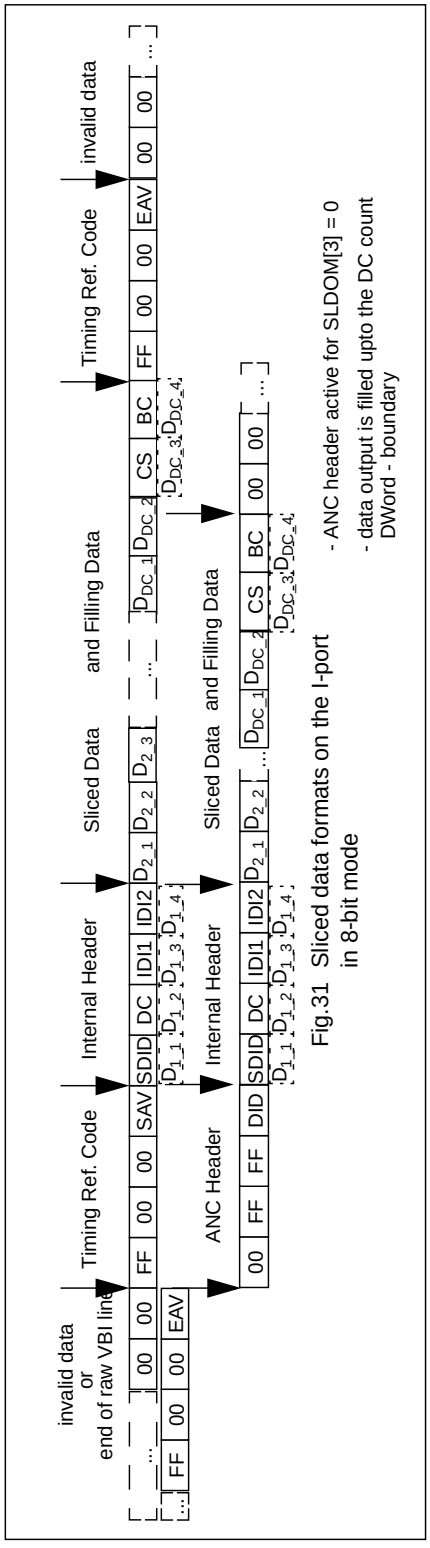


Fig.31 Sliced data formats on the I-port in 8-bit mode

Table 25 Explanation to Fig.31

NAME	EXPLANATION
SAV	start of active data; see Table 26
SDID	sliced data identification: NEP(1), EP(2), SDID5 to SDID0, freely programmable via I2C-bus subaddress 5EH, D5 to D0, e. g. to be used as source identifier
DC	Dword count: NEP(1), EP(2), DC5 to DC0. DC describes the number of succeeding 32-bit words: • For SAV/EAV mode DC is fixed to 12 Dwords (byte value 8CH) • For ANC mode the data count DC can be taken from table 27. The count starts with the SDID byte and ends with BC It should be noted that the number of valid bytes inside the stream can be seen in the BC byte.
IDI1	internal data identification 1: OP(3), FID (field 1 = 0, field 2 = 1), LineNumber8 to LineNumber3 = Dword 1 byte 1; see Table 26
IDI2	internal data identification 2: OP(3), LineNumber2 to LineNumber0, DataType3 to DataType0 = Dword 1 byte 2; see Table 26
Dn_m	Dword number n, byte number m
DDC_4	last Dword byte 4, note: for SAV/EAV framing DC is fixed to 0BH, missing data bytes are filled up; the fill value is A0H
CS	the check sum byte, the check sum is accumulated from the SAV (respectively DID) byte to the DDC_4 byte
BC	number of valid sliced bytes counted from the D1_3 byte
EAV	end of active data; see Table 26

Notes

1. Inverted EP (bit 7); for EP see note 2.
2. Even parity (bit 6) of bits 5 to 0.
3. Odd parity (bit 7) of bits 6 to 0.

Table 26 Bytes stream of the data slicer

NICK NAME	COMMENT	D7	D6	D5	D4	D3	D2	D1	D0
DID, SAV, EAV	subaddress 5DH SLDOM[3:2] = '00'	NEP	EP	0	D4[5DH]	D3[5DH]	D2[5DH]	D1[5DH]	D0[5DH]
	subaddress 5DH SLDOM[3:2] = '01'	NEP(1)	EP(2)	0	1	0	FID(3)	I1(4)	I0(4)
	subaddress 5DH SLDOM[3:2] = '10'	0	FID(3)	V(6)	H(7)	P3	P2	P1	P0
	subaddress 5DH SLDOM[3:2] = '11'	1	FID(3)	V(6)	H(7)	P3	P2	P1	P0
SDID	programmable via subaddress 5EH	NEP	EP	D5[5EH]	D4[5EH]	D3[5EH]	D2[5EH]	D1[5EH]	D0[5EH]
DC(8)		NEP	EP(2)	DC5	DC4	DC3	DC2	DC1	DC0
IDI1		OP(9)	FID(3)	LN8(10)	LN7(10)	LN6(10)	LN5(10)	LN4(10)	LN3(10)
IDI2		OP	LN2(10)	LN1(10)	LN0(10)	DT3(11)	DT2(11)	DT1(11)	DT0(11)
CS	check sum byte	CS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0
BC	valid byte count	OP	0	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0

Notes

1. NEP = inverted EP (see note 2).
2. EP = Even Parity of bits 5 to 0.
3. FID = 0: field 1; FID = 1: field 2.
4. I1 = 0 and I0 = 0: before line 1; I1 = 0 and I0 = 1: lines 1 to 23; I1 = 1 and I0 = 0: after line 23; I1 = 1 and I0 = 1: line 24 to end of field.
5. Subaddress 5DH at 3EH and 3FH are used for ITU 656 like SAV/EAV header generation; recommended value.
6. V = 0: active video; V = 1: blanking.
7. H = 0: start of line; H = 1: end of line.
8. DC = Data Count in Dwords according to the data type.
9. OP = Odd Parity of bits 6 to 0.
10. LN = Line Number.
11. DT = Data Type according to table.

Table 27 Data count (DC) in ANC mode for the various VBI standards

Data type		50Hz / 625 Lines	60Hz / 525 Lines
No.	**binary**	**DATA COUNT (DC) IN 32 BIT DW**	**DATA COUNT (DC) IN 32 BIT DW**
0	0000	nop	nop
1	0001	12	10
2	0010	12	10
3	0011	nop	11
4	0100	2	2
5	0101	5	3
6	0110	5	5
7	0111	8	3
8	1000	nop	3
9	1001	2	2
10	1010	12	12
11	1011	12	12
12	1100	nop	nop
13	1101	nop	nop
14	1110	nop	nop
15	1111	nop	nop

Notes

1. ‘nop’ = no data output

8.6 Scaler Backend clock generation (subaddresses 30H to 3FH)

The SAA7115 incorporates with its Audio clock PLL (APLL), its second digital PLL (PLL2) and its second analog PLL (CGC2) the generation of multiple different clocks for internal and external usage. The following types of clocks can be generated:

- A Backend Clock to drive the Scaler backend including Image Port data output (refer to chapter 8.6.1):
  This is an internal clock which is used for the output of data at the image port (I-Port). It can be defined as a square pixel clock for PAL and NTSC (29,5 MHz and 24,5454 MHz respectively).
- A frame locked Audio Master clock (output at device pin 37, AMCLK; refer to chapter 8.7):
  This clock, which is locked to the frame frequency, ensures that there is always the same predefined number of audio samples associated with a frame. This ensures e.g. synchronous recording of audio and video (e.g. capture to hard disk, or non-linear editing).

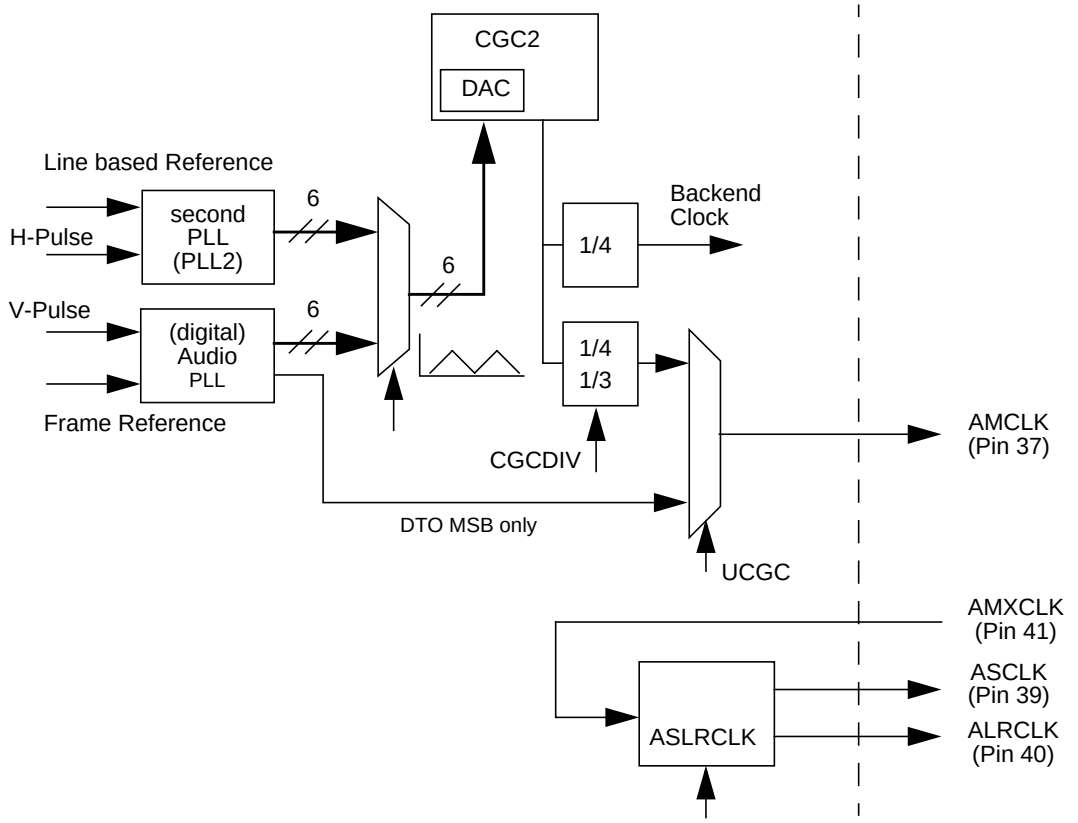


Fig.32 Square Pixel clock and Audio Clock generation

8.6.1 Square Pixel Clock Generation

The SAA7115 is capable to output video data especially in Square Pixel formats. i.e.:

- PAL video line (625 lines per frame) is output with 768/176 continuous active/inactive video pixel at 29.5 MHz clock frequency
- NTSC Video line(525 lines per frame) is output with 640/140 continuous active/inactive video pixel at 24.54 MHz clock frequency.

To generate the clock which allows a continuous data stream at the image port the SAA7115 has implemented the second analog PLL (CGC2) which is stimulated by the line locked second digital PLL (PLL2, alias “Square Pixel” PLL). The CGC2 output clock drives the Scaler Backend and the Pulse Generator to deliver video data with Square Pixel format at the I-Port. To avoid Scaler FIFO overflows/underruns the pixel clock must be phase aligned to the video input signal. Hence the reference of the second digital PLL (PLL2) is a horizontal reference signal obtained from the combfilter decoder or the X-Port input XRH (controlled by SPHSEL, register address F1 H [D1]).

Only the square pixel clock frequencies of 29.5 MHz and 24.5454 MHz are targeted for driving the scaler backend with PLL2 / CGC2.

8.6.1.1 The second PLL (PLL2)

The second PLL (PLL2) consists of a discrete time oscillator (DTO), a phase detector which computes the phase error once per video line while taking into account the current DTO phase and a PI -Loop Filter with programmable P/I coefficients.

If the phase error become less then a programmed locking threshold value SPTHRM [3:0] (register address FF H [3:0]) for a period of time defined number of lines programmed in SPTHRL [3:0] register (register address FF H [7:4]), the PLL2 indicates the status locked. If the PLL is locked, a status register SPLOCK (register address F1H [0]) is set.

The PLL2 is controlled by the following settings:

- Number of target clock cycles per line divided by 4 (SPLPL, register addresses F1 h [D0], F0 H [D7:D0]
- Nominal DTO increment (SPNINC, register addresses F3 H [D7:D0], F2 H [D7:D0]):
  The nominal Increment is basic clock frequency setting for PLL2 and hence for CGC2 clock output (CGC2frequency, in scaler backend clock generation mode). If PLL2 is opened it is the only parameter which defines the defines the clock frequency. It depends on the crystal frequency (32.11 MHz or 24.576 MHz) and is calculated as:

$$SPINC = \text{integer}\left(\left(\frac{CGC2frequency}{4 \cdot XTALfrequency}\right) \cdot 2^{16}\right)$$

- PLL2 operation mode (SPMOD, register address F1 H [D3:D2]):
  - PLL-closed (normal operation mode, SPMOD = 01 bin):
    This is the normal operation mode of the second PLL (PLL2): the nominal increment plus the content of loop filter define the output (CGC2) frequency.
  - Synthesize Clock Mode (SPMOD = 00 bin):
    The PLL2 is opened and hence the generated clock frequency at CGC2 output depends only on the nominal increment defined by the register SPNINC. The contribution of the loop filter is disabled. The I and P proportion of the loop filter is set to zero.
  - PLL-hold (SPMOD = 10 bin):
    The CGC2 output keeps the same clock frequency which was generated when entering this mode. In this mode content of the loop filter of PLL2 will be frozen.
  - PLL-Re-Sync (SPMOD = 11 bin)
    The phase detector of PLL2 is continuously re-synchronized to the selected horizontal reference signal controlled by SPHSEL. The remaining phase error is fed into the loop filter.
- Loop Filter Mode (P/I parameter selection; SPPI, register address F1 H [D7:D4]):
  As long as the PLL2 is in un-locked state the Loop Filter operates at a fast time constant to enable fast locking to the

input signal. As soon as the status is locked the PI-filter is controlled by the SPPI setting. Four different modes can be selected controlled via SPPI:

- Mode 0 H (default); Adaptive mode:
  The proportional part is controlled dynamically by the magnitude of the phase error.
- Mode 1 H; Fast mode
  Both P and I parameters of the Loop Filter remain on the “unlocked” values, even if PLL2 has locked.
- Mode E H; Medium mode:
  The proportional part (P) of the Loop Filter is set to a medium value and the integral part (I) is set to minimum.
- Mode F H; Slow mode:
  Both the proportional part and the integral part are set to minimum value.

8.7 Audio clock generation (subaddresses 30H to 3FH)

The SAA7115 incorporates with its Audio clock PLL (APLL), its second analog PLL (CGC2) the generation of multiple different audio clocks for external usage. There are two basic modes for generating an audio clock (refer to figure 32):

- Generating a frame locked Audio Master clock without using the second analog PLL (CGC2) (refer to chapter 8.7.1):
  This frame locked audio clock is directly obtained from the digital Audio PLL and output at the device pin AMCLK (pin 37). Hence this signal carries the correct number of clock cycles per frame but still has a high frequency jitter. This clock can be fed to an external PLL and than returned to the AMXCLK pin (pin 41) to generate an serial bitclock - output at the ASCLK pin (pin 39) - and a word select signal - output at the ALRCLK pin (pin 40).
  Using this audio clock generation method audio clock frequencies it is not possible to generate frequencies of 384*fs and 512*fs (fs = audio sampling frequency)
- Generating a low jitter frame locked Audio Master clock supported by the second analog PLL (CGC2) (refer to chapter 8.7.2):
  In this mode the digital Audio PLL output signal feeds the internal second analog PLL (CGC2) to remove high frequency jitter from the audio clock signal. The resulting clock is output at the device pin AMCLK (pin 37).
  This is already the audio clock for some high frequency audio clocks. All other audio clocks must be generated by feeding back the AMCLK output signal into the AMXCLK input pin. The audio clock frequency will be defined by the programming value of the SDIV[5:0] register (subaddress 38hex) and output at the ASCLK output pin (pin 39).

Both modes ensure that there is always the same predefined number of audio samples associated with a frame, because the audio clock is locked to the frame frequency.

8.7.1 Audio clock generation without analog PLL (CGC2) enhancement

8.7.1.1 Master audio clock

The audio clock is synthesized from the same crystal frequency as the line-locked video clock is generated. The master audio clock is defined by the parameters:

- Audio master Clocks Per Field, ACPF[17:0] 32H[1:0] 31H[7:0] 30H[7:0] according to the equation:

$$\text{ACPF[17:0]} = \text{round}\left(\frac{\text{audio master clock frequency}}{\text{field frequency}}\right)$$

- Audio master Clocks Nominal Increment, ACNI[21:0] 36H[5:0] 35H[7:0] 34H[7:0] according to the equation:

$$\text{ACNI[21:0]} = \text{round}\left(\frac{\text{audio master clock frequency}}{\text{crystal frequency}} \times 2^{23}\right)$$

See Table 28 for examples.

Remark: For standard applications the synthesized audio clock AMCLK can be used directly as master clock and as input clock for port AMXCLK (short cut) to generate ASCLK and ALRCLK. For high-end applications it is recommended to either use the second CGC for audio clock generation by setting UCGC = 1 (see subaddress 3AH, bit 7) or use an external analog PLL circuit to enhance the performance of the generated audio clock.

Table 28 Programming examples for audio master clock generation (no CGC2 support)

XTALO (MHz)	FIELD (Hz)	ACPF		ACNI	
		DECIMAL	HEX	DECIMAL	HEX
AMCLK = 256 × 48 kHz (12.288 MHz)					
32.11	50	245760	3C000	3210190	30FBCE
	59.94	205005	320CD	3210190	30FBCE
24.576	50	–	–	–	–
	59.94	–	–	–	–
AMCLK = 256 × 44.1 kHz (11.2896 MHz)					
32.11	50	225792	37200	2949362	2D00F2
	59.94	188348	2DFBC	2949362	2D00F2
24.576	50	225792	37200	3853517	3ACCCD
	59.94	188348	2DFBC	3853517	3ACCCD
AMCLK = 256 × 32 kHz (8.192 MHz)					
32.11	50	163840	28000	2140127	20A7DF
	59.94	136670	215DE	2140127	20A7DF
24.576	50	163840	28000	2796203	2AAAAB
	59.94	136670	215DE	2796203	2AAAAB

8.7.1.2 Signals ASCLK and ALRCLK

Two binary divided signals ASCLK and ALRCLK are provided for slower serial digital audio signal transmission and for channel-select. The frequencies of these signals are defined by the following parameters:

- SDIV[5:0] 38H[5:0] according to the equation:

$$f_{ASCLK} = \frac{f_{AMXCLK}}{(SDIV + 1) \times 2} \Rightarrow SDIV[5:0] = \frac{f_{AMXCLK}}{2f_{ASCLK}} - 1$$

- LRDIV[5:0] 39H[5:0] according to the equation:

$$f_{ALRCLK} = \frac{f_{ASCLK}}{LRDIV \times 2} \Rightarrow LRDIV[5:0] = \frac{f_{ASCLK}}{2f_{ALRCLK}}$$

See Table 29 for examples.

Table 29 Programming examples for ASCLK/ALRCLK clock generation

AMXCLK (MHz)	ASCLK (kHz)	SDIV		ALRCLK (kHz)	LRDIV	
		DECIMAL	HEX		DECIMAL	HEX
12.288	1536	3	03	48	16	10
	768	7	07		8	08
11.2896	1411.2	3	03	44.1	16	10
	2822.4	1	01		32	10
8.192	1024	3	03	32	16	10
	2048	1	01		32	10

8.7.2 Audio clock generation with analog PLL (CGC2) support

When generating the Audio clock using the second analog PLL (CGC2) the CGC2 is driven by the digital Audio Clock PLL. The Output of CGC2 again is output at the audio master clock output pin AMCLK (pin 37) controlled by the UCGC (address 3A H [7]) programming register. For audio clock frequencies of 512 * fs, with fs = 48.0 KHz or 44.1 KHz this is already the low jitter audio clock. All other low jitter audio clocks are output at the ASCLK pin (pin 39) using the internal divider controlled by SDIV (address 38 H [5:0]) programming register (refer to table 30 and 31). Therefore the audio master clock AMCLK must be returned into the device via the AMXCLK pin (pin 41).

The audio master clock again is synthesized from the same crystal frequency as the line-locked video clock and is defined as:

- Audio master Clocks Per Field, ACPF[17:0] 32H[1:0] 31H[7:0] 30H[7:0] according to the equation:

$$ACPF[17:0] = \text{round}\left(\left(\frac{\text{audio master clock frequency}}{\text{field frequency}}\right)\cdot\left(\frac{(4 - CGCDIV)}{16}\right)\right)$$

- Audio master Clocks Nominal Increment, ACNI[21:0] 36H[5:0] 35H[7:0] 34H[7:0] according to the equation:

$$ACNI[21:0] = \text{round}\left(\left(\frac{\text{audio master clock frequency}}{\text{crystal frequency}} \times 2^{23}\right)\cdot\left(\frac{(4 - CGCDIV)}{16}\right)\right)$$

Note that in this case the audio master clock is not identical to the clock output by the digital audio clock PLL any more.

The second analog PLL (CGC2) operates at a centre frequency of 36 MHz if CGCDIV (register address 3A H [6]) is set to 1 and 27 MHz if CGCDIV is set to 0. CGC2 can operate in a range of -18% and +15.8% around these centre frequencies.

Table 30 Programming examples for frame locked audio clock generation supported by CGC2, fxtal = 24.576 MHz, 625 /525 line systems

n * fs	CGCDIV [bin]	AMCLK Freq. [MHz]	ACNI		ACPF		SDIV		AMXCLK / ASCLK Ratio	Audio Clock	
			[dec]	[hex]	625 / 525 [dec]	[hex]	[dec]	[hex]		[MHz]	Output pin (AMCLK / ASCLK)
fs = 48 KHz											
512	0	24.576	2097152	200000	122880 / 102502	1e000 / 19066	na.	na.	na.	24.576	AMCLK
384	1	36.864	2359296	240000	138240 / 115315	21c00 / 1c273	0	00	2	18.432	ASCLK
256	0	24.576	2097152	200000	122880 / 102502	1e000 / 19066	0	00	2	12.288	ASCLK
192	1	36.864	2359296	240000	138240 / 115315	21c00 / 1c273	1	01	4	9.216	ASCLK
128	1	36.864	2359296	240000	138240 / 115315	21c00 / 1c273	2	02	6	6.144	ASCLK
96	1	36.864	2359296	240000	138240 / 115315	21c00 / 1c273	3	03	8	4.608	ASCLK
64	1	36.864	2359296	240000	138240 / 115315	21c00 / 1c273	5	05	12	3.072	ASCLK
48	1	36.864	2359296	240000	138240 / 115315	21c00 / 1c273	7	07	16	2.304	ASCLK
32	1	36.864	2359296	240000	138240 / 115315	21c00 / 1c273	11	0B	24	1.536	ASCLK
fs = 44.1 KHz											
512	0	22.5792	1926758	1d6666	112896 / 94174	1b900 / 16fde	na.	na.	na.	22.5792	AMCLK
384	1	33.8688	2167603	211333	127008 / 105946	1f020 / 19dda	0	00	2	16.9344	ASCLK
256	0	22.5792	1926758	1d6666	112896 / 94174	1b900 / 16fde	0	00	2	11.2896	ASCLK
192	1	33.8688	2167603	211333	127008 / 105946	1f020 / 19dda	1	01	4	8.4672	ASCLK
128	1	33.8688	2167603	211333	127008 / 105946	1f020 / 19dda	2	02	6	5.6448	ASCLK

n * fs	CGCDIV [bin]	AMCLK Freq. [MHz]	ACNI		ACPF		SDIV		AMXCLK / ASCLK Ratio	Audio Clock	
			[dec]	[hex]	625 / 525 [dec]	[hex]	[dec]	[hex]		[MHz]	Output pin (AMCLK / ASCLK)
96	1	33.8688	2167603	211333	127008 / 105946	1f020 / 19dda	3	03	8	4.2336	ASCLK
64	1	33.8688	2167603	211333	127008 / 105946	1f020 / 19dda	6	06	12	2.8224	ASCLK
48	1	33.8688	2167603	211333	127008 / 105946	1f020 / 19dda	7	07	14	2.1168	ASCLK
32	1	33.8688	2167603	211333	127008 / 105946	1f020 / 19dda	11	0b	24	1.4112	ASCLK
fs = 32 KHz											
512	1	32.768	2097152	200000	122880 / 102502	1e000 / 19066	0	00	2	16.384	ASCLK
384	0	24.576	2097152	200000	122880 / 102502	1e000 / 19066	0	00	2	12.288	ASCLK
256	1	32.768	2097152	200000	122880 / 102502	1e000 / 19066	1	01	4	8.192	ASCLK
192	1	36.864	2359296	240000	138240 / 115315	21c00 / 1c273	2	02	6	6.144	ASCLK
128	0	24.576	2097152	200000	122880 / 102502	1e000 / 19066	2	02	6	4.096	ASCLK
96	1	36.864	2359296	240000	138240 / 115315	21c00 / 1c273	5	05	12	3.072	ASCLK
64	1	36.864	2359296	240000	138240 / 115315	21c00 / 1c273	8	08	18	2.048	ASCLK
48	1	36.864	2359296	240000	138240 / 115315	21c00 / 1c273	11	0b	24	1.536	ASCLK
32	1	36.864	2359296	240000	138240 / 115315	21c00 / 1c273	17	11	36	1.024	ASCLK

Table 31 Programming examples for frame locked audio clock generation supported by CGC2, fxtal = 32.11MHz, 625 /525 line systems

n * fs	CGCDIV [bin]	AMCLK Freq. [MHz]	ACNI		ACPF		SDIV		AMXCLK / ASCLK Ratio	Audio Clock	
			[dec]	[hex]	625 / 525 [dec]	[hex]	[dec]	[hex]		[MHz]	Output pin (AMCLK / ASCLK)
fs = 48 KHz											
512	0	24.576	1605095	187de7	122880 / 102502	1e000 / 19066	na.	na.	na.	24.576	AMCLK
384	1	36.864	1805732	1b8da4	138240 / 115315	21c00 / 1c273	0	00	2	18.432	ASCLK
256	0	24.576	1605095	187de7	122880 / 102502	1e000 / 19066	0	00	2	12.288	ASCLK
192	1	36.864	1805732	1b8da4	138240 / 115315	21c00 / 1c273	1	01	4	9.216	ASCLK
128	1	36.864	1805732	1b8da4	138240 / 115315	21c00 / 1c273	2	02	6	6.144	ASCLK
96	1	36.864	1805732	1b8da4	138240 / 115315	21c00 / 1c273	3	03	8	4.608	ASCLK
64	1	36.864	1805732	1b8da4	138240 / 115315	21c00 / 1c273	5	05	12	3.072	ASCLK
48	1	36.864	1805732	1b8da4	138240 / 115315	21c00 / 1c273	7	07	16	2.304	ASCLK
32	1	36.864	1805732	1b8da4	138240 / 115315	21c00 / 1c273	11	0B	24	1.536	ASCLK
fs = 44.1 KHz											
512	0	22.5792	1474681	168079	112896 / 94174	1b900 / 16fde	na.	na.	na.	22.5792	AMCLK
384	1	33.8688	1659016	195088	127008 / 105946	1f020 / 19dda	0	00	2	16.9344	ASCLK
256	0	22.5792	1474681	168079	112896 / 94174	1b900 / 16fde	0	00	2	11.2896	ASCLK
192	1	33.8688	1659016	195088	127008 / 105946	1f020 / 19dda	1	01	4	8.4672	ASCLK
128	1	33.8688	1659016	195088	127008 / 105946	1f020 / 19dda	2	02	6	5.6448	ASCLK

n * fs	CGCDIV [bin]	AMCLK Freq. [MHz]	ACNI		ACPF		SDIV		AMXCLK / ASCLK Ratio	Audio Clock	
			[dec]	[hex]	625 / 525 [dec]	[hex]	[dec]	[hex]		[MHz]	Output pin (AMCLK / ASCLK)
96	1	33.8688	1659016	195088	127008 / 105946	1f020 / 19dda	3	03	8	4.2336	ASCLK
64	1	33.8688	1659016	195088	127008 / 105946	1f020 / 19dda	6	06	12	2.8224	ASCLK
48	1	33.8688	1659016	195088	127008 / 105946	1f020 / 19dda	7	07	14	2.1168	ASCLK
32	1	33.8688	1659016	195088	127008 / 105946	1f020 / 19dda	11	0b	24	1.4112	ASCLK
fs = 32 KHz											
512	1	32.768	1605095	187de7	122880 / 102502	1e000 / 19066	0	00	2	16.384	ASCLK
384	0	24.576	1605095	187de7	122880 / 102502	1e000 / 19066	0	00	2	12.288	ASCLK
256	1	32.768	1605095	187de7	122880 / 102502	1e000 / 19066	1	01	4	8.192	ASCLK
192	1	36.864	1805732	1b8da4	138240 / 115315	21c00 / 1c273	2	02	6	6.144	ASCLK
128	0	24.576	1605095	187de7	122880 / 102502	1e000 / 19066	2	02	6	4.096	ASCLK
96	1	36.864	1805732	1b8da4	138240 / 115315	21c00 / 1c273	5	05	12	3.072	ASCLK
64	1	36.864	1805732	1b8da4	138240 / 115315	21c00 / 1c273	8	08	18	2.048	ASCLK
48	1	36.864	1805732	1b8da4	138240 / 115315	21c00 / 1c273	11	0b	24	1.536	ASCLK
32	1	36.864	1805732	1b8da4	138240 / 115315	21c00 / 1c273	17	11	36	1.024	ASCLK

8.7.3 Other control signals for audio clock generation

Further control signals are available to define reference clock edges and vertical references:

APLL[3AH[3]]; Audio PLL mode:

0: PLL closed

1: PLL open

AMVR[3AH[2]]; Audio Master clock Vertical Reference:

0: internal V

1: external V

LRPH[3AH[1]]; ALRCLK Phase

0: invert ASCLK, ALRCLK edges triggered by falling edge of ASCLK

1: don’t invert ASCLK, ALRCLK edges triggered by rising edge of ASCLK

SCPH[3AH[0]]; ASCLK Phase:

0: invert AMXCLK, ASCLK edges triggered by falling edge of AMXCLK

1: don’t invert AMXCLK, ASCLK edges triggered by rising edge of AMXCLK.

9 INPUT/OUTPUT INTERFACES AND PORTS

The SAA7115 has 5 different I/O interfaces:

- Analog video input interface, for analog CVBS and/or Y and C input signals
- Audio clock port
- Digital real-time signal port (RT port)
- Digital video expansion port (X-port), for unscaled digital video input and output
- Digital image port (I-port) for scaled video data output and programming
- Digital host port (H-port) for extension of the image port (output mode) or expansion port (input mode) from 8 to 16-bit.

9.1 Analog terminals

The SAA7115 has 6 analog inputs AI21 to AI24 and AI11 to AI12 for composite video CVBS or S-video Y/C signal pairs.

Additionally, there are two differential reference inputs, which must be connected to ground via a capacitor equivalent to the decoupling capacitors at the 6 inputs. Per connected input there are no peripheral components required other than a decoupling capacitor of 47nF directly connected to the analog device inputs pins), an 18 Ω (connected in series directly to the source) and 56 Ω (connected between the capacitor and the 18 Ω resistor to ground) termination resistor. Two anti-alias filters are integrated.

Clamp and gain control for the ADCs are also integrated. An analog video output (pin AOUT) is provided for testing purposes.

Table 32 Analog pin description

SYMBOL	PIN	I/O	DESCRIPTION	BIT
AI11 and AI12	20, 18	I	analog video signal inputs, e.g. six CVBS signals or two Y/C plus two CVBS pairs signal groups can be connected simultaneously to this device; several combinations are possible; see table 54.	MODE3 to MODE0 (02H[3:0])
AI21, AI22, AI23 and AI24	16, 14, 12, 10			
AOUT	22	O	analog video output, for test purposes	AOSL2 to AOSL0 (01H[7], 14H[5:4])
AI1D, AI2D	19, 13	I	analog reference pins for differential ADC operation; connect to ground via 47 nF	–

9.2 Audio clock signals

The SAA7115 also synchronizes the audio clock and sampling rate to the video frame rate, via a very slow PLL. This ensures that the multimedia capture and compression processes always gather the same predefined number of samples per video frame.

There are two basic modes as described in chapter 8.7 . Depending on these modes the signals AMCLK, ASCLK and ALRCLK are generated (Note: To generate ASCLK and ALRCLK the Audio Master clock AMCLK must be fed back into the device via the AMXCLK pin.).

- Generating a frame locked Audio Master clock without using the second analog PLL (CGC2):
  - AMCLK: is the audio clock.
  - ASCLK: can be used as audio serial clock.
  - ALRCLK: audio left/right channel clock.
- Generating a low jitter frame locked Audio Master clock supported by the second analog PLL (CGC2):
  - AMCLK: is the audio clock for 512*fs (fs = 48KHz or 44.1KHz).

– ASCLK: is the audio clock for all other audio clock frequencies.

The ratios are programmable; see also chapter 8.7.

Table 33 Audio clock pin description

SYMBOL	PIN	I/O	DESCRIPTION	BIT
AMCLK	37	O	Audio master clock output without use of CGC2	ACPF[17:0] (32H[1:0] 31H[7:0] 30H[7:0]), ACNI[21:0] (36H[5:0] 35H[7:0] 34H[7:0]), AMVR (3AH[2]), APLL (3AH[3]), UCGC (3AH[3]; must be set to 0)
			Audio master clock output using of CGC2 (low jitter audio clock)	ACPF[17:0] (32H[1:0] 31H[7:0] 30H[7:0]), ACNI[21:0] (36H[5:0] 35H[7:0] 34H[7:0]), AMVR (3AH[2]), APLL (3AH[3]), UCGC (3AH[3]; must be set to 1), CGCDIV (3AH[6])
AMXCLK	41	I	External audio master clock input for the clock division circuit, can be directly connected to output AMCLK for standard applications	–
ASCLK	39	O	Serial audio clock output, can be synchronized to rising or falling edge of AMXCLK	SDIV[5:0] (38H[5:0]), SCPH (3AH[0]),
ALRCLK	40	O	Audio channel (left/right) clock output, can be synchronized to rising or falling edge of ASCLK.	LRDIV[5:0] (39H[5:0]), LRPH(3AH[1])
		I	Strapping during reset determines the crystal oscillator frequency to be used.	-

9.3 Clock and real-time synchronization signals

For the generation of the line-locked video (pixel) clock LLC, and of the frame-locked audio serial bit clock, a crystal accurate frequency reference is required. An oscillator is built-in for fundamental or third harmonic crystals. The supported crystal frequencies are 32.11 MHz and 24.576 MHz (defined during reset by strapping pin ALRCLK).

Alternatively pin XTALI can be driven from an external single-ended oscillator.

The crystal oscillation can be propagated as a clock to other ICs in the system via pin XTOUT.

The Line-Locked Clock (LLC) is the double pixel clock of nominal 27 MHz. It is locked to the selected video input, generating baseband video pixels according to *“ITU recommendation 601”*. In order to support interfacing circuits, a direct pixel clock (LLC2) is also provided.

The pins for line and field timing reference signals are RTCO, RTS1 and RTS0. Various real-time status information can be selected for the RTS pins. The signals are always available (output) and reflect the synchronization operation of the decoder part in the SAA7115. The function of the RTS1 and RTS0 pins can be defined by bits RTSE1[3:0] 12H[7:4] and RTSE0[3:0] 12H[3:0].

Table 34 Clock and real-time synchronization signals

SYMBOL	PIN	I/O	DESCRIPTION	BIT
Crystal oscillator				
XTALI	7	I	input for crystal oscillator or reference clock	–
XTALO	6	O	output of crystal oscillator	–
XTOUT	4	O	reference (crystal) clock output drive (optional)	XTOUTE (14H[3])
Real-time signals (RT port)				
LLC	28	O	line-locked clock, nominal 27 MHz, double pixel clock locked to the selected video input signal, for backward compatibility only, do not use for new applications	–
LLC2	29	O	line-locked pixel clock, nominal 13.5 MHz, for backward compatibility only, do not use for new applications	–
RTCO	36	O	real-time control output, transfers real-time status information supporting RTC level 3.1 (see document “RTC Functional Description”, available on request)	–
		I	Strapping during reset determines the I^2C read/write addresses address.	-
RTS0	34	O	real-time status information line 0, can be programmed to carry various real-time information (see Table 70)	RTSE0[3:0] (12H[3:0])
RTS1	35	O	real-time status information line 1, can be programmed to carry various real-time information (see Table 71)	RTSE1[3:0] (12H[7:4])

9.4 Video expansion port (X-port)

The expansion port can be used either to output eight or ten bit video from the combfilter decoder directly or to receive video data from other external digital video sources such as MPEG decoder for output at the image port (I-port) whilst.

The expansion port consists of three main groupings of signals:

- 8-bit dithered or 10-bit data output of component video Y-C_B-C_R 4 : 2 : 2, i.e. in C_B-Y-C_R-Y, sequence. In 10-bit wide video mode the two data LSB’s are output on the XRH and XRV signal lines.

  Exceptionally raw video samples (e.g. ADC test).
- 8-bit data input of component video Y-C_B-C_R 4 : 2 : 2, i.e. C_B-Y-C_R-Y, byte serial. In input mode optionally the data bus can be extended to 16-bit by pins HPD7 to HPD0. In this mode XPD [7:0] carries the luminance data and HPD [7:0] carries the Chrominance data.
- Clock, synchronization and auxiliary I/O signals, accompanying the data stream.

The data transfers through the expansion port represent a single D1 port, with half duplex mode. The SAV and EAV codes may be inserted optionally for data input (controlled by bit XCODE (92H[3])). The input/output direction is switched for complete fields only.

Table 35 Signals dedicated to the expansion port

SYMBOL	PIN	I/O	DESCRIPTION	BIT
XPD7 to XPD0	81, 82, 84 -87, 89, 90	I/O	X-port data: in output mode controlled by decoder section, data format see Table 36; in input mode Y-CB-CR 4 : 2 : 2 serial input data or luminance part of a 16-bit Y-CB-CR 4 : 2 : 2 data stream	OFTS[3:0] (1BH[4], 13H[2:0]), CONLV (91H[7], C1H[7]), HLDFV (91H[6], C1H[6]), SCSRC[1:0] (91H[5:4], C1H[5:4]), SCRQE (91H[3], C1H[3]), FSC[2:0] (91H[2:0], C1H[2:0])
HPD7 to HPD0	64 -67, 69 - 72	I/(O)	With the X-port, these signals are used as input only, for 16-bit Y-CB-CR 4 : 2 : 2 video data. In this case HPD[7:0] carries chrominance data.	ICKS[3:0] (80H[3:0]), SCSRC[1:0] (91H[5:4], C1H[5:4])
XCLK	94	I/O	clock at expansion port: if output, then copy of LLC; as input normally a double pixel clock of up to 32 MHz or a gated clock (clock gated with a qualifier)	XCKS (92H[0], C2H[0])
XDQ	95	I/O	data valid flag of the expansion port input (qualifier): if output, then decoder (HREF and VGATE) gate (see Fig.24)	–
XRDY	96	O	data request flag = ready to receive, to work with optional buffer in external device, to prevent internal buffer overflow; second function: input related task flag A/B	XRQT (83H[2])
XRH	92	I/O	horizontal reference signal for the X-port: as output: HREF or HS from the decoder (see Fig.24) or bit 1 of D1 decoder 10 bit output; as input: a reference edge for horizontal input timing and a polarity for input field ID detection can be defined	XRHS (13H[6]), XFDH (92H[6], C2H[6]), XDH (92H[2], C2H[2]]
XRV	91	I/O	vertical reference signal for the X-port: as output: V123 or field ID from the decoder, see Figs 22 and or 23 or bit 0 of D1 decoder 10 bit output; as input: a reference edge for vertical input timing and for input field ID detection can be defined	XRVS[1:0] (13H[5:4]), XFDV (92H[7], C2H[7]), XDV[1:0] (92H[5:4], C2H[5:4])
XTRI	80	I	port control: switches X-port input 3-state	XPE[1:0] (83H[1:0])

9.4.1 X-PORT CONFIGURED AS OUTPUT

If data output is enabled at the expansion port, then the data stream from the decoder is presented. The data format of the 8-bit data bus is dependent on the chosen data type, selectable by the line control registers LCR2 to LCR24; see Table 6. In contrast to the image port, the sliced data format is not available on the expansion port. Instead, raw CVBS samples are always transferred if any sliced data type is selected.

Some details of data types on the expansion port are as follows:

- **Active video** (data types 0 and 15): contains component Y-C_B-C_R 4 : 2 : 2 signal, 720 active pixels per line. The amplitude and offsets are programmable via DBRI7 to DBRI0, DCON7 to DCON0, DSAT7 to DSAT0, OFFU1, OFFU0, OFFV1 and OFFV0. For nominal levels see Fig.18.
- **Test line** (data type 14): is similar to the active video format, with some constraints within the data processing:
  - adaptive chrominance comb filter, vertical filter (chrominance comb filter for NTSC standards, PAL phase error correction) within the chrominance processing are disabled
  - adaptive luminance comb filter, peaking and chrominance trap are bypassed within the luminance processing

  This data type is defined for future enhancements. It could be activated for lines containing standard test signals within the vertical blanking period. Currently the most sources do not contain test lines. For nominal levels see Fig.18.
- **Raw samples** (data types 1 to 13): C_B-C_R samples are similar to data type 6, but CVBS samples are transferred instead of processed luminance samples within the Y time slots.

  The amplitude and offset of the CVBS signal is programmable via RAWG7 to RAWG0 and RAWO7 to RAWO0; see Chapter 16, Tables 78 and 79. For nominal levels see Fig.19.

The relationship of LCR programming to line numbers is described in Section 8.4, see Tables 7 to 10.

The data type selections by LCR are overruled by setting OFTS[3:0] = 1110 (ADC1 bypass mode) or OFTS[3:0] = 1111 (ADC2 bypass mode) at subaddresses 1BH, bit 4 and 13H bit 2 to 0. This setting is mainly intended for device production test. The X-port (XPD[7:0]) carries the upper 8 bits of either of the two ADCs, the LSB is provided on pin XRH; see Table 72 “RT / X-port output control (SA 13, SA 1B)”. The analog input configuration is done via MODE[3:0] 02H[3:0] settings; see table 53 “Analog control 1 (SA 02)”. No timing reference codes are generated in this mode.

The SAV/EAV timing reference codes define the start and end of valid data regions. The ITU-blanking code sequence ‘- 80 - 10 - 80 - 10 -...’ is transmitted during the horizontal blanking period between EAV and SAV.

The position of the F-bit is constant in accordance with ITU 656; see Tables 38 and 39.

The V-bit can be generated in two different ways (see Tables 38 and 39) controlled via OFTS1 and OFTS0; see Table 72.

In case of enabling 10-bit video output mode via OFTS[3:0] then XPD[7:0] carries the video data bits 9 to 2 and SAV/EAV codes and the signals XRH and XRV the data LSBs 1 and 0 respectively. During blanking both LSBs are zero.

The F and V bits change synchronously with the EAV code.

Table 36 Data format on the expansion port

BLANKING PERIOD			**TIMING REFERENCE CODE (HEX)**[1]				**720 PIXELS Y-C_B-C_R 4 : 2 : 2 DATA**[2]									**TIMING REFERENCE CODE (HEX)**[1]				**BLANKING PERIOD**		
...	**80**	**10**	**FF**	**00**	**00**	**SAV**	**CB 0**	**Y0**	**CR 0**	**Y1**	**CB 2**	**Y2**	**...**	**CR718**	**Y719**	**FF**	**00**	**00**	**EAV**	**80**	**10**	**...**

Notes

1. The generation of the timing reference codes and the ITU-blanking code sequence can be suppressed by setting OFTS[3:0] to ‘x010’, see Table 72.
2. If raw samples or sliced data are selected by the line control registers (LCR2 to LCR24), the Y samples are replaced by CVBS samples.

Table 37 Format of the control byte of SAV/EAV codes on expansion port XPD7 to XPD0

BIT 7	BIT 6 (F)	BIT 5 (V)	BIT 4 (H)	BIT 3 (P3)	BIT 2 (P2)	BIT 1 (P1)	BIT 0 (P0)
1	field bit 1st field: F = 0 2nd field: F = 1	vertical blanking bit VBI: V = 1 active video: V = 0	format H = 0 in SAV format H = 1 in EAV format	reserved; evaluation not recommended (protection bits according to ITU 656)			
	for vertical timing see Tables 38 and 39						

Table 38 525 lines/60 Hz vertical timing

LINE NUMBER	F (ITU 656)	V	
		OFTS[3:0] = 0000 OR OFTS[3:0] = 1000 (ITU 656)	OFTS[3:0] = 0001 OR OFTS[3:0] = 1001
1 to 3	1	1	according to selected VGATE position type via VSTA and VSTO (subaddresses 15H to 17H); see Tables 75 to 76
4 to 19	0	1	
20	0	0	
21	0	0	
22 to 261	0	0	
262	0	0	
263	0	0	
264 and 265	0	1	
266 to 282	1	1	
283	1	0	
284	1	0	
285 to 524	1	0	
525	1	0	

Table 39 625 lines/50 Hz vertical timing

LINE NUMBER	F (ITU 656)	V	
		OFTS[3:0] = 0000 OR OFTS[3:0] = 1000 (ITU 656)	OFTS[3:0] = 0001 OR OFTS[3:0] = 1001
1 to 22	0	1	according to selected VGATE position type via VSTA and VSTO (subaddresses 15H to 17H); see Tables 75 to 76
23	0	0	
24 to 309	0	0	
310	0	0	
311 and 312	0	1	
313 to 335	1	1	
336	1	0	
337 to 622	1	0	
623	1	0	
624 and 625	1	1	

9.4.2 X-PORT CONFIGURED AS INPUT

If data input mode is selected at the expansion port, then the scaler can choose its input data stream from the on-chip video decoder, or from the expansion port (controlled by bit SCSRC[1:0] (91H[5:4]), C1H[5:4])). Byte serial Y-C_B-C_R 4 : 2 : 2, or subsets for other sampling schemes, or raw samples from an external ADC may be input (see also bits FSC[2:0] (91H[2:0], C1H[2:0])). The input stream must be accompanied by an external clock (XCLK), qualifier XDQ and reference signals XRH and XRV. Instead of the reference signal, embedded SAV and EAV codes according to ITU 656 are also accepted. The protection bits are not evaluated.

XRH and XRV carry the horizontal and vertical synchronization signals for the digital video stream through the expansion port. The field ID of the input video stream is carried in the phase (edge) of XRV and state of XRH, or directly as FS (frame sync, odd/even signal) on the XRV pin (controlled by XFDV (92H[7], C2H[7[), XFDH (92H[6], C2H[6]) and XDV[1:0] (92H[5:4], C2H[5:4])).

The trigger events on XRH (rising/falling edge) and XRV (rising/falling/both edges) for the scalers acquisition window are defined by XDV[1:0] and XDH (92H[2], C2H[2]). The signal polarity of the qualifier can also be defined (bit XDQ (92H[1], C2H[1])). Alternatively to a qualifier, the input clock can be applied to a gated clock (means clock gated with a data qualifier, controlled by bit XCKS (92H[0], C2H[0])). In this case, all input data will be qualified.

In case if 16 bit wide data input is required for the X-port input then the HPD[7:0] port is enabled for input via SCSRC[1:0] (91H[5:4], C1H[5:4]) whilst the I-port must be set to 8-bit output mode by ICKS[3:0] (80H[3:0]).

9.5 Image port (I-port)

The image port transfers data from the scaler as well as from the VBI-data slicer, if selected (maximum 33 MHz). The reference clock is available at the ICLK pin, as an output, or as an input (maximum 33 MHz). As output, ICLK is derived either from the line-locked decoder or from the expansion port input clock or from PLL2/CGC2 combination, which enables square pixel clock generation feature.

The data stream from the scaler output is usually discontinuous, which basically depends on the scale ratio. Therefore valid data during a clock cycle is accompanied by a data qualifying (data valid) flag on pin IDQ. For pin constrained applications the IDQ pin can be programmed to function as a gated clock output (bit ICKS2[80H[2]]).

The pulsegenerator allows however to squeeze all pixels of a video line so that a continuous video stream at the I-port output is obtained. For details refer to chapter 8.2..

The data formats at the image port are defined in Dwords of 32 bits (4 bytes), such as the related FIFO structures. However the physical data stream at the image port is only 16-bit or 8-bit wide; in 16-bit mode data pins HPD7 to HPD0 are used for chrominance data. The four bytes of the Dwords are serialized in words or bytes.

Available formats are as follows:

- Y-C_B-C_R 4 : 2 : 2
- Y-C_B-C_R 4 : 1 : 1
- Raw samples
- Decoded VBI-data.

For handshake with the receiving VGA controller, or other memory or bus interface circuitry, F, H and V reference signals and programmable FIFO flags are provided. The information is provided on pins IGP0, IGP1, IGPH and IGPV. The functionality on these pins is controlled via subaddresses 84H and 85H.

VBI-data is collected over an entire line in its own FIFO, and transferred as an uninterrupted block of bytes. Decoded VBI-data can be indicated by the VBI flag on pin IGP0 or IGP1.

As scaled video data and decoded VBI-data may come from different and asynchronous sources, an arbitration scheme is needed. Normally the VBI-data slicer has priority.

The image port consists of the pins and/or signals, as listed in Table 40.

For pin constrained applications, or interfaces, the relevant timing and data reference signals can also be encoded into the data stream. Therefore the corresponding signal pins do not need to be connected. The minimum image port configuration requires 9 pins only, i.e. 8 pins for data including codes, and 1 pin for clock or gated clock. The inserted codes are defined in close relationship to the ITU-R BT.656 (D1) recommendation, where possible.

In the case of scaling and for CMOD [80[7]] = '0', the following deviations from *"ITU 656 recommendation"* are implemented at the SAA7115s image port interface:

- SAV and EAV codes are only present in those lines, where data is to be transferred, i.e. active video lines, or VBI raw samples, no codes for empty lines (=lines not covered by the scalers window definition)
- There may be more or less than 720 pixels between SAV and EAV depending on the scaler settings
- Data content and the number of clock cycles during horizontal and vertical blanking is undefined, and may not be constant. To get a regular pattern in case of scaling, the internal trigger positions for data packing (see section 8.5.4.2.) need to be balanced.
- Data stream may be interleaved with not-valid data, 00H codes or old data (see bit INS80 [93[6]]), but SAV and EAV 4-byte codes are not interleaved with not-valid data codes
- There may be an irregular pattern of not-valid data, or IDQ, and as a result, C_B-Y-C_R-Y is not in a fixed phase to a regular clock divider
- VBI raw sample streams are enveloped with SAV and EAV, like normal video
- Decoded VBI-data is transported as Ancillary (ANC) data or enveloped with SAV and EAV (see bits SLDOM [5D[4:0]]), two modes:
  - direct decoded VBI-data bytes (8-bit), 00H and FFH codes may appear in the data block (violation to ITU-R BT.656)
  - recoded VBI-data bytes (8-bit), 00H and FFH codes will be recoded to even parity codes 03H and FCH to suppress invalid ITU-R BT.656 codes.

Sliced VBI data are transferred as continuous packages with no empty cycles.
The data codes 00H and FFH are suppressed (changed to 01H or FEH respectively) in the active video stream, as well as in the VBI raw sample stream (VBI pass-through). Optionally, the number range can be further limited (see bit ILLV [85[5]]).
If the video data are not packed and ITRDY = '1', due to the internal 32 bit wide backend FIFO, valid data occur as 4 byte (8 bit output), respec. 2 byte (16 bit output) packages of valid data.

Table 40 Signals dedicated to the image port

SYMBOL	PIN	I/O	DESCRIPTION	BIT
IPD7 to IPD0	54 -57, 59 -62	I/O	I-port data	ICODE (93H[7], C3H(7)), ISWP[1:0] (85H[7:6]), IPE[1:0] (87H[1:0])
HPD7 to HPD0	64 -67, 69 - 72	(I)/O	With the I-port, these signals are used as output only, for 16-bit Y-CB-CR 4 : 2 : 2 video data. In this case HPD[7:0] carries chrominance data.	ICKS[3:0] (80H[3:0]), SCSRC[1:0] (91H[5:4], C1H[5:4]), IPE[1:0] (87H[1:0])
ICLK	45	I/O	continuous reference clock at image port, can be input or output, as output decoder LLC or XCLK from X-port	ICKS[3:0] (80H[3:0]), IPE[1:0] (87H[1:0])
IDQ	46	O	data valid flag at image port, qualifier, with programmable polarity; secondary function: gated clock	ICKS[3:0] (80H[3:0]), IPE[1:0] (87H[1:0]) IDQP[85H[0]]
IGPH	53	O	horizontal reference output signal, copy of the H-gate signal of the scaler, with programmable polarity; alternative function: HRESET pulse	IDH[1:0] (84H[1:0]), IRHP(85H[1]), IPE[1:0] 87H[1:0]
IGPV	52	O	vertical reference output signal, copy of the V-gate signal of the scaler, with programmable polarity; alternative function: VRESET pulse	IDV[1:0] 84H[3:2], IRVP (85H[2]), IPE[1:0] (87H[1:0])
IGP1	49	O	general purpose output signal for I-port	IDG12 (86H[4]), IDG1[1:0] (84H[5:4]), IG1P (85H[3]), IPE[1:0] (87H[1:0])
IGP0	48	O	general purpose output signal for I-port	IDG02 (86H[5]), IDG0[1:0] (84H[7:6]), IG0P (85H[4]), IPE[1:0] (87H[1:0])
ITRDY	42	I	target ready input signals	–
ITRI	47	I	port control, switches I-port into 3-state	IPE[1:0] (87H[1:0])

9.6 Host port for 16-bit extension of video data I/O (H-port)

The H-port pins HPD can be used for extension of the data I/O paths to 16-bit. For the X-port HPD[7:0] are used as 16-bit input extension where as the I-port uses HPD[7:0] as 16-bit output extension.

The I-port has functional priority. If a 16 bit output mode is set via ICKS[3:2], see table 121 “I-port and scaler backend clock selection (SA 80)” the output drivers of the H-port are enabled depending on the I-port enable control.

Table 41 Signals dedicated to the host port

SYMBOL	PIN	I/O	DESCRIPTION	BIT
HPD7 to HPD0	64 -67, 69 - 72	I/(O)	With the X-port, these signals are used as input only, for 16-bit Y-CB-CR 4 : 2 : 2 video data. In this case HPD[7:0] carries chrominance data.	ICKS[3:0] (80H[3:0]), SCSRC[1:0] (91H[5:4], C1H[5:4]), IPE[1:0] (87H[1:0]), ITRI ([8FH[6])
		(I)/O	With the I-port, these signals are used as output only, for 16-bit Y-CB-CR 4 : 2 : 2 video data. In this case HPD[7:0] carries chrominance data.	

9.7 Basic input and output timing diagrams I-port and X-port

9.7.1 I-PORT OUTPUT TIMING

The following diagrams (figures 33 to 39) illustrate the output timing via the I-port. IGPH and the scalers IGPV are logic 1 active gate signals. If reference pulses are programmed, these pulses are generated on the rising edge of the logic 1 active gates. Valid data is accompanied by the output data qualifier on pin IDQ.
An data request via ITRDY = ‘1’ is answered with the next clock cycle by marking this cycle as valid or invalid data. Due to the scaling and the output processing, it may last several ITRDY = ‘1’ cycles, before a request is answered with valid data. After running in and if the requested data rate is matched to the scaled data rate, valid data are normally provided with the next clock cycle.
The behaviour during invalid clock cycles depend on the INS80 bit and the ITRDY input.
For INS80 = ‘0’ the value 00H is inserted on IPD[7:0], resp. HPD[7:0], for all clock cycles marked with IDQ = ‘0’
For INS80 = ‘1’ data are hold during a line, if ITRDY =’0’ or IDQ=’0’. Outside the active line and in 8 bit output mode, the inserted blanking values (‘80H’, ‘10H’) change with every ITRDY = ‘1’.

As there are now internal counters for data packing implemented (see sect. 8.5.4.2 and parameters PGHAPS, PGHBPS and PGHCPS), the ITRDY packing is mainly useful for burst data transfers.

The IDQ output pin may be defined to be a gated clock output signal (ICLK AND internal IDQ).

9.7.2 X-PORT INPUT TIMING

At the X-port the input timing requirements are the same as those for the I-port output. But different to those below:

- It is not necessary to mark invalid cycles with a 00H code
- No constraints on the input qualifier (can be a random pattern)
- XCLK may be a gated clock (XCLK AND external XDQ).

Remark: All timings illustrated in figures 33 to 39 are given for an uninterrupted output stream (no handshake with the external hardware).

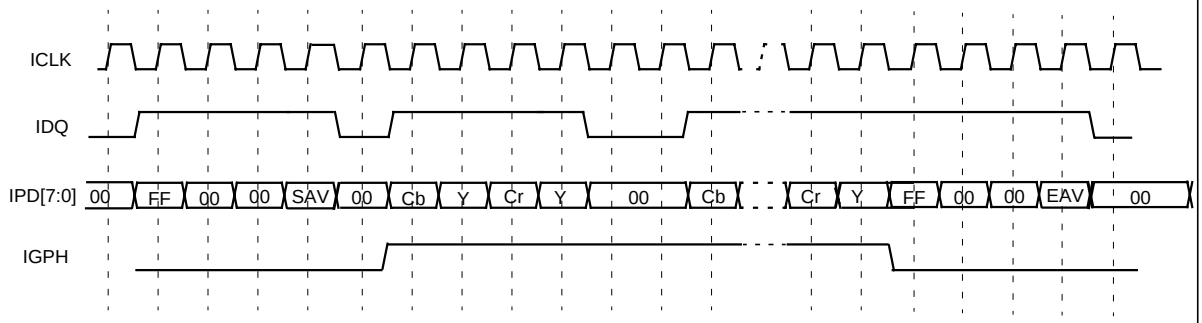


Fig.33 Output Timing I-port for serial 8 Bit Data
(ICODE = 1, INS80 = 0)

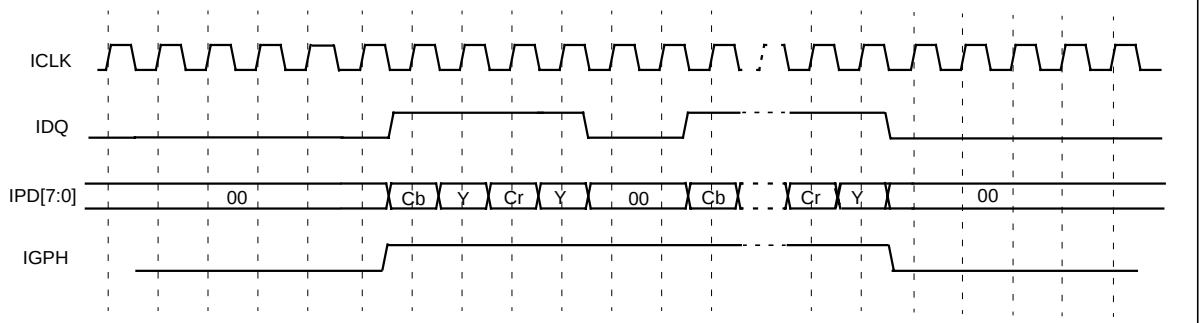


Fig.34 Output Timing I-port for serial 8 Bit Data
(ICODE = 0, INS80 = 0)

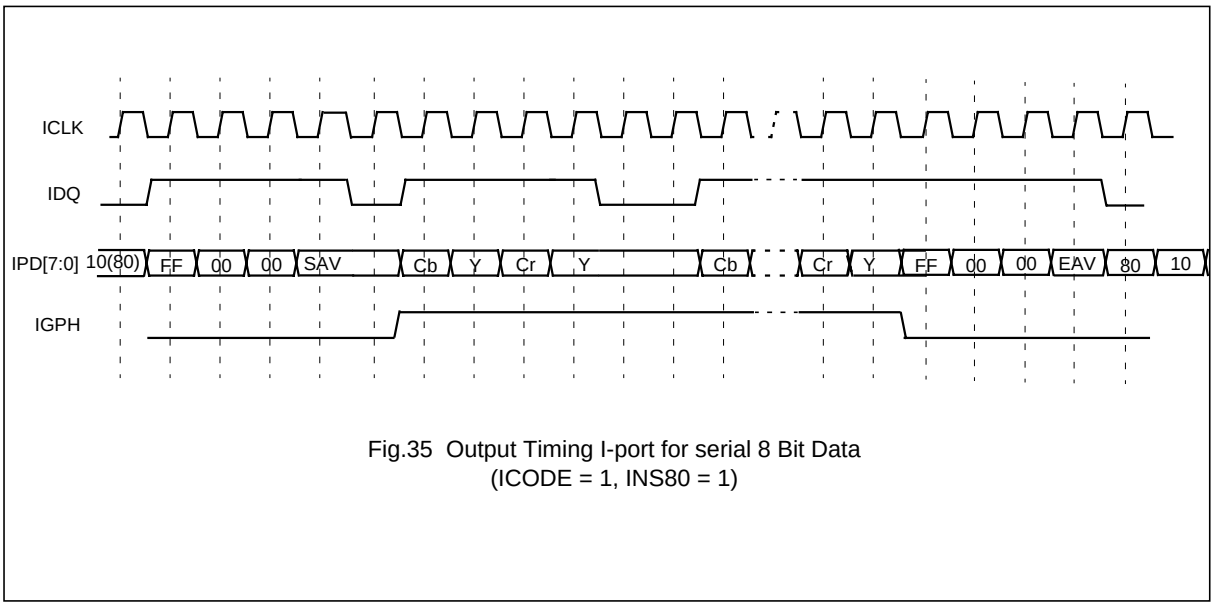


Fig.35 Output Timing I-port for serial 8 Bit Data
(ICODE = 1, INS80 = 1)

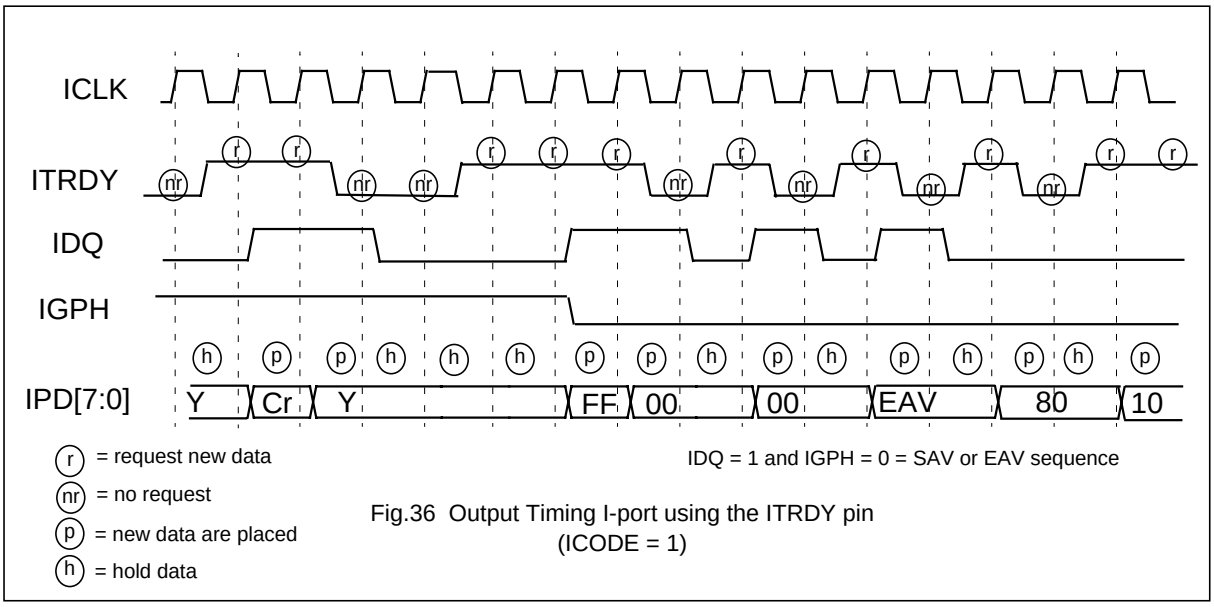


Fig.36 Output Timing I-port using the ITRDY pin
(ICODE = 1)

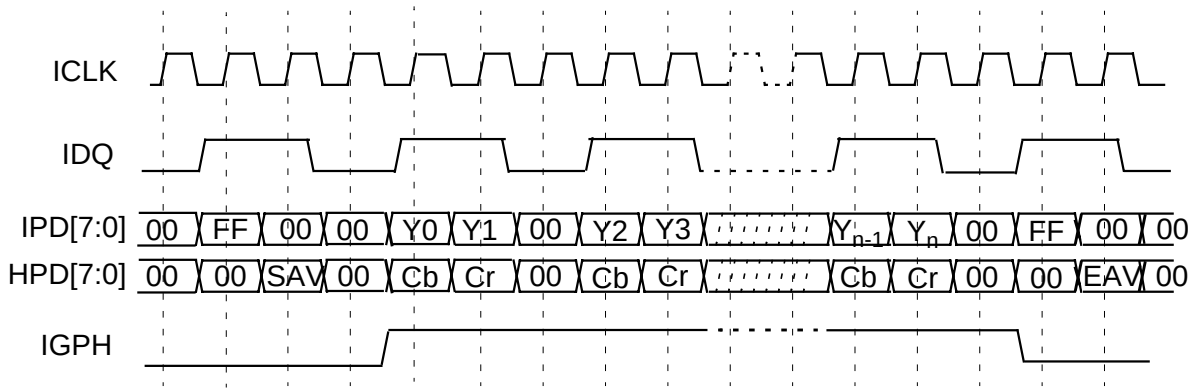


Fig.37 Output Timing for 16 Bit Data output via I-port and H-port with codes (ICODE = 1, INS80 = 0), timing is like 8 bit output, but packages of 2 bytes per valid cycle

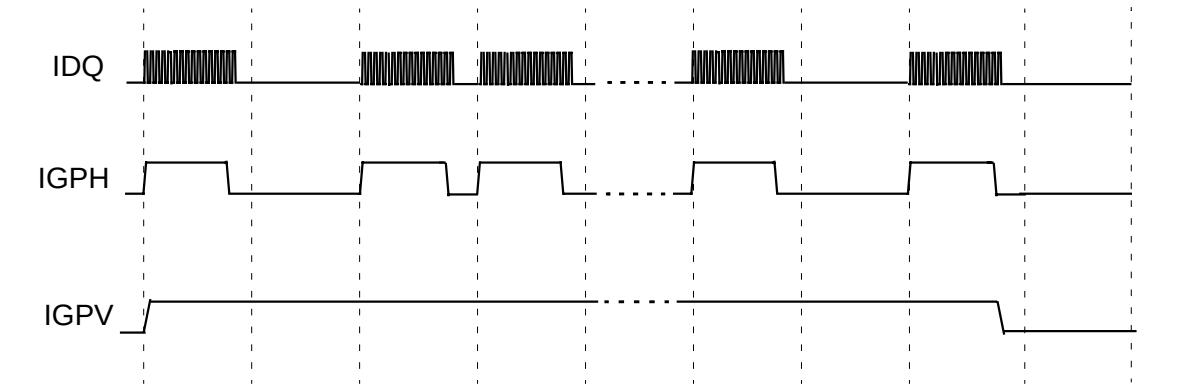


Fig.38 the scalers H-gate and V-gate output timing

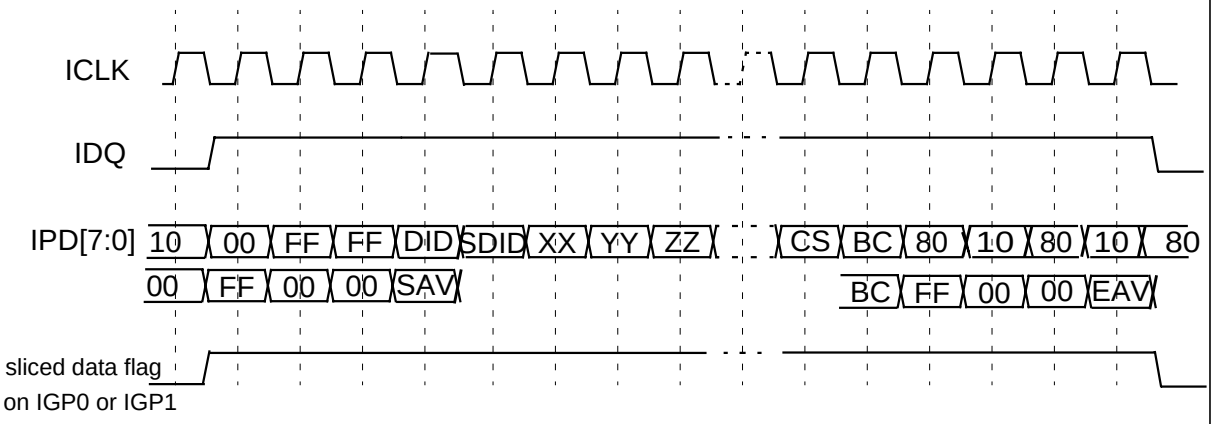


Fig.39 Output Timing for sliced VBI data in 8 Bit serial output mode (for INS80 = 1)

10 BOUNDARY SCAN TEST

The SAA7115 has built-in logic and 5 dedicated pins to support boundary scan testing which allows board testing without special hardware (nails). The SAA7115 follows the *"IEEE Std. 1149.1 - Standard Test Access Port and Boundary-Scan Architecture"* set by the Joint Test Action Group (JTAG) chaired by Philips.

The 5 special pins are Test Mode Select (TMS), Test Clock (TCK), Test Reset (TRSTN), Test Data Input (TDI) and Test Data Output (TDO).

The Boundary Scan Test (BST) functions BYPASS, EXTEST, INTEST, SAMPLE, CLAMP and IDCODE are all supported (see Table 42). Details about the JTAG BST-TEST can be found in specification "*IEEE Std. 1149.1"*. A file containing the detailed Boundary Scan Description Language (BSDL) description of the SAA7115 is available on request.

Table 42 BST instructions supported by the SAA7115

INSTRUCTION	DESCRIPTION
BYPASS	This mandatory instruction provides a minimum length serial path (1 bit) between TDI and TDO when no test operation of the component is required.
EXTEST	This mandatory instruction allows testing of off-chip circuitry and board level interconnections.
SAMPLE	This mandatory instruction can be used to take a sample of the inputs during normal operation of the component. It can also be used to preload data values into the latched outputs of the boundary scan register.
CLAMP	This optional instruction is useful for testing when not all ICs have BST. This instruction addresses the bypass register while the boundary scan register is in external test mode.
IDCODE	This optional instruction will provide information on the components manufacturer, part number and version number.
INTEST	This optional instruction allows testing of the internal logic (no customer support available).
USER1	This private instruction allows testing by the manufacturer (no customer support available).

10.1 Initialization of boundary scan circuit

The TAP (Test Access Port) controller of an IC should be in the reset state (TEST_LOGIC_RESET) when the IC is in functional mode. This reset state also forces the instruction register into a functional instruction such as IDCODE or BYPASS.

To solve the power-up reset, the standard specifies that the TAP controller will be forced asynchronously to the TEST_LOGIC_RESET state by setting the TRSTN pin LOW.

10.2 Device identification codes

A device identification register is specified in *"IEEE Std. 1149.1b-1994"*. It is a 32-bit register which contains fields for the specification of the IC manufacturer, the IC part number and the IC version number. Its biggest advantage is the possibility to check for the correct ICs mounted after production and determination of the version number of ICs during field service.

When the IDCODE instruction is loaded into the BST instruction register, the identification register will be connected between TDI and TDO of the IC. The identification register will load a component specific code during the CAPTURE_DATA_REGISTER state of the TAP controller and this code can subsequently be shifted out. At board level this code can be used to verify component manufacturer, type and version number. The device identification register contains 32 bits, numbered 31 to 0, where bit 31 is the most significant bit (nearest to TDI) and bit 0 is the least significant bit (nearest to TDO); see Fig.40.

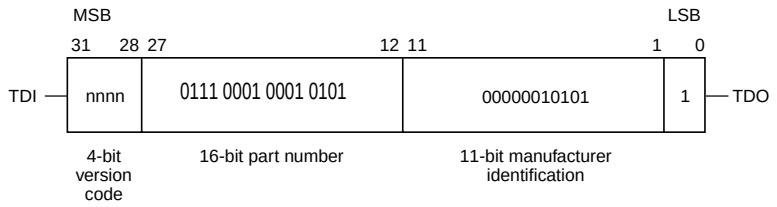


Fig.40 32 bits of identification code.

11 LIMITING VALUES

Table 43 Limiting Values

SYMBOL	PARAMETER	Conditions	MIN	MAX	UNIT
VDDx	supply voltage digital		-0.5	+4.6	V
VDDAx	supply voltage analog		-0.5	+4.6	V
VIA	input voltage at analog inputs	note 3	-0.5	VDDA + 0.5 (4.6 max)	V
VOA	output voltage at analog output		-0.5	VDDA + 0.5	V
VID	input voltage at digital inputs	outputs in tristate, note 2, 3	-0.5	+5.5	V
VOD	output voltage at digital outputs	outputs active	-0.5	VDDx + 0.5	V
VdiffGND	difference voltage between VSSAall and VSSall		-	100	mV
Tstg	storage temperature		-65	+150	°C
Tamb	operating ambient temperature range		0	+70	°C
VESD	electrostatic handling for all pins	note 1	-2000	+2000	V

Note
1. Equivalent to discharging a 100pF capacitor through an 1.5kW series resistor (Human Body Model)
2. With the exception of pin XTALI
3. The chip must be supplied correctly with at least the minimum supply voltage of 3.0V

12 THERMAL CHARACTERISTICS

Table 44 Thermal characteristics

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	52.5	K/W

13 CHARACTERISTICS

Table 45 Characteristics

V_{DDD} = 3.0 to 3.6 V; V_{DDA} = 3.1 to 3.5 V; T_{amb} = 25 °C; timings and levels refer to drawings and conditions illustrated in Fig.41; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
I_{DDD}	digital supply current	X-port 3-state; 8-bit I-port	–	**TBD.**	–	mA
P_D	power dissipation digital part		–	tbd.	–	mW
V_{DDA}	analog supply voltage		3.1	3.3	3.5	V
I_{DDA}	analog supply current	AOSL1 and AOSL0 = 0				
		CVBS mode	–	tbd.	–	mA
		Y/C mode	–	tbd.	–	mA
		component mode	–	tbd.	–	mA
P_A	power dissipation analog part	CVBS mode	–	tbd.	–	mW
		Y/C mode	–	tbd.	–	mW
		component mode	–	tbd.	–	mW
$P_{tot(A+D)}$	total power dissipation analog and digital part	CVBS mode	–	tbd.	–	mW
		Y/C mode	–	tbd.	–	mW
$P_{tot(A+D)(pd)}$	total power dissipation analog and digital part in power-down mode	CE pulled down to ground	–	**TBD.**	–	mW
$P_{tot(A+D)(ps)}$	total power dissipation analog and digital part in power-save mode	I^2C-bus controlled via subaddress 88H	–	tbd.	–	mW
$P_{tot(A+D)(ps)}$	total power dissipation analog and digital part in power-save mode	Controlled via chip enable input (CE, Pin 27)	–	tbd.	–	mW
Analog part						
I_{clamp}	clamping current	V_I = 1 V DC	–	±8	–	µA
$V_{i(p-p)}$	input voltage (peak-to-peak value)	for normal video levels 1 V (p-p), –3 dB termination 18/56 Ω and AC coupling required; coupling capacitor is 47 nF	–	0.7	–	V
$\lvert Z_i \rvert$	input impedance	clamping current off	200	–	–	kΩ
C_i	input capacitance		–	–	10	pF
α_{cs}	channel crosstalk	f_i < 5 MHz	–	–	–50	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
9-bit analog-to-digital converters						
B	analog bandwidth	at −3 dB	–	7	–	MHz
ϕ_{diff}	differential phase	amplifier plus anti-alias filter bypassed	–	2	–	deg
G_{diff}	differential gain	amplifier plus anti-alias filter bypassed	–	2	–	%
$f_{clk(ADC)}$	ADC clock frequency		25.4	–	28.6	MHz
$LE_{dc(d)}$	DC differential linearity error		–	0.7	–	LSB
$LE_{dc(i)}$	DC integral linearity error		–	1	–	LSB
ΔG_{ADC}	ADC gain inequality	$\left(\frac{\text{maximum deviation}}{\text{minimum deviation}} - 1\right) \times 100$ note 1	–	3	–	%
Digital inputs						
$V_{IL(SCL,SDA)}$	LOW-level input voltage pins SDA and SCL	note 2	–0.5	–	$+0.3V_{DD(I2C)}$	V
$V_{IH(SCL,SDA)}$	HIGH-level input voltage pins SDA and SCL	note 2	$0.7V_{DD(I2C)}$	–	$V_{DD(I2C)}$ + 0.5	V
$V_{IL(XTALI)}$	LOW-level CMOS input voltage pin XTALI		–0.3	–	+0.8	V
$V_{IH(XTALI)}$	HIGH-level CMOS input voltage pin XTALI		2.0	–	V_{DDD} + 0.3	V
$V_{IL(n)}$	LOW-level input voltage all other inputs		–0.3	–	+0.8	V
$V_{IH(n)}$	HIGH-level input voltage all other inputs		2.0	–	5.5	V
I_{LI}	input leakage current		–	–	1	µA
$I_{LI/O}$	I/O leakage current		–	–	10	µA
C_i	input capacitance	I/O at high-impedance	–	–	8	pF
Digital outputs; note 3						
$V_{OL(SDA)}$	LOW-level output voltage pin SDA	SDA at 3 mA sink current	–	–	0.4	V
$V_{OL(clk)}$	LOW-level output voltage for clocks		–0.5	–	+0.6	V
$V_{OH(clk)}$	HIGH-level output voltage for clocks		2.4	–	V_{DDD} + 0.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{OL(n)}$	LOW-level output voltage all other digital outputs		0	–	0.4	V
$V_{OH(n)}$	HIGH-level output voltage all other digital outputs		2.4	–	V_{DDD} + 0.5	V
Clock output timing (LLC and LLC2); note 4						
C_L	output load capacitance		15	–	50	pF
T_{cy}	cycle time	pin LLC	35	–	39	ns
		pin LLC2	70	–	78	ns
δ	duty factors t_{CLKH}/T_{cy}	C_L = 40 pF	40	–	60	%
t_r	rise time LLC and LLC2	0.2 V to V_{DDD} − 0.2 V	–	–	5	ns
t_f	fall time LLC and LLC2	V_{DDD} − 0.2 V to 0.2 V	–	–	5	ns
$t_{d(LLC-LLC2)}$	delay time between LLC and LLC2 output	measured at 1.5 V; C_L = 25 pF	tbd.	–	tbd.	ns
Horizontal PLL						
$f_{hor(n)}$	nominal line frequency	50 Hz field	–	15625	–	Hz
		60 Hz field	–	15734	–	Hz
$\Delta f_{hor}/f_{hor(n)}$	permissible static deviation		–	–	5.7	%
Subcarrier PLL						
$f_{sc(n)}$	nominal subcarrier frequency	PAL BGHI	–	4433619	–	Hz
		NTSC M	–	3579545	–	Hz
		PAL M	–	3575612	–	Hz
		PAL N	–	3582056	–	Hz
Δf_{sc}	lock-in range		±400	–	–	Hz
Crystal oscillator for 32.11 MHz; note 5						
$f_{xtal(nom)}$	nominal frequency	3rd harmonic	–	32.11	–	MHz
$\Delta f_{xtal(nom)}$	permissible nominal frequency deviation		–	–	$\pm 70 \times 10^{-6}$	
$\Delta f_{xtal(nom)(T)}$	permissible nominal frequency deviation with temperature		–	–	$\pm 30 \times 10^{-6}$	
CRYSTAL SPECIFICATION (X1)						
$T_{amb(X1)}$	ambient temperature		0	–	70	°C
C_L	load capacitance		8	–	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R_s	series resonance resistor		–	40	80	Ω
C_1	motional capacitance		–	1.5 ±20%	–	fF
C_0	parallel capacitance		–	4.3 ±20%	–	pF
Crystal oscillator for 24.576 MHz; note 5						
$f_{xtal(n)}$	nominal frequency	3rd harmonic	–	24.576	–	MHz
$\Delta f_{xtal(n)}$	permissible nominal frequency deviation		–	–	$\pm 50 \times 10^{-6}$	
$\Delta f_{xtal(n)(T)}$	permissible nominal frequency deviation with temperature		–	–	$\pm 20 \times 10^{-6}$	
CRYSTAL SPECIFICATION (X1)						
$T_{amb(X1)}$	ambient temperature		0	–	70	°C
C_L	load capacitance		8	–	–	pF
R_s	series resonance resistor		–	40	80	Ω
C_1	motional capacitance		–	1.5 ±20%	–	fF
C_0	parallel capacitance		–	3.5 ±20%	–	pF
Expansion port (X-Port) output timing with XCLK clock output						
T_{cy}	cycle time	XCLK output	35	–	39	ns
C_L	output load capacitance		15	–	50	pF
δ	duty factors for t_{XCLKH}/t_{XCLKL}		tbd.	–	tbd.	%
t_r	rise time	0.6 to 2.6 V	–	–	tbd.	ns
t_f	fall time	2.6 to 0.6 V	–	–	tbd.	ns
Data and control signal output timing X-port including RT port, related to XCLK output (for XPCK[1:0] 83H[5:4] = 11); note 4						
C_L	output load capacitance		15	–	50	pF
$t_{OHD;DAT}$	output data hold time	**VALID FOR OUTPUTS: XPD [7:0], XRH, XRV, XDQ, RTS0, RTS1, RTCO**	tbd.	-	–	ns
t_{PD}	propagation delay from positive edge of XCLK output		-	-	tbd.	ns
Expansion port (X-Port) input timing with XCLK clock input						
T_{cyX}	XCLK cycle time	XCLK input	31	–	45	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
δ	duty factor: t_{XCLKH}/T_{cy}		tbd.	50	tbd.	%
t_r	rise time		–	–	5	ns
t_f	fall time		–	–	5	ns
Data and control signal input timing X-port, related to XCLK input (for XPCK[1:0] 83H[5:4] = 11);						
$t_{SU;DAT}$	input data set-up time	**VALID FOR INPUTS: XPD [7:0], HPD [7:0], XRH, XRV, XDQ**	tbd.	-	–	ns
$t_{HD;DAT}$	input data hold time		–	-	tbd.	ns
$t_{OHD;DAT}$	output data hold time	**VALID FOR OUTPUT: XRDY**	tbd.	-	–	ns
t_{PD}	propagation delay from positive edge of XCLK input		-	-	tbd.	ns
Image port (I-Port) output timing with ICLK clock output						
C_L	output load capacitance		15	–	50	pF
T_{cy}	cycle time		31	–	90	ns
δ	duty factor: t_{ICLKH}/t_{ICLKL}	C_L = 40 pF	tbd.	–	tbd.	%
t_r	rise time	0.6 to 2.6 V	–	–	5	ns
t_f	fall time	2.6 to 0.6 V	–	–	5	ns
Data and control signal output timing I-port, related to ICLK output (for IPCK[1:0] 87H[5:4] = 11)						
C_L	output load capacitance at all outputs		15	–	50	pF
$t_{OHD;DAT}$	output data hold time	**VALID FOR OUTPUTS: IPD [7:0], HPD [7:0], IGPH, IGPV, IDQ, IGP1, IGP0**	tbd.	-	–	ns
$t_{o(d)}$	output delay time		–	-	23	ns
Data and control signal input timing I-port, related to ICLK output (for IPCK[1:0] 83H[5:4] = 11);						
$t_{SU;DAT}$	input data set-up time	Valid for input: ITRDY	18	-	–	ns
$t_{HD;DAT}$	input data hold time		–	-	tbd.	ns
Image port (I-Port) output timing with ICLK clock input						
T_{cy}	cycle time		31	–	100	ns
δ	duty factors: t_{ICLKH}/Tcy		tbd.	50	tbd.	%
t_r	rise time	0.6 to 2.6 V	–	–	5	ns
t_f	fall time	2.6 to 0.6 V	–	–	5	ns
Data and control signal output timing I-port, related to ICLK input (for IPCK[1:0] 87H[5:4] = 11)						

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_L	output load capacitance at all outputs		15	–	50	pF
$t_{OHD;DAT}$	output hold time	**VALID FOR OUTPUTS: IPD [7:0], HPD [7:0], IGPH, IGPV, IDQ, IGP1, IGP0**	tbd.	-	–	ns
t_{PD}	propagation delay from positive edge of LLC output		–	-	tbd.	ns
Data and control signal input timing I-port, related to ICLK input (for IPCK[1:0] 83H[5:4] = 11);						
$t_{SU;DAT}$	input data set-up time	Valid for input: ITRDY	tbd.	-	–	ns
$t_{HD;DAT}$	input data hold time		–	-	tbd.	ns
AMCLK clock output						
C_L	output load capacitance		15	–	50	pF
t_r	rise time	0.6 to 2.6 V	–	–	5	ns
t_f	fall time	2.6 to 0.6 V	–	–	5	ns

Notes

1. ADC1 is not taken into account, since component video is always converted by ADC2, ADC3 and ADC4.
2. $V_{DD(I2C)}$ is the supply voltage of the I^2C-bus. For $V_{DD(I2C)}$ = 3.3 V is $V_{IL(SCL,SDA)(max)}$ = 1 V; for $V_{DD(I2C)}$ = 5 V is $V_{IL(SCL,SDA)(max)}$ = 1.5 V. For $V_{DD(I2C)}$ = 3.3 V is $V_{IH(SCL,SDA)(min)}$ = 2.3 V; for $V_{DD(I2C)}$ = 5 V is $V_{IH(SCL,SDA)(min)}$ = 3.5 V.
3. The levels must be measured with load circuits; 1.2 kΩ at 3 V (TTL load); C_L = 50 pF.
4. The effects of rise and fall times are included in the calculation of $t_{OHD;DAT}$ and t_{PD}. Timings and levels refer to drawings and conditions illustrated in Fig.41.
5. The crystal oscillator drive level is typical 0.28 mW.

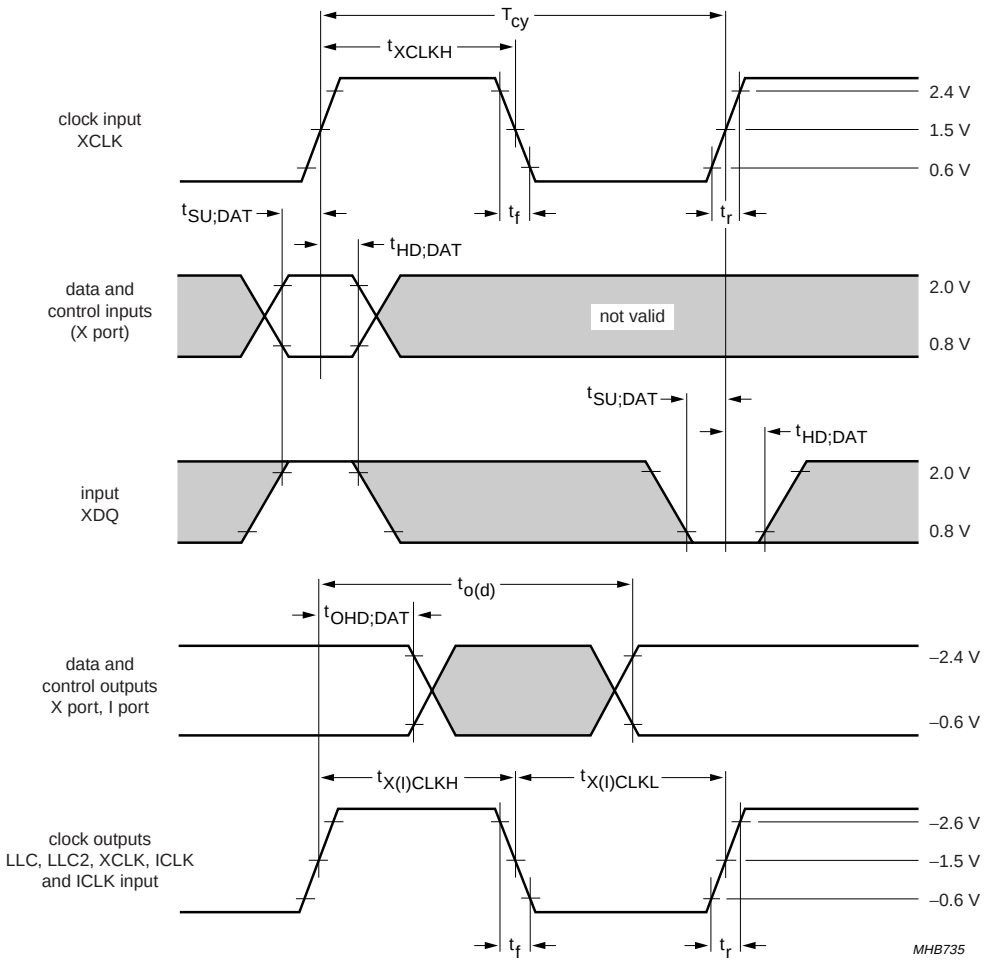


Fig.41 Data input/output timing diagram (X-port, RT port and I-port).

14 APPLICATION INFORMATION

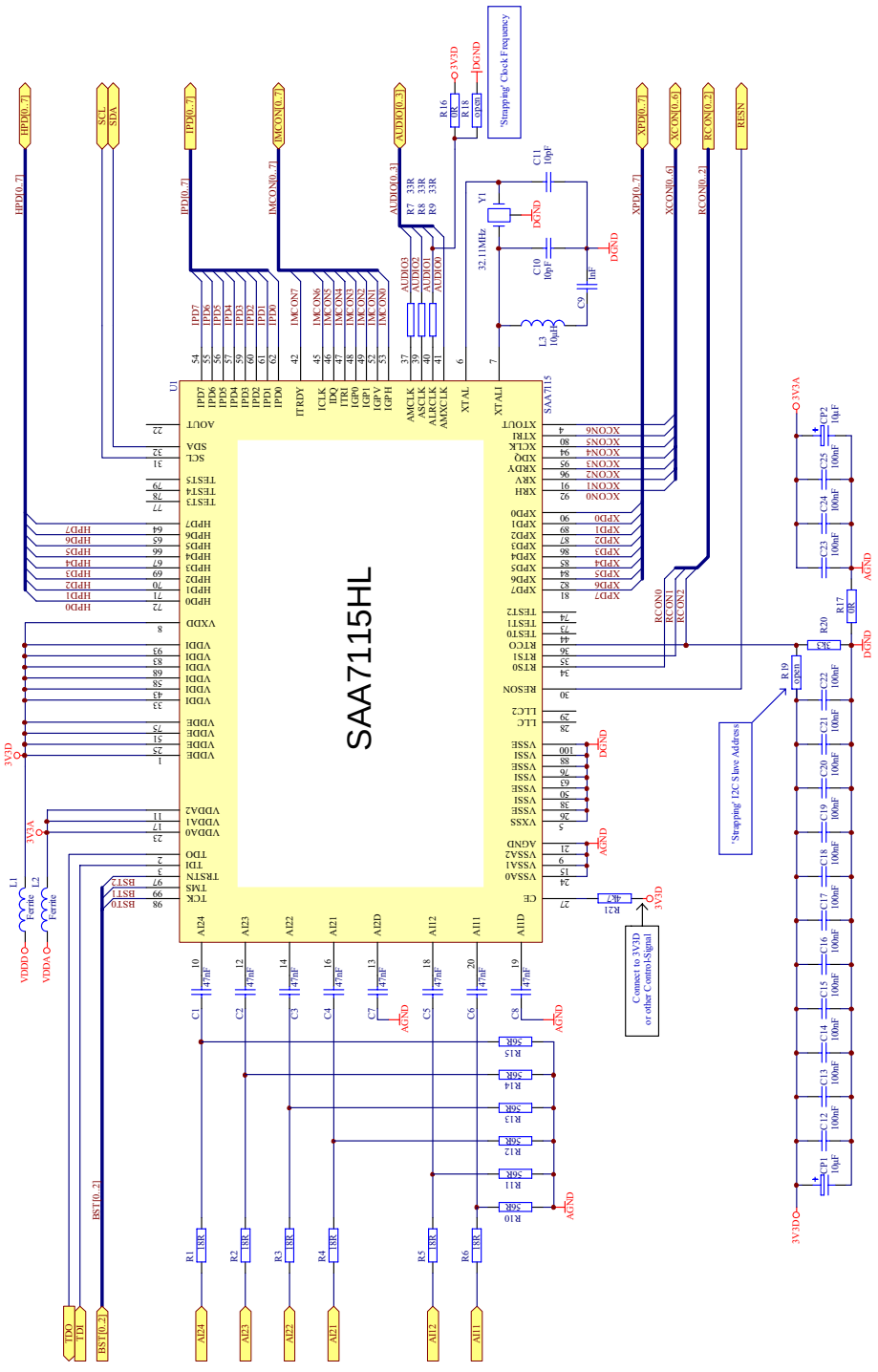
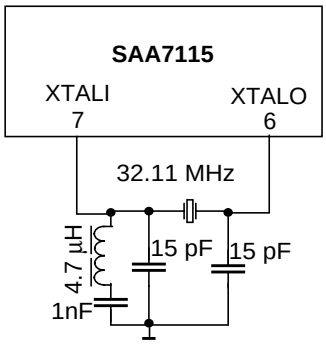
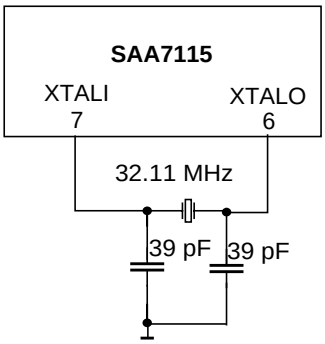


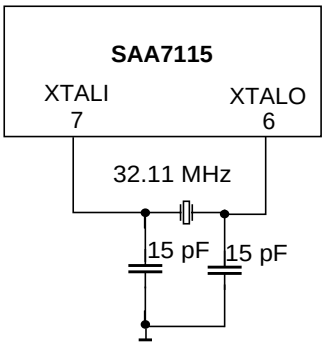
Fig.42 Application example



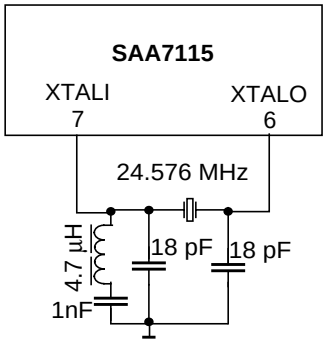
(1a) With 3rd harmonic quartz.
Crystal load = 8 pF



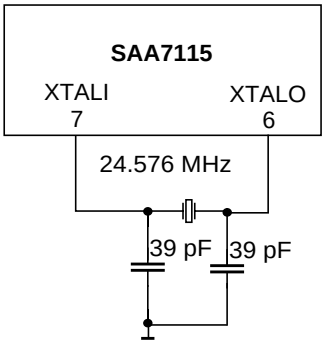
(1b) With fundamental quartz.
Crystal load = 20 pF



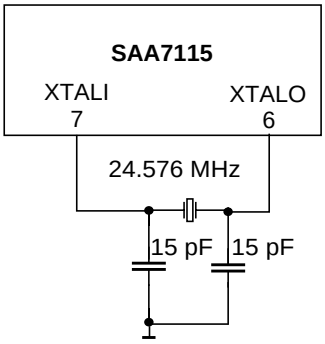
(1c) With fundamental quartz.
Crystal load = 8 pF



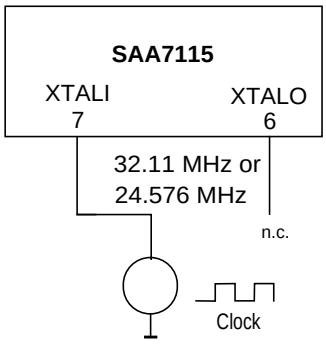
(2a) With 3rd harmonic quartz.



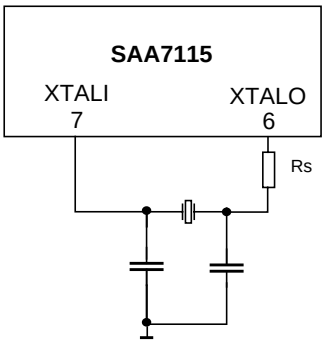
(2b) With fundamental quartz.



(2c) With fundamental quartz.



(3a) With direct clock

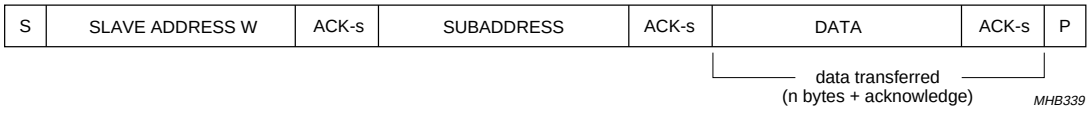


(3b) With fundamental quartz crystal and restricted drive level. When Pdrive of the internal oscillator is too high a resistance Rs can be placed in series with the output of the oscillator XTALO.
Note: The decreased crystal amplitude results in a lower drive level but on the other hand the jitter performance will decrease.

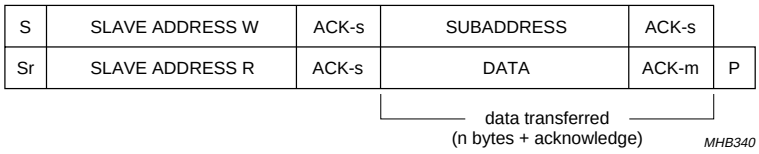
Fig.43 Oscillator applications

15 DEVICE PROGRAMMING OVERVIEW

15.1 I2C-bus description



a. Write procedure.



b. Read procedure (combined).

Fig.44 I^2C-bus format.

Table 46 Description of I^2C-bus format

CODE	DESCRIPTION
S	START condition
Sr	repeated START condition
SLAVE ADDRESS W	‘0100 0010’ (42H, default) or ‘0100 0000’ (40H; note 1)
SLAVE ADDRESS R	‘0100 0011’ (43H, default) or ‘0100 0001’ (41H; note 1)
ACK-s	acknowledge generated by the slave
ACK-m	acknowledge generated by the master
SUBADDRESS	subaddress byte; see Tables 47 and 48
DATA	data byte; see figure 44; if more than one byte DATA is transmitted the subaddress pointer is automatically incremented
P	STOP condition
X	read/write control bit (LSB slave address); X = 0, order to write (the circuit is slave receiver); X = 1, order to read (the circuit is slave transmitter)

Note

1. If pin RTCO strapped to supply voltage via a 4.7 kΩ resistor.

15.2 Register Overview

Table 47 Subaddress description and access

SUBADDRESS	DESCRIPTION	ACCESS (READ/WRITE)
00H	chip version	read only
Video decoder: 01H to 2FH		
01H to 05H	front-end part	read and write
06H to 19H	decoder part	read and write
1AH to 1DH	color decoding, misc	read and write
1EH to 1FH	video decoder status byte	read only
20H to 2FH	reserved	–
Audio clock generation: 30H to 3FH		
30H to 3AH	audio clock generator	read and write
3BH to 3FH	reserved	–
General purpose VBI-data slicer: 40H to 7FH		
40H to 5BH	VBI-data slicer	read and write
5CH	reserved	–
5DH to 5EH	VBI-data slicer	read and write
5FH	reserved	–
60H to 65H	VBI-data slicer status	read only
66H to 7FH	I^2C readback of sliced VBI data	read only
X-port, I-port, scaler and power save control: 80H to EFH		
80H to 8FH	task independent global settings	read and write
90H to BFH	task A definition	read and write
C0H to EFH	task B definition	read and write
Second PLL (PLL2) and Pulsegenerator: F0H to FFH		
F0H to F4H	Second PLL settings	read and write
F5H to FBH	Pulsegenerator	read and write
FCH to FEH	reserved	read and write
FFH	Second PLL, lock status definition	read and write

Table 48 I²C-subaddress Overview(1)

REGISTER FUNCTION	SUB ADDR	D7	D6	D5	D4	D3	D2	D1	D0
Register 00 to 2F used by chip version part									
Chip version (read only)	00	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Registers 01 to 1F used by the video decoder part									
Increment Delay	01	AOSL2	WPOFF	GUDL1	GUDL0	IDEL3	IDEL2	IDEL1	IDEL0
Analog Input Control 1	02	FUSE1	FUSE0	0	0	MODE3	MODE2	MODE1	MODE0
Analog Input Control 2	03	TEST	HLNRS	VBSL	CPOFF	HOLDG	GAFIX	GAI28	GAI18
Analog Input Control 3	04	GAI17	GAI16	GAI15	GAI14	GAI13	GAI12	GAI11	GAI10
Analog Input Control 4	05	GAI27	GAI26	GAI25	GAI24	GAI23	GAI22	GAI21	GAI20
Horizontal sync start	06	HSB7	HSB6	HSB5	HSB4	HSB3	HSB2	HSB1	HSB0
Horizontal sync stop	07	HSS7	HSS6	HSS5	HSS4	HSS3	HSS2	HSS1	HSS0
Sync Control	08	AUFD	FSEL	FOET	HTC1	HTC0	HPLL	VNOI1	VNOI0
Luminance Control	09	BYPS	YCOMB	LDEL	LUBW	LUFI3	LUFI2	LUFI1	LUFI0
Luminance Brightness adjustment	0A	DBRI7	DBRI6	DBRI5	DBRI4	DBRI3	DBRI2	DBRI1	DBRI0
Luminance Contrast adjustment	0B	DCON7	DCON6	DCON5	DCON4	DCON3	DCON2	DCON1	DCON0
Chroma Saturation adjustment	0C	DSAT7	DSAT6	DSAT5	DSAT4	DSAT3	DSAT2	DSAT1	DSAT0
Chroma Hue control	0D	HUEC7	HUEC6	HUEC5	HUEC4	HUEC3	HUEC2	HUEC1	HUEC0
Chroma Control 1	0E	CDTO	CSTD2	CSTD1	CSTD0	DCVF	FCTC	AUTO0	CCOMB
Chroma Gain Control	0F	ACGC	CGAIN6	CGAIN5	CGAIN4	CGAIN3	CGAIN2	CGAIN1	CGAIN0
Chroma Control 2	10	OFFU1	OFFU0	OFFV1	OFFV0	CHBW	LCBW2	LCBW1	LCBW0
Mode/Delay Control	11	COLO	RTP1	HDEL1	HDEL0	RTP0	YDEL2	YDEL1	YDEL0
RT signal Control	12	RTSE13	RTSE12	RTSE11	RTSE10	RTSE03	RTSE02	RTSE01	RTSE00
RT / X-port output Control	13	RTCE	XRHS	XRVS1	XRVS0	HLSEL	OFTS2	OFTS1	OFTS0
analog / ADC / compatibility control	14	CM99	UPTCV	AOSL1	AOSL0	XTOUTE	AUTO1	APCK1	APCK0
VGATE start, FID change	15	VSTA7	VSTA6	VSTA5	VSTA4	VSTA3	VSTA2	VSTA1	VSTA0
VGATE stop	16	VSTO7	VSTO6	VSTO5	VSTO4	VSTO3	VSTO2	VSTO1	VSTO0

(1) Colour codes in this table:
- green: new or modified functionality (related to ALL previous decoder designs),
- yellow: new or modified functionality already realized in SAA7118 (where SAA7115 is mainly derived from)
- red: hidden functionality

REGISTER FUNCTION	SUB ADDR	D7	D6	D5	D4	D3	D2	D1	D0
MISC / VGATE MSB's	17	LLCE	LLC2E	LATY2	LATY1	LATY0	VGPS	VSTO8	VSTA8
Raw Data Gain	18	RAWG7	RAWG6	RAWG5	RAWG4	RAWG3	RAWG2	RAWG1	RAWG0
Raw Data Offset	19	RAWO7	RAWO6	RAWO5	RAWO4	RAWO3	RAWO2	RAWO1	RAWO0
ColorKiller Thresholds	1A	QTHR3	QTHR2	QTHR1	QTHR0	STHR3	STHR2	STHR1	STHR0
MISC /TVVCRDET	1B	ATVT1	ATVT0	0	OFTS3	0	0	ACOL	FSQC
enhanced comb ctrl1	1C	HODG1	HODG0	VEDG1	VEDG0	MEDG1	MEDG0	CMBT1	CMBT0
enhanced comb ctrl2	1 D	0	0	0	0	0	0	VEDT1	VEDT0
Status Byte Decoder 1 (read only)	1E	NFLD	HLCK	SLTCA	GLIMT	GLIMB	WIPA	DCSTD1	DCSTD0
Status Byte Decoder 2 (read only)	1F	INTL	HLVLN	FIDT	STTB	TYPE3	COLSTR	COPRO	RDCAP
Registers 20 to 2F reserved for future extensions (e.g. component processing saa7118+)									
reserved	20 to 2F	0	0	0	0	0	0	0	0
Registers 30 to 3F used by audio clock generator									
audio master clock cycles per field	30	ACPF7	ACPF6	ACPF5	ACPF4	ACPF3	ACPF2	ACPF1	ACPF0
audio master clock cycles per field	31	ACPF15	ACPF14	ACPF13	ACPF12	ACPF11	ACPF10	ACPF9	ACPF8
audio master clock cycles per field	32	0	0	0	0	0	0	ACPF17	ACPF16
reserved for future extensions	33	0	0	0	0	0	0	0	0
audio master clock nominal increment	34	ACNI7	ACNI6	ACNI5	ACNI4	ACNI3	ACNI2	ACNI1	ACNI0
audio master clock nominal increment	35	ACNI15	ACNI14	ACNI13	ACNI12	ACNI11	ACNI10	ACNI9	ACNI8
audio master clock nominal increment	36	0	0	ACNI21	ACNI20	ACNI19	ACNI18	ACNI17	ACNI16
reserved for future extensions	37	0	0	0	0	0	0	0	0
clock ratio AMXCLK to ASCLK	38	0	0	SDIV5	SDIV4	SDIV3	SDIV2	SDIV1	SDIV0
clock ratio ASCLK to ALRCLK	39	0	0	LRDIV5	LRDIV4	LRDIV3	LRDIV2	LRDIV1	LRDIV0
audio clock gen. basic setup	3A	UCGC	CGCDIV	0	0	APLL	AMVR	LRPH	SCPH
reserved	3B to 3F	0	0	0	0	0	0	0	0
Registers 40 to 7F used by general purpose VBI data slicer									
AC1	40	CHKWSS	HAM_N	FCE	HUNT_N	0	0	0	0
LCR2	41	LCR02_7	LCR02_6	LCR02_5	LCR02_4	LCR02_3	LCR02_2	LCR02_1	LCR02_0

REGISTER FUNCTION	SUB ADDR	D7	D6	D5	D4	D3	D2	D1	D0
LCR3	42	LCR03_7	LCR03_6	LCR03_5	LCR03_4	LCR03_3	LCR03_2	LCR03_1	LCR03_0
...	...	...	...	...	...	...	...	...	...
LCR23	56	LCR23_7	LCR23_6	LCR23_5	LCR23_4	LCR23_3	LCR23_2	LCR23_1	LCR23_0
LCR24	57	LCR24_7	LCR24_6	LCR24_5	LCR24_4	LCR24_3	LCR24_2	LCR24_1	LCR24_0
FC	58	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0
HOFF	59	HOFF7	HOFF6	HOFF5	HOFF4	HOFF3	HOFF2	HOFF1	HOFF0
VOFF	5A	VOFF7	VOFF6	VOFF5	VOFF4	VOFF3	VOFF2	VOFF1	VOFF0
HVOFF	5B	FOFF	0	VEP	VOFF8	0	HOFF10	HOFF9	HOFF8
reserved	5C	0	0	0	0	0	0	0	0
sliced data output mode	5D	0	0	0	SLDOM4	SLDOM3	SLDOM2	SLDOM1	SLDOM0
D7,D6 are read only, 2nd text data ident. code SDID	5E	FC8V	FC7V	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0
reserved	5F	0	0	0	0	0	0	0	0
reserved (don't use)	65	-	-	-	-	-	-	-	-
i2c-Readback 1 CC-header	66	CCH_7	CCH_6	CCH_5	CCH_4	CCH_3	CCH_2	CCH_1	CCH_0
i2c-Readback 2 CC-odd byte 1	67	CCO1_7	CCO1_6	CCO1_5	CCO1_4	CCO1_3	CCO1_2	CCO1_1	CCO1_0
i2c-Readback 3 CC-odd byte 2	68	CCO2_7	CCO2_6	CCO2_5	CCO2_4	CCO2_3	CCO2_2	CCO2_1	CCO2_0
i2c-Readback 4 CC-even byte 1	69	CCE1_7	CCE1_6	CCE1_5	CCE1_4	CCE1_3	CCE1_2	CCE1_1	CCE1_0
i2c-Readback 5 CC-even byte 2	6A	CCE2_7	CCE2_6	CCE2_5	CCE2_4	CCE2_3	CCE2_2	CCE2_1	CCE2_0
i2c-Readback 6 WSS-header	6B	WSSH_7	WSSH_6	WSSH_5	WSSH_4	WSSH_3	WSSH_2	WSSH_1	WSSH_0
i2c-Readback 7 WSS-odd byte 1	6C	WSSO1_7	WSSO1_6	WSSO1_5	WSSO1_4	WSSO1_3	WSSO1_2	WSSO1_1	WSSO1_0
i2c-Readback 8 WSS-odd byte 2	6D	WSSO2_7	WSSO2_6	WSSO2_5	WSSO2_4	WSSO2_3	WSSO2_2	WSSO2_1	WSSO2_0
i2c-Readback 9 WSS-odd byte 3	6E	WSSO3_7	WSSO3_6	WSSO3_5	WSSO3_4	WSSO3_3	WSSO3_2	WSSO3_1	WSSO3_0
i2c-Readback 10 WSS-even byte 1	6F	WSSE1_7	WSSE1_6	WSSE1_5	WSSE1_4	WSSE1_3	WSSE1_2	WSSE1_1	WSSE1_0
i2c-Readback 11 WSS-even byte 2	70	WSSE2_7	WSSE2_6	WSSE2_5	WSSE2_4	WSSE2_3	WSSE2_2	WSSE2_1	WSSE2_0
i2c-Readback 12 WSS-even byte 3	71	WSSE3_7	WSSE3_6	WSSE3_5	WSSE3_4	WSSE3_3	WSSE3_2	WSSE3_1	WSSE3_0
i2c-Readback 13 GS1-header	72	GS1H_7	GS1H_6	GS1H_5	GS1H_4	GS1H_3	GS1H_2	GS1H_1	GS1H_0
i2c-Readback 14 GS1-odd 1	73	GS1O1_7	GS1O1_6	GS1O1_5	GS1O1_4	GS1O1_3	GS1O1_2	GS1O1_1	GS1O1_0

REGISTER FUNCTION	SUB ADDR	D7	D6	D5	D4	D3	D2	D1	D0
i2c-Readback 15 GS1-odd 2	74	GS1O2_7	GS1O2_6	GS1O2_5	GS1O2_4	GS1O2_3	GS1O2_2	GS1O2_1	GS1O2_0
i2c-Readback 16 GS1-even 1	75	GS1E1_7	GS1E1_6	GS1E1_5	GS1E1_4	GS1E1_3	GS1E1_2	GS1E1_1	GS1E1_0
i2c-Readback 17 GS1-even 2	76	GS1E2_7	GS1E2_6	GS1E2_5	GS1E2_4	GS1E2_3	GS1E2_2	GS1E2_1	GS1E2_0
i2c-Readback 18 GS2-header	77	GS2H_ 7	GS2H_ 6	GS2H_ 5	GS2H_ 4	GS2H_ 3	GS2H_ 2	GS2H_ 1	GS2H_ 0
i2c-Readback 19 GS2-odd 1	78	GS2O1_ 7	GS2O1_ 6	GS2O1_ 5	GS2O1_ 4	GS2O1_ 3	GS2O1_ 2	GS2O1_ 1	GS2O1_ 0
i2c-Readback 20 GS2-odd 2	79	GS2O2_ 7	GS2O2_ 6	GS2O2_ 5	GS2O2_ 4	GS2O2_ 3	GS2O2_ 2	GS2O2_ 1	GS2O2_ 0
i2c-Readback 21 GS2-odd 3	7A	GS2O3_ 7	GS2O3_ 6	GS2O3_ 5	GS2O3_ 4	GS2O3_ 3	GS2O3_ 2	GS2O3_ 1	GS2O3_ 0
i2c-Readback 22 GS2-odd 4	7B	GS2O4_ 7	GS2O4_ 6	GS2O4_ 5	GS2O4_ 4	GS2O4_ 3	GS2O4_ 2	GS2O4_ 1	GS2O4_ 0
i2c-Readback 23 GS2-even 1	7C	GS2E1_ 7	GS2E1_ 6	GS2E1_ 5	GS2E1_ 4	GS2E1_ 3	GS2E1_ 2	GS2E1_ 1	GS2E1_ 0
i2c-Readback 24 GS2-even 2	7D	GS2E2_ 7	GS2E2_ 6	GS2E2_ 5	GS2E2_ 4	GS2E2_ 3	GS2E2_ 2	GS2E2_ 1	GS2E2_ 0
i2c-Readback 25 GS2-even 3	7E	GS2E3_ 7	GS2E3_ 6	GS2E3_ 5	GS2E3_ 4	GS2E3_ 3	GS2E3_ 2	GS2E3_ 1	GS2E3_ 0
i2c-Readback 26 GS2-even 4	7F	GS2E4_ 7	GS2E4_ 6	GS2E4_ 5	GS2E4_ 4	GS2E4_3	GS2E4_ 2	GS2E4_ 1	GS2E4_ 0
registers 80 to FF used by X - port, I - port and the scaler									
Task independent Global Settings 1									
Global Control1	80	CMOD	0	TEB	TEA	ICKS3	ICKS2	ICKS1	ICKS0
reserved	81	0	0	0	0	0	FTIME	V_EAV1	V_EAV0
reserved	82	0	0	0	0	0	0	0	0
X-port I/O delay and enable control	83	0	0	XPCK1	XPCK0	0	XRQT	XPE1	XPE0
I - port signal Definitions	84	IDG11	IDG10	IDG01	IDG00	IDV1	IDV0	IDH1	IDH0
I-port signal polarities	85	ISWP1	ISWP0	ILLV	IG1P	IG0P	IRVP	IRHP	IDQP
I - port FIFO flag control and arbitration	86	IMPAK	VITX	IDG12	IDG02	FFL1	FFL0	FEL1	FEL0
I-port I/O delay and enable control	87	IPCK3	IPCK2	IPCK1	IPCK0	0	0	IPE1	IPE0
power save control	88	CH2EN	CH1EN	SWRST	DPROG	SLM3	0	SLM1	SLM0
reserved	89 to 8E	0	0	0	0	0	0	0	0
scaler status information	8F	XTRI	ITRI	FFIL	FFOV	PRDON	ERR_OF	FIDSCI	FIDSCO

REGISTER FUNCTION	SUB ADDR	D7	D6	D5	D4	D3	D2	D1	D0
Task A Definition registers 90 to BF									
Basic Settings and Acquisition Window definition									
Task Handling Control	90	CONLH	OFIDC	FSKP2	FSKP1	FSKP0	RPTSK	STRC1	STRC0
X - port formats and configuration	91	CONLV	HLDFV	SCSRC1	SCSRC0	SCRQE	FSC2	FSC1	FSC0
X - port Input Reference Signal Definition	92	XFDV	XFDH	XDV1	XDV0	XCODE	XDH	XDQ	XCKS
I - port formats and configuration	93	ICODE	INS80	FYSK	FOI1	FOI0	FSI2	FSI1	FSI0
Horizontal input window start (1)	94	XO7	XO6	XO5	XO4	XO3	XO2	XO1	XO0
(continue)	95	0	0	0	0	XO11	XO10	XO9	XO8
Horizontal input window length	96	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0
(continue)	97	0	0	0	0	XS11	XS10	XS9	XS8
Vertical input window start (	98	YO7	YO6	YO5	YO4	YO3	YO2	YO1	YO0
(continue)	99	0	0	0	0	YO11	YO10	YO9	YO8
Vertical input window length	9A	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0
(continue)	9B	FMOD	0	0	0	YS11	YS10	YS9	YS8
Horizontal output window length	9C	XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0
(continue)	9D	0	0	0	0	XD11	XD10	XD9	XD8
Vertical output window length	9E	YD7	YD6	YD5	YD4	YD3	YD2	YD1	YD0
(continue)	9F	0	0	0	0	YD11	YD10	YD9	YD8
FIR Filtering and Prescaling									
Horiz. prescaling	A0	0	0	XPSC5	XPSC4	XPSC3	XPSC2	XPSC1	XPSC0
Accumulation length	A1	0	0	XACL5	XACL4	XACL3	XACL2	XACL1	XACL0
Prescaler DC gain and FIR Prefilter control	A2	PFUV1	PFUV0	PFY1	PFY0	XC2_1	XDCG2	XDCG1	XDCG0
reserved	A3	0	0	0	0	0	0	0	0
Luminance brightness	A4	BRIG7	BRIG6	BRIG5	BRIG4	BRIG3	BRIG2	BRIG1	BRIG0
Luminance contrast	A5	CONT7	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0
Chroma saturation	A6	SATN7	SATN6	SATN5	SATN4	SATN3	SATN2	SATN1	SATN0
reserved	A7	0	0	0	0	0	0	0	0
Horizontal Phase Scaling									
Horiz. Scaling Increment Luma	A8	XSCY7	XSCY6	XSCY5	XSCY4	XSCY3	XSCY2	XSCY1	XSCY0

REGISTER FUNCTION	SUB ADDR	D7	D6	D5	D4	D3	D2	D1	D0
(continue)	A9	0	0	0	XSCY12	XSCY11	XSCY10	XSCY9	XSCY8
Horizontal Phase Offset Luma	AA	XPHY7	XPHY6	XPHY5	XPHY4	XPHY3	XPHY2	XPHY1	XPHY0
reserved	AB								
Horiz. Scaling Increment Chroma	AC	XSCC7	XSCC6	XSCC5	XSCC4	XSCC3	XSCC2	XSCC1	XSCC0
(continue)	AD	0	0	0	XSCC12	XSCC11	XSCC10	XSCC9	XSCC8
Horizontal Phase Offset Chroma	AE	XPHC7	XPHC6	XPHC5	XPHC4	XPHC3	XPHC2	XPHC1	XPHC0
reserved	AF	0	0	0	0	0	0	0	0
Vertical Scaling									
Vertical Scaling Increment Luma	B0	YSCY7	YSCY6	YSCY5	YSCY4	YSCY3	YSCY2	YSCY1	YSCY0
(B0 continued)	B1	YSCY15	YSCY14	YSCY13	YSCY12	YSCY11	YSCY10	YSCY9	YSCY8
Vertical Scaling Increment Chroma	B2	YSCC7	YSCC6	YSCC5	YSCC4	YSCC3	YSCC2	YSCC1	YSCC0
(B2 continued)	B3	YSCC15	YSCC14	YSCC13	YSCC12	YSCC11	YSCC10	YSCC9	YSCC8
Vertical Scaling Mode Control	B4	0	0	0	YMIR	0	0	0	YMODE
reserved	B5 to B7								
Vertical Phase Offset Chroma ‘00’	B8	YPC07	YPC06	YPC05	YPC04	YPC03	YPC02	YPC01	YPC00
Vertical Phase Offset Chroma ‘01’	B9	YPC17	YPC16	YPC15	YPC14	YPC13	YPC12	YPC11	YPC10
Vertical Phase Offset Chroma ‘10’	BA	YPC27	YPC26	YPC25	YPC24	YPC23	YPC22	YPC21	YPC20
Vertical Phase Offset Chroma ‘11’	BB	YPC37	YPC36	YPC35	YPC34	YPC33	YPC32	YPC31	YPC30
Vertical Phase Offset Luma ‘00’	BC	YPY07	YPY06	YPY05	YPY04	YPY03	YPY02	YPY01	YPY00
Vertical Phase Offset Luma ‘01’	BD	YPY17	YPY16	YPY15	YPY14	YPY13	YPY12	YPY11	YPY10
Vertical Phase Offset Luma ‘10’	BE	YPY27	YPY26	YPY25	YPY24	YPY23	YPY22	YPY21	YPY20
Vertical Phase Offset Luma ‘11’	BF	YPY37	YPY36	YPY35	YPY34	YPY33	YPY32	YPY31	YPY30
Task B Definition registers C0 to EF									
Basic Settings and Acquisition Window definition									
Task Handling Control	C0	CONLH	OFIDC	FSKP2	FSKP1	FSKP0	RPTSK	STRC1	STRC0
X - port formats and configuration	C1	CONLV	HLDFV	SCSRC1	SCSRC0	SCRQE	FSC2	FSC1	FSC0

REGISTER FUNCTION	SUB ADDR	D7	D6	D5	D4	D3	D2	D1	D0
Input Reference Signal Definition Control	C2	XFDV	XFDH	XDV1	XDV0	XCODE	XDH	XDQ	XCKS
I - port formats and configuration	C3	ICODE	INS80	FYSK	FOI1	FOI0	FSI2	FSI1	FSI0
Horizontal input window start (1)	C4	XO7	XO6	XO5	XO4	XO3	XO2	XO1	XO0
(continue)	C5	0	0	0	0	XO11	XO10	XO9	XO8
Horizontal input window length	C6	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0
(continue)	C7	0	0	0	0	XS11	XS10	XS9	XS8
Vertical input window start (	C8	YO7	YO6	YO5	YO4	YO3	YO2	YO1	YO0
(continue)	C9	0	0	0	0	YO11	YO10	YO9	YO8
Vertical input window length	CA	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0
(continue)	CB	FMOD	0	0	0	YS11	YS10	YS9	YS8
Horizontal output window length	CC	XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0
(continue)	CD	0	0	0	0	XD11	XD10	XD9	XD8
Vertical output window length	CE	YD7	YD6	YD5	YD4	YD3	YD2	YD1	YD0
(continue)	CF	0	0	0	0	YD11	YD10	YD9	YD8
FIR Filtering and Prescaling									
Horiz. prescaling	D0	0	0	XPSC5	XPSC4	XPSC3	XPSC2	XPSC1	XPSC0
Accumulation length	D1	0	0	XACL5	XACL4	XACL3	XACL2	XACL1	XACL0
Prescaler DC gain and FIR Prefilter control	D2	PFUV1	PFUV0	PFY1	PFY0	XC2_1	XDCG2	XDCG1	XDCG0
reserved	D3	0	0	0	0	0	0	0	0
Luminance brightness	D4	BRIG7	BRIG6	BRIG5	BRIG4	BRIG3	BRIG2	BRIG1	BRIG0
Luminance contrast	D5	CONT7	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0
Chroma saturation	D6	SATN7	SATN6	SATN5	SATN4	SATN3	SATN2	SATN1	SATN0
reserved	D7	0	0	0	0	0	0	0	0
Horizontal Phase Scaling									
Horiz. Scaling Increment Luma	D8	XSCY7	XSCY6	XSCY5	XSCY4	XSCY3	XSCY2	XSCY1	XSCY0
(continue)	D9	0	0	0	XSCY12	XSCY11	XSCY10	XSCY9	XSCY8
Horizontal Phase Offset Luma	DA	XPHY7	XPHY6	XPHY5	XPHY4	XPHY3	XPHY2	XPHY1	XPHY0
reserved	DB	0	0	0	0	0	0	0	0
Horiz. Scaling Increment Chroma	DC	XSCC7	XSCC6	XSCC5	XSCC4	XSCC3	XSCC2	XSCC1	XSCC0

REGISTER FUNCTION	SUB ADDR	D7	D6	D5	D4	D3	D2	D1	D0
(continue)	DD	0	0	0	XSCC12	XSCC11	XSCC10	XSCC9	XSCC8
Horizontal Phase Offset Chroma	DE	XPHC7	XPHC6	XPHC5	XPHC4	XPHC3	XPHC2	XPHC1	XPHC0
reserved	DF	0	0	0	0	0	0	0	0
Vertical Scaling									
Vertical Scaling Increment Luma	E0	YSCY7	YSCY6	YSCY5	YSCY4	YSCY3	YSCY2	YSCY1	YSCY0
(E0 continued)	E1	YSCY15	YSCY14	YSCY13	YSCY12	YSCY11	YSCY10	YSCY9	YSCY8
Vertical Scaling Increment Chroma	E2	YSCC7	YSCC6	YSCC5	YSCC4	YSCC3	YSCC2	YSCC1	YSCC0
(E2 continued)	E3	YSCC15	YSCC14	YSCC13	YSCC12	YSCC11	YSCC10	YSCC9	YSCC8
Vertical Scaling Mode Control	E4	0	0	0	YMIR	0	0	0	YMODE
reserved	E5 to E7	0	0	0	0	0	0	0	0
Vertical Phase Offset Chroma ‘00’	E8	YPC07	YPC06	YPC05	YPC04	YPC03	YPC02	YPC01	YPC00
Vertical Phase Offset Chroma ‘01’	E9	YPC17	YPC16	YPC15	YPC14	YPC13	YPC12	YPC11	YPC10
Vertical Phase Offset Chroma ‘10’	EA	YPC27	YPC26	YPC25	YPC24	YPC23	YPC22	YPC21	YPC20
Vertical Phase Offset Chroma ‘11’	EB	YPC37	YPC36	YPC35	YPC34	YPC33	YPC32	YPC31	YPC30
Vertical Phase Offset Luma ‘00’	EC	YPY07	YPY06	YPY05	YPY04	YPY03	YPY02	YPY01	YPY00
Vertical Phase Offset Luma ‘01’	ED	YPY17	YPY16	YPY15	YPY14	YPY13	YPY12	YPY11	YPY10
Vertical Phase Offset Luma ‘10’	EE	YPY27	YPY26	YPY25	YPY24	YPY23	YPY22	YPY21	YPY20
Vertical Phase Offset Luma ‘11’	EF	YPY37	YPY36	YPY35	YPY34	YPY33	YPY32	YPY31	YPY30
second PLL (PLL2) and Pulsegenerator Programming									
LFCO’s per line	F0	SPLPL7	SPLPL6	SPLPL5	SPLPL4	SPLPL4	SPLPL2	SPLPL1	SPLPL0
P-/I- Param. Select., PLL Mode, PLL H-Src., LFCO’s per line	F1	SPPI3	SPPI2	SPPI1	SPPI0	SPMOD1	SPMOD0	SPHSEL	SPLPL8
Nominal PLL2 DTO Increment	F2	SPNINC7	SPNINC6	SPNINC5	SPNINC4	SPNINC3	SPNINC2	SPNINC1	SPNINC0
	F3	SPNINC15	SPNINC14	SPNINC13	SPNINC12	SPNINC11	SPNINC10	SPNINC9	SPNINC8
PLL2 Status	F4	0	0	0	0	0	0	0	SPLOCK
Pulsgen. line length	F5	PGLEN7	PGLEN6	PGLEN5	PGLEN4	PGLEN3	PGLEN2	PGLEN1	PGLEN0
Pulse A Position, Pulsgen Resync. Pulsgen. H-Src., Pulsgen. line length	F6	PGHAPS3	PGHAPS2	PGHAPS1	PGHAPS0	0	PGRES	PGHSEL	PGLEN8
Pulse A Position	F7	PGHAPS11	PGHAPS10	PGHAPS9	PGHAPS8	PGHAPS7	PGHAPS6	PGHAPS5	PGHAPS4

REGISTER FUNCTION	SUB ADDR	D7	D6	D5	D4	D3	D2	D1	D0
Pulse B Position	F8	PGHBPS3	PGHBPS2	PGHBPS1	PGHBPS0	0	0	0	0
Pulse B Position	F9	PGHBPS11	PGHBPS10	PGHBPS9	PGHBPS8	PGHBPS7	PGHBPS6	PGHBPS5	PGHBPS4
Pulse C Position	FA	PGHCPS3	PGHCPS2	PGHCPS1	PGHCPS0	0	0	0	0
Pulse C Position	FB	PGHCPS11	PGHCPS10	PGHCPS9	PGHCPS8	PGHCPS7	PGHCPS6	PGHCPS5	PGHCPS4
reserved	FC	0	0	0	0	0	0	0	0
reserved	FD	0	0	0	0	0	0	0	0
reserved	FE	0	0	0	0	0	0	0	0
S_PLL max. phase error threshold, PLL2 no. of lines threshold	FF	SPTHRL3	SPTHRL2	SPTHRL1	SPTHRL0	SPTHRM3	SPTHRM2	SPTHRM1	SPTHRM0

16 DETAILED DESCRIPTION OF THE CONTROL REGISTERS

16.1 Chip Version / Ident Register

16.1.1 CHIP VERSION

Table 49 Chip version (SA00), read only register

FUNCTION (1)	LOGIC LEVELS			
	ID07	ID06	ID05	ID04
CHIP VERSION (CV)	CV3	CV2	CV1	CV0

1. This register contains the current version identification number of the chip. Initial version: 0001.

16.1.2 CHIP ID

Table 50 Chip ID (SA00)

FUNCTION (1)	WRITE (HEX)	READ BACK (HEX) ID3 TO ID0
CHIP ID	00	1
	01	F
	02	7
	03	1
	04	1
	05	5
	06	D
	07	0
	08	E
	09	VERSION
	0A .. OF	0

1. This register can be evaluated by alternating write/read cycles

16.2 Programming Register Decoder

16.2.1 Subaddress 01 Analog Input Control 0, Increment Delay

Table 51 Horizontal Increment delay (SA 01)

FUNCTION (1)	IDEL3	IDEL2	IDEL1	IDEL0
no update	1	1	1	1
min. delay	1	1	1	0
recommended position	**1**	**0**	**0**	**0**
max delay	0	0	0	0

1. The programming of the horizontal Increment delay is used to match internal processing delays to the delay of the AD-converter. Use recommended position only.

Table 52 Analog control 0 (SA01)

FUNCTION	LOGIC LEVELS	
Update hysteresis for 9-bit gain, see FIGURE 8 ON PAGE 26	**control bits D5 and D4**	
	GUDL 1	**GUDL 0**
OFF	0	0
± 1 LSB	0	1
± 2 LSB	1	0
± 3 LSB	1	1
White Peak Control off	**control bit D6**	
	WPOFF	
White peak control active (AD-signal is attenuated, if nominal luminance output white level is exceeded)	**0**	
White peak control disabled	1	

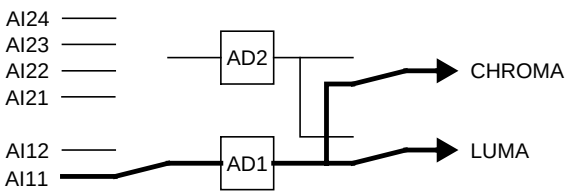
16.2.2 SUBADDRESS 02 ANALOG INPUT CONTROL 1

Table 53 Analog control 1 (SA 02)

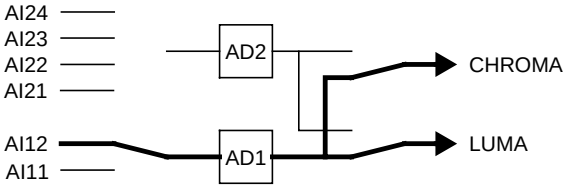
FUNCTION	**LOGIC LEVELS**			
Analog control 1 (Mode select, see Table 54 on page 130) (1)	**control bits D3 to D0**			
	MODE3	**MODE2**	**MODE1**	**MODE0**
Mode 0: CVBS (automatic gain) from AI11 (pin 20)	0	0	0	0
Mode 1: CVBS (automatic gain) from AI12 (pin 18)	0	0	0	1
Mode 2: CVBS (automatic gain) from AI21 (pin 16)	0	0	1	0
Mode 3: CVBS (automatic gain) from AI22 (pin 14)	0	0	1	1
Mode 4: CVBS (automatic gain) from AI23 (pin 12)	0	1	0	0
Mode 5: CVBS (automatic gain) from AI24 (pin 10)	0	1	0	1
Mode 6: Y (automatic gain) from AI11 (pin 20) + C (gain adjusted via GAI2[8:0]) from AI21 (pin 16)	0	1	1	0
Mode 7: Y (automatic gain) from AI12 (pin 18) + C (gain adjusted via GAI2[8:0]) from AI22 (pin 14)	0	1	1	1
Mode 8: Y (automatic gain) from AI11 (pin 20) + C (gain channel 2 adapted to Y gain) from AI21 (pin 16)	1	0	0	0
Mode 9: Y (automatic gain) from AI12 (pin 18) + C (gain channel 2 adapted to Y gain) from AI22 (pin 14)	1	0	0	1
Mode 10 to 15: reserved	1	0	1	
	1	...	...	...
	1	1	1	1
Analog function select FUSE, see Figure 7 on page 25	**control bits D7 and D6**			
	FUSE 1		**FUSE 0**	
Amplifier plus anti-alias filter bypassed	0		0	
	0		1	
Amplifier active	1		0	
Amplifier plus anti-alias filter active	1		1	

1. In order to reduce power consumption of the device use the registers CH1EN and CH2EN (subaddress 88h, bits 7 and 6) to switch of either of the ADCs not used in CVBS modes.

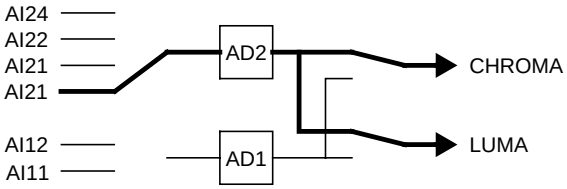
Note: To take full advantage of the YC-modes 6 to 9 the I^2C-bit BYPS (sub address 09h, bit 7) must be set to “1” (full luminance bandwidth)



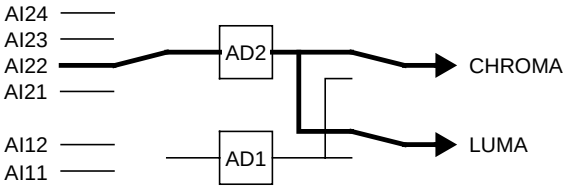
MODE 0 CVBS (automatic gain)



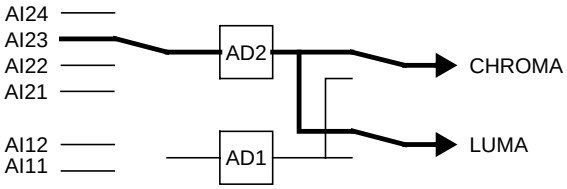
MODE 1 CVBS (automatic gain)



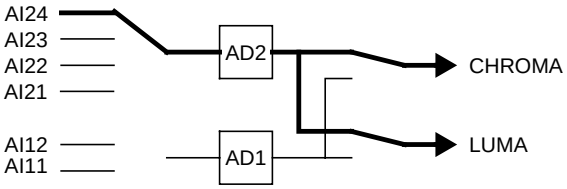
MODE 2 CVBS (automatic gain)



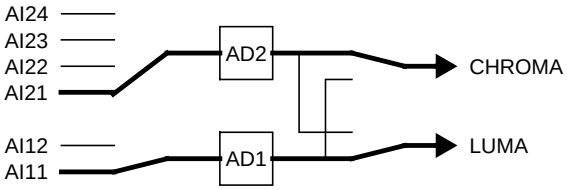
MODE 3 CVBS (automatic gain)



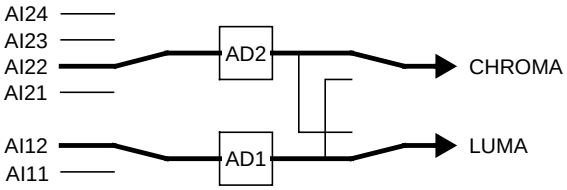
MODE 4 CVBS (automatic gain)



MODE 5 CVBS (automatic gain)



MODE 6 Y+C (gain channel 2 adjusted via GAI2)



MODE 7 Y+C (gain channel 2 adjusted via GAI2)

Table 54 Effects of MODE[3:0] settings

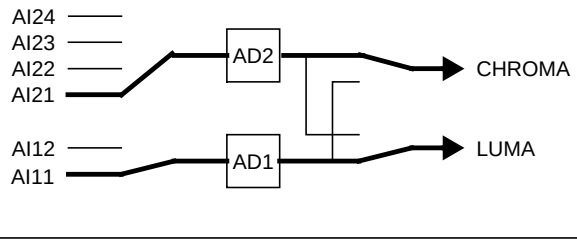
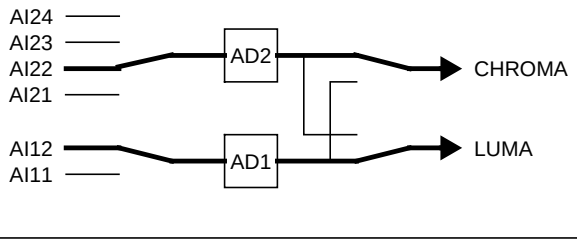
	
MODE 8 Y+C (gain channel 2 adapted to Y-gain)	**MODE 9 Y+C (gain channel 2 adapted to Y-gain)**

Table 54 Effects of MODE[3:0] settings

Note: To take full advantage of the YC-modes 6 to 9 the control-bit BYPS (sub address 09h, bit 7) should be set to “1” (full luminance bandwidth)

16.2.3 SUBADDRESS 03 ANALOG INPUT CONTROL 2

Table 55 Analog control 2 (AICO2) (SA03)

FUNCTION	LOGIC LEVEL	DATA BIT
Static gain control channel 1 (GAI18) (see SA04)		
Sign bit of gain control	see Table 56	D0
Static gain control channel 2 (GAI28) (see SA05)		
Sign bit of gain control	see Table 57	D1
Gain control fix (GAFIX)		
Automatic gain controlled by MODE[3:0]	0	D2
Gain is user programmable via GAI1 + GAI2	1	
Automatic gain control integration (HOLDG)		
AGC active	0	D3
AGC integration hold (frozen)	1	
Color peak off (CPOFF)		
Color peak control active (AD-signal is attenuated, if maximum input level is exceeded, avoids clipping effects on screen)	0	D4
Color peak off	1	
AGC hold during Vertical blanking period (VBSL)		
Short vertical blanking (AGC disabled during equalization- and serration pulses)	0	D5
Long vertical blanking (AGC disabled from start of pre equalization pulses until start of active video (line 22 for 60 Hz, line 24 for 50 Hz)	1	
HL not reference select (HLNRS)		
Normal clamping if decoder is in unlocked state	0	D6
Reference select if decoder is in unlocked state	1	

16.2.4 Subaddress 04 Analog Input Control 3

Table 56 Gain control analog (AIC03); static gain control channel 1 GAI1 (SA 03, SA 04)

DECIMAL VALUE	GAIN (dB)	SIGN BIT 03H D0	CONTROL BITS 04H D7 TO 04H D0							
		GAI18	GAI17	GAI16	GAI15	GAI14	GAI13	GAI12	GAI11	GAI10
0....	–3.0	0	0	0	0	0	0	0	0	0
....144	0	0	1	0	0	1	0	0	0	0
145....	0	0	1	0	0	1	0	0	0	1
....511	+6.0	1	1	1	1	1	1	1	1	1

16.2.5 Subaddress 05 Analog Input Control 4

Table 57 Gain control analog (AIC04); static gain control channel 2 GAI2 (SA 03, SA 05)

DECIMAL VALUE	GAIN (dB)	SIGN BIT 03H D1	CONTROL BITS 05H D7 to 05H D0							
		GAI28	GAI27	GAI26	GAI25	GAI24	GAI23	GAI22	GAI21	GAI20
0....	-3.0	0	0	0	0	0	0	0	0	0
....144	0	0	1	0	0	1	0	0	0	0
145....	0	0	1	0	0	1	0	0	0	1
....511	+6.0	1	1	1	1	1	1	1	1	1

16.2.6 Subaddress 06 Horizontal Sync Start

Table 58 Horizontal sync begin (SA 06)

DELAY TIME (STEP SIZE = 8/LLC)	CONTROL BITS D7 to D0							
	HSB7	HSB6	HSB5	HSB4	HSB3	HSB2	HSB1	HSB0
-128...-109 (50Hz) -128...-108 (60Hz)	forbidden (outside available central counter range)							
-108 (50Hz) ... -107 (60Hz) ...	1 1	0 0	0 0	1 1	0 0	1 1	0 0	0 1
...108 (50Hz) ...107 (60Hz)	0 0	1 1	1 1	0 0	1 1	1 0	0 1	0 1
109...127 (50Hz) 108...127 (60Hz)	forbidden (outside available central counter range)							

16.2.7 SUBADDRESS 07 HORIZONTAL SYNC STOP

Table 59 Horizontal sync stop (SA 07)

DELAY TIME (STEP SIZE = 8/LLC)	CONTROL BITS D7 to D0							
	HSS7	**HSS6**	**HSS5**	**HSS4**	**HSS3**	**HSS2**	**HSS1**	**HSS0**
-128...-109 (50Hz) -128...-108 (60Hz)	forbidden (outside available central counter range)							
-108 (50Hz) ... -107 (60Hz) ...	1 1	0 0	0 0	1 1	0 0	1 1	0 0	0 1
...108 (50Hz) ...107 (60Hz)	0 0	1 1	1 1	0 0	1 1	1 0	0 1	0 1
109...127 (50Hz) 108...127 (60Hz)	forbidden (outside available central counter range)							

16.2.8 SUBADDRESS 08 SYNC CONTROL

Table 60 Sync control (SA 08)

FUNCTION	CONTROL BITS	LOGIC LEVELS	DATA BITS
Vertical noise reduction (VNOI)			
Normal mode (**recommended setting**)	VNOI1	0	D1
	VNOI0	0	D0
Fast mode (applicable for stable sources only, automatic field detection [AUFD] must be disabled)	VNOI1	0	D1
	VNOI0	1	D0
Free running mode	VNOI1	1	D1
	VNOI0	0	D0
Vertical noise reduction bypassed	VNOI1	1	D1
	VNOI0	1	D0
Horizontal PLL (HPLL)			
PLL closed	HPLL	0	D2
PLL open, horizontal frequency fixed	HPLL	1	
Horizontal time constant selection (HTC1, HTC0)			
TV mode (recommended for poor quality TV signals only, do not use for new applications)	HTC1, HTC0	00	D4,D3
VTR mode (recommended if a deflection control circuit is directly connected at the output of the decoder)		01	
automatic TV/VRC detection **(recommended setting)** threshold is programmable via ATVT[1:0], see SA 1B		10	
fast locking mode		11	
Forced ODD/EVEN toggle FOET			
ODD/EVEN-signal toggles only with interlaced source	FOET	0	D5
ODD/EVEN-signal toggles field wise even if source is non-interlaced		1	
Field selection (FSEL, active, if AUFD = 1)			
50 Hz, 625 lines	FSEL	0	D6
60 Hz, 525 lines		1	
Automatic field detection (AUFD)			
Field state directly controlled via FSEL	AUFD	0	D7
Automatic field detection (**recommended setting**)		1	

16.2.9 SUBADDRESS 09 LUMINANCE CONTROL

Table 61 Luminance control (SA 09)

FUNCTION	BITS	LOGIC LEVELS	DATA BITS
Sharpness Control, Luminance filter characteristic (LUFI), see Figure 17 on page 37			
resolution enhancement filter 8.0 dB at 4.1 MHz	LUFI[3:0]	0001	D3 .. D0
resolution enhancement filter 6.8 dB at 4.1 MHz	LUFI[3:0]	0010	
resolution enhancement filter 5.1 dB at 4.1 MHz	LUFI[3:0]	0011	
resolution enhancement filter 4.1 dB at 4.1 MHz	LUFI[3:0]	0100	
resolution enhancement filter 3.0 dB at 4.1 MHz	LUFI[3:0]	0101	
resolution enhancement filter 2.3 dB at 4.1 MHz	LUFI[3:0]	0110	
resolution enhancement filter 1.6 dB at 4.1 MHz	LUFI[3:0]	0111	
PLAIN	LUFI[3:0]	0000	
low pass filter 2 dB at 4.1 MHz	LUFI[3:0]	1000	
low pass filter 3 dB at 4.1 MHz	LUFI[3:0]	1001	
low pass filter 3 dB at 3.3 MHz, 4 dB at 4.1 MHz	LUFI[3:0]	1010	
low pass filter 3 dB at 2.6 MHz, 8 dB at 4.1 MHz	LUFI[3:0]	1011	
low pass filter 3 dB at 2.4 MHz, 14 dB at 4.1 MHz	LUFI[3:0]	1100	
low pass filter 3 dB at 2.2 MHz, notch at 3.4 MHz	LUFI[3:0]	1101	
low pass filter 3 dB at 1.9 MHz, notch at 3.0 MHz	LUFI[3:0]	1110	
low pass filter 3 dB at 1.7 MHz, notch at 2.5 MHz	LUFI[3:0]	1111	
Remodulation bandwidth for luminance (LUBW), see figures 13 **to** 16			
Small remodulation bandwidth (narrow chroma notch => higher luminance bandwidth)	LUBW	0	D4
Large remodulation bandwidth (wider chroma notch => smaller luminance bandwidth)	LUBW	1	
Processing delay in non combfilter mode (LDEL)			
Processing delay is equal to internal pipelining delay **(recommended setting)**	LDEL	0	D5
One (NTSC-standards) or two (PAL-standards) video lines additional processing delay	LDEL	1	
Adaptive luminance comb filter (YCOMB)			
Disabled (= chrominance trap enabled, if BYPS = 0)	YCOMB	0	D6
Active, if BYPS = 0	YCOMB	1	
Chrominance trap / comb filter bypass (BYPS)			
Chrominance trap or luminance comb filter active, default for CVBS mode	BYPS	0	D7
Chrominance trap or luminance comb filter bypassed; default for S-Video mode	BYPS	1	

16.2.10 Subaddress 0A Decoder Brightness

Table 62 Luminance brightness control decoder part DBRI7 to DBRI0 (SA 0A)

OFFSET	CONTROL BITS D7 to D0							
	DBRI7	DBRI6	DBRI5	DBRI4	DBRI3	DBRI2	DBRI1	DBRI0
255 (bright)	1	1	1	1	1	1	1	1
128 (ITU level)	1	0	0	0	0	0	0	0
0 (dark)	0	0	0	0	0	0	0	0

16.2.11 Subaddress 0B Decoder Contrast

Table 63 Luminance contrast control decoder part DCON7 to DCON0 (SA 0B)

GAIN	CONTROL BITS D7 to D0							
	DCON7	DCON6	DCON5	DCON4	DCON3	DCON2	DCON1	DCON0
1.984 (maximum)	0	1	1	1	1	1	1	1
1.063 (ITU level)	0	1	0	0	0	1	0	0
1.0	0	1	0	0	0	0	0	0
0 (luminance off)	0	0	0	0	0	0	0	0
−1.0 (inverse luminance)	1	1	0	0	0	0	0	0
−2.0 (inverse luminance)	1	0	0	0	0	0	0	0

16.2.12 Subaddress 0C Decoder Saturation

Table 64 Chrominance saturation control decoder part DSAT7 to DSAT0 (SA 0C)

GAIN	CONTROL BITS D7 to D0							
	DSAT7	DSAT6	DSAT5	DSAT4	DSAT3	DSAT2	DSAT1	DSAT0
1.984 (maximum)	0	1	1	1	1	1	1	1
1.0 (ITU level)	0	1	0	0	0	0	0	0
0 (colour off)	0	0	0	0	0	0	0	0
−1.0 (inverse chrominance)	1	1	0	0	0	0	0	0
−2.0 (inverse chrominance)	1	0	0	0	0	0	0	0

16.2.13 SUBADDRESS 0D CHROMINANCE HUE

Table 65 Chrominance hue control HUEC7 to HUEC0 (SA 0D)

HUE PHASE (DEG)	CONTROL BITS D7 to D0							
	HUEC7	HUEC6	HUEC5	HUEC4	HUEC3	HUEC2	HUEC1	HUEC0
+178.6....	0	1	1	1	1	1	1	1
....0....	0	0	0	0	0	0	0	0
....–180.0	1	0	0	0	0	0	0	0

16.2.14 SUBADDRESS 0E CHROMINANCE CONTROL 1

Table 66 Chrominance control 1 (SA 0E)

FUNCTION	NAME	LOGIC LEVELS	DATA BITS
Adaptive chrominance comb filter (CCOMB)			
Disabled	CCOMB	0	D0
Active		1	

FUNCTION	NAME	LOGIC LEVELS	DATA BITS

Automatic chrominance standard detection control 0 (AUTO0)
NOTE: Automatic chrominance standard detection control 1 (AUTO1) is located at subaddress 14h, D2

The automatic standard detection circuit does not only search and lock to any broadcast standard, but provides also some default settings dependent on the chosen automatic level. e.g it automatically disables the combfilter or remodulation functionality if Y/C-mode is selected or a B&W source is present. Also the bandwidths of the internal filters are adapted to the detected standard.
However, if these setting are not convenient for the customers application, lower auto levels can be chosen, so that only the standard search and lock is active and all other settings can be programmed independently.

Disabled								AUTO[1:0]	00	SA14:D2, SA0E: D1
Auto mode active (highest level), filter settings and Sharpness control are preset to default values according to the detected standard and mode (**recommended position**) The following registers are automatically set dependent on the following conditions:									01	
Mode	DCVF	LCBW	LUBW	YCOMB	CCOMB	LUFI	CHBW			
PAL comb	0	110	0	p	p	0000	0			
PAL nocomb	0	000	0	p	p	0110	0			
PAL Y/C	0	110	0	0	0	0000	1			
NTSC comb	1	110	0	p	p	0000	0			
NTSC nocomb	0	000	0	p	p	0110	0			
NTSC Y/C	1	110	0	0	0	0000	1			
SECAM	x	000	1	0	x	1011	0			
SECAM Y/C	x	000	x	0	x	0000	0			
B & W	x	xxx	x	0	x	0000	x			
p: programming is required and valid x: setting has no influence Y/C-mode has to be selected via BYPS = 1										
Auto mode active (medium level), filter settings are preset to default values according to the detected standard and mode like AUTO[1:0] = 01, with the following differences: Sharpness control (LUFI[3:0]) is freely programmable CCOMB is freely programmable CHBW is freely programmable									10	
Auto mode active (lowest level), automatic standard recognition, but no filter presets									11	

FUNCTION		NAME	LOGIC LEVELS	DATA BITS
Fast colour time constant (FCTC)				
Nominal time constant		FCTC	0	D2
Fast time constant for special applications (High quality input source, fast chroma lock required, automatic standard detection OFF			1	
Disable chrominance vertical filter and PAL phase error correction (DCVF)				
Chrominance vertical filter, PAL phase error correction on (during active video lines)		DCVF	0	D3
Chrominance vertical filter, PAL phase error correction permanently off			1	
Colour standard selection in non AUTO-mode (CSTD0 to CSTD2); logic levels 110 and 111 are reserved, do not use				
50 Hz / 625 lines	60 Hz / 525 lines		**LOGIC LEVELS**	**DATA BITS**
PAL BGDHI (4.43Mhz)	NTSC M (3.58MHz)	CSTD[2:0]	000	D6 TO D4
NTSC 4.43 (50 Hz)	PAL 4.43 (60 Hz)		001	
Combination-PAL N (3.58MHz)	NTSC 4.43 (60 Hz)		010	
NTSC N (3.58MHz)	PAL M (3.58MHz)		011	
reserved	NTSC-Japan (3.58MHz)		100	
SECAM	reserved		101	
reserved	reserved		110	
reserved	reserved		111	
Colour standard selection (CSTD0 to CSTD2) in AUTO Mode (Auto mode is selected if either AUTO0 or AUTO1 is set, see above)				
50 Hz / 625 lines	60 Hz / 525 lines		**LOGIC LEVELS**	**DATA BITS**
preferred Standard is PAL BGDHI (4.43Mhz)	preferred Standard is NTSC M (3.58MHz)	CSTD[2:0]	000	D6 TO D4
reserved	reserved		001	
reserved	reserved		010	
reserved	reserved		011	
preferred Standard is PAL BGDHI (4.43Mhz)	preferred Standard is NTSC-Japan (3.58MHz, no 7.5 IRE-Offset)		100	
preferred Standard is SECAM	preferred Standard is NTSC M (3.58MHz)		101	
reserved	reserved		110	
reserved	reserved		111	
Note: The meaning of “preferred standard” is, that the internal search machine will always give priority to the selected standard, thus the recognition time for these standards is kept short.				

FUNCTION	NAME	LOGIC LEVELS	DATA BITS
Clear DTO (CDTO)			
Disabled	CDTO	0	D7
Every time CDTO is set, the internal subcarrier DTO phase is reset to 0° and the RTCO output generates a logic 0 at time slot 68. So an identical subcarrier phase can be generated by an external device (e.g. an encoder). The DTO-reset takes also care that the internal remodulation carrier's phase aligned to the internal demodulation phase. A DTO-reset must be initiated after reprogramming the color standard CSTD in non auto mode. However, if automatic standard searching mode is activated via AUTO[1:0] <> 00 an internal DTO-reset is generated after change of standard. That means it is only necessary to generate a DTO reset after connection to an external encoder.		1	

16.2.15 SUBADDRESS 0F CHROMINANCE GAIN CONTROL

Table 67 Chrominance Gain control (SA 0F)

FUNCTION	**LOGIC LEVELS**						
Chroma Gain Value (if ACGC is set to 1)	**control bits**						**D6 to D0**
	CGAIN6	**CGAIN5**	**CGAIN4**	**CGAIN3**	**CGAIN2**	**CGAIN1**	**CGAIN0**
minimum gain (0.5)	0	0	0	0	0	0	0
nominal gain (1.125)	0	1	0	0	1	0	0
maximum gain (7.5)	1	1	1	1	1	1	1
Automatic Chroma Gain Control ACGC	**control bit**						**D7**
ON **(recommended setting)**	0						
programmable gain via CGAIN[6:0],	1						

16.2.16 SUBADDRESS 10 CHROMINANCE/LUMINANCE CONTROL 2

Table 68 Chrominance/Luminance control 2 (SA 10)

FUNCTION	**LOGIC LEVELS**		
COMBINED LUMINANCE/CHROMINANCE BANDWIDTH ADJUSTMENT (SEE FIGURES 11 **TO** 16**)**	**control bits**		**D2 to D0**
	LCBW2	**LCBW1**	**LCBW0**
smallest chrominance bandwidth / largest luminance bandwidth	0	0	0
recommended setting for non combfilter mode (YCOMB=0,CCOMB=0)	**0**	**0**	**1**
recommended setting for active adaptive combfilter (YCOMB=1,CCOMB=1)	**1**	**1**	**0**
largest chrominance bandwidth / smallest luminance bandwidth	1	1	1
Chrominance bandwidth (see figures 11 **and** 12**)**	**control bit**		**D3**
	CHBW		
small	0		
wide	1		
Fine offset adjustment R-Y component	**control bits**		**D5 and D4**
	OFFV1		**OFFv0**
0 LSB	0		0
+1/4 LSB	0		1
+1/2 LSB	1		0
+3/4 LSB	1		1
Fine offset adjustment B-Y component	**control bits**		**D7 and D6**
	OFFU1		**OFFU0**
0 LSB	0		0
+1/4 LSB	0		1
+1/2 LSB	1		0
+3/4 LSB	1		1

16.2.17 SUBADDRESS 11 MODE / DELAY CONTROL

Table 69 Mode / Delay control **SA 11**

FUNCTION	**LOGIC LEVELS**		
Luminance delay compensation (steps in 2/LLC)	**control bits**		**D2 to D0**
	YDEL2	**YDEL1**	**YDEL0**
–4...	1	0	0
...0...**(recommended)**	0	0	0
...3	0	1	1
Output Polarity RTS0	**control bit**		**D4**
	RTP0		
RTS0 non inverted	0		
RTS0 inverted	1		
Fine position of HS-pulse, available on outputs RTSO, RTS1 and XDH, step size of 2/LLC	**control bits**		**D5 and D4**
	HDEL1		**HDEL0**
0	0		0
1	0		1
2	1		0
3	1		1
Output Polarity RTS1	**control bit**		**D6**
	RTP1		
RTS1 non inverted	0		
RTS1 inverted	1		
Colour on	**control bit**		**D7**
	COLO		
Automatic colour killer enabled (**recommended setting**)	0		
Colour forced on	1		

16.2.18 SUBADDRESS 12 RTS0/1 OUTPUT CONTROL

Table 70 RTS0 output control (SA 12)

FUNCTION	LOGIC LEVELS			
RTS0 OUTPUT CONTROL (1)	**D3 to D0**			
	RTSE03	**RTSE02**	**RTSE01**	**RTSE00**
tristate	0	0	0	0
constant LOW	0	0	0	1
CREF (13.5 MHz toggling pulse, see Figure 24 on page 48)	0	0	1	0
CREF2 (6.75 MHz toggling pulse, see Figure 24 on page 48)	0	0	1	1
HL (horizontal lock indicator), selectable via HLSEL (sub addr. 11h, bit 4): HLSEL = 0: standard horizontal lock indicator HLSEL =1: fast horizontal lock indicator (use is not recommended for sources with unstable timebase e. g. VCR's) 0: unlocked 1: locked	0	1	0	0
VL (Vertical & horizontal lock) 0: unlocked 1: locked	0	1	0	1
DL (Vertical & horizontal lock & color detected) 0: unlocked 1: locked	0	1	1	0
reserved	0	1	1	1
HREF horizontal reference signal: indicates 720 pixels valid data on the expansion port. The positive slope marks the beginning of a new active line. HREF is also generated during the vertical blanking interval, see Figure 24 on page 48	1	0	0	0
HS, programmable width in LLC8 steps via HSB[7:0] and HSS[7:0] (sub addr. 06h and 07h), fine position adjustment in LLC2 steps via HDEL[1:0] (sub addr. 11h, bits 5:4), see Figure 24 on page 48)	1	0	0	1
HQ (HREF gated with VGATE)	1	0	1	0
reserved	1	0	1	1
V123 (Vertical sync, see Figure 22 on page 46 and Figure 23 on page 47)	1	1	0	0
VGATE (programmable via VSTA[8:0], VSTO[8:0] and VGPS, sub addresses 15h, 16h, and 17h)	1	1	0	1
reserved	1	1	1	0
FID (position programmable via VSTA[8:0], sub addresses 15h and 17h, see Figure 22 on page 46 and Figure 23 on page 47)	1	1	1	1

Note

1. The polarity of any signal on RTS0 can be inverted via RTP0 (sub address 11 bit 3).

Table 71 RTS1 output control (SA 12)

FUNCTION	LOGIC LEVELS			
RTS1 OUTPUT CONTROL (1)	**D7 to D4**			
	RTSE13	**RTSE12**	**RTSE11**	**RTSE10**
tristate	0	0	0	0
constant LOW	0	0	0	1
CREF (13.5 MHz toggling pulse, see Figure 24 on page 48)	0	0	1	0
CREF2 (6.75 MHz toggling pulse, see Figure 24 on page 48)	0	0	1	1
HL (horizontal lock indicator), selectable via HLSEL (sub addr. 11h, bit 4): HLSEL = 0: standard horizontal lock indicator HLSEL =1: fast horizontal lock indicator (use is not recommended for sources with unstable timebase e. g. VCR's) 0: unlocked 1: locked	0	1	0	0
VL (Vertical & horizontal lock) 0: unlocked 1: locked	0	1	0	1
DL (Vertical & horizontal lock & color detected) 0: unlocked 1: locked	0	1	1	0
reserved	0	1	1	1
HREF horizontal reference signal: indicates 720 pixels valid data on the expansion port. The positive slope marks the beginning of a new active line. HREF is also generated during the vertical blanking interval, see Figure 24 on page 48	1	0	0	0
HS, programmable width in LLC8 steps via HSB[7:0] and HSS[7:0] (sub addr. 06h and 07h), fine position adjustment in LLC2 steps via HDEL[1:0] (sub addr. 11h, bits 5:4), see Figure 24 on page 48)	1	0	0	1
HQ (HREF gated with VGATE)	1	0	1	0
reserved	1	0	1	1
V123 (Vertical sync, see Figure 22 on page 46 and Figure 23 on page 47)	1	1	0	0
VGATE (programmable via VSTA[8:0], VSTO[8:0] and VGPS, sub addresses 15h, 16h, and 17h)	1	1	0	1
reserved	1	1	1	0
FID (position programmable via VSTA[8:0], sub addresses 15h and 17h, see Figure 22 on page 46 and Figure 23 on page 47)	1	1	1	1

Note

1. The polarity of any signal on RTS1 can be inverted via RTP1 (sub address 11 bit 6).

16.2.19 SUBADDRESS 13 AND 1B RT / X-PORT OUTPUT CONTROL

Table 72 RT / X-port output control (SA 13, SA 1B)

FUNCTION					LOGIC LEVELS			
XPD[7:0] - port output format selection, see also chapter 9.4	**X-PORT OUTPUT**				**1BH D4**	**13H D2 TO D0**		
	XPD[7:0]	**XRH**	**XRV**	**XDQ**	**OFTS3**	**OFTS2**	**OFTS1**	**OFTS0**
ITU656 - 8 Bit standard mode	Y, C_B, C_R [7:0]	Horizontal Sync. Signal controlled by XRHS	Vertical Sync. Signal controlled by XRVS[1:0]	HREF && VGATE	0	0	0	0
modified ITU656-8-bit mode: standard Vflag is replaced by VGATE, programmable via VSTA,VSTO					0	0	0	1
8-bit multiplexed Y,Cb,Cr-mode, ITU- Codes and 10/80 blanking values are disabled					0	0	1	0
reserved	reserved				0	0	1	1
reserved					0	1	0	0
reserved					0	1	0	1
ADC1-bypass-mode (msbs only)	AD1[8:1]				0	1	1	0
ADC2-bypass-mode (msbs only)	AD2[8:1]				0	1	1	1
ITU656-10-bit standard mode	Y, C_B, C_R [9:2]	Y, C_B, C_R [1]	Y, C_B, C_R [0]		1	0	0	0
modified ITU656-10-bit mode: standard Vflag is replaced by VGATE, programmable via VSTA,VSTO					1	0	0	1
10-bit multiplexed Y,Cb,Cr-mode, ITU- Codes and 10/80 blanking values are disabled					1	0	1	0
reserved	reserved	reserved	reserved		1	0	1	1
reserved					1	1	0	0
reserved					1	1	0	1
ADC1-bypass-mode (9 bits)	AD1[8:1]	AD1[0]			1	1	1	0
ADC2-bypass-mode (9 bits)	AD2[8:1]	AD2[0]			1	1	1	1

Table 73 RT / X-port output control **SA 13**

FUNCTION	**LOGIC LEVELS**	
Horizontal lock indicator selection HLSEL	**control bits**	**D3**
	HLSEL	
copy of inverted HLOCK status bit (default)	0	
fast horizontal lock indicator (for special applications only)	1	
X - port XRV output selection XRVS	**control bits**	**D5 and D4**
	XRVS1	**XRVS0**
V123 (see **FIGURE 22 ON PAGE 46** and **FIGURE 23 ON PAGE 47**)	0	0
ITU656 related field ID (see **FIGURE 22 ON PAGE 46** and **FIGURE 23 ON PAGE 47**)	0	1
inverted V123	1	0
inverted ITU656 related field ID	1	1
X - port XRH output selection XRHS	**control bits**	**D6**
HREF, see Figure 24 on page 48	0	
HS (programmable: width in LLC8-steps via HSB[7:0] and HSS[7:0] fine position in LLC2 steps via HDEL[1:0]), see Figure 24 on page 48	1	
RTCO output enable RTCE	**control bits**	**D7**
tristate	0	
enabled	1	

16.2.20 SUBADDRESS 14 ANALOG / ADC / AUTO/ COMPATIBILITY CONTROL

Table 74 analog / ADC / compatibility control **SA 14**

FUNCTION	**LOGIC LEVELS**	
ADC sample clock phase delay	**control bits**	**D1 AND D0**
	APCK1	**APCK0**
application dependent	0	0
	0	1
	1	0
	1	1

FUNCTION	LOGIC LEVELS			
Automatic chrominance standard detection control 1 (AUTO1), see explanation at subaddress 0Eh	**control bit**		**D2**	
XTOUT output enable (XTOUTE)	**control bit**		**D3**	
pin 4 (XTOUT) tristated	0			
pin 4 (XTOUT) enabled	1			
Analog test select (AOSL)	**control bits**		**01H D7 AND 14H D5, D4**	
		AOSL2 **01H D7**	**AOSL1** **14H D5**	**AOSL0** **14H D4**
AOUT connected to ground (recommended)		0	0	0
AOUT connected to input CH1 video		0	0	1
AOUT connected to input CH2 video		0	1	0
AOUT connected to input BPFOUT (LLC)		0	1	1
AOUT connected to input BPFOUT2		1	0	0
reserved (gnd)		1	0	1
reserved (gnd)		1	1	0
reserved (gnd)		1	1	1
Update time interval for AGC-value (UPTCV)	**control bit**		**D6**	
Horizontal update (once per line)		0		
Vertical update (once per field)		1		
Compatibility switch for SAA7199 (CM99)	**control bit**		**D7**	
off (default)		0		
on (to be set only if SAA7199 is used for re-encoding in conjunction with RTCO active		1		

16.2.21 SUBADDRESS 15, 17VGATE START

Table 75 Start of VGATE-pulse (01-transition) and polarity change of FID-pulse, VGPS = 0, see figures 22 and 23 (SA 15, SA 17)

FIELD		Frame line counting	Decimal value	17H D0	CONTROL BITS 15H D7 to 15H D0							
				VSTA8	VSTA7	VSTA6	VSTA5	VSTA4	VSTA3	VSTA2	VSTA1	VSTA0
50 HZ	1ST	1	312	1	0	0	1	1	1	0	0	0
	2ND	314										
	1ST	2	0....	0	0	0	0	0	0	0	0	0
	2ND	315										
	1ST	312	310	1	0	0	1	1	0	1	1	1
	2ND	625										
60 HZ	1ST	4	262	1	0	0	0	0	0	1	1	0
	2ND	267										
	1ST	5	0....	0	0	0	0	0	0	0	0	0
	2ND	268										
	1ST	265	260	1	0	0	0	0	0	1	0	1
	2ND	3										

16.2.22 SUBADDRESS 16, 17 VGATE STOP

Table 76 Stop of VGATE-pulse (10-transition), VGPS = 0, see figures 22 and 23 (SA 16, SA 17)

FIELD		Frame line counting	Decimal value	17H D0	CONTROL BITS 16H D7 to 16H D0							
				VSTO8	VSTO7	VSTO6	VSTO5	VSTO4	VSTO3	VSTO2	VSTO1	VSTO0
50 HZ	1ST	1	312	1	0	0	1	1	1	0	0	0
	2ND	314										
	1ST	2	0....	0	0	0	0	0	0	0	0	0
	2ND	315										
	1ST	312	310	1	0	0	1	1	0	1	1	1
	2ND	625										
60 HZ	1ST	4	262	1	0	0	0	0	0	1	1	0
	2ND	267										
	1ST	5	0....	0	0	0	0	0	0	0	0	0
	2ND	268										
	1ST	265	260	1	0	0	0	0	0	1	0	1
	2ND	3										

16.2.23 SUBADDRESS 17 MISC./VGATE-MSB'S

Table 77 Misc./VGATE-MSB's (SA 17)

FUNCTION	LOGIC LEVELS	CONTROL BITS
VSTA8, see SA 15		
MSB VGATE start	see Table 76	D0
VSTO8, see SA 16		
MSB VGATE stop	see Table 76	D1
Alternative VGATE position (VGPS)		
VGATE position according to tables and 76	0	**D2**
VGATE occurs one line earlier during field 2	1	
Standard detection search loop latency (LATY)		
reserved	000	**D5 TO D3**
one field	001	
...	...	
three fields (**recommended value**)	011	
...	...	
seven fields	111	
LLC (pin 48) output enable (LLC2E)		
enabled	0	**D6**
tristate	1	
LLC (pin 46) output enable (LLCE)		
enabled	0	**D7**
tristate	1	

16.2.24 Subaddress 18 Raw data Gain Control

Table 78 Raw data gain control RAWG7 to RAWG0 (SA 18)

GAIN	CONTROL BITS D7 to D0							
	RAWG7	RAWG6	RAWG5	RAWG4	RAWG3	RAWG2	RAWG1	RAWG0
255 (double ampl.)	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
128 (nominal level)	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**
0 (off)	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

16.2.25 Subaddress 19 Raw data Offset Control

Table 79 Raw data offset control RAWO7 to RAWO0 (SA 19)

OFFSET	CONTROL BITS D7 to D0							
	RAWO7	RAWO6	RAWO5	RAWO4	RAWO3	RAWO2	RAWO1	RAWO0
- 128 LSB	0	0	0	0	0	0	0	0
0 LSB	1	0	0	0	0	0	0	0
+128 LSB	1	1	1	1	1	1	1	1

16.2.26 Subaddress 1A Color Killer Level Control

Table 80 SECAM Color Killer Level Control (SA 1A)

SECAM COLOR KILLER LEVEL	CONTROL BITS D3 TO D0			
	STHR3	STHR2	STHR1	STHR0
minimum level: color is switched on at low subcarrier levels	0	0	0	0
recommended value	**0**	**1**	**1**	**1**
maximum	1	1	1	1

Table 81 PAL/NTSC Color Killer Level Control (SA 1A)

PAL/NTSC COLOR KILLER LEVEL	CONTROL BITS D7 TO D4			
	QTHR3	QTHR2	QTHR1	QTHR0
minimum: color is switched on at low subcarrier levels	0	0	0	0
recommended value	**0**	**1**	**1**	**1**
maximum	1	1	1	1

16.2.27 Subaddress 1B Misc. Chroma Control

Table 82 Automatic VCR/TV-Detection Threshold (SA 1B)

AUTOMATIC VCR/TV-DETECTION THRESHOLD	D7,D6
	ATVT[1:0]
very sensitive to phase errors => early switching to fast horizontal time constant	00
recommended value	**01**
less sensitive to phase errors	10
insensitive to phase errors => late switching to fast horizontal time constant	11

Table 83 Automatic Color Limiter (SA 1B)

AUTOMATIC COLOR LIMITER	D1
	ACOL
disabled	0
active: reduces oversaturated color in case of nonstandard burst/picture_content relation (recommended)	**1**

Table 84 Fast Sequence Correction (SA 1B)

FAST PAL/SECAM SEQUENCE CORRECTION	D0
	FSQC
sequence correction enabled once per field (recommended)	**0**
to be used, if immediate (linewise) sequence correction is required	1

16.2.28 SUBADDRESS 1C ENHANCED COMBFILTER CONTROL 1

Table 85 Horizontal Difference Gain (SA 1C)

HORIZONTAL DIFFERENCE GAIN	D7,D6
	HODG[1:0]
lowest luminance bandwidth at horizontal transients	00
higher luminance bandwidth at horizontal transients	01
recommended value	**10**
highest luminance bandwidth at horizontal transients	11

Table 86 Vertical Difference Gain (SA 1C)

VERTICAL DIFFERENCE GAIN	D5,D4
	VEDG[1:0]
highest luminance bandwidth at vertical transients	00
lower luminance bandwidth at vertical transients	01
recommended value	**10**
lowest luminance bandwidth at vertical transients	11

Table 87 Median Filter Gain (SA 1C)

MEDIAN FILTER GAIN	D3,D2
	MEDG[1:0]
highest luminance bandwidth at high color saturation	00
lower luminance bandwidth at high color saturation	01
recommended value	**10**
lowest luminance bandwidth at high color saturation	11

Table 88 Combfilter Threshold (SA 1C)

COMB THRESHOLD	D1,D0
	CMBT[1:0]
lowest comb strength for signals containing small chrominance content	00
recommended value	**01**
higher comb strength for signals containing small chrominance content	10
highest comb strength for signals containing small chrominance content	11

16.2.29 Subaddress 1D Enhanced Combfilter Control 2

Table 89 Vertical Difference Threshold (SA 1C)

VERTICAL DIFFERENCE THRESHOLD	D1,D0
	VEDT[1:0]
highest comb strength for signals containing large vertical chrominance differences	00
recommended value	**01**
lower comb strength for signals containing large vertical chrominance differences	10
lowest comb strength for signals containing large vertical chrominance differences	11

16.2.30 SUBADDRESSES 1E, 1F STATUS BYTES VIDEO DECODER (READ-ONLY REGISTER)

Table 90 Status byte 1 video decoder (SA 1E)

I²C-BUS CONTROL BITS	FUNCTION	DATA BIT
DCSTD[1:0]	detected color standard: 00: No color [BW] 01: NTSC 10: PAL 11: SECAM	D1, D0
WIPA	white peak loop is activated; active HIGH	D2
GLIMB	gain value for active luminance channel is limited [min (bottom)]; active HIGH	D3
GLIMT	gain value for active luminance channel is limited [max (top)]; active HIGH	D4
SLTCA	slow time constant active in WIPA-mode; active HIGH	D5
HLCK	status bit for locked horizontal frequency; LOW = locked, HIGH = unlocked	D6
NFLD	status bit for field length; LOW = nonstandard field length, HIGH = standard field length	D7

Table 91 Status byte 2 video decoder (SA 1F)

I²C-BUS CONTROL BITS	FUNCTION	DATA BIT
RDCAP	Ready for Capture (all internal loops locked); active HIGH	D0
COPRO	Copy protected source detected according to Macrovision version up to 7.01	D1
COLSTR	Macrovision encoded Colorstripe burst detected (any type)	D2
TYPE3	Macrovision encoded Colorstripe burst type 3 (4 line version) detected	D3
STTB	status bit for timebase of input signal; LOW = nonstable timebase (e.g. VCR) HIGH = stable timebase (e.g. broadcast/DVD-source)	D4
FIDT	identification bit for detected field frequency; LOW = 50 Hz, HIGH = 60 Hz	D5
HLVLN	status bit for horizontal and vertical loop: LOW = both loops locked, HIGH = unlocked	D6
INTL	status bit for interlace detection, LOW = non interlaced, HIGH = interlaced	D7

16.3 Programming Register Audio Clock Generation

See equations in chapter 8.6 and examples on Table 28 on page 83, Table 30 on page 85 and Table 31 on page 87

16.3.1 Subaddresses 30 to 32 AMCLK Cycles per Field

Table 92 Audio Master Clock: cycles per field (SA 30, SA 31, SA 32)

AUDIO MASTER CLOCK: CYCLES PER FIELD	CONTROL BITS D7 to D0							
SA 30	ACPF7	ACPF6	ACPF5	ACPF4	ACPF3	ACPF2	ACPF1	ACPF0
SA 31	ACPF15	ACPF14	ACPF13	ACPF12	ACPF11	ACPF10	ACPF9	ACPF8
SA 32							ACPF17	ACPF16

16.3.2 Subaddresses 34 to 36 AMCLK Nominal Increment

Table 93 Audio Master Clock: nominal increment (SA 34, SA 53, SA 36)

AUDIO MASTER CLOCK: NOMINAL INCREMENT	CONTROL BITS D7 to D0							
SA 34	ACNI7	ACNI6	ACNI5	ACNI4	ACNI3	ACNI2	ACNI1	ACNI0
SA 35	ACNI15	ACNI14	ACNI13	ACNI12	ACNI11	ACNI10	ACNI9	ACNI8
SA 36			ACNI21	ACNI20	ACNI19	ACNI18	ACNI17	ACNI16

16.3.3 Subaddress 38 Ratio AMXCLK to ASCLK

Table 94 Clock ratio Audio Master Clock to Serial Clock (bit clock) ASCLK (SA 38)

CLOCK RATIO AUDIO MASTER CLOCK TO SERIAL CLOCK	CONTROL BITS D5 TO D0					
SA 38	SDIV5	SDIV4	SDIV3	SDIV2	SDIV1	SDIV0
	Refer to chapter 8.7					

16.3.4 Subaddress 39 Ratio ASCLK to ALRCLK

Table 95 Clock ratio Serial Clock ASCLK to ALRCLK (channel select clock) (SA 39)

CLOCK RATIO SERIAL CLOCK ASCLK TO ALRCLK	CONTROL BITS D5 TO D0					
SA 39	LRDIV5	LRDIV4	LRDIV3	LRDIV2	LRDIV1	LRDIV0
	Refer to chapter 8.7					

16.3.5 Subaddress 3A Audio Clock Control

Table 96 Audio clock control (SA 3A)

FUNCTION	NAME	LEVELS	BITS
ASCLK phase			
ASCLK edges triggered by falling edges of AMCLK	SCPH	0	D0
ASCLK edges triggered by rising edges of AMCLK		1	
ALRCLK phase			
ALRCLK edges triggered by falling edges of ASCLK	LRPH	0	D1
ALRCLK edges triggered by rising edges of ASCLK		1	
Audio Master clock Vertical Reference			
Vertical reference pulse is taken from internal decoder	AMVR	0	D2
Vertical reference is taken form XRV-input (expansion port)		1	
Audio PLL mode			
PLL active, AMCLK is frame-locked to the incoming video signal (Vertical reference pulse)	APLL	0	D3
PLL open, AMCLK is free running		1	
Audio PLL mode (only active if UCGC = 1)			
internal Audio master clock is divided by 4	CGCDIV	0	D6
internal Audio master clock is divided by 3		1	
Audio clock: CGC Generation mode			
Second CGC (CGC2) bypassed (e.g. in case CGC2 is used for scaler backend clock generation): Audio clock as generated by the Audio PLL is output on pin AMCLK	UCGC	0	D7
Second CGC (CGC2) in use for Audio clock generation: Enhances the jitter, performance of the generated audio master clock on pin AMCLK		1	

16.4 Programming Register VBI data slicer

16.4.1 Subaddress 40 Basic Slicer Settings

Table 97 Amplitude searching (SA 40)

Slicer Set (40h)	D4
Amplitude searching	control bit
	HUNT_N
Amplitude searching active [default]	0
Amplitude searching stopped	1

Table 98 Framing Code Error (SA 40)

Slicer Set (40h)	D5
Framing Code Error	control bit
	FCE
One framing code error allowed	0
No framing code errors allowed	1

Table 99 Hamming Check (SA 40)

Slicer Set (40h)	D6
Hamming Check	control bit
	HAM_N
Hamming check for 2 bytes after framing code, depending on data type [default]	0
No Hamming check	1

Table 100WSS-Check (SA 40)

Slicer Set (40h)	D7
WSS525 CRC code check (1)	**control bit**
	CHKWSS
All WSS525 packets are considered valid (provided that the start bit is detected), regardless of CRCERR	0
Only WSS525 packets with CRCERR = 0 are considered valid	1

1. The VBI slicer will only track the amplitude of data that it considers to be valid; this tracking is important for optimal acquisition performance. If no valid data is found for several successive frames, then the slicer will enter amplitude searching (Hunting) mode until valid data is found again. CHKWSS alters the definition of "valid" data.
   Side effect if '1': if WSS525 data is present but containing incorrect CRC bits, the slicer will enter Hunting mode, and acquisition may intermittently fail even with an undistorted signal.
   Side effect if '0': if the slicer is set to acquire WSS525 from lines containing noise, or another data type, then false detections of "valid" data are more likely to occur which will upset the amplitude tracking mechanism. (Note that Hunting can still occur if the WSS525 start bits are never detected.)

16.4.2 Subaddress 41 to 57 Line Control Register

Table 101LCR Register 2...24 (SA41 .... SA57)

LCR Register 2...24 (41h ....57h) (1)		D7..D4	D3..D0
60HZ / 525 LINES STANDARDS	**50HZ / 625 LINES STANDARDS**	**DT[3:0] field 1**	**DT[3:0] field 2**
do not acquire (active video)	do not acquire (active video)	0000	0000
US Teletext (WST525)	Euro Teletext (WST625)	0001	0001
NABTS	Euro Teletext with progammable Framing Code	0010	0010
Moji	reserved	0011	0011
US Closed Caption (CC525)	Euro Closed Caption (CC625)	0100	0100
CGMS (WSS525)	Euro Wide Screen Signalling (WSS625)	0101	0101
VITC525	VITC625	0110	0110
Gemstar2x	VPS	0111	0111
Gemstar1x	reserved	1000	1000
reserved	reserved	1001	1001
Open1 (5 MHz)	Open1 (5 MHz)	1010	1010
Open2 (5,7272 MHz)	Open2 (5,7272 MHz)	1011	1011
reserved	reserved	1100	1100
do not acquire (RAW)	do not acquire (RAW)	1101	1101
do not acquire (Test)	do not acquire (Test)	1110	1110
do not acquire (active video)	do not acquire (active video)	1111	1111

1. Line Control Register LCR0 to LCR23 are assigned to one VBI dataline of a VBI region each. Line Control Register LCR24 is assigned to all other VBI data lines / active video lines.

16.4.3 Subaddress 58 Programmable Framing Code

Table 102 Framing Code for programmable Data Types (SA58)

Slicer Set (580h)	D7...0
Framing Code for programmable Data Types according to the DT table	**control bits**
	FC7...0
[default]	40h

16.4.4 SUBADDRESS 59 HORIZONTAL OFFSET

Table 103 Horizontal Offset (SA 59, SA 5B)

Slicer Set (59h, 5Bh)	5Bh,D2...0	59h,D7...0
Horizontal Offset	**control bits**	**control bits**
	HOFF10...8	**HOFF7...0**
recommended value	3h	47h

16.4.5 SUBADDRESS 5A VERTICAL OFFSET

Table 104 Vertical Offset (SA 5A, SA 5B)

Slicer Set (5Ah, 5Bh)	5Bh,D4	5Ah,D7...0
Vertical Offset	**control bit**	**control bits**
	VOFF[8]	**VOFF[7:0]**
Minimum value 0	0	0
Maximum value 312	1	38
value for 50 Hz/625 lines input	0	03
value for 60 Hz/525 lines input and ITU656 line counting (1)	0	06
value for 60 Hz/525 lines input and consistent field ID (1)	0	03

1. for 60 Hz offsets; please refer to sect.8.2 and sect.8.4

16.4.6 SUBADDRESS 5B FIELD OFFSET, MSB'S H/V-OFFSETS

Table 105 Field Offset, MSB's for Vertical and Horizontal Offsets (SA 5B)

Slicer Set (5Bh)	D5
Vertical Trigger Edge	**control bit**
	VEP
VBI slicer triggers on the negative edge of the internal V123 V-sync (Default)	0
VBI slicer triggers on the positive edge of the internal V123 V-sync	1

Table 106 Field Offset, MSB's for Vertical and Horizontal Offsets (SA 5B)

Slicer Set (5Bh)	**D7**
Field Offset	**control bit**
	FOFF
no modification of internal field indicator, (default for 50 Hz/625 lines input sources)	0
Invert field indicator (default for 60 Hz/525 lines input sources)	1

16.4.7 SUBADDRESS 5D: SLDOM CODES

Table 107 Sliced data output modes (SA 5D)

Slicer Set (5Dh)	D4	D3	D2	D1	D0
Sliced Data Output Mode	**SLDOM4**	**SLDOM3**	**SLDOM2**	**SLDOM1**	**SLDOM0**
Output from VBI slicer through I-port is disabled (VITX[1] function of SAA7114)	X	0	0	0	0
no recoding	X	X	X	X	0
recode data values 00h and FFh to even parity values 03h and FCh	X	X	X	X	1
ANC header with constant DID byte, programmable via SDID (addr. 5Eh)	X	0	0	1	X
ANC header (VIP-DID) for DT 1 - 8, A and B plus timing codes (empty packages) for lines 1 and after line 23	X	0	1	0	X
ANC header (VIP-DID) for DT 1 - 8, A and B no timing codes	X	0	1	1	X
SAV-EAV framed output lines, with D2 as T-Bit of SAV/EAV byte	X	1	T (1)	X	X
SAV-EAV framing for the defined VBI standards of DT 1 - 8, A and B and DT 9	X	1	T (1)	0	X
SAV-EAV framing for the defined VBI standards except for those Data Types which are accessible via I2C readback registers. Suppressed standards are: CC525/625, WSS525/625 (CGMS), Gemstar1x/Gemstar2x	X	1	T (1)	1	X
if regions overlap, output of sliced VBI and scaled video for a certain line	0	1	T (1)	X	X
if regions overlap, output of video is suppressed for SAV-EAV framed sliced VBI lines	1	1	T (1)	X	X

1. corresponds to the T-Bit of SAV/EAV codes

16.4.8 SUBADDRESS 5E SDID CODES

Table 108 SDID codes (SA 5E)

Slicer Set (5Eh)	D5	D4	D3	D2	D1	D0
SDID codes	**SDID5**	**SDID4**	**SDID3**	**SDID2**	**SDID1**	**SDID0**
SDID5..0 = 0h [default]	0	0	0	0	0	0

16.4.9 SUBADDRESS 5E (READ-ONLY REGISTER)

Table 109 Slicer Status Bit (SA 5E), read only

Slicer Status Bit (5Eh) read only	D7
Framing Code Valid	**control bit**
	FC8V
No Framing code (0 error) in the last frame detected	0
Framing code with 0 error detected	1

Table 110 Slicer Status Bit (SA 5E), read only

Slicer Status Bit (5Eh) read only	D6
Framing Code Valid	**control bit**
	FC7V
No Framing code (1 error) in the last frame detected	0
Framing code with 1 error detected	1

16.4.10 Subaddress 66 to 7F I²C Readback of decoded VBI Data (read-only register)

16.4.10.1 Subaddress 66 to 6A I²C Readback of Closed Caption Data (CC525 and CC625) (read-only register)

Table 111 Closed Caption (CC525 and CC625) I²C readback (66h, ... , 6Ah) read only

Register Content (1)	**REG. ADDR.**	**D7**	**D6**	**D5**	**D4**	**D3 .. D0**
Status Header	66 h	CCH_7	CCH_6	CCH_5	CCH_4	CCH_3 .. CCH_0
		odd field		even field		free running field counter
		being updated	data erroneous	being updated	data erroneous	
CC payload data byte 1 of odd field	67 h	CCO1_7 .. CCO1_0				
CC payload data byte 2 of odd field	68 h	CCO2_7 .. CCO2_0				
CC payload data byte 1 of even field	69 h	CCE1_7 .. CCE1_0				
CC payload data byte 2 of even field	6A h	CCE2_7 .. CCE2_0				

1. All decoded VBI data is written into the registers starting with the LSB of each register first until all data is stored

Table 112 Closed Caption (CC525 and CC625) data order in WSS I²C readback registers

Register Name	CCO1 / CCE1								CCO2 / CCE2							
Register Addr.	6C h / 6F h								6D h / 70 h							
Register Bit	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
CC525 Bit No. (1)	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8
CC625 Bit No. (1)	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8

1. CC data bits in order they appear in the VBI data line (beginning with bit 0)

16.4.10.2 Subaddress 6B to 71 I²C Readback of Closed Caption Data (WSS525 and WSS625) (read-only register)

Table 113 Widescreen Signalling (WSS525 and WSS625) I²C readback (6Bh, ... , 71h) read only

REGISTER CONTENT (1)	**REG. ADDR.**	**D7**	**D6**	**D5**	**D4**	**D3 .. D0**
Status Header	6B h	WSSH_7	WSSH_6	WSSH_5	WSSH_4	WSSH_3 .. WSSH_0
		odd field		even field		free running field counter
		being updated	data erroneous	being updated	data erroneous	
WSS payload data byte 1 of odd field	6C h	WSSO1_7 .. WSSO1_0				
WSS payload data byte 2 of odd field	6D h	WSSO2_7 .. WSSO2_0				
WSS payload data byte 2 of odd field	6E h	WSSO3_7 .. WSSO3_0				
WSS payload data byte 1 of even field	6F h	WSSE1_7 .. WSSE1_0				
WSS payload data byte 2 of even field	70 h	WSSE2_7 .. WSSE2_0				
WSS payload data byte 3 of even field	71 h	WSSE3_7 .. WSSE3_0				

1. All decoded VBI data is written into the registers starting with the LSB of each register first until all data is stored

Table 114 Widescreen Signalling (WSS525 and WSS625) data order in WSS I²C readback registers

Register Name	WSSO1 / WSSE1								WSSO2 / WSSE2								WSSO3 / WSSE3							
Register Addr.	6C h / 6F h								6D h / 70 h								6E h / 71 h							
Register Bit	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
WSS525 Bit No. (1)	8	7	6	5	4	3	2	1	16	15	14	13	12	11	10	9	C (2)	-	-	-	20	19	18	17
WSS625 Bit No. (3)	7	6	5	4	3	2	1	0	-	-	13	12	11	10	9	8	-	-	-	-	-	-	-	-

1. WSS525 data bits in order they appear in the VBI data line (beginning with bit 1)
2. This bit carries the result of the CRC-check. It is '0' if the received CRC code is identical to the calculated CRC Code, else it is set to '1'
3. WSS625 data bits in order they appear in the VBI data line (beginning with bit 0)

16.4.10.3 Subaddress 72 to 76 I²C Readback of Gemstar1x Data (read-only register)

Table 115 Gemstar1x I²C readback (72h, ... , 76h) read only

Register Content (1)	**REG. ADDR.**	**D7**	**D6**	**D5**	**D4**	**D3 .. D0**
Status Header	72 h	GS1H_7	GS1H_6	GS1H_5	GS1H_4	GS1H_3 .. GS1H_0
		odd field		even field		free running field counter
		being updated	data erroneous	being updated	data erroneous	
GS1 payload data byte 1 of odd field	73 h	GS1O1_7 .. GS1O1_0				
GS1 payload data byte 2 of odd field	74 h	GS1O2_7 .. GS1O2_0				
GS1 payload data byte 1 of even field	75 h	GS1E1_7 .. GS1E1_0				
GS1 payload data byte 2 of even field	76 h	GS1E2_7 .. GS1E2_0				

1. All decoded VBI data is written into the registers starting with the LSB of each register first until all data is stored

Table 116 Gemstar 1x data order in Gemstar 1x I²C readback registers

Register Name	GS1O1 / GS1E1								GS1O2 / GS1E2							
Register Addr.	73 h / 75 h								74 h / 76 h							
Register Bit	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
Gemstar 1x Bit No. (1)	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8

1. Gemstar 1x data bits in order they appear in the VBI data line (beginning with bit 0)

16.4.10.4 Subaddress 77 to 7F I²C Readback of Gemstar2x Data (read-only register)

Table 117 Gemstar2x I²C readback (77 h, ... , 7F h) read only

Register Content (1)	REG. ADDR.	D7	D6	D5	D4	D3 .. D0
Status Header	77 h	GS2H_7	GS2H_6	GS2H_5	GS2H_4	GS2H_3 .. GS2H_0
		odd field		even field		free running field counter
		being updated	data erroneous	being updated	data erroneous	
GS2 payload data byte 1 of odd field	78 h	GS2O1_7 .. GS2O1_0				
GS2 payload data byte 2 of odd field	79 h	GS2O2_7 .. GS2O2_0				
GS2 payload data byte 2 of odd field	7A h	GS2O3_7 .. GS2O3_0				
GS2 payload data byte 2 of odd field	7B h	GS2O4_7 .. GS2O4_0				
GS2 payload data byte 1 of even field	7C h	GS2E1_7 .. GS2E1_0				
GS2 payload data byte 2 of even field	7D h	GS2E2_7 .. GS2E2_0				
GS2 payload data byte 3 of even field	7E h	GS2E3_7 .. GS2E3_0				
GS2 payload data byte 4 of even field	7F h	GS2E3_7 .. GS2E3_0				

1. All decoded VBI data is written into the registers starting with the LSB of each register first until all data is stored

Table 118 Gemstar 2x data order in Gemstar 2x I²C readback registers

Register Name	GS2O1 / GS2E1								GS2O2 / GS2E2								GS2O1 / GS2E1								GS2O2 / GS2E2							
Register Addr.	78 h / 7C h								79 h / 7D h								7A h / 7E h								7B h / 7F h							
Register Bit	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Gemstar 2x Bit No. (1)	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	23	22	21	20	19	18	17	16	31	30	29	28	27	26	25	24

1. Gemstar 2x data bits in order they appear in the VBI data line (beginning with bit 0)

16.5 Programming Register - Interfaces and Scaler Part

16.5.1 Subaddress 80: Global Settings

Table 119 Continuous Mode (continuous field mode) (SA 80)

Global Set (80H)	**D7**
Continuous field mode	**control bit**
	CMOD
field processing is done according the trigger conditions and window definitions of an enabled programming page	0
permanent processing of the enabled task according to TEB (0x80) and TEA (0x80) settings until SW reset of the scaler. The vertical window definitions are ignored and the selected V-sync (see V_EAV1,VEAV0) defines the blanking interval	1

Table 120 Task Enable Control (SA 80)

GLOBAL SET (80H)	**D5**	**D4**
Task Enable Control	**control bits**	**control bits**
	TEB	**TEA**
task of register set A is disabled	x	0
task of register set A is enabled	x	1
task of register set B is disabled	0	x
task of register set B is enabled	1	x

Table 121 I-port and scaler backend clock selection (SA 80)

GLOBAL SET (80H)			D3	D2	D1	D0
I - port and scaler backend clock selection			**CONTROL BITS**			
MODE	**I-PORT OUTPUT CLOCK**	**SCALER BACKEND CLOCK**	**ICKS 3**	**ICKS 2**	**ICKS 1**	**ICKS 0**
8-bit output mode (byte) at full clock rate: - full data rate at full clock rate	line locked clock from decoder PLL		0	0	0	0
	input clock at XCLK input of the X-Port		0	0	0	1
	clock from feature PLL (PLL2)		0	0	1	0
	external input clock from ICLK		0	0	1	1
General 16-bit output mode: - full data rate at full clock rate Luminance data (Y) at IPD[7:0] output pins and decoded chrominance data (CB,CR) at HPD[7:0] output pins	line locked clock from decoder PLL		0	1	0	0
	input clock at XCLK input of the X-Port		0	1	0	1
	clock from feature PLL (PLL2)		0	1	1	0
	external input clock from ICLK		0	1	1	1
“DMSD2-Legacy” 16-bit output mode - half data rate at half clock rate Luminance data (Y) at IPD[7:0] output pins, decoded chrominance data (CB,CR) at HPD[7:0] output pins “CREF” function is provided on in IDQ. As an alternative IDQ can also be used as clock (adjustable delay via IPCK[3:2])	line locked clock from decoder PLL	line locked clock / 2 from decoder PLL	1	0	0	0
	input clock at XCLK input of the X-Port	input clock at XCLK input of the X-Port divided by 2	1	0	0	1
	clock from feature PLL (PLL2)	clock from feature PLL (PLL2) divided by 2	1	0	1	0
	external input clock from ICLK	external input clock from ICLK divided by 2	1	0	1	1
“Zoomed Video” 16-bit output mode: - half data rate at half clock rate (Luminance data (Y) at IPD[7:0] output pins, decoded chrominance data (CB,CR) at HPD[7:0] output pins) IDQ obsolete	line locked clock / 2 from decoder PLL		1	1	0	0
	input clock at XCLK input of the X-Port divided by 2		1	1	0	1
	clock from feature PLL (PLL2) divided by 2		1	1	1	0
	reserved		1	1	1	1

Table 122 Vertical sync and Field ID source selection (SA 81)

GLOBAL SET (81H)	D1	D0
Vertical sync and Field ID source selection for the generation of V- and F-Bit in SAV / EAV codes and the V-sync and FID function on pins IGPV and IGP0/1	**control bits**	**control bits**
	V_EAV1	**V_EAV0**
V-blanking signal from scaler input (VBLNK_CCIR from decoder or XRV from X-port) with corresponding Field ID (EVEN_CCIR or detected from X-port)	0	0
programmable V-gate signal VGATE_L from decoder (see VSTA,VSTO reg. 0x15 and 0x16 of decoder part) or XRV from X-port with corresponding Field ID (but detected ID from X-port shifted by one line)	0	1
LCR table controlled V-gate and Field ID from the text data path	1	0
CONLV controlled region and page dependent V-gate from scaler data path, Field ID is snatched to scalers V-trigger (see V123 timing)	1	1

Table 123 Characteristic of the retimed V and F signals (SA 81)

GLOBAL SET (81H)	D2
change of 1/2 line characteristic of the retimed V and F signals (see IGPV and IGP0/1 functions, signals VS_i and FID_i)	**control bits**
	FTIME
FID ‘0’ -> V-edge after End Of Line (EOL), FID change 0->1 after Start Of Line (SOL) FID ‘1’ -> V-edge after SOL, FID change 1->0 after EOL	0
upper V and FID timing characteristics change from EOL to SOL and .vv.	1

16.5.2 Subaddress 83 to 87: Global Interface Configurations

Table 124 X-port output clock phase control (SA 83)

GLOBAL SET (83H)	D5	D4
X-port output clock phase control	**control bits**	**control bits**
	XPCK1	**XPCK0**
XCLK inverted input/output phase	0	0
Recommended setting, if XCLK-pin is used as input	0	1
ICLK inverted and phase shifted by about 3 nsec	1	0
Recommended setting, if XCLK-pin is used as output	1	1

Table 125 X-port I/O enable control (SA 83)

GLOBAL SET (83H)	D2	D1	D0
X-port I/O enable control, controls pins XPD[7:0], XDQ, XRH, XRV and XCLK	**control bits**	**control bits**	**control bits**
	XRQT	**XPE1**	**XPE0**
X - port output is disabled by software	x	0	0
X - port output is enabled by software	x	0	1
X - port output is enabled by pin XTRI at “0”	x	1	0
X - port output is enabled by pin XTRI at “1”	x	1	1
XRDY output signal is A/B task flag from event handler (A = “1”)	0	x	x
XRDY output signal is ready signal from scaler path (XRDY = “1” means scaler is ready to receive data)	1	x	x

Table 126 I-port output signal definitions IGPH / IGPV (SA 84)

GLOBAL SET (84H)	D3	D2	D1	D0
I - port output signal definitions IGPH / IGPV	**control bits**	**control bits**	**control bits**	**control bits**
	IDV1	**IDV0**	**IDH1**	**IDH0**
IGPH is a h -gate signal, framing the scaler output	x	x	0	0
IGPH is an extended h-gate (framing h-gate during scaler output and scaler input H-reference outside the scaler window)	x	x	0	1
IGPH is a horizontal trigger pulse on the rising edge of h-gate	x	x	1	0
IGPH is a horizontal trigger pulse on the rising edge of extended h-gate	x	x	1	1
IGPV is a v - gate signal as defined by V_EAV[81[1:0]]	0	0	x	x
IGPV is a V-sync like signal, as defined by V_EAV, with emulated 1/2 line characteristic (VS_i)	0	1	x	x
IGPV is a vertical trigger pulse on the rising edge of the v-gate	1	0	x	
IGPV is a vertical trigger pulse on the rising edge of the V-sync like signal	1	1	x	x

Table 127 I-port signal definitions IGP0 (SA 84)

GLOBAL SET (84H AND 86H)	86H D4	84H D5	84H D4
I - port signal definitions IGP0	**control bits**	**control bits**	**control bits**
	IDG02	**IDG01**	**IDG00**
IGP0 is output field ID, as defined by V_EAV[81[1:0]]	0	0	0
IGP0 is a field ID, as defined by V_EAV and FTIME[81[2]], with emulated 1/2 line characteristic (FID_i)	0	0	1
IGP0 is sliced data flag, framing the sliced VBI data at the I-port	0	1	0
IGP0 is A/B task flag, as defined by CONLH [90[7]]	0	1	1
IGP0 is the output FIFO almost filled flag	1	0	0
IGP0 is the output FIFO almost full flag, level to be programmed in addr. 86h	1	0	1
IGP0 is the output FIFO almost empty flag, level to be programmed in addr. 86h	1	1	0
IGP0 is set to “0” (default polarity)	1	1	1

Table 128 I-port signal definitions IGP1 (SA 84)

GLOBAL SET (84H AND 86H)	86H D5	84H D7	84H D6
I - port signal definitions IGP1	**control bits**	**control bits**	**control bits**
	IDG12	**IDG11**	**IDG10**
IGP1 is output field ID, as defined by V_EAV[81[1:0]]	0	0	0
IGP1 is a field ID, as defined by V_EAV and FTIME[81[2]], with emulated 1/2 line characteristic (FID_i)	0	0	1
IGP1 is sliced data flag, framing the sliced VBI data at the I-port	0	1	0
IGP1 is A/B task flag, as defined by CONLH [90[7]]	0	1	1
IGP1 is the output FIFO almost filled flag	1	0	0
IGP1 is the output FIFO almost full flag, level to be programmed in addr. 86h	1	0	1
IGP1 is the output FIFO almost empty flag, level to be programmed in addr. 86h	1	1	0
IGP1 is set to “0” (default polarity)	1	1	1

Table 129 I-port reference signal polarities (SA 85)

GLOBAL SET (85H)	D4	D3	D2	D1	D0
I - port reference signal polarities	**control bits**	**control bits**	**control bits**	**control bits**	**control bits**
	IGP1P	**IGP0P**	**IRVP**	**IRHP**	**IDQP**
IDQ at default polarity (‘1’ active)	x	x	x	x	0
IDQ is inverted	x	x	x	x	1
IGPH at default polarity (‘1’ active)	x	x	x	0	x
IGPH is inverted	x	x	x	1	x
IGPV at default polarity (‘1’ active)	x	x	0	x	x
IGPV is inverted	x	x	1	x	x
IGP0 at default polarity	x	0	x	x	x
IGP0 is inverted	x	1	x	x	x
IGP1 at default polarity	0	x	x	x	x
IGP1 is inverted	1	x	x	x	x

Table 130 I-port signal definitions (SA 85)

GLOBAL SET (85H)	D7	D6	D5
I - port signal definitions IPD[7:0] (HPD[7:0])	control bits	control bits	control bits
	ISWP1	ISWP0	ILLV
video data limited to range 1 to 254	x	x	0
video data limited to range 8 to 247	x	x	1
D-word byte swap, influences serial output timing D0 D1 D2 D3 => FF 00 00 SAV CB0 Y0 CR0 Y1	0	0	x
D1 D0 D3 D2 => 00 FF SAV 00 Y0 CB0 Y1 CR0	0	1	x
D2 D3 D0 D1 => 00 SAV FF 00 CR0 Y1 CB0 Y0	1	0	x
D3 D2 D1 D0 => SAV 00 00 FF Y1 CR0 Y0 CB0	1	1	x

Table 131 I-port signal definitions (SA 86)

GLOBAL SET (86H)	D3	D2	D1	D0
I - port signal definitions	**control bits**	**control bits**	**control bits**	**control bits**
	FFL1	**FFL0**	**FEL1**	**FEL0**
FAE fifo flag almost empty level < 16 D-words	x	x	0	0
< 8 D-words	x	x	0	1
< 4 D-words	x	x	1	0
= 0 D-words	x	x	1	1
FAF fifo flag almost full level >= 16 D-words	0	0	x	x
>= 24 D-words	0	1	x	x
>= 28 D-words	1	0	x	x
= 32 D-words	1	1	x	x

Table 132 I-port Packing mode (continuous pixel mode) (SA 86)

Global Set (86H)	**D7**
I-Port Packing mode	**control bit**
	IMPAK
data packing controlled by ITRDY pin	0
data packing is done internally, by HREF synchronous delayed trigger pulses. The trigger delay can be defined per active data type (data of page A, page B and data of text path C). Trigger signals are generated by the Pulse Generator (see reg. F6h to FBh parameters PGHAPS, PGHBPS, PGHCPS)	1

Table 133 I-port signal definitions,FFD1,0 (SA 86)

GLOBAL SET (86H)	**D6**
I - port signal definitions, FFD1,0 related to subaddr. “84”	**control bits**
	VITX
I-port video data output is inhibited	0
I-port video data are transferred	1
Note: text data transfer is now controlled by new SLDOM control byte (reg. 0x5D)	

Table 134 I-port output clock and gated clock phase control (SA 87)

GLOBAL SET (87H)	D7	D6	D5	D4
I-port input/output clock and gated clock phase control (IDQ, ICLK)	**control bits**	**control bits**	**control bits**	**control bits**
	IPCK3	**IPCK2**	**IPCK1**	**IPCK0**
ICLK inverted input/output phase	x	x	0	0
Recommended setting, if ICLK-pin is used as input	x	x	0	1
ICLK inverted and phase shifted by about 3 nsec	x	x	1	0
Recommended setting, if ICLK-pin is used as output	x	x	1	1
Note: IPCK[3:2] only effects the gated clock or qualifier on pin IDQ in DMSD-legacy mode (see also addr. 80h, ICKS[3:0])				
tbf	0	0	x	x
tbf	0	1	x	x
tbf	1	0	x	x
tbf	1	1	x	x

Table 135 I-port I/O control (SA 87)

GLOBAL SET (87H)	D1	D0
I-port I/O control (IPD[7:0], IDQ, IGPH, IGPV, IGP0, IGP1)	**control bits**	**control bits**
	IPE1	**IPE0**
I - port output is disabled by software (including the H-port HPD[7:0] if used as 16-bit extension for the I-port)	0	0
I - port output is enabled by software	0	1
I - port output is enabled by pin ITRI at “0”	1	0
I - port output is enabled by pin ITRI at “1”	1	1

16.5.3 SUBADDRESS 88: SLEEP AND POWER SAVE CONTROL

Table 136 Power save control (SA 86)

GLOBAL SET (88H)	D3	D1	D0
power save control	control bits	control bits	control bits
	SLM3	SLM1	SLM0
decoder and VBI slicer are in operational mode	x	x	0
decoder and VBI slicer are in power down Note: scaler only operates, if scaler input and ICLK source is the X-port (refer to addr. 80h and 91/C1h)	x	x	1
scaler is in operational mode	x	0	x
scaler is in power down Note: scaler in power down stops I-port output!!	x	1	x
audio clock generation active	0	x	x
audio clock generation in power down and output disabled	1	x	x

Table 137 ADC-port output control/ startup control (SA 88)

GLOBAL SET (88H)	D7	D6	D5	D4
ADC-port output control/ startup control	control bits	control bits	control bits	control bits
	CH2EN	CH1EN	SWRST	DPROG
DPROG =’0’ after reset	x	x	x	0
DPROG = ’1’, can be used to assign that the Device has been PROGrammed.This bit can be monitored in the scalers status byte, bit PRDON. If DPROG was set to ‘1’ and PRDON status bit shows a ‘0’ a power or startup fail has occurred	x	x	x	1
scaler path is reset to it’s ‘idle’ state, software reset	x	x	0	x
scaler is switched back to operation	x	x	1	x
AD1x analog channel is in power-down mode	x	0	x	x
AD1x analog channel is active	x	1	x	x
AD2x analog channel is in power-down mode	0	x	x	x
AD2x analog channel is active	1	x	x	x

16.5.4 SUBADDRESS 8F (READ-ONLY REGISTER): STATUS INFORMATION SCALER PART

Table 138 Status information scaler bits (SA 8F)

I²C-BUS STATUS BITS	**NOTE: STATUS INFO IS UNSYNCHRONIZED AND SHOWS THE ACTUAL STATUS AT THE TIME OF IIC-READ** **FUNCTION**	**DATA BIT**
FIDSCO	status of the field sequence ID at the scalers output, scaler processing dependent	D0
FIDSCI	status of the field sequence ID at the scalers input	D1
ERR_OF	error flag of scalers output formatter, normally set, if the output processing needs to be interrupted, due to input/output data rate conflicts, e.g. if output data rate is much too low and all internal FIFO capacity used	D2
PRDON	copy of bit DPROG, can be used to detect power up and start up fails	D3
FFOV	status of the internal ‘FIFO overflow’ flag	D4
FFIL	status of the internal ‘FIFO almost filled’ flag	D5
ITRI	status on input pin ITRI, if not used for tri-state control, usable as hardware flag for software use	D6
XTRI	status on input pin XTRI, if not used for tri-state control, usable as hardware flag for software use	D7

16.5.5 SUBADDRESS 90: EVENT HANDLER CONTROL

Table 139 Event handler control (SA 90; SA C0)

REGISTER SET A (90H) AND B (C0H)	**D2**	**D1**	**D0**
event handler control	**control bits**	**control bits**	**control bits**
	RPTSK	**STRC1**	**STRC0**
event handler triggers immediately after finishing a task	x	0	0
event handler triggers with next V sync	x	0	1
event handler triggers with field ID = “0”	x	1	0
event handler triggers with field ID = “1”	x	1	1
if active task is finished, handling is taken over by the next task	0	x	x
active task is repeated once, before handling is taken over by the next task	1	x	x

Table 140 Event handler control (SA 90; SA C0)

REGISTER SET A (90H) AND B (C0H)	D5	D4	D3
event handler control	**control bits**	**control bits**	**control bits**
	FSKP2	**FSKP1**	**FSKP0**
active task is carried out directly	0	0	0
1 field is skipped before active task is carried out	0	0	1
.. fields are skipped before active task is carried out	..	..	..
6 fields are skipped before active task is carried out	1	1	0
7 fields are skipped before active task is carried out	1	1	1

Table 141 Event handler control (SA 90; SA C0)

REGISTER SET A (90H) AND B (C0H)	D7	D6
event handler control	**control bits**	**control bits**
	CONLH	**OFIDC**
output field ID is field ID from scaler input	x	0
output field ID is task status flag, which changes every time an selected task is activated (not synchronized to input field ID)	x	1
scaler SAV/EAV byte bit D7 and task flag = ‘1’, default	0	x
scaler SAV/EAV byte bit D7 and task flag = ‘0’	1	x

16.5.6 SUBADDRESS 91 TO 93: SCALER INPUT AND I-PORT OUTPUT CONFIGURATION

Table 142 Scaler Input Format and ConfigurationFormat Control (SA 91; SA C1)

REGISTER SET A (91H) AND B (C1H)	D2	D1	D0
Scaler Input Format and Configuration Format Control	**control bits**	**control bits**	**control bits**
	FSC2	**FSC1**	**FSC0**
input is YUV 4:2:2 like sampling scheme	x	x	0
input is YUV 4:1:1 like sampling scheme	x	x	1
FSC[2:1] only to be used, if X-port input source don’t provide chroma information for every input line (Note: X-port input stream must contain “dummy” chroma bytes)			
chroma is provided every line, default	0	0	x
chroma is provided every 2nd line	0	1	x
chroma is provided every 3rd line	1	0	x
chroma is provided every 4th line	1	1	x

Table 143 Scaler Input Format and ConfigurationSource Selection (SA 91; SA C1)

REGISTER SET A (91H) AND B (C1H)	D7	D6	D5	D4	D3
Scaler Input Format and Configuration Source Selection	**control bits**	**control bits**	**control bits**	**control bits**	**control bits**
	CONLV	**HLDFV**	**SCSRC1**	**SCSRC0**	**SCRQE**
only if XRQT subaddr. “83” = ‘1’: scaler input source reacts on 7115 request	x	x	x	x	0
scaler input source is a continuous data stream, which can not be interrupted (must be ‘1’, if 7115 decoder part is source of scaler or XRQT subaddr.”83” = ‘0’)	x	x	x	x	1
scaler input source is data from decoder, data type is provided according to table Table 6 on page 43	x	x	0	0	x
scaler input source is YUV data from X-port	x	x	0	1	x
scaler input source is raw digital CVBS from selected analog channel, for backward compatibility only, further use is not recommended	x	x	1	0	x
scaler input source is raw digital CVBS (or 16 bit Y + UV, if no 16 bit output are active) from X-port	x	x	1	1	x
SAV/EAV code bits D6 and D5 (F and V) may change between SAV and EAV	x	0	x	x	x
SAV/EAV code bits D6 and D5 (F and Vbit) are synchronized to scalers output line start	x	1	x	x	x
SAV/EAV code bit D5 (V-bit) and V-gate on pin IGPV as generated by the internal processing, see Fig.38	0	x	x	x	x
SAV/EAV code bit D5 (V-bit) and V-gate are inverted	1	x	x	x	x

Table 144 X-port input Reference signal definitions (SA 92; SA C2)

REGISTER SET A(92H) AND B (C2H)	D3	D2	D1	D0
X - port input Reference signal definitions	**control bits**	**control bits**	**control bits**	**control bits**
	XCODE	**XDH**	**XDQ**	**XCKS**
XCLK input clock and XDQ input qualifier are needed	x	x	x	0
data rate is defined by XCLK only, no XDQ signal used	x	x	x	1
data are qualified at XDQ input at “1”	x	x	0	x
data are qualified at XDQ input at “0”	x	x	1	x
rising edge of XRH input is horizontal reference	x	0	x	x
falling edge of XRH input is horizontal reference	x	1	x	x
reference signals are taken from XRH and XRV	0	x	x	x
reference signals are decoded from EAV and SAV	1	x	x	x

Table 145 Scaler Input Reference signal definitions (SA 92; SA C2)

REGISTER SET A(92H) AND B (C2H)	D7	D6	D5	D4
Scaler Input Reference signal definitions	**control bits**	**control bits**	**control bits**	**control bits**
	XFDV	**XFDH**	**XDV1**	**XDV0**
rising edge of XRV input and decoder V123 is vertical reference	x	x	x	0
falling edge of XRV input and decoder V123 is vertical reference	x	x	x	1
XRV is a V- sync or V-gate signal	x	x	0	x
XRV is a frame sync, V - pulses are generated internally on both edges of FS input	x	x	1	x
X-port field ID is state of XRH at reference edge on XRV (defined by XFDV)	x	0	x	x
field ID (decoder and X-port field ID) is inverted	x	1	x	x
reference edge for field detection is falling edge of XRV	0	x	x	x
reference edge for field detection is rising edge of XRV	1	x	x	x

Table 146 I-port output formats and configuration (SA 93; SA C3)

REGISTER SET A(93H) AND B (C3H)	D4	D3	D2	D1	D0
I - port output formats and configuration	**control bits**	**control bits**	**control bits**	**control bits**	**control bits**
	FOI1	**FOI0**	**FSI2**	**FSI1**	**FSI0**
4:2:2 D word formatting	x	x	0	0	0
4:1:1 D word formatting	x	x	0	0	1
4:2:0, only every 2nd line Y + UV output, in between Y only output	x	x	0	1	0
4:1:0, only every 4th line Y + UV output, in between Y only output	x	x	0	1	1
Y only	x	x	1	0	0
not defined	x	x	1	0	1
not defined	x	x	1	1	0
not defined	x	x	1	1	1
number of leading Y only lines, before 1rst Y + UV line is output: 00 = no leading Y only line .. 11= 3 leading Y only lines	0	0	x	x	x
	0	1	x	x	x
	1	0	x	x	x
	1	1	x	x	x

Table 147 I-port output formats and configuration (SA 93; SA C3)

REGISTER SET A (93H) AND B (C3H)	D7	D6	D5
I - port output formats and configuration	**control bits**	**control bits**	**control bits**
	ICODE	**INS80**	**FYSK**
all lines will be output	x	x	0
skip the number of leading Y only lines, as defined by FOI1,0	x	x	1
remaining blanking intervals and cycles with invalid data are filled with 0x00	x	0	x
remaining blanking intervals are filled with 0x80 for chroma and 0x10 for luma bytes and data are hold during cycles with invalid data	x	1	x
no ITU656 like SAV,EAV codes are available	0	x	x
ITU656 like SAV,EAV codes are inserted in the output data stream, framed by a qualifier	1	x	x

16.5.7 Subaddress 94 to 9B: Scaler Input Acquisition Window Definition

Table 148 Horizontal input acquisition window definition offset (SA 94, SA95; SA C4, SAC5)

REGISTER SET A (94H ....95H) AND B (C4H ... C5H)	95H / C5H D3 .. D0	94H / C4H D7..D4	94H / C4H D3 .. D0
horizontal input acquisition window definition offset in X (horizontal) direction **reference for counting are luminance samples**	**XO11..8**	**XO7..4**	**XO3..0**
a minimum of '2' should be kept, due to a line counting mismatch	0 0 0 0	0 0 0 0	0 0 1 0
odd offsets are changing the UV sequence in the output stream to VU sequence	0 0 0 0	0 0 0 0	0 0 1 1
maximum possible pixel offset = 4095	1 1 1 1	1 1 1 1	1 1 1 1

Table 149 Horizontal input acquisition window definition input window length (SA 96, SA97; SA C6, SAC7)

REGISTER SET A (96H ....97H) AND B (C6H ... C7H)	97H / C7H D3 .. D0	96H / C6H D7..D4	96H / C6H D3 .. D0
horizontal input acquisition window definition input window length in X (horizontal) direction **reference for counting are luminance samples**	**XS11..8**	**XS7..4**	**XS3..0**
no output	0 0 0 0	0 0 0 0	0 0 0 0
odd lengths are allowed, but will be rounded up to even lengths	0 0 0 0	0 0 0 0	0 0 0 1
...	...	...	...
maximum possible no. of input pixels = 4095	1 1 1 1	1 1 1 1	1 1 1 1

Table 150 Vertical input acquisition window definition offset (SA 98, SA99; SA C8, SA C9)

REGISTER SET A (98H ....99H) AND B (C8H ... C9H)	99H / C9H D3 .. D0	98H / C8H D7..D4	98H / C8H D3 .. D0
vertical input acquisition window definition offset in Y (vertical) direction	**YO11..8**	**YO7..4**	**YO3..0**
Note: for trigger condition (addr. 90, STRC[1:0])!= '00' YO + YS > (number of input lines/field -2), will result in field dropping	0 0 0 0	0 0 0 0	0 0 0 0
	0 0 0 0	0 0 0 0	0 0 0 1
maximum line offset = 4095 offsets > (number of input lines/field -2) will result in field dropping	1 1 1 1	1 1 1 1	1 1 1 1

Table 151 Vertical input acquisition window definition (SA 9A, SA 9B; SA CA, SA CB)

REGISTER SET A (9AH ....9BH) AND B (CAH ... CBH)	9BH / CBH D3 ..D0	9AH / CAH D7..D4	9AH / CAH D3 ..D0
vertical input acquisition window definition input window length in Y (vertical) direction	**YS11..8**	**YS7..4**	**YS3..0**
Note: for trigger condition (addr. 90, STRC[1:0])!= '00' YO + YS > (number of input lines/field -2), will result in field dropping	0 0 0 0	0 0 0 0	0 0 0 0
	0 0 0 0	0 0 0 0	0 0 0 1
	...	...	...
maximum possible number of input lines = 4095 lengths > (number of input lines/field -2) will result in field dropping	1 1 1 1	1 1 1 1	1 1 1 1

Table 152 Field processing mode (SA 9A; SACB)

Register Set A (9Bh) and B (CBh)	D7
Field mode (continuous task mode)	**control bit FMOD**
vertical processing is defined by offset and length parameters, if a V trigger occurs before YS input lines are processed field dropping may occur	0
vertical processing is defined by start and end line parameters (YO = start line, YS = end line), if a V trigger occurs before end line is reached, the vertical window is cut, if the start line is not reached at V trigger the processing is started, if the trigger occurs inside the defined region	1

16.5.8 Subaddress 9C to 9F: Scaler Output Window Definition

Table 153 Horizontal output acquisition window definition (SA 9C, SA 9D; SA CC, SA CD)

REGISTER SET A (9CH ....9DH) AND B (CCH ... CDH)	9DH / CDH D3 ..D0	9CH / CCH H D7..D4	9CH / CCH D3 ..D0
horizontal output acquisition window definition number of desired output pixel in X (horizontal) direction reference for counting are luminance samples	**XD11..8**	**XD7..4**	**XD3..0**
no output	0 0 0 0	0 0 0 0	0 0 0 0
odd lengths are allowed, but will be filled up to even lengths	0 0 0 0	0 0 0 0	0 0 0 1
...	...	...	...
maximum possible number of input pixels= 4095 if the desired output length is greater, than the number of scaled output pixels, the last scaled pixel is repeated	1 1 1 1	1 1 1 1	1 1 1 1

Table 154 Vertical output acquisition window definition (SA 9E, SA 9F; SA CE, SA CF)

REGISTER SET A (9EH ....9FH) AND B (CEH ... CFH)	9FH / CFH D3 ..D0	9EH / CEH D7..D4	9EH / CEH D3 ..D0
vertical output acquisition window definition number of desired output lines in Y (vertical)direction	**YD11..8**	**YD7..4**	**YD3..0**
no output	0 0 0 0	0 0 0 0	0 0 0 0
1 pixel	0 0 0 0	0 0 0 0	0 0 0 1
...	...	...	...
maximum possible number of output lines = 4095 if the desired output length is greater, than the number of scaled output lines, the processing is cut	1 1 1 1	1 1 1 1	1 1 1 1

16.5.9 Subaddress A0 to A2: Prescaling and FIR filtering

Table 155 Horizontal integer prescaling ratio XPSC (SA A0; SA D0)

REGISTER SET A (A0H) AND B (D0H)	D5	D4	D3	D2	D1	D0
Horizontal integer prescaling ratio XPSC	**control bits**	**control bits**	**control bits**	**control bits**	**control bits**	**control bits**
	XPSC5	**XPSC4**	**XPSC3**	**XPSC2**	**XPSC1**	**XPSC0**
!! not allowed !!	0	0	0	0	0	0
down scale = 1	0	0	0	0	0	1
down scale = 1/2	0	0	0	0	1	0
	..	..	..	..	..	..
down scale = 1/63	1	1	1	1	1	1

Table 156 Horizontal prescaler accumulation Sequence Length XACL (SA A1; SA D1)

REGISTER SET A (A1H) AND B (D1H)	D5	D4	D3	D2	D1	D0
Horizontal prescaler accumulation Sequence Length XACL	**control bits**	**control bits**	**control bits**	**control bits**	**control bits**	**control bits**
	XACL5	**XACL4**	**XACL3**	**XACL2**	**XACL1**	**XACL0**
accu length = 1	0	0	0	0	0	0
accu length = 2	0	0	0	0	0	1
	..	..	..	..	..	..
accu length = 64	1	1	1	1	1	1

Table 157 Prescaler DC gain and FIR prefilter Control (SA A2; SA D2)

REGISTER SET A (A2H) AND B (D2H)	D3	D2	D1	D0
Prescaler DC gain and FIR prefilter Control	**control bits**	**control bits**	**control bits**	**control bits**
	XC2_1	**XDCG2**	**XDCG1**	**XDCG0**
prescaler output is renormalized by gain factor = 1	x	0	0	0
gain factor = 1/2	x	0	0	1
gain factor = 1/4	x	0	1	0
gain factor = 1/8	x	0	1	1
gain factor = 1/16	x	1	0	0
gain factor = 1/32	x	1	0	1
gain factor = 1/64	x	1	1	0
gain factor = 1/128	x	1	1	1
weighting of all accumulated samples is factor ‘1’ e.g. XACL = 4 => sequence 1+ 1+ 1+ 1+ 1	0	x	x	x
weighting of samples inside sequence is factor ‘2’ e.g. XACL = 4 => sequence 1+ 2+ 2+ 2+ 1	1	x	x	x

Table 158 Prescaler DC gain and FIR prefilter Control (SA A2; SA D2)

REGISTER SET A (A2H) AND B (D2H)	D7	D6	D5	D4
Prescaler DC gain and FIR prefilter Control	**control bits**	**control bits**	**control bits**	**control bits**
	PFUV1	**PFUV0**	**PFY1**	**PFY0**
luminance FIR filter bypassed	x	x	0	0
H_y(z) = 1/4 * (1 2 1)	x	x	0	1
H_y(z) = 1/8 * (-1 1 1.75 4.5 1.75 1 -1)	x	x	1	0
H_y(z) = 1/8 * (1 2 2 2 1)	x	x	1	1
chrominance FIR filter bypassed	0	0	x	x
H_uv(z) = 1/4 * (1 2 1)	0	1	x	x
H_uv(z) = 1/32 * (3 8 10 8 3)	1	0	x	x
H_uv(z) = 1/8 * (1 2 2 2 1)	1	1	x	x

16.5.10 Subaddress A4 to A6: Brightness, Contrast and Saturation Control

Table 159 Luminance Brightness Setting (SA A4; SA D4)

REGISTER SET A (A4H) AND B (D4H)	D7	D6	D5	D4	D3	D2	D1	D0
Luminance Brightness Setting	control bits	control bits	control bits	control bits	control bits	control bits	control bits	control bits
	BRIG7	BRIG6	BRIG5	BRIG4	BRIG3	BRIG2	BRIG1	BRIG0
	0	0	0	0	0	0	0	0
nominal value = 128	1	0	0	0	0	0	0	0
	1	1	1	1	1	1	1	1

Table 160 Luminance Contrast Setting (SA A5; SA D5)

REGISTER SET A (A5H) AND B (D5H)	D7	D6	D5	D4	D3	D2	D1	D0
Luminance Contrast Setting	control bits	control bits	control bits	control bits	control bits	control bits	control bits	control bits
	CONT7	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0
gain = 0	0	0	0	0	0	0	0	0
gain = 1/64	0	0	0	0	0	0	0	1
nominal gain = 64	0	1	0	0	0	0	0	0
gain = 127/64	0	1	1	1	1	1	1	1

Table 161 Chrominance Saturation Setting (SA A6; SA D6)

REGISTER SET A (A6H) AND B (D6H)	D7	D6	D5	D4	D3	D2	D1	D0
Chrominance Saturation Setting	control bits	control bits	control bits	control bits	control bits	control bits	control bits	control bits
	SATN7	SATN6	SATN5	SATN4	SATN3	SATN2	SATN1	SATN0
gain = 0	0	0	0	0	0	0	0	0
gain = 1/64	0	0	0	0	0	0	0	1
nominal gain = 64	0	1	0	0	0	0	0	0
gain = 127/64	0	1	1	1	1	1	1	1

16.5.11 SUBADDRESS A8 TO AE: HORIZONTAL PHASE SCALING

Table 162 Horizontal Luminance Scaling Increment (SA A8, SA A9; SA D8, SA D9)

REGISTER SET A (A8H ....A9H) AND B (D8H ... D9H)	A9H / D9H D7..D4	A9H / D9H D3 ..D0	A8H / D8H D7..D4	A8H / D8H D3 ..D0
Horizontal Luminance Scaling Increment	**XSCY15..12**	**XSCY11..8**	**XSCY7..4**	**XSCY3..0**
scale = 1024/1 (theoretical) zoom	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
scale = 1024/294, lower limit defined by data path structure	0 0 0 0	0 0 0 1	0 0 1 0	0 1 1 0
scale = 1024/1023 zoom	0 0 0 0	0 0 1 1	1 1 1 1	1 1 1 1
scale = 1, equals 1024	0 0 0 0	0 1 0 0	0 0 0 0	0 0 0 0
scale = 1024/1025 down scale	0 0 0 0	0 1 0 0	0 0 0 0	0 0 0 1
scale = 1024/8191 down scale	0 0 0 1	1 1 1 1	1 1 1 1	1 1 1 1

Table 163 Horizontal Luminance Phase Offset (SA AA; SA DA)

REGISTER SET A (AAH) AND B (DAH)	D7	D6	D5	D4	D3	D2	D1	D0
Horizontal Luminance Phase Offset	**control bits**	**control bits**	**control bits**	**control bits**	**control bits**	**control bits**	**control bits**	**control bits**
	XPHY7	**XPHY6**	**XPHY5**	**XPHY4**	**XPHY3**	**XPHY2**	**XPHY1**	**XPHY0**
offset = 0	0	0	0	0	0	0	0	0
offset = 1/32 pixel	0	0	0	0	0	0	0	1
offset = 32/32 = 1 pixel	0	0	1	0	0	0	0	0
offset = 255/32 pixel	1	1	1	1	1	1	1	1

Table 164 Horizontal Chrominance Scaling Increment (SA AC, SA AD; SA DC, SA DD)

REGISTER SET A (ACH ....ADH) AND B (DCH ... DDH)	ADH / DDH D7..D4	ADH / DDH D3 ..D0	ACH / DCH D7..D4	ACH / DCH D3 ..D0
Horizontal Chrominance Scaling Increment	**XSCC15..12**	**XSCC11..8**	**XSCC7..4**	**XSCC3..0**
Note: this value must be set to the luminance value XSCY / 2	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1
	0 0 0 1	1 1 1 1	1 1 1 1	1 1 1 1

Table 165 Horizontal Chrominance Phase Offset (SA AE; SA DE)

REGISTER SET A (AEH) AND B (DEH)	D7	D6	D5	D4	D3	D2	D1	D0
Horizontal Chrominance Phase Offset	control bits	control bits	control bits	control bits	control bits	control bits	control bits	control bits
	XPHC7	XPHC6	XPHC5	XPHC4	XPHC3	XPHC2	XPHC1	XPHC0
Note: this values must be set to XPHY/2	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	1
	1	1	1	1	1	1	1	1

16.5.12 SUBADDRESS B0 TO BF: VERTICAL SCALING CONTROL

Table 166 Vertical Luminance Scaling Increment (SA B0, SA B1; SA E0, SA E1)

REGISTER SET A (B0H ....B1H) AND B (E0H ... E1H)	B1H / E1H D7..D4	B1H / E1H D3 ..D0	B0H / E0H D7..D4	B0H / E0H D3 ..D0
Vertical Luminance Scaling Increment	YSCY15..12	YSCY11..8	YSCY7..4	YSCY3..0
scale = 1024/1 (theoretical) zoom	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1
scale = 1024/1023 zoom	0 0 0 0	0 0 1 1	1 1 1 1	1 1 1 1
scale = 1, equals 1024	0 0 0 0	0 1 0 0	0 0 0 0	0 0 0 0
scale = 1024/1025 down scale	0 0 0 0	0 1 0 0	0 0 0 0	0 0 0 1
scale = 1/63.999 down scale	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1

Table 167 Vertical Chrominance Scaling Increment (SA B2, SA B3; SA E2, SA E3)

REGISTER SET A (B2H ....B3H) AND B (E2H ... E3H)	B3H / E3H D7..D4	B3H / E3H D3 ..D0	B2H / E2H D7..D4	B2H / E2H D3 ..D0
Vertical Chrominance Scaling Increment	YSCC15..12	YSCC11..8	YSCC7..4	YSCC3..0
Note: this value must be set to the luminance value YSCY	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1
	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1

Table 168 Vertical Scaling Mode Control (SA B4; SA E4)

REGISTER SET A (B4H) AND B (E4H)	D4	D0
Vertical Scaling Mode Control	**control bits**	**control bits**
	YMIR	**YMODE**
vertical scaling performs linear interpolation between lines	x	0
vertical scaling performs higher order accumulating interpolation, better alias suppression	x	1
no mirroring	0	x
lines are mirrored	1	x

Table 169 Vertical Phase Offsets Chroma / Luma (SA B8, SA BC; SA E8, SA EC)

REGISTER SET A (B8H) AND B (E8H) REGISTER SET A (BCH) AND B (ECH)	D7	D6	D5	D4	D3	D2	D1	D0
Vertical Phase Offsets Chroma / Luma	**control bits**	**control bits**	**control bits**	**control bits**	**control bits**	**control bits**	**control bits**	**control bits**
	YPC07 YPY07	**YPC06 YPY06**	**YPC05 YPY05**	**YPC04 YPY04**	**YPC03 YPY03**	**YPC02 YPY02**	**YPC01 YPY01**	**YPC00 YPY00**
offset = 0	0	0	0	0	0	0	0	0
offset of 32/32 = 1 line	0	0	1	0	0	0	0	0
offset of 255/32 lines	1	1	1	1	1	1	1	1

16.6 Programming Register - second PLL (PLL2) and Pulse Generator

16.6.1 Subaddress F0 to F5 and FF: second PLL (PLL2) Programming Parameters

Table 170 Number of LFCO cycles (= number of clock cycles divided by 4) per line (SA F0, SA F1)

SECOND PLL REGISTER SET (F0H, F1H)	F1 h, D0	F0 h, D7...0
	SPLPL8	SPLPL7 .. SPLPL0
Number of LFCO cycles per line (= number of target clock cycles per line divided by 4)		
Target Clock Frequency = 29,5 MHz (625 lines per frame)	1D8 h	
Target Clock Frequency = 24,5454 MHz (525 lines per frame)	186 h	
Target Clock Frequency = 27 MHz (625 lines per frame)	1B0 h	
Target Clock Frequency = 27 MHz (525 lines per frame)	1AD h	
Calculation Formula:	SPLPL[8:0] = (number of target clock cycles per line) / 4	

Table 171 Selecting the source of horizontal reference signal for the second PLL (PLL2) (SA F1)

Second PLL Register Set (F1 h)	D1
second PLL (PLL2) horizontal reference signal source	**SPHSEL**
The combfilter decoder is selected as horiz. sync. source.	0
The XRH signal of the X-Port (input mode) is selected as horiz. sync. source.	1

Table 172 Selecting the operation mode of the second PLL (PLL2) (SA F1)

Second PLL Register Set (F1 h)	D3	D2
second PLL (PLL2) operation mode	**SPMOD1**	**SPMOD1**
Synthesize Clock: The generated (CGC2) frequency depends on the nominal increment (SPNINC) only. The contribution of the loop filter is disabled. The I and P proportion of the loop filter is set to zero.	0 0	
PLL-closed (normal operation mode): This is the normal operation mode of the second PLL (PLL2): the nominal increment plus the content of loop filter define the output (CGC2) frequency.	0 1	
PLL-hold: The PLL keeps the last frequency before entering this mode. The content of the loop filter will be frozen.	1 0	
PLL-Re-Sync (pll_mode = 11) The phase detector is constantly re-synchronized to the horizontal reference signal. The remaining phase error is fed into the loop filter.	1 1	

Table 173 Loopfilter mode of the second PLL (PLL2) (SA F1)

Second PLL Register Set (F1 h)	D7 .. D4
second PLL (PLL2) Loop Filter mode (P- / I-Parameter selection)	**SPPI3 .. SPPI 0**
Default adaptive mode (recommended)	0000
Fast mode	0001
reserved	0002
	. . .
	1101
Medium mode	1110
Slow mode	1111

Table 174 Nominal DTO increment (SA F2, SA F3)

SECOND PLL REGISTER SET (F2 H, F3 H)	CRYSTAL CLOCK FREQUENCY	F3 h, D7 .. D0	F2 h, D7.. 0
		SPNINC15 .. SPNINC8	SPNINC7 .. SPNINC0
Nominal Increment for the DTO of the second PLL (PLL2)			
Target Clock Frequency = 29,5 MHz	32.11 MHz	3ACC h	
	24.576 MHz	4CD2 h	
Target Clock Frequency = 24,545 MHz	32.11 MHz	30EC h	
	24.576 MHz	3FEB h	
Target Clock Frequency = 27 MHz	32.11 MHz	35D0 h	
	24.576 MHz	4650 h	
Calculation Formula for the nominal increment depending on the Target Clock Frequency	XTALFREQ	integer of ((Target Clock Frequency) / (4 * XTALFREQ) * 2^16))	

Table 175 Lock Status of the second PLL (PLL2) (SA F4)

Second PLL Register Set (F4 H)	D0
Lock Status of the second PLL (PLL2)	**SPLOCK**
second PLL (PLL2) un-locked	0
second PLL (PLL2) locked	1

Table 176 Maximum Phase Error Threshold for lock detection of the second PLL (PLL2) (SA FF)

Second PLL Register Set (FF h)	**D3 .. D0**
Maximum Phase Error Threshold for lock detection of the second PLL (PLL2)	**SPTHRM3 .. SPTHRM0**
Maximum Phase Error >= 0 %	0000
Maximum Phase Error >= 6.25 %	0001
Maximum Phase Error >= 12.5 %	0010
Maximum Phase Error >= 18.75 %	0011
Maximum Phase Error >= 25 %	0100
Maximum Phase Error >= 31.5 %	0101
Maximum Phase Error >= 37.5 %	0110
Maximum Phase Error >= 44 %	0111
Maximum Phase Error >= 50 %	1000
Maximum Phase Error >= 56 %	1001
Maximum Phase Error >= 63 %	1010
Maximum Phase Error >= 69 %	1011
Maximum Phase Error >= 75 %	1100
Maximum Phase Error >= 81 %	1101
Maximum Phase Error >= 88 %	1110
Maximum Phase Error >= 94 %	1111

Table 177 Number of Lines Threshold for lock detection of the second PLL (PLL2) (SA FF)

Second PLL Register Set (FF h)	D7 .. D4
Minimum Number of Lines while SPTHRM[3:0] must be smaller than specified before for lock detection of the second PLL (PLL2) will be indicated	**SPTHRL3 .. SPTHRL0**
7 lines	0000
15 lines	0001
23 lines	0010
31 lines	0011
39 lines	0100
47 lines	0101
55 lines	0110
63 lines	0111
71 lines	1000
79 lines	1001
87 lines	1010
95 lines	1011
103 lines	1100
111 lines	1101
119 lines	1110
127 lines	1111

16.6.2 SUBADDRESS F6 TO FB: PULSE GENERATOR PROGRAMMING

Table 178 Number of LFCO cycles (= number of clock cycles divided by 4) per line (SA F5, SA F6)

PULSE GENERATOR REGISTER SET (F5H, F6H)	F6 h, D0	F5 h, D7...0
	PGLEN8	PGLEN7 .. PGLEN0
This setting must be equal to the number of LFCO cycles per line since it defines the output line length at the I-port when driven by the Pulse Generator		
Target Clock Frequency = 29,5 MHz (625 lines per frame)	1D8 h	
Target Clock Frequency = 24,5454 MHz (525 lines per frame)	186 h	
Target Clock Frequency = 27 MHz (625 lines per frame)	1B0 h	
Target Clock Frequency = 27 MHz (525 lines per frame)	1AD h	
Calculation Formula:	PGLEN[8:0] = (number of target clock cycles per line) / 4	

Table 179 Selecting the source of horizontal reference signal for the PULSE Generator (SA F6)

PULSE Generator Register Set (F6 H)	D1
PULSE Generator horizontal reference signal source for re-synchronisation	**PGHSEL**
The combfilter decoder is selected as horiz. sync. source.	0
The XRH signal of the X-Port (input mode) is selected as horiz. sync. source.	1

Table 180 Resetting (Resynchronizing) the PULSE Generator to a horizontal synchronisation event. (SA F6)

PULSE Generator Register Set (F6 H)	D2
PULSE Generator horizontal reference signal source for re-synchronisation	**PGRES**
The Pulse generator is in free running mode.	0
Software reset/resync for the Pulse Generator. The internal counter and thus all generated signals (Pulse A trigger, Pulse B trigger and Pulse C trigger) will be resyncronized to the incoming horiz. sync. source (defined by PGHSEL) as long as pulse_gen_res is programmed to '1'	1

Table 181 Pulse C trigger position for Task A (SA F6, SA F7)

PULSE Generator Register Set for Start of line for scaler Register Set A (F6h ... F7h)	F6H D7 ..D4	F7H D7..D4	F7H D3 ..D0
Pulse C trigger position for Task A data relative to the pulse generator counter measured in clock cycles.	**PGHAPS 11...8**	**PGHAPS 7...4**	**PGHAPS 3...0**
lowest value of pulse A	0 0 0 0	0 0 0 0	0 0 0 0
...	...	...	...
Recommended value for ITU style receiver operating with SAV codes aligned	60E hex (1550 decimal)		
Recommended value for ITU style receiver operating with EAV codes aligned	60E hex (1550 decimal)		
...	...	...	...
latest position of pulse A Note: If PGHAPS is greater than PGLEN * 4 then the pulse A will not be generated!	1 1 1 1	1 1 1 1	1 1 1 1

Table 182 Pulse B trigger position for Task B (SA F8, SA F9)

PULSE Generator Register Set for Start of line for scaler Register Set B (F8h ... F9h)	**F8H D7 ..D04**	**F9H D7..D4**	**F9H D3 ..D0**
Pulse B trigger position for Task B data relative to the pule generator counter measured in clock cycles.	**PGHBPS 11...8**	**PGHBPS 7...4**	**PGHBPS 3...0**
lowest value of pulse B	0 0 0 0	0 0 0 0	0 0 0 0
...	...	...	...
Recommended value for ITU style receiver operating with SAV codes aligned	PGHBPS = PGHAPS 60E hex (1550 decimal)		
Recommended value for ITU style receiver operating with EAV codes aligned	PGHBPS = PGHAPS 60E hex (1550 decimal)		
...	...	...	...
latest position of pulse B Note: If PGHBPS is greater than PGLEN * 4 then the pulse B will not be generated!	1 1 1 1	1 1 1 1	1 1 1 1

Table 183 Pulse C trigger position for sliced VBI data (SA FA, SA FB)

PULSE Generator Register Set for end of line definition (FAh ... FBh)	**FAH D7 ..D04**	**FBH D7..D4**	**FBH D3 ..D0**
Pulse C trigger position for sliced VBI data relative to the pule generator counter measured in clock cycles.	**PGHCPS 11...8**	**PGHCPS 7...4**	**PGHCPS 3...0**
lowest value of pulse C	0 0 0 0	0 0 0 0	0 0 0 0
...	...	...	...
Recommended value for ITU style receiver operating with SAV codes aligned	PGHCPS = PGHBPS = PGHAPS 60E hex (1550 decimal)		
Recommended value for ITU style receiver operating with EAV codes aligned	PGHCPS = (PGHAPS - 48 + (XD * 2)) mod (PGLEN * 4)		
...	...	...	...
latest position of pulse C Note: If PGHCPS is greater than PGLEN * 4 then the pulse C will not be generated!	1 1 1 1	1 1 1 1	1 1 1 1

17 PROGRAMMING START SET-UP

17.1 Decoder part

The given values force the following behaviour of the SAA7115 video decoder part:

- Analog input conditions: NTSC M, PAL B, D, G, H, I or SECAM signal in CVBS format on input AI11(column 1) or Y/C-format on inputs AI11, AI21 (column 2)
- Analog anti-alias filter and AGC active
- Automatic field detection enabled
- Automatic TV/VCR detection enabled
- Automatic color standard detection enabled (column 1 and 2: Auto mode 3: predefined filters, sharpness control disabled)
- Standard ITU 656 output format enabled on expansion (X) port, see also subaddress 83h (X-port control)
- Contrast, brightness and saturation control in accordance with ITU standards
- Adaptive comb filter for luminance and chrominance activated
- Pins LLC, LLC2, XTOUT, RTS0, RTS1 and RTCO are set to 3-state
- I-port (scaled video-output) and audio clock generation are disabled (lower power consumption), see corresponding sections to activate their functionality.
- Columns 3 to 5 are examples for typical settings in non auto mode.

Table 184 Decoder part start set-up values for auto mode and the three main standards

SUB ADDR. (HEX)	REGISTER FUNCTION	CONTROL NAMES(1)	REMARKS	VALUES (HEX)				
				(1) FULL AUTO MODE (CVBS)	(2) FULL AUTO MODE (Y/C)	(3) NTSC M (CVBS)	(4) PAL B, D, G, H AND I (CVBS)	(5) SECAM (CVBS)
00	chip version	ID7 to ID0		read only				
01	increment delay	AOSL2, WPOFF, GUDL1, GUDL0 and IDEL3 to IDEL0	white peak control activated	08	08	08	08	08
02	analog input control 1	FUSE1, FUSE0, X,X, and MODE3 to MODE0	CVBS signal expected at input AI11 (CVBS-modes) Y signal expected at input AI11, C signal expected at input AI21 (Y/C-mode)	C0	C8	C0	C0	C0

SUB ADDR. (HEX)	REGISTER FUNCTION	CONTROL NAMES(1)	REMARKS	VALUES (HEX)				
				(1) FULL AUTO MODE (CVBS)	(2) FULL AUTO MODE (Y/C)	(3) NTSC M (CVBS)	(4) PAL B, D, G, H AND I (CVBS)	(5) SECAM (CVBS)
03	analog input control 2	X, HLNRS, VBSL, CPOFF, HOLDG, GAFIX, GAI28 and GAI18	AGC active with long vertical blanking, color peak control active	20	20	20	20	20
04	analog input control 3	GAI17 to GAI10	no influence	90	90	90	90	90
05	analog input control 4	GAI27 to GAI20	no influence	90	90	90	90	90
06	horizontal sync start	HSB7 to HSB0	just an example	EB	EB	EB	EB	EB
07	horizontal sync stop	HSS7 to HSS0	just an example	E0	E0	E0	E0	E0
08	sync control	AUFD, FSEL, FOET, HTC1, HTC0, HPLL, VNOI1 and VNOI0	automatic field detection active, automatic time constant setting active, vertical noise reduction active	B0	B0	B0	B0	B0
09	luminance control	BYPS, YCOMB, LDEL, LUBW and LUFI3 to LUFI0	LUBW and LUFI controls are automatically adjusted via AUTO[1:0] = 01 (= auto mode 3), therefore these settings take only effect at lower auto levels!	40	80	40	40	1B
0A	luminance brightness control	DBRI7 to DBRI0	default brightness	80	80	80	80	80
0B	luminance contrast control	DCON7 to DCON0	default contrast	44	44	44	44	44
0C	chrominance saturation control	DSAT7 to DSAT0	default saturation	40	40	40	40	40
0D	chrominance hue control	HUEC7 to HUEC0	default hue	00	00	00	00	00

SUB ADDR. (HEX)	REGISTER FUNCTION	CONTROL NAMES(1)	REMARKS	VALUES (HEX)				
				(1) FULL AUTO MODE (CVBS)	(2) FULL AUTO MODE (Y/C)	(3) NTSC M (CVBS)	(4) PAL B, D, G, H AND I (CVBS)	(5) SECAM (CVBS)
0E	chrominance control 1	CDTO, CSTD2 to CSTD0, DCVF, FCTC, AUTO0 and CCOMB	DCVF control is automatically adjusted via AUTO[1:0] = 01or 10 (= auto modes 2 and 3), therefore this setting takes only effect in auto modes 0 or 1 (AUTO[1:0] = 00 or 11)	07	07	8D	85	D4
0F	chrominance gain control	ACGC and CGAIN6 to CGAIN0	automatic color gain control active via ACGC = 0, CGAIN setting has no effect	2A	2A	2A	2A	2A
10	chrominance control 2	OFFU1, OFFU0, OFFV1, OFFV0, CHBW and LCBW2 to LCBW0	auto level 3 active in column 1 and 2, CHBW and LCBW settings have no effect	06	06	06	06	00
11	mode/delay control	COLO, RTP1, HDEL1, HDEL0, RTP0 and YDEL2 to YDEL0	automatic color killer active	00	00	00	00	00
12	RT signal control	RTSE13 to RTSE10 and RTSE03 to RTSE00	RTS0 and RTS1 are tristated	00	00	00	00	00
13	RT/X-port output control	RTCE, XRHS, XRVS1, XRVS0, HLSEL and OFTS2 to OFTS0	RTCO is tristated, Xport output format is set to ITU656-mode	00	00	00	00	00
14	analog/ADC/compatibility control	CM99, UPTCV, AOSL1, AOSL0, XTOUTE, AUTO1, APCK1 and APCK0	analog output is disabled, crystal clock output is disabled, default adc sample phase selected	01	01	01	01	01
15	VGATE start, FID change	VSTA7 to VSTA0	just an example	11	11	11	11	11
16	VGATE stop	VSTO7 to VSTO0	just an example	FE	FE	FE	FE	FE
17	miscellaneous, VGATE configuration and MSBs	LLCE, LLC2E, LATY2 to LATY0, VGPS, VSTO8 and VSTA8	LLC and LLC2-outputs tristated, standard search latency is set to 3 fields (default)	D8	D8	D8	D8	D8

SUB ADDR. (HEX)	REGISTER FUNCTION	CONTROL NAMES(1)	REMARKS	VALUES (HEX)				
				(1) FULL AUTO MODE (CVBS)	(2) FULL AUTO MODE (Y/C)	(3) NTSC M (CVBS)	(4) PAL B, D, G, H AND I (CVBS)	(5) SECAM (CVBS)
18	raw data gain control	RAWG7 to RAWG0	default raw data gain	40	40	40	40	40
19	raw data offset control	RAWO7 to RAWO0	default raw data offset	80	80	80	80	80
1A	QUAM/SECAM color killer levels	QTHR3 to QTHR0, STHR3 to STHR0	default color killer thresholds	77	77	77	77	77
1B	TV/VCR-detection sensitivity, xport output format (MSB), automatic color limiter, fast sequence correction control	ATVT1 to ATVT0, X, OFTS3, x, ACOL, FSQC	default TV/VCR-switch sensitivity, xport output format 8 bit, automatic color limiter active, noise insensitive PAL/SECAM sequence correction	42	42	42	42	42
1C	enhanced combfilter control 1	HODG1 to HODG0, VEDG1 to VEDG0, MEDG1 to MEDG0, CMBT1 to CMBT0, VEDT1 to VEDT0	default combfilter parameters	A9	A9	A9	A9	A9
1D	enhanced combfilter control 2	X, X, X, X, X, X, VEDT1 to VEDT0	default combfilter parameters	01	01	01	01	01
1E	status byte 1 video decoder	NFLD, HLCK, SLTCA, GLIMT, GLIMB, WIPA, DCSTD1 and DCSTD0		read only				
1F	status byte 2 video decoder	INTL, HLVLN, FIDT, STTB, TYPE3, COLSTR, COPRO and RDCAP		read only				

SUB ADDR. (HEX)	REGISTER FUNCTION	CONTROL NAMES[1]	REMARKS	VALUES (HEX)				
				(1) FULL AUTO MODE (CVBS)	(2) FULL AUTO MODE (Y/C)	(3) NTSC M (CVBS)	(4) PAL B, D, G, H AND I (CVBS)	(5) SECAM (CVBS)
41 to 57	Line Control registers (located in the data slicer section)	LCR02[7:0] to LCR24[7:0]	request processed video data type for all lines at xport	00	00	00	00	00
83	Xport IO Control registers (located in the scaler global section)	XPCK1 to XPCK0, XRQT, XPE1 to XPE0	enable xport output with correct timing	31	31	31	31	31
88	Power save control registers (located in the scaler global section)	XPCK1 to XPCK0, XRQT, XPE1 to XPE0	enable only the required ADC's and the video decoder, switch scaler and audio clock generation into sleep mode.	4A	CA	4A	4A	4A

Note

1. All "X" values must be set to logic 0.

17.2 Audio clock generation part

The given values force the following behaviour of the SAA7115 audio clock generation part:

- Used crystal is 24.576 MHz
- Expected field frequency is 59.94 Hz (e.g. NTSC M standard)
- Generated audio master clock frequency at pin AMCLK is 256 × 44.1 kHz = 11.2896 MHz
- AMCLK is frame-locked to the incoming video signal
- AMCLK is directly generated by the audio clock PLL, no CGC2 is used
- AMCLK is externally connected to AMXCLK [short-cut between pins 37 and 41]
- ASCLK (bit clock) = 32 × 44.1 kHz = 1.4112 MHz
- ALRCLK (word select) is 44.1 kHz.

Table 185 Audio clock part set-up values

SUB ADDRESS (HEX)	REGISTER FUNCTION	BIT NAME(1)	START VALUES								
			7	6	5	4	3	2	1	0	HEX
30	audio master clock cycles per field; bits 7 to 0	ACPF7 to ACPF0	1	0	1	1	1	1	0	0	BC
31	audio master clock cycles per field; bits 15 to 8	ACPF15 to ACPF8	1	1	0	1	1	1	1	1	DF
32	audio master clock cycles per field; bits 17 and 16	X, X, X, X, X, X, ACPF17 and ACPF16	0	0	0	0	0	0	1	0	02
33	reserved	X, X, X, X, X, X, X, X	0	0	0	0	0	0	0	0	00
34	audio master clock nominal increment; bits 7 to 0	ACNI7 to ACNI0	1	1	0	0	1	1	0	1	CD
35	audio master clock nominal increment; bits 15 to 8	ACNI15 to ACNI8	1	1	0	0	1	1	0	0	CC
36	audio master clock nominal increment; bits 21 to 16	X, X, ACNI21 to ACNI16	0	0	1	1	1	0	1	0	3A
37	reserved	X, X, X, X, X, X, X, X	0	0	0	0	0	0	0	0	00
38	clock ratio AMXCLK to ASCLK	X, X, SDIV5 to SDIV0	0	0	0	0	0	0	1	1	03
39	clock ratio ASCLK to ALRCLK	X, X, LRDIV5 to LRDIV0	0	0	0	1	0	0	0	0	10
3A	audio clock generator basic set-up	UCGC, CGCDIV, X, X, APLL, AMVR, LRPH, SCPH	0	0	0	0	0	0	0	0	00
3B to 3F	reserved	X, X, X, X, X, X, X, X	0	0	0	0	0	0	0	0	00

Note

1. All “X” values must be set to logic 0.
2. See also chapter 8.7: “Audio clock generation (subaddresses 30H to 3FH)” for more examples.

17.3 Data slicer and data type control part

The given values force the following behaviour of the SAA7115 VBI-data slicer part:

- Closed captioning data are expected at line 21 of field 1 (60 Hz/525 line system)
- All other lines are processed as active video
- Sliced data are framed by ITU 656 like SAV/EAV sequence, no re-coding of data bytes.
- Sliced data packages for all defined vbi standards, see Table 107: “Sliced data output modes (SA 5D)”
- example for ITU656 correct line counting, field ID of VBI slicer is swapped (see 8.2 and 8.4)

Table 186 Data slicer start set-up values

SUB ADDRESS (HEX)	REGISTER FUNCTION	BIT NAME(1)	START VALUES								
			7	6	5	4	3	2	1	0	HEX
40	slicer control 1	CHKWSS, HAM_N, FCE, HUNT_N, X, X, X, X	0	1	0	0	0	0	0	0	40
41 to 53	line control register 2 to 20	LCRn_7 to LCRn_0 (n = 2 to 20)	0	0	0	0	0	0	0	0	00
54	line control register 21	LCR21_7 to LCR21_0	0	1	0	0	0	0	0	0	4F
55 to 57	line control register 22 to 24	LCRn_7 to LCRn_0 (n = 22 to 24)	0	0	0	0	0	0	0	0	00
58	programmable framing code	FC7 to FC0	0	0	0	0	0	0	0	0	00
59	horizontal offset for slicer	HOFF7 to HOFF0	0	1	0	0	0	1	1	1	47
5A	vertical offset for slicer	VOFF7 to VOFF0	0	0	0	0	0	1	1	0	06(2)
5B	field offset and MSBs for horizontal and vertical offset	FOFF, X, VEP, VOFF8, X, HOFF10 to HOFF8	1	0	0	0	0	0	1	1	83(2)
5C	reserved	X, X, X, X, X, X, X, X	0	0	0	0	0	0	0	0	00
5D	sliced data output mode	X, X, X, SLDOM4 to SLDOM0	0	0	0	0	1	1	0	0	0C
5E	sliced data identification code	X, X, SDID5 to SDID0	0	0	0	0	0	0	0	0	00
5F	reserved	X, X, X, X, X, X, X, X	0	0	0	0	0	0	0	0	00
60	slicer status byte 0	–, FC8V, FC7V, VPSV, PPV, CCV, –, –	read-only register								
61	slicer status byte 1	–, –, F21_N, LN8 to LN4	read-only register								
62	slicer status byte 2	LN3 to LN0, DT3 to DT0	read-only register								

Notes

1. All X values must be set to logic 0.
2. Changes for 50 Hz/625 line systems: subaddress 5AH = 03H and subaddress 5BH = 03H.

17.4 Scaler and interfaces

Table 187 shows some examples for the scaler programming with:

- prsc = prescale ratio
- fisc = fine scale ratio
- vsc = vertical scale ratio.

The ratio is defined as: $\frac{\text{number of input pixel}}{\text{number of output pixel}}$

In the following settings the VBI-data slicer is inactive. To activate the VBI-data slicer, SLDOM 5DH[4:0] has to be set to > ‘00H’.

To compensate the running-in of the vertical scaler, the vertical input window lengths are extended by 2 to 290 lines, respectively 242 lines for XS, but the scaler increment calculations are done with 288, respectively 240 lines.

Trigger condition

For trigger condition STRC[1:0]90H[1:0] not equal ‘00’.

If the value of (YO + YS) is greater equal 262 (NTSC), respectively 312 (PAL) the output field rate is reduced to 30 Hz, respectively 25 Hz.
Horizontal and vertical offsets (XO and YO) have to be used to adjust the displayed video in the display window. As this adjustment is application dependent, the listed values are only dummy values.

Maximum zoom factor

The maximum zoom factor is dependent on the back-end data rate and therefore back-end clock and data format dependent (8 or 16-bit output). The maximum horizontal zoom is limited to about 3.5, due to internal data path restrictions.

17.4.1 EXAMPLES

Table 187 Example configurations

EXAMPLE NUMBER	SCALER SOURCE AND REFERENCE EVENTS	INPUT WINDOW	OUTPUT WINDOW	SCALE RATIOS

1	analog input to 8-bit I-port output, with SAV/EAV codes and '8010' blanking, 8-bit serial byte stream decoder output at X-port; acquisition trigger at rising edge vertical and rising edge horizontal reference signal; '1' active H and V-gates on IGPH and IGPV, IGP0 = field ID, IGP1 = sliced VBI data flag, IMPAK = '1' = the pulse generator need to be programmed (addr. 0xF5 to 0xFB)
	IDQ qualifier logic 1 active
		720 × 240	720 × 240	prsc = 1;
				fisc = 1;
				vsc = 1

2	**window definitions and scale ratio according SQP NTSC-M**
	analog input to 8-bit I-port output, with SAV/EAV codes and '8010' blanking, 8-bit serial byte stream decoder output at X-port; acquisition trigger at rising edge vertical and rising edge horizontal reference signal; '1' active H and V-gates on IGPH and IGPV, IGP0 = field ID, IGP1 = sliced VBI data flag, IMPAK = '1' = the pulse generator need to be programmed (addr. 0xF5 to 0xFB)
	PLL2 clock used (ICKS[1:0] = 2),
	refer to section 17.5 , Example 2
	IDQ qualifier logic 1 active
		704 × 240	640 × 240	prsc = 1;
				fisc = 1.1;
				vsc = 1

3	**window definitions and scale ratio according SQP PAL-BG**
	analog input to 16-bit output, without SAV/EAV codes, Y on I-port, C_B-C_R on H-port and decoder output at X-port; acquisition trigger at rising edge vertical and rising edge horizontal reference signal; '1' active H-gate and V-sync on IGPH and IGPV, IGP0= field ID, IGP1 = filled flag,
	IMPAK = '1' = the pulse generator need to be programmed (addr. 0xF5 to 0xFB)
	PLL2 clock used (ICKS[1:0] = 2)
	refer to sect.17.5 , Example 3
	IDQ = CREF like qualifier at (PLL2 clock)/2 data rate
		704 × 288	768 × 288	prsc = 1;
				fisc = 0.91667;
				vsc = 1

4	X-port input 8 bit with SAV/EAV codes, no reference signals on XRH and XRV, XCLK as gated clock; field detection and acquisition trigger on different events; acquisition triggers at falling edge vertical and rising edge horizontal; I-port output 8 bit with SAV/EAV codes like example number 1	720 × 240	352 × 288	prsc = 2;
				fisc = 1.022;
				vsc = 0.8333

5	X-port and H-port for 16-bit Y-CB-CR 4 : 2 : 2 input (if no 16-bit output selected); XRH and XRV as references; field detection and acquisition trigger at falling edge vertical and rising edge horizontal; I-port output 8 bit with SAV/EAV codes, but Y only output	720 × 288	200 × 80	prsc = 2;
				fisc = 1.8;
				vsc = 3.6

Table 188 Scaler and interface configuration example

I²C-BUS ADDRESS (HEX)	MAIN FUNCTIONALITY	EXAMPLE 1		EXAMPLE 2		EXAMPLE 3		EXAMPLE 4		EXAMPLE 5	
		HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC
Global settings											
80	task enable, IDQ and back-end clock definition	90	–	92	–	9A	–	10	–	10	–
81	V-blanking and FID source selection	00	–	00	–	00	–	00	–	00	–
83	XCLK output phase and X-port output enable	31	–	31	–	31	–	10	–	10	–
84	IGPH, IGPV, IGP0 and IGP1 output definition	80	–	80	–	04	–	A0	–	A0	–
85	signal polarity control and I-port byte swapping	00	–	00	–	00	–	10	–	10	–
86	FIFO flag thresholds, video enable and data packing, if IMPAK = ‘1’, the pulse generator needs to be programmed (addr. 0xF5 to 0xFB)	C5	–	C5	–	EA	–	45	–	45	–
87	ICLK and IDQ output phase and I-port enable	31	–	31	–	31	–	31	–	31	–
88	power save control and software reset	F0	–	F0	–	F0	–	F0	–	F0	–
Task A: scaler input configuration and output format settings											
90	task handling	00	–	00	–	00	–	00	–	00	–
91	scaler input source and format definition	08	–	08	–	08	–	18	–	38	–
92	reference signal definition at scaler input	00	–	00	–	00	–	19	–	11	–
93	I-port output formats and configuration	C0	–	C0	–	00	–	C0	–	84	–
Input and output window definition											
94	horizontal input offset (XO)	04	4	10	16	10	16	04	4	04	4
95		00	–	00	–	00	–	00	–	00	–
96	horizontal input (source) window length (XS)	D0	720	C0	704	C0	704	D0	720	D0	720
97		02	–	02	–	02	–	02	–	02	–
98	vertical input offset (YO)	07	263	07	263	39	313	0A	10	0A	10
99		01	–	01	–	01	–	00	–	00	–
9A	vertical input (source) window length (YS)	06	262	06	262	38	312	F2	242	22	290
9B		01	–	01	–	01	–	00	–	01	–
	FMOD bit D7	1	1	1	1	1	1	0	0	0	0

I²C-BUS ADDRESS (HEX)	MAIN FUNCTIONALITY	EXAMPLE 1		EXAMPLE 2		EXAMPLE 3		EXAMPLE 4		EXAMPLE 5	
		HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC
9C	horizontal output (destination) window length (XD)	D0	720	80	640	00	768	60	352	C8	200
9D		02	–	02	–	03	–	01	–	00	–
9E	vertical output (destination) window length (YD)	07	263	07	263	39	313	20	288	50	80
9F		01	–	01	–	01	–	01	–	00	–
Prefiltering and prescaling											
A0	integer prescale (value ‘00’ not allowed)	01	–	01	–	01	–	02	–	02	–
A1	accumulation length for prescaler	00	–	00	–	00	–	02	–	03	–
A2	FIR prefilter and prescaler DC normalization	00	–	00	–	00	–	AA	–	F2	–
A4	scaler brightness control	80	128	80	128	80	128	80	128	80	128
A5	scaler contrast control	40	64	40	64	40	64	40	64	11	17
A6	scaler saturation control	40	64	40	64	40	64	40	64	11	17
Horizontal phase scaling											
A8	horizontal scaling increment for luminance	00	1024	66	1126	AA	938	18	1048	34	1844
A9		04	–	04	–	03	–	04	–	07	–
AA	horizontal phase offset luminance	00	–	00	–	00	–	00	–	00	–
AC	horizontal scaling increment for chrominance	00	512	33	563	D5	469	0C	524	9A	922
AD		02	–	02	–	01	–	02	–	03	–
AE	horizontal phase offset chrominance	00	–	00	–	00	–	00	–	00	–
Vertical scaling											
B0	vertical scaling increment for luminance	00	1024	00	1024	00	1024	55	853	66	3686
B1		04	–	04	–	04	–	03	–	0E	–
B2	vertical scaling increment for chrominance	00	1024	00	1024	00	1024	55	853	66	3686
B3		04	–	04	–	04	–	03	–	0E	–
B4	vertical scaling mode control	00	–	00	–	00	–	00	–	01	–
B8 to BF	vertical phase offsets luminance and chrominance (need to be used for interlace correct scaled output)	start with B8 to BF at 00H, if there are no problems with the interlaced scaled output optimize according to Section 8.3.3.2 start with B8 to BF at 00H, if there are no problems with the interlaced scaled output optimize according to Section 8.3.3.2									

17.5 PLL2 and pulse generator control part

The given values force the following behaviour of the SAA7115 PLL2 clock and pulse generation part, where the pulse generation values are for 8 bit I-port output with ITU like code sequences:

- Example 1:
  PLL2 - synthesis of line locked square pixel clock of 24.545454 MHz from 24.576 MHz crystal
  pulse generator - pulse generation for 1560 clock cycles per line and video (640 pixel=1288 bytes) from page A and raw data (1448 bytes) from page B, no deep buffering, delay only used for EAV alignment, VBI stream as timing master
  a corresponding scaler programming (only for page A) can be found in sect. 17.4 , Example 2
- Example 2:
  PLL2 - synthesis of line locked square pixel clock of 29.5 MHz from 32.11 MHz crystal
  pulse generator - pulse generation for 1888 clock cycles per line and video A (768 pixel=1544 bytes) + sliced VBI, EAV aligned, medium pixel buffering, PGHCPS somewhere in the allowed range
  a corresponding scaler programming can be found in sect. 17.4 , Example 3
- PLL2 in normal operation (SPMOD[1:0] = ‘01’) for all examples
- for 32.11 Mhz crystal (external strapping resistor required)

Table 189 PLL2 and pulse generator start set-up values

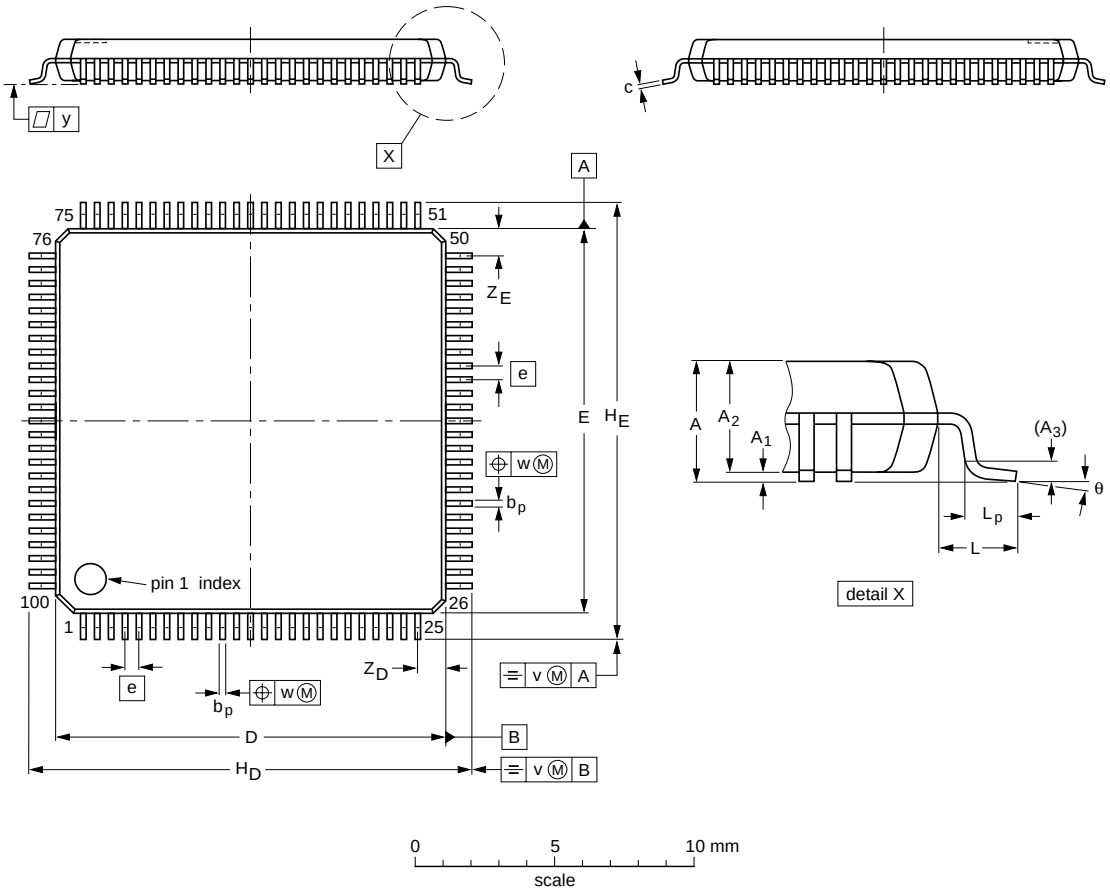
SUB ADDRESS (HEX)	REGISTER FUNCTION	BIT NAME(1)	EXAMPLE 1		EXAMPLE 2	
			HEX	DEC	HEX	DEC
F0	LFCO's per line (LSB's)	SPLPL7 to SPLPL0	86	390	D8	472
F1	PI-parameter selection, PLL mode, PLL-Hsync-selection, LFCO's per line (MSB)	SPPI3 to SPPI0, SPMOD1, SPMOD0, SPHSEL, SPLPL8	05		05	
F2	Nominal PLL2 DTO increment (LSB's)	SPNINC7 to SPNINC0	EB	16363	CC	15052
F3	Nominal PLL2 DTO increment (MSB's)	SPNINC15 to SPNINC8	3F		3A	
F4	PLL2 lock status	–, –, –, –, –, –, –, SPLOCK				
F5	Pulse generator line length (LSB's)	PGLEN7 to PGLEN0	86	390	D8	472
F6	Pulse A position (LSB's), Pulsegen resync and Hsync selection, Pulse generator line length (MSB)	PGHAPS3 to PGHAPS0, X, PGRES, PGHSEL, PGLEN8	01		C1	
F7	Pulse A position (MSB's)	PGHAPS11 to PGHAPS4	13	304	2B	700
F8	Pulse B position (LSB's)	PGHBPS3 to PGHBPS0,X,X,X,X	00	144	00	0
F9	Pulse B position (MSB's)	PGHBPS11 to PGHBPS4	09		00	
FA	Pulse C position (LSB's)	PGHCPS3 to PGHCPS0,X,X,X,X	00	1536	C0	300
FB	Pulse C position (MSB's)	PGHCPS11 to PGHCPS4	60		12	
FC to FE	reserved	X, X, X, X, X, X, X, X	00	0	00	0
FF	PLL locking thresholds	SPTHRL3 to SPTHR0, SPTHRM3 to SPTHRM0	88	136	88	136

Notes

1. All X values must be set to logic 0.
2. max. values for pulse positions are 4 x PGLEN[8:0], e.g. PGLEN = 429, PGHxPS max = 1716.
3. the position counter starts with count '1', for the value of '0' no trigger pulses are generated

18 PACKAGE OUTLINE

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1.0	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT407-1	136E20	MS-026				~~00-01-19~~ 00-02-01