REALTEK

RTL8139C(L)+

Advanced PCI/Mini-PCI/Cardbus 3.3V Single-Chip 10/100M Fast Ethernet Controller

General Description

This product is covered by one or more of the following patents:
US5,307,459, US5,434,872, US5,732,094, US6,570,884, US6,115,776, and US6,327,625.

The Realtek RTL8139C(L)+ is a highly integrated and cost-effective single-chip Fast Ethernet controller. It provides enhanced buffer management with descriptor-based TX/RX architecture to greatly reduce CPU utilization. Fully complying with Microsoft NDIS5 Checksum and Segmentation Task-offload feature, the RTL8139C(L)+ is able to optimize system performance. Also supporting IEEE802.1Q VLAN (Virtual Bridged Local Area Network) and PCI DAC (Dual Address Cycle), the new chip provides an optimum LAN solution for high-end and heavy-trafficked computers and network servers.

The RTL8139C(L)+ provides optional Boot ROM and MII interfaces, respectively for diskless workstations and extra applications such as Phyceiver and fiber connections. The chip is equipped with an ACPI (Advanced Configuration Power Interface) management function to provide efficient power management for advanced operating systems with OSPM (Operating System Directed Power Management). The RTL8139C(L)+ also provides a remote wake-up function by Magic Packet & Wake-up Frame to increase cost-efficiency in network maintenance and management. It supports the Cardbus interface for PC Card applications and is also an ideal solution for notebook/motherboard-embedded network design as well as for NIC card design.

Features

- 128-pin QFP/LQFP (pin-to-pin compatible to RTL8139C(L))
- Supports PCI/Mini-PCI/Cardbus Interfaces
- Integrates Fast Ethernet MAC, physical chip and transceiver into one single chip
- 10 Mb/s and 100 Mb/s operations
- Supports 10 Mb/s and 100 Mb/s N-way auto-negotiation operation
- Supports descriptor-based buffer management
- Supports MicrosoftR NDIS5 Checksum Offloads (IP, TCP, UDP) and Large Send Offload
- Supports IEEE802.1Q VLAN tagging
- Supports Transmit (Tx) Priority Queue for QoS, CoS applications
- Compliant to PCI Revision 2.2 standard, PC99/PC2001
- Supports PCI Memory Read Line, Memory Read Multiple, Memory Write and Invalidate, and Dual Address Cycle
- Provides PCI bus master data transfer
- Provides PCI memory space or I/O space mapped data transfer
- Supports ACPI power management
- Advanced power saving mode when LAN function or wakeup function is not used
- Supports Link Change, Microsoft "Wake-up Frame" and AMD "Magic Packet" for Wake-On-LAN function
- Supports auxiliary power auto-detection
- Half/Full-duplex capability
- Supports Full-duplex Flow Control (IEEE 802.3x)
- Provides interface to 93C46/93C56 EEPROM to store resource configuration and ID parameters
- Supports either MII or Boot ROM interface, but only one interface can be implemented at a time
- Supports up to 128K-byte Flash Memory/Boot ROM interface
- Supports LED pins for network activity indications
- Supports 25MHz Crystal/25M OSC to reduce BOM cost
- 3.3V CMOS process

Applications

- PCI NIC cards
- Mini-PCI modules
- Cardbus PC cards
- LOM (LAN on motherboards) and LON (LAN on notebooks) applications