RadiSys® R400EX

High-Integration Intel486 System Controller

Complete, Long-Life, PC-Compatible Intel486 System Controller

System Overview

The RadiSys R400EX High-Integration Intel486* System Controller is a member of the RadiSys family of long-life em-bedded core logic. Designed specifically to support Intel486 processors, the R400EX is a true third-generation embedded chip set that addresses the functional needs of embedded app-lications, as well as their requirement for a long product life. The R400EX incorporates features needed for a PC-compatible embedded system design and provides a simple, low-cost, seamless interface to additional chips such as video controllers or PCMCIA controllers. RadiSys is committed to long-term support for the R400EX.

The functional design of the R400EX is based on PC architecture. The DRAM controller is compatible with both Fast-Page-Mode (FPM) and Extended-Data-Out (EDO) DRAM. The keyboard/mouse controller and real-time clock are PC-compatible. The enhanced IDE interface supports a maximum transfer rate of 7.33MB per second.

The ISAbus controller has a separate data bus, and manages the ISA signals to ensure a quiet bus for cycles not directed to the ISA address space.

Feature Summary

- Supports Intel486 CPUs including ULP486 SX
- EDO/FPM DRAM controller supports from 1MB to 128MB
- Supports L1 write-back cache
- Two integrated 16550-compatible UARTs
- Integrated real-time clock
- Enhanced IDE interface or DRAM parity support
- Keyboard and mouse controller
- Power management
- SMI support
- 5V or 3.3V operation
- Complete PC-engine logic
- Supports seven PC-compatible DMA channels
- Supports fifteen PC-compatible ISAbus interrupts
- Integrated 8254-compatible timer/counter
- Supports local bus and ISAbus peripherals
- Four programmable I/O chip selects
- ROM or flash ROM interface
- BIOS shadowing
- Speaker interface
- 208-pin PQFP
- Watchdog Timer

The power-management capabilities of the R400EX include clock-source switching, halt detection, SMI event generation, and a programmable clock-restart delay. The processor clock source can be switched between the CLK2OSC input and the 32.768kHz real-time clock oscillator to reduce power consumption.

The RadiSys world-wide web site features a PC-compatible reference design that is a good starting point for systems using the R400EX.

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I. Technical Overview

The RadiSys R400EX is a basic companion chip for the 486 that performs many of the accompanying functions necessary in a PC-compatible embedded system design.

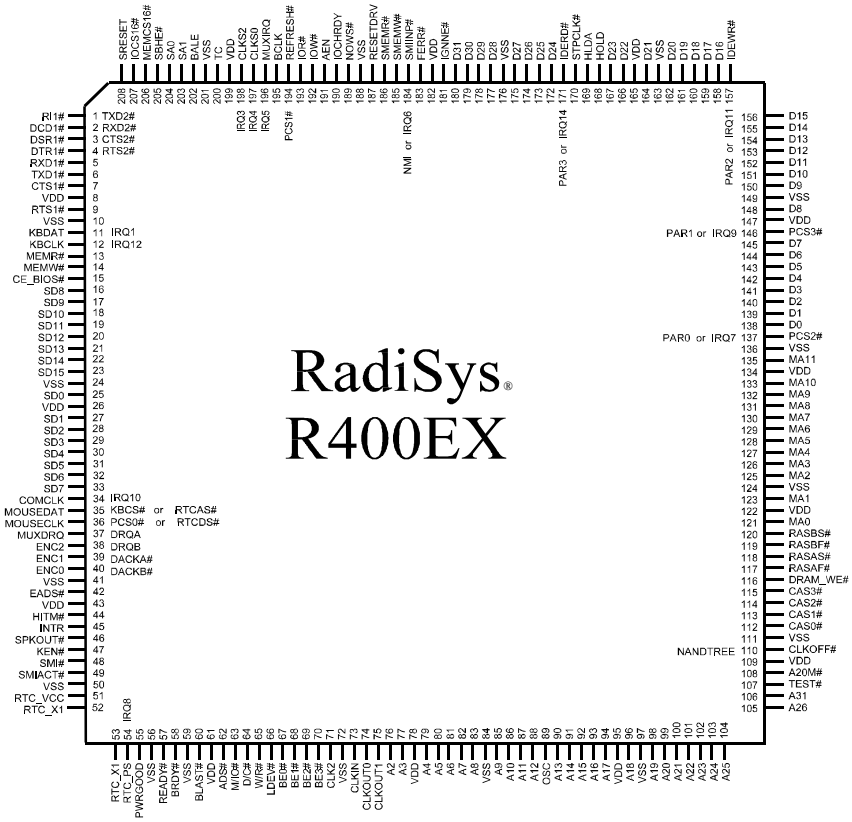
The major objectives of the R400EX are flexibility (of different system designs), ease of use (simplicity of system design), and low system cost.

The RadiSys Advantage

The RadiSys R400EX is a fully-featured system controller tailored for embedded applications using a 486 class processor.

As a company, RadiSys is committed to the long-term support of the R400EX. Unlike designing with short-lived parts from the PC chipset commodity market, this RadiSys commitment makes designing with the R400EX a safe choice.

R400EX PINOUT



Note: The primary pin functions are named on the outside and the alternate pin functions are named on the inside.

SYSTEM INTEGRATION

The R400EX doesn't attempt to incorporate every feature needed in every design; instead, its philosophy is to incorporate directly the features needed in most or all designs, and then provide simple, low-cost, "glueless" interfaces to additional chips for functions that may or may not be needed, such as for a full PC keyboard, a video controller, or a PCMCIA controller.

To maximize the functionality incorporated into the R400EX, pin multiplexing has been used; however, this has been done carefully to insure that almost all functions can be obtained in parallel by the incremental addition of a few small "glue chips."

To obtain the maximum functionality, a total of 3 external 16-pin SOICs must be added, at a cost of less than one dollar.

In general, system designs that meet the following requirements need no extra external glue chips:

1. Those with two or fewer ISAbus DMA channels needed (may be any DMA channels desired); support for all DMA channels can be added with two 16-pin glue chips
2. Those where byte parity on the DRAM is not needed
3. Those where an integrated Enhanced IDE controller is not needed

System designs of type 2 and 3 require the addition of only a single 16-pin glue chip (‘151 or ‘251).

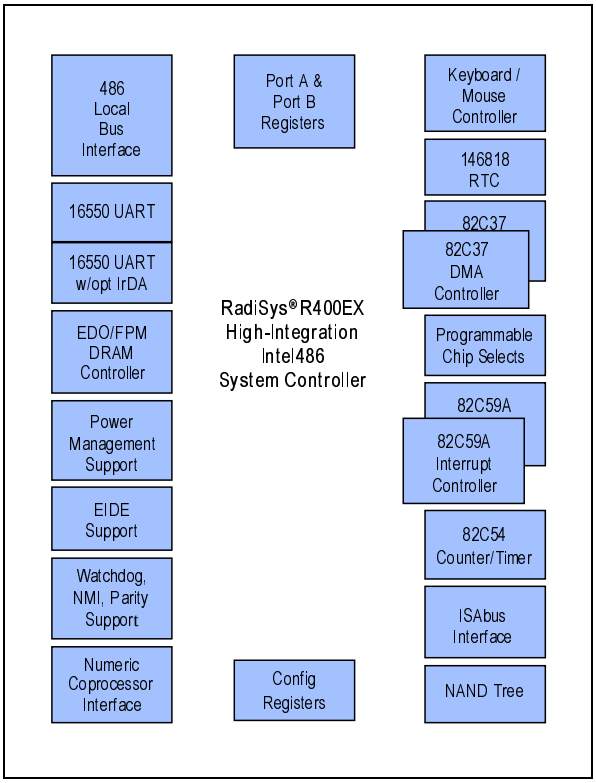


Figure 1.1: R400EX Features

R400EX REFERENCE DESIGN

RadiSys can make available upon request a set of preliminary reference design schematics for the R400EX.

> *Note: This design has not been built or tested. RadiSys assumes no responsibility for any errors that may appear in the design and reserves the right to modify the reference design without notice.*

FEATURES INCLUDED IN THE R400EX

- Support for 486 SX (including HB32), DX2, DX4 (50MHz highest local bus speed -5V only)
- 5V or 3.3V operation
- Support for L1 write-back cache
- ISAbus support (no PCI)
- EDO DRAM support, four RAS#, four CAS#, twelve multiplexed address spaces (1MB–128MB of DRAM support)
- Shadow BIOS in DRAM
- Local bus (to support VGA/SCSI chips)
- Standard PC support in the form of an integrated 82C206 (146818, 8254, 8259, 8237, 74LS612):
  - Real-time clock
  - Timer/counters
  - Interrupt control
  - DMA control
  - Address mapping
- Two 16550 UARTs, which can be configured as a single 8-pin port or as two 4-wire ports or as a 6-wire and a 2-wire COM port. Optionally, the 2-wire COM port can be configured to support IrDA modulation and demodulation
- Keyboard controller that supports the standard PC/AT command set
- PS/2 compatible mouse port
- Power-management features tailored to small, battery-powered applications (SMI#, SIMACT#, STPCLK)
- DRAM byte parity support; multiplexed with Enhanced IDE (EIDE) support
- EIDE support; multiplexed with parity support
- Programmable chip select
- Watchdog timer
- BIOS chip select
- Port B (0x61) and Port A (0x92) support
- NAND-tree for ATE testability
- Low-cost 208-pin PQFP

FEATURES NOT INCLUDED IN THE R400EX

Note: The R400EX can be operated at 5V in conjunction with other 5V-tolerant system parts that are operated at 3.3V (like a 5V-tolerant 486). The R380EX can also be operated at 3.3V while other parts in the system are operated at 5V, provided inputs to the R380EX are limited to 3.3V.

- PCI
- Internal ISA address buffers
- L2 cache support
- 486 2x clock input support
- 5V safe inputs when operated at 3.3V. However, the R400EX may be operated at 5V in conjuction with other system parts that are operated at 3.3V and are 5V-tolerant, such as a 5V-tolerant 486. The R400EX may also be operated at 3.3V while other system parts operate at 5V, provided inputs to the R400EX are limited to 3.3V.
- Support for MASTER mode on the ISAbus

486 LOCAL BUS INTERFACE

The R400EX connects directly to the 486(5x86) CPU local bus. The R400EX is involved in all local bus transactions, except when a local bus slave asserts the LDEV signal into the R400EX. When this happens, the R400EX segregates bus transactions into LDEV cycles and bus cycles it handles directly, which include:

- DRAM references
- Internal registers
- ISA/Xbus cycles
- Special cycles (includes Halt/shutdown and cache flush)
- Interrupt Acknowledge
- DMA cycle.

Each of these cycles is listed and described on the following pages.The R400EX also supports other local bus masters. These devices need to acquire the bus using HOLD/HLDA protocol and then emulate the timing and protocol of 486 bus cycles. The R400EX cannot tell the difference between a 486 bus cycle and another local bus master cycle.

LDEV CYCLES

LDEV cycles are controlled primarily by another local bus device operating in a slave mode. These cycles are denoted by another local bus device, like a video controller, asserting LDEV. In this case of a video controler, the local bus device must meet the CPU's ready timing and drive RDY# directly with a 3-state driver. These can be any type of cycle. The R400EX only monitors them; otherwise it ignores them.

DRAM REFERENCES

Access to memory addresses that span the DRAM address range are handled by the R400EX. DRAM is autosized by the BIOS on boot-up. All burst DRAM cycles are terminated with BRDY. Timing depends on the values in the DRAM control registers. All local bus masters that want to access the R400EX's DRAM must emulate 486 bus cycles. In a system with parity, this means the local bus master is responsible for generating and driving even parity for each valid byte during a write.

INTERNAL REGISTERS

The R400EX handles internal register references. Registers should be accessed using 16-bit I/O read or write cycles. These cycles are echoed on the ISAbus. The cycle is terminated with the assertion of RDY#. The timing for internal registers is done using 16-bit ISA I/O timing. Data is undefined for the nonexistent byte, but 8-bit references to these 16-bit registers will terminate correctly.

ISA CYCLES

ISA bus memory cycles are generated for the following kinds of references:

- Not a reference to the DRAM address space
- Not local bus (LDEV# is deasserted)
- Addresses that fall below 16MB (or A31 is set and BIOS_CE is not asserted)

ISA bus I/O cycles are generated for the following kinds of references:

- Not local bus (LDEV# is deasserted)
- Not a special cycle (D/C# = 1)
- Not to R400EX internal registers

ISA bus cycles are always terminated with a RDY#.

HALT OR SPECIAL CYCLES

The R400EX returns RDY# for all of the Halt or special cycle transactions that include Write-Back, First Flush Acknowledge cycles, Flush, Second Flush Acknowledge cycles, Shutdown, and Stop Grant Acknowledge cycles. Optionally, the R400EX can provide other functions in response to Halt, Shutdown, and Stop Grant Acknowledge cycles.

In response to Halt cycles, the R400EX can do any of the following:

1. Only return RDY#
2. Return RDY# and generate an SMI event
3. Return RDY#, issue STPCLK#, and after receiving the Stop Grant bus cycle, switch to the 32KHz clock as the CPU/system clock; place DRAMs into self-refresh mode; after a programmable delay, de-assert STPCLK#

Option 3 allows the system designer to bring the whole system power consumption down to a few milliamps or even less for properly designed systems, but requires the use of self-refresh-capable DRAMs. To achieve the lowest power-consumption, the CPU clock oscillator must be powered down by the OSC_OFF# signal from the R400EX.

Note: While the DRAMs are in the self-refresh mode, no ISAbus REFRESH or other ISA activity will occur.

When option 3 (above) is used, STPCLK#, if enabled, is asserted upon detection of a processor HALT cycle. After detection of a Stop Grant bus cycle, CLKOUT1 and 0 (one of these should be connected to the CPU's CLK input), is switched to 32KHz clock frequency and the DRAM is placed into a self-refresh mode.

While in this state, the R400EX monitors the CPU's INTR and SMI# pin. If one of these pins transitions, OSCOFF# is immediately de-asserted, the CLK2OSC (divided by 2) is muxed to the CLKOUT1 and 0 outputs. After a programmable delay of 1ms to 64ms, STPCLK# is deasserted, placing the CPU back in the Auto Halt Power- Down state where it immediately transitions to the Normal State, due to the detection of an INTR or SMI# pin transitioning.

When returning from this low-power state in a properly designed system, the only state information that needs to be fixed should be the time of day in DOS systems. Correction of the DOS time of day is done by using a status bit HLTS in the Clock Control register. This bit is set when a HALT instruction is detected by the R400EX. The DOS time of day interrupt may check this bit to see if the time of day needs to be reloaded from the RTC. Refer to the Clock/reset control register and the SMI control register definitions for more details.

In response to a Shutdown bus cycle, the R400EX simply initiates a hardware reset. In this case, both CPURESET and RESETDRV pins are driven asserted for a minimum of 16 CLKIN periods.

3.3V/5V OPERATION

A single pin at power-on reset (MA0) is used to determine the switching level on all pins declared as "ttlin" in the pin description table (mostly local and ISAbus pins). For 3.3V operation MA0 should be pulled low with a 10K ohm resistor to set the thresholds of all the input buffers to CMOS levels. If MA0 is pulled high, the R400EX must be operated from a 5V supply and will set the buffers declared as "ttlin" to TTL input levels. When operating at 3.3V, bus speeds up to 33MHz are supported. When operating from 5V, bus speeds up to 50MHz are supported.

INTERRUPT CONTROLLERS

There are two fully compatible 8259A interrupt controllers in the R400EX, providing up to 14 external interrupts. IRQ0 is always connected internally to the 8254's counter 0 output. Optionally, IRQ1, IRQ8, and IRQ10 also can be driven internally from the keyboard controller, the RTC, and the internal watchdog timer, respectively.

DMA AND MEMORY MAPPER

The R400EX contains two fully compatible 8237A DMA controllers that provide up to four 8-bit DMA channels and three 16-bit DMA channels. The integral 74LS612 compatible memory mapper provides the upper 8-bits of the 24-bit DMA address that is sourced during an access. The CPU is held in the HOLD state while the DMA is being serviced. The DMA clock rate, MEMR# pin timing and 8-and 16- bit DMA wait states are controlled by a single control register, the 82C206 configuration register. Another R400EX extension register supports DMA into memory above the 16MB PC/AT address limit.

TIMER/COUNTER

The R400EX contains a fully compatible 8254 that supports three counter/timers. Each counter/timer's clock input is driven by a 1.19MHz clock derived from the OSCIN signal divided by 12. The output of counter 0 drives IRQ0 and is normally used to keep track of the time of day. The output of counter is connected to the SPKOUT and its TMRGATE is driven from a PORTB register bit. Counter 1 is used in older PCs to generate refresh cycles, but in the R400EX, refresh timing is generated independently by the DRAM controller. Thus, counter 1 on the R400EX can be used as a general-purpose timer.

DRAM MEMORY CONTROLLER

The memory controller supports up to two banks (four modules) of memory. Each bank can support upto a 32- (36 with parity) bit wide Fast-Page-Mode (FPM) DRAM or Extended-Data-Out (EDO) DRAM, each of which range from 1MB to 128MB . Within a bank, both the DRAM size and DRAM type (EDO vs. FPM) must be the same if both x32 modules are populated; however, banks may differ from each other in the size of DRAM. All banks must contain either FPM DRAM or EDO DRAM, but cannot contain a mixture of both types. Even byte DRAM parity support is optionally provided by the R400EX. When parity support is enabled, the R400EX relies on the processor to generate parity during processor initiated DRAM writes. The R400EX only generates parity for DMA writes to memory and also checks all DRAM reads for even parity. If a parity error occurs and parity checking and NMI are enabled, then NMI is signaled to the processor. To enable access to the R400EX's parity pins, an external multiplexer is required to support the IRQ pins that are displaced by the parity function.

Bank A's first memory module always begins at address 0. The second memory module of a bank always contiguously follows the first.

Caution: Make sure to initialize the whole DRAM before enabling parity checking.

The R400EX allows the DRAM to be put into a mode that supports software detection of the type of DRAM (EDO or FPM) installed in each bank, without requiring presence detect or other external hardware means. The only extra system hardware required to support this is a single pull-up resistor on DRAM data bit 0. To conserve power in the HALT and IDLE modes, the system designer should either add pull-ups to the CPU's address and data bus or use a CPU that includes bus keepers. By using the appropriate EDO memories, burst memory read timings of 3-1-1-1 can be supported for bus speeds up to 33MHz.

The R400EX always asserts all four CASx# lines on a DRAM read. Thus, when parity checking is enabled, the R400EX will check parity on all four byte lanes on all DRAM reads, even if the read only requires one or two bytes to be returned.

REAL-TIME CLOCK

The R400EX contains an integrated real-time clock, providing the PC function of the date/time clock, alarm, programmable periodic interrupt, 114 bytes of additional battery backed CMOS RAM, I/O registers 070h and 071h, and crystal and battery input.

Note: The RTCAS and RTCDS pins transition in a "Motorola" fashion to save an R400EX interface pin, so when interfacing to an external 146818 style of RTC, the RTC's MOT (Motorola/Intel#) pin should be tied to Motorola mode.

The RTC has pins for the battery source (RTCVCC and RCTGND), a reset signal for the CMOS RAM (RTCRES#), two crystal pins (X1, and X2) for a 32.768KHz crystal.

The RTC is integrated into the R400EX because it is part of most PC-compatible embedded designs. However, since some designs have a need to use an external RTC, the ability to completely disable the RTC is provided (by pin strapping). In this case, the R400EX contains glue logic to generate control signals RTCAS and RTCDS for an external RTC chip. RTCAS is asserted for a write access to I/O address 070h. RTCDS is asserted for a read/write access to I/O address 071h.

POWER MANAGEMENT

The R400EX contains some basic support for System Management Mode (SMM) and for system-environment power management. The R400EX allows the system designer to pursue any one or a combination of several different power-conservation strategies, including:

1. setting application or OS level software to issue a HALT instruction to place the system into the low-power mode (described in the Halt/Shutdown section)
2. setting software to write to a CPU clock divider control register to reduce the CPU's/system's clock speed
3. generating a system-management interrupt (SMI) in response to an external event or an interval timer expiring in the R400EX—the SMI routine can then handle powering system peripherals down or entering the hardware-supported HALT state as in strategy 1or reducing the system clock speed as in strategy 2.

The R400EX contains all of the HALT detection logic, SMI generation logic, and glitchless clock switching logic to perform these functions (above). The SMI logic and clock-switching logic are detailed in the following paragraphs.

SMI AND CLOCK-SWITCHING LOGIC

The R400EX contains a single SMI idle latch and timer. The idle timer counts down to zero from one of a few programmable frequencies. The idle timer is reset (to the idle latch value) in one of the following ways:

1. hitting the 0 value in conjunction with the SMI being acknowledged by the CPU (SMIACT# pin is asserted)
2. assertion of an external SMIINP# pin if it is enabled as an ACTIVITY# pin
3. assertion of a programmable chip select (if it is enabled).

The idle timer is 12 bits wide and may be clocked by either a 1024- or a 16-Hertz clock. Both of these clocks are derived from the 32,768-Hertz input clock. When clocked by the 1024-Hertz clock, the idle timer can be set to expire at about 1 millisecond boundaries beginning with 1 millisecond, and going up to a total of 4 seconds. When clocked by the 16-Hertz clock, an idle timer expiration time of up to 256 seconds can be achieved with a 62.5 millisecond granularity. In this case, the smallest idle time that can be set is 62.5 milliseconds.

The R400EX contains an SMI interrupt output pin. Sources for this interrupt in the R400EX are the following:

1. The idle timer hitting the 0 value (if enabled to assert SMI)
2. The assertion of the SMIINP# input pin (if enabled to assert SMI)
3. The detection of a HALT cycle (when enabled)
4. The setting of an SMI register bit to be triggered by software

Status bits also exist to show what source(s) initiated the SMI interrupt. When SMI# is asserted it continues to be asserted until SMIACT# is asserted. If another SMI event occurs while SMIACT# is asserted it is saved in the SMI control/status register and not signaled until SMIACT# is de-asserted, but only if the SMI handling software does not reset the associated SMI status bit before exiting. Thus, if the SMIINP# signal caused the SMI, the external SMIINP# signal must also be
de-asserted before exiting the SMI handler to prevent re-entering the SMI handler immediately due to SMIINP# still being asserted (level sensitive).

The R400EX contains an SMIACT# input pin, which is driven by the corresponding CPU pin to indicate that the CPU is in SMM. The R400EX relies on using the SMBASE relocation feature present in 486-class processors. SMBASE may be located in either the top 256KB of DRAM or in a 128KB region at 0x000A0000-0x000BFFFF. When SMM support is enabled for these regions in the R400EX, these regions of DRAM memory can only be accessed by the processor when the SMIACT# is asserted.

Note: Some 486 CPUs cannot run with the slower CPU clock rates that are supported by the R400EX.

Software can reduce the CPU/system "CLK" clock frequency by writing to two register bits that control the CLKOUT0 and CLKOUT1 signals. The bits allow the input oscillator clock to be divided by 2,8, or 32 (refer to the appropriate register described in this guide). When reset, the clock is automatically divided by 2. Software may subsequently set the two bits to speed up or slow down the clock speed, depending on whether performance or power-conservation is required. Clock-speed changes will be accompanied by a programmable STOPCLK# delay to allow the CPU's PLL to lock to the new frequency before the CPU returns to normal operation.

ROM/FLASH ROM INTERFACE

The ROM/Flash ROM interface supports a variety of ROM/Flash devices placed on the ISAbus. Most PC-compatible implementations use an 8-bit BIOS that is shadowed in DRAM, but 16-bit shadowed and non-shadowed ISAbus Flash devices are supported also.

The registers in the R400EX are specifically aimed at supporting the Intel 28F004BR-T or similar Flash devices. The upper 128KB (which includes a 16KB boot block) is normally used for the BIOS. The lower 384KB can be used for user code (such as a real -ime OS kernel). If user code is not needed, a smaller device like the 28F001BX-T can be used. The BIOS usually consists of at least a 16KB boot block, and a 112KB System BIOS. Once shadowed, the BIOS running in DRAM normally occupies only 64K in the F-page of the low 1MB of memory.

Write protection of the Flash is an important system issue. ROMs, of course, do not need write protection. The R400EX provides write protection through several register bits. There are two independent register bits (BIOSWE, APPWE). The intent is to allow one to protect independently, the system BIOS (BIOS) and the application program (AP). For a given region, the register bit is set to allow writes to the Flash. This allows one to make it possible for manufacturers to update the system BIOS and application programs without corrupting the other parts of the device.

We recommend that bit 10 of the Power-Up option register (sourced from MA10) be used by the BIOS to determine if a forced BIOS Flash update is needed. If

bit 10 is high (external 1K pull-up is jumpered onto MA10), a forced BIOS Flash update is being requested regardless of the state of the code or the CHECKSUM in the BIOS. This is a mechanism used by certain BIOS vendors like Phoenix, which allows an external jumper to determine whether to process a BIOS update. When MA10 is interpreted in this manner, a 10K ohm pull-down must always be installed on MA10 or alternately jumpered onto MA10.

16C550 UARTS

Two 16C550 UARTs can be configured as standard PC-compatible COM1 and COM2 ports. These COM ports share eight pins, allowing: (1) a single, full-COM port interface (8-signal plus ground); (2) dual 4-signal interfaces (Rx, Tx, RTS, CTS); or (3) a two-signal COM2 (Rx, Tx) and a six-signal COM1 (Rx, Tx, RTS, CTS, DSR, DTR).

The two-signal version of the COM2 port can also be configured to support IrDA (IrTX and IrRX) directly. As in a standard PC, COM1 is accessed in the I/O address space at 0x3f8-3ff and signals interupts on IRQ4. COM2 is accessed at 0x2f8-0x2ff and signals interupts on IRQ3. These COM ports can share the IRQ3 and IRQ4 interrupt lines with external COM ports or with other devices that require these IRQ lines.

The COM clock can be configured to be CLK2OSC divided by an even divisor up to 64. Divisor values of 54 and 36 (27 and 18 placed in the divisor register respectively) allow the COM clock to operate at ~1.85MHz clock for CLK2OSC frequencies of 100MHz and 66.6MHz. The COM clock can also be sourced from an external pin when the IRQ10 input is not needed externally.

KEYBOARD/MOUSE CONTROLLER

The R400EX contains a PC/AT-compatible keyboard controller with PS/2-compatible mouse controller extensions. If it is not needed or if an external keyboard is desired, it can be disabled (refer to the sections covering Power-Up options and the Miscellaneous Configuration Register later in this guide). The keyboard and mouse pins can then be used for other functions or an external keyboard can be supported.

The keyboard controller is clocked by BCLK, the ISAbus system clock frequency (also referred to as SYSCLK). Response to keyboard commands is immediate (usually within one BCLK) due to the fact that this function is implemented as a hard-wired state machine internally.

Note: Do not confuse the "Output Port and "Input Port" with the similarly named "Output Buffer" and "Input Buffer."

The keyboard controller responds to the following I/O addresses 0x60 (data) and 0x64 (Command/status). An I/O write to 0x60 will fill the keyboard controller's "Input Buffer." An I/O read from 0x60 will return the contents of the keyboard controller's "Output Buffer."

The keyboard controller contains two other registers called the "Output Port" and "Input Port," which are associated with port pins that connect to other signals inside the R400EX. Commands are issued to the keyboard controller by performing I/O writes to 0x64. The integrated keyboard controller supports the commands listed in Table 1.1. All commands except Fx and D4 are executed in the same bus cycle in which they are issued.

Table 1.1: Keyboard Controller Commands

Command	Function
20	Read Command Byte
21-2F	Read RAM
60	Write Command Byte
61-6F	Write RAM
A7	Disable Mouse
A8	Enable Mouse
A9	Mouse Interface Test
AA	Self Test
AB	Keyboard Interface Test
AD	Disable Keyboard
AE	Enable Keyboard
C0	Read Input Port
D0	Read Output Port
D1	Write Output Port
D4	Transmit to Mouse
E0	Read Test Inputs
Fx	Pulse Output Port

COMMAND DESCRIPTIONS

Read Command Byte(20). A Read Command Byte will place the Command Byte in the Output buffer. An I/O read to an address of 0x60 returns the output buffer contents.

Read RAM (21-2F) The keyboard controller contains one extra byte of RAM beyond the Command byte. Execution of a 0x21 to 0x2F command will cause the contents of this RAM to be dumped into the Output buffer.

Write Command Byte (60). The Write Command Byte places the next data byte written to I/O address 0x60

into the Command Byte. When reset, the Command Byte is set to 70. The byte is shown in Table 1.2.

Table 1.2: Write Command Byte

Bit	Function
0	Enable Key Interrupt
1	Enable Mouse Interrupt
2	System Flag
3	Inhibit Override
4	Disable Keyboard
5	Disable Mouse
6	Enable Scan Code Translation
7	0

Write RAM (61-6F). The internal keyboard controller contains one byte of RAM. A command of 0x21-0x2F will cause this RAM location to be updated by the next I/O write to address 0x60.

Disable Mouse (A7). A Disable Mouse command will clear bit 5 of the Command Byte.

Enable Mouse (A8). An Enable Mouse command will set bit 5 of the Command Byte.

Mouse Interface Test (A9). A Test Mouse Interface command will place a 00 in the Output Buffer. An Interface test will not actually occur.

Self Test (AA). A Self-Test Command will place a 55 in the Output Buffer.

Keyboard Interface Test (AB). A Test Keyboard Interface command will place a 00 in the Output Buffer. An Interface test will not actually occur.

Disable Keyboard (AD). A Disable Keyboard command will set bit 4 of the Command Byte.

Enable Keyboard (AE). A Enable Keyboard command will clear bit 4 of the Command Byte.

Read Input Port (C0). A Read Input Port command will place the contents of the Input Port in the Output Buffer.

Read Output Port (D0). A Read Output Port command will place the contents of the Output Port in the Output Buffer.

Write Output Port (D1). The Write Output Port command will place the next data byte written to I/O 0x60 to the Output Port.

Transmit to Mouse (D4). This command will cause the next byte written to the data port to be sent to the mouse. The execution time of this command will depend upon the mouse.

Read Test Inputs (E0). A Read Test Inputs command will place T0 and T1 in D0 and D1, respectively, of the Output Buffer. Bits D2 - D7 will be 0.

Pulse Output Port (Fx). The Pulse Output Port Command will pulse bits 0–3 of the Output Port low for at least 6 usec. Bits 0–3 of this command determine which bits will be pulsed. A command of FF will execute in the same bus cycle in which it is issued.

GATEA20 AND RESET

Since the D1 command takes place in the same bus cycle in which it is issued, a change in GATEA20 will happen immediately. An Fx command will take from 6.4 to 128us to generate a reset depending on the clock speed. An FF command will take place in the same bus cycle in which it is issued.

KEYBOARD STATUS REGISTER

Table 1.3 below describes the keyboard status register. At reset, the Keyboard Status Register will be set to 00.

Table 1.3: Keyboard Status Register

Bit	Function
0	Output Buffer Full
1	Input Buffer Full
2	System Flag
3	Command/Data
4	Inhibit Switch
5	Mouse Data
6	Time-out
7	0

KEYBOARD AND MOUSE INTERFACE

The keyboard nterface will support a standard AT keyboard. The mouse interface will support a standard PS/2 mouse. The internal port pins are configured as in Table 1.4. At reset, all P2 port bits will be set high.

Table 1.4: Configuration of Internal Port Pins

Signal	Function
P1(0)	Key data
P1(1)	Mouse data
P2(0)	CPURESET
P2(1)	GATEA20
P2(4)	IRQ1
P2(5)	IRQ12

TIMINGS

The keyboard controller clock is driven at the BCLK frequency. The clock speed will determine certain timings as shown in Table 1.5.

Table 1.5: Timings

Timing	BCLK @ 8MHz
Fx Command execution (except FF)	5.1us
Transmission backoff	80us
Transmission time-out	2.5ms

Note: The FF command executes in one bus cycle.

PC SPEAKER INTERFACE

The R400EX contains a speaker output (SPKROUT), that is the logical AND of bit 1 of the port B register and the integral 82C54's OUT2 timer 2 signal.

ISAbus INTERFACE

The ISAbus controller manages a separate data bus and the ISA control signals. It generates cycles on the ISAbus for memory and I/O cycles that are not mapped to devices on the local bus or in the processor or system chip themselves. The controller supports 8- and 16-bit transfers, including translation for 32-bit requests from the CPU to 8-bit or 16-bit ISA devices, and 8-bit requests to 16-bit devices.

The controller also produces the ISA (AT) bus clock. The ISA clock can be the CPU clock divided by 2, 3, or 6.

The R400EX uses the quiet ISA feature. When the R400EX sees an access that is not destined for the ISAbus (a local bus cycle, a non-DMA DRAM cycle, a cycle internal to the R400EX), it does not drive the ISAbus data and control signals. This reduces overall system power consumption.

PC ENGINE LOGIC

The R400EX performs a number of functions in support of a 486-class chip PC hardware architecture.

The R400EX generates the clock signals for the CPU. The R400EX expects a 2x CLK input (CLK2OSC) and generates two low-skew 1x clock outputs (CLKOUT[1:0]. One of the 1x clock outputs needs to drive an input to the R400EX (CLKIN). This clock is used for all timing reference for bus activity in the R400EX.

The R400EX also handles the variety of reset signals and states expected in a PC- compatible system. It has a cold reset (PWRGOOD) input and generates resets for the CPU (SRESET) and the ISAbus (RESETDRV).

The R400EX also contains the PC-compatible register 061h (port B).and register 092h (port A).

PROGRAMMABLE CHIP SELECTS

There are four user-programmable I/O chip selects (CS_USR[3:0]), but only three of these (CS_USR[3:1]) can be made available on the external pins. Each can be programmed and used individually or they can be daisy-chained together to form one extended chip select output that can decode up to four discontiguous regions, or two extended chip selects, each with two discontiguous regions. CS_USR0 can be used to reset the SMI activity timer.

Each chip select has a corresponding single 16-bit mask and compare register (see PCS registers). The upper three bits control whether the chip select is enabled, how it should be decoded (I/O or memory), and whether IOCS16 should be asserted by the chip select.

In the case of an I/O decode, the lower 10 bits are compared against the address bits A[9:2] and SA[1:0] as specified by the MODE bits. On I/O decodes A15 is also always decoded as specified by the mode-control field. Also, address bits A14–A10 must be zero to assert a chip select in I/O mode.

The remaining bits in this register determine whether IOR, IOW are included in the decode and whether the chip select's output is daisy-chained into the next, lower numbered chip select. Local bus memory decodes, A31 and A[26:16] must be compared to the lower 12 bits of the register, and M/IO from the CPU must be asserted.

ENHANCED IDE INTERFACE

The enhanced IDE interface consists of a read and write strobe, IDERD# and IDEWR#, and two chip selects: IDECS1# and IDECS0#. The latter two are actually derived from programmable chip selects, CS_USR3# and CS_USR2#. These pins support an unbuffered interface to an IDE drive when used with a floppy drive. They also support a buffered interface to a newer BIOS as well as EIDE drives with a floppy drive. An older BIOS may require IDECS1# to be set to decode both I/O addresses 0x3F6 and 0x3F7. A buffered IDE that requires both older BIOS support and a floppy drive is not supported directly.

The IDExxx pins are multiplexed with DRAM parity; thus, the R380EX does not support both DRAM parity and an Enhanced IDE interface directly. If DRAM parity is required, an external IDE or EIDE controller can be added easily to the design. The enhanced IDE interface supports both modes 3 and 4 PIO modes of the ATA specification.

IDECS1#, IDECS0#, IDERD# and IDEWR# would normally be connected directly to the IDE connector.

CS_USR2# (IDECS0#) is the primary hard-disk chip select. This chip select is reset to enable I/O address decode of 1F0-1F7h. CS_USR3# (IDECS1#) is the secondary hard-disk chip select. This chip select is reset to enable I/O address decode of 3F6h.

PIO mode 0, 3 and 4 are supported by the interface. The pins IOCS16# and IOCHRDY are used in mode 0 IDE signaling as well.

WATCHDOG TIMER SUPPORT

The watchdog timer can be configured to perform several functions. It can be set to time events (or more accurately, the lack of events) in any duration, from 1ms to 256 seconds.

When the timer/counter reaches zero, a hardware reset or IRQ10 can be signaled depending upon the control bits in watchdog control register.

The timer/counter is reset to the latch value during the following events:

- An ADS# occurs and bus mode is enabled (refer to the Watchdog Control Register)
- Software writes to the idle timer latch
- The counter is at zero

Optionally, the timer can be stopped for the duration of a CPU HALT cycle by another control bit in the watchdog control register.

WRITE-BACK CACHE SUPPORT

In all DMA accesses, after obtaining HLDA, the R400EX first does a snoop cycle (EADS#) with the associated address on the CPU's address bus. If HITM# is asserted on a DRAM read cycle, the R400EX de-asserts HOLD without completing the initial DMA access. After the writeback access occurs, the R400EX re-acquires an HLDA from the CPU and completes the DMA cycle.

II. Signal Descriptions

Table 2.1: Signal Type Abbreviations

Abbreviation	Description
trailing #	The named signal is active low.
cmos in	CMOS level input.
ttl in	The input threshold for these pins is switchable, as a single group, between TTL and CMOS thresholds, by a power-up configuration resistor.
out	CMOS level output. Most outputs can drive a DC load of 8 mA. The ones that can't are labeled 2mA. All outputs, except for NAND_OUT, are actually implemented as bi-directional pins for test purposes.
tristate out	CMOS level output that can become tristated under certain conditions.
cmos io	combined: cmos in out
ttl io	combined: ttl in out
csr	The output buffer has a controlled slew rate. This reduces ground bounce at the expense of an increase in propagation delay.
open drain	Open drain output buffer. Actively drives low; requires an external pull-up resistor.
bus keeper	The pin has a bus keeper circuit that maintains the previous pin state. This uses active CMOS buffers, rather than resistors, to save power. These buffers are very weak and can easily be overdriven.
pull-up	The input has an internal pull-up device.
schmitt	The input has a Schmitt trigger.
ICS	CMOS Schmitt trigger input only.
IC	CMOS level input only.
IOCTx	TTL/CMOS selectable input level buffer, plus an output buffer capable of driving xmA.
IOCTxS	Identical to IOCTx cell, except that the output buffer is slew rate limited.
ICT	TTL/CMOS selectable input only.
IOCx	CMOS level input buffer and xmA output buffer.
IOCxS	Identical to IOCx cell, except that the output buffer is slew-rate limited.
O8S	8mA output only, slew-rate limited.
IDQ	Oscillator input cell.
ODQ	Oscillator output cell.
power	Power pin.

Table 2.2: Clock and Reset Signals

Signal	Type	Description
CLK2OSC	cmos in IC	2x Clock from Oscillator: This is the double-frequency input clock from the system oscillator. This input must be 66MHz for systems that run 33MHz bus cycles. The R400EX divides this input by 2 and outputs it (or a sub-multiple) on CLKOUT[1:0]. Note: *It is extremely important to have a high-quality signal on this input. The clock must be free of excessive overshoot and undershoot and must be monotonic, especially at the CMOS switching threshold of the input buffer (nominally 50% of VCC). Series termination or equivalent design techniques should be employed.*
CLKOUT[1:0]	out IOC16	CPU/1X Output Clocks: These are two low-skew clock outputs that should be used for system clock distribution. These two outputs have low skew between each other when they are terminated to equivalent loads. CLKOUT1 and CLKOUT0 source the same clock waveform except during power-up and when clocks get powered-down when HALT detection is enabled and a HALT is detected by the R400EX. CLKOUT0 is driven low while PWRGOOD is de-asserted to keep PLL-based 486s from locking onto the incorrect frequency when the power-supply voltage is turned on. This means that RESETDRV will be held asserted for more than 1ms after PWRGOOD is asserted to allow the PLL-based 486s to lock onto the correct frequency before reset is de-asserted into the 486. CLKOUT1 continues to switch while PWRGOOD is de-asserted. CLKOUT0 will be driven to ground after a Stop Grant Acknowledge cycle has been executed while the processor is in the HALT state. CLKOUT1 will be switched glitchlessly (and will also ensure that the minimum clock pulse widths are met) to the RTC's clock source (typically 32KHz) after a Stop Grant Acknowledge cycle has been executed with the processor in the HALT state. After an interrupt is detected (SMI# or INTR), both clocks are switched glitchlessly back to the original system clock frequency after observing an oscillator spin-up delay. STPCLK remains asserted for an additional 1ms beyond the spin-up delay to allow the 486's PLL to lock to the system frequency again. In normal operation, the R400EX generates these outputs from CLK2OSC/2 or from a sub-multiple of CLK2OSC/2. Optionally, in standby mode, the R400EX can generate these outputs from the 32.768 KHz clock on RTC_X1.
OSCIN	cmos in IC	14.31818MHz clock input: This clock is divided by 12 to provide a clock to the internal 8254. This input is also used to generate DRAM refresh timing.
CLKIN	cmos in IC	1x Clock Input: This is the primary clock input for the R400EX. It is used to clock the state machines internal to the R400EX. Connect this input to one of the CLKOUT outputs. *Note: It is extremely important to have a high-quality signal on this input. The clock must be free of excessive overshoot and undershoot and must be monotonic, especially about the CMOS input switching threshold (nominally 50% of VCC). Series termination or equivalent design techniques should be employed.*
PWRGOOD	cmos in schmitt ICS	Power Good: The assertion of this input indicates that system power is stable and that normal operation may begin. While PWRGOOD is negated, RESETCPU and RESETDRV are asserted and the internal Real-Time Clock megacell is placed in standby. The R400EX internally latches its power-up configuration from MA[11:0] as PWRGOOD becomes asserted. This input buffer is powered by RTC_VCC and is active even when system power is off.

Table 2.3: CPU/BUS Signals

Signal	Type	
ADS#	cmos io IOCT8S	486 Address Strobe: Connect directly to the corresponding 'x86 output. This indicates that the CPU is driving a valid address and bus cycle definition. This signal is driven by the R400EX during DMA accesses. The R400EX tracks the state of the local bus by monitoring this input at all times.
EADS#	cmos io IOC8	486 External Address Strobe: This ouput is used to force the CPU to perform a cache invalidate on its internal cache. It is driven low during DMA cycles and during T2 of a write-protected memory access from the CPU. This output should be connected directly to the CPU's EADS# pin.
M/IO# D/C# W/R#	cmos io IOCT8S	486 Cycle Type Controls: These signals encode the basic bus transaction type and are hooked directly to the corresponding signals on the CPU. These are driven valid as the ADS# signal is driven asserted. They are encoded as follows: M/IO# D/C# W/R# 0 0 0 interrupt acknowledge 0 0 1 Halt/Special cycle* 0 1 0 I/O data read 0 1 1 I/O data write 1 0 0 memory code read 1 0 1 reserved 1 1 0 memory data read 1 1 1 memory data write * For Halt/Special cycles, the following applies: BE3#-BE0#, A4-A2 0111 000 Writeback 0111 001 First Flush Acknowledge cycle 1101 000 Flush 1101 001 Second Flush Acknowledge cycle 1110 000 Shutdown 1011 000 Halt 1011 100 Stop Grant Acknowledge cycle
BE3-0#	cmos io IOCT8S	486 Byte Enables: These signals determine which data byte lanes are used on an access. During DMA, these become outputs, and they are driven to indicate which data byte lanes are valid.
BLAST#	ttl/cmos in ICT	486 Burst Last: This signal, when asserted by the CPU indicates that the last cycle of a transfer is in progress and that BRDY#, if asserted, will complete the transaction.
BRDY#	cmos io IOCT8	486 Burst Ready: This signal is both monitored and driven active by the R400EX. The R400EX drives it active during DRAM burst read and write cycles to indicate to the processor that data is valid or has been written. This pin is 3-stated during LDEV# cycles.
RDY#	cmos io IOCT8	486 Ready: This signal is both monitored and driven active by the R400EX. The R400EX drives this signal active at the end of a bus cycle destined for DRAM or the ISA bus. It also drives this signal active to terminate the CPU's Halt/Special cycles. This pin is 3-stated during LDEV# cycles.

Table 2.3: CPU/BUS Signals

Signal	Type	
KEN#	cmos io IOC8	486 Cacheable Enable: This signal is driven inactive by the R400EX to indicate to the CPU that current bus transaction is not cacheable. KEN# is 3-stated during LDEV# cycles.
INTR	out IOC8S	486 Interrupt: This is an active high output that is used to signal to the CPU that an interrupt request has been received from the internal 8259s.
LDEV#	ttl/cmos in ICT	Local Device Pin: This input, when asserted, tells the R400EX that the current access on the 486 bus should not be forwarded to the DRAM or ISAbus, but instead will be handled by some other local bus controller/peripheral.
HOLD	cmos io IOC8	486 HOLD Pin: The R400EX drives this pin asserted to gain control of the 486 address and data bus.
HLDA	cmos in ICT	486 HOLD Acknowledge: The R400EX waits for this signal to be asserted by the 486 as acknowledgment that the R400EX has been granted the bus.
HITM#	ttl/cmos in ICT	486 Hit Modified: This pin supports write-back-configured L1 CPU caches. When asserted by the CPU, the R400EX removes itself from the bus (if it is the bus owner) and allows the L1 cache-modified data to be updated into DRAM.
FERR#	ttl/cmos in ICT	486 Floating-Point Error: This signal is driven active by the CPU to indicate that a floating-point error has occurred and causes IRQ13 to be generated.
IGGNE#	cmos io IOC8S	486 Ignore Numeric Error: This signal is driven active by the R400EX during writes to 0xF0, 0xF1, if FERR# is active. It remains asserted until FERR# is driven inactive by the CPU.
A20M#	cmos io IOC8S	486 A20 Mask: This signal should be tied directly to the CPU's A20M# pin. This pin is driven by the R400EX from the OR of its internal keyboard controller's GATEA20 pin with the Port 92 GATE A20 bit. A20M# is also forced inactive when SMIACT# is asserted.
SRESET	cmos io IOC8S	486 Reset CPU Only: This signal should be tied directly to CPU's SRESET pin. This pin is driven by the R400EX from the OR of its internal keyboard controller's RESETCPU pin with the Port 92 Reset CPU bit. This signal is driven active for a minimum of 15 CLKIN periods.
A31, A26-A2	ttl/cmos io IOCT8S	486 Address Lines: These are the CPU's address lines. These lines are driven by the R400EX during DMA accesses and are used as inputs at all other times.
D31-0	ttl/cmos io IOCT8S	486 Data Bus: When an external pull-up is added to D0, this data line may be used by the system designer to determine the type of DRAM (EDO versus FPM)installed in the system automatically.

Table 2.3: CPU/BUS Signals

Signal	Type	
DP3-0	ttl/cmos io IOCT8S	486 Data Parity Bits: Even parity is checked by the R400EX only during all DRAM read cycles (DMA or processor-initiated). These bits are only driven by the R400EX during a DMA memory write. For processor initiated accesses, the processor supplies the parity bits. Multiplexed with: DP0 is multiplexed with CS_USR2# and IRQ7 DP1 is multiplexed with CS_USR3# and IRQ9 DP2 is multiplexed with IDEWR# and IRQ11 DP3 is multiplexed with IDERD# and IRQ14.
NMI	cmos io IOCT8S	486 Non Maskable Interrupt: This is an active high output that is used to signal to the CPU that a parity error has been asserted. Multiplexed with: SMIINP#, IRQ6

Table 2.4: Power-Management Signals

Signal	Type	Description
STPCLK#	cmos io csr IOC8S	Stop Clock: This output is driven active by the R400EX to signal a change in clock frequency to the CPU. The actual clock frequency change occurs after the R400EX sees a Stop Grant Acknowledge bus cycle.
SMI#	cmos io csr IOC8	System Management Interrupt: Connect directly to the corresponding CPU input. This output is asserted whenever any system management event occurs, or when SMIINP# input is asserted and is configured as external SMI# expansion pin.
SMIACT#	cmos in ICT	System Management Interrupt Active: This input is used to acknowledge an SMI# interrupt. When active, it allows access to either the top 256KB of DRAM or the 128KB of DRAMat addresses 0x000A0000-0x000BFFFF. When active, CPU accesses must not be write-back cached. This can be accomplished by tying SMIACT# to the WB/WT# pin of the CPU or by always forcing the CPU to perform write-through accesses.

Table 2.5: DRAM Signals

Signal	Type	Description
RASAF#, RASAS#, RASBF#, RASBS#	cmos out IOC16	Row Address Strobes: These are row address strobes to the DRAM that support up to four modules of DRAM.
CAS3-0#	cmos out IOC12	Column Address Strobes : These are column address strobes to the DRAM. Each CASx# line is associated with its respective data byte line (for example, CAS0# is associated with D7-D0).
MA11-MA0	cmos io IOC08 (MA2-11) IOC12 (MA0-1)	Multiplexed address: These signals drive the address inputs of the DRAM subsystem directly. They are also used at power-on reset to determine the initial configuration of several pins on the R400EX.
WE#	cmos out IOC12	DRAM Write Enable: This signal is asserted by the R400EX during a write to DRAM. It is also asserted at the end of read cycles in case the DRAM type is set to EDO as a way of disabling the DRAM's output buffers.

Table 2.6: ISAbus Interface Signals

Signal	Type	Description
IRQ3-7, IRQ9, 11, IRQ14	ttl/cmos in ICT (see multiplexed function for output buffer strength)	Interrupt Request Lines: These are the asynchronous input to the internal 8259s. Each of these has a dedicated pin, if desired. If DRAM parity, EIDE, IRQ15, or the full set of ISA DMA pin functions are required, these inputs are supplied through an external multiplexer ('151 or '251) and the MUXIRQ pin. Multiplexed with: IRQ3 is muxed with CLKS2 IRQ4 is muxed with CLKS0 IRQ5 is muxed with MUXIRQ IRQ6 is muxed with SMIINP# IRQ7 is muxed with DP0 or CS_USR1# IRQ9 is muxed with DP1 or CS_USR2# IRQ11 is muxed with DP2 or IDEWR# IRQ14 is muxed with DP3 or IDERD#
IRQ10	ttl/cmos in ICT	Interrupt Request Lines: This is an asynchronous input to the internal 8259. This interrupt is available externally, if the internal UARTs derive their clocks from a divided version of the CLKIN input. Multiplexed with: COM_CLK
IRQ12,IRQ1	ttl/cmos in open drain ICT	Interrupt Request Lines: These are asynchronous inputs to the internal 8259s. If the internal keyboard controller is disabled, these two interrupt pins are available. If the internal keyboard controller is enabled, then IRQ1 is supplied from the internal keyboard controller, and IRQ12 is supplied from the mouse-controller function, if it is enabled. Multiplexed with: IRQ12 is muxed with KB_CLK IRQ1 is muxed with KB_DATA

IRQ8#	cmos in IC	Interrupt Request 8: This is an asynchronous input to the internal 8259 when an external RTC is selected. Multiplexed with: RTCPS
MUXIRQ	ttl/cmos in ICT	Multiplexed Interrupt Request: When configured as MUXIRQ, this input pin supplies IRQ3, 4, 5, 6, 7, 9, 11, 14 input information in a time-multiplexed fashion to the internal 8259s. CLKS2, BCLK, and CLKS0 pins feed the MSB to LSB select bits of the multiplexer, respectively. The IRQs should be connected to the external D0-D7 '151 or '251 multiplexer pins in the order specified above (IRQ3 goes to D0, IRQ4 goes to D1, etc). Multiplexed with: IRQ5
DRQA, DRQB	ttl/cmos io ICT (DRQA) IOCT8S (DRQB)	Direct Memory Access Request lines: When configured as discrete DRQ inputs, these two pins can be programmed to any DRQ input desired. The selected DMA request lines are then multiplexed into the internal 8237. If both pins are programmed to assert the same internal DMA request pin, like DRQ2, then the effect will be to internally OR the external DRQA/B pins together (not normally desired). DRQA is paired with DACKA#. DRQB is paired with DACKB#. Multiplexed with: DRQA is muxed with MUXDRQ DRQB is muxed with DACKENC2
DACKA#, DACKB#	ttl/cmos io IOC8S	Direct Memory Access Acknowledge lines: These signals are DACK outputs from an internal 8237. DACKA# is paired with DRQA. DACKB# is paired with DRQB. The actual DACK# mapping is governed by the associated DRQ pin programming. Multiplexed with: DACKA# is muxed with DAKENC1 DACKB# is muxed with DAKENC0
MUXDRQ	ttl/cmos in ICT	Multiplexed Direct Memory Access Request: When configured as MUXDRQ, this input pin supplies DRQ0, DRQ1, DRQ2, DRQ3, IRQ15, DRQ5, DRQ6, DRQ7 input information in a time-multiplexed fashion to the internal 8237s (and 8259 in the case of IRQ15). CLKS2, BCLK, and CLKS0 pins must feed the MSB to LSB select bits of the multiplexer, respectively. The IRQs should be connected to the external D0-D7 '151 or '251 multiplexer pins in the order specified above (DRQ0 goes to D0, DRQ1 goes to D1, etc). Multiplexed with: DRQA
DAKENC2-0	ttl/cmos io IOC8S	DACK Encoded lines: When configured in this manner, these pins support the full complement of DMA channels through the use of an external '138 decoder. DAKEN2, DAKENC1, and DAKENC0 should be connected to the MSB to LSB decode select pins, respectively. In addition, AT.AEN should be used to enable the '138. When connected in this fashion, the DACK#x outputs come from the respective '138 output (DACK0# from D0# of the '138, DACK1# from D1#, etc.). Multiplexed with: DAKENC0 is muxed with DACKB# DAKENC1 is muxed with DACKA# DAKENC2 is muxed with DRQB
TC	cmos io IOC8S	Terminal Count: This signal is asserted by the R400EX when a DMA channel reaches its terminal count.

AEN	out csr IOC8S	Address Enable: This output is asserted during DMA and ISA Refresh cycles. It indicates that the SA outputs are driving a memory address and not an I/O address. (ISA DMA cycles are fly-by and never have an I/O address associated with them). ISA peripherals accessed via I/O instructions must disable their address decode while this output is asserted; otherwise they respond incorrectly to memory addresses when the IOR# or IOW# signal becomes asserted together with MEMR# or MEMW# during a DMA cycle. I/O devices participating in a DMA cycle should select themselves using DACKx# directly from the R400EX (or from the '138 when the R400EX encodes the DACK signals).
BALE	out IOC8	Bus Address Latch Enable: This output is pulsed asserted at the beginning of a normal ISA cycle. It is continuously asserted during DMA cycles. It indicates that a valid address is present on the bus. In a generic ISA system, this signal is used to latch the high-order bits of the address bus. The R400EX keeps all addresses stable for the duration of the ISA cycle, so they don't need to be latched by BALE.
BCLK	out IOC8	Bus Clock: This is the ISAbus clock signal. It is CLKIN divided by 2,3,4, or 6 When divide by 3 is selected, the duty cycle of this output is ~33% high, 66% low. For all other divisors, the output duty cycle is ~50%. Since, generally, the ISAbus is asynchronous, BCLK shouldn't be used to sample inputs or drive outputs. The one exception is NOWS#, which is synchronously sampled by the R400EX. When external multiplexers are used in conjunction with the R400EX to enable EIDE or DRAM parity or full DMA support, the BCLK pin should also be routed to the intermediate select pin of a '151 or '251 type of multiplexer. *Note: The* IBM Technical Reference, Personal Computer AT *refers to this output as CLK in the pin descriptions, but refers to it as SYSCLK in the actual schematics. This document uses the name chosen by Solari in* ISA & EISA Theory & Operation.
IOCHRDY	ttl/cmos in ICT	I/O Channel Ready: On the ISAbus, this input is implemented as open-collector, held asserted by a pull-up resistor. It may be negated by an ISA memory or an I/O device to extend the duration of the current ISA cycle. To extend a cycle, an ISA device must negate IOCHRDY within a specific time after the assertion of MEMR#, MEMW#, IOR#, or IOW#. When the device is ready for the cycle to complete, it must release IOCHRDY and allow the resistor to pull it asserted. Alternatively, to speed up the completion of the cycle, the device can actively drive IOCHRDY asserted and then tristate it. IOCHRDY negated overrides NOWS# asserted. Normal ISA cycles are extended by integral numbers of BCLK cycles. ISA DMA cycles are extended by even numbers of BCLK cycles. The DRAM refresh controller only remembers a single pending refresh, so if IOCHRDY is held negated for too long, ISA and DRAM refresh cycles may be lost.
IOCS16#	ttl/cmos in ICT	I/O Chip Select 16: On the ISAbus, this input is implemented as open-collector, held negated by a pull-up resistor. An ISA bus I/O device that can support 16-bit accesses may assert IOCS16# via a straight decode of SA[9:0] (while SA[9:0] is sufficient in some systems, it is recommended that a decode of SA[15:0] be used) without qualification by any control strobes. This tells the R400EX to perform a 16-bit access to the device if possible. IOCS16# is ignored by the R400EX except during ISA I/O cycles.

IOR#	out IOC8	I/O Read Strobe: This command strobe output instructs an ISA I/O device, if selected, to drive data onto the data bus. An I/O device is selected by an address during an I/O cycle and by a DACKx# during a DMA cycle.
IOW#	out IOC8	I/O Write Strobe: This command strobe output instructs an ISA I/O device, if selected, to accept data from the data bus. An I/O device is selected by an address during an I/O cycle and by a DACKx# during a DMA cycle.
MEMCS16#	ttl/cmos in ICT	Memory Chip Select 16: On the ISAbus, this input is implemented as open-collector, held negated by a pull-up resistor. An ISAbus memory device that can support 16-bit accesses may assert MEMCS16# via a straight decode of SA[23:0] without qualification by any control strobes. This tells the R400EX to perform a 16-bit access to the device if possible. MEMCS16# is ignored by the R400EX except during ISA memory cycles. In a generic ISAbus, SA[16:0] don't have the proper timing to allow them to participate in decoding MEMCS16#. The R400EX drives all SA lines with the same timing, so all twenty-four may be used. Or, for backward compatibility with generic ISA, the decode may be limited to using SA[23:17].
MEMR#	out IOC8	Memory Read Strobe: This command-strobe output instructs an ISA memory device, if selected, to drive data onto the data bus. A memory device is always selected by an address, never by a DACKx#. This output is asserted together with REFRESH# during an ISA refresh cycle.
MEMW#	out IOC8	Memory Write Strobe: This command strobe output instructs an ISA memory device, if selected, to accept data from the data bus. A memory device is always selected by an address, never by a DACKx#.
NOWS#	ttl/cmos in ICT	No Wait State: On the ISAbus, this input is implemented as open-collector, held negated by a pull-up resistor. Unlike all other inputs from the ISA bus, NOWS# is synchronous. It must meet specified setup and hold times to BCLK. The sampling point varies with the cycle type. Solari, *ISA & EISA Theory & Operation,* should be consulted to understand the subtleties of designing with this signal. IOCHRDY negated overrides NOWS# asserted. NOWS# is sampled only in memory and I/O cycles and is ignored during DMA and refresh cycles. *Note:* The IBM Technical Reference, Personal Computer AT *refers to this pin as 0WS. This document uses the name chosen by Solari in* ISA & EISA Theory & Operation*. An alternate name used interchangeably by Solari is SRDY#.*
REFRESH#	out csr IOC8S	Refresh: This output indicates that the current ISA cycle is a refresh cycle. Since ISA refresh is rarely used, it may be disabled by setting a register bit. *Note: The R400EX does not support add-on bus owners (Master Mode DMA), so contrary to the ISA specifications, this output is totem pole, not open collector.* Multiplexed with: CS_USR3
RESETDRV	out csr IOC8S	Reset Drive: This output indicates an ISAbus reset. It can also be used to drive the RESET input into the CPU. RESETDRV is guaranteed to be asserted for at least 10 BCLK cycles. *Note: Solari in* ISA & EISA Theory & Operation *refers to this output as RESET. To avoid confusion with any other reset signals in the system, this document uses the name specified in the* IBM Technical Reference, Personal Computer AT.

SA[1:0]	out csr IOC16S	System Address: These two outputs, together with AEN and SBHE# and an external CPU address bus latch/buffer, provide either a memory address or an I/O address for the ISAbus. The R400EX converts the BE3-0# inputs from the 486 into the ISAbus SA1 and SA0 outputs. Generally, there is no way of knowing in advance whether the ISA cycle will be to memory or to I/O until one of the command strobes becomes asserted. Each ISA device must wait for a command strobe before acting on the address. IOCS16# and MEMCS16# are exceptions. The device must generate them by decoding SA in advance of a command strobe. The x86 architecture supports 16 I/O address lines, and any or all of SA[15:0] may be used to generate IOCS16#. However, the ISAbus generally uses only SA[9:0] to decode I/O addresses. *Note: A generic ISA bus has two types of addresses: SA[19:0] are stable throughout a transfer, and LA[23:16] may change before a transfer completes. BALE is used in a generic ISAbus to latch the LA signals before they change. In an R400EX design, all twenty-four addresses are stable throughout an entire ISA cycle, so there is no need to latch them.*
SBHE#	out csr IOC8S	System Byte High Enable: This output indicates a transfer of data on SD[15:8], the upper byte of the ISAdata bus. Sixteen-bit devices use SBHE# to condition their upper data bus buffers.
SD[15:0]	ttl/cmos io csr IOCT8S	System Data: These signals make up the ISA data bus. The R400EX links the ISA data bus to the CPU data bus. Eight-bit devices always use SD[7:0] only, regardless of whether they are at an odd or an even address. Sixteen-bit devices use SD[15:0], at an even address only, and must inform the R400EX of their capability by asserting either IOCS16# or MEMCS16#.
SMEMR#	out IOC8	Small Memory Read Strobe: This command-strobe output has the identical function and timing as MEMR#, except that it is further qualified by being asserted only in the lowest megabyte of ISA memory address space (SA[23:20] == 0).
SMEMW#	out IOC8	Small Memory Write Strobe: This command-strobe output has the identical function and timing as MEMW#, except that it is further qualified by being asserted only in the lowest megabyte of ISA memory address space (SA[23:20] == 0).

Table 2.7: Real Time Clock Interface Signals

Signal	Type	Description
RTC_VCC	power	Real-Time Clock VCC: This provides power only to the internal Real-Time Clock megacell, its associated battery-backed CMOS RAM, and a few associated input and output buffers. If using the internal RTC, connect this pin to a power-management circuit that switches between system VCC and a backup battery. If not using the internal RTC, connect this pin directly to the system VCC plane.
RTC_X1	cmos in IDQ	Crystal input: This is the input side of the 32.768 KHz crystal oscillator for the internal Real Time Clock megacell. This input must be grounded when supplying an external clock to RTC_X2. This input buffer is powered by RTC_VCC and is active even when the system power is off. *Caution: Pay careful attention to how RTC_X1 and RTC_X2 are connected. This arrangement is somewhat different than other oscillator circuits.*
RTC_X2	cmos io drives crystal only ODQ	Crystal input/output: This is the output side of the 32.768 KHz crystal oscillator for the internal Real-Time Clock megacell. This output should be connected only to a crystal, since it doesn't have the ability to drive other loads. To use the internal oscillator, connect a parallel resonant crystal between RTC_X1 and RTC_X2. To supply an external 32.768 KHz clock, ground RTC_X1 and use RTC_X2 as the clock input. The R400EX needs a 32.768 KHz clock even if using an external RTC chip. The clock is needed for DRAM refresh, as the source of CLK2OUT when the 486 is in stop clock mode, and as the clock for the SMI timer. This output buffer is powered by RTC_VCC and is active even when system power is off. *Caution: Pay careful attention to how RTC_X1 and RTC_X2 are hooked up. This arrangement is somewhat different than other oscillator circuits.*
RTC_PS	cmos in IC	Real-Time Clock Power Sense: This input, when negated, clears the VRT bit in Register D of the internal Real-Time Clock megacell. This indicates that RTC battery power has failed, and that the RTC no longer has valid RAM or time. This pin is also used in conjunction with the TEST# pin to enable the NANDTREE function. When both the TEST# pin is low (asserted) and RTC_PS is low, all outputs float (except NANDOUT) and the NANDTREE testing is enabled. This input buffer is powered by RTC_VCC and is active even when system power is off. Multiplexed with: IRQ8#

Table 2.8: Keyboard Interface Signals

Signal	Type	Description
CS_KB#	out IOCS8	Keyboard Controller Chip Select: This pin is the chip-select output for an external keyboard controller. This function is only enabled if the internal keyboard controller is *disabled* and the internal RTC is *enabled*. Multiplexed with: MO_DATA and RTC_AS
KB_CLK	cmos io csr open drain schmitt IOCT8S	Keyboard Clock: This bi-directional open-drain signal implements the IBM PS/2 protocol for the keyboard clock. *Note: This I/O cell is not open drain.* Multiplexed with: IRQ12
KB_DATA	cmos io csr open drain schmitt IOCT8S	Keyboard Data: This bi-directional open-drain signal implements the IBM PS/2 protocol for keyboard data. *Note: This I/O cell is not open drain.* Multiplexed with: IRQ1
MO_CLK	cmos io csr open drain schmitt IOCS8S	Mouse Clock: This bi-directional open drain signal implements the IBM PS/2 protocol for the mouse clock. *Note: This I/O cell is not open drain, but simulates an open drain by running the mouse clk output into both the 3-state enable and grounding the input of the output buffer.* Multiplexed with: RTC_DS and CS_USR0#
MO_DATA	cmos io csr open drain schmitt IOCS8S	Mouse Data: This bi-directional open drain signal implements the IBM PS/2 protocol for mouse data. *Note: This I/O cell is not open drain.* Multiplexed with: RTC_AS and CS_KB#

Table 2.9: Comm Port Interface Signals

Signal	Type	Description
RXD1#	ttl in csr ICT	Receive Data: The receiver uses this pin to shift serial data out. Data is transmitted least significant bit first.
TXD1#	ttl io csr IOCT8S	Transmit data: The transmitter uses this pin to shift serial data out. Data is transmitted least significant bit first.
CTS1#	ttl in csr ICT	Clear to Send: This indicates that the modem or data set is ready to exchange data with UART.
RTS1#	ttl io csr IOCT8S	Request To Send: This indicates to the modem or data set that the UART is ready to exchange data.
DCD1#	ttl in csr ICT	Data Carrier Detect: This indicates that modem or data set is ready to establish the communications link with the UART. Multiplexed with: RXD2# and IrRX
RI1#	ttl io csr IOCT8S	Ring Indicator: This indicates that the modem or data set has detected a telephone ringing signal. This is an input only signal when the pin is configured in this mode. Multiplexed with: TXD2# and IrTX
DSR1#	ttl in csr ICT	Data Set Ready: This ndicates that the modem or data set is ready to establish the communications link with the UART. Multiplexed with: CTS2#
DTR1#	ttl in csr ICT	Data Terminal Ready: This indicates to the modem or data set that the UART channel is ready to establish a communications link. Multiplexed with: RTS2#
RXD2#	ttl in csr ICT	Receive Data: The receiver uses this pin to shift serial data out. Data is transmitted least significant bit first. Multiplexed with: DCD1# and IrRX
IrTX	ttl io csr IOCT8S	Transmit data: This pin transmits the infrared modulated version of a serial bit stream. The R400EX modulates the serial output connection of the internal 16C550 and outputs this to the pin. Data is transmitted least significant bit first. Multiplexed with: RI1# and TXD2#
CTS2#	ttl in csr ICT	Clear to Send: This indicates that the modem or data set is ready to exchange data with UART. Multiplexed with: DSR1#
RTS2#	ttl io csr IOCT8S	Request To Send: This indicates to the modem or data set that the UART is ready to exchange data. Multiplexed with: DTR1#

COMCLK	cmos/ttl in ICT	Communications Clock: If selected as the UART clock source, this input should be driven with the desired frequency (usually 1.843 MHz for PC- compatibility). Multiplexed with: IRQ10

Table 2.10: Miscellaneous Signals

Signal	Type	Description
CE_BIOS#	out csr IOC8S	BIOS Chip Enable: This output is the chip select for the system BIOS. Typically, it is connected to the CE# input of the BIOS chip. The BIOS resides on the ISAbus and can be "shadowed" into DRAM. The R400EX may be configured for the range of addresses for which it will assert CE_BIOS#.
NANDOUT/ OSCOFF#	out csr O8S	NAND Chain Out: If TEST# and RTC_PS pins are both low, this pin is the output of the NAND chain that connects all other package pins, except for power pins, ground pins, the TEST# pin, and the RTC pins that are powered by RTC_VCC. If either TEST# or RTC_PS is high (normal system mode), this pin becomes an output that, when asserted, indicates that the R400EX has entered a low power standby mode. In this mode, this pin may be used to powerdown the system's clocks (except the RTC clock). This allows the system to get to a very low power state.
TEST#	cmos in weak pull-up IC PU	Test mode: When asserted, this input places the R400EX into a test mode. If RTCPS is held low while TEST# is asserted (held low). All output and i/o pins are tri-stated, and the internal NAND chain is enabled connecting all pins except power and ground. This allows ATE testing of the R400EX. If RTCPS is held high while TEST# is asserted, other test modes are invoked. The output of the NAND chain is NANDOUT.
SPKR_OUT	out csr IOC8S	Speaker Out: This output is bit 1 of the R400EX PortB register ANDed with the TMROUT2 input from 8254 timer 2. The AND is an enable function defined by the AT architecture.
SMIINP#	ttl in ICT	SMIINP#: When asserted, this pin either causes the R400EX to assert an SMI interrupt, or it resets the SMI activity timer to its starting value. The exact function is defined by a bit in the SMI control register. When configured to assert the SMI# pin, any assertion pulse greater than 10ns will be asynchronously latched internally. SMI-handling software must clear both the external SMIINP# (level sensitive) source and the status bit associated with the SMIINP# to prevent re-entering the SMI handler. Multiplexed with: IRQ6 and NMI
IDE_RD#	out csr IOCT8S	IDE I/O Read Strobe: When not using IDE PIO mode 3/4, this output is identical to the IOR# output for accesses that fall into IDE address domain. It is never asserted for accesses outside of the IDE address range. In IDE PIO mode 3, this output switches much more quickly than it would for a standard ISA I/O read cycle; thus, the IOR# pin stays disabled for PIO mode 3 accesses. This allows much faster transfer rates between the IDE device than would otherwise be possible. This pin can be tied directly to the direction pin of a '245 type of data buffer to control a buffered data path to an IDE/EIDE drive. Multiplexed with: DP3
IDE_WR#	out csr IOCT8S	IDE I/O Write Strobe: When not using IDE PIO mode 3/4, this output is identical to the IOW# output. In IDE PIO mode 3, this output switches much more quickly than it would for a standard ISA I/O write cycle. This allows much faster transfer rates between the IDE device than would otherwise be possible. Multiplexed with: DP2

Table 2.10: Miscellaneous Signals

Signal	Type	Description
CS_USR[3:0]#	out csr IOC8S	User-Programmable Chip Selects: These outputs are programmable chip selects for memory or I/O devices. Each output is asserted based on a decode of a variable size memory or I/O address. All chip selects are initialized to 0 (chip select disabled). When I/O decode mode is selected, each decode, optionally, may be qualified by being ANDed with IOR# or IOW# or both. In addition, each decode may also optionally assert IOCS16#. This assertion of IOCS16# is only internal, and is not driven out on the IOCS16# pin. This allows either 8-bit or 16-bit I/O devices to be selected. Also, CS_USR(n+1) may be OR'ed into CS_USR(n). Finally, CS_USR0#, although not available as a pin, can be internally connected as an input that restarts the internal SMI activity timer. Multiplexed with: CS_USR0# is multiplexed with MO_CLK and RTC_DS CS_USR1# is multiplexed with REFRESH# CS_USR2# is multiplexed with IRQ7 and DP0 CS_USR3# is multiplexed with IRQ9 and DP1
RTC_AS	cmos io csr open drain schmitt ICS8S	Real-Time Clock Address Strobe: This signal is used to latch the address for an external Real- Time Clock. This signal is asserted during I/O byte writes to address 0x70. Multiplexed with: MO_DATA and CS_KB#
RTC_DS	cmos io csr open drain schmitt ICS8S	Real-Time Clock Data Strobe: This signal is used to latch the data for an external Real-Time Clock. This signal is asserted during I/O byte read/writes to address 0x71. Multiplexed with: MO_CLK and CS_USR0#
CLKS2, CLKS0	out csr IOCT8S	User-Programmable Chip Selects: These pins are configured as clock outputs whenever the R400EX is configured to support EIDE, DRAM parity, or the full complement of DMA support through the use of external multiplexers. CLKS2 should be connected to the multiplexer's most significant select line, and CLKS0 should be connected to the multiplexer's least significant select line. Multiplexed with: CLKS2 is multiplexed with IRQ3 CLKS0 is multiplexed with IRQ5

III. Power-Up Configuration Options

The R400EX is highly configurable. While PWRGOOD is negated, the MA pins are configuration inputs that select various operating modes. By reading the Power-Up Options register, software can also determine how the board is configured at Power-Up. Once operating, additional modes are selected through the use of miscellaneous configuration register bits.

None of the MA pins have internal pull-up or pull-down resistors. Therefore, external configuration resistors are required for all pins. When the R400EX is in low-power standby, it re-drives all the pins with the values latched at the assertion of PWRGOOD. This reduces standby power consumption by eliminating DC current through the resistors. Table 3.1 describes the Power-Up configuration options.

Table 3.1: Power-Up Configuration Options

Signal	State	Description
MA0		R400EX operating voltage.
	0	3.0 or 3.3 volt VCC operation; 'ttl in' pins have CMOS input thresholds.
	1	5.0 volt VCC operation; 'ttl in' pins have TTL input thresholds.
MA1		Internal real-time clock megacell; this bit is also written into bit 3 (EXRTC bit) of the 0utput register at power-up.
	0	Enabled.
	1	Disabled; mouse pins are enabled when the internal keyboard/mouse controller is enabled. CS_KB# and CS_USR0# are enabled to the RTC_AS/MO_DATA and the RTC_DS/MO_CLK pins, respectively, when the internal keyboard is also disabled.
MA2		Internal keyboard and mouse controller megacell.
	0	Enabled.
	1	Disabled.
MA3		Select between 8-bit or 16-bit BIOS on the ISAbus
	0	8-bit BIOS is on the ISAbus.
	1	16-bit BIOS is on the ISAbus.
MA4		Select between full- or two-channel DMA support.
	0	Two-channel DMA support only; the four DMA pins are configured as DRQA, DRQB, DACKA#, and DACKB#.
	1	Seven-channel support; the four DMA pins are configured as MUXDRQ, DAKENC2-0. This also disables the IRQ3 and IRQ4 pins and enables CLKS2 and CLKS0.
MA5		Select between EIDE/DRAM parity or demultiplexed IRQ support.
	0	Demultiplexed IRQ support; IRQ3 and IRQ4 (unless MA4 is set) and IRQ5, 6, 7, 9, 11, and 14 are directly connected to the R400EX.
	1	EIDE/DRAM parity support; the MUXIRQ, CLKS2, BCLK, and CLKS0 pins are used to input all IRQ inputs through the use of the external multiplexer. The IRQ5, 6, 7, 9, 11, and 14 pins are redefined to perform either EIDE or DRAM parity support.
MA6		Select between EIDE or DRAM parity functions. This bit is ignored if MA5=0.
	0	EIDE support.
	1	DRAM parity support.

Table 3.1: Power-Up Configuration Options

Signal	State	Description
MA7		Select between REFRESH# and CS_USR1# pin functions.
	0	REFRESH#.
	1	CS_USR1#.
MA8		COM port pin partitioning.
	0	Enable COM1 to all 8 pins.
	1	Enable 6-pin COM1 and 2-pin COM2 ports. This setting should also be used for 4/4 pin COM1/COM2 pin partitioning and the 6-pin COM1 and 2-pin IrDA-compatible COM2 partitioning. However, the COMCLK control register must be updated after Power-Up and before using the COM port pins when the latter two pin partitioning options are needed.
MA9		Enable COMCLK.
	0	IRQ10 input enabled.
	1	COMCLK input is enabled.
MA11, MA10		These can be user-definable bits; however, many times a BIOS will interpret MA10 set as a force BIOS update function, and MA11 set as a condition to cause a manufacturing loop test to be executed. These bits are sampled with reset and are available for software to read from the Power-Up option register.

IV. Register Descriptions

There are two types of internal registers in the R400EX:

1. PC-Compatible Registers. These registers are defined by the PC architecture and are addressable at standard I/O addresses. This includes the RTC registers, the keyboard controller registers, PortA and the PortB registers, the 8259 registers, the 8254 registers, the 8237 registers, and the 74LS612 DMA page registers.

   Table 4.1 lists all of the fixed I/O addresses that are decoded internally by the R400EX. (For more information on the 8259A, 8237A, and 8254 megafunctions, refer to their respective *Data Guides*.)

2. R400EX-Specific Registers. These registers are referenced with an index and data register. There are two sets of these registers. The first set configures the internal 82C206 and the second set configures the remainder of the R400EX. All defined registers (PortB, 0x60, 0x64, 0x70, 0x71, 0x92,) and I/O chip-select decodes (IDE strobes, KB_CS, etc.) use full 16-bit I/O address decoding to prevent aliasing.

For descriptions of the R400EX's registers, refer to the following pages.

Table 4.1: Fixed I/O Addresses Decoded Internally by the R400EX

I/O address (hex)	Register(s)
000-00F	DMA controller 1 - 8237A
020-021	Master 8259A
022-023	Internal 82C206 configuration register: index and data
024-025	R400EX index register
026-027	R400EX data register
040-043	8254A timer/counter
060/064	Keyboard controller data and control registers
061	PortB
070-071	146818 RTC - NMI mask
080-08F	74LS612 style DMA page registers
092	PortA
0A0-0A1	Slave 8259A
0C0-0DF	DMA controller 2 - 8237A
0F0	Clear math co-processor busy
0F1	Reset match co-processor
2F8-2FF	COM2 registers
3F8-3FF	COM1 registers

82C206 INDEX/DATA REGISTER

The internal 82C206 has only one configuration register that resides at an index value of 0x01.

Any value, other than a 0x01, written to the 82C206 index register disable reads and writes to the single 82C206 Configuration Data register that is accessed through I/O address 0x23.

The Index value at port 0x22 is write-only. Also, a write to 0x23 will disable subsequent accesses (read or write) to the 82C206 Configuration Data register. To re-enable access to the 82C206 Configuration Data register, the Index register at 0x22 must again be written to a value of 0x01.

7	6	5	4	3	2	1	0	Adr
Index								022
Data								023

Figure 4.1: 82C206 Index/Data Register

82C206 CONFIGURATION DATA REGISTER

The IOWS, DMA16WS, and DMA8WS bits control the number of wait states inserted during the respective operation. The IOWS bits control the number of BCLK wait states that are inserted for I/O accesses to the 82C206 peripherals (8259,8237,8254).

7	6	5	4	3	2	1	0	Idx
IOWS		DMA16WS		DMA8WS		EMEMR	DMACLK	01

Figure 4.2: 82C206 Configuration Data Register

The DMA16WS bits control the number of DMACLK wait states that are inserted for 16-bit DMA channel (DRQ5-7) operations. DMA8WS bits control the number DMACLK wait states that are inserted for 8-bit DMA channel operations. Table 4.2 lists the wait-state encodings.

Table 4.2: Wait-State Encodings

Wait state encoding	Number of wait states inserted
00	1 wait state
01	2 wait states
10	3 wait states
11	4 wait states

EMEMR, when set, causes the assertion of MEMR# to occur one DMA clock earlier than standard PC/AT timing. When clear, the assertion of the MEMR# signal follows the timing in the original PC/AT.

DMACLK, when set, will cause BCLK to be sourced to the internal DMA controllers (8237s). When clear, BCLK/2 is sourced to the internal DMA controller.

R400EX INDEX/DATA REGISTER

These registers form an index/data register pair for accessing R400EX registers. Only the lower six bits of the index register are implemented. Accesses to address 026 return or modify the register that is selected indirectly by the 6-bit address register's content. Attempting to write to a single byte of the data register (writing a single byte only 026h or 027h) will result in both bytes of the selected register being written.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Adr
Index																024
Data																026

Figure 4.3: R400EX Index/Data Register

KEYBOARD DATA REGISTER

7	6	5	4	3	2	1	0	Adr
Keyboard data								060

Figure 4.4: Keyboard Data Register

KEYBOARD STATUS/COMMAND REGISTER

7	6	5	4	3	2	1	0	Adr
Keyboard status/command								064

Figure 4.5: Keyboard Status/Command Register

PORT B REGISTER

The Port B register supports NMI generation, timer/counter2, and speaker control.

7	6	5	4	3	2	1	0	Adr
Parity Check	0	Timer Counter 2 OUT Status	Refresh Toggle	RAM	Enable DRAM Parity Check	Speaker Data Enable	Timer Counter 2 GATE Enable	061

Figure 4.6: Port B Register

- Timer Counter 2 Enable, when set, enables counting. This bit controls the GATE input to Counter 2. This bit is cleared on HW reset.
- Speaker Data Enable, is ANDed with the Counter 2 OUT signal to drive the SPKR output signal.
- Bits 2 enable the parity feature when set to 0. When enabled, parity errors can cause an NMI to be generated.
- Bit 7 of port 0x70 must also be set to allow NMI to be signaled. When bit 2 is written to a 1, bit 7 is cleared.
- Refresh toggle is a bit that toggles every time a DRAM refresh occurs. This bit is cleared on HW reset.
- Timer Counter 2 OUT Status reflects the state of the TIM2_OUT pin.
- Bits 6 and 7 are read-only bits. In PC architecture, they reflect IOCHCK and parity errors respectively. Bit 7 is set by a parity error. To clear bit 7, the parity enable bit (bit 2) must be set to one.

RTC REGISTERS

These registers are for an index/data register pair for accessing the RTC and CMOS RAM.

Bit 7 of register 70 is the DISNMI bit. When clear , this bit enables the NMI function. This bit is preset to a 1, disabling the NMI function at power-up.

The register at 0x070 is a write-only register.

7	6	5	4	3	2	1	0	Adr
DISNMI	RTC index							070
RTC data								071

Figure 4.7: RTC Registers

PORT A (PORT 92) REGISTER
This register is PS/2 compatible.

When SRESET is set, the SRESET pin is asserted on the R400EX for a minimum of 16 CLKIN cycles. The A20M register bit is "AND'ed" with the CPU's A20 bit to supply the system's A20 address bit.

7	6	5	4	3	2	1	0	Adr
Reserved						A20M	SRESET	092

Figure 4.8: Port A (Port 92) Register

IDENTIFICATION REGISTER
The upper 12 bits of the ID register form a read-only constant that identifies the part and its revision number.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Idx
0	1	0	0	0	0	0	0	0	0	0	0	BIOS Revision				0

Figure 4.9: Identification Register

Bits 7–4 are intended to encode the stepping revision. The remaining four register bits are read/writeable and are reserved for BIOS use only. These bits are reset to 0 by a hardware reset.

POWER-UP OPTION REGISTER
This read-only register latches the state of the strappable options.

11	10	9	8	7	6	5	4	3	2	1	0	Idx
MA[11:0], latched while PWRGOOD is de-asserted.												01

Figure 4.10: Power-Up Option Register

Bits 0-11 control the initial configuration of the R400EX (refer to Power-Up Configuration options). When the R400EX enters the low-power HALT state, it re-drives the contents of this register out to the MA[11:0] lines to remove the static power consumption that the external pull-up or pull-down resistors would otherwise consume.

BIOS CONTROL REGISTER
This register is used to control access to the Flash boot device using the CE_BIOS# and WE_FLASH# pins. DRAM shadowing of the CE_BIOS# regions take precedence over the generation of CE_BIOS# (the opposite of the RadiSys R380EX).

15	14	13	12n	11	10	9	8	Idx
			ZWS	BIOSSIZE	LFLSHWE	BIOSWE	APPWE	02
7	6	5	4	3	2	1	0	Idx
F8000-FFFFF	F0000-7FFFF	E8000-EFFFF	E0000-E7FFF	D8000-DFFFF	D0000-D7FFF	C8000-CFFFF	C0000-C7FFF	02

Figure 4.11. BIOS Control Register

The least significant 8 bits enable, when set, the address decode of each of the address regions represented by the bit into an overall CE_BIOS#. APPWE, when set, allows WE_FLASH# to be asserted for all CE_BIOS# address regions except the top 128KB where the BIOS normally resides.

BIOSWE, when set, enables writes to the BIOS system code portion of the Flash device at both the top of memory and just below 1MB (in conjunction with LFLSHWE). This is the region in the upper 128KB of memory. This bit is cleared on HW reset.

LFLSHWE, when set, enables writes to the flash region below 1MB. This bit is cleared on HW reset. Both LFLSHWE and BIOSWE must be set to write to the low BIOS region, and LFLSHWE and APPWE must both be able to write the application Flash below 1MB.

The BIOSSIZE, when set, enables the decode of the top 4MB (0XFFC0_0000-0xFFFF_FFFF) and causes CE_BIOS to be asserted for this address range. If clear, only the top 1MB causes CE_BIOS to be asserted. The BIOS wait states field determines the number of wait states inserted into a BIOS read access as follows: the ZWS bit, if set, causes the ISAbus transaction to the BIOS to use fast ISAbus memory timing (as if the NOWS# pin had been asserted). Pin MA3 is sampled at Power-Up to determine whether BIOS accesses are sequenced to the ISAbus as 8-bit or 16-bit transactions.

SHADOW 1 REGISTER

This register contains two shadow control bits for each region shown in Figure 4.12.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Idx
D4000-D7FFF		D0000-D3FFF		CC000-CFFFF		C8000-CBFFF		C4000-C7FFF		C0000-C3FFF		B0000-BFFFF		A0000-AFFFF		03

Figure 4.12. Shadow 1 Register

The register is cleared to 0 by reset. These bits take precedence over the BIOS control register bits. That is, an ISA cycle to the BIOS cannot take place unless the respective shadow region has been defined as read/write ISA (the power-on default). The two bits control the routing of memory accesses for their respective regions and are encoded as shown in Table 4.3. This register is cleared on HW reset.

Table 4.4: Encoding

Encoding	Function
00	Read/write ISA
01	Read ISA; write to DRAM
10	Read DRAM; write to the bit-bucket (neither an ISA nor a DRAM access is generated, but ready is returned to the CPU)
11	Read/write DRAM

SHADOW 2 REGISTER

The shadow control bits in this register are interpreted in the same manner as they are in Shadow register 1.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Idx
F8000-FFFFF		F0000-F7FFF		EC000-EFFFF		E8000-EBFFF		E4000-E7FFF		E0000-E3FFF		DC000-DFFFF		D8000-DBFFF		04

Figure 4.13. Shadow 2 Register

PARITY ADDRESS HIGH REGISTER

The Parity Address Low and Parity Address High registers are used to save the address of an access that caused a parity error. Under program control, these registers can only be read.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Idx
BE3-BE0				SMI	A26-A16											07

Figure 4.14. Parity Address High Register

The Address Parity High register is continuously updated while both the Save Parity Address (SPA) bit of the DRAM control register is set and PortB (I/O address 0x61) bit 7 is clear (no parity error has occurred yet). Once bit 7 of Port B is set, the register is no longer updated until Port B bit 7 is cleared again and the SPA bit is set.

When this register is in the continuous update mode, bits 15–12 store the current cycles byte enables (0 means that the respective byte enable is asserted). Bit 11 stores the SMIACT# pin (0 means that SMI is active) and bits 10–0 store the address lines A26-A16 respectively.

PARITY ADDRESS LOW REGISTER

Except for bit 0, the Parity Address Low register is continuously updated while both the SPA bit of the DRAM control register is set, and the PortB (I/O address 0X61) bit 7 is clear (no parity error has occurred yet).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Idx
A15:A2														HLDA	PM	08

Figure 4.15. Parity Address Low Register

Once bit 7 of Port B is set, the register is no longer updated until Port B bit 7 is cleared again and the SPA bit is set. When this register is in the continuous update mode (waiting for a parity error to occur), bits 15–2 are updated with the local bus's A15–A2 address signals. Bit 1 is updated with the HLDA signal (to allow a DMA address to be differentiated from a CPU access). Bit 0 is the Parity Missed (PM) bit. This bit is set if a parity error occurs, but the parity address is not stored in the Parity Address Low and High registers. This could happen if the SPA is clear or if this register already contains an address of a previous parity error (bit 7 of Port B is clear). The PM bit is cleared at the same time that bit 7 of PortB is cleared. This is done by setting bit 2 of PortB.

MISCELLANEOUS PIN CONFIGURATION REGISTER

This register may be used to redefine the pin functions that are established by reset.

When DIS_KB is set, the keyboard clock and data pins are disabled and these pins are treated as IRQ1 and IRQ12 inputs. The internal keyboard and mouse decodes are also disabled and instead, the I/O accesses to the keyboard addresses send/receive data from the ISAbus.

When DIS_KB is set and EXRTC is clear, CS_USR0# is connected to an external pin instead of the MO_CLK or RTC_DS.

7	6	5	4	3	2	1	0	Idx
X	IDEMD		DISPAR	EXRTC	CSUSR1	DIS_KB	COMCLK	0A
X	0	0	MA8	MA1	MA7	MA2	MA9	Reset

Figure 4.16. Miscellaneous Pin Configuration Register

The CSUSR1 bit, when clear, causes the ISAbus REFRESH# function to be connected to an R400EX pin. When set, CS_USR1# function is connected instead to the R400EX pin.

The EXTRTC bit, when set, causes IRQ8# (instead of RTCPS) to be connected to the external pins of the R400EX. It also causes all RTC accesses (I/O to 0x70 and 0x71) to be sourced to/from the ISAbus.

The DISPAR bit, when set, disables parity generation and detection. It also enables the CS_USR2#, CS_USR3#, IDEWR#, IDERD#, and SMIINP# functions on the shared pins of DP0-3 and NMI respectively. When clear, parity generation and detection are enabled and the shared pin functions become DP0-3 and SMIINP#.

The IDEMD bits define the EIDE modes supported by the R400EX as described in Table 4.5.

Table 4.5: IDEMD Bits and Functions

IDEMD	function
00	PIO mode 0
01	PIO mode 3 (valid only at 40MHz or slower CLKIN)
10	PIO mode 4 (CLKIN = 50MHz, also works suboptimally for slower frequencies)
11	PIO mode 4 (CLKIN < 40MHz)

The IDEMD bit settings allow the R400EX to support EIDE drives (PIO mode 3 or 4) at a much higher transfer rate. Not all PIO mode 3 IDE drives will be able to support the minimum read/write cycle time of the R400EX (180ns at 33MHz CLKIN), but all PIO mode 4 IDE drives should be capable of supporting this cycle time. In any case, the

specific EIDE drive specifications must be checked for compatibility. When this bit is clear, PIO mode 0 (the old IDE timing) is supported.

SMI TIMER CONTROL REGISTER

Writes to this register set the clock prescaler value (PRE) and the 12-bit idle timer latch. Writes to the idle timer latch write through the latch into the counter, as well. Reads at this address return the value in the counter, as well as the value of the PRE bit.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Idx
PRE	Reserved			Idle timer latch (wr), timer/counter (rd)												0B

Figure 4.17. SMI Timer Control Register

If PRE is set, a 16-Hertz clock is used to decrement the timer counter. When PRE is 0, a 1024-Hertz clock is used to decrement the timer/counter. Thus, the counter can be set in the range of 63 milliseconds to 256 seconds or from about 1 milisecond to 4 seconds.

The timer/counter is reset to the latch value whenever the following events occur:

- The SMIINP# pin is asserted and configured for the ACTIVITY# function
- The internal programmable chip select is asserted and enabled
- The idle timer latch is written to by software
- The counter is at zero and the SMI has been acknowledged by the CPU (SMIACT is asserted)

When the timer/counter reaches zero, an SMI event is signaled (if SMI is enabled) and the timer is stopped. In this case, the timer is reloaded in response to SMIACT being asserted. The timer/counter does not count down unless the ENTIM bit is set in the SMI control/status register; however, writes to the SMI Timer control continue to update the timer/counter independent of the ENTIM bit value. Both the latch and the timer/counter are cleared on HW reset. The prescaling counter (counts down) is also preset to all ones by a reset or a write to this register.

SMI CONTROL/STATUS REGISTER

This register controls the sources of SMI, the global SMI enable and the SMM RAM Map enable. It also contains several read-only status bits.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Idx
RESERVED			HLTS	RSV	TEXP	EXT0	SMTOP	SMAB	ENPCS	ENSMI	SWSMI	ENHLT	ENTIM	EACT	EEXT	0C

Figure 4.18. SMI Control/Status Register

The EEXT bit enables an SMI event when the SMIINP# is asserted. This bit is cleared on HW reset.

The EACT bit enables the SMIINP# to reset the SMI activity counter to its starting valued. This bit is cleared on HW reset. If both the EEXT and the EACT bits are set, the SMIINP# will both reset the activity timer and cause and the SMI event to be asserted. ENTIM enables the SMI timer counting process and the SMI timing event when the SMI timer reaches 0. This bit is cleared on HW reset.

ENHLT enables an SMI event when a HALT bus cycle is detected on the CPU bus. This bit is cleared on HW reset.

SWSMI is an SMI event bit triggered by software. When set, an SMI event is signaled. This bit is cleared on HW reset.

ENSMI is the overall SMI event enable. This bit must be set to allow an SMI to be signaled to the CPU. This bit is cleared on HW reset.

The SMTOP and SMAB bits allow the SMI memory to be mapped to different regions of the DRAM when SMIACT is asserted. If SMTOP is asserted, the top 256KB of DRAM memory can be accessed only when the SMIACT# pin is asserted. If SMAB is asserted, then DRAM behind addresses 0xA0000-0xBFFFF will be accessed when SMIACT# is asserted (overrides shadow register settings). These bits are cleared on HW reset.

SMI status portion. The TEXP and EXT bits are status bits to indicate which of the respective SMI sources caused the SMI interrupt.. When an SMI is signaled to the CPU, the corresponding bit is set to indicate the source of the SMI

event. These bits are cleared on HW reset or can be cleared by writing a "0" to the corresponding bit. Writing a "1" into each of these bits allows the prewrite state of these bits to be maintained.

The SMI handler must clear the status bit(s) causing the SMI before exiting the SMI handler to prevent the SMI# being signaled again when exiting the SMI handler. The SMI handler should write a "1" to any status bit that it has not yet handled.

PCS 0 COMPARE AND MASK

The OR bit, when set, normally causes CS_USR(x+1) to be OR'ed into CS_USR(x). To eliminate building a circular latch circuit, CS_USR3 is a "boundary case" that does not implement the normal OR bit function. The OR bit, in this case, is just read/writeable and serves no other function. For PCS0, the OR bit, when set, causes CS_USR1 to be OR'ed into CS_USR0.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Idx
MODE			OR	IOR	IOW	Compare and mask bits										0D

Figure 4.19. PCS 0 Compare and Mask Register

In an I/O decode mode, the IOR bit , when set, requires the ISAbus's IOR to be asserted along with the appropriate address to assert this chip select. If the I/O peripheral is connected to the local bus (LDEV# asserted), this bit may not be set. If a memory decode mode is selected (see Table 4.6), this bit is matched against processor address A31.

In an I/O decode mode, the IOW bit , when set, requires the ISAbus's IOW to be asserted along with the appropriate address to assert this chip select. If both IOR AND IOW bits are set, the chip select is asserted whenever IOR or IOW is asserted along with the appropriate address. If neither bit is set, the chip select is asserted on the basis of the address decode alone. If the I/O peripheral is connected to the local bus (LDEV# asserted), neither of these bits can be set.

If a memory decode mode is selected (see Table 4.6), this bit is matched against processor address bit A26.

The 10 bit compare and mask bits field is interpreted on the basis of the MODE bits as described in Table 4.6.

Table 4.6: Compare and Mask Bits Field Interpretation

Mode	Decode function
000	Disables the chip select.
001	Decodes a single-byte I/O address using the compare and mask bits as A[9:0] comparison bits only. A15–A10 must be low. I/O peripheral must not be connected to the local bus.
010	Decodes a power of 2 region of I/O address space using the compare and mask bits as described below. A15–A10 must be low.
011	Decodes a power of 2 region of I/O address space using the compare and mask bits as described below. A15 must be high. A14–A10 must be low.
100	Decodes a power of 2 region of local bus memory region using the lower 12 bits as compare and mask bits. Bits IOR and IOW are re-defined to match A31 and A26, respectively, and A[25-16] are matched to the remaining bits. Only memory accesses are decoded (M/IO = 1).
101	Decodes a single 64KB local bus memory region using the lower 12 bits as comparisons only.. Only memory accesses are decoded (M/IO = 1).
110	This is the same as the 010 encoding, but in addition, it asserts IOCS16.
111	This is the same as the 110 encoding, but in addition, it asserts IOCS16.

Note: The smallest local bus peripheral I/O address space that can be decoded correctly is a 4- byte, naturally aligned region.

When the MODE bits are set to x1x or 100, the compare and mask bits are used as follows. The least significant bit of the compare and mask bits that is a "0" specifies the demarcation line that separates the compare bits from the mask bits. The bits of lower significance ("1") than the first 0, cause the corresponding address bit to be masked off.

Only the compare and mask bits to the left of the first 0 are used to compare to the corresponding processor address bits to determine if the chip select is to be asserted.

For example, if the compare and mask field contains a 'b01,1111,0011, and the MODE bits are set to x1z, the I/O address range 0x1F0-0x1F7 causes the chip select to be asserted. I/O addresses down to a byte granularity can be decoded correctly for a peripheral that is connected to the ISAbus.

MODES 100 and 101 work in a fashion similar to MODES 010 and 001, respectively. However, only local bus memory accesses are decoded and bits 9–0 of the register are used to match A25–A16. In these MODES, bit 11 (IOR bit) is compared to A31 (never used in a mask fashion), and bit 10 (IOW bit) is compared to A26 (never used in a mask fashion).

PCS 1 COMPARE AND MASK

This has the same function as PCS0, except that CS_USR1 is asserted when the comparitor matches, and the OR bit causes the CS_USR2 to be OR'ed into CS_USR1.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Idx
MODE			OR	IOR	IOW	Compare and Mask bits										0E

Figure 4.20. PCS 1 Compare and Mask Register

PCS 2 COMPARE AND MASK

This has the same function as PCS0, except that CS_USR2 is asserted when the comparitor matches, and the OR bit causes the CS_USR3 to be OR'ed into CS_USR2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Idx
MODE			OR	IOR	IOW	Compare and Mask Bits										0F

Figure 4.21. PCS 2 Compare and Mask Register

PCS 3 COMPARE AND MASK

This has the same function as PCS0 except that CS_USR3 is asserted when the comparitor matches. The OR bit serves no useful purpose for this boundary case.

The PCSx registers are all cleared on HW reset.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Idx
MODE			OR	IOR	IOW	Compare and Mask Bits										10

Figure 4.22. PCS 3 Compare and Mask Register

CLOCK/RESET CONTROL REGISTER

All register bits except CDIV1are cleared by HW reset. CDIV1 and CDIV0 specify the CLK2OSC- divide ratio that is used to generate the CLKOUT pins as shown in Table 4.7.

9	8	7	6	5	4	3	2	1	0	Idx
RSVD	HLTS	RSVD	DEL1	DEL0	ENHLT	SDIV1	SDIV0	CDIV1	CDIV0	12

Figure 4.23. Clock/Reset Control Register

CDIV1 and CDIV0 are initially reset to 0. If the R400EX detects a transition in CDIV, 0 encodings, when writing to this register, it will issue STPCLK# and wait for a Stop Grant bus cycle before changing the frequency. STPCLK# will then continue to be asserted for 1 millisecond before being de-asserted. This allows the CPU's PLL to lock onto the new frequency before resuming.

Table 4.7: CLK2OSC Divide Ratio

CDIV1, CDIV0	CLK2OUTx output
0-	CLK2OSC divided by 2
10	CLK2OSC divided by 8
11	CLK2OSC divided by 32

SDIV1 and SDIV0 specify the CLKIN divide ratio for the ISAbus BCLK pin (and CLKS2 and CLKS0 if needed) according to Table 4.8. When CLKOUTx output is connected to the CLKIN input on the R400EX, as recommended, the BCLK and CLK2OUT dividers act in a series. For example, if all four clock-divide bits are set to 0, a 66MHz CLK2OSC input are divided down to 33MHz to supply the CLKOUT pin. The BCLK output is 11 MHz in this case.

Table 4.8: CLKIN Divide Ratio

SDIV1, SDIV0	BCLK output	CLKS2 (if needed)	CLKS0 (if needed)
00	CLKIN divided by 3	CLKIN divided by 12	CLKIN divided by 6
01	CLKIN divided by 4	CLKIN divided by 8	CLKIN divided by 2
10	CLKIN divided by 6	CLKIN divided by 12	CLKIN divided by 3
11	CLKIN divided by 2	CLKIN divided by 8	CLKIN divided by 4

ENHLT, when set, enables glitchlessly switching the CLKOUT1 pin to a 32KHz (RTC_X1) frequency, and the CLKOUT0 pin is completed, stopped, and driven low, allowing the system to conserve power while the CPU is in the HALT state. In addition, this bit enables generating an active low OSC_OFF signal (shared with the NAND_OUT pin) that can be used to power down an external oscillator or PLL-clock synthesis chip to reduce system power consumption further.

DEL1 and DEL0 allow a programmable clock reconnection delay to be observed when the main system oscillator has been powered down during a HALT. This allows an oscillator or PLL-clock synthesis chip, that has been powered-down by the OSC_OFF# signal, time to return to its rated output frequency before sourcing the clock back out to the processor. After this delay has been observed, STPCLK# is be held asserted for an additional 1ms to allow the CPU's PLL to lock onto the clock before the processor returns to its normal state. The delay control encodings are described in Table 4.9.

Table 4.9: Delay Control Encodings

DEL1-DEL0	Delay
00	No delay
01	.5 ms
10	2 ms
11	8 ms

HLTS is a status bit that is set when a HALT instruction is executed by the CPU. This bit can be cleared by writing a "0" into it. Writing a "1" into this bit retains the old value of HLTS. This bit can be used by system software like DOS, which uses a time-of-day interrupt to keep time. If set, the interrupt routine copies the RTC data to the DOS time of day, then resets the bit. Otherwise, the time of day should be correct, and the routine updates the time of day using the normal procedure.

DRAM CONTROL REGISTER

The SPA bit, when set, allows the address of an access that causes a parity error to be stored in the Parity High and Low registers. When clear, which is the default, the Parity High and Low registers are protected from being updated.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Idx
				SPA	TP	CACTRL		B2	BANKBSIZE			A2	BANKASIZE			13

Figure 4.24. DRAM Control Register

The TP (Test Parity) bit, when set, causes the R400EX to generate odd parity on DMA accesses (for testing purposes). When clear, which is the default, even parity is generated.

The CACTRL bits control whether the CPU's L1 cache (through the use of the KEN# pin) is enabled for various address regions as shown in Table 4.10.

Table 4.10: Cache Control Bits

Cache Control bits	Function
00	Nothing cached - reset default.
01	Cache all DRAM except A–F pages and memory used for SMM.
1-	Same as 01 except also cache R/W DRAM in the A–F pages.

The BANKBSIZE and BANKASIZE bits each use the 3-bit encoding in the Table 4.11 to determine their respective bank sizes.

Table 4.11: Encoding for Bank Sizes

Bank size bits	Bank size	#Row address.	#Column address
000	bank is not present.	-	-
001	bank first module is 256K x 32 - reset default.	9	9
010	bank first module is 512K x 32.	10	9
011	bank first module is 1024K x 32.	10	10
100	bank first module is 2048K x 32.	11	10
101	bank first module is 4096K x 32.	11/12*	11/10
110	bank first module is 8192K x 32.	12	11
111	bank first module is 16384K x 32.	12	12
*Always supported: 11/11. Supported, provided neither the BANKASIZE or BANKBSIZE exceeds 4096K x 32: 12/10. This restriction comes from the DRAM-address multiplexing scheme shown in Table 4.12.			

BANKASIZE defaults to the 001 encoding listed in Table 4.11 (256Kx32). BANKBSIZE defaults to the 000 encoding (bank not present). Except for the most significant bit of the row address, the row/column address multiplexing is the same for all module/bank sizes as shown in Table 4.12.

Table 4.12: DRAM Address Multiplexing Scheme

Address type	Signal name											
DRAM addr. bits	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
Column address	A25	A23	A21	A10	A9	A8	A7	A6	A5	A4	A3	A2
Row address	A24/23	A22	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11

A24 is placed on MA11 when either bank of memory is set to a bank size of 0x11- (8192K x 32 or 16,384K x 32). If both bank-size bits are set to 0x101 or a smaller size, then A23 is multiplexed as the row address onto bit MA11. This allows DRAM banks to be built from DRAMs that use a 12/10 asymmetric addressing scheme (some 4096K by

X DRAM chips use this addressing scheme); however, these DRAMs are not supported in either bank, if the other bank contains 16,384K x 32 or 32,768 x 32 of DRAM (bank size is 0x11-).

The A2 and B2 bits determine if the second half of their respective banks are present (RASAS# and RASBS#). If present, these banks must be the same size as the first module in the bank (the bank size bits also specify the size of the second module, if present), and, the second module's starting address immediately follows the ending address of the first module in the bank. If A2 is set, the R400EX asserts RASAS# for the appropriate address range. The B2 also helps determine if the second module of bank B is present.

DRAM TIMING REGISTER

The DAF and DNAF bits control when LDEV# is sampled by the R400EX. The DAF bit controls the LDEV# sample point for the 0x000A0000-0x000FFFFF region of memory. The DNAF controls the sample point for all other address regions.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Idx
RSVD		MODE		DAF	DNAF	REFTIM		REFI	RASW	CRP	ASR	RAH	WRT	RDTIM		14

Figure 4.25. DRAM Timing Register

When the DAF or DNAF bit is set, LDEV# is sampled by the R400EX in the second T2 state (default) for the respective address region. When clear, LDEV# is sampled in the first T2 of a 386 bus cycle. Clearing the bits allows DRAM cycles to start sooner, but at the expense of requiring any local bus peripheral to assert/de-assert LDEV# very quickly in response to a new address/bus cycle on the 486 bus.

Table 4.13: MODE Function Codes

MODE	Function
00	RDY#, no burst cycles, no page-mode, reset default
01	BRDY#, burst cycles, no page-mode
10	RDY#, no burst cycles, no page-mode, slow reads to allow EDO detect
11	BRDY#, burst cycles, page-mode, normal operation

Table 4.14: REFTIM Function Codes

REFTIM	Function
00	Refresh disabled
01	Every 15.50 usec (OSCIN / 222) reset default
10	Every 93.03 usec (OSCIN / 1332)
11	Special test mode

The REFI bit, when set, enables the ISAbus refresh function. When clear, which is the reset default, the ISAbus refresh function is disabled.

The RASW bit, when set (default), sets the RAS precharge minimum time to 2.5 CLKs and the RAS active minimum during refresh to 3.5 CLKs. When clear, the RAS precharge minimum time is set to 1.5 CLKs and the minimum RAS active time during refresh is set to 2.5 CLKs.

The CRP bit, when set (default), sets the CAS to RAS precharge time to a 1 CLK minimum. When clear, the CAS to RAS precharge time is 0.5 CLKs, minimum.

The ASR bit, when set (default), sets the address setup before the assertion of RAS to a minimum of 1 CLK. When clear, the address setup to assertion of RAS is set to a 0.5 CLK minimum.

The RAH bit, when set (default), sets the address hold after the assertion of RAS to be nominally 1 CLK. When clear, the address hold is nominally 0.5 CLK.

The WRT bit, when set, sets the DRAM burst-write timing to be X-3-3-3 (two wait states for the second through last burst-write access). When clear, the burst write timing becomes X-2-2-2.

The RDTIM bits define the DRAM type and the read burst timing (assuming page-mode, burst-ready is selected in the MODE field) as shown in Table 4.15. The timing for the first word of data is governed by other bits and by whether the first word is a page miss or hit. Subsequent words in a burst access are guaranteed to be a page hit when the MODE bits are set to page-mode, burst ready.

Table 4.15: RDTIM Functions

RDTIM	Function
00	EDO, X-1-1-1
01	EDO, X-2-2-2
10	FPM, X-2-2-2
11	FPM, X-3-3-3, reset default

WATCHDOG TIMER

Writes to this register set the clock prescaler value (PRE) and the 12-bit idle timer latch. Writes to the watchdog timer latch write through latch into the counter also. Reads at this address return the value in the counter as well as the value of the PRE bit.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Idx
PRE	Reserved			Watchdog Timer Latch (wr), Timer/Counter (rd)												15

Figure 4.26. Watchdog Timer

If PRE is set, a 16 Hz clock is used to decrement the timer counter. When PRE is 0, a 1024 Hz clock is used to decrement the timer/counter. Thus, the counter can be set in the range of about 63 ms and 256 seconds, or in a range of about 1 ms to 4 seconds.

The timer/counter is reset to the latch value whenever the following events occur:

- An ADS# occurs and bus mode is enabled (see Watchdog Control Register)
- The idle timer latch is written to by software
- The counter is at zero

When the timer/counter reaches zero, a hardware reset or IRQ10 can be signaled, depending upon the control bits in watchdog control register. Both the latch and the timer/counter are cleared on HW reset. The prescaling counter (counts down) is preset to all ones by reset or by a write to this register. The timer/counter does not count down unless the ENIRQ10 or the ENRES bit is set (refer to the following Watchdog Control Register description).

WATCHDOG CONTROL REGISTER

The DISHLT signal, when set, stops the watchdog countdown process while the CPU is in HALT mode. If this signal is clear, HALT mode does not stop the watchdog timer countdown process.

7	6	5	4	3	2	1	0	Idx
X	X	X	X	ENIRQ10	ENRES	ENBUS	DISHLT	16

Figure 4.27. Watchdog Control Register

When set, ENBUS causes the timer/counter to be reloaded from the watchdog timer latch whenever ADS# is detected. When clear, only software writes to the watchdog timer latch or the watchdog timer reaching zero cause the watchdog timer to be reloaded with the watchdog timer latch contents.

ENRES, when set, causes a hardware reset to be generated when the timer reaches zero.

ENIRQ10, when set, causes an IRQ10 to be signaled. Once set, IRQ10 will continue to be signaled until the Watchdog control register is read.

If both ENIRQ10 and ENRES bits are 0, the timer/counter does not count down. These bits are all cleared to zero by a Power-On reset.

DMA EXTENSION REGISTER

The bits in this register are sourced onto the CPU's address bus during a DMA. These bits are all cleared by reset.

7	6	5	4	3	2	1	0	Idx
A31	Reserved				A26	A25	A24	17

Figure 4.28. DMA Extension Register

DMA PIN REGISTER

The bits in this register are used to define DRQA/DACKA# and DRQB/DACKB# pins' connection to the internal 8237 DMA controller.

7	6	5	4	3	2	1	0	Idx
RSVD		DRQBENC			DRQAENC			18

Figure 4.29. DMA Pin Register

When external DMA multiplexing has been configured during reset, these register bits have no effect. This register is set by reset to connect DRQB/DACKB# to DRQ2/DACK2# and DRQA/DACKA# to DRQ1/DACK1# internally.

COM CONTROL REGISTER

The CLKSRC bit, when set, configures the COMCLK (shared with IRQ10) to be sourced into the COM1 and COM2 UART's clock inputs.

When the CLKSRC bit is clear, the COM clocks are sourced by the CLK2OSC divider circuit. COM2 may be disabled by configuring all of the pins to be COM1 pins. COM1 may also be disabled by setting DCOM1 to a "1." When DCOM1 is 0, the COM1 port is enabled.

8	7	6	5	4	3	2	1	0	Idx
CLKSRC	DCOM1	PINENC		CLK2OSC divisor					19
MA9	0	MA8	MA8	1	1	0	1	1	Reset

Figure 4.30. COM Control Register

The PINENC bits define how the eight physical R400EX pins get allocated between the two internal COM ports as shown in Table 4.16.

Table 4.16: Pin Allocation Between Internal COM Ports

PINENC	Function
00	COM1 is connected to all 8 external COM port pins. COM2 is disabled.
01	4 pins (RXD, TXD, CTS, RTS) for each COM port are connected to the external pins
10	COM2 is configured for IrDA (IrRX, IrTX) and 6 pins (RXD, TXD, CTS, RTS, DSR, DTR) of COM1 are connected externally.
11	RXD and TXD are connected to COM2 and RXD, TXD, CTS, RTS, DSR, DTR are connected externally to COM1

The CLK2OSC value in this register is used to by a loadable count down counter. When the counter reaches 1, it toggles the internal COMCLK signal and reloads the counter from COMCLK divisor register. Thus, COMCLK = CLK2OSC/(divisor*2) when a value of 0 in this register produces invalid behavior.

V. Electrical Characteristics

Table 5.1: Maximum Ratings

Condition	Maximun Rating
Case Temperature Under Bias	-65C to 110C
Storage Temperature	-65C to 150C
Supply Voltage with Respect to Ground	-0.5V to Vcc + 0.5V
Voltage on any pin	-0.5V to Vcc + 0.5V

Caution: Stressing the device beyond the Absolute Maximum Ratings may cause permanent damage. These are stress ratings only. Operation beyond the Operating Conditions is not recommended and extended exposure beyond the Operating Conditions may affect reliability.

Table 5.2: DC Characteristics: 5.0 Volt (VCC = 5.0V ± 10%, Tc = -40 C to +85 C)

Symbol	Parameter	Min	Max	Units	Test Conditions	Notes
V_{IL}	Input low voltage		0.8	V		
V_{IH}	Input high voltage	2.0		V		
V_{OL1}	Output low voltage		0.4	V	I_{OL} = 16mA	1
V_{OH1}	Output high voltage	2.4		V	I_{OH} = -16mA	1
V_{OL2}	Output low voltage		0.4	V	I_{OL} = 8mA	2
V_{OH2}	Output high voltage	2.4		V	I_{OH} = -8mA	2
V_{OL3}	Output low voltage		0.4	V	I_{OL} = 2mA	3
V_{OH3}	Output high voltage	2.4		V	I_{OH} = -2mA	3
I_{IL1}	Input leakage current		±15	µA		
I_{IL2}	Input leakage current		±350	µA		4
I_{LO}	Output leakage current		±15	µA		
C_{IN}	Input capacitance		8	pF		
C_{OUT}	Output or I/O capacitance		15	pF	@ 1MHz	
I_{CC}	V_{CC} supply current		200	mA	@33MHz, V_{CC} = 5.25V	

Notes:
1. Applies to outputs with 16mA drivers.
2. Applies to outputs with 8mA drivers.
3. Applies to outputs with 4mA drivers.
4. Applies to inputs that have weak internal pull-ups or pull-downs.

Table 5.3: DC Characteristics: 3.3 Volt (VCC = 3.3V ± 0.3V), Tc = -40°C to +85°C)

Symbol	Parameter	Min	Max	Units	Test Conditions	Notes
V_{IL}	Input low voltage		0.8	V		
V_{IH}	Input high voltage	2.0		V		
V_{OL1}	Output low voltage		0.4	V	I_{OL} = 8mA	1
V_{OH1}	Output high voltage	2.4		V	I_{OH} = -8mA	1
V_{OL2}	Output low voltage		0.4	V	I_{OL} = 2mA	2
V_{OH2}	Output high voltage	2.4		V	I_{OH} = -2mA	2
V_{OL3}	Output low voltage		0.4	V	I_{OL} = 1mA	3
V_{OH3}	Output high voltage	2.4		V	I_{OH} = -1mA	3
I_{IL1}	Input leakage current		±15	µA		
I_{IL2}	Input leakage current		±350	µA		4
I_{LO}	Output leakage current		±15	µA		
C_{IN}	Input capacitance		8	pF		
C_{OUT}	Output or I/O capacitance		15	pF	@ 1MHz	
I_{CC}	V_{CC} supply current		130	mA	@33MHz, V_{CC} = 3.45V	

Notes:
1. Applies to outputs with 16mA drivers.
2. Applies to outputs with 8mA drivers.
3. Applies to outputs with 4mA drivers.
4. Applies to inputs that have weak internal pull-ups or pull-downs.

VI. Mechanical & Thermal Specifications

MECHANICAL SPECIFICATIONS

The R400EX is packaged in a 208-pin plastic quad flat pack.

THERMAL SPECIFICATIONS

The R400EX operates over the case temperature range of -40C to +85C. The thermal characteristics of the package are to be included in a future update of this document.

> *Caution: The case temperature of the package should never exceed 105° C.*

VII. Testability

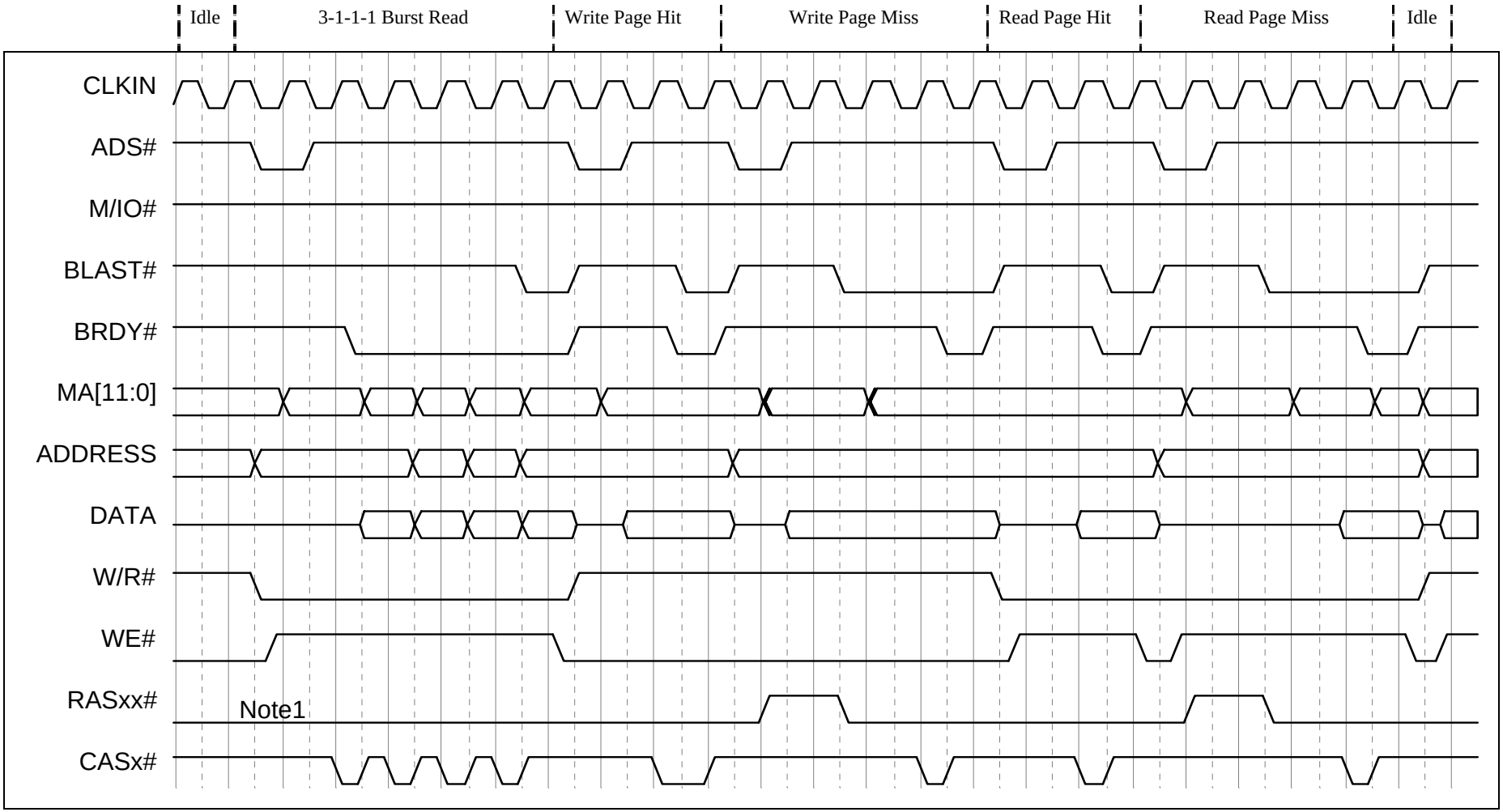
GLOBAL TRISTATE

Asserting the TEST input causes all of the output and I/O pins except for the NAND output to be tristate and enables the NAND tree. If any one input is low and all others are high, the NAND signal is high; otherwise it is low. The TEST input should be unasserted for normal operation.

NAND TREE ORDER

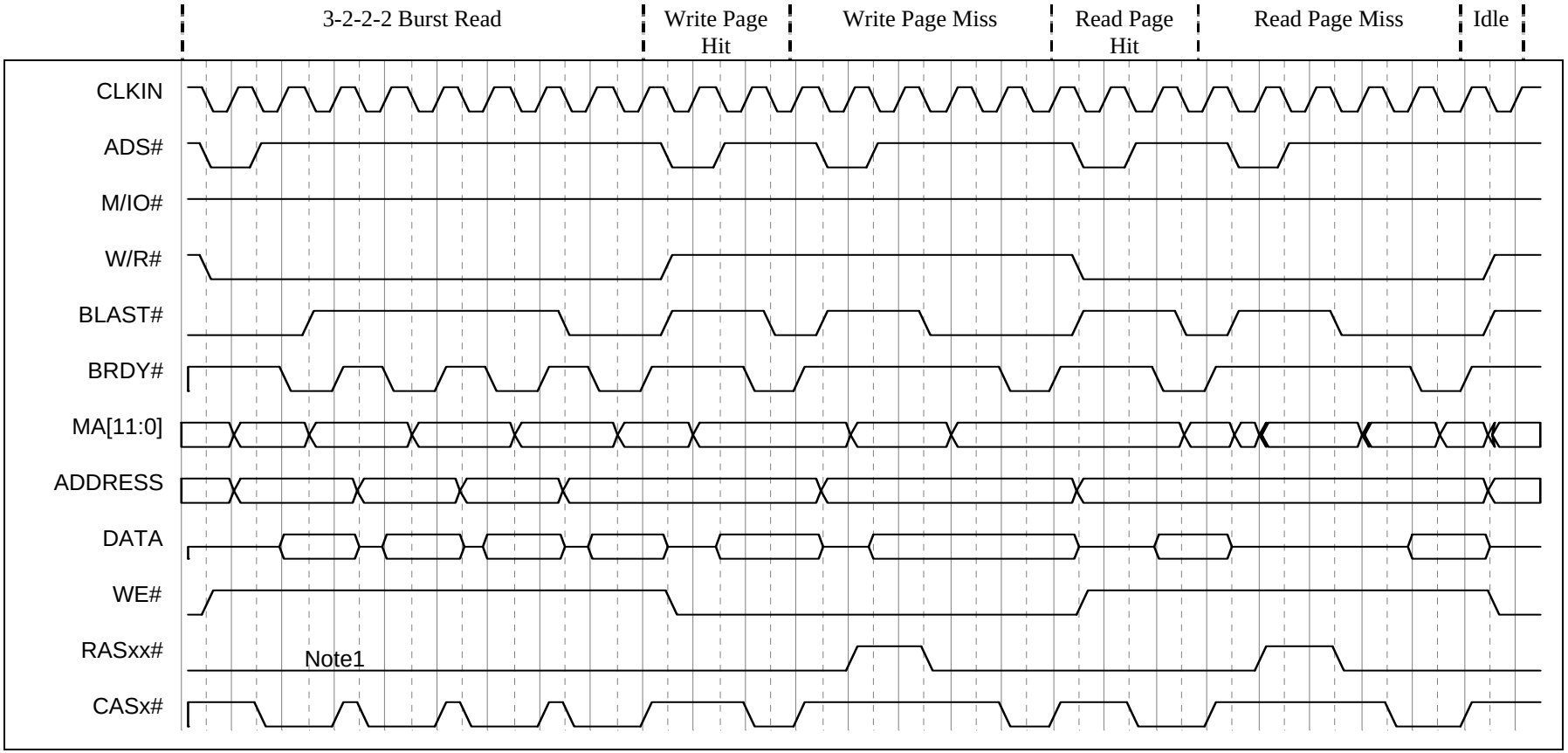
This will be included in a future update of this document.

Figure 1A: R400EX EDO DRAM Access Overview



Note:
1. RASxx# Asserted in previous non-burst read cycle
2. DRAM Timing register set to fastest timing mode

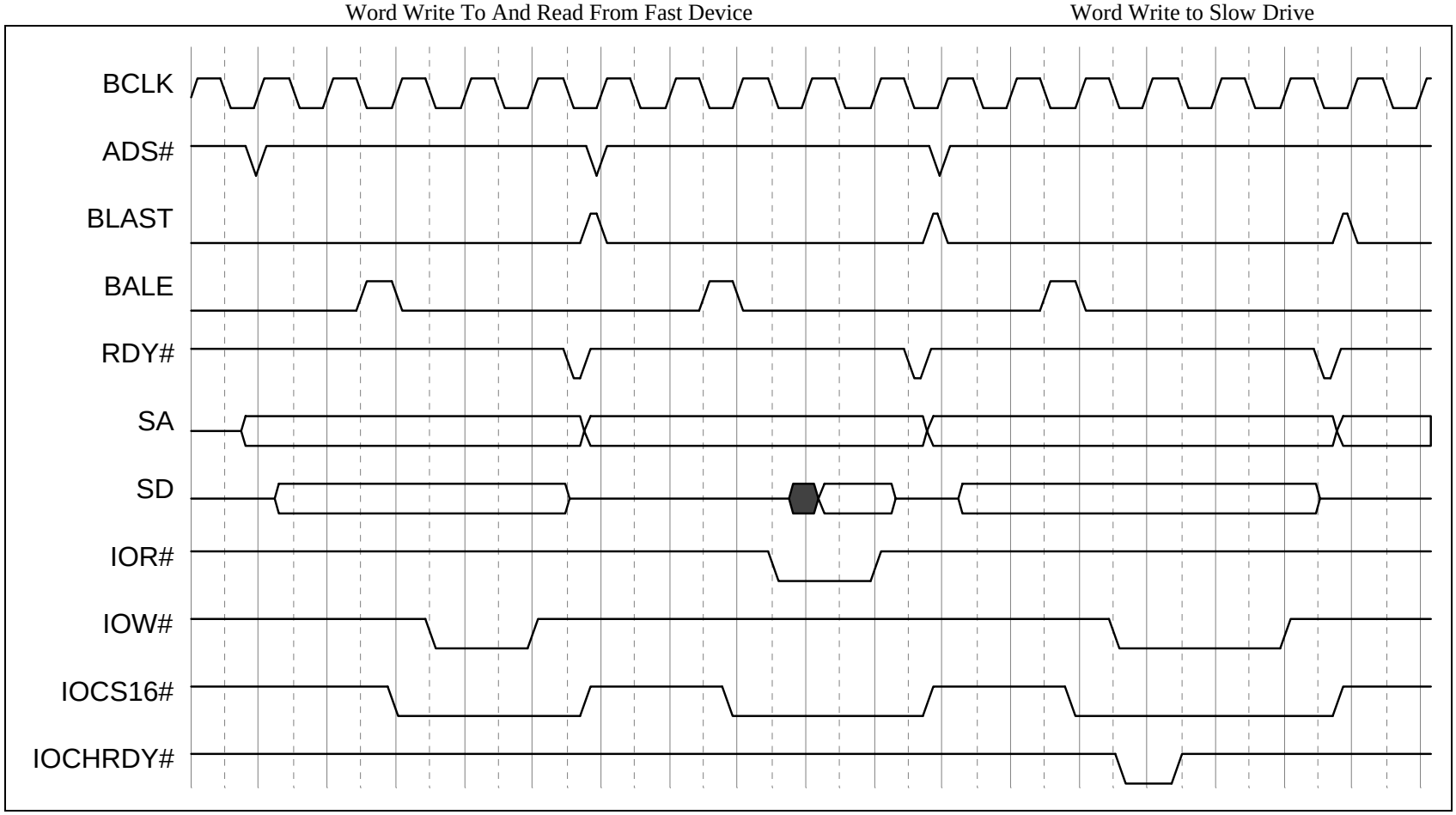
Figure 1B: R400EX FPM DRAM Access Overview



Note

1. RASxx# Asserted in previous non-burst read cycle
2. DRAM Timing register set to fastest timing mode

Figure 2A: R400EX 16 Bit ISA I/O Device Access Overview



Note: High order SA/LA address lines are stable until the end of the ISA bus cycle
The original IBM PC, XT and AT platforms did not support 16 bit ISA no-wait-state cycle

Figure 2B: R400EX 8 Bit ISA I/O Device Access Overview

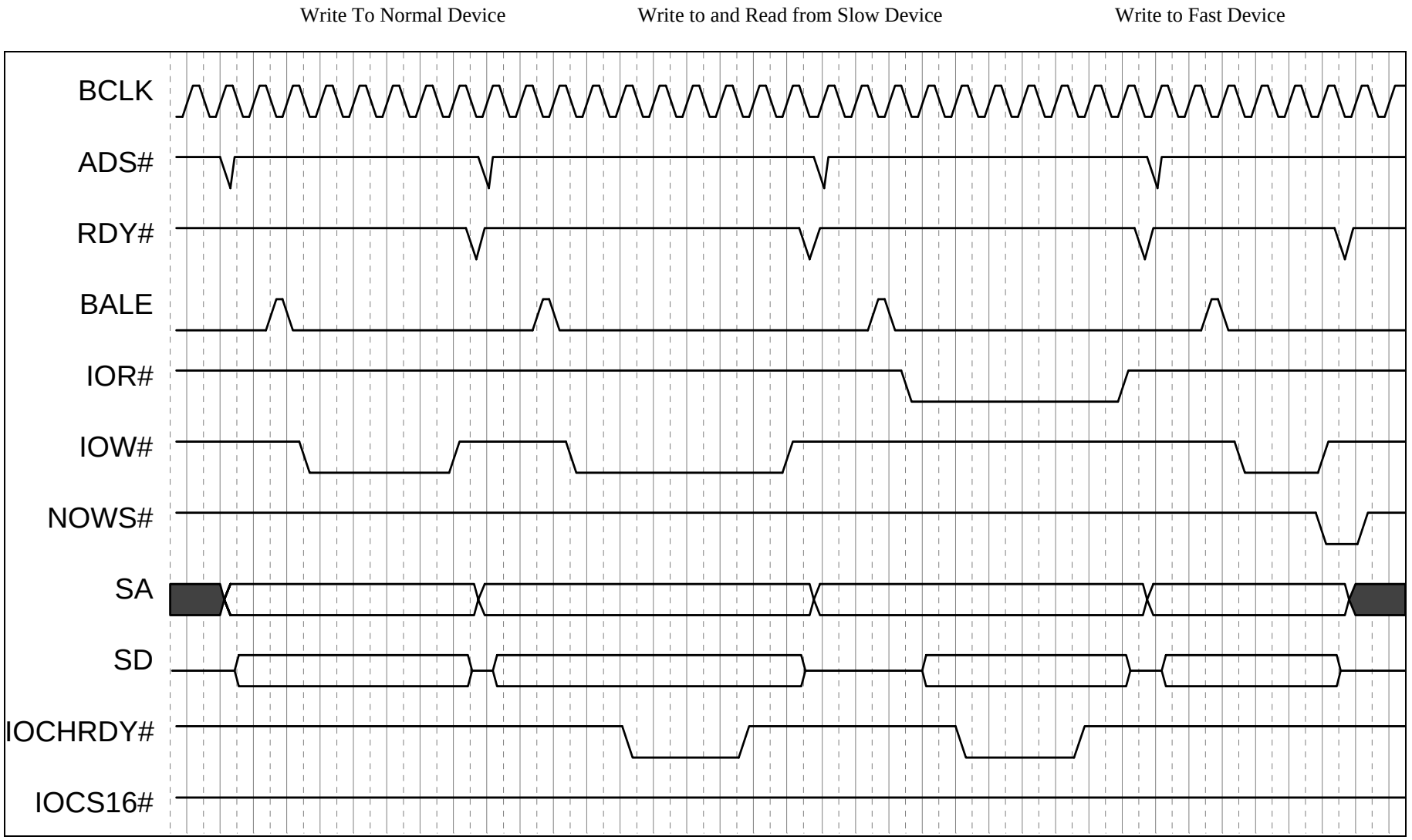


Figure 3A: R400EX 16 Bit ISA Memory Device Access Overview

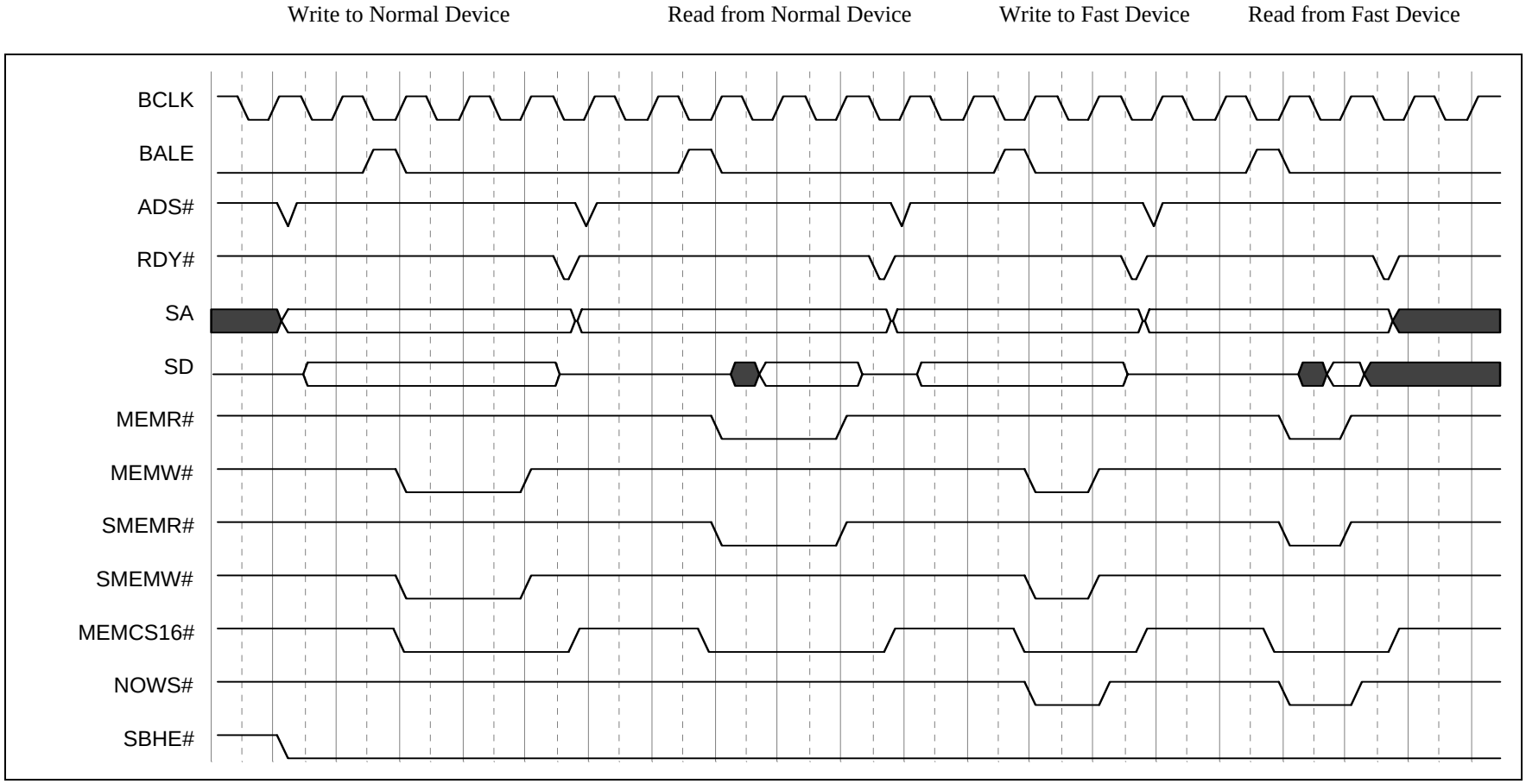


Figure 3B: R400EX 8 Bit ISA Memory Device Access Overview

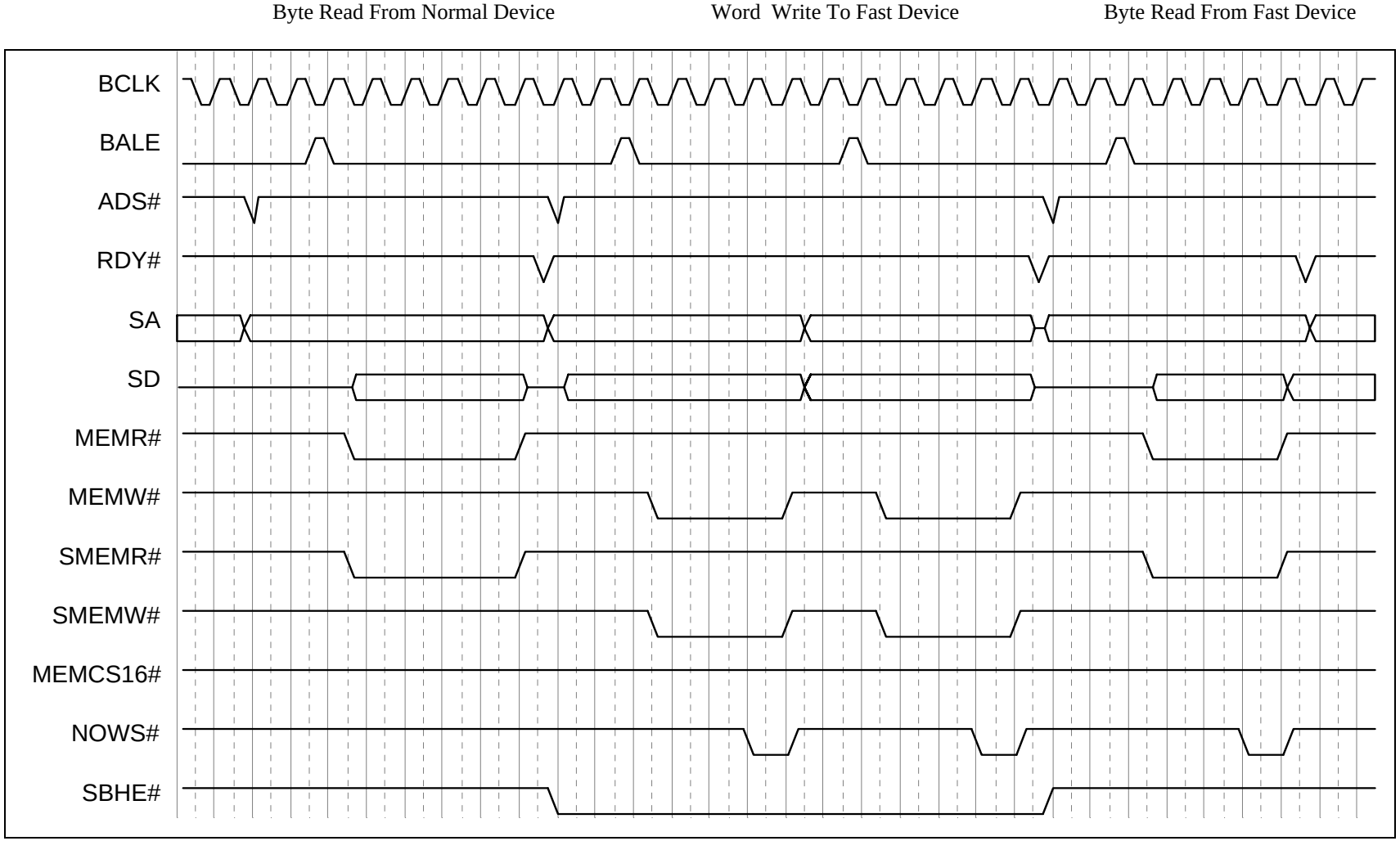


Figure 4A: R400EX 16 Bit DMA Read To DRAM Write Access Overview

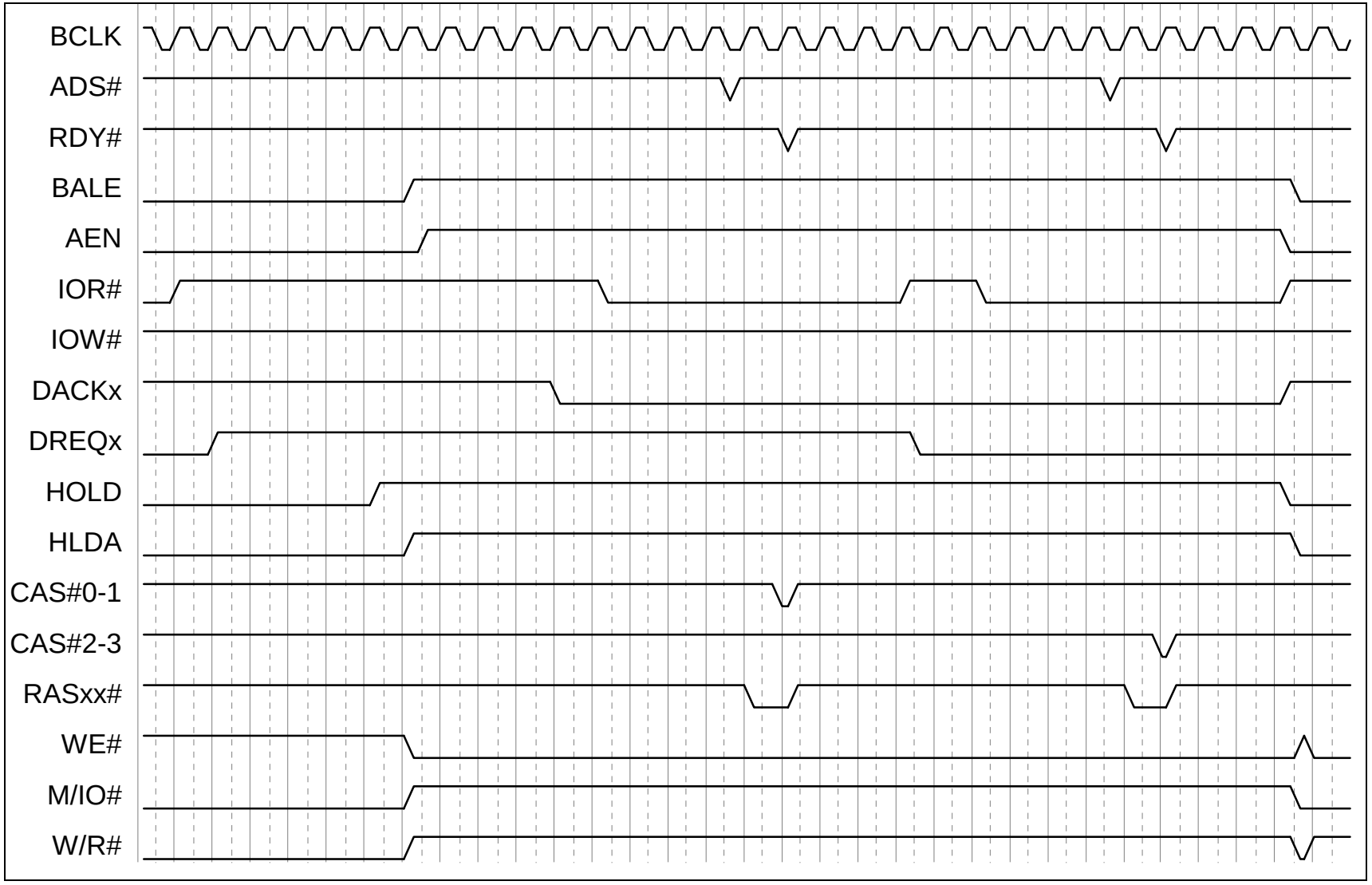


Figure 4B: R400EX 16 Bit DMA Write To DRAM Read Access Overview

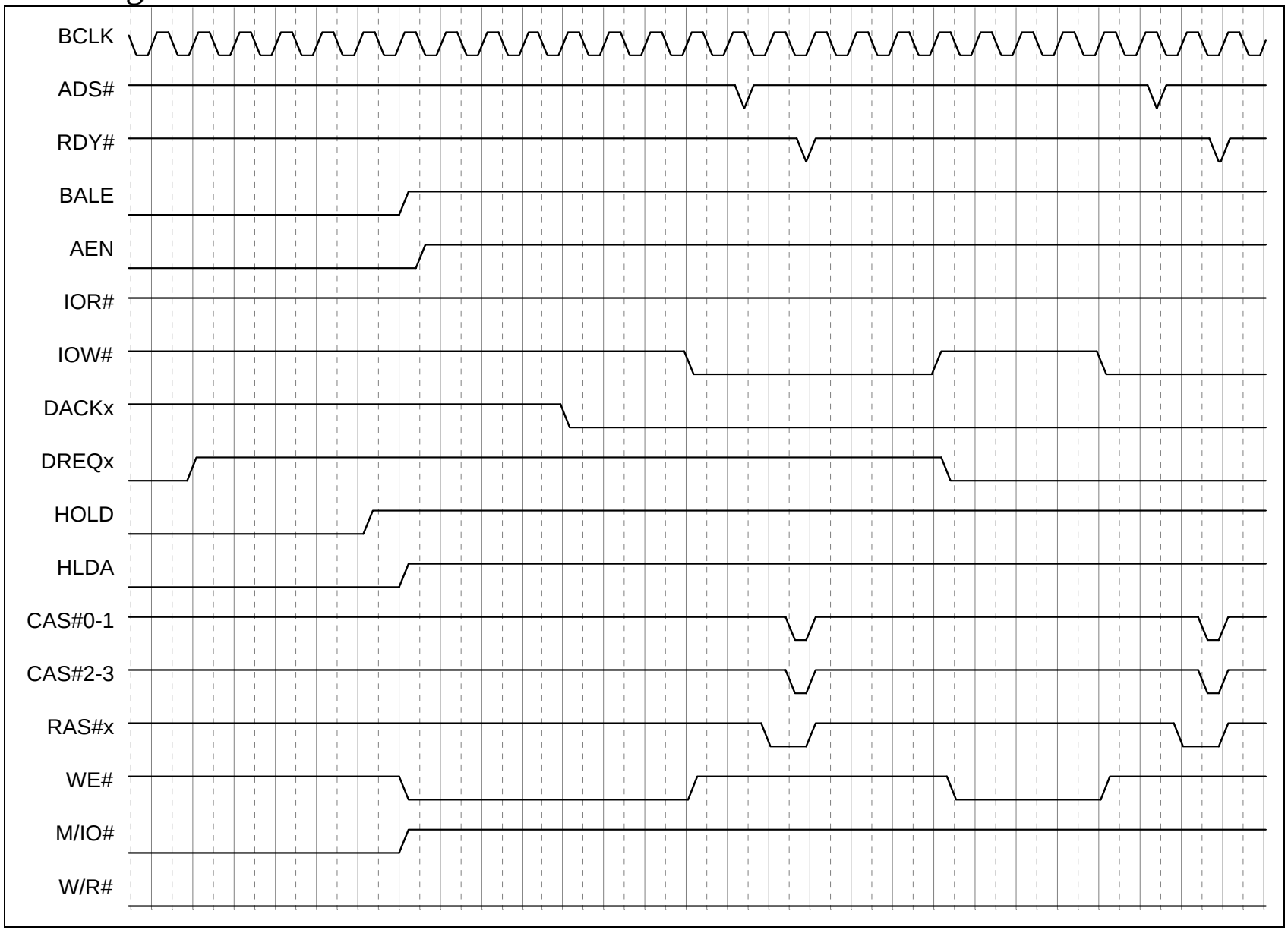


Figure 5: R400EX Flash Device Access Overview

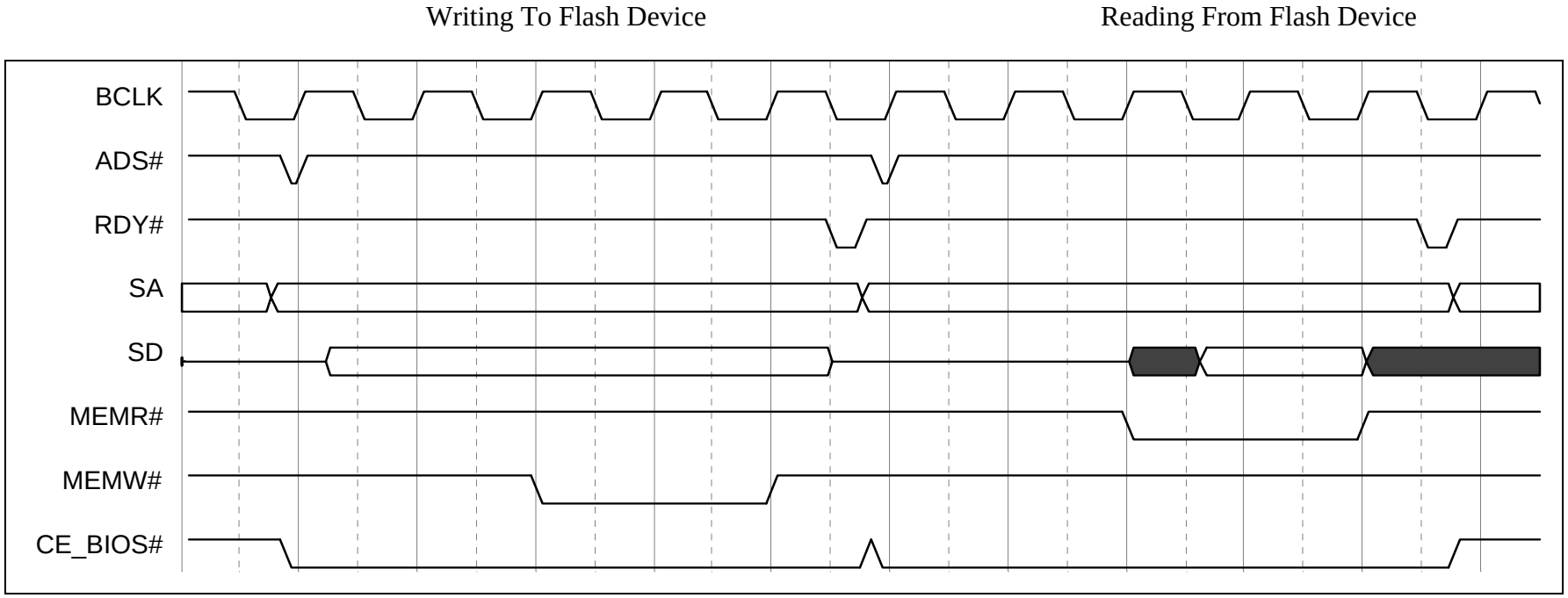
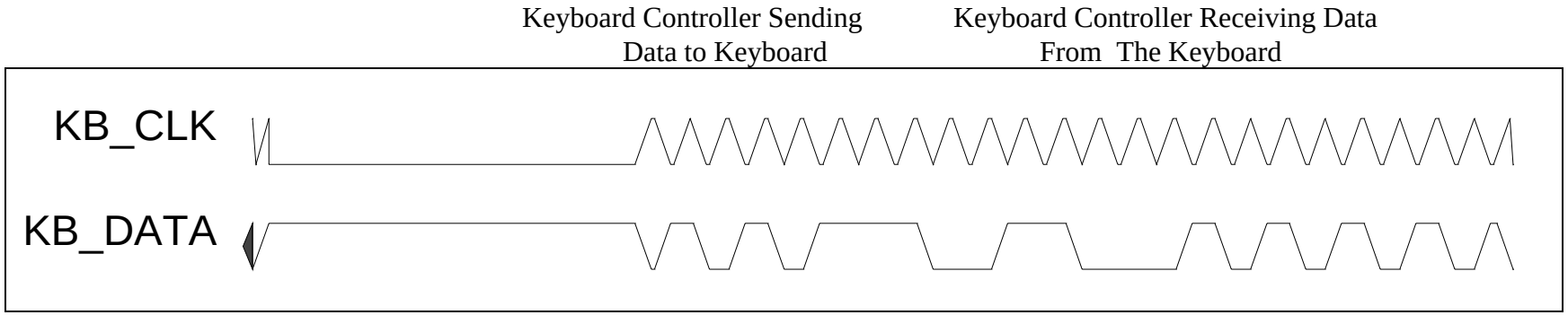


Figure 6 : R400EX Key Board and Mouse Controller Access Overview



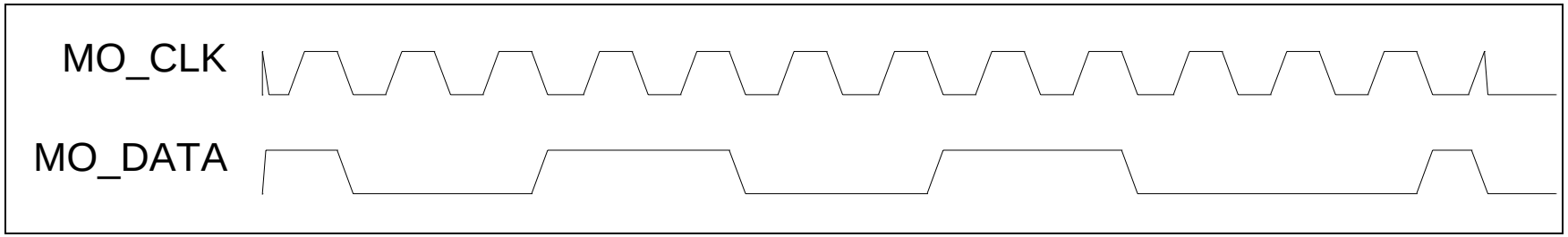


Figure 7 : R400EX System Management Interrupt Cycle Overview

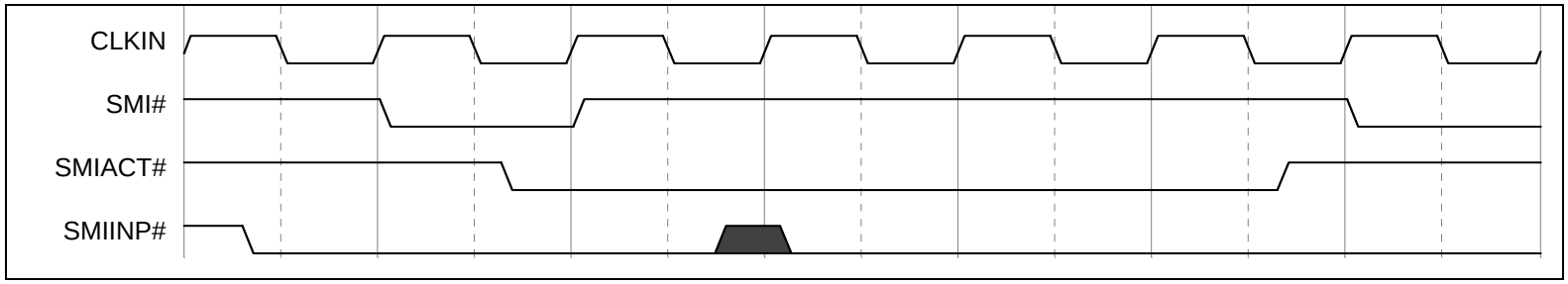


Figure 8A: R400EX I/O User Chip Select Access Overview

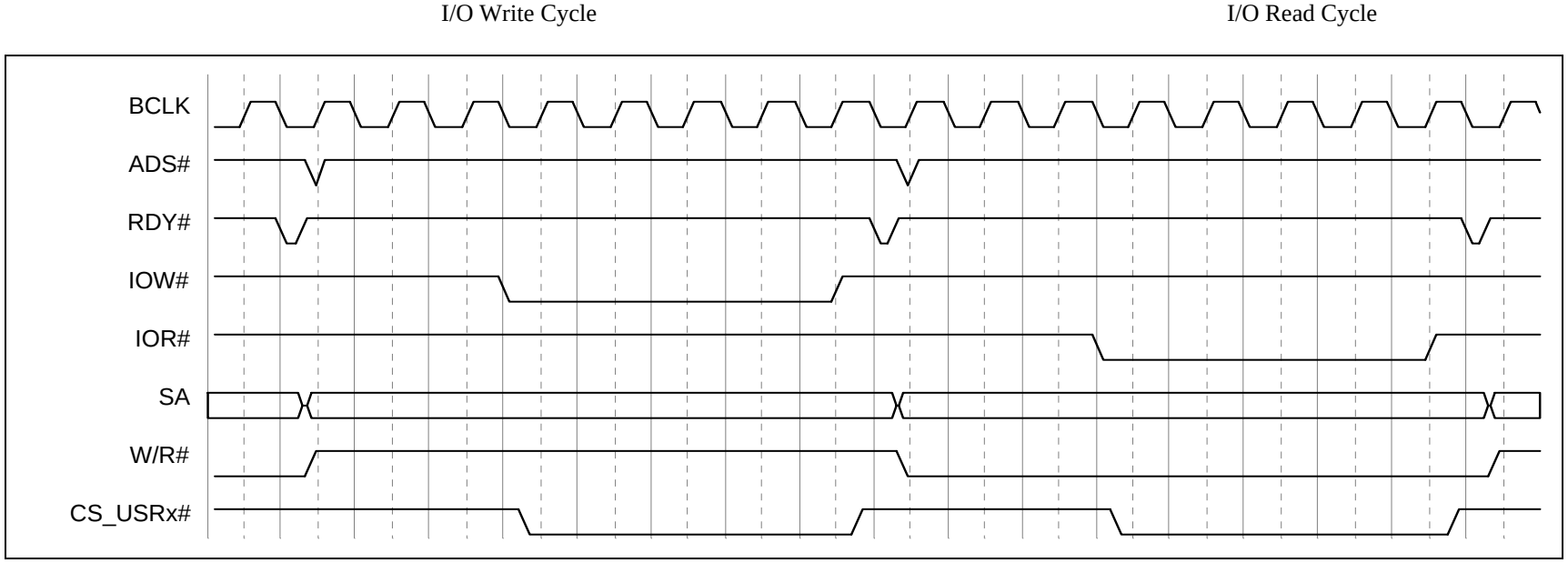


Figure 8B: R400EX Memory User Chip Select Access Overview

Memory Write Cycle Memory Read Cycle

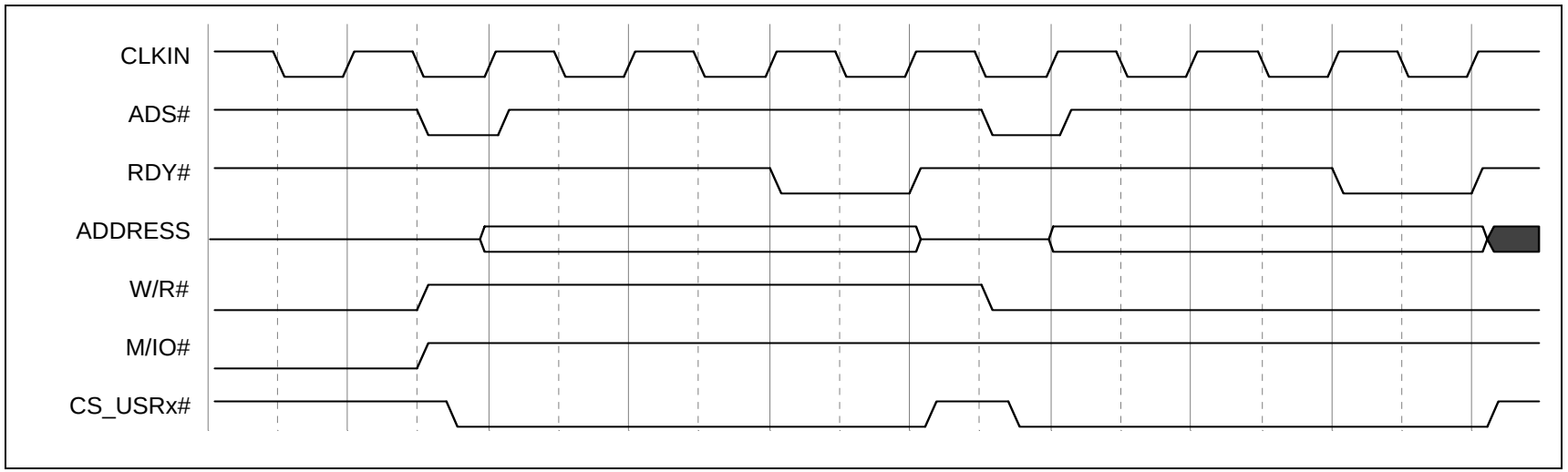


Figure 9 : R400EX AT Interrupt Acknowledge Cycle Overview

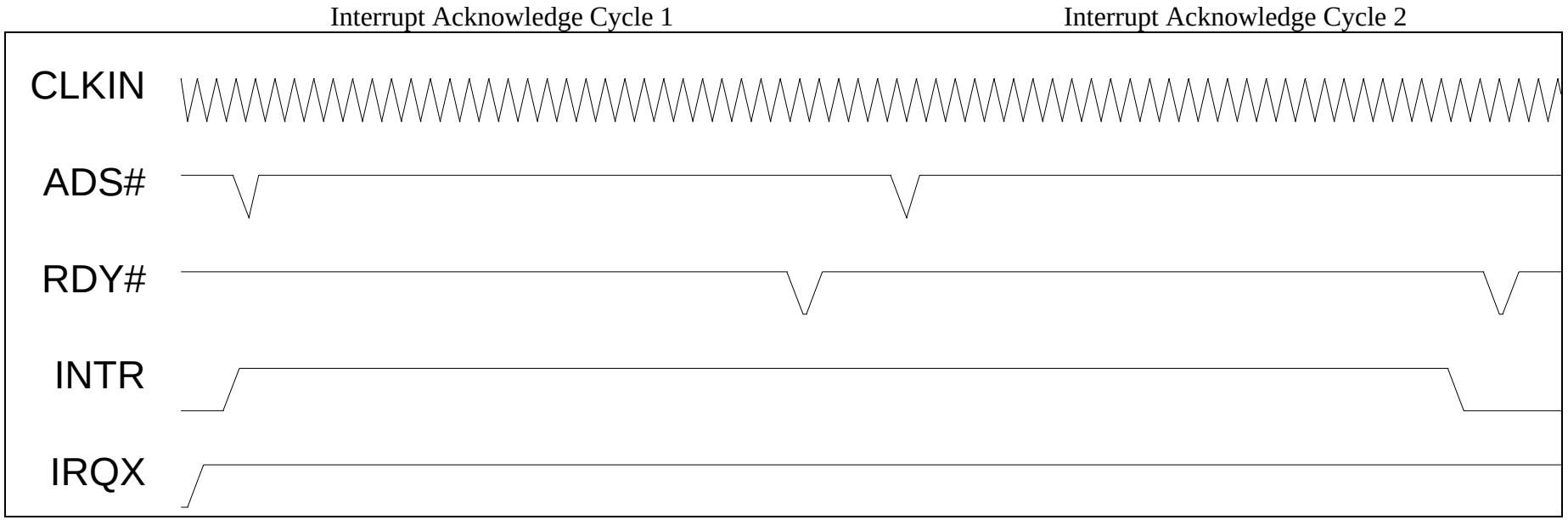


Figure 10A : R400EX IDE Mode0 and Mode3 Access Overview

Mode0 Write and Read Switching To Mode3 Mode3 Read and Write

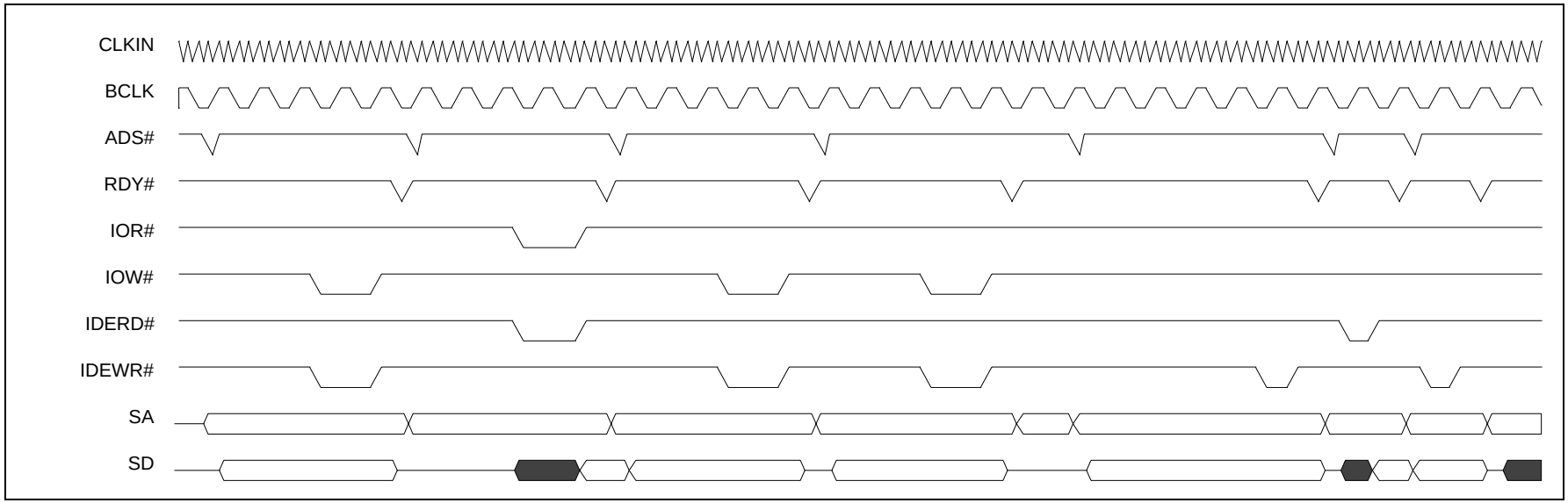


Figure 10B : R400EX IDE Mode4(33Mhz) and Mode4(50Mhz) Access Overview

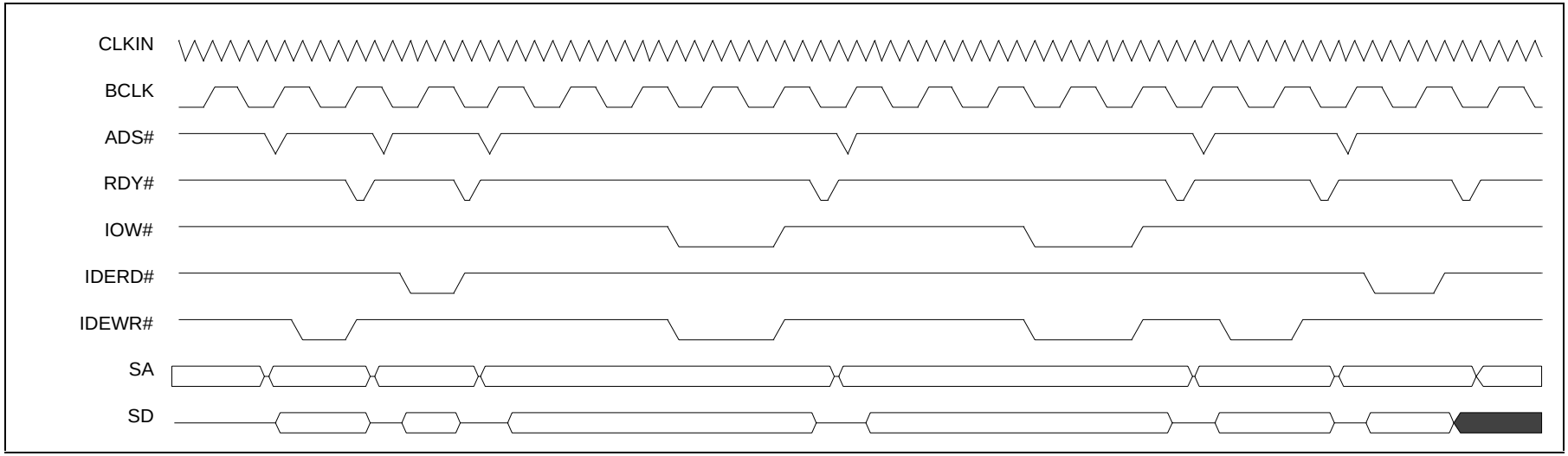
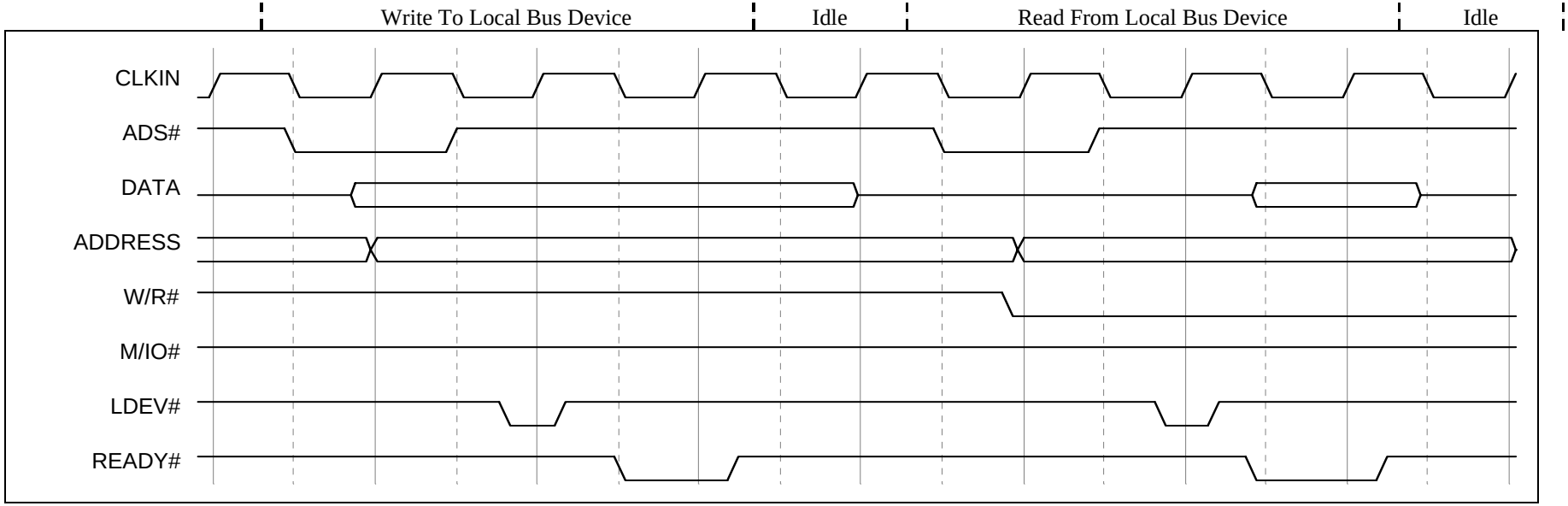


Figure 11 : R400EX Local Bus Device Access Overview



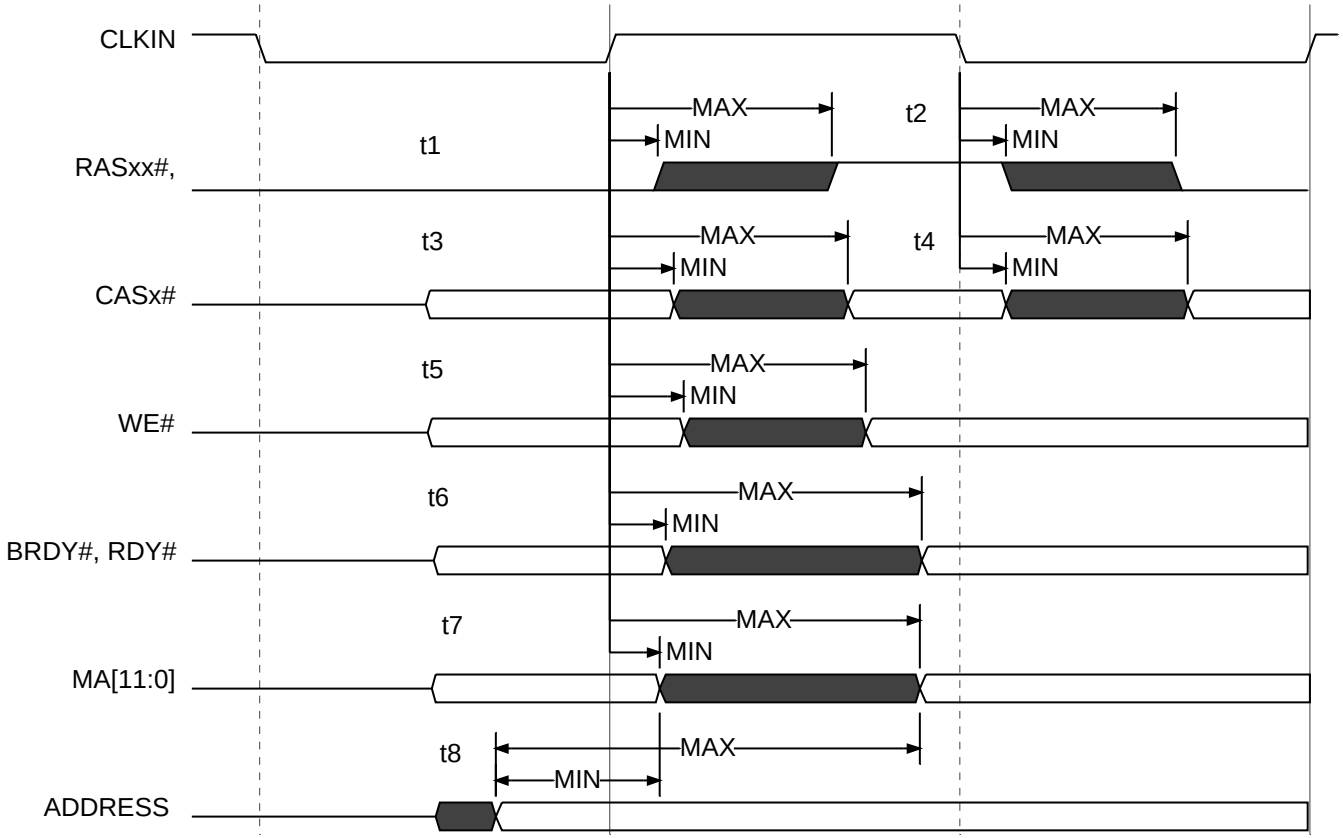


Figure 12: R400EX AC Timing Waveforms DRAM Signals Valid Delay Timing

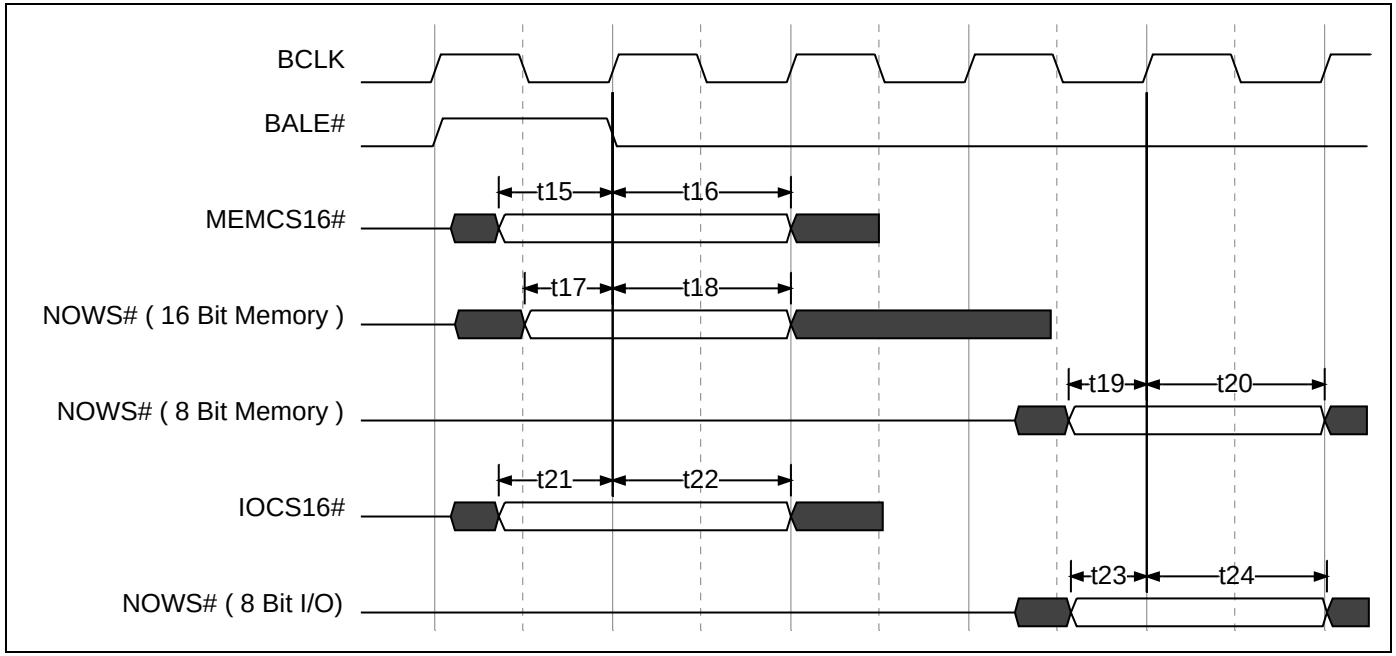


Figure 13: R400EX AC Timing Waveforms Input Setup and Hold Timing and ISA, IDE Valid Delay Timing

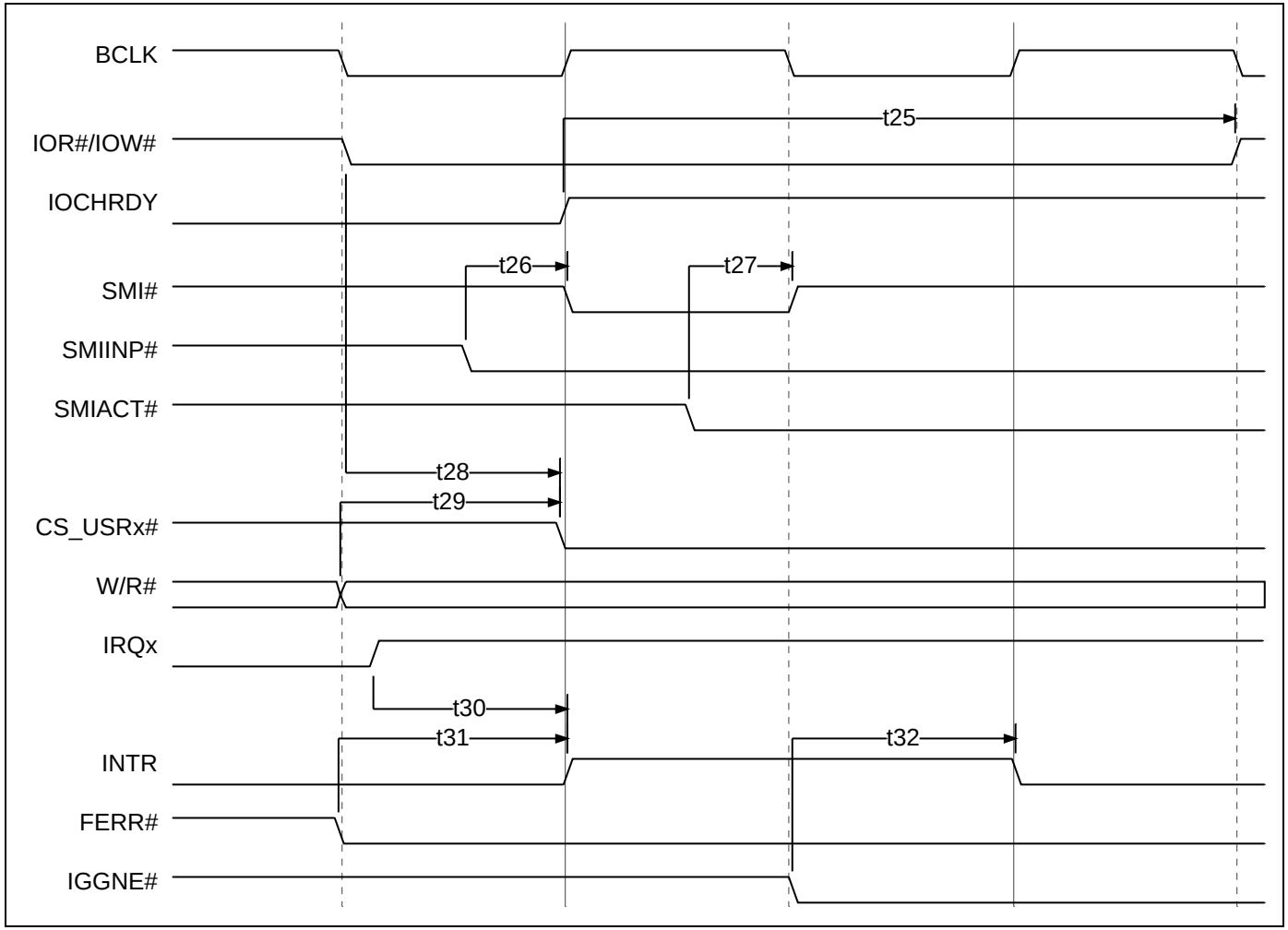


Figure 14: R400EX AC Timing Waveforms Relative Signal Timing