RadiSys R300EX Memory/Bus Controller

Complete DRAM interface and bus control all in one package

System Overview

The R300EX Memory/Bus Controller greatly simplifies Intel386 EX systems designed to run PC-oriented applications. RadiSys is committed to long term support for the R300EX, consistent with Intel's commitment to support of the Intel386 EX.

The R300EX is designed specifically for use with the Intel386 EX. It provides the support required by the Intel386 EX and its peripheral devices. This includes DRAM, Flash or EPROM control, Reset synchronization, Ready generation, data bus transceiver control, and support for the Synchronous Expansion Bus.

The DRAM controller includes address multiplexers, page hit logic for address pipelining, RAS and CAS generation, and refresh control.

The R300EX provides control signals for Flash memory, real time clock chips, IDE interface, and keyboard/mouse controller chips. It also generates a clock synchronized RESET signal for the Intel386 EX, and the READY# signal for non Local Bus Access cycles. Signals are generated for the Synchronous Expansion Bus (SEB), which is a subset of the ISA bus.

Additionally, a data buffer control signal is provided to prevent data bus contention that could result from direct use of the Intel386 EX RD# signal as the output enable for external devices.

R300EX Feature Summary

- Supports Intel386 EX A-Step, B-Step, and full 33MHz C-Step processors
- Pipelined, zero wait state, fast page mode DRAM controller for fast system response
- Complete support for 1, 2, 4, 8, and 16MB DRAM memory systems
- Integrated DRAM address multiplexers
- CAS before RAS refresh
- Support for Flash ROM, real time clock, IDE, and keyboard controllers
- 100 pin PQFP
- Integrated dynamic bus sizing and READY# generation minimizes external logic
- Reset - CLK synchronization for Intel386 EX
- Implements an ISA-subset, Synchronous Expansion Bus (SEB)
- Shutdown cycle - NMI generation circuit for PC-like shutdown cycle handling
- Fully tri-stateable with NAND-tree output for ATE (bed of nails) testing

Technical Overview:

Intel386 EX Processor Support

The R300EX supports the 5V Intel386 EX C-step device up through 33MHz. It also supports the 5V B-step device up through 25MHz. The 5V A-step is supported up through 25MHz with NA# not connected.

DRAM Control

The fast page mode DRAM controller provides complete support for 1, 2, 4, 8, and 16MB memory systems. The integrated page hit register enables the system to run zero wait states, rather than two, on a pipelined, same page access.

Systems using a 33MHz C-step version of the Intel386 EX processor need 60nS or better fast page mode DRAM. To run with a 25MHz B-step Intel386 EX, systems can use 70nS or better DRAMs.

The DRAM controller integrates the address multiplexers and CAS before RAS refresh circuitry to simplify system design.

Flash Control

Control logic provides support for Flash memory. The chip generates the proper write enable and chip selects to support programming of Boot Block Flash Memory systems. It also supports accessing the same Flash device at the top of both the 64M and the 1M address space.

Synchronous Expansion Bus

The Synchronous Expansion Bus (SEB) implements a functional subset of the ISA bus. It is intended to allow a selected set of peripherals to be used without implementing an entire ISA bus. The SEB is asynchronous from the peripherals point of view, but is generated synchronously to the Intel386 EX processor. The SEB includes:

- Intel386 EX processor address line A25-A1, BHE# and BLE#
- Buffered data bus D15-D0
- Command strobes, IOR#, IOW#, MEMR#, MEMW#, BALE
- Control input IOCHRDY, MEMCS16#, IOCS16#

The R300EX generates or recognizes:

- IOR#
- IOW#
- MEMR#
- MEMW#
- BALE#
- IOCS16#
- MEMCS16#
- IOCHRDY

SMEMR# and SMEMW# are not generated by the R300EX, but they can be easily generated from MEMR# and MEMW#. 0WS# is not supported.

Data Bus Sizing

The R300EX generates the BS8# signal used in conjunction with the dynamic bus sizing capability of the Intel386 EX processor. This capability provides the 16 bit to 8 bit conversion cycles that are necessary when an 8 bit device is accessed with a “word” bus cycle.

Wait States and Ready Generation

The R300EX generates READY# to terminate any bus cycle that is not an Intel386 EX local bus access. Those cycles that do not have LBA# active include “Halt/Shutdown” cycles, SEB and DRAM accesses, and Flash accesses below 1MB.

Wait states are generated as part of the READY# logic. Two wait states are inserted into Flash accesses. DRAM accesses vary in length from 0 to 2 wait states depending on the type of access (page hit or miss for example). “Halt/shutdown” and 16-bit SEB cycles are 8 CPU wait states, while 8-bit SEB cycles are 15 CPU wait states. This is the equivalent of 2 and 4 ISA wait states respectively. SEB accesses can be extended using IOCHRDY.

The R300EX drives READY# when LBA# is not active. It is forced high for the cycle immediately after it is sampled low by the CPU. Any time LBA# is active, the READY# output will be tri-stated.

Preventing Data Bus Contention

An integrated bus tracker state machine follows the CPU bus activity. The bus tracker generates a signal used to disable the data bus transceivers between the CPU and peripheral devices. This buffer eliminates the possibility of data bus contention when the CPU transitions from a read cycle to a write cycle. This signal disables the transceivers for all T1, T1P, and Ti cycles following T2 and T2P cycles.

CPU Shutdown Recognition

CPU Shutdown cycles are recognized by the R300EX, and it will assert the NMI signal in response. The NMI signal is released when the UCS# signal is detected. This allows the NMI service routine to handle shutdown cycles in a manner similar to PCs.

Real Time Clock Control

The R300EX generates the necessary AS and DS control signals to interface real time clock chips like the MC1468C18A to the Intel386 EX.

IDE Interface Control

Data bus control signals for an IDE interface are generated by the R300EX. The access time and bus size for IDE transfers are determined through the use of IOCS16#. These cycles run with the standard 8 or 15 wait states of the Synchronous Expansion Bus.

Keyboard/Mouse Controller Access

The R300EX generates ISA-like I/O read and write strobes for the keyboard/mouse controller which it expects to find on the local address and data buses. By configuring the Intel386 EX CS1# for I/O addresses 60h and 64h with zero wait states and external READY, these accesses will be run as 15 wait state, 8-bit SEB I/O cycles with the R300EX returning READY#.

CLK-Reset Synchronization

The RESET signal is generated from the CLK2 and PWRGD input signals. The RESET signal output to the Intel386 EX is synchronized with the rising edge of CLK2, and is also used internally to keep track of clock phase as part of the bus tracker state machine.

R300EX Package and Test Features

The R300EX comes in a 100 pin PQFP package, with an enhanced capability that eases system testing. All outputs are fully tri-stateable for use in conjunction with an internal NAND-Tree that links all of the pins back to a single output. Using a bed-of-nails ATE tester, and tri-stating the device, it is possible to verify that all of the pins on the device are connected to the circuit board.

The RadiSys Advantage

The RadiSys R300EX is a low cost component which greatly simplifies Intel386 EX systems that are designed to run PC oriented applications. As a company, RadiSys is committed to long term support for our products. Unlike designing with the short lived parts from the PC chipset commodity market, this RadiSys commitment makes designing with the R300EX a safe bet.

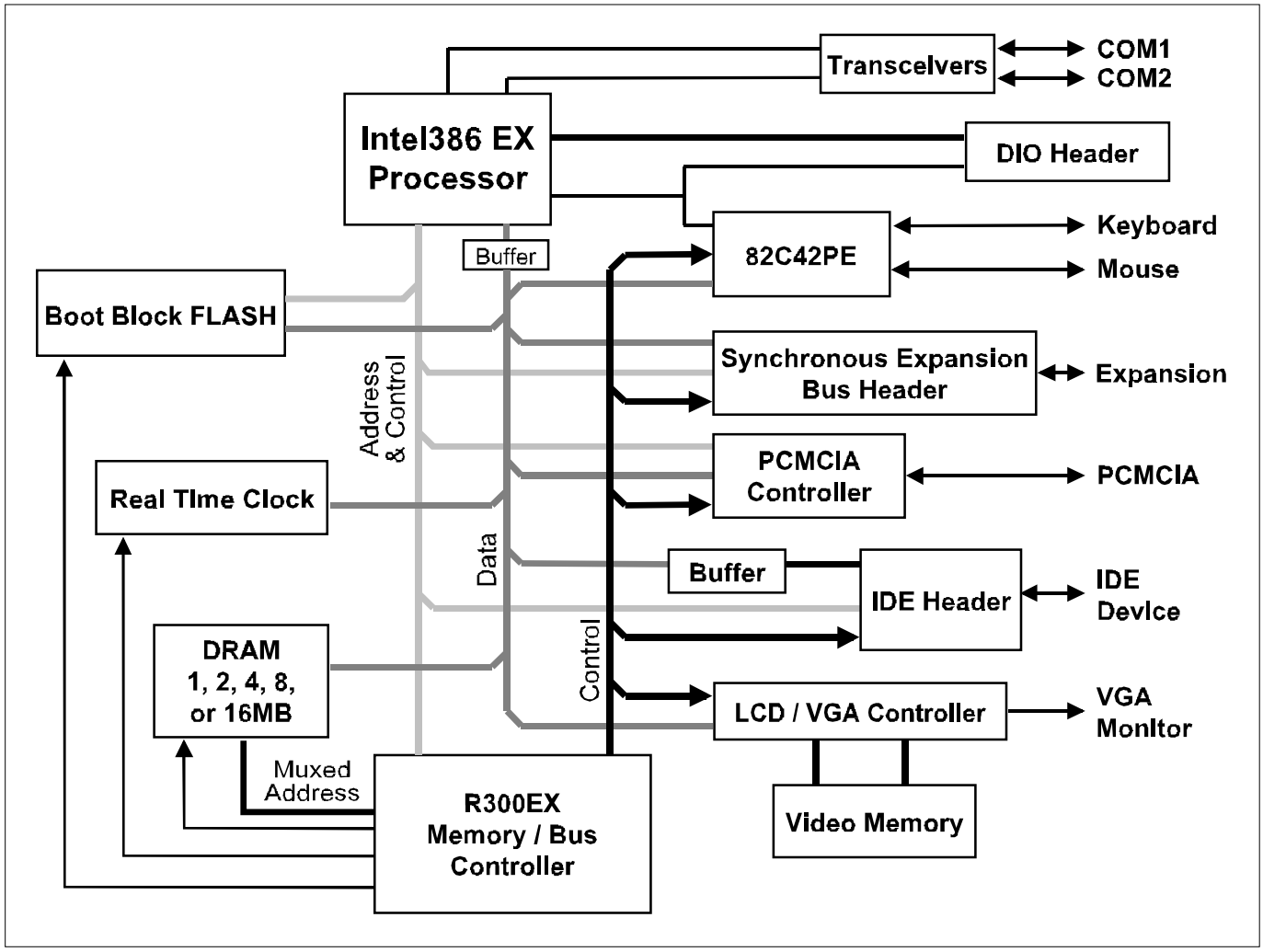


Figure 1: Example System using R300EX

Table 1: RadiSys R300EX Pin Definition

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	A9	26	A4	51	MA7	76	Vss
2	A8	27	CS3#	52	MA6	77	MA0
3	A11	28	Vss	53	Vdd	78	BALE
4	A21	29	A3	54	WE#	79	TEST
5	Vdd	30	A2	55	MA5	80	NC
6	CS1#	31	MA10	56	M/IO#	81	RTC_AS
7	A7	32	KBDCS#	57	MA4	82	NC
8	IOCHRDY	33	A14	58	BLE#	83	MEMW#
9	A6	34	A18	59	MEMCS16#	84	Vdd
10	FLSHA18	35	CASBH#	60	NAND_OUT	85	A22
11	IDE_ENL#	36	Vdd	61	Vss	86	A13
12	IDE_ENH#	37	A20	62	A10	87	IOW#
13	Vss	38	CASAH#	63	FLSHWE#	88	Vss
14	DATA_DE	39	D/C#	64	MA3	89	CLK2
15	FLSHCS#	40	Vss	65	MEMR#	90	LBA#
16	CS2#	41	Vdd	66	A23	91	Vss
17	A1	42	PWRGD	67	BS8#	92	A19
18	RAS#	43	RDY#	68	Vdd	93	Vdd
19	ONE_4MEG	44	MA9	69	RESET	94	CS5#
20	Vdd	45	Vss	70	NMI	95	CS4#
21	CASAL#	46	IOCS16#	71	RTC_DS	96	A16
22	A12	47	UCS#	72	MA2	97	Vss
23	NA#	48	MA8	73	A17	98	W/R#
24	A5	49	BHE#	74	MA1	99	ADS#
25	CASBL#	50	CS6#	75	I/OR#	100	A15

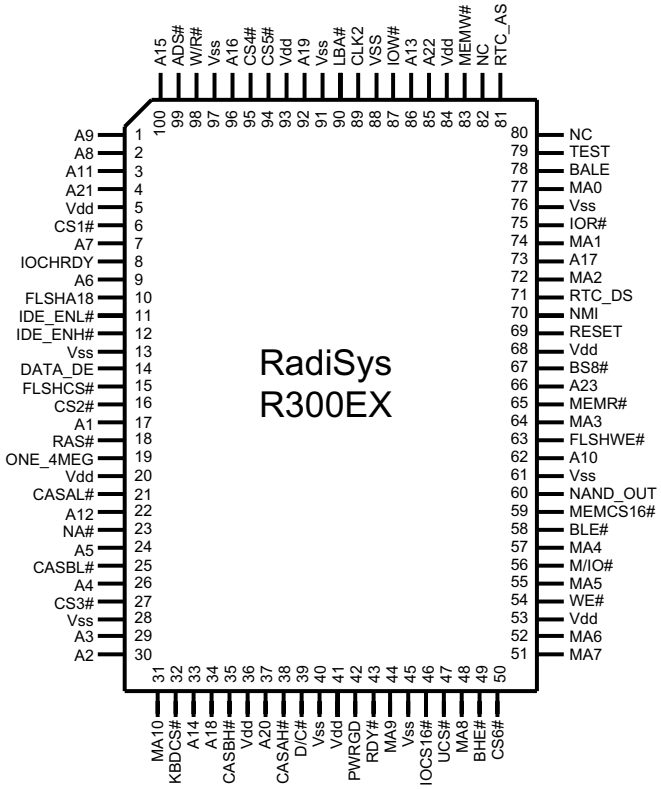


Figure 2: RadiSys R300EX 100 Pin PQFP Pin Assignment

Signal Definitions

Table 3: Signal Description Abbreviations

#	The named signal is active low
CMOS in	CMOS level input.
Schmitt	The input has a Schmitt trigger.
TTL in	TTL level input at 5V Vcc.
out	CMOS level output. All outputs except for the NAND pin are actually implemented as CMOS I/O for test purposes.
TS out	Tri-state CMOS level output.
power	Power pin
ground	Ground pin
CSR	output buffer has a controlled slew rate

Table 4: Clock and Reset Signals

Signal	Type	Drive Strength	Description
CLK2	CMOS in		**2x Input Oscillator:** This pin is the 2x input clock from the system oscillator. For systems that run at 25MHz bus cycles, the clock frequency is 50MHz.
PWRGD	Schmitt TTL in		**Power Good Input:** This signal is used to generate RESET.
RESET	out	8 mA	**CPU Reset:** This signal is the reset to the Intel386 EX. It is a clock synchronized version of PWRGD. RESET is used internally to set the phase of the bus tracker state machine to be consistent with the Intel386 EX internal clock phasing. This signal can drive up to 25pF on a system using a 66MHz CLK2 signal with guaranteed timing over the full temperature range. For a 50MHz CLK2 system, this increases to 50pF.

Table 5: Host Bus Interface Signals

Signal	Type	Drive Strength	Description
A[23:1]	TTL in		**Address Bus:** The address bus is connected directly to the Address lines of the Intel386 EX. Indicates, in conjunction with BHE# and BLE#, a physical memory or I/O address.
ADS#	TTL in		**Address Strobe:** This signal is connected to the Intel386 EX ADS# pin. Indicates a valid bus cycle definition and address. Signals A[23:1], W/R#, D/C#, M/IO#, BHE#, and BLE# are valid when ADS# is asserted.

Table 5 Continued

Signal	Type	Drive Strength	Description
BLE# BHE#	TTL in		**Byte Enables (Byte High Enable, Byte Low Enable):** Indicates which data bytes are valid. BHE# BLE# 0 0 word transfer 0 1 upper byte transfer (D[15:8])* 1 0 lower byte transfer 1 1 refresh cycle** * If BS8# is asserted then D[7:0] has the data. ** Intel 386 EX defines refresh cycles with a REFRESH# pin
M/IO# D/C# W/R#	TTL in		**Bus Cycle Definition Signals (Memory/IO, Data/Control, and Write/Read):** These three status signals define the current bus cycle type. **M/IO# D/C# W/R#** 0 0 0 Interrupt acknowledge cycle 0 0 1 Intel Reserved † 0 1 0 I/O data read 0 1 1 I/O data write 1 0 0 memory code read 1 0 1 halt or shutdown* 1 1 0 memory data read** 1 1 1 memory data write * For halt or shutdown cycles, the following applies: **A1** 0 Shutdown 1 Halt ** Intel 386 EX defines refresh cycles with a REFRESH# pin. † I/O Code Write cycles are sometimes used on microprocessor emulators to keep track of “branch take messages.”
CS1# CS2# CS3# CS4# CS5# CS6#	TTL in		**General Chip Selects 1 - 6:** CS1# is used to access the Keyboard/Mouse controller at I/O addresses 60h, and 64h. CS2# is used for Real Time Clock accesses at I/O addresses 70 - 71h CS3# is used to access IDE_CS1# at I/O addresses 3F6-3F7h. CS4# is used to access IDE_CS0# at I/O addresses 1F0-1F7h. CS5# is used to access DRAM. CS6# is used to access the Flash below 1MB
UCS#	TTL in		**Upper Chip Select:** UCS# is used to indicate an access to Flash at the top of memory.
LBA#	TTL in		**Local Bus Access:** This signal indicates that the Intel386 EX is doing a local bus access and will provide READY# to terminate the bus cycle. READY# will not be driven by the R300EX whenever LBA# is asserted.

Table 5 Continued

Signal	Type	Drive Strength	Description
READY#	TS TTL	4 mA	**Ready:** This bi-directional pin indicates that the current bus cycle is completed. The R300EX drives this pin to complete a bus cycle. This signal changes state 1/4 T-State, or one CLK2 phase, into the T-State, rather than at the beginning or middle of the T-State. The READY# signal is forced high for the cycle immediately after it is sampled low by the CPU. The only time that READY# is tri-stated is when the LBA# signal is active.
NA#	out	4 mA	**Next Address:** This signal is asserted to indicate that the R300EX can accept a new bus cycle definition. NA# will only be asserted during a DRAM cycle. The A-step Intel386 EX does not support pipelining, so the CPU's NA# input must be pulled high and not connected to the R300EX NA# output.
BS8#	out	4 mA	**Bus Size 8:** This signal is driven low during access to an 8-bit peripheral. It is asserted 3/4 T-State, or three CLK2 phases, into the T-State, and is deasserted 1/4 T-State, or one CLK2 phase into the T-State, rather than at the beginning or middle of the T-State. This signal must be driven externally if an 8-bit boot memory is used.

Table 6: DRAM Interface Signals

Signal	Type	Drive Strength	Description
MA[10:0]	TTL	8 mA CSR	**Memory Address:** 1MB, 4MB and 16MB DRAM is usually organized as 2 banks, 16 bits wide. A19 is used to select the bank (CASAx# or, CASBx#) for 1MB and 4MB cases. A23 is used to select the bank for the 16MB case. 2MB and 8MB DRAM typically have only one bank, thus they should be configured to use A23 bank selection. During operation these signals provide a 22-bit multiplexed DRAM memory address output as shown below. (Mux = Col or Row) MA10 = A22 or A21 MA9 = A21 or A20 if ONE_4MEG is high or MA9 = A19 or A20 if ONE_4MEG is low MA8 = A18 or A9 MA7 = A17 or A8 MA6 = A16 or A7 MA5 = A15 or A6 MA4 = A14 or A5 MA3 = A13 or A4 MA2 = A12 or A3 MA1 = A11 or A2 MA0 = A10 or A1

Table 6 Continued

Signal	Type	Drive Strength	Description
CASAL# CASAH# CASBL# CASBH#	out	8 mA	**Column Address Strobe:** These signals are used to strobe the column address into the two banks of fast page mode DRAM. CASAL# or CASBL# enables access to the low order byte and CASAH# or CASBH# enables access to the high order byte. CASAx# accesses the first bank, and CASBx# accesses the second bank.
RAS#	out	8 mA	**Row Address Strobe:** This signal is used to strobe the row address into the DRAM.
WE#	out	8 mA	**DRAM Write Enable:** This signal in conjunction with RAS, CASAx# and CASBx# causes a write to occur to the DRAM.
ONE_4MEG	TTL in		**One Meg / 4 Meg Memory Selection:** This signal is used to select the appropriate DRAM multiplexing scheme. Total DRAM supported is 1, 2, 4, 8, or 16MB. For 1MB, or 4MB configurations, ONE_4MEG must be high. For 2MB, 8MB, or 16MB configurations ONE_4MEG must be low.

Table 7: Synchronous Expansion Bus Interface Signals

Signal	Type	Drive Strength	Description
BALE	out	4 mA	**Address Latch Enable:** This signal is used to latch valid addresses and memory decodes from the microprocessor. It indicators a valid microprocessor address.
IOR#	out	8 mA	**I/O Read Strobe:** This signal instructs an I/O device, if selected, to drive its data onto the data bus.
IOW#	out	8 mA	**I/O Write Strobe:** This signal instructs an I/O device, if selected, to read the data off the data bus.
MEMR#	out	8 mA	**Memory Read Strobe:** This signal instructs a memory device, if selected, to drive its data onto the data bus.
MEMW#	out	8 mA	**Memory Write Strobe:** This signal instructs a memory device, if selected, to read the data off the data bus.

Table 7 Continued

Signal	Type	Drive Strength	Description
IOCHRDY	TTL in		**I/O Channel Ready:** This signal is negated (pulled low or not ready) by a memory or I/O device to lengthen I/O or memory cycles. Any slow device using this line should negate it immediately upon detecting its valid address and a Read or Write command. Machine cycles are extended by an integral number of T-states (two CLK2 cycles). This signal should not be held negated for more than 15 microseconds or memory refresh will not occur. This signal is synchronized and sampled in the middle of SEB state 13, and will be sampled again in the middle of each subsequent SEB wait state (T-state). This signal should pulled-up or driven externally.
MEMCS16#	TTL in		**Memory Cycle is 16 bits:** This signal indicates that the current SEB memory cycle is a 16-bit transfer.
IOCS16#	TTL in		**I/O Cycle is 16 bits:** This signal indicates that the current SEB I/O cycle is a 16-bit transfer.

Table 8: Real Time Clock Interface Signals

Signal	Type	Drive Strength	Description
RTC_AS	out	4 mA	**Real Time Clock Address Strobe:** This signal is used to latch the address for an external Real Time Clock. This signal is asserted when CS2#, BLE#, and IOW# are all asserted.
RTC_DS	out	4 mA	**Real Time Clock Data Strobe:** This signal is used to latch the Data for an external Real Time Clock. This signal is asserted when CS2#, BHE#, and IOR# or IOW# are all asserted and BLE# is not asserted.

Table 9: Flash Interface Signals

Signal	Type	Drive Strength	Description
FLSHA18	out	4 mA	**FLASH A18:** This signal is used as the most significant address bit of the Flash memory device. When UCS# is asserted (e.g. at the top of the full address space), FLSHA18 is the normal version of the A18 input pin. When CS6# is asserted (e.g. at the top of the 1M address space), FLSHA18 is the inverted version of the A18 input pin.

Table 9 Continued

Signal	Type	Drive Strength	Description
FLSHCS#	out	8 mA	**FLASH Chip Select:** This signal is the Flash Memory Chip Enable.
FLSHWE#	out	8 mA	**FLASH Write Enable:** This signal is the Flash Memory Write Enable.

Table 10: Keyboard Interface Signals

Signal	Type	Drive Strength	Description
KBDCS#	out	4 mA	**Keyboard/Mouse Controller Chip Select:** This signal is the Keyboard/Mouse Controller Chip Select. This signal is asserted when CS1# and BLE# are asserted, and BHE# is not asserted.

Table 11: IDE and Miscellaneous Signals

Signal	Type	Drive Strength	Description
IDE_ENH#	out	4 mA	**IDE Enable High:** This signal enables the high-byte data buffer in an IDE interface. This signal is asserted when CS4#, IOCS16#, and IOR# or IOW# are all asserted
IDE_ENL#	out	4 mA	**IDE Enable Low:** This signal enables the low-byte data buffer in an IDE interface. This signal is asserted when CS4# or CS3#, and IOR# or IOW# are asserted
DATA_DE	out	8 mA	**Data Buffer Disable:** This signal is used to disable data buffers between the CPU and peripheral devices for all T1, T1P and Ti cycles. This buffer eliminates the possibility of data bus contention when the CPU transitions from a read cycle to a write cycle. This signal is active for one full T-State after every READY#. DATA_DE is asserted high, and can be fed directly into the asserted low output enable on a tri-state buffer.
NMI	out	4 mA	**Non-Maskable Interrupt:** The NMI signal is asserted when a Shutdown cycle is recognized. It is de-asserted by the next assertion of UCS#.
TEST	TTL in		**Test Mode:** This signal places the R300EX into test mode. All outputs except NAND_OUT are tri-stated. This signal must be pulled down for normal operation.

Table 11 Continued

Signal	Type	Drive Strength	Description
NAND_OUT	out	4 mA	**NAND Tree Out:** This pin is the output of a NAND chain connecting all other package pins except for no-connect and power pins. It allows parametric testing of all inputs, and functional testing of all other signals.
NC			**No Connect:** This pin is not connected to any internal function. It has no bond wire from the die to the package. It can be tied high, low, or left floating..
Vdd	Power		**Positive Voltage Input** This pin is connected to the 5 Volt ±10% supply.
Vss	Power		**Negative Voltage Input** This pin is connected to the return ground supply.

FUNCTIONAL DESCRIPTION

Clock, Power Good, and Reset

The R300EX generates the RESET output by synchronizing the Power Good signal (PWRGD) to the CLK2 input signal. The CLK2 input must be the same clock and phasing as the CLK2 signal provided to the Intel386 EX. The RESET signal also synchronizes the R300EX internal bus tracker state machine with the internal state of the Intel386 EX, thus enabling it to follow the state of the CPU. The PWRGD signal has a Schmitt trigger input. The RESET signal has an 8 mA drive capability.

Host Bus Interface

The host bus interface signals connect the Intel386 EX to the RadiSys R300EX. The address from the CPU is qualified by the address strobe (ADS#), byte enables (BHE#, BLE#), cycle type indicator (M/IO#, D/C#, W/R#), chip selects (CS[1..6]# and UCS#), and the local bus access (LBA#) signals to determine the response of the R300EX.

The R300EX generates the READY# signal for all non-local bus addresses. This prevents a bus “hang” which can occur when “polling” to determine the existence of a resource. The READY# signal is forced high for the cycle immediately after it is sampled low by the CPU. The only time that READY# is tri-stated is when the LBA# signal is active. It should be noted that the LBA# signal timing has changed with the release of the C-Step Intel386 EX. This change is noted in the timing diagram for Flash memory accesses shown later in this document.

The Flash memory devices used must be in a “by 16” configuration unless external logic is used to generate BS8# for UCS# accesses. The Flash devices must have 80nS (or better) access time for use in a 25MHz system, and 60nS (or better) for use in a 33MHz system. The Flash device should be a 2Mb or a 4Mb part.

A DRAM access will result in the assertion of the NA# signal. After the first read, a subsequent DRAM read that has the same row address will result in a page hit. This results in a zero wait state, rather than a two wait state, DRAM access. The page hit condition will continue until there is an access outside the DRAM page, an idle bus cycle, or a refresh cycle is started by the Intel386 EX. A refresh cycle is indicated by ADS# being asserted without either BHE# or BLE# being asserted.

The R300EX accommodates both Intel386 EX internal and external I/O mapped peripherals. The internal peripheral accesses are recognized from the assertion of the LBA# signal. LBA# cycles are completely controlled by the Intel386 EX. These cycles are indicated by the assertion of LBA# from the Intel386 EX. The Intel386 EX generates READY# for LBA# cycles. Some external devices require the use of a chip select while others perform the address decode themselves. Those devices specifically handled by the R300EX are shown in Table 2.

The R300EX will assert BS8# each time a non-LBA#, 8-bit access is detected. This includes those devices specifically limited to 8-bits, as defined in Table 2, as well as those devices on the which do not return MEMCS16#, or IOCS16#.

The R300EX expects the General Chip Select configuration shown in Table 2. If some functions supported by these CSx# pin inputs are not needed in the system design, then these input pins may be tied high (deasserted). This allows the

corresponding CSx# pins on the Intel386 EX to be used for some other system function. For example, if an IDE drive is not needed in the system design, then the CS3# and CS4# R300EX pins may be tied high, and the Intel386 EX CS3# and CS4# pins may be programmed to some other chip select address range.

Table 12. Expected Chip Select Utilization

Chip Select	Address Type	Device	Expected Address Range(HEX)	Wait States	Data Width	Notes
CS1#	I/O	Keyboard / Mouse Controller	0060, 0064	15d	8	(1)
CS2#	I/O	Real Time Clock	0070-0071	15d	8	(1)
CS3#	I/O	IDE_CS1#	03F6-03F7	15d	8	(1)
CS4#	I/O	IDE_CS0#	01F0-01F7	8/15d	8/16	(1, 2)
CS5#	Memory	1MB DRAM	0000000-00FFFFF	0, 1, 2	16	
		2MB DRAM	0000000-01FFFFF			
		4MB DRAM	0000000-03FFFFF			
		8MB DRAM	0000000-07FFFFF			
		16MB DRAM	0000000-0FFFFFF			
CS6#	Memory	128KB FLASH	00E0000-00FFFFF	2	16	(3)
		256KB FLASH	00C0000-00FFFFF			
UCS#	Memory	512KB FLASH	3F80000-3FFFFFF	2	16	(4)
none	Memory	Synchronous Expansion Bus	00A0000-00DFFFF 00A0000-00BFFFF	8/15	16/8	(1, 2, 3)

Notes:

1) Default cycles are 15 wait states for 8-bit and 8 wait states for 16-bit. The Intel386 EX chip select register should be programmed to 0 wait states with external Ready.
2) The R300EX forces 8 bit cycles, with BS8#, if external logic does not assert MEMCS16#.
3) CS6# and SEB accesses in the range 00A0000-00FFFFF are complementary. If 128KB FLASH is selected from 00E0000-00FFFFF then the SEB is accessed from 00A0000-00DFFFF. If the 256KB FLASH is selected from 00C0000-00FFFFF then the SEB is accessed from 00A0000-00BFFFF.
4) At power-on the Intel386 EX uses 15 wait states and generates READY#.

It should be noted that the DRAM chip select will overlap the CS6# and the SEB area in the lower 1MB of the memory map. The R300EX will inhibit DRAM accesses for 00A0000h-00FFFFFh and enable the SEB to be accessed in this region when CS6# is not active. When CS6# is active, it generates two wait state Flash accesses.

Memory Map

The diagram below shows the suggested memory map for systems utilizing the R300EX.

Note that all memory accesses to areas above CS5# (DRAM) but below UCS# are directed to the SEB. This allows the flexibility to access a VGA controller or a PCMCIA controller for example, in extended memory when utilizing 16MB of DRAM.

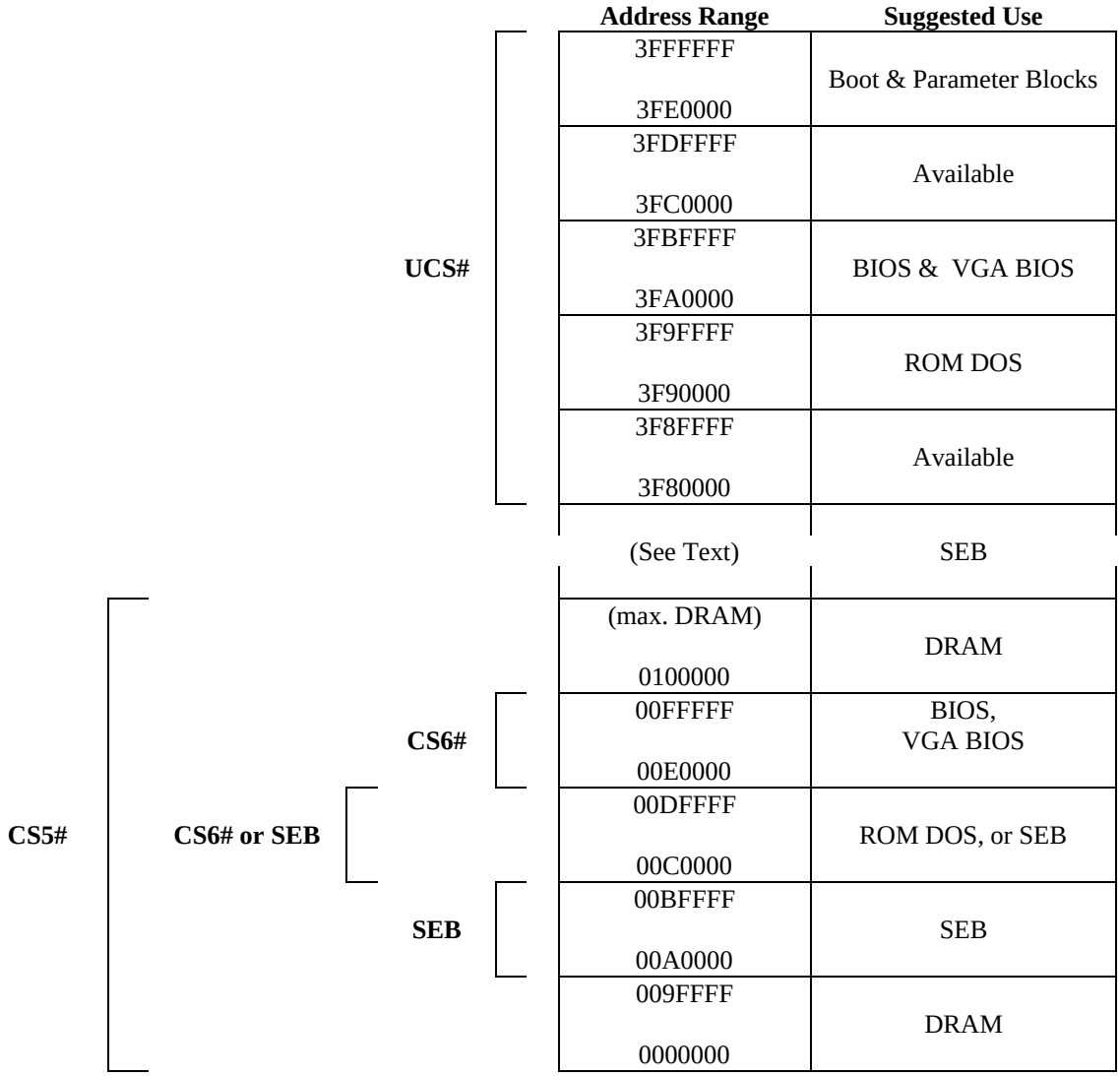


Figure 3. Suggested System Memory Map

Halt or Shutdown Cycles

Halt cycles are terminated by the R300EX by returning READY#. No other action is taken. Shutdown cycles initiate a software based reset by asserting NMI. It is expected that the BIOS will handle the NMI and reset the CPU through port 92 internal to the Intel386 EX. The NMI will be deasserted upon detection of the next UCS# assertion.

DRAM Interface

The R300EX includes a DRAM controller with built in address multiplexers and supports 1MB, 2MB, 4MB, 8MB or 16MB DRAM. Fast page mode DRAM is required. The DRAM should be autosized by the BIOS on boot-up. Cycles can be either 8- or 16-bit. Cycles are terminated with the assertion of READY#. The 2MB and 8MB DRAM must be configured for a single RAS# and only 2 CAS# signals (CASAL# and CASAH#). This point requires careful attention because many 2MB and 8MB DRAM SIMMs require 2 RAS# signals and 4 CAS#. One exception to this is a 512K x 32 memory built from asymmetrically addressed DRAMs as is discussed below.

The addresses from the Intel386 EX are taken in on A[23:1] and are multiplexed onto MA[10:0] with the proper timing for the row and column address selection of the DRAM memory chips. These MA addresses along with the RAS# and CASxx# signals select the proper data from the memory. The mapping of A[23:1] to MA[10:0] depends upon the ONE_4MEG input signal as shown in Table 3. The MA signals use 8 mA controlled slew rate outputs and should not normally need external series termination resistors.

Table 13: Address To Multiplexed Address Mapping Based Upon ONE_4MEG Signal

	ONE_4MEG = High (for 1MB or 4MB)		ONE_4MEG = Low (for 2MB, 8MB or 16MB)	
Multiplexed	Row	Column	Row	Column
MA10	A22	A21	A22	A21
MA9	A20	A21	A20	A19
MA8	A18	A9	A18	A9
MA7	A17	A8	A17	A8
MA6	A16	A7	A16	A7
MA5	A15	A6	A15	A6
MA4	A14	A5	A14	A5
MA3	A13	A4	A13	A4
MA2	A12	A3	A12	A3
MA1	A11	A2	A11	A2
MA0	A10	A1	A10	A1

The DRAM address multiplexing function supports symmetrically addressed fast page mode DRAM. Note that 1MB, 4MB and 16MB DRAM SIMMs are usually organized as 2 banks, 16 bits wide, while 2MB and 8MB DRAM SIMMs often have only one 16-bit wide bank.

For 1MB or 4MB configurations the ONE_4MEG signal must be high so that A19 is used to select the bank (CASAx# or, CASBx#). For 2MB, 8MB or 16MB configurations the ONE_4MEG signal must be low so that A23 is used to select the bank.

In addition, 2 bank 512K x 16 (512K x 32) DRAM modules built from 512K x 8 asymmetrically addressed (10 Row - 9 Column) DRAMs can also be supported by tying the ONE_4MEG pin high, even though this is 2MB of DRAM.

One RAS and four CAS strobes are generated by the R300EX. The four CAS signals select from the two banks and the two bytes of the word wide DRAM. CASAH# selects the high byte of DRAM bank A. CASAL# selects the low byte of DRAM bank A. CASBH# selects the high byte of DRAM bank B. CASBL# selects the low byte of DRAM bank B. Both CASxH# and CASxL# from one bank can be active at the same time, thus selecting the entire word.

On write cycles the WE# signal works with the CASxx# signals to cause a write to occur to the DRAM.

Address pipelining is only available for DRAM accesses. The use of pipelining depends upon the upper addresses bits matching between subsequential back-to-back DRAM accesses. If the current cycle is a DRAM access, then the NA# signal will be asserted, requesting that the next address and cycle type be pipelined onto the bus. If the upper bits of the next address match the upper bits of the current address, then the RAS# signal is left asserted, and CASxx# will start the next DRAM access. This results in a zero wait state DRAM read cycle. If the next DRAM access is a write, then CASxx# will be delayed by one T-state (two CLK2 cycles), and then the DRAM access will be started by CASxx#. The wait states required for various accesses are shown in Table 4.

DRAM refresh cycles are recognized from the assertion of ADS# with neither BHE# or BLE# asserted. When the R300EX sees this condition, it transitions into the DRAM refresh mode and asserts all four CASxx# signals before asserting RAS# thereby initiating a DRAM refresh using the DRAM's internal refresh address counter.

Table 14: DRAM Accesses and Wait States

State	Non-Pipelined	Pipelined	Reason
RAS# already off	2 Wait States		RAS# off after a refresh or non DRAM access.
Page miss		2 Wait states	RAS# precharge required.
Read page hit		0 Wait states	CASxx# only access.
Write page hit		1 Wait state	CASxx# only access. Wait state required to guarantee write access time.

The DRAM State Machine state diagram is shown below.

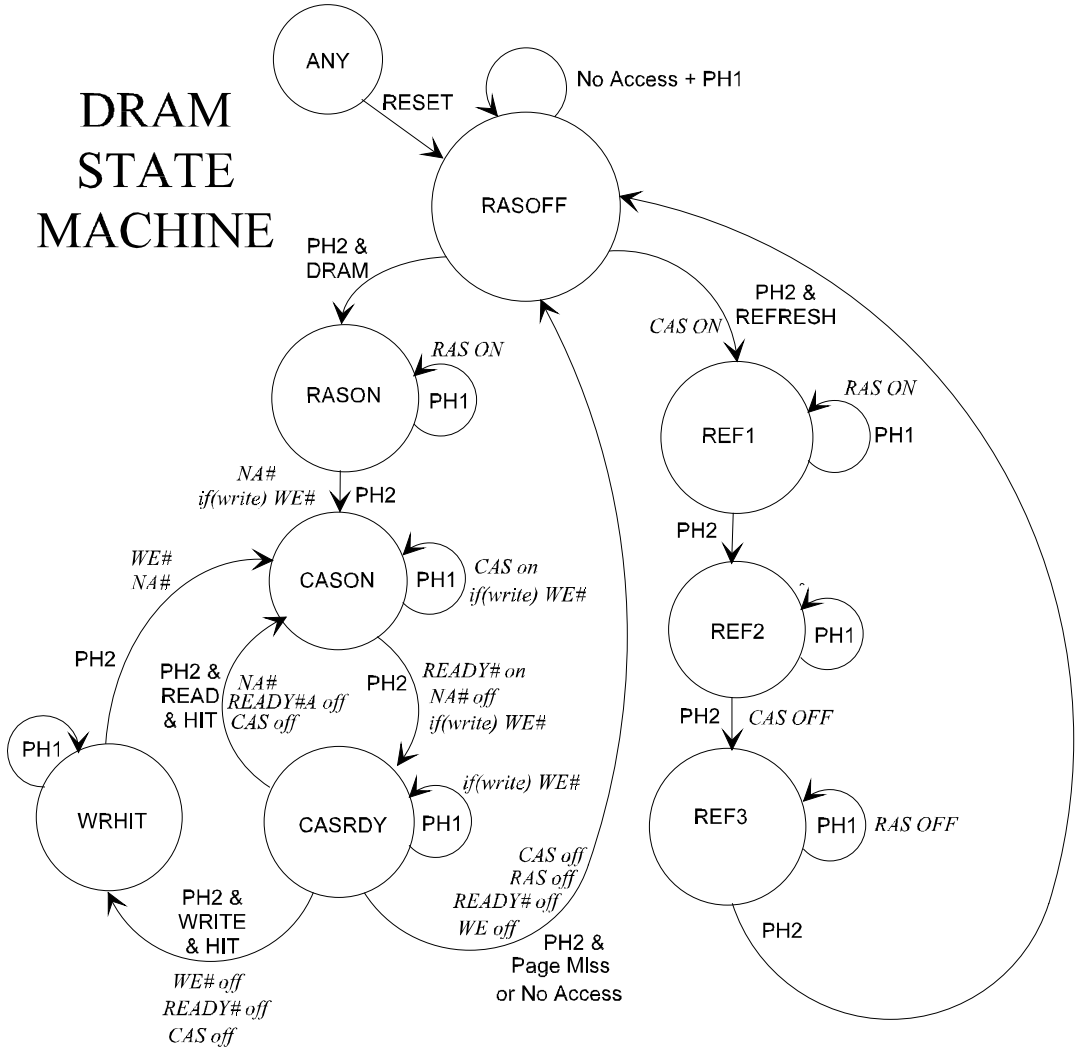


Figure 4: DRAM State Machine

Note:

1. The signals in *italics* with “on” and “off” indicate when the named output signal is asserted or de-asserted. The signal stays in its current state unless explicitly changed as noted by “on” or “off”.

2. The BHE# and BLE# signals are tested to determine if a DRAM cycle is a refresh cycle, or a read/write cycle.

3. The multiplexed address pins follow the row address in the RASOFF and RASON states. They follow the column address in all other states.

Synchronous Expansion Bus Interface Signals

The Synchronous Expansion Bus contains a subset of the ISA bus. The R300EX generates cycles on the SEB for memory and I/O cycles that are not mapped to devices on the local bus, or internal to the processor chip itself. The controller supports 8- and 16-bit transfers, including translation for 16-bit requests from the CPU to 8-bit devices, and 8-bit requests to 16-bit devices. The R300EX does not expand the interrupt and DMA capabilities of the Intel386 EX. Thus the interrupt and DMA channels available are exactly those of the Intel386 EX.

Valid addresses on the SEB are indicated by BALE. This signal can be used to latch the current address, if necessary, and start the decode process to determine if assertion of MEMCS16#, IOCS16#, or IOCHRDY is required.

The assertion of MEMR# or MEMW# indicate a memory address. If the addressed memory device handles 16-bit data, then it needs to assert MEMCS16#. If it does not, it will be accessed as an 8-bit device, and a second 8-bit cycle will be run to complete a 16-bit transfer. The R300EX does not generate refresh cycles for the SEB bus.

SMEMR# and SMEMW# may be generated, if necessary, by ANDing a “LOWMEMCS” (below one megabyte address decode) with the respective memory strobe. This can be done using either an unused Intel386 EX chip select or external address decoding.

The assertion of IOR# or IOW# indicate that the address bus has an I/O address. If the addressed I/O device handles 16-bit data, then it needs to assert IOCS16#. If it does not, it will be accessed as an 8-bit device, and a second 8-bit cycle will be run to complete a 16-bit transfer.

IOCHRDY is negated (pulled low or not ready) by a memory or I/O device to lengthen memory or I/O cycles. Any slow device using this line should negate it immediately upon detecting its valid address and a read or write command. Machine cycles are extended by an integral number of T-States. This signal should not be held negated for more than 15 microseconds or memory refresh will not occur.

It should be noted that while the SEB is ISA-bus-like, some of the timing characteristics are slightly different, and should be carefully studied to avoid any “unpleasant surprises”. Figure 4 below shows the SEB state diagram. As can be seen from the state diagram, MEMCS16# and IOCS16# are sampled at the end of state 5, and IOCHRDY is sampled at the end of state 13.

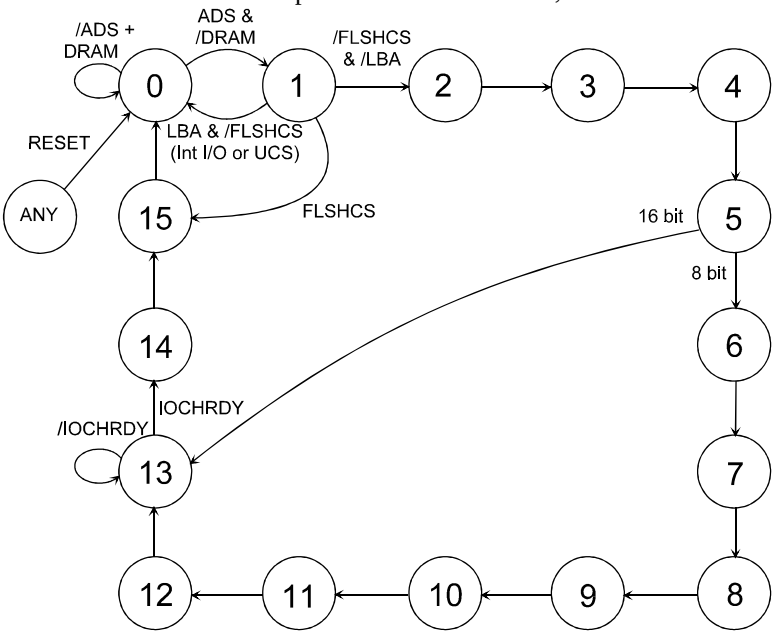


Figure 5: SEB State Machine

Notes:

1. FLSHCS# = CS6# + UCS#

2. A transition from state #0 to state #1 occurs at the end of any T1 or T1P that is not directed to DRAM.

3. LBA# is checked at the end of state #1 to identify internal Intel386 EX processor I/O accesses and non-flash accesses (the CPU generates the RDY#) and returns the state machine to state #0 to await the next bus cycle. Accesses to Flash with CS6# or UCS# send the state machine to state #15, providing 2 Wait States. All other cycles are directed to the SEB.

4. BALE is asserted at the beginning of state #1 and will be deasserted at the end of state #1 if the next state is either state #0 or state #15 (LBA# active). If the next state is state #2 (LBA# inactive), then BALE will be deasserted in the middle of that state (LBA# inactive).

5. In state #5, IOCS16# or MEMCS16# is sampled to determine whether the access is to an 8 or 16 bit device to adjust the wait states.

6. At state #13, the clock synchronized version of IOCHRDY is sampled to allow the accessed device to extend the cycle.

7. RDY# is set active at the end of state #15 for one T-state. RDY# changes state 1/4 T-State, or one CLK2 phase, into the T-State, rather than at the beginning or middle of the T-State.

8. IOR# and MEMR# are asserted at the end of state #2. They are deasserted at the end of the first state #0 following state #15. IOW# and MEMW# are asserted at the end of state #2. They are deasserted at the end of state #15.

The dynamic bus sizing capability of the Intel386 EX processor, via the BS8# signal, is used to provide the 16 bit to 8 bit conversion cycles when an 8 bit device is accessed with a “word” bus cycle.

BALE is set active at the beginning of state #1 and is de-asserted at the end of state #1 (LBA# active) or in the middle of state #2 (LBA# inactive). The appropriate SEB command strobe (MEMR#, MEMW#, IOR# or IOW#) is set active at the beginning of state #3. The read strobes are held active until the end of state #0 while the write strobes are de-asserted at the end of state #15 to insure the required data and address hold time. Ready is asserted at the transition from state #15 to state #0, and is deasserted one T-state (two CLK2’s) later.

Real Time Clock Interface Signals

The Real Time Clock interface is through two signals: RTC_AS and RTC_DS. These are the address strobe and data strobe signals for interfacing to a real time clock chip such as the MC1468C18A, or Dallas Semiconductor DS1287. These signals provide all of the correct timing for accessing the RTC chip, and are generated in response to CS2#. Cycles accessing the RTC conform to the basic SEB timing.

Flash Interface Signals

The interface to the Flash memory is made up of three signals: FLSHA18, FLSHCS#, and FLSHWE#. The FLASHA18# signal is used as the most significant address bit of the Flash memory device, in place of A18 directly from the CPU. When UCS# is asserted (i.e. at the top of the full address space), FLSHA18 is the normal version of A18. When CS6# is asserted (i.e. at the top of the 1M address space), FLSHA18 is the inverted version of A18. This enables the same physical Flash memory device to easily be mapped into two locations in the address map. In this way, the boot code can show up at the top of the physical address space, while the BIOS can be found at the top of the 1M address space as expected, and still only require one physical device.

The FLSHCS# signal is used as the chip select for the Flash memory device. It has an 8 mA drive capability.

The FLSHWE# signal is used as the write enable signal for programming Flash memory devices. It has an 8 mA drive capability.

If the R300EX is used in a system utilizing a 256K Flash device rather than a 512K Flash device, then the following changes need to be made to properly utilize the FLSHA18 signal. The A17 and A18 signals from the Intel386 EX should be swapped so they feed into A18 and A17 on the R300EX. The FLSHA18 signal from the R300EX would then, in essence, be the FLSHA17# signal and should be fed into the highest order address pin of the 256K flash device (A17 on a by 8 device and A16 on a by 16 device.) Figure 5 shows the connection schemes for systems using 4Mb or 2Mb Flash devices.

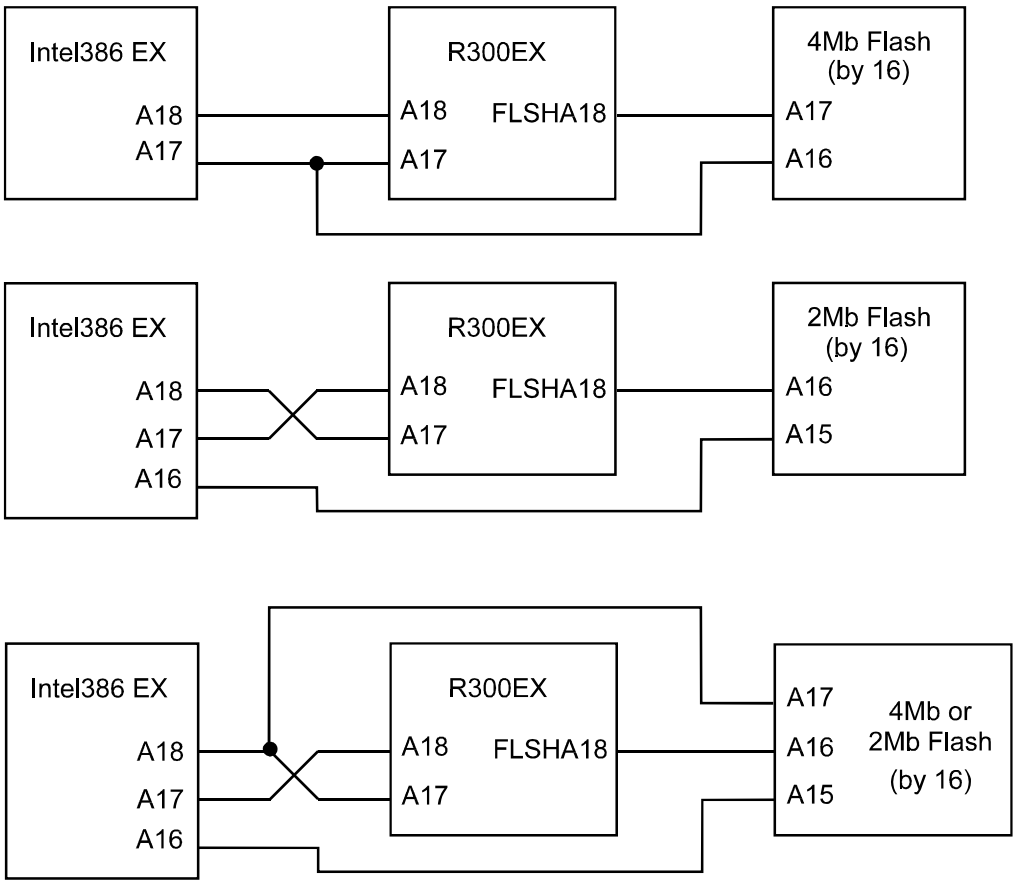


Figure 6: Connection Diagram for 2Mb and 4Mb Systems

Keyboard Interface Signal

The KBDCS# signal is used as the chip select for the keyboard/mouse controller chip. It is generated in response to CS1# being asserted. Cycles accessing the keyboard/mouse controller conform to the basic SEB timing.

CS1# from the Intel386 EX should be configured for I/O addresses 60-61h and 64-65h. BLE# is used internally to further qualify this address range down to address 60h and 64h.

IDE Interface

The IDE interface consists of two buffer enables IDE_ENH# and IDE_ENL#. The R300EX uses IOCS16# to determine the access time and bus sizing. These cycles are run at the SEB standard of 8 or 15 wait states. Chip select CS4# should be programmed as the primary IDE device select and asserted for accesses to I/O addresses 1F0-1F7h. Chip select CS3# should be programmed as the secondary IDE device select and asserted for accesses to I/O addresses 3F6h and 3F7h. The IDE_ENH# and IDE_ENL# signals should be connected to the enable inputs of ‘245-style bi-directional buffers for the 16-bit data path to the IDE connector. Cycles accessing the IDE Interface conform to the basic SEB timing.

Data Bus Buffer Disable

This signal disables data buffers between the CPU and peripheral devices for all T1, T1P and Ti cycles that follow a T2 or T2P cycle. This buffer eliminates the possibility of data bus contention when the CPU transitions from a read cycle to a write cycle. This signal is asserted high in order to disable data buffers. It is intended that DATA_DE be connected to the asserted low output enable of a ‘245 type data buffer.

NMI Generation

The NMI signal will be asserted in response to the R300EX recognizing a CPU Shutdown cycle. The NMI will be deasserted upon detection of the next UCS# assertion. A Shutdown cycle initiates a software based reset by asserting NMI. It is expected that the BIOS will handle the NMI and reset the CPU through port 92, internal to the Intel386 EX. This allows the NMI service routine to handle shutdown cycles in a manner similar to PCs.

TEST Mode and NAND Tree Output

The R300EX has a test mode which, when used with an ATE bed-of-nails tester, allows verification of the connection between the circuit board and the chip itself for all of the non-power pins. When the TEST mode pin is asserted, all of the normal outputs are tri-stated and become test inputs. Each of the regular inputs along with the test inputs feeds into a chain of NAND gates which connect all of the non-power pins together. After asserting TEST, the testing process is started by taking all of the input pins in the NAND chain high, and monitoring the NAND_OUT pin. By starting with the first pin in the chain and bringing it low, then high, then low and leaving it low, the NAND_OUT pin can be seen to toggle. By leaving the input low, it cuts off the previous portion of the chain, and allows isolations of the next pin for testing. The process is repeated with the next pin in the chain until each input has been verified. Thus, by using an ATE tester probing the vias which feed the pads soldered to the pins of the chip, it is possible to verify that there is an electrical connection from the via, through the chip, and back out to another via. By sequentially going through all of the non-power pins, it is possible to verify the board's connection to each signal pin on the chip.

The NAND-Tree connection sequence starts with pin one and continues through pin 100. The connection skips the power and ground pins, the TEST input, the NC pins, and the NAND output.

No Connect Pins

There are two NC pins on the R300EX. They are not connected to the NAND tree test chain, and are not used for any function. They have no bond wire from the die to the package. They can be tied high, low, or left floating.

OPERATIONAL SPECIFICATIONS

Table 15: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Notes
Vdd	DC Supply Voltage	-0.3	7.0	V	
Vin	Input Pin Voltage	-0.3	Vdd+0.3	V	
Iin	Input Pin Current	-10.0	10.0	mA	25 °C
Tstrg	Storage Temperature	-55	150	°C	
Tlead	Lead Temperature		300	°C	10 Sec

Table 16: Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
Vdd	DC Supply Voltage	4.5	5.5	V	(2)
Idd	Static Supply Current		100	µA	(1)
Icc	Dynamic Supply Current		55	mA	(3)
Vss	Circuit Ground	0.0	0.0	V	
Ta	Ambient Temperature	0	70	°C	(2)

(1) Static Idd current is exclusive of input/output drive requirements and is measured with the clocks stopped and all inputs tied to Vdd or Vss, configured to draw minimum current.

(2) The input and output parametric values in the Parametric Voltage and Current Levels, parts 1, 2, and 3, are directly related to ambient temperature and DC supply voltage.

(3) Worst case calculated value with CLK2 input of 66MHz. Typical value expected to be 40mA.

Parametric Voltage and Current Levels

Table 17: INPUTS:

Type	Vil	Vih	Iil (1)		Iih (2)		Hyst	Note
			Min	Max	Min	Max		
All except those listed below.	0.8V	2.0V	NA	-1µA	NA	1µA	NA	TTL
PWRGD	0.7V	2.1V	NA	-1µA	NA	1µA	0.4V	TTL--Schmitt
CLK2	0.3Vdd	0.7Vdd	NA	-1µA	NA	1µA	NA	CMOS

(1) Iil is tested at Vdd = 5.5 Volts and Vin = 0 Volts.
(2) Iih is tested at Vdd = 5.5 Volts and Vin = 5.5 Volts.

Table 18: OUTPUTS:

Type	Vol	Voh	Iol (3)	Ioh (4)	Ioz (5)	Note (6)
NAND_OUT	0.4V	2.4V	4mA	-4mA	NA	NA

(3) Vol, Iol are tested at Vdd = 4.5 Volts.
(4) Voh, Ioh are tested at Vdd = 4.5 Volts.
(6) Ioz is tested with Vdd = 5.5 Volts.
(6) At test time a 1.5k Ohm resistor is tied to Vdd or Vss on open drain devices to force a signal level when the device is in a high-impedance state.

BIDIRECTIONALS:

Table 19: **INPUT SECTION:**

Type	Vil	Vih	Iil(7)		Iih(8)		Hyst	Note
			Min	Max	Min	Max		
All	0.8V	2.0V	NA	NA	NA	NA	NA	TTL

(7) Iil is tested at Vdd = 5.5 Volts and Vin = 0 Volts.
(8) Iih is tested at Vdd = 5.5 Volts and Vin = 5.5 Volts.

Table 20: OUTPUT SECTION:

Type	Vol	Voh	Iol (9)	Ioh (10)	Ioz(11)		Note
					Min	Max	
All except those listed below.	0.4V	2.4V	4mA	-4mA	-10µA	10µA	TTL
RESET, MA[10..0], CASAH#, CASAL#, CASBH#, CASBL#, RAS# WE#, FLSHWE#, FLSHCS#, BALE#, MEMR#, MEMW#, IOR#, IOW#, DATA_DE	0.4V	2.4V	8.0mA	-8.0mA	-10µA	10µA	TTL, (12)

(9) Vol, Iol are tested at Vdd = 4.5 Volts.
(10) Voh, Ioh are tested at Vdd = 4.5 Volts.
(11) Ioz is tested with Vdd = 5.5 Volts.
(12) MA[0..10] have controlled edge rate buffers.

INPUT CAPACITANCE

Input capacitance for any pin: 15pF max.

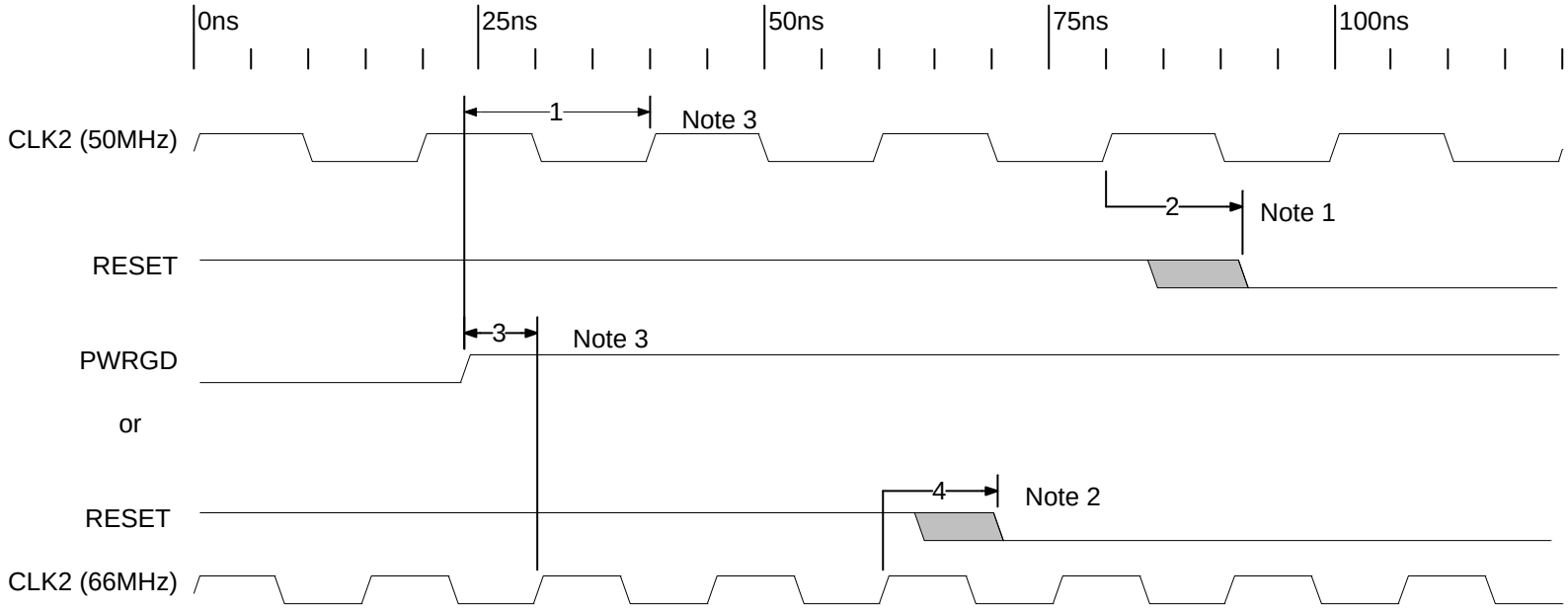
SIGNAL TIMING INFORMATION

The accompanying waveform diagrams show the timing relationships between signals. The timing diagrams show the relationships for the output signals from the R300EX, and a few non-CPU input signals. The timing relationships for the input signals from the Intel386 EX to the R300EX are as shown in the table below.

Table 21: R300EX Signal Timing

Signal Name	Setup Time	Hold Time	Comments
A[23:1], ADS#, BHE#, BLE# W/R#, M/IO#, D/C#,	5nS	2nS	Relative to CLK2 input to R300EX
UCS#, CS[1:6], LBA#	5nS	2nS	Relative to CLK2 input to R300EX

Figure 7: Clock - Reset Timing Waveforms



Note 1: ¸Load on RESET assumed to be 50pF or less with 50MHz CLK2
Note 2: ¸Load on RESET assumed to be 25pF or less with 66MHz CLK2
Note 3: ¸PWRGD can be fully asynchronous. Meeting the PWRGD setup ¸time to CLK2 guarantees recognition on that CLK2 edge.

Table 22: Clock - Reset AC Characteristics

Signal	Signal Name	Min	Max	Description
1	tSU_CLK2:PWRGDH	3		Setup time from CLK2 to PWRGD
2	tCO_CLK2:RESETL (50pF)	4	12	Prop Delay from CLK2 to RESET Low (up to 50pF load)
3	tSU_CLK2:RESETGDH	3		Setup time from CLK2 to PWRGD
4	tCO_CLK2:RESETL (20pF)	3	10	Prop Delay from CLK2 to RESET Low (up to 20pF load)

Figure 8: DRAM Access Waveforms

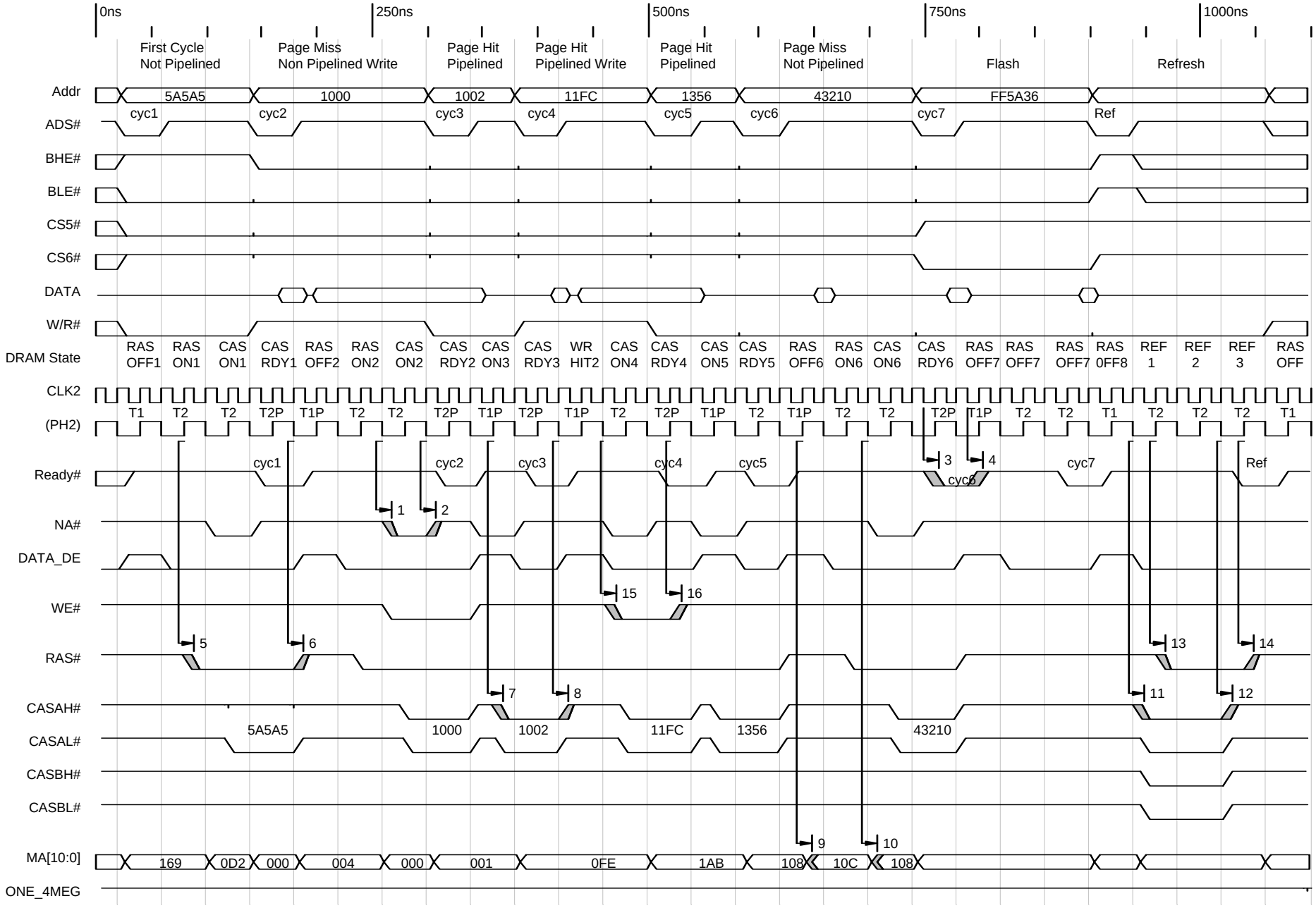
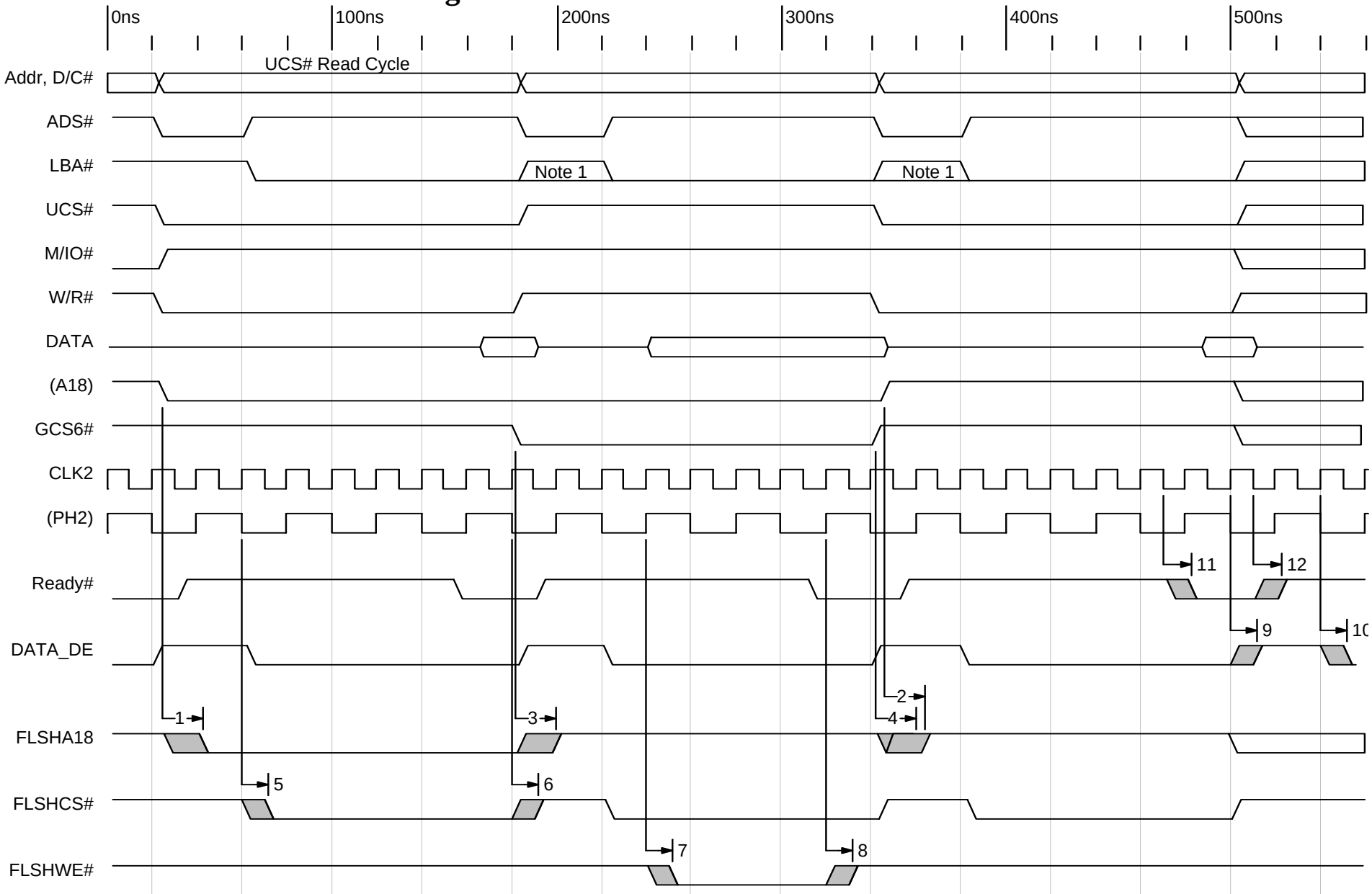


Table 23: R300EX - DRAM Access Timing

Signal	Signal Name	Min	Max	Description
1	tPD_CLK2:NAL	3	9	Prop delay from CLK2 to NA# Low
2	tPD_CLK2:NAH	3	9	Prop delay from CLK2 to NA# High
3	tPD_CLK2:RDYL	3	13	Prop delay from falling edge of CLK2 to READY# Low
4	tPD_CLK2:RDYH	3	13	Prop delay from falling edge of CLK2 to READY# High
5	tPD_CLK2:RASL	3	9	Prop delay from CLK2 to RAS# Low
6	tPD_CLK2:RASH	3	9	Prop delay from CLK2 to RAS# High
7	tPD_CLK2:CASL	3	9	Prop delay from CLK2 to CASxx# Low
8	tPD_CLK2:CASH	3	9	Prop delay from CLK2 to CASxx# High
9	tPD_CLK2:MARAS	3	9	Prop delay from CLK2 to valid RAS address on MA
10	tPD_CLK2:MACAS	3	9	Prop delay from CLK2 to valid CAS address on MA
11	tPD_CLK2:REFCASL	3	9	Prop delay from CLK2 to Refresh CASxx# Low
12	tPD_CLK2:REFCASH	3	9	Prop delay from CLK2 to Refresh CASxx# High
13	tPD_CLK2:REFRASL	3	9	Prop delay from CLK2 to Refresh RAS# Low
14	tPD_CLK2:REFRASH	3	9	Prop delay from CLK2 to Refresh RAS# High
15	tPD_CLK2:WEL	4	11	Prop delay from CLK2 to WE# Low
16	tPD_CLK2:WEH	4	11	Prop delay from CLK2 to WE# High

Figure 9: Flash Access Waveforms

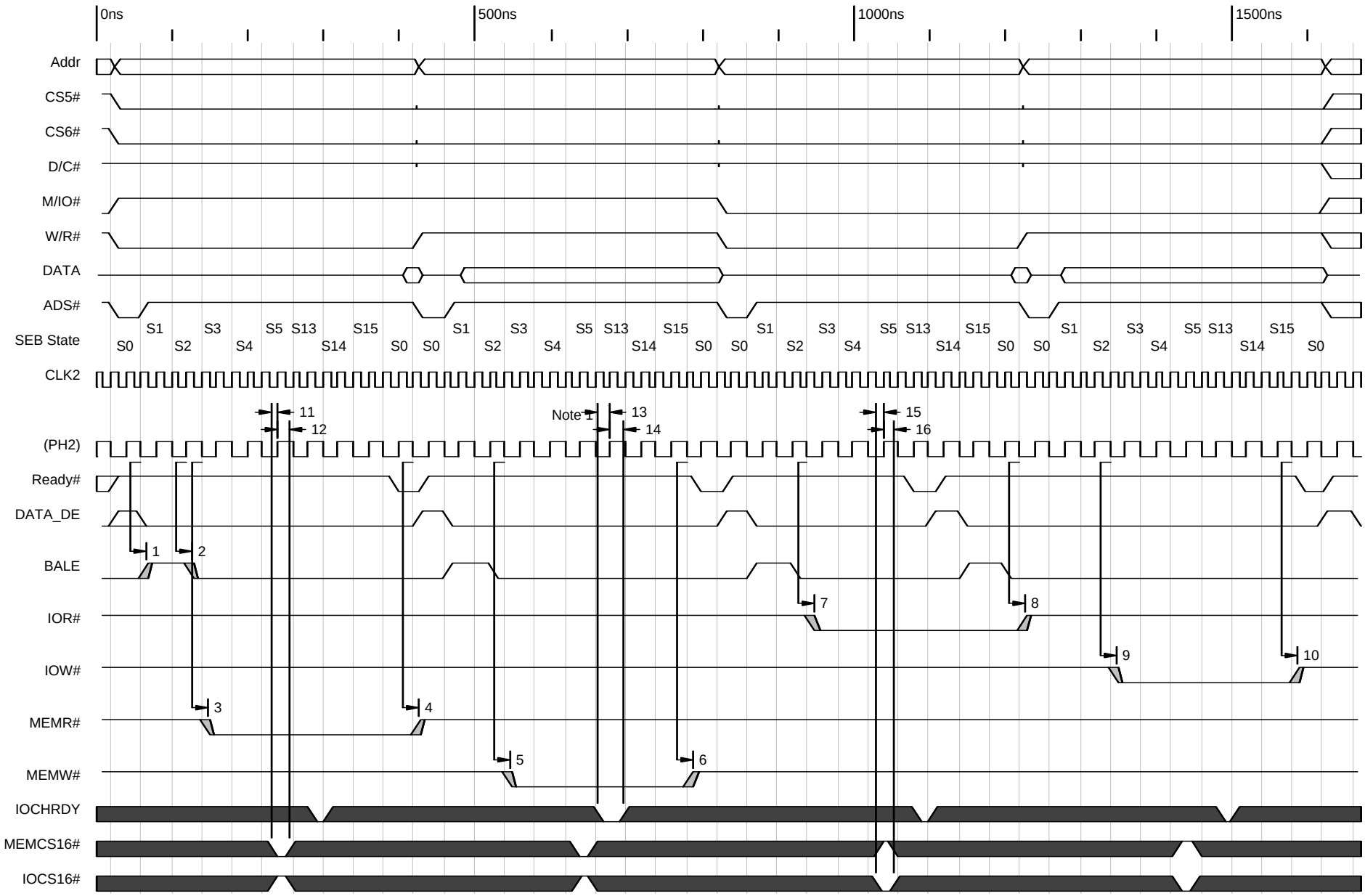


Note1: LBA# Continues assertion on Step-C Intel386 EX devices

Table 24: R300EX - Flash Memory Access Timing

Signal	Signal Name	Min	Max	Description
1	tPD_A18:FLSHA18L	2	18	Prop delay from A18 to FLSHA18 Low
2	tPD_A18:FLSHA18H	2	18	Prop delay from A18 to FLSHA18 High
3	tPD_CS6:A18I	2	18	Prop delay from CS6# to FLSHA18 Inverting
4	tPD_CS6:A18N	2	18	Prop delay from CS6# to FLSHA18 Non-Inverting
5	tPD_CLK2:FCSL	2	12	Prop delay from CLK2 to FLSHCS# Low
6	tPD_CLK2:FCSH	2	12	Prop delay from CLK2 to FLSHCS# High
7	tPD_CLK2:FWEL	2	12	Prop delay from CLK2 to FLSHWE# Low
8	tPD_CLK2:FWEH	2	12	Prop delay from CLK2 to FLSHWE# High
9	tPD_CLK2:DDEL	2	12	Prop delay from CLK2 to DATA_DE Low
10	tPD_CLK2:DDEH	2	12	Prop delay from CLK2 to DATA_DE High
11	tPD_CLK2:RDYL	3	13	Prop delay from CLK2 to READY# Low (25pF Load)
12	tPD_CLK2:RDYH	3	13	Prop delay from CLK2 to READY# High (25pF Load)

Figure 9:16 Bit SEB Access Waveforms

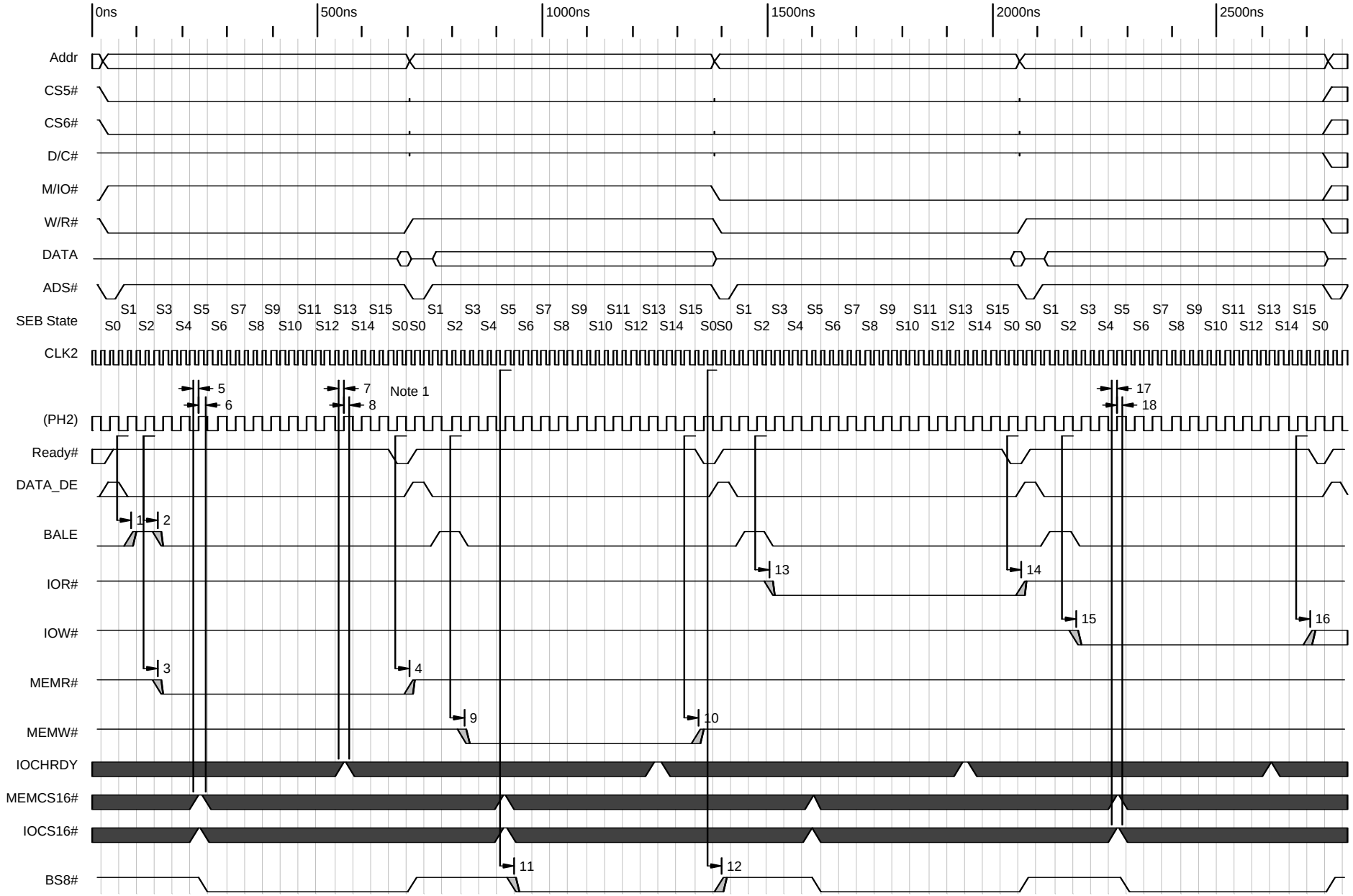


Note 1, To guarantee recognition on this clock the setup time must be met.

Table 25: 16-Bit SEB Access Timing

Signal	Signal Name	Min	Max	Description
1	tPD_CLK2:BALEH	2	8	Prop delay from CLK2 to BALE High
2	tPD_CLK2:BALEL	2	8	Prop delay from CLK2 to BALE Low
3	tPD_CLK2:MEMRL	2	8	Prop delay from CLK2 to MEMR# Low
4	tPD_CLK2:MEMRH	2	8	Prop delay from CLK2 to MEMR# High
5	tPD_CLK2:MEMWL	3	8	Prop delay from CLK2 to MEMW# Low
6	tPD_CLK2:MEMWH	3	8	Prop delay from CLK2 to MEMW# High
7	tPD_CLK2:IORL	2	8	Prop delay from CLK2 to IOR# Low
8	tPD_CLK2:IORH	2	8	Prop delay from CLK2 to IOR# High
9	tPD_CLK2:IOWL	2	8	Prop delay from CLK2 to IOW# Low
10	tPD_CLK2:IOWH	2	8	Prop delay from CLK2 to IOW# High
11	tSU_MEMCS16:CLK2	5		Setup time for MEMCS16# Low to CLK2
12	tHLD_CLK6:MEMCS16L	5		Hold time from CLK2 to MEMCS16# Low
13	tSU_IOCHRDY:CLK2	5		Setup time for IOCHRDY# Low to CLK2
14	tHLD_CLK6:IOCHRDY	5		Hold time from CLK2 to IOCHRDY# Low
15	tSU_IOCS16:CLK2	5		Setup time for IOCS16# Low to CLK2
16	tHLD_CLK6:IOCS16L	5		Hold time from CLK2 to IOCS16# Low

Figure 10: 8 Bit SEB Access Waveforms



Note 1, To guarantee recognition on this clock the setup time must be met.

Figure 26: 8-Bit SEB Access Timing

Signal	Signal Name	Min	Max	Description
1	tPD_CLK2:BALEH	2	8	Prop delay from CLK2 to BALE High
2	tPD_CLK2:BALEL	2	8	Prop delay from CLK2 to BALE Low
3	tPD_CLK2:MEMRL	2	8	Prop delay from CLK2 to MEMR# Low
4	tPD_CLK2:MEMRH	2	8	Prop delay from CLK2 to MEMR# High
5	tSU_MEMCS16:CLK2	5		Setup time for MEMCS16# to CLK2
6	tHLD_CLK2:MEMCS16L	5		Hold time from CLK2 to MEMCS16# Low
7	tSU_IOCHRDY:CLK2	5		Setup time for IOCHRDY# to CLK2
8	tHLD_CLK2:IOCHRDYL	5		Hold time from CLK2 to IOCHRDY Low
9	tPD_CLK2:MEMWL	3	8	Prop delay from CLK2 to MEMW# Low
10	tPD_CLK2:MEMWH	3	8	Prop delay from CLK2 to MEMW# High
11	tPD_CLK2:BS8L	3	9	Prop delay from falling edge of CLK2 to BS8# Low
12	tPD_CLK2:BS8H	3	9	Prop delay from falling edge of CLK2 to BS8# High
13	tPD_CLK2:IORL	2	8	Prop delay from CLK2 to IOR# Low
14	tPD_CLK2:IORH	2	8	Prop delay from CLK2 to IOR# High
15	tPD_CLK2:IOWL	2	8	Prop delay from CLK2 to IOW# Low
16	tPD_CLK2:IOWH	2	8	Prop delay from CLK2 to IOW# High
17	tSU_IOCS16:CLK2	5		Setup time for IOCS16# to CLK2
18	tHLD_CLK2:IOCS16L	5		Hold time from CLK2 to IOCS16# Low

Figure 11: Keyboard / Mouse Access Waveforms

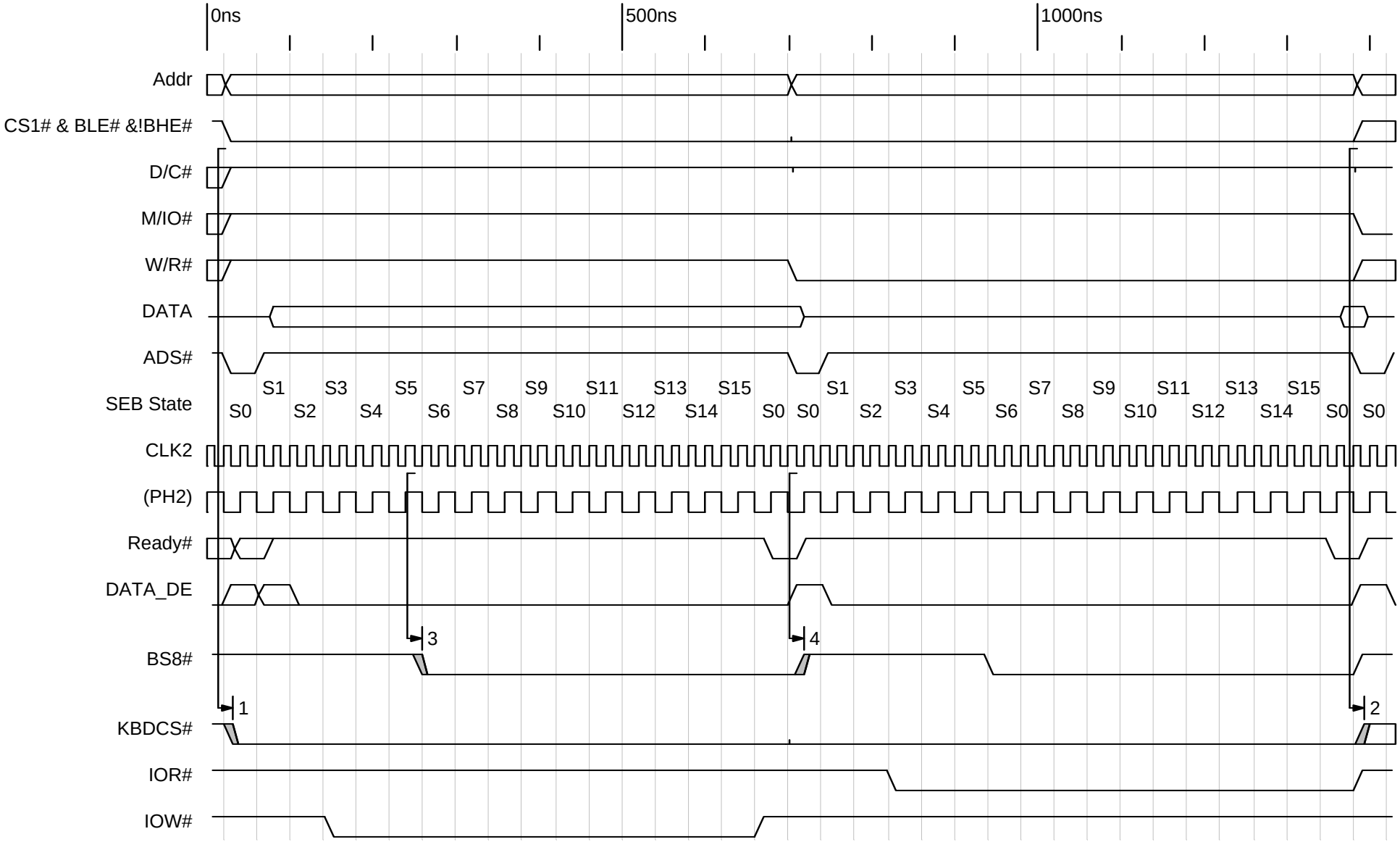


Table 27: Keyboard / Mouse Access Timing

Signal	Signal Name	Min	Max	Description
1	tPD_CS2:KBDCSL	3	9	Prop delay from (CS1# & BLE# & !BHE#) to KBDCS# Low
2	tPD_CS2:KBDCSH	3	9	Prop delay from (CS1# & BLE# & !BHE#) to KBDCS# High
3	tPD_CLK2:BS8L	3	9	Prop delay from falling edge of CLK2 to BS8# Low
4	tPD_CLK2:BS8H	3	9	Prop delay from falling edge of CLK2 to BS8# High

Figure 12: Real Time Clock Access Waveforms

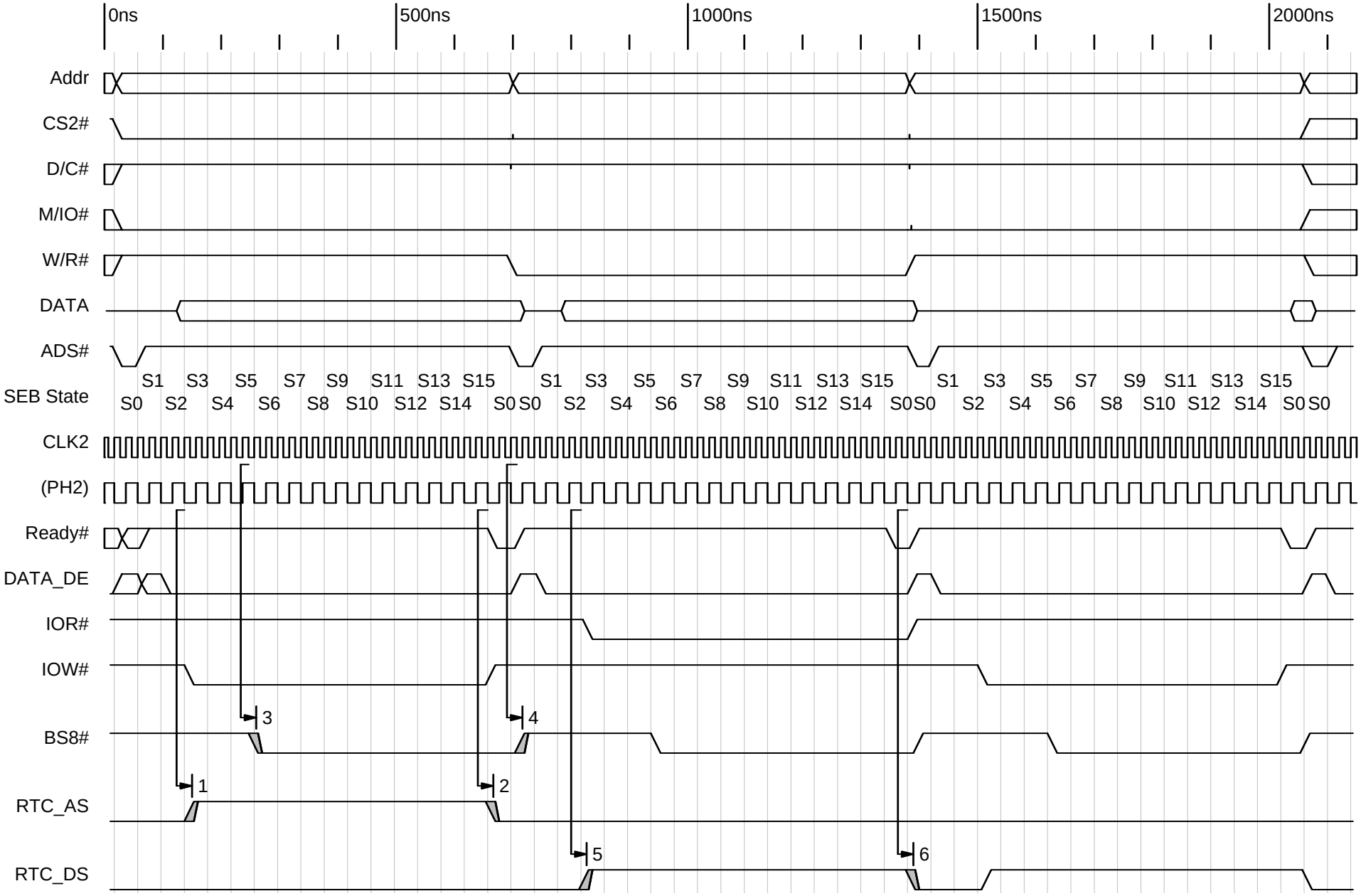


Table 28 Real Time Clock Access Timing

Signal	Signal Name	Min	Max	Description
1	tPD_CLK2:RTCASH	4	11	Prop delay from CLK2 to RTC_AS High
2	tPD_CLK2:RTCASH	4	11	Prop delay from CLK2 to RTC_AS Low
3	tPD_CLK2:BS8L	4	11	Prop delay from falling edge of CLK2 to BS8# Low
4	tPD_CLK2:BS8H	4	11	Prop delay from falling edge of CLK2 to BS8# High
5	tPD_CLK2:RTCDSH	4	11	Prop delay from CLK2 to RTC_DS Low
6	tPD_CLK2:RTCDSL	4	11	Prop delay from CLK2 to RTC_DS High

Figure 13: IDE Access Waveforms

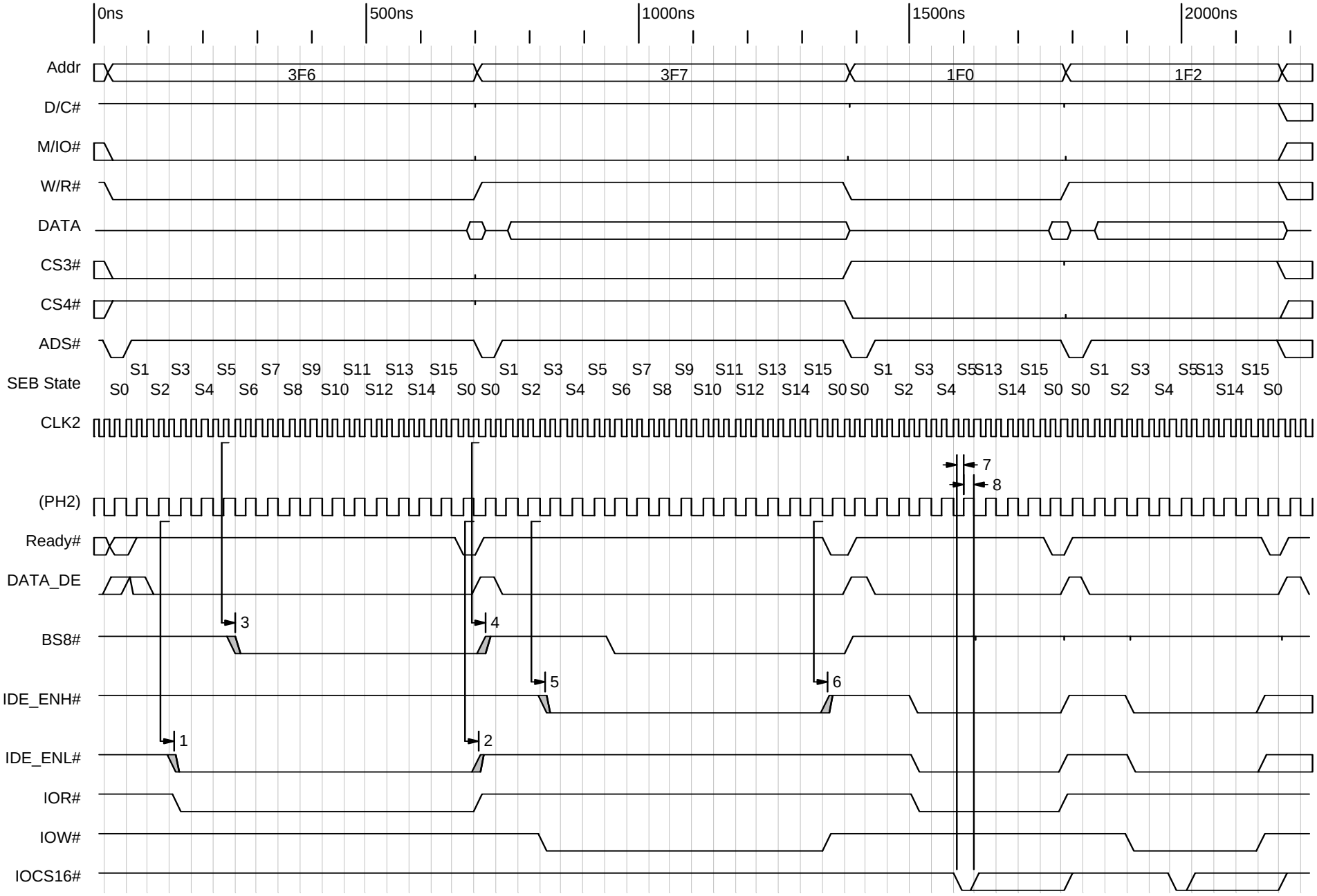


Figure 29: IDE Access Timing

Signal	Signal Name	Min	Max	Description
1	tPD_CLK2:IDEENLL	3	10	Prop delay from CLK2 to IDE_ENL Low
2	tPD_CLK2:IDEENHL	3	10	Prop delay from CLK2 to IDE_ENL High
3	tPD_CLK2:BS8L	3	10	Prop delay from falling edge of CLK2 to BS8# Low
4	tPD_CLK2:BS8H	3	10	Prop delay from falling edge of CLK2 to BS8# High
5	tPD_CLK2:IDEENHL	3	10	Prop delay from CLK2 to IDE_ENH Low
6	tPD_CLK2:IDEENHH	3	10	Prop delay from CLK2 to IDE_ENH High
7	tSU_IOCS16L:CLK2	5		Setup time from IOCS16# Low to CLK2
8	tHLC_IOCS16L:CLK2	5		Hold time from IOCS16# Low from CLK2

Figure 14: NMI Response Waveforms

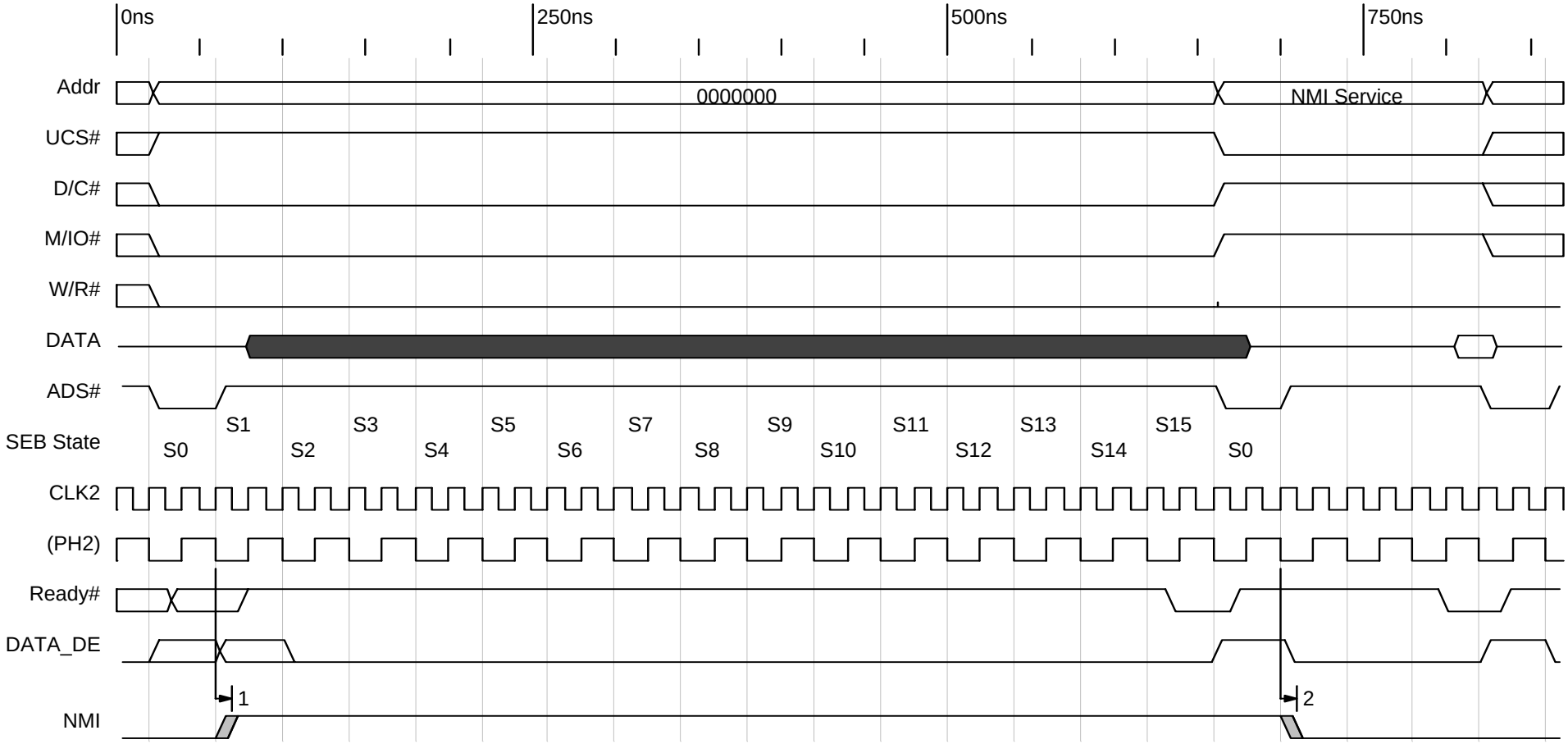
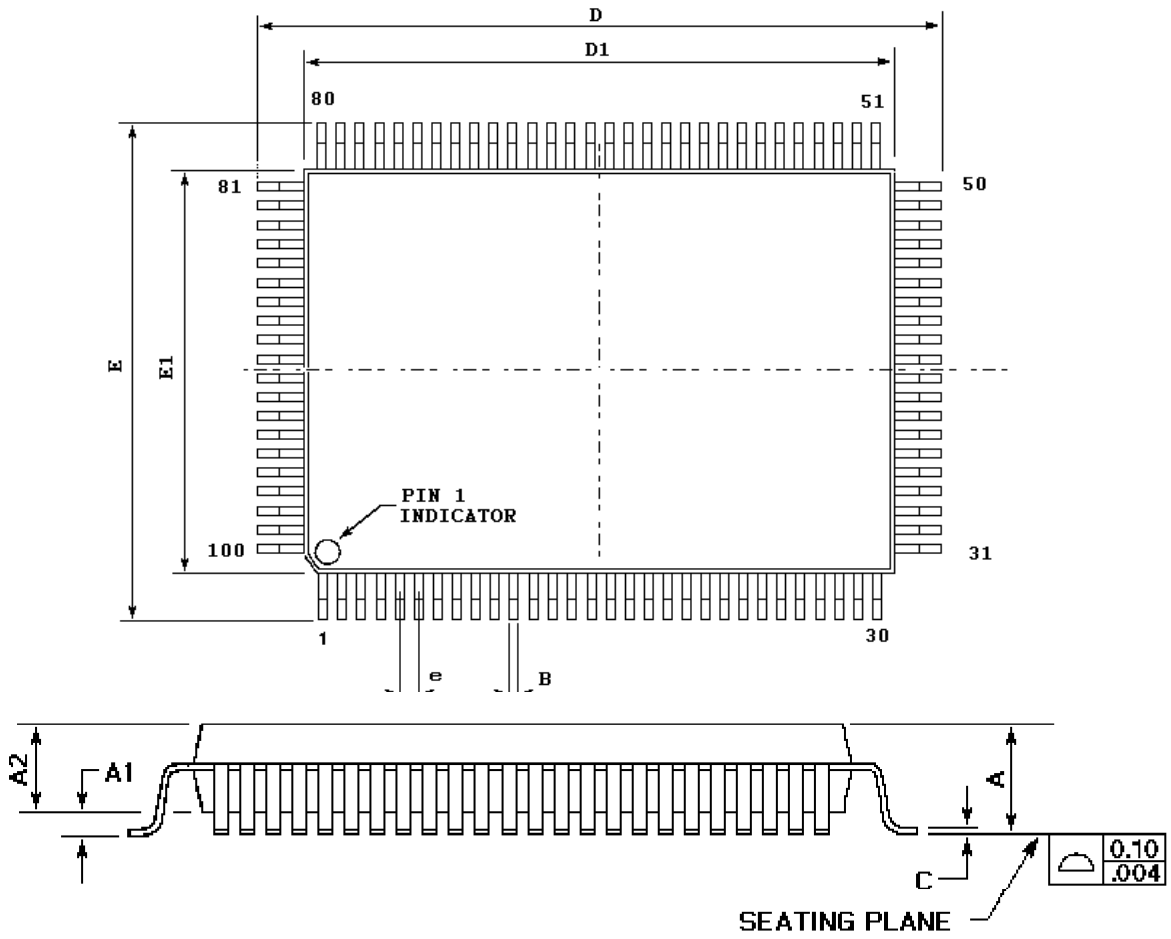
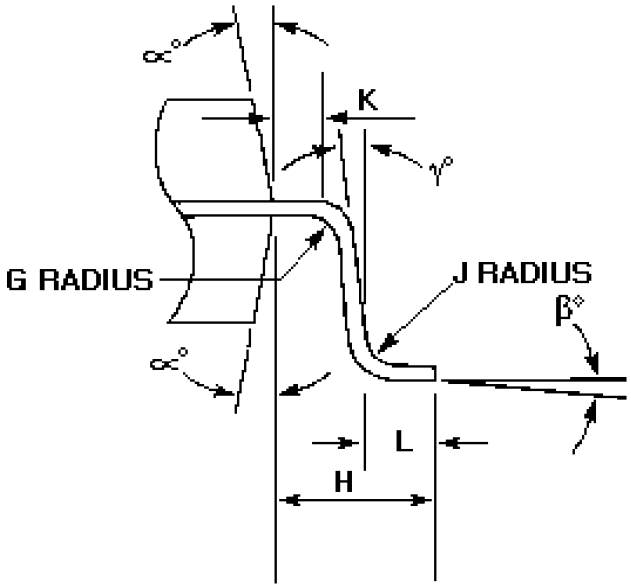


Table 30: NMI Response Timing

Signal	Name	Min	Max	Description
1	tPD_CLK2:NMIH	3	10	Prop Delay from CLK2 to NMI High
2	tPD_CLK2:NMIH	3	10	Prop Delay from CLK2 to NMI low



Pins	100	
Body Size	14 X 20 mm	
Symbol	Min.	Max.
A	-	3.40
A1	0.25	-
A2	2.57	2.87
D	23.65	24.15
D1	19.90	20.10
E	17.65	18.15
E1	13.90	14.10
L	0.65	0.95
e	0.65 BSC	
B	0.22	0.38
c	0.13	0.23
α°	12	16
β°	0	7
γ°	0	-
G	0.13	-
H	1.95 REF	
J	0.13	0.30
K	0.40	-
2H	3.9	



Note: All dimension in mm