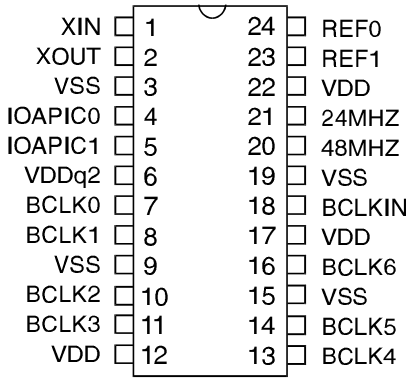
Clock Generator with Zero Delay Output Buffers

FEATURES

- Generates 7 synchronous zero delay PCI bus clocks.
- Designed to work with PLL52C64-05 or PLL52C64-25 for EMI reduction.
- Less than 250ps propagation delay from BCLKIN to BCLK output when equally loaded.
- Two 14.318Mz reference clocks
- Two 2.5V IOAPIC clocks for dual processors.
- One 24Mhz and one 48Mhz USB clock
- All outputs have very low Cycle to cycle jitter (<150ps)
- < 250ps output skew between PCI bus clock
- < 250ps output skew between IOAPIC clock
- 50% duty cycle outputs.
- Available in 300mil 24 pin SOP.

PIN INFORMATION

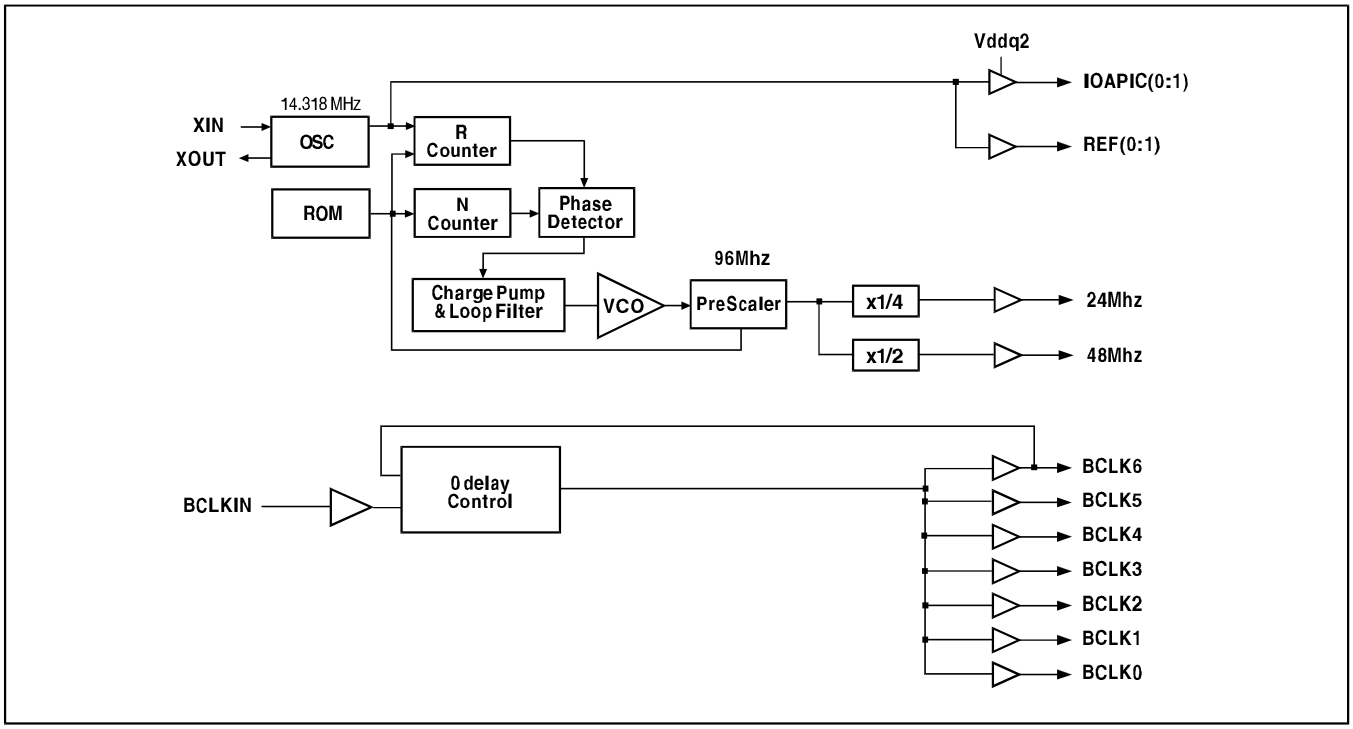


PLL52C64-06

DESCRIPTION

The PLL52C64-06 is a high performance clock generator designed specifically to support the very tight timing requirement of Pentium PC Motherboards. All output clocks skew and jitter performance are designed to be fully compliant with INTEL Pentium CPU timing requirements. This device associates with PLL52C64-05/-25 is the solution for the very stringent EMI specifications when applied to PC Motherboards with up to 4 DIMM SDRAM.

BLOCK DIAGRAM



SIGNAL DESCRIPTIONS

NAME		PIN TYPE	DESCRIPTION
VDD	12,17,22	P	Power supply (3V ~ 5V)
VDDq2	6	P	Power supply 2.5V~5V
VSS	3,9,15,19	P	Ground.
XIN	1	I	14.318Mhz crystal input to be connected to one end of the crystal.This input can also be connected directly to other source of 14.318Mhz from PC board.
XOUT	2	O	14.318Mhz crystal out put.
BCLK(0:6)	7,8,10,11, 1314,16	O	PCI bus clock output. To achieve zero delay between BCLKIN and BCLK, all BCLK outputs must be loaded equally. The BCLK6 pin is advised to have a capacitive load since this pin is used to feedback to internal 0-delay circuits for delay adjusting.
BCLKIN	18	I	PCI clock input
IOAPIC(0:1)	4,5	I	2.5V14.318Mhz Reference clock out put for parallel processing.
24Mhz	21	O	24Mhz output for super I/O
48Mhz	20	O	48Mhz output for USB
REF(0:1)	23,24	O	Buffered reference clock at 14.318Mhz

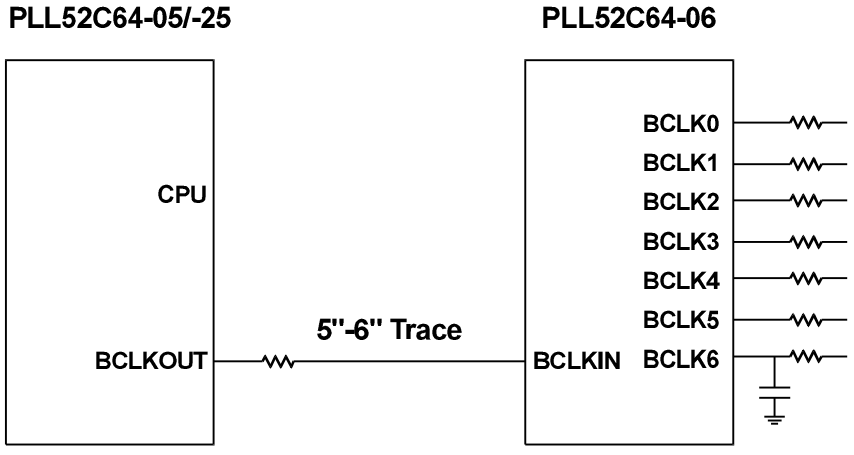
45437 Warm Springs Blvd., Fremont, California 94539, Tel : 510-492-0990 Fax : 510-492-0991

ZERO DELAY DESIGN GUIDELINE

- To comply with the CPU vs BCLK skew specification, the trace length from BCLK of 5264-05/-25 to BUSIN of 5264-06 is required to be layout accurately. We recommend to use 0.5~0.6" trace with 50 ohm impedance in connecting with two chips. The skew calculation is as follow:

	CPU to BCLK skew		6" TRACE (1.66ns/feet)		BCLKIN to BCLK		CPU to BCLK
MINIMUM	0.6ns	+	0.8ns	+	(0.25ns)	=	1.15ns
TYPICAL	1.2ns	+	0.8ns	+	0.0ns	=	2.0ns
MAXIMUM	1.8ns	+	0.8ns	+	0.25ns	=	2.85ns

- For zero delay between BUSIN and all BCLK(0:6), all BCLK output pins should be equally loaded. Equal loading of BCLK ensures additionally zero output to output skew between all BCLK clocks.
- Since BCLK6 pin is used as feedback to the internal zero delay control circuits, its relative loading can be used for the adjustment of the input to output propagation delay between BUSIN and all BCLK(0:6). It ensures additionally zero output to output skew between all BCLK pins except BCLK6 when equally loading of BCLK. It is therefore suggested to reserve a separate capacitive load on output of BCLK6 as shown below.



MAXIMUM RATINGS

SUPPLY VOLTAGE	VSS-0.5 TO 7V
INPUT VOLTAGE	VSS-0.5V to VDD+0.5V
ESD VOLTAGE	2000V
POWER DISSIPATION	0.75W

Exposure of the device under conditions beyond the limits specified by Maximum Ratings may cause permanent damage to the device

AC SPECIFICATIONS

VDD=3.3V±10% 0°C to 70°C						
PARAMETERS	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Reference input clock rise time	T_{IR}	From 0.8 V to 2V			2	ns
Reference input clock fall time	T_{IF}	From 2V to 0.8V			2	ns
Duty cycle	D_T	All output clocks @ 15pF load.	45	50/50	55	%
Clock Skew (20pF load, @ 1.4V)	T_{SKW}	BLCK to BCLK		250	500	ps
		IOAPIC to IOAPIC		250	500	ps
Delay	T_{DLY}	BCLKIN to BCLK		250		ps
Jitter, Absolute (20pF load)	T_{JA}	BCLK(0:6)	-250		250	ps
Jitter, One Sigma (20pF load)	T_{JO}	BCLK(0:6)		50	200	ps

DC SPECIFICATIONS

VDD=3.3V±10% 0°C to 70°C						
PARAMETERS	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Dynamic Current	I_{DYN}	BCLK at 66.6 MHZ no load		40	80	mA
Static Current	I_{STAT}	BCLKIN=LOW		250	500	µA
Input High Voltage	V_{IH}	BCLKIN	2			V
Input Low Voltage	V_{IL}	BCLKIN			0.8	V
Output Low Current @VOL=0.4V	I_{OL}	All outputs except XOUT	1			mA

45437 Warm Springs Blvd., Fremont, California 94539, Tel : 510-492-0990 Fax : 510-492-0991

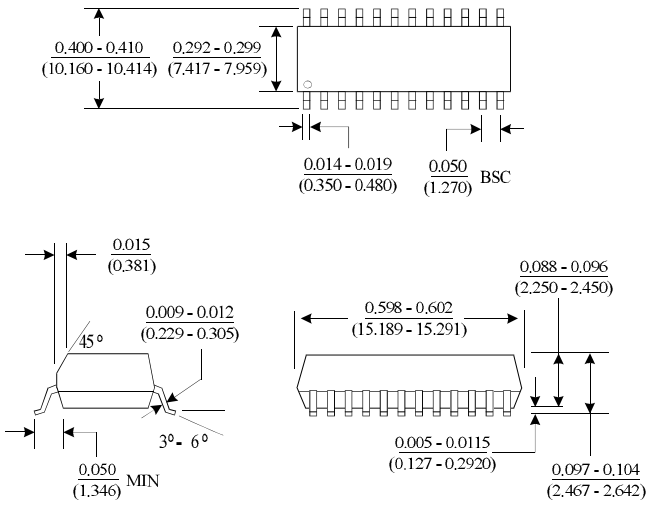
BUFFER SPECIFICATIONS

TYPE 2 (=2.5V±5%) : IOAPIC(0:1) BUFFER Characteristics						
PARAMETERS	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Output High Current	I_{OH}	VOUT=1.4V	-36			mA
		VOUT=2.7V			-29	
Output Low Current	I_{OL}	VOUT=1.0V	36			mA
		VOUT=0.2V			28	
Output rise time	T_{OR}	From 0.4V to 2.0V, 10pf Load	1			V/ns
		From 0.4V to 2.0V, 20pf Load			4	
Output fall time	T_{OF}	From 2.0V to 0.4V, 10pf Load	1			V/ns
		From 2.0V to 0.4V, 20pf Load			4	

TYPE 3 (=3.3V±5%) : REF(0:1),24Mhz,48Mhz BUFFER Characteristics						
PARAMETERS	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Output High Current	I_{OH}	VOUT=1.0V	-29			mA
		VOUT=3.135V			-23	
Output Low Current	I_{OL}	VOUT=1.95V	29			mA
		VOUT=0.4V			27	
Output rise time	T_{OR}	From 0.4V to 2.4V, 10pf Load	0.5			V/ns
		From 0.4V to 2.4V, 20pf Load			2	
Output fall time	T_{OF}	From 2.4V to 0.4V, 10pf Load	0.5			V/ns
		From 2.4V to 0.4V, 20pf Load			2	

TYPE 5 (=3.3V±5%) : BCLK(0:6) BUFFER Characteristics						
PARAMETERS	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Output High Current	I_{OH}	VOUT=1.0V	-33			mA
		VOUT=3.135V			-33	
Output Low Current	I_{OL}	VOUT=1.95V	30			mA
		VOUT=0.4V			38	
Output rise time	T_{OR}	From 0.4V to 2.4V, 15pf Load	1			V/ns
		From 0.4V to 2.4V, 30pf Load			4	
Output fall time	T_{OF}	From 2.4V to 0.4V, 15pf Load	1			V/ns
		From 0.4V to 2.4V, 30pf Load			4	

PACKAGE INFORMATION



24 PIN SOIC

ORDERING INFORMATION

For part ordering, please contact our Sales Department:

45437 Warm Springs Blvd.,Fremont,CA 94539, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
device number, package type and operating temperature range.

PLL52C64-06 S C

PART NUMBER

TEMPERATURE
C=COMMERCIAL
M=MILITARY
I=INDUSTRIAL

PACKAGE TYPE
S=SOIC