

Programmable macro logic

PML™

PLHS501/PLHS501I

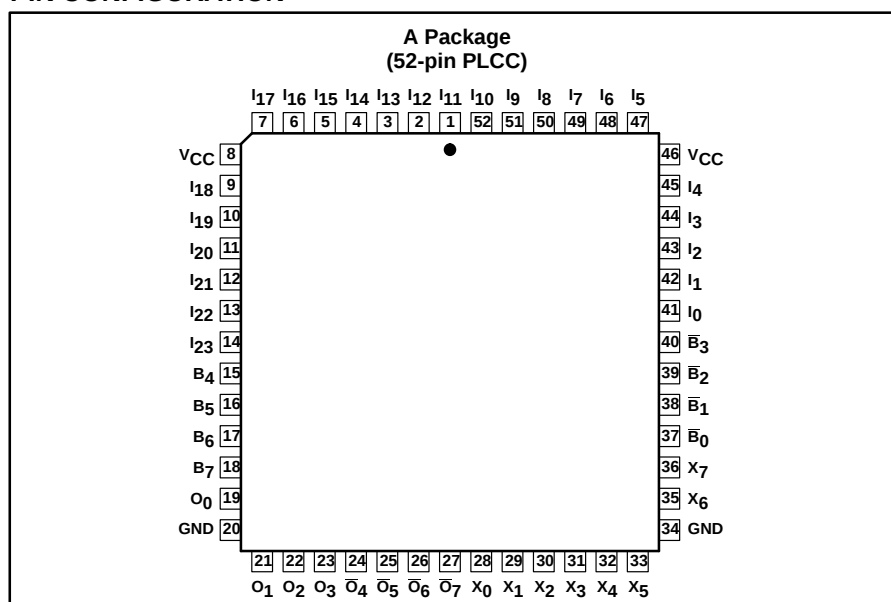
FEATURES

- Programmable Macro Logic device
- Full connectivity
- TTL compatible
- SNAP development system:
 - Supports third-party schematic entry formats
 - Macro library
 - Versatile netlist format for design portability
 - Logic, timing, and fault simulation
- Delay per internal NAND function = 6.5ns (typ)
- Testable in unprogrammed state
- Security fuse allows protection of proprietary designs

STRUCTURE

- NAND gate based architecture
 - 72 foldback NAND terms
- 136 input-wide logic terms
- 44 additional logic terms
- 24 dedicated inputs ($I_0 - I_{23}$)
- 8 bidirectional I/Os with individual 3-State enable:
 - 4 Active-High ($B_4 - B_7$)
 - 4 Active-Low ($\overline{B}_0 - \overline{B}_3$)
- 16 dedicated outputs:
 - 4 Active-High outputs
 - O_0, O_1 with common 3-State enable
 - O_2, O_3 with common 3-State enable
 - 4 Active-Low outputs:
 - $\overline{O}_4, \overline{O}_5$ with common 3-State enable
 - $\overline{O}_6, \overline{O}_7$ with common 3-State enable
 - 8 Exclusive-OR outputs:
 - X_0, X_1 with common 3-State enable
 - X_2, X_3 with common 3-State enable
 - X_4, X_5 with common 3-State enable
 - X_6, X_7 with common 3-State enable

PIN CONFIGURATION



DESCRIPTION

The PLHS501 is a high-density Bipolar Programmable Macro Logic device. PML incorporates a programmable NAND structure. The NAND architecture is an efficient method for implementing any logic function. The SNAP software development system provides a user friendly environment for design entry. SNAP eliminates the need for a detailed understanding of the PLHS501 architecture and makes it transparent to the user. PLHS501 is also supported on the Philips Semiconductors SNAP software development systems.

The PLHS501 is ideal for a wide range of microprocessor support functions, including bus interface and control applications.

The PLHS501 is also processed to industrial requirements for operation over an extended temperature range of -40°C to $+85^{\circ}\text{C}$ and supply voltage of 4.5V to 5.5V.

ARCHITECTURE

The core of the PLHS501 is a programmable fuse array of 72 NAND gates. The output of each gate folds back upon itself and all other NAND gates. In this manner, full connectivity of all logic functions is achieved in the PLHS501. Any logic function can be created within the core of the device without wasting valuable I/O pins. Furthermore, a speed advantage is acquired by implementing multi-level logic within a fast internal core without incurring any delays from the I/O buffers.

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ORDERING INFORMATION

DESCRIPTION	OPERATING CONDITIONS	ORDER CODE	DRAWING NUMBER
52-Pin Plastic Leaded Chip Carrier	Commercial Temperature Range ±5% Power Supply	PLHS501A	0397E
52-Pin Plastic Leaded Chip Carrier	Industrial Temperature Range ±10% Power Supply	PLHS501IA	0397E

DESIGN DEVELOPMENT TOOLS

SNAP

The SNAP Software Development System provides the necessary tools for designing with PML. SNAP provides the following:

- Schematic entry netlist generation from third-party schematic design packages such as OrCAD/SDT III™ and FutureNet™.
- Macro library for standard TTL functions and user defined functions
- Boolean equation entry
- State equation entry
- Syntax and design entry checking
- Simulator includes logic simulation, fault simulation and timing simulation.

SNAP operates on an IBM® PC/XT, PC/AT, PS/2, or any compatible system with DOS 2.1 or higher. The minimum system configuration for SNAP is 640K bytes of RAM and a hard disk.

SNAP provides primitive PML function libraries for third-party schematic design packages. Custom macro function libraries can be defined in schematic or equation form.

After the completion of a design, the software compiles the design for syntax and completeness. Complete simulation can be carried out using the different simulation tools available.

The programming data is generated in JEDEC format. Using the Device Programmer Interface (DPI) module of SNAP,

the JEDEC fusemap is sent from the host computer to the device programmer.

DESIGN SECURITY

The PLHS501 has a programmable security fuse that controls the access to the data programmed in the device. By using this programmable feature, proprietary designs implemented in the device cannot be copied or retrieved.

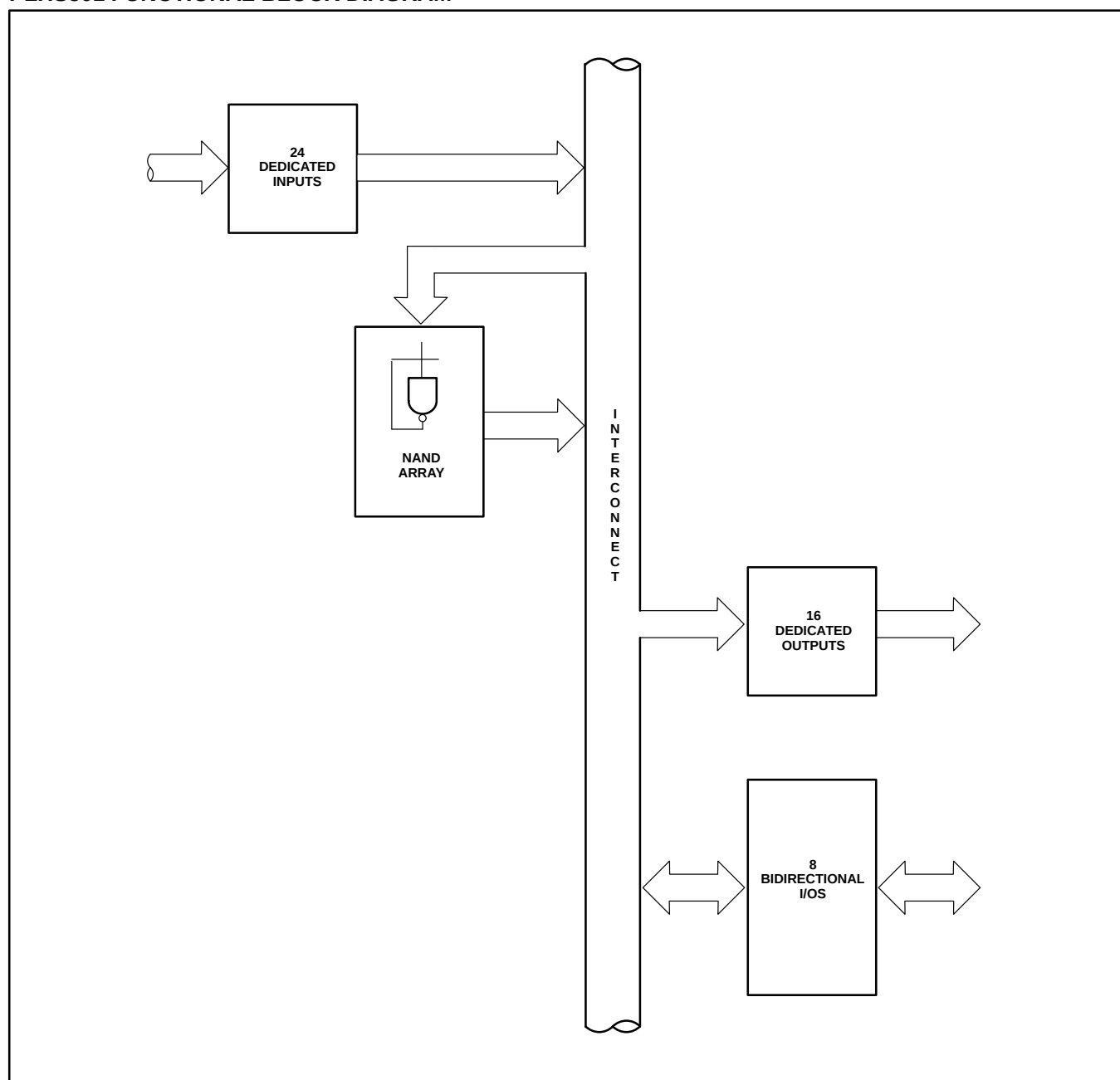
PROGRAMMING/SOFTWARE SUPPORT

Refer to Section 9 (*Development Software*) and Section 10 (*Third-party Programmer/Software Support*) of this data handbook for additional information.

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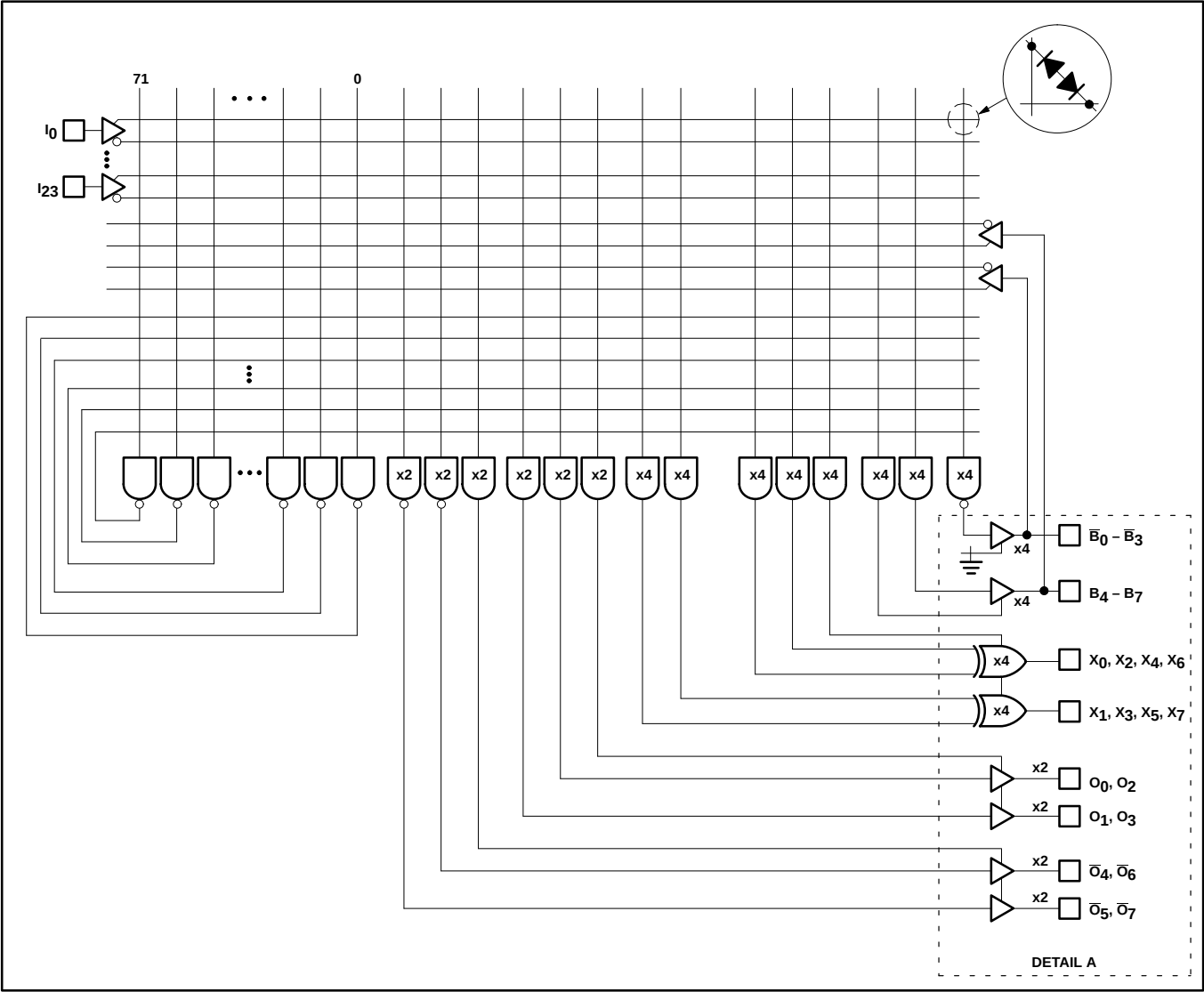
PLHS501 FUNCTIONAL BLOCK DIAGRAM



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FUNCTIONAL DIAGRAM

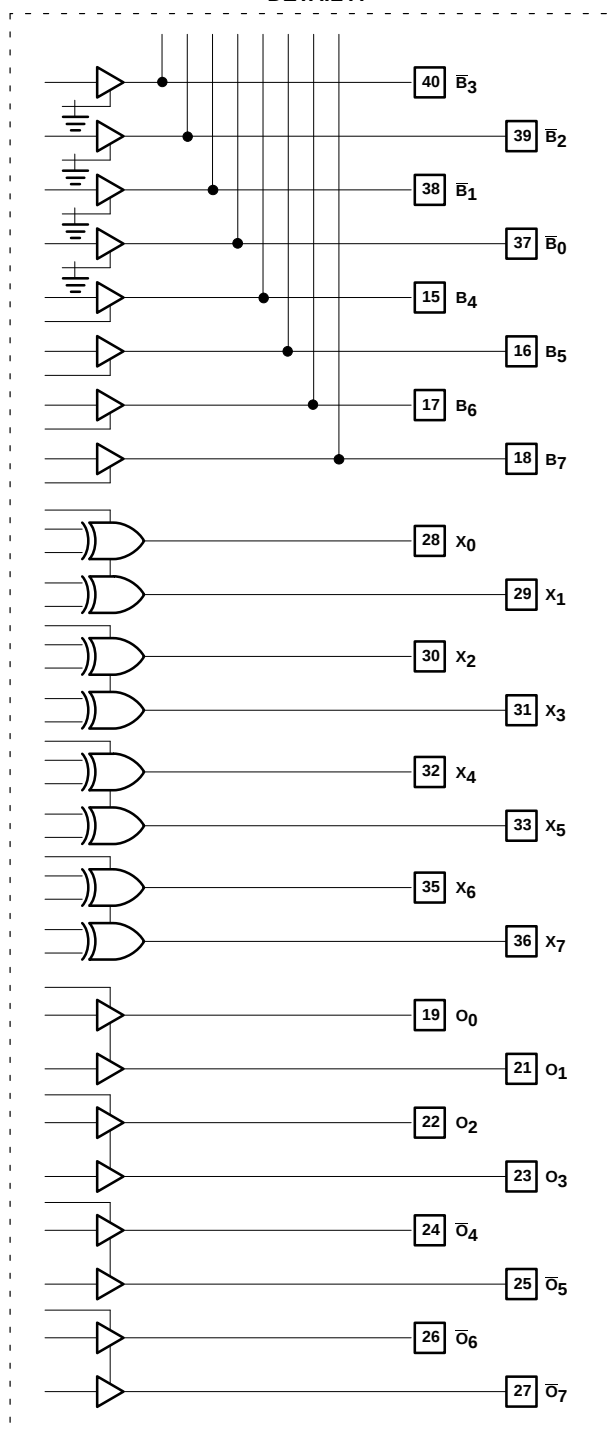


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DETAIL A



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ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V _{CC}	Supply voltage		+7	V _{DC}
V _{IN}	Input voltage		+5.5	V _{DC}
V _{OUT}	Output voltage		+5.5	V _{DC}
I _{IN}	Input currents	−30	+30	mA
I _{OUT}	Output currents		+100	mA
T _{amb}	Operating temperature range	0	+75	°C
T _{stg}	Storage temperature range	−65	+150	°C

NOTE:

- Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

VIRGIN STATE

A factory shipped virgin device contains all fusible links open, such that:

- All product terms are enabled.
- All bidirectional (B) pins are outputs.
- All outputs are enabled.
- All outputs are Active-High **except** $\overline{B}_0 - \overline{B}_3$ (fusible I/O) and $\overline{O}_4 - \overline{O}_7$ which are Active-Low.

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DC ELECTRICAL CHARACTERISTICS

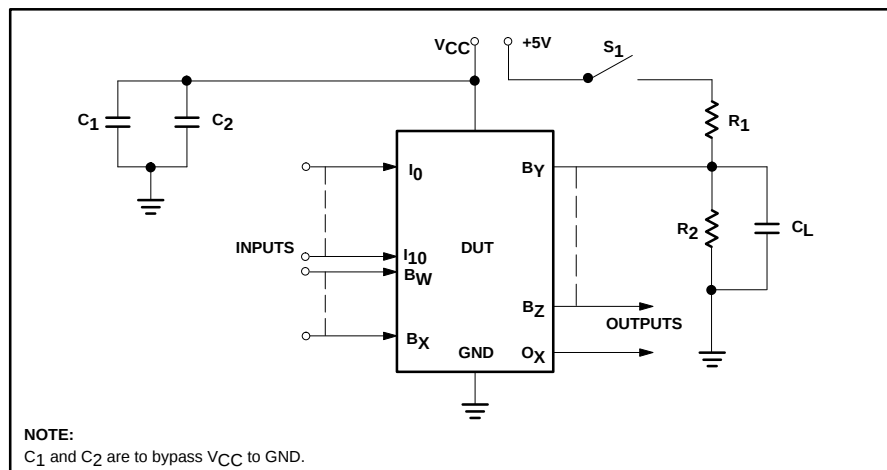
Commercial= $0^{\circ}\text{C} \leq T_{\text{amb}} \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$ Industrial = $-40^{\circ}\text{C} \leq T_{\text{amb}} \leq +85^{\circ}\text{C}$, $4.5\text{V} \leq V_{\text{CC}} \leq 5.5\text{V}$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN	TYP ¹	MAX	
Input voltage ²						
V _{IL} V _{IH} V _{IC}	Low High Clamp ^{2, 3}	V _{CC} = MIN V _{CC} = MAX V _{CC} = MIN, I _{IN} = −12mA	2.0		0.8 −0.8 −1.2	V V V
Output voltage						
V _{OL} V _{OH}	Low ^{2, 4} High ^{2, 5}	V _{CC} = MIN I _{OL} = 10mA I _{OH} = −2mA	2.4		0.45	V V
Input current						
I _{IL} I _{IH}	Low High	V _{CC} = MAX V _{IN} = 0.45V V _{IN} = 5.5V			−100 40	μA μA
Output current						
I _{O(OFF)} I _{OS}	Hi-Z state ⁹ Short circuit ^{3, 5, 6}	V _{CC} = MAX V _{OUT} = 5.5V V _{OUT} = 0.45V V _{OUT} = 0V	 −15		80 −140 −70	μA mA
I _{CC}	V _{CC} supply current ⁸	V _{CC} = MAX		225	295	mA
Capacitance						
C _{IN} C _B	Input I/O	V _{CC} = 5V V _{IN} = 2.0V V _{OUT} = 2.0V		8 15		pF pF

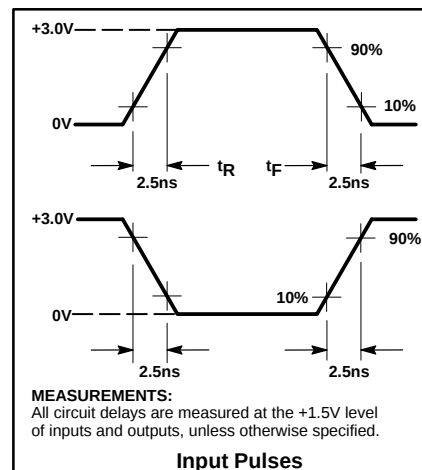
NOTES:

1. All typical values are at $V_{\text{CC}} = 5\text{V}$, $T_{\text{amb}} = +25^{\circ}\text{C}$.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. For Pins 15 – 19, 21 – 27 and 37 – 40, V_{OL} is measured with Pins 5 and 41 = 8.75V, Pin 43 = 0V and Pins 42 and 44 = 4.5V. For Pins 28 – 33 and 35 – 36, V_{OL} is measured under same conditions EXCEPT Pin 44 = 0V.
5. V_{OH} is measured with Pins 5 and 41 = 8.75V, Pins 42 and 43 = 4.5V and Pin 44 = 0V.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with all dedicated inputs at 0V and bidirectional and output pins open.
8. Measured at $V_{\text{T}} = V_{\text{OL}} + 0.5\text{V}$.
9. Leakage values are a combination of input and output leakage.

TEST LOAD CIRCUITS



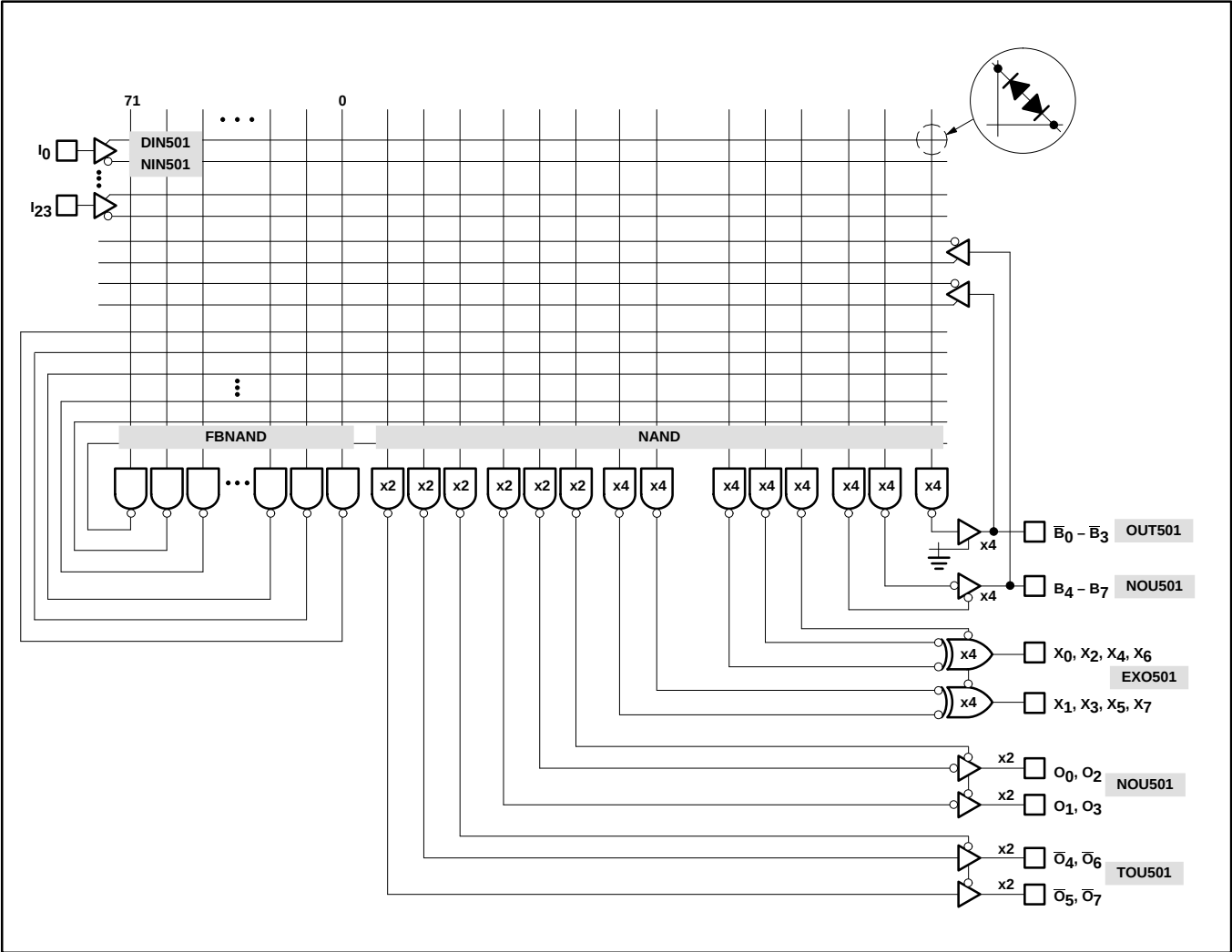
VOLTAGE WAVEFORMS



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SNAP RESOURCE SUMMARY DESIGNATIONS



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MACRO CELL SPECIFICATIONS¹ (SNAP Resource Summary Designations in Parantheses)

Commercial: $T_{amb} = 0^{\circ}\text{C}$ to $+75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$, $C_L = 30\text{pF}$, $R_2 = 1000\Omega$, $R_1 = 470\Omega$ Industrial: $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$, $C_L = 30\text{pF}$, $R_2 = 1000\Omega$, $R_1 = 470\Omega$

Input Buffer (DIN501 [Non-inverting], NIN501 [Inverting])



SYMBOL	LIMITS			UNIT
	MIN	TYP	MAX	
Δt_{HL}	0.05	0.1	0.15	ns/p-term
Δt_{LH}	-0.02	-0.05	-0.08	ns/p-term

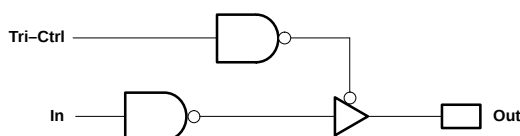
SYMBOL	PARAMETER		LIMITS			UNIT	NOTES
	To (Output)	From (Input)	MIN	TYP	MAX		
t_{PHL}	X	I	4.5	5.5	6.5	ns	With 0 p-terms load
t_{PLH}	X	I	5	6	7.5	ns	
t_{PHL}	Y	I	2.5	3	3.5	ns	With 0 p-terms load
t_{PLH}	Y	I	4	4	4.5	ns	

Input Pins: 1 – 7, 9 – 14, 41 – 45, 48 – 52.

Bidirectional Pins: 15 – 18, 37 – 40.

Maximum internal fan-out: 16 p-terms on X or Y.

NAND Output Buffer with 3-State Control (TOU501)



SYMBOL	PARAMETER		LIMITS			UNIT
	To (Output)	From (Input)	MIN	TYP	MAX	
t_{PHL}	Out	In	8.5	14.0	17.5	ns
t_{PLH}	Out	In	8.5	14.0	16	ns
t_{OE}^2	Out	Tri-Ctrl	8.5	15	18.5	ns
t_{OD}^2	Out	Tri-Ctrl	8.5	12.5	17.0	ns

Output Pins: 24 – 27.

Internal Foldback NAND (FBNAND)



SYMBOL	LIMITS			UNIT
	MIN	TYP	MAX	
Δt_{PHL}	0.05	0.1	0.15	ns/p-term
Δt_{PLH}	-0.0	-0.05	-0.1	ns/p-term

SYMBOL	PARAMETER		LIMITS			UNIT	NOTES
	To (Output)	From (Input)	MIN	TYP	MAX		
t_{PHL}	Out	Any	4.0	4.5	6.8	ns	With 0 p-terms load
t_{PLH}	Out	Any	5.5	6.5	8	ns	

Maximum internal loading of 16 terms.

Notes are on following page.

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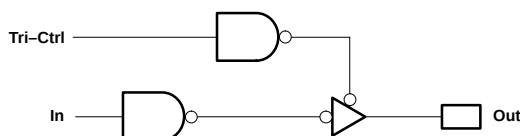
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MACRO CELL SPECIFICATIONS¹ (Continued) (SNAP Resource Summary Designations in Parantheses)

Commercial: $T_{amb} = 0^{\circ}\text{C}$ to $+75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$, $C_L = 30\text{pF}$, $R_2 = 1000\Omega$, $R_1 = 470\Omega$ Industrial: $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$, $C_L = 30\text{pF}$, $R_2 = 1000\Omega$, $R_1 = 470\Omega$

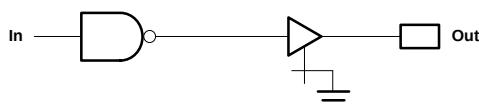
AND Output Buffer with 3-State Control (NOU501)



SYMBOL	PARAMETER		LIMITS			UNIT
	To (Output)	From (Input)	MIN	TYP	MAX	
t_{PHL}	Output	In	8.0	11	13	ns
t_{PLH}	Output	In	8.0	11	13	ns
t_{OE}^2	Out	Tri-Ctrl	8.5	15	18.5	ns
t_{OD}^2	Out	Tri-Ctrl	8.5	12.5	17.0	ns

Bidirectional and Output Pins: 19, 21, 22, 23, 15 – 18.

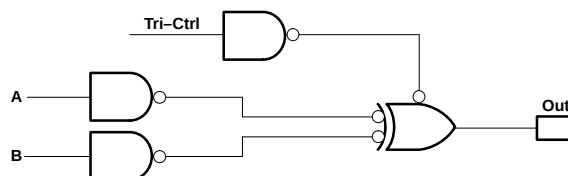
NAND Output Buffer (OUT501)



SYMBOL	PARAMETER		LIMITS			UNIT
	To (Output)	From (Input)	MIN	TYP	MAX	
t_{PHL}	Out	In	8.5	14	17.5	ns
t_{PLH}	Out	In	8.5	14	16.0	ns

Bidirectional Pins: 37 – 40.

Ex-OR Output Buffer (EXO501)



SYMBOL	PARAMETER		LIMITS			UNIT
	To (Output)	From (Input)	MIN	TYP	MAX	
t_{PHL}	Out	A or B	8.5	14	17.5	ns
t_{PLH}	Out	A or B	8.5	14	16.0	ns
t_{OE}^2	Out	Tri-Ctrl	8.5	15	18.5	ns
t_{OD}^2	Out	Tri-Ctrl	8.5	12.5	17.0	ns

Ex-OR Output Pins: 28 – 33.

NOTES:

- Limits are guaranteed with internal feedback buffers simultaneously switching cumulative maximum of eight outputs.
- For 3-State output; output enable times are tested with $C_L = 30\text{pF}$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5\text{pF}$. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5\text{V})$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5\text{V})$ level with S_1 closed.

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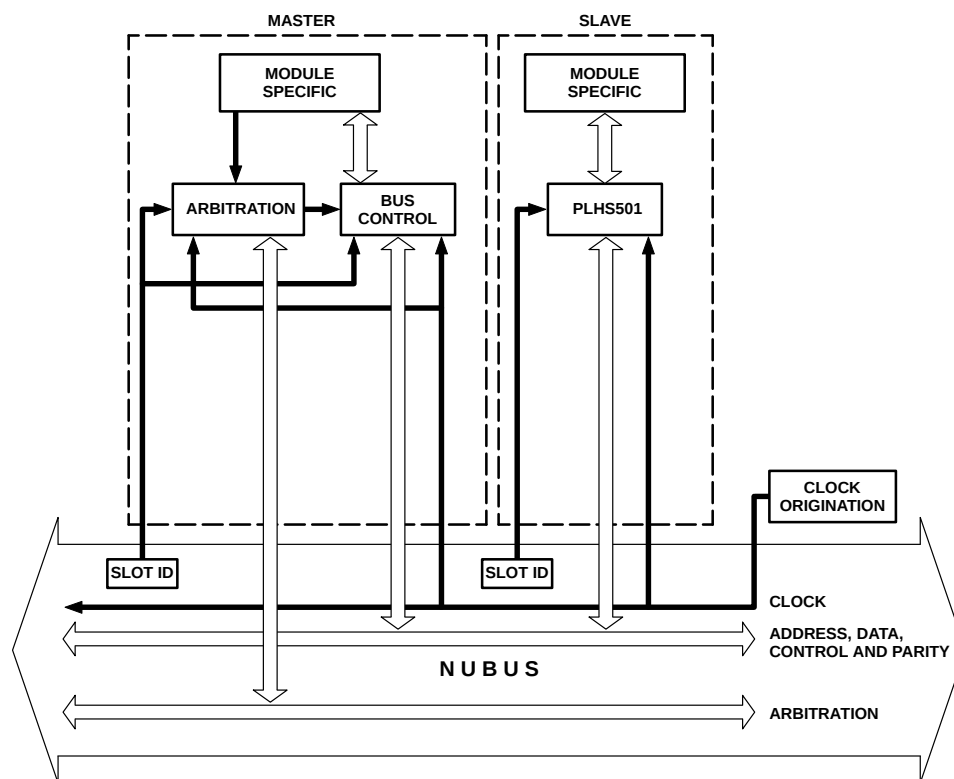
PLHS501 GATE AND SPEED ESTIMATE TABLE

FUNCTION	INTERNAL NAND EQUIVALENT	TYPICAL t_{PD}	f_{MAX}	COMMENTS
Gates				
NANDs	1	6.5ns		For 1 to 32 input variables
ANDs	1	6.5ns		For 1 to 32 input variables
NORs	1	6.5ns		For 1 to 32 input variables
ORs	1	6.5ns		For 1 to 32 input variables
Decoders				
3-to-8	8	11ns		Inverted inputs available
4-to-16	16	11ns		Inverted inputs available
5-to-32	32	11ns		Inverted inputs available (24 chip outputs only)
Encoders				
8-to-3	15	11ns		Inverted inputs, 2 logic levels
16-to-4	32	11ns		Inverted inputs, 2 logic levels
32-to-5	41	11ns		Inverted inputs, 2 logic levels, factored solution.
Multiplexers				
4-to-1	5	11ns		Inverted inputs available
8-to-1	9	11ns		
16-to-1	17	11ns		
27-to-1	28	11ns		Can address only 27 external inputs - more if internal
Flip-Flops				
D-type Flip-Flop	6		30MHz	With asynchronous S-R
T-type Flip-Flop	6		30MHz	With asynchronous S-R
J-K-type Flip-Flop	10		30MHz	With asynchronous S-R
Adders				
8-bit	45	15.5ns		Full carry-lookahead (four levels of logic)
Barrel Shifters				
8-bit	72	11ns		2 levels of logic
Latches				
D-latch	3			2 levels of logic with one shared gate

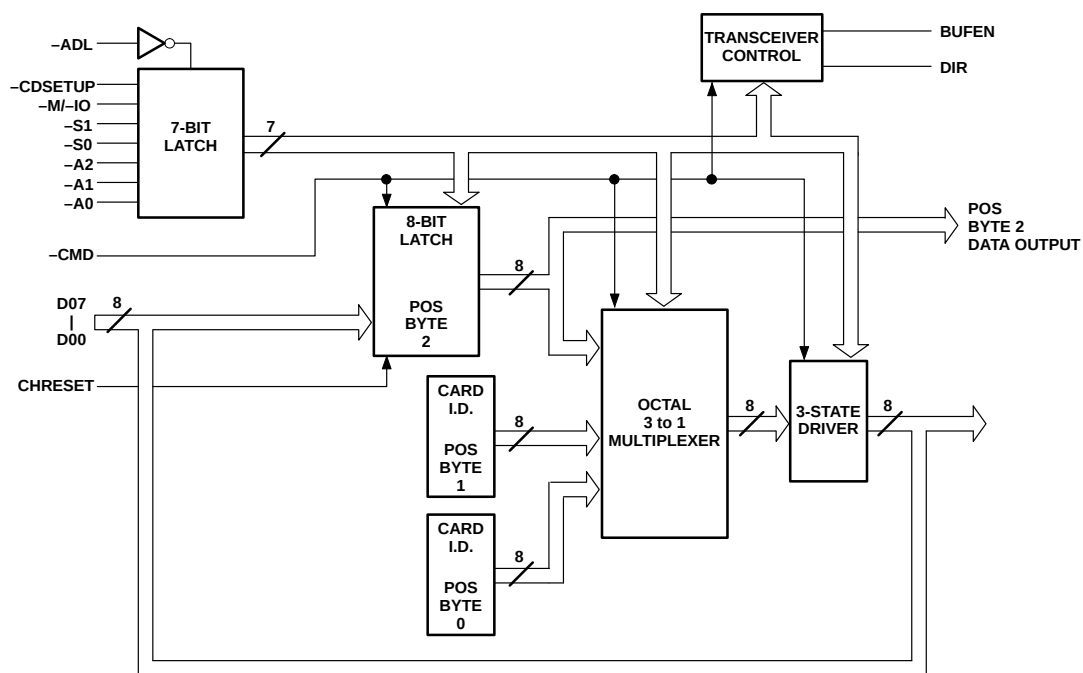
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APPLICATIONS



Simplified NuBus™ Diagram (10MHz Operating Frequency)



Block Diagram of Basic POS Implementation in PLHS501