PROMISE®
TECHNOLOGY, INC.

PDC20621

PCI Bus Mastering

ATA RAID Accelerator

Programming Guide for

Fastrak Sx4 Applications

Revision 1.2

Powered by PROMISE ATA RAID

1 CHANGE HISTORY

Draft Rev. 0.0: ---------- May. 15, 1999

2 INTRODUCTION

The PDC20621 ASIC that created by PROMISE Technology is a PCI bus mastering RAID 0/1/10/3/5 engine that supports hardware commands for ATA/ATAPI and XOR operation to accelerate ATA-RAID system. It communicates with the PCI bus using burst bus mastering and advanced packet command based scatter/gather mechanism, and up to 2GB local DIMM supports for caching algorithm to enhance overall system performance. In addition, PROMISE Technology provides a 32-bit software driver that supports 32-bit operating system functionality.

3 FEATURES

3.1 GENERAL

1. Highly system level integration that available in a 388-pin Ball Grid Array Package (BGA) adopting high speed CMOS technology.
2. Single chip, high performance ATA-RAID implementation for easy integrated on to motherboards and occupying less board space in add-on cards.
3. Bus mastering design takes full advantage of multi-tasking, multi-threading operating systems and greatly improves performance.
4. Supports a Chip-to-Chip (C2C©) bus to do cross chip registers setting for multiple PDC20621 application.
5. Master and companion mode configurable that is flexible to expand available HDD up to sixteen into a multiple PDC20261 RAID system, which also can co-operation with a local SA-110 RISC processor to form an intelligent hardware RAID.
6. Provides extended Memory Mapped I/O programming Interface that can be applied to some platforms which without I/O space addressing capability.

3.2 HOST INTERFACE

1. Triple pin-shared host interface can be supported. There is PCI-Device mode to connect PDC20621 to a standard PCI bus to form a host based RAID organization. A PCI- Bridge mode to connect to others PCI controller, up to two dedicated PCI controller can be arbitrated, that like as PCI interface SCSI controller or PCI Ethernet controller to form a device based RAID system. Finally, or direct interface to Strong-ARM RISC to form a hardware RAID. All of there can be selected by hardware strap for various system organizations.
2. PCI mode host interface that complies with PCI Local Bus Specification Revision 2.2.
3. PCI mode host interface that provides PCI Power Management 1.1 capability.
4. Supports 32-bit PCI bus master with zero wait burst protocol, bus speed up to 66 MHz and provides 267

MB/sec sustained transfer rate.

5. Supports full set of configuration headers for easy implementation of plug and play BIOS features.
6. Programmable Device ID, sub-system vendor ID & sub-system device ID, which will be automatic, fetched from local flash memory after system RESET#.
7. Provides mechanism to use single flash memory to support PCI BIOS and F/W for local SA-110 RISC.
8. Provides mechanism to detect how clock frequency the PCI bus supported, this information can be used to adjust internal PLL to generate a suitable system clock for reliable operation even bus over speed operation.
9. Local processor's program and data memory can be shadowed to DIMM to enhance performance.

3.3 RAID ENGINE

1. Provides advanced packet command based Scatter/Gather queuing that is optimization for XOR, host DMA and four independent ATA/ATAPI operations. Process data from local DIMM to broken data transfer bandwidth bottleneck.
2. Supports direct interface for external low power SRAM. When backed by battery that can keep some log files for RAID status records.
3. Supports special protocol to monitoring status that like as FAN, temperature, etc. from external hot-swap RAID box and can send control signal to box for turn on/off POWER, turn on/off status LED and so on.

3.4 ATA/ATAPI INTERFACE

1. Compatible with the latest PCI IDE, ATA/ATAPI-6 and enhanced IDE specifications. Have primary, secondary, tertiary and quaternary ATA/ATAPI controller built into a single chip, supporting up to four concurrent ATA operations in a single PDC20621 controller.
2. Supports ATA and ATAPI proposal PIO Mode 0, 1, 2, 3, 4, DMA Mode 0, 1, 2 and Ultra DMA Mode 0, 1, 2, 3, 4, 5. The IDE drive transfer rate is capable of up to 100 MB/sec per channel.
3. Supports large LBA ATA command format.
4. Uses slew rate controlled I/O pad to minimize ATA bus close-talk effect.
5. Automatically detects whether or not the cable is suitable for mode 3, 4, 5 of Ultra DMA.
6. Supports four individual IDE channel, access timings and protocols for four drives attached to IDE bus.
7. Independent access timing for Task-register and data register.
8. Both of hardware and software that can set access timing for data transfer. Timing parameter for PIO, DMA, & UDMA, optimize for

100 MHz clock, can be set to timing register automatically after "Set Feature Command" when the corresponding sub-command is "Set Transfer Mode".

9. Supports external clock to overcome drives timing problem when PCI clock over speed.
10. Supports IDE drives hot plugging capability.

3.5 MEMORY INTERFACE

1. The SDRAM controller supports 2-DIMM/8-Bank of 3.3V SDRAM. The maximum memory size supported per bank is 256MB, with a total of 2GB local memory.
2. The memory clock frequency is operated up to 100MHz and in the synchronous mode with respect to the PDC20621 internal frequency. For power saving or during system power crash, the SDRAM will be put into suspend mode by controller when SDRAM power backed by battery.
3. Distributed on-chip bus arbitration for multiple PDC20621 access to DIMM. For single controller application, this on-chip arbitration can be disable. (Patent Claiming Required)
4. The SDRAM controller supports that PC-100 SDRAM, 1Gbytes/s transfer rate over memory bus. All timing parameter can be setting up using SPD or memory check utility.
5. Provides hardware single bit error recovers and two bits error detects ECC when to access ECC-DIMM, this function can be enabled or disabled by software.
6. Direct interface to external SRAM up to 64KB.
7. Direct interface to external flash memory up to 128KB for PCI BIOS purpose, or up to 2M Bytes for local SA-110.

3.6 MISCELLANEOUS

1. Supports 16 GPIO ports, one of the output pin that is designed for programmed frequency generator.
2. Supports Auto Serial interface.
3. Supports keypads scan functions that can supports for 4-key input.
4. GPIO, Serial interface, & 4-key are exclusive shared with flash memory interface.
5. Supports direct interface to control UART & LCD controller, access timing is programmable.
6. Compliance with the PC2001, WHQL hardware requirements.
7. Comes with installation utility program and device drivers for Windows 95/98/ME, Windows NT/2000, Linux, & NetWare.
8. Direct control to optional external BIOS that allows it to support drives larger than 128GB. When drives that can support large LBA format command, 281 tera sectors will be address.
9. Come with design reference materials - Application schematics, Gerber file, BIOS, and application notes.

4 REGISTERS DESCRIPTION

The following illustrated programmable registers defined in PDC20621.

4.1 PCI configuration register

Offset	[31:24]	[23:16]	[15:8]	[7:0]
00h	*Device ID (6621h)*		*Vendor ID (105Ah)*	
04h	Status (02b0h)		Command (0000h)	
08h	Class Code (010485h)			*Revision ID (01h)*
0Ch	*Reserved*	*Header Type (00h)*	Latency Timer (00h)	CacheLine Size (00h)
10h	Base Address register #0, for ATA (8001h)			
14h	Base Address register #1, for XOR, HOST DMA, Chip (8101h)			
18h	Base Address register #2, for Sequence Control (8201h)			
1Ch	Base Address register #3, for memory resources#1 (FLASH, SRAM, and memory mapped IO) (00800000h)			
20h	Base Address register #4 for memory resources#2 (SDRAM) (80000000h)			
24h	Base Address register #5 (Reserved)			
2Ch	Sub-System Device ID (6621h)		Sub-System Vendor ID (105Ah)	
30h	Expansion ROM Register (00080000h)			
34h	*Reserved*			*Cap_Ptr (60h)*
3Ch	Max_LAT (12h)	Min_GNT (04h)	*Interrupt Pin (01h)*	Interrupt Line (0Eh)
40h	Reserved	Sub-system ID read only (0b)	Retry timer (00h)	Target ready timer (00h)
60h	*Power Management Capabilities (0221h)*		*Next Item Ptr (00h)*	*Capability ID (01h)*
64h	*Data (00h)*	*PMCSR_BSE Bridge Support Extensions (00h)*	*Power Management Control/Status Register*	
Others	*Reserved*			

* Latency Timer “00h” that implied burst disabled, so software have to check this register when chip initialization.

* *Italic that indicates Read Only field.* Highlight with pink color is RESET# default value.

* The target ready timer on offset 40h is the maximum number of clock for bus master waiting TRDY#

* The Retry timer on offset 41h is the maximum number of retries before abort for bus master.

* Sub-system ID read only. This bit will set the Sub-system Device ID and Sub-system Vender ID on offset 40h to read only.

4.2 Power Management Register Block Definition

This section describes the PCI Power Management Interface registers.

Table 8.1 illustrates the organization of the PCI Power Management Register Block. The first 16 bits (Capabilities ID and Next Item Pointer) are used for the linked list infrastructure.

The next 32 bits (*PMC* and *PMCSR* registers) are required for compliance with this specification. The next 8-bit register (bridge support *PMCSR* extensions) is required only for bridge functions, and the remaining 8-bit *Data* register is optional for any class of function. As with all PCI configuration registers, these registers may be accessed as bytes, 16-bit words, or 32-bit DWORDs.

Unless otherwise specified, all write operations to reserved registers must be treated as no-ops; that is, the access must be completed normally on the bus and the data discarded.

Read accesses to reserved or unimplemented registers must be completed normally and a data value of 0 returned.

Offset = 60h	Power Management Capabilities (PMC)		Next Item Ptr	Capability ID
Offset = 64h	Data	PMCSR_BSE Bridge Support Extensions	Power Management Control/Status Register (PMCSR)	

Table 8.1: Power Management Register Block

The offset for each register is listed as an offset from the beginning of the linked list item which is determined either from the *Cap_Ptr* (If Power Management is the first item in the list) or the *Next_Item_Ptr* of the previous item in the list.

Capability Identifier - Cap_ID (Offset = 60h)

The *Capability Identifier,* when read by system software as 01h indicates that the data structure currently being pointed to is the PCI Power Management data structure. Each function of a PCI device may have only one item in its capability list with *Cap_ID* set to
01h.

Bits	Value	Type	Description
7:0	***01h***	*Read Only*	***ID*** *- This field, when "01h" identifies the linked list item as being the PCI Power Management registers.*

Next Item Pointer - Next_Item_Ptr (Offset = 61h)

The *Next Item Pointer* register describes the location of the next item in the function's capability list. The value given is an offset into the function's PCI Configuration Space.

If the function does not implement any other capabilities defined by the PCI SIG for inclusion in the capabilities list, or if power management is the last item in the list, then this register must be set to 00h.

Bits	Value	Type	Description
7:0	***00h***	*Read Only*	***Next Item Pointer*** *- This field provides an offset into the function's PCI Configuration Space pointing to the location of next item in the function's capability list. If there are no additional items in the Capabilities List, this*

			register is set to 00h

PMC - Power Management Capabilities (Offset = 62h)

The *Power Management Capabilities* register is a 16-bit read-only register that provides information on the capabilities of the function related to power management.

The information in this register is generally static and known at design time.

Bits	***Value***	Type	***Description***
15:11	***00000b***	*Read Only*	***PME_Support*** *– This 5-bit field indicates the power states in which the function may assert* ***PME#****. A value of 0b for any bit indicates that the function is not capable of asserting the* ***PME#*** *signal while in that power state.* *bit(11) XXXX1b -* ***PME#*** *can be asserted from* ***D0*** *bit(12) XXX1Xb -* ***PME#*** *can be asserted from* ***D1*** *bit(13) XX1XXb -* ***PME#*** *can be asserted from* ***D2*** *bit(14) X1XXXb -* ***PME#*** *can be asserted from* ***D3 hot*** *bit(15) 1XXXXb -* ***PME#*** *can be asserted from* ***D3 cold***
10	***0b***	*Read Only*	***D2_Support*** *- If this bit is a "1", this function supports the* ***D2*** *Power Management State.* *Functions that do not support* ***D2*** *must always return a value of "0" for this bit.*
9	***1b***	*Read Only*	***D1_Support*** *- If this bit is a "1", this function supports the* ***D1*** *Power Management State.* *Functions that do not support* ***D1*** *must always return a value of "0" for this bit.*
8:6	***000b***	*Read Only*	***Reserved***
5	***1b***		***DSI*** *- The Device Specific Initialization bit indicates whether special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it.* *Note that this bit is not used by some operating systems. Microsoft Windows and Windows NT, for instance, do not use this bit to determine whether to use* ***D3****. Instead, they use the driver's capabilities to determine this.* *A "1" indicates that the function requires a device specific initialization sequence following transition to the* ***D0*** *uninitialized state. Refer to Section 8.3.*
4	***0b***	*Read Only*	*Reserved*
3	***0b***	*Read Only*	***PME Clock*** *– When this bit is a "1", it indicates that the function relies on the presence of the PCI clock for* ***PME#*** *operation.* *When this bit is a "0", it indicates that no PCI clock is required for the function to generate* ***PME#.*** *Functions that do not support* ***PME#*** *generation in any state must return "0" for this field.*
2:0	***001b***	*Read Only*	***Version*** *- A value of 001b indicates that this function complies with Revision 1.1 of the PCI Power Management Interface Specification.*

PMCSR - Power Management Control/Status (Offset = 63h)

This 16-bit register is used to manage the PCI function's power management state as well as to enable/monitor PMEs.

The PME support bits, **PME_Status** and **PME_En**, are defined to be sticky bits for functions that can generate

PMEs from ***D3cold***, in that their states are not affected by power on reset or transitions from ***D3cold*** to the ***D0*** Uninitialized state. Preservation of these bits is typically achieved by either powering them with an auxiliary power source, or by using non-volatile storage cells for them. The only way to clear out these bits is to have system software write to them with the appropriate values.

As mentioned previously, the PME Context is defined as the logic responsible for identifying PMEs, the logic responsible for generating the **PME#** signal, and the bits within this register that provide the standard system interface for this functionality. PME Context also contains any device class specific status that must survive the transition to the ***D0*** Uninitialized state as well.

If a function supports **PME#** generation from ***D3cold***, its PME Context is not affected by either a PCI Bus Segment Reset (hardware component reset) or the internal "soft" re-initialization that occurs when restoring a function from ***D3hot***. This is because the function's PME functionality itself may have been responsible for the wake event which caused the transition back to ***D0***. Therefore, the PME Context must be preserved for the system software to process.

If **PME#** generation is not supported from ***D3cold*** , then all PME Context is initialized with the assertion of a bus segment reset.

Because a PCI bus **RST#** assertion does not necessarily clear all functions' PME Context (functions that support **PME#** from ***D3cold***), the system software is required to explicitly initialize all PME Context, including the PME support bits, for all functions during initial operating system load. In terms of the *PMCSR*, this means that during the initial operating system load each function's **PME_En** bit must be written with a "0", and each function's **PME_Status** bit must be written with a "1" by system software as part of the process of initializing the system.

Bits	***Value***	Type	***Description***
15	***0b***	*Read Only*	***PME_Status*** *- This bit is set when the function would Normally assert the* ***PME#*** *signal independent of the state of the* ***PME_En*** *bit.* *Writing a "1" to this bit will clear it and cause the function to stop asserting a* ***PME#*** *(if enabled). Writing a "0" has no effect.* *This bit defaults to "0" if the function does not support* ***PME#*** *generation from* ***D3 cold*** *.* *If the function supports* ***PME#*** *from* ***D3 cold*** *, then this bit is sticky and must be explicitly cleared by the operating system each time the operating system is initially loaded.*
14:13	***00b***	*Read Only*	***Data_Scale*** *- This 2-bit read-only field indicates the scaling factor to be used when interpreting the value of the Data register. The value and meaning of this field will vary depending on which data value has been selected by the* ***Data_Select*** *field.* *This field is required for any function that implements the Data register; otherwise it is optional. See Section 3.2.6 for more details.*
12:9	***0000b***	*Read Only*	***Data_Select*** *- This 4-bit field is used to select which data is to be reported through the Data register and* ***Data_Scale*** *field.* *This field is required for any function that implements the Data register. Otherwise it is optional.*
8	***0b***	*Read Only*	***PME_En*** *- A "1" enables the function to assert* ***PME#.*** *When "0",* ***PME#*** *assertion is disabled.* *This bit defaults to "0" if the function does not support* ***PME#*** *generation from* ***D3 cold*** *.*

			*If the function supports **PME#** from **D3 cold** , then this bit is sticky and must be explicitly cleared by the operating system each time it is initially loaded.*
7:2	***000000b***	*Read Only*	***Reserved***
1:0	***RRb*** ***"R" for Register Value***	*Read/ Write*	***PowerState** - This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. The definition of the field values is given below.* *00b - **D0*** *01b - **D1*** *10b - **D2*** *11b - **D3 hot*** *If software attempts to write an unsupported, optional state to this field, the write operation must complete normally on the bus; however, the data is discarded and no state change occurs.* *Any state other than D0 will power down the PLL of PDC20621.*

PMCSR_BSE - PMCSR PCI to PCI Bridge Support Extensions (Offset = 66h)

PMCSR_BSE supports PCI bridge specific functionality and is required for all PCI-to-PCI bridges.

Bits	***Value***	Type	***Description***
7	***0b***	*Read Only*	**BPCC_En (Bus Power/Clock Control Enable)** - A "1" indicates that the bus power/clock control mechanism as defined in Section 4.7.1 is enabled. A "0" indicates that the bus power/clock control policies defined in Section 4.7.1 have been disabled. When the Bus Power/Clock Control mechanism is disabled, The bridge's *PMCSR* **PowerState** field cannot be used by the system software to control the power or clock of the bridge's secondary bus.
6	***0b***	*Read Only*	**B2_B3# (*B2/B3 support for D3hot*)** - The state of this bit determines the action that is to occur as a direct result of programming the function to ***D3hot***. A "1" indicates that when the bridge function is programmed to ***D3hot***, its secondary bus's PCI clock will be stopped (***B2***). A "0" indicates that when the bridge function is programmed to ***D3hot***, its secondary bus will have its power removed (***B3***). This bit is only meaningful if bit 7 (BPCC_En) is a "1". See Section 4.7.1 for details.
5:0	***000000b***	*Read Only*	**Reserved**

Data (Offset = 67h)

The *Data* register is an optional, 8-bit read-only register that provides a mechanism for the function to report state dependent operating data such as power consumed or heat dissipation. Typically the data returned through the *Data* register is a static copy (look up table, for example) of the function's worst case "DC characteristics" data sheet. This data, when made available to system software, could then be used to intelligently make decisions about power

budgeting, cooling requirements, etc.

Any type of data could be reported through this register, but only power usage is defined by this version of the specification.

If the *Data* register is implemented, then the **Data_Select** and **Data_Scale** fields must also be implemented. If this register is not implemented, a value of 0 should always be returned by this register as well as for the **Data_Select** and **Data_Scale** fields.

Bits	***Our Value***	Type	***Description***
7:0	***00h***	*Read Only*	**Data** - This register is used to report the state dependent data requested by the **Data_Select** field. The value of this register is scaled by the value reported by the **Data_Scale** field.

4.3 ATA Control Register (Base Address Register#0)

Register Definition

	Byte3	Byte2	Byte1	Byte0
00h	IDE#0 Start Address[31:0]			
04h	IDE#0 Control & Status Port			
08h	Reserved			IDE#0 Index
0Ch	IDE#0 Data Port			
10h	IDE#1 Start Address[31:0]			
14h	IDE#1 Control & Status Port			
18h	Reserved			IDE#1 Index
1Ch	IDE#1 Data Port			
20h	IDE#2 Start Address[31:0]			
24h	IDE#2 Control & Status Port			
28h	Reserved			IDE#2 Index
2Ch	IDE#2 Data Port			
30h	IDE#3 Start Address[31:0]			
34h	IDE#3 Control & Status Port			
38h	Reserved			IDE#3 Index
3Ch	IDE#3 Data Port			

IDE Command Packet Control Register Definition (00h ~ FFh)

	Byte3	Byte2	Byte1	Byte0
0h	IDE Start Address[31:0]			
4h	IDE Control & Status			
8h	Reserved			IDE Index
Ch	IDE Data Port			

IDE Start Address Port

31:3 (r/w)	2:0 (r)
IDE Start Address Port	000b

Bit[31:3]: This register is command packet start address. See Channel #0 IDE Command Packet Pointer Register (index_IDE0:40h | BA#3 + C0240h).

Bit[2:0]: Reserved.

IDE Control & Status Port

31:0 (r/w)
IDE Control & Status Port

Bit[31:0]: See Channel #0 Global Control & Status Register (CGCR0) (index_IDE0: 48h | MMIO: BA#3 + C0248h).

IDE Index Port

7 (r)	6:2 (r/w)	1:0 (r)
Reserved	IDE Index Port	00b

Bit[7]: Reserved.

Bit[6:2]: Index address Port for ATA Control Registers.

Bit[1:0] Reserved.

IDE Data Port

31:0 (r/w)
IDE Data Port

Bit[31:0]: IDE Data Port.

4.4 XOR/Host DMA/Host Control Register (Base Address Register#1)

	Byte3	Byte2	Byte1	Byte0
00h	DMA Start Address[31:0]			
04h	DMA Control & Status Port			
08h	Reserved			DMA Index
0Ch	DMA Data Port			
3Fh~10h	Reserved			
40h	XOR Start Address[31:0]			
44h	XOR Control & Status Port			
48h	Reserved			XOR Index
4Ch	XOR Data Port			
7F~50h	Reserved			
80h	Reserved			
84h	Reserved			
88h	Reserved			Chip index
8Ch	Chip Data port			

4.4.1 DMA Command Packet Control Register Definition (00h ~ 3Fh)

	Byte3	Byte2	Byte1	Byte0
0h	DMA Start Address[31:0]			
4h	DMA Control & Status Port			
8h	Reserved			DMA Index
Ch	DMA Data Port			

DMA Start Address Port

31:3 (r/w)	2:0 (r)
DMA Start Address Port	000b

Bit[31:3]: See HOST DMA Command Packet Pointer Register (index_HDMA:00h | BA#3 + C0100h).

Bit[1:0]: Reserved.

DMA Control & Status Port

31:0 (r/w)
DMA Control & Status Port

Bit[31:0]: See HOST DMA Global Control & Status Register (index_HDMA: 04h | BA#3 + C0104h).

DMA Index Port

7 (r)	6:2 (r/w)	1:0 (r)
Reserved	DMA Index Port	00b

Bit[7]: Reserved.

Bit[5:2]: Index address Port for DMA Control Registers.

Bit[1:0] Reserved.

DMA Data Port

31:0 (r/w)
Host Data Port

Bit[31:0]: DMA Data Port.

4.4.2 XOR Command Packet Control Register Definition (40h ~ 7Fh)

	Byte3	Byte2	Byte1	Byte0
0h	XOR Start Address[31:0]			
4h	XOR Control & Status Port			
8h	Reserved			XOR Index
Ch	XOR Data Port			

XOR Start Address Port

31:3 (r/w)	2:0 (r)
XOR Start Address Port	000b

Bit[31:3]: This register is XOR command packet start address. See XOR Command Packet Pointer Register (index XOR: 00h | BA#3 + C0180h).

Bit[2:0]: Reserved.

XOR Control & Status Port

31:0 (r/w)
XOR Control Port

Bit[31:0]: See .

XOR Index Port

7 (r)	6:2 (r/w)	1:0 (r)
Reserved	XOR Index Port	00b

Bit[7]: Reserved.

Bit[6:2]: Index address Port for XOR Control Registers.

Bit[1:0] Reserved.

XOR Data Port

31:0 (r/w)
XOR Data Port

Bit[31:0]: XOR Data Port.

4.4.3 Chip Control Register Definition (00h ~ 3Fh)

	Byte3	Byte2	Byte1	Byte0
0h	Reserved			
4h	Reserved			
8h	Reserved			Chip Index
Ch	Chip Data Port			

Chip Index Port

7:2 (r)	1:0 (r)
CID Index Port	00b

Bit[7:2]: Index Port for C2C_ID #n Registers.

Bit[1:0]: Reserved.

Chip Data Port

31:0 (r/w)
CID Data Port

Bit[31:0]: Data Port for C2C_ID #n Registers.

4.5 PDC20621 Sequence Control register (Base Address Register#2)

	Byte3	Byte2	Byte1	Byte0
00h	SEQ#0 Control & Status Port			
04h	SEQ#1 Control & Status Port			
08h	SEQ#2 Control & Status Port			
0Ch	SEQ#3 Control & Status Port			
10h	SEQ#4 Control & Status Port			
14h	SEQ#5 Control & Status Port			
18h	SEQ#6 Control & Status Port			
1Ch	SEQ#7 Control & Status Port			
20h	SEQ#8 Control & Status Port			
24h	SEQ#9 Control & Status Port			
28h	SEQ#A Control & Status Port			
2Ch	SEQ#B Control & Status Port			
30h	SEQ#C Control & Status Port			
34h	SEQ#D Control & Status Port			
38h	SEQ#E Control & Status Port			
3Ch	SEQ#F Control & Status Port			
40h	SEQ#10 Control & Status Port			
44h	SEQ#11 Control & Status Port			
48h	SEQ#12 Control & Status Port			
4Ch	SEQ#13 Control & Status Port			
50h	SEQ#14 Control & Status Port			
54h	SEQ#15 Control & Status Port			
58h	SEQ#16 Control & Status Port			
5Ch	SEQ#17 Control & Status Port			
60h	SEQ#18 Control & Status Port			
64h	SEQ#19 Control & Status Port			
68h	SEQ#1A Control & Status Port			
6Ch	SEQ#1B Control & Status Port			
70h	SEQ#1C Control & Status Port			
74h	SEQ#1D Control & Status Port			
78h	SEQ#1E Control & Status Port			
7Ch	SEQ#1F Control & Status Port			
80h	Sequence Interrupt Status Port			
84h	Reserved			
88h	Reserved			C2C ID Assign
8Ch	Reserved			C2C ID Inquire

4.5.1 Sequence Control Register

SEQ#N Control & Status Port

31:0 (r)
SEQ#N Control & Status Port

Bit[31:0]: See Sequence Counter Control Register0 (BA#2: 0h | BA#3 + C0400h).

Sequence Interrupt Status Port

31:0 (r/w)
Sequence Interrupt Status Port

Bit[31:0]: See Sequence Interrupt Status register (BA#2: 80h | BA#3 + C0480h) (Interrupt should be cleared when Bit[31:0] is read).

4.5.2 Chip To Chip Control Register

C2C ID Assign Register

7:4 (w)	3:0 (w)
Reserved	ID Assign Port

Bit[7:0]: See C2C ID Assign Register (BA#2: 88h | BA#3 + C0488h).

C2C ID Inquire Port

7:4 (r)	3 (r)	2 (r)	1 (r)	0 (r)
Reserved	Reserved	Reserved	Reserved	ID Present

Bit[7:0]: See C2C ID Inquire Register (BA#2: 8Ch | BA#3 + C048Ch).

4.6 Extended register

There are extended registers for special purpose and timing adjustment. All of these register can be accessed by memory mapped IO or index IO (addressing by index register and data register contents data).
The base address of memory mapped IO is at [offset 0x1Ch of configuration space, BA#3].
When these registers are accessed by index IO, users must program index register first then R/W the data register and program these registers by double word.

4.6.1 HOST Module Control Register

Host Identification Register (index_CID0: 00h | BA#3 +C0000h)

31:8 (r)	7:4 (r)	3:0 (r)
Reserved	Device ID	Revision ID

Bit[31:9]: Reserved.

Bit[7:4]: Device ID, 0001b for PDC20621. *** Any PCI Device ID changed has to update this ID.

Bit[3:0]: Revision ID, 0001b. *** Any PCI Revision ID changed have to update this ID.

SRAM/Flash Control Register (index_CID0: 04h | BA#3 + C0004h)

31: 30 (r/w)	29:26 (r/w)	25:24 (r/w)	23:22 (r/w)	21:18 (r/w)	17:16 (r/w)
TFAS (11b)	TFPW (1111b)	TFAH (11b)	Tsas (11b)	Tspw (1111b)	TSAH (11b)

15:12 (r/w)	11:8 (r/w)	7:4 (r/w)	3:0 (r/w)
SRAM#1 start address (1000b)	SRAM#1 end address (1111b)	SRAM#0 start address (0000b)	SRAM#0 end address (0111b)

Bit[31:30]: FLASH Address setup time. It defines the minimum time from address valid and FCSN low to FOEN or FWEN low.

Bit[29:26]: FLASH Minimum pulse width. It is the minimum pulse width of FOEN and FWEN.

Bit[25:24]: FLASH Address hold time. It defines the minimum time from FOEN or FWEN high to address transition and FCSN high.

Bit[21:18]: SRAM# Minimum pulse width. It is the minimum pulse width of SOEN/SWEN.

Bit[23:22]: SRAM# Address setup time. It defines the minimum time from address valid and SCSN low to OEN or WEN low.

Bit[17:16]: SRAM# Address hold time. It defines the minimum time from OEN or WEN high to address transition and SCSN high.

Bit[15:12]: SRAM#1 start address. It defines the start address of SRAM#1 in P-BUS and the real address is "(SSADR1+1)*32K+0x800000".

Bit[11:8]: SRAM#1 start end address. It defines the end address of SRAM#1 in P-BUS and the real address is "SEADR1*32K+0x800000 -1".

Bit[7:4]: SRAM#1 start address. It defines the start address of SRAM#0 in P-BUS and the real address is "SSADR0*32K+0x800000".

Bit[3:0]: SRAM#1 start end address. It defines the end address of SRAM#0 in P-BUS and the real address is "(SEADR0+1)*32K+0x800000 -1".

PCI Control & Status register (index_CID0: 8h | BA#3 + C0008h)

7:6 (r)	5 (r)	4 (r)	3:2 (r)	1:0 (r)
Chip Type	Disable flash memory BIOS	Initial state for IO /memory /PCI master /BIOS	BIOS size (BIOS_SIZE)	SDRAM window size (DIMM_SIZE)

15(r)	14(r/w)	13(r/w)	12(r/w)	11(r)	10(r)	9(r/w)	8(r/w)
Reserved	PLL MX(00b)		Slave Software Reset (1)	Disable PLL power down	PLL Test mode	BIOS Load Waiting (0)	BIOS Shadow Enable (0)

31:30 (r/w)	29:25 (r/w)	24:23(r/w)	22:16 (r/w)
PLL's OD parameter (10b)	PLL's R parameter (0Dh)	Reserved	PLL's F parameter (58h)

Bit[1:0]: SDRAM window size.

00: 32K

01: 64K

10: 128K

11: 2G

These two bits can be extracted automatically from Flash memory after RESET#.

Bit[3:2]: BIOS size.

00: 32K

01: 64K

10: 128k

11: 256k

These two bits can be extracted automatically from Flash memory after RESET#.

Bit-4: the initial state of PCI device's IO/Memory/bus master (PCI command register bit0,1,2) / BIOS (expansion ROM base address register bit0).

1:enable

0:disable

These two bits can be extracted automatically from Flash memory while RESET# goes from low to height.

Bit-5: disable flash memory.

1: disable flash memory. This bit will override the definition of bit4.

2: flash memory can be accessed.

Bit[7:6]: Chip Type. It is a same description as the hardware strap description.

11: Host acts with the microprocessor mode and C2C acts with the C2C slave mode.

10: Host acts with the PCI bridge mode and C2C acts with the C2C master mode.

01: Host acts with the PCI device mode and C2C acts with the C2C slave mode.

00: Host acts with the PCI device mode and C2C acts with the C2C master mode.

Bit[8]: BIOS Shadow Enable. When the bit is set, the SDRAM memory defined in "PCI BIOS Window" is used as the shadow memory of PCI BIOS.

Bit[9]: BIOS Load Waiting. When the bit is set and system accesses PCI BIOS ROM, the raid controller will hold BIOS read until the bit is reset.

Bit[10]: PLL Test Mode.

Bit[11]: Disable PLL's power down mode. '1': the PLL as always active. '0': the PLL's power down is determined by PMCSR bit1-0. Any value expect 00b will makes PLL power down.

Bit[12]: Slave Software Reset. This bit controls the SLVRSTN directly. Writing '0' to this bit will reset all slave devices.

Bit[14:13]: PLL MX parameter. Output selector.

Bit[15]: Reserved.

Bit[24:16]: PLL's F parameter. Feedback 9bit divider.

Bit[29:25]: PLL's R parameter. Input 5 bit divider.

Bit[31:30]: PLL's OD parameter. Output divider control.

PCI DIMM Window Control Register (index_CID0: 0Ch | BA#3 + C000Ch)

15: 0(r/w)
PCI Data Window SDRAM Page(PDPAGE) (0200h)

31:16(r/w)
PCI BIOS Window SDRAM Page(PBPAGE) (0100h)

Bit[15:0]: PCI Data Window for SDRAM. It controls the base address of the SDRAM window showed in PCI based address #4. The system controller can access all SDRAM memory space through the

window. SDRAM is organized into 2^16 pages, each of which can be 32K byte long. The real address in P-bus is "PCI address – BA#3 + SDPAGE*32K". When DIMM_SIZE is 64K, bit0 is reserved. When DIMM_SIZE is 128K, bit1 and bit0 are reserved. When DIMM_SIZE is 2G, all bits are reserved.

Bit[31:16]: PCI BIOS Window for SDRAM. When "PCI BIOS Shadow Enable" is set, it controls the base address of the SDRAM window showed in PCI Expansion ROM Register. SDRAM is organized into 2^16 pages, each of which can be 32K byte long. The real address in P-bus is "PCI address – BA#ROM + SDPAGE*32K". When BIOS_SIZE is 64K, bit0 is reserved. When BIOS_SIZE is 128K, bit0 and bit1 are reserved. When BIOS_SIZE is 256K, bit0, bit1 and bit2 are reserved.

Time Control Register (index_CID0: 3Ch | BA#3 +C003Ch)

7 (r/w)	6 (r)	5 (r/w)	4 (r/w)	3 (r/w)	2 (r/w)	1 (r/w)	0 (r/w)
Timer Enable	Reserved	Timer Interrupt Mask	Timer Interrupt Sequence ID				

31:11(r)	10(r/w)	9 (r/w)	8 (r/w)
Reserved.	Buzzer Output Enable	Timer Mode	

Bit[31:11]: Reserved.

Bit[10]: Buzzer Output Enable. When the bit is set, it will enable the Buzzer Output.

Bit[9:8]: Timer Mode.

00: Periodically Real-Time Timer Interrupt.

01: Once Timer Interrupt for time-out.

1x: Timer Test Mode Enable

Bit[7]: Timer Enable. When the bit is set, it will enable the internal timer.

Bit[6]: Reserved.

Bit[5]: Timer INT Mask. When the bit is set, it will mask an interrupt generated by this timer.

Bit[4:0]: Timer INT Sequence ID. It indicates the sequence ID of the interrupt generated by this engine.

Time Period Register (index_CID0: 40h | BA#3 + C0040h)

31: 0 (r/w)
Time Period(0000FFFFh)

Bit[31:0]: Time Period Register. It indicates the period of timer interrupt.

Time Counter Register (index_CID0: 44h | BA#3 + C0044h)

31: 0 (r)
Time Counter(TCOUNT)

Bit[31:0]: Time Counter Register. TCOUNT is the count register. When the timer is enabled, it is decreased as often as once every internal clock cycle. When the counter reaches zero, an interrupt is generated. TCOUNT is then reloaded from the TPERIOD register and the count begins again.

Serial Interface/Keypad Control Register (index_CID0: 48h | BA#3 + C0048h)

7(r/w)	6(r/w)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
Serial Interface Start(0)	Serial Interface R/W(0)	Serial Interface/ Keypad INT Mask(0)	Serial Interface/Keypad INT Sequence ID(0)				

15(r)	14(r)	13(r/w)	12(r/w)	11(r/w)	10(r/w)	9(r/w)	8(r/w)
Reserved		Serial Interface/ Keypad Test Mode(0)	Serial Interface/Keypad Period(1fh)				

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
Reserved	Reserved	Reserved	Serial Interface No Acknowledge	Reserved	Reserved	Reserved	Serial Interface Complete

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
Reserved				Keypad Data			

Bit[31:28]: Reserved.

Bit[27:24]: Keypad Data. It determines which key is pushed.

Bit[23:21]: Reserved.

Bit[20]: Serial Interface No Acknowledge. When this slave-receiver doesn't acknowledge the slave address, it responds an error. This Bit is cleared when Bit[23:16] is read.

Bit[19:17]: Reserved.

Bit[16]: Serial Interface Complete. It indicates this serial interface protocol completes normally. This Bit is cleared when Bit[23:16] is read.

Bit[15:14]: Reserved.

Bit[13]: Serial Interface/Keypad Test Mode.

Bit[12:8]: Serial Interface/Keypad Period.

Bit[7]: Serial Interface Start. Setting '1' to this bit will start the serial interface protocol.

Bit[6]: Serial Interface R/W. This bit determinates the direction of the message. A 'zero' means that the master will writes information to a select slave. A 'one' means that the master will read information from the slave.

Bit[5]: Serial Interface/Keypad INT Mask. When the bit is set, it will mask an interrupt generated by this serial interface engine.

Bit[4:0]: Serial Interface/Keypad INT Sequence ID. It indicates the sequence ID of the interrupt generated by this engine

Note: When PDC20621 is in the C2C master mode, the Serial Interface engine works. When PDC20621 is in the C2C slave mode, the Keypad engine works.

Serial Interface Address/Data Register (index_CID0: 4Ch | BA#3 + C004Ch)

7(r)	6(r)	5(r)	4(r)	3(r)	2(r)	1(r)	0(r)
Reserved							

15:8(r/w)
Serial Interface Data

23:16(r/w)
Serial Interface Sub Address

31(r)	30:24 (r/w)
Reserved	Serial Interface Device Address

Bit[31]: Reserved.

Bit[30:24]: Serial Interface Device Address. These seven bits determinate which device will be selected by the master.

Bit[23:16]: Serial Interface Sub Address. These bits indicate which register of the serial interface slave device will be selected.

Bit[15:8]: Serial Interface Data. When serial interface runs in a read protocol, these bits determinate the data obtained from the slave device. When serial interface runs in a write protocol, the bits determinate the data that will be sent to the slave device.

Bit[7:0]: Reserved.

PLL Counter Register (index_CID0: 54h | BA#3 + C0054h)

31:18 (r)	17:0 (r)
Reserved.	PLL Counter

Bit[15:0]: PLL Counter. For PDC20621 Test only.

Bit[31:18]: Reserved.

4.6.2 SDRAM Timing & Control Register

DIMM #0 DIMM Module Control Register (index_CID0: 80h | BA#3 + C0080h)

7 (r/w)	6 (r/w)	5:4 (r/w)	3 (r/w)	2:0 (r/w)
Module bank size(0)	Component bank size(0)	Row address size(0)	Buffer DIMM(0)	Column address size(0)

31:24 (r/w)	23:16 (r/w)	15:14 (r/w)	13:12 (r/w)	11:10 (r/w)	9:8 (r/w)
DIMM start address (00)	DIMM end address (3F)	TCLAT(2)	TCMIN(2)	TRCD(2)	TRP(2)

Bit[31:24]: DIMM module start address. It defines the start address of DIMM module in P-BUS and the real

address is “DSADR*16M”. If the DIMM start address is greater than 2G, it will disable the DIMM module decoder.

Bit[23:16]: DIMM module end address. It defines the end address of DIMM module in P-BUS and the real address is “(DEADR+1)*16M-1”. If the DIMM end address is greater than 2G, it will disable the DIMM module address decoder.

Bit[15:14]: CAS latency. The first output appears in CAS latency number of clock cycle after the issue of burst read command.

Bit[13:12]: Minimum data burst cycle. It defines the minimum data cycle when the memory controller executes the burst write or read command. The value defined in tCMIN is “tRAS-tRCD-tRP”.

Bit[11:10]: RASN to CASN delay. The read or write operation can occur after a time delay of tRCD from the time of bank activation. The minimum number of clock cycles required between bank active and read or write command should be calculated by dividing tRCD with cycle time of the clock and rounding up to the next higher integer.

Bit[9:8]: Pre-charge time . It is defined as the minimum number of clock cycles required to complete row pre-charge is calculated by dividing tRP with clock cycle time and rounding up to the next higher integer.

Bit[7]: Module Bank Size.

0: 1 Bank

1: 2 Bank

Bit[6]: Component Bank Size.

0: 2 Bank

1: 4 Bank

Bit[5:4]: Row Address Size.

00: 11bit

01: 12bit

10: 13bit

11: 14bit

Bit[3]: Buffer DIMM. DIMM #0 is accessed as the Buffer DIMM Protocol.

Bit[2:0]: Column Address Size.

000: 8bit

001: 9bit

010: 10bit

011: 11bit

1x0: 12bit

1x1: 13bit

DIMM #1 DIMM Module Control Register (index_CID0: 84h | BA#3 + C0084h)

7 (r/w)	6 (r/w)	5:4 (r/w)	3 (r/w)	2:0 (r/w)
Module bank size	Component bank size	Row address size	Buffer DIMM	Column address size

31:24 (r/w)	23:16 (r/w)	15:14 (r/w)	13:12 (r/w)	11:10 (r/w)	9:8 (r/w)
DIMM start address (00)	DIMM end address (3F)	TCLAT(2)	TCMIN(2)	TRCD(2)	TRP(2)

See DIMM #0 DIMM Module Space Control Register

DIMM Module Global Control Register (index_CID0: 88h | BA#3 +C0088h)

15:14 (r/w)	13:12(r/w)	11:8 (r/w)	7:4 (r/w)	3:0 (r/w)
DIMM Control Output Driving Selection (00)	DIMM Data Output Driving Selection (00)	TRFC(9)	Refresh Number (RN)(f)	Refresh Period (RP)(1)

23 :22(r)	21 (r/w)	20 (r/w)	19 (r/w)	18 (r/w)	17 (r/w)	16 (r/w)
Reserved.	DIMM Power Down Disable(1)	DIMM Arbitration Disable(0)	DIMM Initialization Enable(0)	DIMM Initialization Select(0)	Refresh Enable (0)	ECC Enable (0)

31 (r)	30 (r)	29 (r)	28 (r)	27 (r)	26 (r)	25 (r)	24 (r/w)
Reserved (0)						CKE Status	CKE Release

Bit[3:0]: DIMM Refresh Period. The refresh request can be performed one in tclk***RP****1024 ns.

Bit[7:4]: DIMM Refresh Number. The controller refreshes SDRAM RN times in a refresh request.

Bit[11:8]: DIMM Refresh Cycle Time. The time required to complete the auto refresh operation is specified by tRFC.

Bit[13:12]: DIMM Data output driving capability selection.

00: 6 mA,

01: 8 mA.

10: 10 mA

11: 12 mA

Bit[15:14]: DIMM Control output driving capability selection.

00: 6 mA,

01: 8 mA.

10: 10 mA

11: 12 mA

Bit[16]: DIMM ECC enable. When this bit is set, the memory controller will enable ECC function. During PDC20621 DIMM write period, the memory controller generates check bits for ECC. During PDC20621 DIMM read period, the memory controller reads check bits for ECC, checks and corrects error.

Bit[17]: DIMM refresh enable. When this bit is set, the memory controller will enable DIMM modules auto refresh function.

Bit[18]: DIMM initialization Select.

Bit[19]: DIMM initialization enable.

Bit[20]: DIMM Arbitration Disable. When the bit is set and the controller is the bus master, the controller will never release DBSYN and be always the bus master.

Bit[21]: DIMM power down disable. When this bit is set, the memory controller will never power down all DIMM modules.

Bit[23:22]: Reserved.

Bit[24]: DCKE Release. This bit indicates that this PDC20621 master device asks the glue logic on board to release the DCKE signal. When the DCKE signal is released, it is reset to zero.

Bit[25]: DCKE Status. The bit indicates the status of the DCKE signal. When this bit is zero, these DIMM modules are in the power-down mode. We can set bit[24] one to leave the power-down mode and these DIMM modules will not be initiated.

Bit[26:31]: Reserved.

4.6.3 Host DMA Module Control Register

HOST DMA Command Packet Pointer Register (index_HDMA:00h | BA#3 + C0100h)

31:4 (r/w)	3:0 (r)
Base address of Command Packet	Reserved(000)

Bit[31:3]: The DMA Command Packet Pointer must be QWORD aligned.

Bit[2:0]: Reserved.

HOST DMA Global Control & Status Register (index_ HDMA: 04h | BA#3 + C0104h)

7 (r)	6 (r)	5 (r)	4 (r)	3 (r)	2 (r)	1 (r)	0 (r/w)
Reserved							NCA Pause

15(r)	14(r)	13(r)	12(r)	11(r)	10:8(r)
Reserved					Memory Access Cycle

23 (r)	22 (r)	21 (r)	20 (r)	19 (r)	18 (r)	17 (r)	16 (r)
Soft ECC Error	Hard ECC Error	PCI Parity Error	PCI System Error	Reserved	Reserved	Direct Command Complete	Packet Command Complete

31 (r)	30 (r)	29 (r)	28 (r)	27 (r)	26 (r)	25 (r)	24 (r)
Reserved	Reserved	Packet Command Cycle	Delay Transaction	Reserved			

Bit-0: NCA Pause. When this bit is set, the DMA engine will not execute the next command packet.

Bit[7:1]: Reserved.

Bit[10:8]: Memory Access Cycle.

001: Packet Command Access Cycle.

01x: PRD Table Access Cycle.

1xx: SG Data Access Cycle.

Bit[15:11]: Reserved.

Bit-16: Packet Command Complete.

Bit-17: Direct Command Complete.

Bit-18: Reserved.

Bit-19: Reserved.

Bit-20: PCI System Error.

Bit-21: PCI Parity Error.

Bit-22: Local Hard ECC error (un-correctable error).

Bit-23: Local soft ECC error (correctable error)

Bit[27:24]: Reserved

Bit-28: Delay Transaction Status. This command packet is executed on delay transaction.

Bit-29: Packet Command Cycle.

Bit-30: Reserved.

Host DMA Descriptor Table Pointer Register0 (index_ HDMA: 08h | BA#3 + C0108h)

31:3 (r/w)	2:0 (r)
Base address of Descriptor table. Corresponds to A[31:3]	000b

Bit[31:2]: It indicates the PSG of PCI host memory. The Descriptor Table must be QWORD aligned.

Bit[1:0]: Reserved.

Host DMA Descriptor Table Pointer Register1 (index_ HDMA: 0Ch | BA#3 + C010Ch)

31:3 (r/w)	2:0 (r)
Base address of Descriptor table. Corresponds to A[31:3]	000b

Bit[31:2]: It indicates the PSG of local DIMM memory. The Descriptor Table must be QWORD aligned.

Bit[1:0]: Reserved.

HOST DMA #0 S/G Engine Address counter Register (index_HDMA:18h | BA#3 + C0118h)

31:0 (r)
Value of S/G engine address counter

Bit[31-0]: The value of channel #0's S/G engine address counter. When test mode is set (System Control register bit-10), the counter is cut to four 8bit counters and its value can be read from this register.

HOST DMA #0 S/G Engine byte count counter Register (index_HDMA:1Ch | BA#3 + C011Ch)

31:24 (r)	23:0 (r)
Reserved	Value of S/G engine byte count counter

Bit[31:24]: Reserved

Bit[23:0]: The value of channel #1's S/G engine byte count counter 0. When test mode is set, the counter's clock is switched to PCI clock, the counter is broken to two 8bit counter and its value can be read from this register.

HOST DMA #1 S/G Engine Address counter Register (index_HDMA:20h | BA#3 + C0120h)

31:0 (r)
Value of S/G engine address counter

Bit[31-0]: The value of channel #0's S/G engine address counter. When test mode is set, the counter is cut to four 8bit counters and its value can be read from this register.

HOST DMA #1 S/G Engine byte count counter Register (index_HDMA:24h | BA#3 + C0124h)

31:24 (r)	23:0 (r)
Reserved	Value of S/G engine byte count counter

Bit[31:24]: Reserved

Bit[23:0]: The value of channel #1's S/G engine byte count counter 0. When test mode is set, the counter is broken to three 8bit counter and its value can be read from this register.

HOST DMA Next Command Packet Pointer Register (index_HDMA:28h | BA#3 + C0128h)

31:4 (r/w)	3:0 (r/w)
Base address of Next Command Packet	Reserved(000)

Bit[31:3]: The Host DMA Next Command Packet Pointer must be QWORD aligned.

Bit[2:0]: Reserved.

HOST DMA Control & Status Register (index_ HDMA: 2Ch | BA#3 + C012Ch)

7 (r/w)	6 (r/w)	5 (r)	4 (r/w)	3 (r/w)	2 (r/w)	1 (r/w)	0 (r/w)
HOST DMA Start/Stop	HOST DMA R/W Direction	Reserved	Interrupt Sequence ID				

15(r)	14(r)	13(r)	12(r)	11(r/w)	10(r/w)	9(r/w)	8(r)
Reserved				DMA Software Reset	Mask INT (0)	Test Mode (0)	Reserved

23 (r)	22 (r)	21 (r)	20 (r)	19 (r)	18 (r)	17 (r)	16 (r)
Resvered							

31 (r)	30 (r)	29 (r)	28 (r)	27 (r)	26 (r)	25:24 (r)
Data FIFO Empty	Control FIFO Empty	Reserved				

Bit[4:0]: Interrupt Sequence ID.

Bit-5: Reserved.

Bit-6: HOST DMA Read or Write Control. '0' for bus master read. '1' for bus master write.

Bit-7: HOST DMA Start/Stop. Setting '1' to this bit will enable bus master operation of the controller. Writing '0' to this bit can halt master operation. All state machine information is lost when a '0' is written. Master mode operation can not be stopped and then resumed. If this bit is reset while bus master operation is still active and the DMA module has not yet finished its data transfer, the bus master command is said to be aborted and data transferred from the SDRAM may discarded before

being written to system memory. This bit is intended to be reset after the data transfer is completed.

Bit-8: Reserved.

Bit-9: Host DMA Controller Test Mode.

Bit-10: Mask INT. When this bit is set, the interrupt from Host DMA controller will not pass to PCI.

Bit-11: This bit controls the Host DMA module software reset. Write '1' to this will reset Host DMA module.

Bit[29:12]: Reserved

Bit-30: Control FIFO empty. The Control FIFO is empty

Bit-31: Data FIFO empty. The data FIFO is empty

4.6.4 XOR Module Control Register

XOR Command Packet Pointer Register (index_ XOR: 00h | BA#3 + C0180h)

31:5 (r/w)	4:0 (r)
Base address of Command Packet	Reserved(000)

Bit[31:3]: The XOR Command Packet Pointer must be QWORD aligned.

Bit[2:0]: Reserved.

XOR Global Control & Status Register (index_ XOR: 04h | BA#3 + C0184h)

7(r)	6(r)	5(r)	4(r)	3(r)	2(r)	1(r)	0(r/w)
Reserved							NCA Pause

15(r)	14(r)	13(r)	12(r)	11(r)	10:8(r)
Reserved	PSGx Active			Reserved	Memory Access Cycle

23 (r)	22 (r)	21 (r)	20 (r)	19 (r)	18 (r)	17 (r)	16 (r)
Soft ECC Error	Hard ECC Error	Compare Error	Reserved (0)	Reserved (0)	Reserved (0)	Direct Command Complete	Packet Command Complete

31 (r)	30 (r)	29 (r)	28 (r)	27 (r)	26:24 (r)
Reserved	Reserved	Packet Command Cycle	Delay Transaction	Reserved (0)	

Bit-0: NCA Pause. When this bit is set, the XOR engine will not execute the next command packet.

Bit[7:1]: Reserved.

Bit[10:8]: Memory Access Cycle.

001: Packet Command Access Cycle.

01x: PRD Table Access Cycle.

1xx: SG Data Access Cycle.

Bit-11: Reserved.

Bit[14:12]: PSGx Active.

000: PSG0 Active.

001: PSG1 Active.

010: PSG2 Active.

011: PSG3 Active.

100: PSG4 Active.

101: PSG5 Active.

11x: Reserved.

Bit-15: Reserved.

Bit-16: Packet Command Interrupt.

Bit-17: Direct Command Interrupt.

Bit[20:18]: Reserved.

Bit-21: Compare Error.

Bit-22: Local Hard ECC error (un-correctable error).

Bit-23: Local soft ECC error (correctable error)

Bit[27:24]: Reserved

Bit-28: Delay Transaction Status. This command packet is executed on delay transaction.

Bit-29: Packet Command Cycle.

Bit-30: Reserved.

XOR Descriptor Table Pointer Register0 (index_XOR: 08h | BA#3 + C0188h)

31:5 (r/w)	4:0 (r)
Base address of Descriptor table. Corresponds to A[31:3]	000b

Bit[31:0]: It indicates the PSG table of XOR Entry0. The Descriptor Table must be QWORD aligned.

XOR Descriptor Table Pointer Register1 (index_XOR: 0Ch | BA#3 + C018Ch)

31:3 (r/w)	2:0 (r)
Base address of Descriptor table. Corresponds to A[31:3]	000b

Bit[31:0]: It indicates the PSG table of XOR Entry1. The Descriptor Table must be QWORD aligned.

XOR Descriptor Table Pointer Register2 (index_ XOR: 10h | BA#3 + C0190h)

31:3 (r/w)	2:0 (r)
Base address of Descriptor table. Corresponds to A[31:3]	000b

Bit[31:0]: It indicates the PSG table of XOR Entry2. The Descriptor Table must be QWORD aligned.

XOR Descriptor Table Pointer Register3 (index_ XOR: 14h | BA#3 + C0194h)

31:3 (r/w)	2:0 (r)
Base address of Descriptor table. Corresponds to A[31:3]	000b

Bit[31:0]: It indicates the PSG table of XOR Entry3. The Descriptor Table must be QWORD aligned.

XOR Descriptor Table Pointer Register4 (index_ XOR: 18h | BA#3 + C0198h)

31:3 (r/w)	2:0 (r)
Base address of Descriptor table. Corresponds to A[31:3]	000b

Bit[31:0]: It indicates the PSG table of XOR Entry4. The Descriptor Table must be QWORD aligned.

XOR Descriptor Table Pointer Register5 (index_ XOR: 1Ch | BA#3 + C019Ch)

31:3 (r/w)	2:0 (r)
Base address of Descriptor table. Corresponds to A[31:3]	000b

Bit[31:0]: It indicates the PSG table of XOR Entry5. The Descriptor Table must be QWORD aligned.

XOR #0 S/G Engine Address counter Register (index_XOR: 20h | BA#3 + C01A0h)

31:0 (r)
Value of S/G engine address counter

Bit[31-0]: The value of channel #0's S/G engine address counter. When test mode is set, the counter is cut to four 8bit counters and its value can be read from this register.

XOR #0 S/G Engine byte count counter Register (index_XOR:24h | BA#3 + C01A4h)

31:24 (r)	23:0 (r)
Reserved	Value of S/G engine byte count counter

Bit[31:24]: Reserved.

Bit[23:0]: The value of channel #1's S/G engine byte count counter 0. When test mode is set, the counter is broken to three 8bit counter and its value can be read from this register.

XOR #1 S/G Engine Address counter Register (index_XOR: 28h | BA#3 + C01A8h)

31:0 (r)
Value of S/G engine address counter

Bit[31-0]: The value of channel #0's S/G engine address counter. When test mode is set, the counter is cut to four 8bit counters and its value can be read from this register.

XOR #1 S/G Engine byte count counter Register (index_XOR:2Ch | BA#3 + C01ACh)

31:24 (r)	23:0 (r)
Reserved	Value of S/G engine byte count counter

Bit[31:24]: Reserved.

Bit[23:0]: The value of channel #1's S/G engine byte count counter 0. When test mode is set, the counter is broken to three 8bit counter and its value can be read from this register.

XOR #2 S/G Engine Address counter Register (index_XOR: 30h | BA#3 + C01B0h)

31:0 (r)
Value of S/G engine address counter

Bit 31-0: The value of channel #0's S/G engine address counter. When test mode is set, the counter is cut to four 8bit counters and its value can be read from this register.

XOR #2 S/G Engine byte count counter Register (index_XOR:34h | BA#3 + C01B4h)

31:24 (r)	23:0 (r)
Reserved	Value of S/G engine byte count counter

Bit[31:24]: Reserved.

Bit[23:0]: The value of channel #1's S/G engine byte count counter 0. When test mode is set, the counter is broken to three 8bit counter and its value can be read from this register.

XOR #3 S/G Engine Address counter Register (index_XOR: 38h | BA#3 + C01B8h)

31:0 (r)
Value of S/G engine address counter

Bit[31-0]: The value of channel #0's S/G engine address counter. When test mode is set, the counter is cut to four 8bit counters and its value can be read from this register.

XOR #3 S/G Engine byte count counter Register (index_XOR:3Ch | BA#3 + C01BCh)

31:24 (r)	23:0 (r)
Reserved	Value of S/G engine byte count counter

Bit[31:24]: Reserved.

Bit[23:0]: The value of channel #1's S/G engine byte count counter 0. When test mode is set, the counter is broken to three 8bit counter and its value can be read from this register.

XOR #4 S/G Engine Address counter Register (index_XOR: 40h | BA#3 + C01C0h)

31:0 (r)
Value of S/G engine address counter

Bit[31-0]: The value of channel #0's S/G engine address counter. When test mode is set, the counter is cut to four 8bit counters and its value can be read from this register.

XOR #4 S/G Engine byte count counter Register (index_XOR:44h | BA#3 + C01C4h)

31:24 (r)	23:0 (r)
Reserved	Value of S/G engine byte count counter

Bit[31:24]: Reserved.

Bit[23:0]: The value of channel #1's S/G engine byte count counter 0. When test mode is set, the counter is broken to three 8bit counter and its value can be read from this register.

XOR #5 S/G Engine Address counter Register (index_XOR: 48h | BA#3 + C01C8h)

31:0 (r)
Value of S/G engine address counter

Bit[31-0]: The value of channel #0's S/G engine address counter. When test mode is set, the counter is cut to four 8bit counters and its value can be read from this register.

XOR #5 S/G Engine byte count counter Register (index_XOR:4Ch | BA#3 + C01CCh)

31:24 (r)	23:0 (r)
Reserved	Value of S/G engine byte count counter

Bit[31:24]: Reserved.

Bit[23:0]: The value of channel #1's S/G engine byte count counter 0. When test mode is set, the counter is broken to three 8bit counter and its value can be read from this register.

XOR Next Command Packet Pointer Register (index_ XOR: 50h | BA#3 + C01D0h)

31:5 (r/w)	4:0 (r)
Base address of Next Command Packet	Reserved(000)

Bit[31:3]: The XOR Next Command Packet Pointer must be QWORD aligned.

Bit[2:0]: Reserved.

XOR Control & Status Register (index_ XOR: 54h | BA#3 + C01D4h)

7(r/w)	6(r/w)	5(r)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
XOR Start/Stop	XOR Type	Reserved	Interrupt Sequence ID				

15(r)	14(r)	13(r)	12(r)	11(r/w)	10(r/w)	9(r/w)	8(r)
Reserved				XOR Software Reset	Mask INT (0)	Test Mode (0)	Reserved

23 (r)	22 (r)	21 (r)	20 (r)	19 (r)	18 (r)	17 (r)	16 (r)
Reserved							

31 (r)	30 (r)	29 (r)	28 (r)	27 (r)	26:24 (r)
Data FIFO Empty	Control FIFO Empty	Reserved	Reserved (0)	Reserved (0)	Reserved

Bit[4:0]: Interrupt Sequence ID.

Bit[5]: Reserved.

Bit-6: XOR Type.

'1' = execute XOR command.

'0' = execute Compare Command.

Bit-7: XOR start/stop. Setting '1' to this bit will enable XOR operation of the controller. Writing '0' to this bit will halt XOR operation. All state machine information is lost when a '0' is written. XOR operation can not be stopped and then resumed. If this bit is reset while XOR operation is still active, the XOR command is said to be aborted. This bit is intended to be reset after the XOR command is completed.

Bit-8: Reserved.

Bit-9: XOR Controller Test Mode.

Bit-10: Mask INT. When this bit is set, the interrupt from XOR controller will not pass to PCI.

Bit-11: This bit controls the XOR module software reset. Write '1' to this will reset XOR module.

Bit[15:12]: Reserved.

Bit[29:16]: Reserved.

Bit-30: Control FIFO empty. The task FIFO of channel 0 is empty

Bit-31: Data FIFO empty. The data FIFO of channel 0 is empty

4.6.5 ATA Timing & Control Register

4.6.5.1 IDE Channel 0 Timing & Control Register

Channel #0 Data Register (index_IDE0: 00h | MMIO: BA#3 + C0200h)

31:16 (r)	15:0(r/w)
Reserved(0)	Data Register

The register contains the same information as the Data register defined in ATA specification.

Channel #0 Feature/Error Register (index_IDE0: 104h | MMIO: BA#3 + C00204h)

31:8 (r)	7:0 (r/w)
Reserved(0)	Feature or Error Register

The register contains the same information as the Feature-Status register defined in ATA specification.

Channel #0 Sector Count Register (index_IDE0: 08h | MMIO: BA#3 + C0208h)

31:8 (r)	7:0 (r/w)
Reserved(0)	Sector Count Register

The register contains the same information as the Sector-Count register defined in ATA specification.

Channel #0 Sector Number Register (index_IDE0: 0Ch | MMIO: BA#3 + C020Ch)

31:8 (r)	7:0 (r/w)
Reserved(0)	Sector Number Register

The register contains the same information as the Sector-Number register defined in ATA specification.

Channel #0 Cylinder Low Register (index_IDE0: 10h | MMIO: BA#3 + C0210h)

31:8 (r)	7:0 (r/w)
Reserve(0)	Cylinder Low Register

The register contains the same information as the Cylinder-Low register defined in ATA specification.

Channel #0 Cylinder High Register (index_IDE0: 14h | MMIO: BA#3 + C00114h)

31:8 (r)	7:0 (r/w)
Reserved(0)	Cylinder High Register

The register contains the same information as the Cylinder-High register defined in ATA specification.

Channel #0 Device / Head Register (index_IDE0: 18h | MMIO: BA#3 + C0218h)

31:24 (r)	7:0 (r/w)
Reserved(0)	Device/Head Register

The register contains the same information as the Device-Head register defined in ATA specification.

Channel #0 Command/Status Register (index_IDE0: 1Ch | MMIO: BA#3 + C021Ch)

31:8 (r)	7::0 (r/w)
Reserved (0)	Command or Status Register

The register contains the same information as the Command-Status register defined in ATA specification.

Channel #0 Alternate Status / Device Control Register (index_IDE0: 38h | BA#3 + C0238h)

31:8 (r)	7:0 (r/w)
Reserved (0)	Alternate Status or Device Control Register

The register contains the same information as the Alternate-Status or Device-Control register defined in ATA specification.

Channel #0 IDE Command Packet Pointer Register (index_IDE0:40h | BA#3 + C0240h)

31:6 (r/w)	2:0 (r/w)
Base address of Command Packet	Reserved(000)

Bit[31:3]: The ATA Command Packet Pointer must be QWORD aligned.

Bit[2:0]: Reserved.

Channel #0 Descriptor Table Pointer Register (index_IDE0:44h | BA#3 + C0244h)

31:3 (r/w)	2:0 (r)
Base address of Descriptor table. Corresponds to A[31:5]	Reserved(000)

Bit[31:0]: It indicates the PSG of ATA DMA Command. The Descriptor Table must be QWORD aligned.

Channel #0 Global Control & Status Register (CGCR0) (index_IDE0: 48h | MMIO: BA#3 + C0248h)

7 (r)	6 (r)	5 (r)	4 (r)	3 (r)	2 (r)	1 (r)	0 (r/w)
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	NCA Pause

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
Reserved	Reserved	Reserved	Reserved	Reserved	Memory Access Cycle		

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
Soft ECC Error	Hard ECC Error	Drive Error	Under Run Error	Over Run Error	Reserved	Direct Command Complete	Packet Command Complete

31 (r)	30 (r)	29 (r)	28 (r)	27 (r)	26 (r)	25 (r)	24 (r)
Reserved	Reserved	Packet Command Cycle	Delay Transaction	Reserved			

Bit-0: NCA Pause. When this bit is set, the ATA engine will not execute the next command packet.

Bit[7:1]: Reserved.

Bit[10:8]: Memory Access Cycle.

001: Packet Command Access Cycle.

01x: PRD Table Access Cycle.

1xx: SG Data Access Cycle.

Bit[15:11]: Reserved.

Bit-16: the interrupt descriptor0. Bit “1”: the interrupt assert for packet command completion

Bit-17: the interrupt descriptor1. Bit “1”: the interrupt assert for direct command from host

Bit-18: Reserved.

Bit-19: Overrun Error.

Bit-20: Underrun Error.

Bit-21: Drive Error.

Bit-22: Local Hard ECC error (un-correctable error).

Bit-23: Local soft ECC error (correctable error)

Bit[27:24]: Reserved.

Bit[28]: Delay Transaction Status. This command packet is executed on delay transaction.

Bit-29: Packet Command Cycle.

Bit[31:30]: Reserved.

DRV #0 Configuration and Timing Control Register 0(index_IDE0: 4Ch | MMIO: BA#3 + C0024Ch)

31 (r/w)	30:29 (r/w)	28:24 (r/w)	23:21 (r/w)	20:16 (r/w)	15:14 (r/w)	13:8 (r/w)	7:5 (r/w)	4:0 (r/w)
Reserve	TDN	tDCYCH	TDENV	TDCYCL	Reserve	TPRCYC	TPRCV	TPENV

Bit[4:0]: tPENV. PIO envelope. It is the number of clock to initialize PIO transformation

Bit[7:5]: tPRCV. PIO recovery time. It is the number of clock between two PIO transformations.

Bit[13:8]: tPRCYC. Cycle time of DIOR_/DIOW_. It is the pulse width of DIOR_/DIOW_ in PIO register (8bit) transformation.

Bit[20:16]: tDCYCL: cycle time of low pulse of DIOR_/DIOW_ in DMA mode. It is the pulse width when DIOR_/DIOW_ is low in DMA transformation.

Bit[23:21]: tDENV. Cycle time of DMA envelope. It is the number of clock from DACK_ to DIOR_/DIOW_.

Bit[28:24]: tDCYCH: cycle number of high pulse of DIOR_/DIOW_ in DMA mode. It is the pulse width when DIOR_/DIOW_ is high in DMA transformation.

Bit[30:29]: tDN. CS0_, CS1_ hold time in DMA mode. It is the number of clock from DIOR_/DIOW_ to CS0_, CS1_.

DRV #0 Configuration and Timing Control Register 1(index_IDE0: 50h | MMIO: BA#3 + C0250h)

15:14 (r)	13 (r/w)	12:8 (r/w)	7:4 (r/w)	3:2 (r/w)	1:0 (r/w)
Reserve	tHOLD (1)	tCYC	tMLI	tENV	TACK

31:26 (r/w)	25 (r/w)	24 (r/w)	23:21 (r/w)	20:16 (r/w)
TPDCYC	Reserved	PIO mode IORDY enable	tSS	TRP

Bit[1:0] : tACK. Setup and hold time from DACK_ in UDMA mode.

Bit[3:2]: tENV. Envelope time.

Bit[7:4]: tMLI. Inter-lock time with minimum.

Bit[12:8]: tCYC. Cycle time of UDMA.

Bit-13: tHOLD. '1' for add half clock for DATA hold time.

Bit[20:16]: ready-to-pause time.

Bit[23:21]: tSS. Timing from last STROBE edge to STOP

Bit-24: PIO mode IORDY enable.
'1': the PIO mode transformation will be finished after IORDY being high.
'0': the PIO mode transformation will be finished regardless status of IORDY.

Bit-25: Reserved.

Bit[31:26]: tPDCYC. Cycle time of DIOR_/DIOW_. It is the pulse width of DIOR_/DIOW_ in PIO data (16bit) transformation.

Bit-31: Reserved

Channel #0 S/G Engine Address counter Register (index_IDE0: 54h | MMIO: BA#3 + C0254h)

31:0 (r)
Value of S/G engine address counter

Bit[31:0]: The value of channel #0's S/G engine address counter. When test mode is set, the counter is cut to four 8bit counter and its value can be read from this register.

Channel #0 S/G Engine byte count counter Register (index_IDE0: 58h | MMIO: BA#3 + C0258h)

31:24 (r)	23:0 (r)
Reserved	Value of S/G engine byte count counter 0

Bit[31:24]: Reserved.

Bit[23:0] : The value of channel #0's S/G engine byte count counter 0. When test mode is set, the counter is broken to three 8bit counter and its value can be read from this register.

Channel #0 ATA Next Command Packet Pointer Register (index_IDE0:5Ch | BA#3 + C025Ch)

31:6 (r/w)	2:0 (r/w)
Base address of Next Command Packet	Reserved(000)

Bit[31:3]: The ATA Next Command Packet Pointer must be QWORD aligned.

Bit[2:0]: Reserved.

Channel #0 IDE Control & Status Register (CICR0) (index_IDE2:60h | BA#3 + C0260h)

7 (r/w)	6 (r/w)	5 (r)	4 (r/w)	3 (r/w)	2 (r/w)	1 (r/w)	0 (r/w)
DMA Start/Stop	DMA R/W Direction	Reserved.	Interrupt Sequence ID				

15(r)	14(r/w)	13 (r/w)	12 (r/w)	11 (r/w)	10 (r/w)	9 (r/w)	8 (r/w)
Reserved	IDE output Driving Selection	IDE Bus Floating that Dependent on CBLID# (0)	ATA bus Tri-state	ATA Software Reset	Mask INT (0)	Test Mode (0)	CSN Disable (0)

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

31 (r)	30 (r)	29 (r)	28 (r)	27 (r)	26 (r)	25 (r)	24 (r)
Data FIFO Empty	Control FIFO Empty	Reserved	Drive DMARQ Status	Drive INT Status	Reserved	Cable Status	

Bit[4:0]: Interrupt Sequence ID. It indicates the sequence ID of the interrupt generated by this engine.

Bit[5]: Reserved.

Bit-6: Host set the Direction of DMA data. 1: chip to HD. 0: HD to chip

Bit-7: DMA start/stop. Setting '1' to this bit will enable DMA operation of the controller. Writing '0' to this bit will halt DMA operation. All state machine information is lost when a '0' is written. DMA operation can not be stopped and then resumed. If this bit is reset while DMA operation is still active, the DMA command is said to be aborted. This bit is intended to be reset after the DMA command is completed.

Bit-8: CSN Disable. When this bit is set and IDE is during PIO cycle, CS0N and CS1N will be released.

Bit-9: ATA Module Test mode.

Bit-10: Mask INT. When this bit is set, the interrupt from ATA module will not pass to PCI.

Bit-11: This bit controls the ATA module software reset. Write '1' to this will reset ATA module.

Bit-12: ATA bus tri-state. When this bit is set to '1', the ATA bus will be floating.

Bit-13: '1', Primary CBLID# can control the enable signal of IDE tri-state pad. See the following figure. If this bit is set and case of HD is removed from HDD holder. A pull high resistance make CBLID# high and IDE tri-state pad floating. If this bit is reset, There is no effect when case of HD is removed from holder.

Bit-14: Primary IDE output driving capability selection.
0: 8 mA, 1: 10 mA.

Bit[23:15]: Reserved.

Bit-24: Cable ID status that latched on the rising edge of RESET#

Bit-25: Directed connected to CBLID_.

Bit-27: Drive INT status. The status of ATA's INTRQ.

Bit-28: Drive DMARQ status. The status of DMARQ can be monitored directly from here.

Bit-29: Reserved.

Bit-30: Control FIFO empty. The Control FIFO of channel 0 is empty

Bit-31: Data FIFO empty. The data FIFO of channel 0 is empty

4.6.5.2 IDE Channel 1 Timing & Control Register

Channel #1 Data Register (index_IDE0: 00h | MMIO: BA#3 + C0280h)

31:16	15:0 (r/w)
Reserved(0)	Data Register

See **Channel #0 Data Register**

Channel #1 Feature / Error Register (index_IDE1: 04h | MMIO: BA#3 + C0284h)

31:8	7:0 (r/w)
Reserved(0)	Feature / Error Register

See **Channel #0 Feature / Error Register**

Channel #1 Sector Count Register (index_IDE1: 08h | MMIO: BA#3 + C0288h)

31:8	7:0 (r/w)
Reserved(0)	Sector Count Register

See **Channel #0 Sector Count Register**

Channel #1 Sector Number Register (index_IDE1: 0Ch | MMIO: BA#3 + C028Ch)

31:8	7:0 (r/w)
Reserved(0)	Sector Number Register

See **Channel #0 Sector Number Register**

Channel #1 Cylinder Low Register (index_IDE1: 10h | MMIO: BA#3 + C0290h)

31:8	7:0 (r/w)
Reserve(0)	Cylinder Low Register

See **Channel #0 Cylinder Low Register**

Channel #1 Cylinder High Register (index_IDE1: 14h | MMIO: BA#3 + C0294h)

31:8	7:0 (r/w)
Reserved(0)	Cylinder High Register

See **Channel #0 Cylinder High Register**

Channel #1 Device / Head Register (index_IDE1: 18h | MMIO: BA#3 + C0298h)

31:24	7:0 (r/w)
Reserved(0)	Device/Head Register

See **Channel #0 Device / Head Register**

Channel #1 Command / Status Register (index_IDE1: 1Ch | MMIO: BA#3 + C0298h)

31:8	7::0 (r/w)
Reserved (0)	Command or Status Register

See **Channel #0 Command / Status Register**

Channel #1 Alternate Status / Device Control Register (index_IDE1: 38h | MMIO: BA#3 + C02B8h)

31:8	7:0 (r/w)
Reserved (0)	Alternate Status or Device Control Register

See **Channel #0 Alternate Status Register / Device Control Register**

Channel #1 ATA Command Packet Pointer Register (index_IDE1:40h | BA#3 + C02C0h)

31:6 (r/w)	2:0 (r)

Base address of Command Packet	Reserved

See **Channel#0 ATA Command Packet Pointer Register**.

Channel #1 Descriptor Table Pointer Register (index_IDE1:44h | BA#3 + C02C4h)

31:3 (r/w)	2:0 (r)
Base address of Descriptor table. Corresponds to A[31:3]	Reserved(000)

See **Channel #0 Descriptor Table Pointer Register**

Channel #1 Global Control & Status Register (CGCR1) (index_IDE1:48h | BA#3 + C02C8h)

7 (r)	6 (r)	5 (r)	4 (r)	3 (r)	2 (r)	1 (r)	0 (r/w)
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	NCA Pause

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
Reserved	Reserved	Reserved	Reserved	Reserved	Memory Access Cycle		

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
Soft ECC Error	Hard ECC Error	Drive Error	Under Run Error	Over Run Error	Reserved	Direct Command Complete	Packet Command Complete

31 (r)	30 (r)	29 (r)	28 (r)	27 (r)	26 (r)	25 (r)	24 (r)
Reserved	Reserved	Packet Command Cycle	Delay Transaction	Reserved			

See **Channel #0 Global Control Register (CGCR**0**)**

DRV #1 Configuration and Timing Control Register 0 (index_IDE1:4Ch | BA#3 + C02CCh)

31 (r/w)	30:29 (r/w)	28:24 (r/w)	23:21 (r/w)	20:16 (r/w)	15:14 (r/w)	13:8 (r/w)	7:5 (r/w)	4:0 (r/w)
Reserve	TDN	TDCYCH	TDENV	TDCYCL	Reserve	TPRCYC	TPRCV	TPENV

See DRV #0 Configuration and Timing Control Register 0

DRV #1 Configuration and Timing Control Register 1 (index_IDE1:50h | BA#3 + C02D0h)

15:14 (r/w)	13 (r/w)	12:8 (r/w)	7:4 (r/w)	3:2 (r/w)	1:0 (r/w)
Reserve	tHOLD (1)	tCYC	tMLI	tENV	TACK

31:26 (r/w)	25 (r/w)	24 (r/w)	23:21 (r/w)	20:16 (r/w)
TPDCYC	Reserved	PIO mode IORDY enable	tSS	TRP

See DRV #0 Configuration and Timing Control Register 1

Channel #1 S/G Engine Address counter Register (index_IDE1:54h | BA#3 + C02D4h)

31:0 (r)
Value of S/G engine address counter

Bit[31-0]: The value of channel #1's S/G engine address counter. When test mode is set, the counter is cut to four 8bit counters and its value can be read from this register.

Channel #1 S/G Engine byte count counter Register (index_IDE1:58h | BA#3 + C02D8h)

31:24 (r)	23:0 (r)
Reserved	Value of S/G engine byte count counter

Bit[31:24]: Reserved.

Bit[23:0]: The value of channel #1's S/G engine byte count counter 0. When test mode is set, the counter is broken to three 8bit counter and its value can be read from this register.

Channel #1 ATA Next Command Packet Pointer Register (index_IDE1:5Ch | BA#3 + C02E0h)

31:6 (r/w)	5:0 (r)
Base address of Next Command Packet	Reserved(000)

See **Channel#0 ATA Next Command Packet Pointer Register**.

Channel #1 IDE Control & Status Register (CGCR1) (index_IDE1:60h | BA#3 + C03E0h)

7 (r/w	6 (r/w)	5 (r)	4 (r/w)	3 (r/w)	2 (r/w)	1 (r/w)	0 (r/w)
DMA Start/Stop	DMA R/W Direction	Reserved.	Interrupt Sequence ID				

15(r)	14(r /w)	13(r /w)	12 (r/w)	11(r /w)	10 (r /w)	9(r/w)	8(r/w)
Reserved	IDE output Driving Selection	IDE Bus Floating that Dependent on CBLID# (0)	ATA bus Tri-state	ATA Software Reset	Mask INT (0)	Test Mode (0)	CSN Disable (0)

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

31 (r)	30 (r)	29 (r)	28 (r)	27 (r)	26 (r)	25 (r)	24 (r)
Data FIFO Empty	Control FIFO Empty	Reserved	Drive DMARQ Status	Drive INT Status	Reserved	Cable Status	

See **Channel#1 IDE Control & Status Register**.

4.6.5.3 IDE Channel 2 Timing & Control Register

Channel #2 Data Register (index_IDE2:00h | BA#3 + C0300h)

31:16	15:0 (r/w)
Reserved(0)	Data Register

See **Channel #0 Data Register**

Channel #2 Feature / Error Register (index_IDE2:04h | BA#3 + C0304h)

31:8	7:0 (r/w)
Reserved(0)	Feature/Error Register

See **Channel #0 Feature / Error Register**

Channel #2 Sector Count Register (index_IDE2:08h | BA#3 + C0308h)

31:8	7:0 (r/w)
Reserved(0)	Sector Count Register

See **Channel #0 Sector Count Register**

Channel #2 Sector Number Register (index_IDE2:0Ch | BA#3 + C030Ch)

31:8	7:0 (r/w)
Reserved(0)	Sector Number Register

See **Channel #0 Sector Number Register**

Channel #2 Cylinder Low Register (index_IDE2: 10h | MMIO: BA#3 + C0310h)

31:8	7:0 (r/w)
Reserve(0)	Cylinder Low Register

See **Channel #0 Cylinder Low Register**

Channel #2 Cylinder High Register (index_IDE2:14h | BA#3 + C0314h)

31:8	7:0 (r/w)
Reserved(0)	Cylinder High Register

See **Channel #0 Cylinder High Register**

Channel #2 Device / Head Register (index_IDE2:18h | BA#3 + C0318h)

31:8	7:0 (r/w)
Reserved (0)	Device/Head Register

See **Channel #0 Device / Head Register**

Channel #2 Command / Status Register (index_IDE2:1Ch | BA#3 + C031Ch)

31:8	7::0 (r/w)
Reserved (0)	Command or Status Register

See **Channel #0 Command / Status Register**

Channel #2 Alternate Status / Device Control Register (index_IDE2:38h | BA#3 + C0338h)

31:8	7:0 (r/w)
Reserved (0)	Alternate Status or Device Control Register

See **Channel #0 Alternate Status / Device Control Register**

Channel #2 ATA Packet Command Pointer Register (index_IDE2:40h | BA#3 + C0340h)

31:6 (r/w)	2:0 (r)
Base address of Command Packet	Reserved

See **Channel#0 ATA Command Packet Pointer Register**.

Channel #2 Descriptor Table Pointer Register (index_IDE2:44h | index_CID0: 244h | BA#3 + C0344h)

31:3 (r/w)	2:0 (r)
Base address of Descriptor table. Corresponds to A[31:3]	Reserved

See **Channel #0 Descriptor Table Pointer Register**

Channel #2 Global Control & Status Register (CGCR2) (index_IDE2:48h | BA#3 + C0348h)

7 (r)	6 (r)	5 (r)	4 (r)	3 (r)	2 (r)	1 (r)	0 (r/w)
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	NCA Pause

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
Reserved	Reserved	Reserved	Reserved	Reserved	Memory Access Cycle		

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
Soft ECC Error	Hard ECC Error	Drive Error	Under Run Error	Over Run Error	Reserved	Direct Command Complete	Packet Command Complete

31 (r)	30 (r)	29 (r)	28 (r)	27 (r)	26 (r)	25 (r)	24 (r)
Reserved	Reserved	Packet Command Cycle	Delay Transaction	Reserved			

See **Channel #0 Global Control Register (CGCR0)**

DRV #2 Configuration and Timing Control Register 0 (index_IDE2:4Ch | BA#3 + C034Ch)

31 (r/w)	30:29 (r/w)	28:24 (r/w)	23:21 (r/w)	20:16 (r/w)	15:14 (r/w)	13:8 (r/w)	7:5 (r/w)	4:0 (r/w)
Reserve	TDN	tDCYCH	TDENV	TDCYCL	Reserve	TPRCYC	TPRCV	TPENV

See DRV #0 Configuration and Timing Control Register 0

DRV #2 Configuration and Timing Control Register 1 (index_IDE2:50h | BA#3 + C0350h)

15:14 (r/w)	13 (r/w)	12:8 (r/w)	7:4 (r/w)	3:2 (r/w)	1:0 (r/w)
Reserve	tHOLD (1)	tCYC	tMLI	tENV	TACK

31:26 (r/w)	25 (r/w)	24 (r/w)	23:21 (r/w)	20:16 (r/w)
TPDCYC	Reserved	PIO mode IORDY enable	TsS	TRP

See DRV #0 Configuration and Timing Control Register 1

Channel #2 S/G Engine Address counter Register (index_IDE2:54h | BA#3 + C0354h)

31:0 (r)
Value of S/G engine address counter

Bit[31-0]: The value of channel #2's S/G engine address counter. When test mode is set, the counter is cut to four 8bit counters and its value can be read from this register.

Channel #2 S/G Engine byte count counter Register (index_IDE2:58h | BA#3 + C0358h)

31:24 (r)	23:0 (r)
Reserved	Value of S/G engine byte count counter

Bit[31:24]: Reserved.

Bit[23:0]: The value of channel #2's S/G engine byte count counter 0. When test mode is set, the counter is broken to three 8bit counter and its value can be read from this register.

Channel #2 ATA Next Command Packet Pointer Register (index_IDE2:5Ch | BA#3 + C035Ch)

31:6 (r/w)	2:0 (r)
Base address of Next Command Packet	Reserved

See **Channel#0 ATA Next Command Packet Pointer Register**.

Channel #2 IDE Control & Status Register (CICR2) (index_IDE2:60h | BA#3 + C0360h)

7 (r/w)	6 (r/w)	5 (r)	4 (r/w)	3 (r/w)	2 (r/w)	1 (r/w)	0 (r/w)
DMA Start/Stop	DMA R/W Direction	Reserved.	Interrupt Sequence ID				

15(r)	14(r/w)	13 (r/w)	12 (r/w)	11(r/w)	10 (r/w)	9(r/w)	8(r/w)
Reserved	IDE output Driving Selection	IDE Bus Floating that Dependent on CBLID# (0)	ATA bus Tri-state	ATA Software Reset	Mask INT (0)	Test Mode (0)	CSN Disable (0)

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

31 (r)	30 (r)	29 (r)	28 (r)	27 (r)	26 (r)	25 (r)	24 (r)
Data FIFO Empty	Control FIFO Empty	Reserved	Drive DMARQ Status	Drive INT Status	Reserved	Cable Status	

See **Channel#0 IDE Control & Status Register**.

4.6.5.4 IDE Channel 3 Timing & Control Register

Channel #3 Data Register (index_IDE3:00h | BA#3 + C0380h)

31:16	15:0 (r/w)
Reserved	Data Register

See **Channel #0 Data Register**

Channel #3 Feature / Error Register (index_IDE3:04h | BA#3 + C0384h)

31:8	7:0 (r/w)
Reserved(0)	Feature or Error Register

See **Channel #0 Feature Register**

Channel #3 Sector Count Register (index_IDE3:08h | BA#3 + C0388h)

31:8	7:0 (r/w)
Reserved(0)	Sector Count Register

See **Channel #0 Sector Count Register**

Channel #3 Sector Number Register (index_IDE3:0Ch | BA#3 + C038Ch)

31:24	23::0 (r/w)
Sector Number Register	Reserved(0)

See **Channel #0 Sector Number Register**

Channel #3 Cylinder Low Register (index_IDE3:10h | BA#3 + C0390h)

31:8	7:0 (r/w)
Reserve(0)	Cylinder Low Register

See **Channel #0 Cylinder Low Register**

Channel #3 Cylinder High Register (index_IDE3:14h | BA#3 + C0394h)

31:8	7:0 (r/w)
Reserved(0)	Cylinder High Register

See **Channel #0 Cylinder High Register**

Channel #3 Device / Head Register (index_IDE3:18h | BA#3 + C0398h)

31:8	7:0 (r/w)
Reserved(0)	Device/Head Register

See **Channel #0 Device / Head Register**

Channel #3 Command / Status Register (index_IDE3:1Ch | index_CID0: 29Ch | BA#3 + C039Ch)

31:8	7::0 (r/w)
Reserved (0)	Command or Status Register

See **Channel #0 Command Register**

Channel #3 Alternate Status / Device Control Register (index_IDE3:38h | BA#3 +3001 C003B8h)

31:8	7:0 (r/w)
Reserved (0)	Alternate Status or Device Control Register

See **Channel #0 Alternate Status / Device Control Register**

Channel #3 ATA Command Packet Pointer Register (index_IDE3:40h | BA#3 + C03C0h)

31:6 (r/w)	2:0 (r)
Base address of Command Packet	Reserved

See **Channel#0 ATA Command Packet Pointer Register**.

Channel #3 Descriptor Table Pointer Register (index_IDE3:44h | BA#3 + C03C4h)

31:3 (r/w)	2:0 (r)
Base address of Descriptor table. Corresponds to A[31:3]	Reserved(000)

See **Channel #0 Descriptor Table Pointer Register**

Channel #3 Global Control & Status Register (CGCR3) (index_IDE3:48h | BA#3 + C03C8h)

7 (r)	6 (r)	5 (r)	4 (r)	3 (r)	2 (r)	1 (r)	0 (r/w)
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	NCA Pause

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
Reserved	Reserved	Reserved	Reserved	Reserved	Memory Access Cycle		

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
Soft ECC Error	Hard ECC Error	Drive Error	Under Run Error	Over Run Error	Reserved	Direct Command Complete	Packet Command Complete

31 (r)	30 (r)	29 (r)	28 (r)	27 (r)	26 (r)	25 (r)	24 (r)
Reserved	Reserved	Packet Command Cycle	Delay Transaction	Reserved			

See **Channel #0 Global Control Register (CGCR0)**

DRV #3 Configuration and Timing Control Register 0 (index_IDE3:4Ch | BA#3 + C03CCh)

31 (r/w)	30:29 (r/w)	28:24 (r/w)	23:21 (r/w)	20:16 (r/w)	15:14 (r/w)	13:8 (r/w)	7:5 (r/w)	4:0 (r/w)
Reserve	TDN	tDCYCH	TDENV	TDCYCL	Reserve	TPRCYC	TPRCV	TPENV

See DRV #0 Configuration and Timing Control Register 0

DRV #3 Configuration and Timing Control Register 1 (index_IDE3:50h | BA#3 + C03CCh)

15:14 (r/w)	13 (r/w)	12:8 (r/w)	7:4 (r/w)	3:2 (r/w)	1:0 (r/w)

Reserve	tHOLD (1)	tCYC	Tmli	tENV	TACK

31:26 (r/w)	25 (r/w)	24 (r/w)	23:21 (r/w)	20:16 (r/w)
TPDCYC	Reserved	PIO mode IORDY enable	tSS	TRP

See DRV #0 Configuration and Timing Control Register 1

Channel #3 S/G Engine Address counter Register (index_IDE3:54h | BA#3 + C03D4h)

31:0 (r)
Value of S/G engine address counter

Bit[31-0]: The value of channel #3's S/G engine address counter. When test mode is set (System Control register bit-10), the counter is cut to four 8bit counters and its value can be read from this register.

Channel #3 S/G Engine byte count counter Register (index_IDE3:58h | BA#3 + C03D8h)

31:24 (r)	23:0 (r)
Reserved	Value of S/G engine byte count counter 0

Bit[31:24]: Reserved.

Bit[23:0]: The value of channel #3's S/G engine byte count counter 0. When test mode is set (System Control register bit-14), the counter's clock is switched to PCI clock, the counter is broken to two 8bit counter and its value can be read from this register.

Channel #3 ATA Next Command Packet Pointer Register (index_IDE3:5Ch | BA#3 + C03DCh)

31:6 (r/w)	2:0 (r)
Base address of Next Command Packet	Reserved(000)

See **Channel#0 ATA Next Command Packet Pointer Register**.

Channel #3 IDE Control & Status Register (CICR3) (index_IDE3:60h | BA#3 + C03E0h)

7 (r/w	6 (r/w)	5 (r)	4 (r/w)	3 (r/w)	2 (r/w)	1 (r/w)	0 (r/w)
DMA Start/Stop	DMA R/W Direction	Reserved.	Interrupt Sequence ID				

15(r)	14(r/w)	13 (r/w)	12 (r/w)	11(r/w)	10 (r/w)	9(r/w)	8(r/w)
Reserved	IDE output Driving Selection	IDE Bus Floating that Dependent on CBLID# (0)	ATA bus Tri-state	ATA Software Reset	Mask INT (0)	Test Mode (0)	CSN Disable (0)

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

31 (r)	30 (r)	29 (r)	28 (r)	27(r)	26(r)	25(r)	24(r)
Data FIFO Empty	Control FIFO Empty	Reserved	Drive DMARQ Status	Drive INT Status	Reserved	Cable Status	

See **Channel#0 IDE Control & Status Register**.

4.6.6 Sequence Interrupt Control Unit

Sequence Counter Control Register0 (BA#2: 0h | BA#3 + C0400h)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

Bit[31]: A15 Error. It indicates an error condition is generated in A#15.

Bit[30]: A14 Error. It indicates an error condition is generated in A#14.

Bit[29]: A13 Error. It indicates an error condition is generated in A#13.

Bit[28]: A12 Error. It indicates an error condition is generated in A#12.

Bit[27]: A11 Error. It indicates an error condition is generated in A#11.

Bit[26]: A10 Error. It indicates an error condition is generated in A#10.

Bit[25]: A9 Error. It indicates an error condition is generated in A#9.

Bit[24]: A8 Error. It indicates an error condition is generated in A#8.

Bit[23]: A7 Error. It indicates an error condition is generated in A#7.

Bit[22]: A6 Error. It indicates an error condition is generated in A#6.

Bit[21]: A5 Error. It indicates an error condition is generated in A#5.

Bit[20]: A4 Error. It indicates an error condition is generated in A#4.

Bit[19]: A3 Error. It indicates an error condition is generated in A#3.

Bit[18]: A2 Error. It indicates an error condition is generated in A#2.

Bit[17]: A1 Error. It indicates an error condition is generated in A#1.

Bit[16]: A0 Error. It indicates an error condition is generated in A#0.

Bit[15]: X3 Error. It indicates an error condition is generated in X#3.

Bit[14]: X2 Error. It indicates an error condition is generated in X#2.

Bit[13]: X1 Error. It indicates an error condition is generated in X#1.

Bit[12]: X0 Error. It indicates an error condition is generated in X#0.

Bit[11]: D3 Error. It indicates an error condition is generated in D#3.

Bit[10]: D2 Error. It indicates an error condition is generated in D#2.

Bit[9]: D1 Error. It indicates an error condition is generated in D#1.

Bit[8]: D0 Error. It indicates an error condition is generated in D#0.

Bit[7:6]: Reserved.

Bit[5]: Sequence Interrupt Mask. When this bit is set, it will mask an interrupt generated by the sequence counter.

Bit[4:0]: Sequence Counter. It indicates how many engines run in a raid sequence. It will collect all interrupts generated by those engines that run in this sequence ID. If it sets zero, all interrupts generated by those engines will pass through.

Sequence Counter Control Register1 (BA#2: 4h | BA#3 + C0404h)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control Register2 (BA#2: 8h | BA#3 + C0408h)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control Register3 (BA#2: Ch | BA#3 + C040Ch)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control Register4 (BA#2: 10h | BA#3 + C0410h)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control Register5 (BA#2: 14h | BA#3 + C0414h)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control Register6 (BA#2: 18h | BA#3 + C0418h)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)

serial interface Error	Reserved	SEQ INT Mask	SEQ CNT

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control Register7 (BA#2: 1Ch | BA#3 + C041Ch)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control Register8 (BA#2: 20h | BA#3 + C0420h)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control Register9 (BA#2: 24h | BA#3 + C0424h)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control RegisterA (BA#2: 28h | BA#3 + C0428h)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control RegisterB (BA#2: 2Ch | BA#3 + C042Ch)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control RegisterC (BA#2: 30h | BA#3 + C0430h)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control RegisterD (BA#2: 34h | BA#3 + C0434h)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control RegisterE (BA#2: 38h | BA#3 + C0438h)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control RegisterF (BA#2: 3Ch | BA#3 + C043Ch)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control Register10 (BA#2: 40h | BA#3 + C0440h)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control Register11 (BA#2: 44h | BA#3 + C0444h)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control Register12 (BA#2: 48h | BA#3 + C0448h)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control Register13 (BA#2: 4Ch | BA#3 + C044Ch)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control Register14 (BA#2: 50h | BA#3 + C0450h)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control Register15 (BA#2: 54h | BA#3 + C0454h)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control Register16 (BA#2: 58h | BA#3 + C0458h)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control Register17 (BA#2:5C h | BA#3 + C045Ch)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control Register18 (BA#2: 60h | BA#3 + C0460h)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control Register19 (BA#2: 64h | BA#3 + C0464h)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control Register1A (BA#2: 68h | BA#3 + C0468h)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control Register1B (BA#2: 6Ch | BA#3 + C046Ch)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control Register1C (BA#2: 70h | BA#3 + C0470h)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control Register1D (BA#2: 74h | BA#3 + C0474h)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control Register1E (BA#2: 78h | BA#3 + C0478h)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Counter Control Register1F (BA#2: 7Ch | BA#3 + C047Ch)

7(r)	6(r)	5(r/w)	4(r/w)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
serial interface Error	Reserved	SEQ INT Mask	SEQ CNT				

15(r)	14(r)	13(r)	12(r)	11(r)	10(r)	9(r)	8(r)
D3 Error	D2 Error	D1 Error	D0 Error	X3 Error	X2 Error	X1 Error	X0 Error

23(r)	22(r)	21(r)	20(r)	19(r)	18(r)	17(r)	16(r)
A7 Error	A6 Error	A5 Error	A4 Error	A3 Error	A2 Error	A1 Error	A0 Error

31(r)	30(r)	29(r)	28(r)	27(r)	26(r)	25(r)	24(r)
A15 Error	A14 Error	A13 Error	A12 Error	A11 Error	A10 Error	A9 Error	A8 Error

See Sequence Counter Control Register0.

Sequence Interrupt Status register (BA#2: 80h | BA#3 + C0480h) (Interrupt should be cleared when Bit[31:0] is read)

7 (r)	6 (r)	5 (r)	4 (r)	3(r)	2(r)	1(r)	0(r)
SEQ#7 INT	SEQ#6 INT	SEQ#5 INT	SEQ#4 INT	SEQ#3 INT	SEQ#2 INT	SEQ#1 INT	SEQ#0 INT

15 (r)	14 (r)	13 (r)	12 (r)	11 (r)	10 (r)	9 (r)	8 (r)
SEQ#F INT	SEQ#E INT	SEQ#D INT	SEQ#C INT	SEQ#B INT	SEQ#A INT	SEQ#9 INT	SEQ#8 INT

23 (r)	22 (r)	21 (r)	20 (r)	19 (r)	18 (r)	17 (r)	16 (r)
SEQ#17 INT	SEQ#16 INT	SEQ#15 INT	SEQ#14 INT	SEQ#13 INT	SEQ#12 INT	SEQ#11 INT	SEQ#10 INT

31 (r)	30 (r)	29 (r)	28 (r)	27 (r)	26 (r)	25 (r)	24 (r)
SEQ#1F INT	SEQ#1E INT	SEQ#1D INT	SEQ#1C INT	SEQ#1B INT	SEQ#1A INT	SEQ#19 INT	SEQ#18 INT

Bit[31]: SEQ#1F Interrupt. It indicates whether the SEQ#F interrupt is generated. This bit is cleared when it is read.

Bit[30]: SEQ#1E Interrupt. It indicates whether the SEQ#E interrupt is generated. This bit is cleared when it is read.

Bit[29]: SEQ#1D Interrupt. It indicates whether the SEQ#D interrupt is generated. This bit is cleared when it is read.

Bit[28]: SEQ#1C Interrupt. It indicates whether the SEQ#C interrupt is generated. This bit is cleared when it is read.

Bit[27]: SEQ#1B Interrupt. It indicates whether the SEQ#B interrupt is generated. This bit is cleared when it is read.

Bit[26]: SEQ#1A Interrupt. It indicates whether the SEQ#A interrupt is generated. This bit is cleared when it is read.

Bit[25]: SEQ#19 Interrupt. It indicates whether the SEQ#9 interrupt is generated. This bit is cleared when it is read.

Bit[24]: SEQ#18 Interrupt. It indicates whether the SEQ#8 interrupt is generated. This bit is cleared when it is read.

Bit[23]: SEQ#17 Interrupt. It indicates whether the SEQ#7 interrupt is generated. This bit is cleared when it is read.

Bit[22]: SEQ#16 Interrupt. It indicates whether the SEQ#6 interrupt is generated. This bit is cleared when it is read.

Bit[21]: SEQ#15 Interrupt. It indicates whether the SEQ#5 interrupt is generated. This bit is cleared when it is read.

Bit[20]: SEQ#14 Interrupt. It indicates whether the SEQ#4 interrupt is generated. This bit is cleared when it is read.

Bit[19]: SEQ#13 Interrupt. It indicates whether the SEQ#3 interrupt is generated. This bit is cleared when it is read.

Bit[18]: EQ#12 Interrupt. It indicates whether the SEQ#2 interrupt is generated. This bit is cleared when it is read.

Bit[17]: SEQ#11 Interrupt. It indicates whether the SEQ#1 interrupt is generated. This bit is cleared when it is read.

Bit[16]: SEQ#10 Interrupt. It indicates whether the SEQ#0 interrupt is generated. This bit is cleared when it is read.

Bit[15]: SEQ#F Interrupt. It indicates whether the SEQ#F interrupt is generated. This bit is cleared when it is read.

Bit[14]: SEQ#E Interrupt. It indicates whether the SEQ#E interrupt is generated. This bit is cleared when it is read.

Bit[13]: SEQ#D Interrupt. It indicates whether the SEQ#D interrupt is generated. This bit is cleared when

it is read.

Bit[12]: SEQ#C Interrupt. It indicates whether the SEQ#C interrupt is generated. This bit is cleared when it is read.

Bit[11]: SEQ#B Interrupt. It indicates whether the SEQ#B interrupt is generated. This bit is cleared when it is read.

Bit[10]: SEQ#A Interrupt. It indicates whether the SEQ#A interrupt is generated. This bit is cleared when it is read.

Bit[9]: SEQ#9 Interrupt. It indicates whether the SEQ#9 interrupt is generated. This bit is cleared when it is read.

Bit[8]: SEQ#8 Interrupt. It indicates whether the SEQ#8 interrupt is generated. This bit is cleared when it is read.

Bit[7]: SEQ#7 Interrupt. It indicates whether the SEQ#7 interrupt is generated. This bit is cleared when it is read.

Bit[6]: SEQ#6 Interrupt. It indicates whether the SEQ#6 interrupt is generated. This bit is cleared when it is read.

Bit[5]: SEQ#5 Interrupt. It indicates whether the SEQ#5 interrupt is generated. This bit is cleared when it is read.

Bit[4]: SEQ#4 Interrupt. It indicates whether the SEQ#4 interrupt is generated. This bit is cleared when it is read.

Bit[3]: SEQ#3 Interrupt. It indicates whether the SEQ#3 interrupt is generated. This bit is cleared when it is read.

Bit[2]: SEQ#2 Interrupt. It indicates whether the SEQ#2 interrupt is generated. This bit is cleared when it is read.

Bit[1]: SEQ#1 Interrupt. It indicates whether the SEQ#1 interrupt is generated. This bit is cleared when it is read.

Bit[0]: SEQ#0 Interrupt. It indicates whether the SEQ#0 interrupt is generated. This bit is cleared when it is read.

General Control Register (BA#2:804h | BA#3 + C0484h)

31:9 (r)	8(r/w)	7:1(r)	0(r/w)
Reserved	INFO Enable	Reserved	Force Host FIFO Dump

Bit[31:1]: Reserved.

Bit[8]: INFO Enable: When this bit is set, the chip information will be sent by CINF[0].

Bit[0]: Force Host FIFO Dump. When this bit is set, all data in the host FIFO will be dumped to the local memory. This bit will be cleared by hardware.

C2C ID Assign Register (BA#2: 88h | BA#3 + C0488h)

31:4 (r)	3:0 (w)
Reserved	ID Assign Port

Bit[31:4]: Reserved.

Bit[3:0]: Device ID Assign Port. When these bits are ‘1110’, it indicates that device ID0 is assigned. When these bits are ‘1101’, it indicates that device ID1 is assigned. When these bits are ‘1011’, it indicates that device ID2 is assigned. When these bits are ‘0111’, it indicates that device ID3 is assigned.

C2C ID Inquire Register (BA#2: 8Ch | BA#3 + C048Ch)

31:4 (r)	3 (r)	2 (r)	1 (r)	0 (r)
Reserved	ID3 Present	ID2 Present	ID1 Present	Reserved

Bit[31:4]: Reserved.

Bit[3]: Device ID3 Present. It indicates whether device ID#3 presents or not. When this bit is zero, it indicates that ID1 is present.

Bit[2]: Device ID2 Present. It indicates whether device ID#2 presents or not. When this bit is zero, it indicates that ID2 is present.

Bit[1]: Device ID1 Present. It indicates whether device ID#1 presents or not. When this bit is zero, it indicates that ID3 is present.

Bit[0]: Reserved.

5 ATA/ATAPI/XOR/HOST DMA packet and SG format

5.1 ATA/ATAPI Packet (Variable size)

BYTE 3	BYTE 2	BYTE 1	BYTE 0	
Delay Sequence ID	Syn. Sequence ID	Reserved	Control	00h
PSG[31:0]				04h
NCA[31:0]				08h
ATRL Data 1_0	ATRL Register 1	ATRL Data 0_0	ATRL Register 0	0Ch
ATRL Data 2_2	ATRL Data 2_1	ATRL Data 2_0	ATRL Register 2	10h
…	ATRL Data 3_0		ATRL Register 3	14h
…	…	…	…	18h
ATRL Data N_0	ATRL Register N	…	…	.

Information about ATRL register please refers to examples that describe as PDC20621 Programming Guide for ATA-ATRL Packet Format.

Delay Sequence ID

7	6	5	4	3	2	1	0
Reserved			Delay Sequence ID				

Bit[3:0]: Delay Sequence ID.

Bit[7:4]: Reserved.

Synchronization Sequence ID

7	6	5	4	3	2	1	0
Reserved			Synchronization Sequence ID				

Bit[3:0]: Synchronization Sequence ID.

Bit[7:4]: Reserved.

ATA/ATAPI Packet Control

7	6	5	4	3	2	1	0
Reserved		NCA Pause	Delay Enable	None Data Command	DMA R/W	Reserved	

Bit[0:1]: Reserved

Bit[2]: 1 = ATA/ATAPI READ DMA command.

0 = ATA/ATAPI WRITE DMA command.

Bit[3]: 1 = ATA/ATAPI None Data Command.

0 = ATA/ATAPI DMA Command.

Bit[4]: 1= Packet command with delay transaction that depends on synchronization sequence ID.

0= Packet command without delay transaction.

Bit[5]: 1=Pause to execute next packet command after this packet command finished.

0=Continue to execute next packet command after this packet command finished.

Bit[7:6]: Reserved.

Local Memory Scatter/Gather Point (PSG)

31:3	2:0
PSG[31:3]	Reserved(000)

Bit[2:0] Reserved.

Bit[31:3] PSG of Local Host Memory.

Next Command Point (NCA)

31:6	5:0
NCA[31:6]	Reserved(000000)

Bit[2:0] Reserved.

Bit[31:3] Next command address. If NCA is '0000_0000_0000_0000_0000', it indicates no next command.

5.2 XOR Packet

BYTE 3	BYTE 2	BYTE 1	BYTE 0	
Delay ID	Syn. ID	Reserved	Control	00h
PSG0[31:0]				04h
PSG1[31:0]				08h
PSG2[31:0]				0Ch
PSG3[31:0]				10h
PSG4[31:0]				14h
PSG5[31:0]				18h
NCA[31:0]				1Ch

Delay Sequence ID

7	6	5	4	3	2	1	0
Reserved			Delay Sequence ID				

Bit[3:0]: Delay Sequence ID.

Bit[7:4]: Reserved.

Synchronization Sequence ID

7	6	5	4	3	2	1	0
Reserved			Synchronization Sequence ID				

Bit[3:0]: Synchronization Sequence ID.

Bit[7:4]: Reserved.

XOR Packet Command Control

7	6	5	4	3	2	1	0
Reserved		NCA Pause	Delay Enable	Reserved			XOR Type

Bit[0]: 1 = execute XOR command.

0 = execute Compare Command.

Bit[3:1]: Reserved.

Bit[4]: 1= Packet command with delay transaction that depends on synchronization sequence ID.
0= Packet command without delay transaction.

Bit[5] 1=Pause to execute next packet command after this packet command finished.
0=Continue to execute next packet command after this packet command finished.

Bit[7:6]: Reserved.

Local Memory Scatter/Gather Point (PSGn)

31:3	2:0
PSGn[31:3]	Reserved(000)

Bit[2:0] Reserved.

Bit[31:3] PSG of Local Host Memory. If PSGn is '0000_0000_0000_0000_0000', it indicates no PSGn.

Next Command Point (NCA)

31:5	4:0
NCA[31:5]	Reserved(00000)

Bit[2:0] Reserved.

Bit[31:3] Next command address. If NCA is '0000_0000_0000_0000_0000', it indicates no next command.

5.3 HOST DMA Packet

BYTE 3	BYTE 2	BYTE 1	BYTE 0	
Delay ID	Syn. ID	Reserved	Control	00h
PSG0[31:0]				04h
PSG1[31:0]				08h
NCA[31:0]				0Ch

Delay Sequence ID

7	6	5	4	3	2	1	0
Reserved			Delay Sequence ID				

Bit[3:0]: Delay Sequence ID.

Bit[7:4]: Reserved.

Synchronization Sequence ID

7	6	5	4	3	2	1	0
Reserved			Synchronization Sequence ID				

Bit[3:0]: Synchronization Sequence ID.

Bit[7:4]: Reserved.

Host DMA Packet Control

7	6	5	4	3	2	1	0
Reserved		NCA Pause	Delay Enable	Reserved	DMA R/W	Reserved	

Bit[1:0] Reserved.

Bit[2]: 1 = PCI bus master write command.

0 = PCI bus master read command.

Bit[3] Reserved.

Bit[4]: 1= Packet command with delay transaction that depends on synchronization sequence ID.

0= Packet command without delay transaction.

Bit[5] 1=Pause to execute next packet command after this packet command finished.

0=Continue to execute next packet command after this packet command finished.

Bit[7:6]: Reserved.

PCI Host Memory Scatter/Gather Point (PSG0)

31:3	2:0
PSG[31:3]	Reserved(000)

Bit[2:0] Reserved.

Bit[31:3] PSG of PCI Host Memory.

Local Memory Scatter/Gather Point (PSG1)

31:3	2:0
PSG[31:3]	Reserved(000)

Bit[2:0] Reserved.

Bit[31:3] PSG of Local Memory.

Next Command Point(NCA)

31:4	3:0
NCA[31:4]	Reserved(0000)

Bit[2:0] Reserved.

Bit[31:3] Next command address. If NCA is '0000_0000_0000_0000_0000', it indicates no next command.

5.4 SG format (8 bytes)

BYTE 3	BYTE 2	BYTE 1	BYTE 0
SG Address			
8 bits control	SG Byte Count		

SG Address

31:3	2:0
SG Address	Reserved(00)

Bit[1:0] Reserved.

Bit[31:2] SG Address. The 4 bytes specify the byte address of a physical memory region.

SG Byte Count

23:3	2:0
SG Byte Count	Reserved(00)

Bit[1:0] Reserved.

Bit[24:2] SG Byte Count. The 3 bytes specify the byte count of a physical memory region. A value of zero in these three bytes indicates 16M.

Control bit definition

7	6	5	4	3	2	1	0
Termination(1)	R	Source (XOR)	Destination (XOR)	Dump (IDE)	Reserved		

Bit[2:0] Reserved.

Bit[3] IDE Scatter/Gather Data Dump.

Bit[5:4] 00b: Don't Care

01b: XOR Destination.

10b: XOR Source.

11b: XOR Source and Destination.

Bit[6] Reserved.

Bit[7] EOT. It indicates the end of table. Bus master operation terminates when the last descriptor has been retired.