

# PC87427 Server/I/O with SensorPath™ Health Monitoring

## General Description

The National Semiconductor PC87427 is targeted for a wide range of servers, workstations and high-end desktops that use the Low Pin Count (LPC) bus for the host interface and an SMBus® interface for either a Baseboard Management Controller (BMC) or mini-BMC (mBMC), both of which are optional.

For LPC and SMBus access, the PC87427 features a fast X-Bus, over which boot flash and I/O devices can be accessed. The PC87427 supports X-Bus address line forcing (to 0 or 1) to create memory windows for BIOS data storage.

When  $V_{SB}$  exists, the BMC or mBMC can access the PC87427 and its fast X-Bus via SMBus. The SMBus also controls serial port float, RTC access, and serial port interconnection (snoop and take-over modes). In addition, the PC87427 provides routing of up to two selected LPC I/O port transactions to the GPIO Extension Port.

The PC87427 provides a  $V_{SB}$ -powered high-frequency clock for on-chip peripherals; it also provides a configurable high-frequency clock for other  $V_{SB}$ -powered platform components.

The PC87427 supports SensorPath health monitor interface to LMPCxx sensors, fan monitoring and control, and a chassis intrusion detector.

The System Wake-Up Control (SWC) module supports flexible wake-up and power-off request mechanisms for all platforms (i.e., with or without BMC/mBMC).

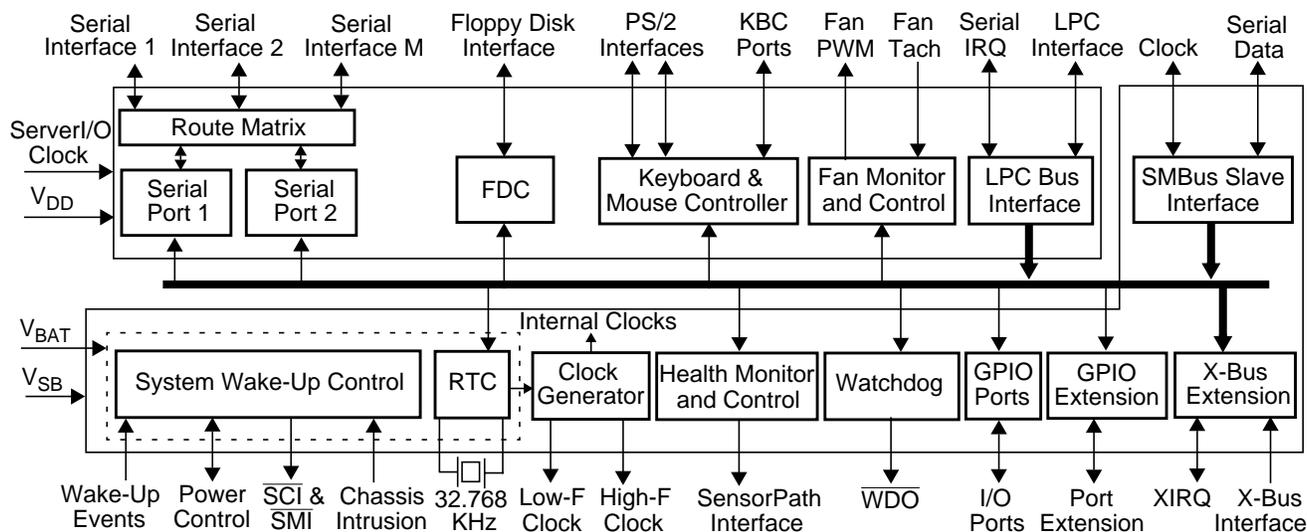
The PC87427 supports both I/O and memory mapping of module registers and enables building legacy-free systems.

The PC87427 also incorporates a Floppy Disk Controller (FDC), two serial ports (UARTs), a Keyboard and Mouse Controller (KBC), General-Purpose Input/Output (GPIO), GPIO extension for additional off-chip GPIO ports, and an interrupt serializer for parallel IRQs.

## Outstanding Features

- Legacy-reduced Advanced I/O, optimized for high-end platforms. Legacy modules: FDC, two Serial Ports (UARTs) and a Keyboard and Mouse Controller (KBC).
- SensorPath system health support for LMXX sensors, fan monitor/control, and chassis intrusion detection, for all platforms (i.e., with or without a BMC or mBMC).
- 8/16-bit fast X-Bus extension for boot flash, memory and I/O.
- I/O-mapped and memory-mapped registers.
- $V_{SB}$ -powered SMBus access to modules and fast X-Bus.
- Two sets of BIOS code and data support, for main and back-up BIOS.
- Extremely low current consumption in Battery Backup mode.
- Serial Interface for manageability (Serial Interface M). Two-to-one multiplexing of Serial Ports 1 and 2.
- 52 GPIO ports with a variety of wake-up events, plus GPIO extension for additional off-chip GPIO ports.
- Watchdog for autonomous system recovery for BIOS Boot process and for operating system use.
- 128-pin PQFP package.

## Block Diagram



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## Features

### System Health Support

- SensorPath interface to sensors optimizes digital/analog partitioning
  - Simplifies board design and routing
  - Supports distributed sensors and centralized control
  - Off-loads SMBus, faster boot time
- Fan Monitor and Control (FMC)
  - Four PWM-based fan controls
  - Eight 16-bit resolution tachometer inputs
  - Software or local temperature feedback control
- Chassis intrusion detection

### Bus Interfaces

- LPC Bus Interface
  - Based on Intel's *LPC Interface Specification Revision 1.0, September 29, 1997*
  - Synchronous cycles using up to 33 MHz bus clock
  - 8-bit I/O and 8-bit Memory read and write cycles
  - Up to four 8-bit DMA channels
  - Serial IRQ
  - Supports bootable memory
  - Supports LPC and FWH boot transactions
  - Supports registers memory and I/O mapping
- SMBus Interface
  - Compliant with *SMBus Specification Revision 2.0, August 3, 2000*
  - Enables a system controller to access the internal functions and the fast X-Bus extension
  - Proprietary commands for read/write byte from/to:
    - Internal register
    - X-Bus I/O device
    - X-Bus memory device
  - Slave address:
    - One of two values selected by strap
    - Programmable through the LPC bus
    - $V_{BAT}$  backed-up
  - Supports  $\overline{SMBALERT}$
  - Concurrent access with the LPC bus
  - $V_{SB}$  powered
  - Optional internal pull-up on the two SMBus pins
- Fast X-Bus Extension
  - Supports I/O and memory read/write operations
  - 8- or 16-bit data bus, 28-bit addressing
  - Accessible from both LPC bus and SMBus
  - $V_{SB}$  powered
  - Boot configuration selected by straps
  - Programmable protection control for access from the LPC bus
  - Supports three XIRQ external interrupts

- Multiplexed address-data lines:
  - Four direct address lines
  - Partial non-multiplexed option
- Four chip-select outputs, each supporting multiple zones:
  - Two BIOS memory zones (up to 32 Mbytes total)
  - Two user-defined memory zones (up to 32 Mbytes total)
  - Four user-defined I/O zones
- Address line forcing (to 0 or 1) for access to two BIOS code and data sets
- Optional indirect addressing of memory
- $\overline{XRD}$ -XEN or  $\overline{XWR}$ -XR/ $\overline{W}$  mode support
- Supports both slow and fast devices
- For faster transactions in 16-bit data bus, strobe signals for address latches change automatically only when the address is changed
- Configuration Control
  - Compliant with *PC01 Specification Revision 1.0, 1999-2000*
  - Compliant with *Hardware Design Guide Version 3.0 for Microsoft Windows 2000 Server, June 30 2000*
  - Plug and Play (PnP) Configuration register structure
  - Base Address strap, to setup the address of the Index-Data register pair
  - Flexible resource allocation for all logical devices:
    - Relocatable base address
    - 15 IRQ routing options to serial IRQ
    - Up to four optional 8-bit DMA channels
  - SMBus control over pin multiplexing, module disable and output TRI-STATE<sup>®</sup> for all Legacy modules

### Legacy Modules

- Serial Ports 1 and 2
  - Software compatible with the 16550A and the 16450
  - Supports shadow register for write-only bit monitoring
  - UART data rates up to 1.5 Mbaud
  - Three sets of Serial Interface pins
    - Serial Interface 1
    - Snoop or Take-over connection of Serial Interface M
    - Two-to-one multiplexing of Serial Ports 1 and 2 to Serial Interface 2
- Floppy Disk Controller (FDC)
  - Programmable write protect
  - Supports FM and MFM modes
  - Supports Enhanced mode command for three-mode Floppy Disk Drive (FDD)
  - Perpendicular recording drive support for 2.88 MB
  - Burst and Non-Burst modes
  - Full support for IBM Tape Drive Register (TDR) implementation of AT and PS/2 drive types

## Features (Continued)

- 16-byte FIFO
- Error-free handling of data overrun and underrun
- Software compatible with the PC8477, which contains a superset of the FDC functions in the  $\mu$ DP8473, NEC  $\mu$ PD765A/B and N82077
- High-performance digital separator
- Supports standard 5.25" and 3.5" FDDs
- Supports one FDD
- Supports fast tape drives (2 Mbps) and standard tape drives (1 Mbps, 500 Kbps and 250 Kbps)
- Keyboard and Mouse Controller (KBC)
  - 8-bit microcontroller, software compatible with 8042AH and PC87911
  - Standard interface (60h, 64h, IRQ1 and IRQ12)
  - Supports two external swappable PS/2 interfaces for keyboard and mouse
  - Five programmable, dedicated, quasi-bidirectional I/O lines (Fast GA20/P21, KBRST/P20, P12, P16, P17)

### General-Purpose I/O Module

- 52 General-Purpose I/O (GPIO) Ports
  - Individually assigned to either LPC or SMBus control
  - 45 ports individually configured as input or output
  - 7 output ports
  - Programmable features for each output pin:
    - Drive type (open-drain, push-pull or TRI-STATE)
    - TRI-STATE on  $V_{DD}$ -fall detection for pins driving  $V_{DD}$ -supplied devices
  - Programmable option for internal pull-up resistor on each input pin
  - Lock option for the configuration and data of each output pin
  - 16 GPIO ports generate  $\overline{\text{IRQ/SIOSMI/SIOSCI}}$  for wake-up events, with individual:
    - Enable control
    - Polarity and edge/level selection
    - Debounce mechanism
  - $V_{SB}$  powered
  - Low-cost external GPIO port extension via a serial bus
  - I/O ports transactions routing to the GPIO port extension
- Real-Time Clock
  - DS1287, MC146818 and PC87911 compatible
  - Battery-backed 242-byte CMOS RAM, in two banks (accessed through 70-71h and 72-73h)
  - Selective lock mechanisms for the RTC RAM
  - Y2K-compliant calendar, including century and automatic leap-year adjustment
  - Time of day in seconds, minutes and hours, which allows a 12-hour or 24-hour format with optional adjustment for daylight saving time

- Separated SMBus access to RTC RAM and RTC Control D register
- Battery level measurement

### Power Management

- Supports *ACPI Specification Revision 2.0b, July 27, 2000*
- System Wake-Up Control (SWC)
  - Wake-up request on detection of:
    - Preprogrammed Keyboard or Mouse sequence
    - External modem ring from  $\overline{\text{RI1}}$  or  $\overline{\text{RI2}}$  on serial ports
    - Predetermined RTC date and time alarm
    - General-Purpose Input Events from up to 16 GPIO pins
    - IRQs of internal logical devices
  - Optional routing of power-up request to SERIRQ, SIOSMI, SIOSCI, PWBTOUT and ONCTL
  - Routing control per input/output event combination
  - Outputs enable/disable per event and system state combination (ACPI Sx states)
  - Implements bank "b" of the ACPI registers
  - Suspend modes via software emulation (control)
  - Battery-backed event-logic configuration
  - Power Button support, featuring:
    - On/Off control
    - Power-off, 4-second override
    - Power Button output
  - Sleep Button support
- Power Supply On/Off control
  - Supports Legacy- and ACPI-compatible Power Button
  - Direct power supply control in response to wake-up events
  - Programmable Crowbar time-out for "On" request
  - On/Off control via software emulation
  - Power-fail recovery
- Enhanced Power Management (PM), including:
  - Special configuration registers for power down
  - Reduced current leakage from pins
  - Low-power CMOS technology
  - Capability for disabling all modules
- Keyboard Events
  - Wake-up on any key
  - Supports programmable 8-byte sequence "password" for Power Management
  - Simultaneous recognition of three programmable keys (sequences): "Power", "Sleep" and "Resume"
- Power Active Timers
  - Two power-on, elapsed-time counters for the main ( $V_{DD}$ ) and standby ( $V_{SB}$ ) power supplies
  - 32-bit counters, clocked by a 1-second clock
  - $V_{BAT}$  backed-up counters

## Features (Continued)

- Watchdog
  - Compliant with *Watchdog Timer Hardware Requirements for Microsoft Windows .NET Server, April 2002*
  - Autonomous system reset and programmable address line forcing on expiration of watchdog timer
  - Generates a 100 ms pulse at  $\overline{WDO}$  pin

## Clocking, Supply and Package Information

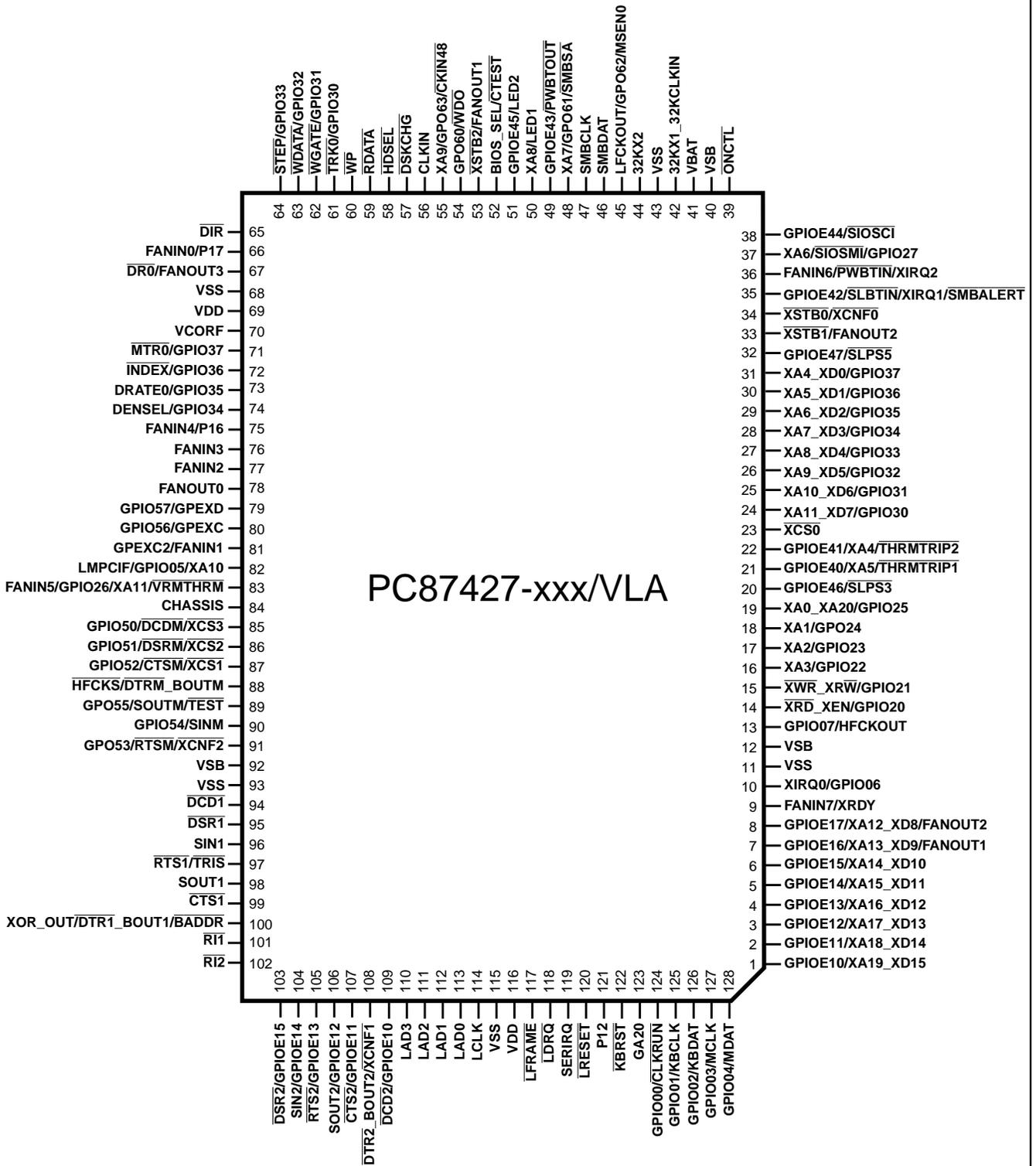
- Strap Input Controlled Operating Modes
  - Base Address ( $\overline{BADDR}$ ) for the PnP Index-Data register pair
  - Input clock presence ( $\overline{CKIN48}$ ) select
  - X-Bus configuration ( $\overline{XCNF2-0}$ ) select
  - SMBus slave address ( $\overline{SMBSA}$ ) select
  - High frequency clock selection ( $\overline{HFCKS}$ )
- Testability
  - XOR tree structure
    - Includes all the device pins (except the supply pins, oscillator pins and CHASSIS pin)
    - Selected at power-up by strap input ( $\overline{TEST}$ )
  - TRI-STATE device pins, selected at power-up by strap input ( $\overline{TRIS}$ )
- Clocks
  - LPC clock input (up to 33 MHz)
  - ServerI/O modules clock: 48 MHz input or internal clock multiplier
  - 32.768 KHz crystal
  - On-chip low-frequency clock generator:
    - 32.768 KHz for RTC, System Wake-Up Control (SWC), Power Active timers and the high-frequency clock generator
    - Very low power consumption
    - $V_{BAT}$  powered

- On-chip high-frequency clock generator:
  - Based on the 32.768 KHz clock
  - $V_{SB}$  powered
- Clock outputs:
  - LFCKOUT - 32.768 KHz or 1 Hz
  - HFCKOUT - configurable up to 48 MHz. The default frequency 6, 10, 24 or 40 MHz, configurable by strap.

- Protection
  - All pins are 5V tolerant and back-drive protected (except the LPC bus pins)
  - Separate battery pin that includes an internal UL protection resistor
  - GPIO multiplexing configuration lock
- Power Supply
  - 3.3V supply operation
  - Separate pins for main ( $V_{DD}$ ) and standby ( $V_{SB}$ ) power supplies
  - Backup battery input for RTC, SWC and Power Active timers
  - Separate pin for core voltage filtering ( $V_{CORF}$ )
  - Reduced standby power consumption
  - Very low power consumption for RTC and timers (0.9  $\mu$ A typical) from backup battery
- Package
  - 128-pin PQFP

# 1.0 Signal/Pin Connection and Description

## 1.1 CONNECTION DIAGRAM



Plastic Quad Flatpack (PQFP), JEDEC  
 Order Number PC87427-xxx/VLA  
 See NS Package Number VLA128A

xxx = Three-character identifier for National data, keyboard ROM and/or customer identification code.

## 1.0 Signal/Pin Connection and Description (Continued)

### 1.2 BUFFER TYPES AND SIGNAL/PIN DIRECTORY

The signal DC characteristics of the pins described in Section 1.4 are denoted by buffer type symbols, which are defined in Table 1. The pin multiplexing information refers to two different types of multiplexing:

- Multiplexed, denoted by a slash (/) between pins in the diagram in Section 1.1. Pins are shared between two different functions. Each function is associated with different board connectivity. Normally, the function selection is determined by the board design and cannot be changed dynamically. The multiplexing options must be configured by the BIOS on power-up to comply with the board implementation.
- Multiple Mode, denoted by an underscore (\_) between pins in the diagram in Section 1.1. Pins have two or more modes of operation within the same function. These modes are associated with the same external (board) connectivity. Mode selection can be controlled by the device driver through the registers of the functional block and does not require a special BIOS setup upon power-up. These pins are not considered multiplexed pins from the Server/I/O configuration perspective. The mode selection method (registers and bits), as well as the signal specification in each mode, are described within the functional description of the relevant functional block.

**Table 1. Buffer Types**

| Symbol            | Description   |
|-------------------|---|
| IN <sub>CS</sub>  | Input, CMOS compatible, with Schmitt Trigger  |
| IN <sub>OSC</sub> | Input, from crystal oscillator (not characterized)                                      |
| IN <sub>PCI</sub> | Input, PCI 3.3V   |
| IN <sub>SM</sub>  | Input, SMBus compatible   |
| IN <sub>T</sub>   | Input, TTL compatible   |
| IN <sub>TS</sub>  | Input, TTL compatible, with Schmitt Trigger   |
| IN <sub>ULR</sub> | Input, power, resistor protected (not characterized)                                    |
| O <sub>p/n</sub>  | Output, push-pull output buffer capable of sourcing <i>p</i> mA and sinking <i>n</i> mA |
| OD <sub>n</sub>   | Output, open-drain output buffer capable of sinking <i>n</i> mA                         |
| O <sub>OSC</sub>  | Output, to crystal oscillator (not characterized)                                       |
| O <sub>PCI</sub>  | Output, PCI 3.3V  |
| OD <sub>PCI</sub> | Output, open-drain, PCI 3.3V  |
| PWR               | Power pin   |
| GND               | Ground pin  |

## 1.0 Signal/Pin Connection and Description (Continued)

### 1.3 PIN MULTIPLEXING

The table below shows only multiplexed pins, their associated functional blocks and the configuration bits for the selection of the multiplexed options used in the PC87427.

**Table 2. Pin Multiplexing Configuration**

| Pin | Functional Block | Signal             | Functional Block | Signal                | Functional Block | Signal              | Functional Block       | Signal                | Configuration Select               |                                 |                               |
|-----|------------------|--------------------|------------------|-----------------------|------------------|---------------------|------------------------|-----------------------|------------------------------------|---------------------------------|-------------------------------|
| 1   | GPIO             | GPIOE10            | X-Bus            | XA19_XD15             |                  |                     |                        |                       | SIOCF3.XDATA16                     |                                 |                               |
| 2   |                  | GPIOE11            |                  | XA18_XD14             |                  |                     |                        |                       |                                    | SIOCF3.XDATA16                  |                               |
| 3   |                  | GPIOE12            |                  | XA17_XD13             |                  |                     |                        |                       |                                    |                                 |                               |
| 4   |                  | GPIOE13            |                  | XA16_XD12             |                  |                     |                        |                       |                                    |                                 |                               |
| 5   |                  | GPIOE14            |                  | XA15_XD11             |                  |                     |                        |                       |                                    |                                 | SIOCF3.XDATA16                |
| 6   |                  | GPIOE15            |                  | XA14_XD10             |                  |                     |                        |                       |                                    |                                 |                               |
| 7   |                  | GPIOE16            |                  | XA13_XD9              | FMC              |                     | FANOUT1                |                       |                                    | SIOCF3.XDATA16 & SIOCFB.FANOUT1 |                               |
| 8   |                  | GPIOE17            |                  | XA12_XD8              |                  | FANOUT2             |                        |                       |                                    | SIOCF3.XDATA16 & SIOCFB.FANOUT2 |                               |
| 9   |                  |                    |                  | XRDY                  |                  | FANIN7              |                        |                       |                                    |                                 | SIOCF4.XRDYMUX                |
| 10  | GPIO             | GPIO06             |                  | XIRQ0                 |                  |                     |                        |                       | SIOCF5.XIRQ0MUX                    |                                 |                               |
| 13  |                  | GPIO07             | Clocks           | HFCKOUT               |                  |                     |                        |                       | SIOCF4.HFCKMUX                     |                                 |                               |
| 14  |                  | GPIO20             | X-Bus            | $\overline{XRD\_XEN}$ |                  |                     |                        |                       |                                    | SIOCF4.NOXBUS                   |                               |
| 15  |                  | GPIO21             |                  | $\overline{XWR\_XRW}$ |                  |                     |                        |                       |                                    |                                 |                               |
| 16  |                  | GPIO22             |                  | XA3                   |                  |                     |                        |                       |                                    |                                 |                               |
| 17  |                  | GPIO23             |                  | XA2                   |                  |                     |                        |                       |                                    |                                 |                               |
| 18  |                  | GPIO24             |                  | XA1                   |                  |                     |                        |                       |                                    |                                 |                               |
| 19  |                  | GPIO25             |                  | XA0_XA20              |                  |                     |                        |                       |                                    |                                 |                               |
| 20  |                  | GPIOE46            | SWC              | $\overline{SLPS3}$    |                  |                     |                        |                       | SIOCF3.EXTSTMUX                    |                                 |                               |
| 21  |                  | GPIO               | GPIOE40          |                       | XA5              | HMC                 | $\overline{THRMTRIP1}$ |                       |                                    | SIOCF4.NOADDIR & SIOCFB.TRIP1   |                               |
| 22  |                  |                    | GPIOE41          |                       | XA4              |                     | $\overline{THRMTRIP2}$ |                       |                                    |                                 | SIOCF4.NOADDIR & SIOCFB.TRIP2 |
| 24  |                  |                    | GPIO30           | X-Bus                 | XA11_XD7         |                     |                        |                       |                                    |                                 | SIOCF4.NOXBUS                 |
| 25  |                  |                    | GPIO31           |                       | XA10_XD6         |                     |                        |                       |                                    |                                 |                               |
| 26  |                  |                    | GPIO32           |                       | XA9_XD5          |                     |                        |                       |                                    |                                 |                               |
| 27  |                  |                    | GPIO33           |                       | XA8_XD4          |                     |                        |                       |                                    |                                 |                               |
| 28  |                  |                    | GPIO34           |                       | XA7_XD3          |                     |                        |                       |                                    |                                 |                               |
| 29  |                  |                    | GPIO35           |                       | XA6_XD2          |                     |                        |                       |                                    |                                 |                               |
| 30  |                  |                    | GPIO36           | XA5_XD1               |                  |                     |                        |                       |                                    |                                 |                               |
| 31  |                  |                    | GPIO37           | XA4_XD0               |                  |                     |                        |                       |                                    |                                 |                               |
| 32  |                  | GPIOE47            | SWC              | $\overline{SLPS5}$    |                  |                     |                        |                       |                                    | SIOCF3.EXTSTMUX                 |                               |
| 33  | X-Bus            | $\overline{XSTB1}$ | FMC              | FANOUT2               |                  |                     |                        |                       | SIOCF5.XSTB1MUX                    |                                 |                               |
| 34  |                  | $\overline{XSTB0}$ | Straps           | $\overline{XCNF0}$    |                  |                     |                        |                       |                                    |                                 |                               |
| 35  |                  | XIRQ1              | GPIO             | GPIOE42               | SWC              | $\overline{SLBTIN}$ | SMBus                  | $\overline{SMBALERT}$ | SIOCF3.SLBTIMUX & SIOCF3.XIRQ1MUX  |                                 |                               |
| 36  |                  | XIRQ2              | FMC              | FANIN6                |                  | $\overline{PWBTIN}$ |                        |                       | SIOCF3.PWBTIMUX & SIOCFB.FANIN6MUX |                                 |                               |
| 37  |                  | XA6                | GPIO             | GPIO27                |                  | $\overline{SIOSMI}$ |                        |                       |                                    | SIOCF3.SMIMUX & SIOCF4.NOADDIR  |                               |
| 38  |                  |                    |                  | GPIOE44               |                  | $\overline{SIOSCI}$ |                        |                       |                                    | SIOCF3.SCIMUX                   |                               |

# 1.0 Signal/Pin Connection and Description (Continued)

## Table 2. Pin Multiplexing Configuration (Continued)

| Pin | Functional Block   | Signal     | Functional Block   | Signal     | Functional Block | Signal  | Functional Block | Signal                              | Configuration Select          |                                |
|-----|--------------------|------------|--------------------|------------|------------------|---------|------------------|-------------------------------------|-------------------------------|--------------------------------|
| 45  | GPIO               | GPO62      | Clocks             | LFCKOUT    | FDC              | MSEN0   |                  |                                     | SIOCF4.LFCKMUX                |                                |
| 48  |                    | GPO61      | X-Bus              | XA7        | Straps           | SMBSA   |                  |                                     | SIOCF4.NOADDR                 |                                |
| 49  |                    | GPIOE43    | SWC                | PWBTOUT    |                  |         |                  |                                     | SIOCF3.PWBTOMUX               |                                |
| 50  | X-Bus              | XA8        |                    | LED1       |                  |         |                  | SIOCF4.NOADDR                       |                               |                                |
| 51  | GPIO               | GPIOE45    |                    | LED2       |                  |         |                  | SIOCF3.LED2MUX                      |                               |                                |
| 52  | X-Bus              | BIOS_SEL   | Straps             | CTEST      |                  |         |                  |                                     |                               |                                |
| 53  | X-Bus              | XSTB2      | FMC                | FANOUT1    |                  |         |                  | SIOCF5.XSTB2MUX                     |                               |                                |
| 54  | GPIO               | GPO60      | Watchdog           | WDO        |                  |         |                  | SIOCF2.WDOMUX                       |                               |                                |
| 55  |                    | GPO63      | X-Bus              | XA9        | Straps           | CKIN48  |                  | SIOCF4.NOADDR                       |                               |                                |
| 61  | GPIO               | GPIO30     | FDC                | TRK0       |                  |         |                  | SIOCF3.GP3AMUX                      |                               |                                |
| 62  |                    | GPIO31     |                    | WGATE      |                  |         |                  |                                     |                               |                                |
| 63  |                    | GPIO32     |                    | WDATA      |                  |         |                  |                                     |                               |                                |
| 64  |                    | GPIO33     |                    | STEP       |                  |         |                  |                                     |                               |                                |
| 66  | FMC                | FANIN0     | KBC                | P17        |                  |         |                  | SIOCF2.P17MUX                       |                               |                                |
| 67  |                    | FANOUT3    |                    | DR0        |                  |         |                  | SIOCFB.FANOUT3                      |                               |                                |
| 71  | GPIO               | GPIO37     | FDC                | MTR0       |                  |         |                  | SIOCF3.GP3AMUX                      |                               |                                |
| 72  |                    | GPIO36     |                    | INDEX      |                  |         |                  |                                     |                               |                                |
| 73  |                    | GPIO35     |                    | DRATE0     |                  |         |                  |                                     |                               |                                |
| 74  |                    | GPIO34     |                    | DENSEL     |                  |         |                  |                                     |                               |                                |
| 75  | FMC                | FANIN4     | KBC                | P16        |                  |         |                  | SIOCF2.P16MUX                       |                               |                                |
| 79  | GPIO               | GPIO57     | GPIO               | GPEXD      |                  |         |                  | SIOCF3.GPEXMUX                      |                               |                                |
| 80  |                    | GPIO56     |                    | GPEXC      |                  |         |                  |                                     |                               |                                |
| 81  | FMC                | FANIN1     |                    | GPEXC2     |                  |         |                  | SIOCFB.FANIN1MUX & SIOCFD.GPEXC2MUX |                               |                                |
| 82  | X-Bus              | XA10       | HMC                | LMPCIF     | GPIO             | GPIO05  |                  |                                     | SIOCF4.NOADDR & SIOCFD.LMPCIF |                                |
| 83  |                    | XA11       |                    | VRMTHRM    |                  | GPIO26  | FMC              | FANIN5                              | SIOCF4.NOADDR & SIOCFB.FANIN5 |                                |
| 85  |                    | XCS3       | Serial Interface M | DCDM       |                  | GPIO50  |                  |                                     |                               | SIOCF3.SIMMUX & SIOCF5.XCS3MUX |
| 86  |                    | XCS2       |                    | DSRM       |                  | GPIO51  |                  |                                     |                               | SIOCF3.SIMMUX & SIOCF5.XCS2MUX |
| 87  |                    | XCS1       |                    | CTSM       |                  | GPIO52  |                  |                                     |                               | SIOCF3.SIMMUX & SIOCF5.XCS1MUX |
| 88  | Straps             | HFCKS      |                    | DTRM_BOUTM |                  |         |                  |                                     |                               |                                |
| 89  |                    | TEST       |                    | SOUTM      |                  | GPO55   |                  |                                     |                               |                                |
| 90  |                    |            |                    | SINM       | GPIO             | GPIO54  |                  | SIOCF3.SIMMUX                       |                               |                                |
| 91  | Straps             | XCNF2      |                    | RTSM       |                  | GPO53   |                  |                                     |                               |                                |
| 97  | Serial Interface 1 | RTS1       | Straps             | TRIS       |                  |         |                  |                                     |                               |                                |
| 100 | Serial Interface 1 | DTR1_BOUT1 | Straps             | BADDR      | Testability      | XOR_OUT |                  |                                     | For XOR_OUT selection         |                                |

## 1.0 Signal/Pin Connection and Description (Continued)

Table 2. Pin Multiplexing Configuration (Continued)

| Pin | Functional Block | Signal  | Functional Block   | Signal | Functional Block | Signal | Functional Block | Signal          | Configuration Select |
|-----|------------------|---------|--------------------|--------|------------------|--------|------------------|-----------------|----------------------|
| 103 | GPIO             | GPIOE15 | Serial Interface 2 | DSR2   |                  |        |                  |                 | SIOCF2.CLKRNMUX      |
| 104 |                  | GPIOE14 |                    | SIN2   |                  |        |                  |                 |                      |
| 105 |                  | GPIOE13 |                    | RTS2   |                  |        |                  |                 |                      |
| 106 |                  | GPIOE12 |                    | SOUT2  |                  |        |                  |                 |                      |
| 107 |                  | GPIOE11 |                    | CTS2   |                  |        |                  |                 |                      |
| 108 |                  | Straps  |                    | XCNF1  | DTR2_BOUT2       |        |                  |                 |                      |
| 109 |                  | GPIOE10 |                    | DCD2   |                  |        |                  | SIOCF2.CLKRNMUX |                      |
| 124 |                  | GPIO00  | LPC                | CLKRUN |                  |        |                  | SIOCF2.CLKRNMUX |                      |
| 125 |                  | GPIO01  | KBC                | KBCLK  |                  |        |                  | SIOCF2.NOKBC    |                      |
| 126 |                  | GPIO02  |                    | KBDAT  |                  |        |                  |                 |                      |
| 127 |                  | GPIO03  |                    | MCLK   |                  |        |                  |                 |                      |
| 128 |                  | GPIO04  |                    | MDAT   |                  |        |                  |                 |                      |

### 1.4 DETAILED SIGNAL/PIN DESCRIPTIONS

This section describes all PC87427 signals.

#### 1.4.1 LPC Interface

| Signal              | Pin(s)  | I/O | Buffer Type                          | Power Well      | Description  |
|---------------------|---------|-----|--------------------------------------|-----------------|--|
| LAD3-0 <sup>1</sup> | 110-113 | I/O | IN <sub>PCI</sub> /O <sub>PCI</sub>  | V <sub>DD</sub> | <b>LPC Address-Data.</b> Multiplexed command, address bidirectional data, and cycle status.  |
| LCLK <sup>1</sup>   | 114     | I   | IN <sub>PCI</sub>                    | V <sub>DD</sub> | <b>LPC Clock.</b> Derived from the PCI clock (up to 33 MHz).   |
| LFRAME <sup>1</sup> | 117     | I   | IN <sub>PCI</sub>                    | V <sub>DD</sub> | <b>LPC Frame.</b> Low pulse indicates the beginning of a new LPC cycle or termination of a broken cycle.                                     |
| LDRQ <sup>1</sup>   | 118     | O   | O <sub>PCI</sub>                     | V <sub>DD</sub> | <b>LPC DMA Request.</b> Encoded DMA request for LPC Interface.   |
| LRESET <sup>1</sup> | 120     | I   | IN <sub>PCI</sub>                    | V <sub>DD</sub> | <b>LPC Reset.</b> Derived from the PCI system reset.   |
| SERIRQ <sup>1</sup> | 119     | I/O | IN <sub>PCI</sub> /O <sub>PCI</sub>  | V <sub>DD</sub> | <b>Serial IRQ.</b> The interrupt requests are serialized over a single pin, where each IRQ level is delivered during a designated time slot. |
| CLKRUN <sup>1</sup> | 124     | I/O | IN <sub>PCI</sub> /OD <sub>PCI</sub> | V <sub>DD</sub> | <b>Clock Run.</b> Indicates that LCLK is going to be stopped and requests full-speed LCLK (same behavior as PCI CLKRUN).                     |

1. This pin is neither 5-Volt tolerant nor back-drive protected.

#### 1.4.2 SMBus (SMB) Interface

| Signal   | Pin(s) | I/O | Buffer Type                       | Power Well      | Description   |
|----------|--------|-----|-----------------------------------|-----------------|---|
| SMBCLK   | 47     | I/O | IN <sub>SM</sub> /OD <sub>6</sub> | V <sub>SB</sub> | <b>SMBus Clock.</b> An internal pull-up for this pin is optional.                       |
| SMBDAT   | 46     | I/O | IN <sub>SM</sub> /OD <sub>6</sub> | V <sub>SB</sub> | <b>SMBus Serial Data.</b> An internal pull-up for this pin is optional.                 |
| SMBALERT | 35     | O   | OD <sub>6</sub>                   | V <sub>SB</sub> | <b>SMBus Alert.</b> SMBus Interrupt line. An internal pull-up for this pin is optional. |

## 1.0 Signal/Pin Connection and Description (Continued)

### 1.4.3 X-Bus Extension

| Signal   | Pin(s)   | I/O | Buffer Type       | Power Well | Description  |
|--|--|-----|-------------------|------------|--|
| $\overline{\text{XRD\_XEN}}$                       | 14   | O   | $O_{6/12}$        | $V_{SB}$   | <b>Read.</b> Active (low) level indicates a read cycle on the X-Bus.<br><b>Enable.</b> Active (high) level indicates valid data on the X-Bus.  |
| $\overline{\text{XWR\_XRW}}$                       | 15   | O   | $O_{14/14}$       | $V_{SB}$   | <b>Write.</b> Active (low) level indicates a write cycle on the X-Bus.<br><b>Read/Write.</b> A high level indicates a read cycle on the X-Bus; a low level indicates a write cycle on the X-Bus.                               |
| XA19_XD15<br>-XA12_XD8<br><br>XA11_XD7<br>-XA4_XD0 | 1-8,<br><br>24-31  | I/O | $IN_{TS}/O_{4/8}$ | $V_{SB}$   | <b>Multiplexed Data/Address Bus Lines.</b> The XA11-4 address lines are multiplexed with the 8-bit data lines XD7-XD0. If the 16-bit data bus is selected, the XA19-12 address lines are multiplexed with data lines XD15-XD8. |
| XA11-1,<br><br><br><br>XA0_XA20                    | 83, 82,<br>55, 50,<br>48, 37,<br>21, 22,<br>16-18,<br>19 | O   | $O_{3/6}$         | $V_{SB}$   | <b>Non-Multiplexed Address Bus Lines.</b> The XA0 address line pin is the XA20 address line for $\overline{\text{XCSn}}$ configured to 16-bit data bus.  |
| $\overline{\text{XSTB2-0}}$                        | 53,<br>33-34   | O   | $O_{3/6}$         | $V_{SB}$   | <b>Address Strokes.</b> Controls the strobe of up to three external latches for the multiplexed address lines.   |
| $\overline{\text{XCS3-0}}$                         | 85-87,<br>23   | O   | $O_{14/14}$       | $V_{SB}$   | <b>Chip Selects.</b> Controls the selection of up to four devices residing on the X-Bus.   |
| XRDY   | 9  | I   | $IN_{TS}$         | $V_{SB}$   | <b>I/O Ready.</b> Instructs the PC87427 to extend the access cycle.  |
| $\overline{\text{XIRQ2-0}}$                        | 36-35,<br>10   | I   | $IN_{TS}$         | $V_{SB}$   | <b>X-Bus Interrupt.</b> Converted into serial interrupt by the Interrupt Serializer. The system configuration includes the interrupt number associated with this signal.   |
| BIOS_SEL   | 52   | O   | $O_{3/6}$         | $V_{SB}$   | <b>BIOS Select.</b> BIOS image selections.   |

### 1.4.4 Serial Port Interfaces (SI1, SI2 and SIM)

| Signal   | Pin(s)    | I/O   | Buffer Type | Power Well | Description   |
|--|-----------|-------|-------------|------------|---|
| $\overline{\text{CTS1}}$                             | 99        | I     | $IN_{TS}$   | $V_{DD}$   | <b>Clear to Send.</b> When low, indicates that the modem or other data transfer device is ready to exchange data.                   |
| $\overline{\text{CTS2}}$<br>$\overline{\text{CTSM}}$ | 107<br>87 |       |             | $V_{SB}$   |   |
| $\overline{\text{DCD1}}$                             | 94        | I     | $IN_{TS}$   | $V_{DD}$   | <b>Data Carrier Detected.</b> When low, indicates that the data transfer device, e.g., modem, has detected the data carrier.        |
| $\overline{\text{DCD2}}$                             | 109       |       |             | $V_{SB}$   |   |
| $\overline{\text{DCDM}}$                             | 85        | $O^1$ | $O_{14/14}$ | $V_{SB}$   |   |
| $\overline{\text{DSR1}}$                             | 95        | I     | $IN_{TS}$   | $V_{DD}$   | <b>Data Set Ready.</b> When low, indicates that the data transfer device, e.g., modem, is ready to establish a communications link. |
| $\overline{\text{DSR2}}$<br>$\overline{\text{DSRM}}$ | 103<br>86 |       |             | $V_{SB}$   |   |

## 1.0 Signal/Pin Connection and Description (Continued)

| Signal         | Pin(s)    | I/O | Buffer Type      | Power Well      | Description  |
|----------------|-----------|-----|------------------|-----------------|--|
| DTR1_ BOUT1    | 100       | O   | O <sub>4/8</sub> | V <sub>DD</sub> | <b>Data Terminal Ready.</b> When low, indicates to the data transfer device, e.g., modem, that the UART is ready to establish a communications link. After a system reset, these pins provide the DTR function and set these signals to inactive high. Loopback operation holds them inactive.<br><b>Baud Output.</b> Provides the associated serial channel baud rate generator output signal if Test mode is selected, i.e., bit 7 of EXCR1 register is set. |
| DTR2_ BOUT2    | 108       |     |                  | V <sub>SB</sub> |  |
| DTRM_ BOUTM    | 88        |     |                  |                 |  |
| RI1            | 101       | I   | IN <sub>TS</sub> | V <sub>DD</sub> | <b>Ring Indicator.</b> When low, indicates that a telephone ring signal was received by the modem. These pins are monitored during V <sub>DD</sub> power-off for wake-up event detection.  |
| RI2            | 102       |     |                  | V <sub>SB</sub> |  |
| RTS1           | 97        | O   | O <sub>3/6</sub> | V <sub>DD</sub> | <b>Request to Send.</b> When low, indicates to the modem or other data transfer device that the corresponding UART is ready to exchange data. A system reset sets these signals to inactive high, and loopback operation holds them inactive.  |
| RTS2<br>RTSM   | 105<br>91 |     |                  | V <sub>SB</sub> |  |
| SIN1           | 96        | I   | IN <sub>TS</sub> | V <sub>DD</sub> | <b>Serial Input.</b> Receives composite serial data from the communications link (peripheral device, modem or other data transfer device).   |
| SIN2<br>SINM   | 104<br>90 |     |                  | V <sub>SB</sub> |  |
| SOUT1          | 98        | O   | O <sub>3/6</sub> | V <sub>DD</sub> | <b>Serial Output.</b> Sends composite serial data to the communications link (peripheral device, modem or other data transfer device). These signals are set active high after a system reset.   |
| SOUT2<br>SOUTM | 106<br>89 |     |                  | V <sub>SB</sub> |  |

1. DCDM is an output signal due to its role in an exchange connection with an external BMC.

### 1.4.5 Fan Monitor & Control (FMC)

| Signal   | Pin(s)                                 | I/O | Buffer Type                          | Power Well      | Description   |
|----------|--|-----|--------------------------------------|-----------------|---|
| FANIN0-7 | 66, 81,<br>77, 76,<br>75, 83,<br>36, 9 | I   | IN <sub>TS</sub>                     | V <sub>DD</sub> | <b>Fan Inputs.</b> Used to feed the fan's tachometer pulse to the Fan Speed Monitor.  |
| FANOUT0  | 78                                     | O   | OD <sub>12</sub> , O <sub>6/12</sub> | V <sub>DD</sub> | <b>Fan Outputs.</b> Pulse Width Modulation (PWM) signals, used to control the speed of cooling fans by controlling the voltage supplied to the fans motors. |
| FANOUT1  | 7<br>53                                |     |                                      |                 |   |
| FANOUT2  | 8<br>33                                |     |                                      |                 |   |
| FANOUT3  | 67                                     |     |                                      |                 |   |

## 1.0 Signal/Pin Connection and Description (Continued)

### 1.4.6 Health Monitoring & Control (HMC)

| Signal      | Pin(s) | I/O | Buffer Type                       | Power Well      | Description   |
|-------------|--------|-----|-----------------------------------|-----------------|---|
| LMPCIF      | 82     | I/O | IN <sub>SM</sub> /OD <sub>6</sub> | V <sub>SB</sub> | <b>LMPC Sensor Interface.</b> Bidirectional, SensortPath proprietary interface signal to LMPC sensor device(s). An internal pull-up for this pin is optional. |
| THRMTRIP1-2 | 21, 22 | I   | IN <sub>TS</sub>                  | V <sub>DD</sub> | <b>Thermal Trip Inputs.</b> Indicates that a thermal trip from a CPU occurred.  |
| VRMTHRM     | 83     | I   | IN <sub>TS</sub>                  | V <sub>DD</sub> | <b>VRM Thermal Warning.</b> Thermal warning from a VRM of a CPU.  |

### 1.4.7 Keyboard and Mouse Controller (KBC)

| Signal   | Pin(s) | I/O | Buffer Type  | Power Well      | Description   |
|----------|--------|-----|--|-----------------|---|
| KBCLK    | 125    | I/O | IN <sub>TS</sub> /OD <sub>14</sub>                     | V <sub>DD</sub> | <b>Keyboard Clock.</b> Keyboard clock signal. An external pull-up resistor is required for PS/2 compliance. This pin is monitored during V <sub>DD</sub> power-off for wake-up event detection. |
| KBDAT    | 126    | I/O | IN <sub>TS</sub> /OD <sub>14</sub>                     | V <sub>DD</sub> | <b>Keyboard Data.</b> Keyboard data signal. An external pull-up resistor is required for PS/2 compliance. This pin is monitored during V <sub>DD</sub> power-off for wake-up event detection.   |
| MCLK     | 127    | I/O | IN <sub>TS</sub> /OD <sub>14</sub>                     | V <sub>DD</sub> | <b>Mouse Clock.</b> Mouse clock signal. An external pull-up resistor is required for PS/2 compliance. This pin is monitored during V <sub>DD</sub> power-off for wake-up event detection.       |
| MDAT     | 128    | I/O | IN <sub>TS</sub> /OD <sub>14</sub>                     | V <sub>DD</sub> | <b>Mouse Data.</b> Mouse data signal. An external pull-up resistor is required for PS/2 compliance. This pin is monitored during V <sub>DD</sub> power-off for wake-up event detection.         |
| KBRST    | 122    | I/O | IN <sub>T</sub> /OD <sub>8</sub> ,<br>O <sub>4/8</sub> | V <sub>DD</sub> | <b>KBD Reset.</b> Keyboard reset (P20) quasi-bidirectional signal.  |
| GA20     | 123    | I/O | IN <sub>T</sub> /OD <sub>8</sub> ,<br>O <sub>4/8</sub> | V <sub>DD</sub> | <b>Gate A20.</b> KBC gate A20 (P21) quasi-bidirectional signal.   |
| P12      | 121    | I/O | IN <sub>T</sub> /OD <sub>8</sub> ,<br>O <sub>4/8</sub> | V <sub>DD</sub> | <b>I/O Port.</b> KBC quasi-bidirectional signal for general-purpose input and output (controlled by KBC firmware).  |
| P16, P17 | 75, 66 | I/O | IN <sub>T</sub> /OD <sub>8</sub> ,<br>O <sub>4/8</sub> | V <sub>DD</sub> | <b>I/O Port.</b> KBC quasi-bidirectional signal for general-purpose input and output (controlled by KBC firmware).  |

## 1.0 Signal/Pin Connection and Description (Continued)

### 1.4.8 General-Purpose I/O (GPIO)

| Signal                 | Pin(s)               | I/O | Buffer Type                          | Power Well      | Description  |  |
|------------------------|----------------------|-----|--------------------------------------|-----------------|--|--|
| GPIO00                 | 124                  | I/O | IN <sub>PCI</sub> /O <sub>PCI</sub>  | V <sub>SB</sub> | <p><b>General-Purpose I/O Ports.</b> Each pin is configured independently as input or I/O with or without static pull-up and with either open-drain or push-pull output type. The GPIOE<math>nn</math> pins have event detection capability.</p> |  |
| GPIO01-04              | 125-128              | I/O | IN <sub>TS</sub> /O <sub>14/14</sub> | V <sub>SB</sub> |  |  |
| GPIO05                 | 82                   | I/O | IN <sub>TS</sub> /O <sub>3/6</sub>   | V <sub>SB</sub> |  |  |
| GPIO06                 | 10                   | I/O | IN <sub>TS</sub> /O <sub>3/6</sub>   | V <sub>SB</sub> |  |  |
| GPIO07                 | 13                   | I/O | IN <sub>TS</sub> /O <sub>14/14</sub> | V <sub>SB</sub> |  |  |
| GPIOE10,<br>GPIOE12-15 | 1, 3-6               | I/O | IN <sub>TS</sub> /O <sub>3/6</sub>   | V <sub>SB</sub> |  |  |
|                        | 109,<br>106-103      |     | IN <sub>TS</sub> /O <sub>14/14</sub> |                 |  |  |
| GPIOE11                | 2                    | I/O | IN <sub>TS</sub> /O <sub>3/6</sub>   | V <sub>SB</sub> |  |  |
|                        | 107                  |     | IN <sub>TS</sub> /O <sub>3/6</sub>   |                 |  |  |
| GPIOE16-17             | 7-8                  | I/O | IN <sub>TS</sub> /O <sub>3/6</sub>   | V <sub>SB</sub> |  |  |
| GPIO20                 | 14                   | I/O | IN <sub>TS</sub> /O <sub>6/12</sub>  | V <sub>SB</sub> |  |  |
| GPIO21                 | 15                   | I/O | IN <sub>TS</sub> /O <sub>14/14</sub> | V <sub>SB</sub> |  |  |
| GPIO22-23              | 16-17                | I/O | IN <sub>TS</sub> /O <sub>3/6</sub>   | V <sub>SB</sub> |  |  |
| GPO24                  | 18                   | O   | O <sub>3/6</sub>                     | V <sub>SB</sub> |  | <b>General-Purpose Output Port.</b>  |
| GPIO25-27              | 19, 83, 37           | I/O | IN <sub>TS</sub> /O <sub>3/6</sub>   | V <sub>SB</sub> |  | <p><b>General-Purpose I/O Ports.</b> Each pin is configured independently as input or I/O with or without static pull-up and with either open-drain or push-pull output type. The GPIOE<math>nn</math> pins have event detection capability.</p> |
| GPIO37,35-31           | 31,29-25             | I/O | IN <sub>TS</sub> /O <sub>4/8</sub>   | V <sub>SB</sub> |  |  |
|                        | 71, 73-<br>74, 64-62 |     | IN <sub>TS</sub> /O <sub>6/12</sub>  | V <sub>DD</sub> |  |  |
| GPIO36,30              | 30, 24               | I/O | IN <sub>TS</sub> /O <sub>4/8</sub>   | V <sub>SB</sub> |  |  |
|                        | 72, 61               |     | IN <sub>TS</sub> /O <sub>3/6</sub>   | V <sub>DD</sub> |  |  |
| GPIOE40-44             | 21-22,<br>35, 49, 38 | I/O | IN <sub>TS</sub> /O <sub>3/6</sub>   | V <sub>SB</sub> |  |  |
| GPIOE45                | 51                   | I/O | IN <sub>TS</sub> /O <sub>14/14</sub> | V <sub>SB</sub> |  |  |
| GPIOE46-47             | 20, 32               | I/O | IN <sub>TS</sub> /O <sub>3/6</sub>   | V <sub>SB</sub> |  |  |
| GPIO50-52              | 85-87                | I/O | IN <sub>TS</sub> /O <sub>14/14</sub> | V <sub>SB</sub> |  |  |
| GPO53                  | 91                   | O   | O <sub>3/6</sub>                     | V <sub>SB</sub> | <b>General-Purpose Output Port.</b>  |  |
| GPIO54                 | 90                   | I/O | IN <sub>TS</sub> /O <sub>3/6</sub>   | V <sub>SB</sub> | <b>General-Purpose I/O Port.</b> The pin is configured independently as input or I/O with or without static pull-up and with either open-drain or push-pull output type.   |  |
| GPO55                  | 89                   | O   | O <sub>3/6</sub>                     | V <sub>SB</sub> | <b>General-Purpose Output Port.</b>  |  |
| GPIO56-57              | 80-79                | I/O | IN <sub>TS</sub> /O <sub>14/14</sub> | V <sub>SB</sub> | <b>General-Purpose I/O Ports.</b> Each pin is configured independently as input or I/O with or without static pull-up and with either open-drain or push-pull output type. The GPIOE $nn$ pins have event detection capability.                  |  |

## 1.0 Signal/Pin Connection and Description (Continued)

| Signal   | Pin(s)          | I/O | Buffer Type                          | Power Well      | Description                                   |
|----------|-----------------|-----|--------------------------------------|-----------------|---|
| GPO60-63 | 54,48,<br>45,55 | O   | O <sub>3/6</sub>                     | V <sub>SB</sub> | <b>General-Purpose Output Ports.</b>          |
| GPEXD    | 79              | I/O | IN <sub>TS</sub> /O <sub>14/14</sub> | V <sub>SB</sub> | <b>General-Purpose I/O Extension Data.</b>    |
| GPEXC    | 80              | O   | O <sub>14/14</sub>                   | V <sub>SB</sub> | <b>General-Purpose I/O Extension Clock.</b>   |
| GPEXC2   | 81              | O   | O <sub>14/14</sub>                   | V <sub>SB</sub> | <b>General-Purpose I/O Extension Clock 2.</b> |

### 1.4.9 Floppy Disk Controller (FDC)

| Signal | Pin(s) | I/O | Buffer Type                         | Power Well      | Description  |
|--------|--------|-----|-------------------------------------|-----------------|--|
| DENSEL | 74     | O   | OD <sub>12</sub> ,O <sub>6/12</sub> | V <sub>DD</sub> | <b>Density Select.</b> Indicates that either a high FDC density data rate (500 Kbps, 1 Mbps or 2 Mbps) or a low density data rate (250 or 300 Kbps) is selected. |
| DIR    | 65     | O   | OD <sub>12</sub> ,O <sub>6/12</sub> | V <sub>DD</sub> | <b>Direction.</b> Determines the direction of the Floppy Disk Drive (FDD) head movement (active = step in; inactive = step out) during a seek operation.         |
| DR0    | 67     | O   | OD <sub>12</sub> ,O <sub>6/12</sub> | V <sub>DD</sub> | <b>Drive Select.</b> Controlled by bit 0 of the Digital Output Register (DOR).   |
| DRATE0 | 73     | O   | OD <sub>12</sub> ,O <sub>6/12</sub> | V <sub>DD</sub> | <b>Data Rate.</b> Reflects the value of bit 0 of the Configuration Control Register (CCR) or the Data Rate Select Register (DSR), whichever was written to last. |
| DSKCHG | 57     | I   | IN <sub>TS</sub>                    | V <sub>DD</sub> | <b>Disk Change.</b> Indicates if the drive door was opened.  |
| HDSEL  | 58     | O   | OD <sub>12</sub> ,O <sub>6/12</sub> | V <sub>DD</sub> | <b>Head Select.</b> Determines which side of the FDD is accessed. Active low selects side 1; inactive selects side 0.  |
| INDEX  | 72     | I   | IN <sub>TS</sub>                    | V <sub>DD</sub> | <b>Index.</b> Indicates the beginning of an FDD track.   |
| MSEN0  | 45     | I   | IN <sub>TS</sub>                    | V <sub>DD</sub> | <b>Automatic Media Sense.</b> Identifies the media type of the floppy disk in drives 1 and 0 (if the drives support this protocol).                              |
| MTR0   | 71     | O   | OD <sub>12</sub> ,O <sub>6/12</sub> | V <sub>DD</sub> | <b>Motor Select.</b> Motor enable lines for drives 0.  |
| RDATA  | 59     | I   | IN <sub>TS</sub>                    | V <sub>DD</sub> | <b>Read Data.</b> Raw serial input data stream read from the FDD.  |
| STEP   | 64     | O   | OD <sub>12</sub> ,O <sub>6/12</sub> | V <sub>DD</sub> | <b>Step.</b> Sends pulses to the disk drive at a software programmable rate to move the head during a seek operation.  |
| TRK0   | 61     | I   | IN <sub>TS</sub>                    | V <sub>DD</sub> | <b>Track 0.</b> Indicates to the controller that the head of the selected floppy disk drive is at track 0.   |
| WDATA  | 63     | O   | OD <sub>12</sub> ,O <sub>6/12</sub> | V <sub>DD</sub> | <b>Write Data.</b> Carries out the pre-compensated serial data that is written to the FDD. Pre-compensation is software selectable.                              |
| WGATE  | 62     | O   | OD <sub>12</sub> ,O <sub>6/12</sub> | V <sub>DD</sub> | <b>Write Gate.</b> Enables the write circuitry of the selected FDD.  |
| WP     | 60     | I   | IN <sub>TS</sub>                    | V <sub>DD</sub> | <b>Write Protected.</b> Indicates that the disk in the selected drive is write protected.  |

## 1.0 Signal/Pin Connection and Description (Continued)

### 1.4.10 System Wake-Up Control (SWC)

| Signal   | Pin(s)                        | I/O   | Buffer Type        | Power Well                   | Description   |                           |                           |               |   |   |   |   |   |                |   |   |                       |   |   |                     |
|--|-------------------------------|---|--------------------|------------------------------|---|---------------------------|---------------------------|---------------|---|---|---|---|---|----------------|---|---|-----------------------|---|---|---------------------|
| GPIOE17-16   | 8-7                           | I   | IN <sub>TS</sub>   | V <sub>SB</sub>              | <b>Wake-up Inputs.</b> Generate a wake-up event or an interrupt. These pins have programmable debounce protection.  |                           |                           |               |   |   |   |   |   |                |   |   |                       |   |   |                     |
| GPIOE15-10   | 103-107, 109                  |   |                    |                              |   |                           |                           |               |   |   |   |   |   |                |   |   |                       |   |   |                     |
| GPIOE11-10   | 2-1                           |   |                    |                              |   |                           |                           |               |   |   |   |   |   |                |   |   |                       |   |   |                     |
| GPIOE40-47   | 21-22, 35, 49, 38, 51, 20, 32 |   |                    |                              |   |                           |                           |               |   |   |   |   |   |                |   |   |                       |   |   |                     |
| $\overline{\text{RI1}}$<br>RI2                           | 101<br>102                    | I   | IN <sub>TS</sub>   | V <sub>SB</sub>              | <b>Ring Indicator Wake-up.</b> When low, generates a wake-up event or an interrupt, indicating that a telephone ring signal was received by the modem. When $\overline{\text{RI}}$ functionality is not required, an internal pull-up resistor allows this pin to be left floating.   |                           |                           |               |   |   |   |   |   |                |   |   |                       |   |   |                     |
| KBCLK  | 125                           | I   | IN <sub>TS</sub>   | V <sub>SB</sub>              | <b>Keyboard Clock Wake-up.</b> Generates a wake-up event or an interrupt, indicating a change in the keyboard clock signal.   |                           |                           |               |   |   |   |   |   |                |   |   |                       |   |   |                     |
| KBDAT  | 126                           | I   | IN <sub>TS</sub>   | V <sub>SB</sub>              | <b>Keyboard Data Wake-up.</b> Generates a wake-up event or an interrupt, indicating a change in the keyboard data signal.   |                           |                           |               |   |   |   |   |   |                |   |   |                       |   |   |                     |
| MCLK   | 127                           | I   | IN <sub>TS</sub>   | V <sub>SB</sub>              | <b>Mouse Clock Wake-up.</b> Generates a wake-up event or an interrupt, indicating a change in the mouse clock signal.   |                           |                           |               |   |   |   |   |   |                |   |   |                       |   |   |                     |
| MDAT   | 128                           | I   | IN <sub>TS</sub>   | V <sub>SB</sub>              | <b>Mouse Data Wake-up.</b> Generates a wake-up event or an interrupt, indicating a change in the mouse data signal.   |                           |                           |               |   |   |   |   |   |                |   |   |                       |   |   |                     |
| $\overline{\text{PWBTIN}}$                               | 36                            | I   | IN <sub>TS</sub>   | V <sub>SB</sub>              | <b>Power Button In.</b> Active (low) level indicates a user request to turn the power on or off. This pin has debounce protection.  |                           |                           |               |   |   |   |   |   |                |   |   |                       |   |   |                     |
| $\overline{\text{PWBTOUT}}$                              | 49                            | O   | OD <sub>6</sub>    | V <sub>SB</sub>              | <b>Power Button Out.</b> Output for the chip-set Power Button input.  |                           |                           |               |   |   |   |   |   |                |   |   |                       |   |   |                     |
| $\overline{\text{SLBTIN}}$                               | 35                            | I   | IN <sub>TS</sub>   | V <sub>SB</sub>              | <b>Sleep Button In.</b> Active (low) level indicates a user request to enter or exit Sleep mode. This pin has debounce protection.  |                           |                           |               |   |   |   |   |   |                |   |   |                       |   |   |                     |
| $\overline{\text{SLPS3}}$ ,<br>$\overline{\text{SLPS5}}$ | 20<br>32                      | I   | IN <sub>TS</sub>   | V <sub>SB</sub>              | <p><b>Sleep State 3 to 5.</b> Active (low) level indicates the system is in one of the sleep states S3, S4 or S5. These signals are generated by an external ACPI controller.</p> <p><b>Pins</b></p> <table border="1"> <thead> <tr> <th><math>\overline{\text{SLPS3}}</math></th> <th><math>\overline{\text{SLPS5}}</math></th> <th>Functionality</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>Working state (S0) or sleep states S1 or S2</td> </tr> <tr> <td>0</td> <td>1</td> <td>Sleep state S3</td> </tr> <tr> <td>0</td> <td>0</td> <td>Sleep states S4 or S5</td> </tr> <tr> <td>1</td> <td>0</td> <td>Illegal combination</td> </tr> </tbody> </table> | $\overline{\text{SLPS3}}$ | $\overline{\text{SLPS5}}$ | Functionality | 1 | 1 | Working state (S0) or sleep states S1 or S2 | 0 | 1 | Sleep state S3 | 0 | 0 | Sleep states S4 or S5 | 1 | 0 | Illegal combination |
| $\overline{\text{SLPS3}}$                                | $\overline{\text{SLPS5}}$     | Functionality                               |                    |                              |   |                           |                           |               |   |   |   |   |   |                |   |   |                       |   |   |                     |
| 1  | 1                             | Working state (S0) or sleep states S1 or S2 |                    |                              |   |                           |                           |               |   |   |   |   |   |                |   |   |                       |   |   |                     |
| 0  | 1                             | Sleep state S3                              |                    |                              |   |                           |                           |               |   |   |   |   |   |                |   |   |                       |   |   |                     |
| 0  | 0                             | Sleep states S4 or S5                       |                    |                              |   |                           |                           |               |   |   |   |   |   |                |   |   |                       |   |   |                     |
| 1  | 0                             | Illegal combination                         |                    |                              |   |                           |                           |               |   |   |   |   |   |                |   |   |                       |   |   |                     |
| $\overline{\text{SIOSCI}}$                               | 38                            | O   | OD <sub>6</sub>    | V <sub>SB</sub>              | <b>System Control Interrupt.</b> Active (low) level indicates that a wake-up event occurred, causing the system to exit its current sleep state.  |                           |                           |               |   |   |   |   |   |                |   |   |                       |   |   |                     |
| $\overline{\text{SIOSMI}}$                               | 37                            | O   | OD <sub>6</sub>    | V <sub>SB</sub>              | <b>System Management Interrupt.</b> Active (low) level indicates that an SMI occurred.  |                           |                           |               |   |   |   |   |   |                |   |   |                       |   |   |                     |
| $\overline{\text{ONCTL}}$                                | 39                            | O   | OD <sub>6</sub>    | V <sub>SB</sub>              | <b>Power Supply On/Off Control.</b> Active level (low) indicates that the power should be turned on. An external pull-up resistor is required   |                           |                           |               |   |   |   |   |   |                |   |   |                       |   |   |                     |
| LED1, LED2   | 50, 51                        | O   | O <sub>14/14</sub> | V <sub>SB</sub>              | <b>LED Drives.</b> These outputs can be connected directly to LED devices. They can be configured, with programmable blink rate for all LEDs, as one dual-colored LED or two single-colored LEDs.   |                           |                           |               |   |   |   |   |   |                |   |   |                       |   |   |                     |
| CHASSIS  | 84                            | I   | IN <sub>CS</sub>   | V <sub>PP</sub> <sup>1</sup> | <b>Chassis Intrusion Input.</b> Any change of this pin sets the intrusion detection. For correct operation, this pin must be tied to V <sub>SS</sub> when it is not used.   |                           |                           |               |   |   |   |   |   |                |   |   |                       |   |   |                     |

1. Internal V<sub>PP</sub> is based on V<sub>SB</sub> and V<sub>BAT</sub>.

## 1.0 Signal/Pin Connection and Description (Continued)

### 1.4.11 Watchdog

| Signal | Pin(s) | I/O | Buffer Type      | Power Well      | Description   |
|--------|--------|-----|------------------|-----------------|---|
| WDO    | 54     | O   | O <sub>3/6</sub> | V <sub>SB</sub> | <b>Watchdog Out.</b> An active pulse (low) of a fixed width; it is generated when a watchdog time-out occurs. |

### 1.4.12 Clocks

| Signal                      | Pin(s) | I/O | Buffer Type        | Power Well                   | Description   |
|-----------------------------|--------|-----|--------------------|------------------------------|---|
| 32KX1_32KCLKIN <sup>1</sup> | 42     | I   | IN <sub>OSC</sub>  | V <sub>PP</sub>              | <b>32.768 KHz Crystal Input.</b> Input from external crystal oscillator circuitry.<br><b>32.768 KHz Clock Oscillator Input.</b> Input from external clock oscillator device. <sup>2</sup> |
| 32KX2 <sup>3</sup>          | 44     | O   | O <sub>OSC</sub>   | V <sub>PP</sub>              | <b>32.768 KHz Crystal Oscillator Output.</b> Output to external crystal oscillator circuitry.   |
| LFCKOUT                     | 45     | O   | O <sub>3/6</sub>   | V <sub>SB</sub>              | <b>Low Frequency Clock Output.</b> The Real-Time Clock frequency (32.768 KHz), or a 1 Hz clock output.  |
| CLKIN                       | 56     | I   | IN <sub>TS</sub>   | V <sub>SB</sub> <sup>4</sup> | <b>Clock Input.</b> 48 MHz for the Legacy functions, or no input clock.   |
| HFCKOUT                     | 13     | O   | O <sub>14/14</sub> | V <sub>SB</sub>              | <b>High Frequency Clock Output.</b> Clock output for system use.  |

1. This pin is not 5-volt tolerant.
2. If the input clock is in TRI-STATE while V<sub>SB</sub> is off, it is recommended to connect an external 10 KΩ pull-down resistor to this pin.
3. This pin is neither 5-volt tolerant nor back-drive protected.
4. The CLKIN signal source can be V<sub>DD</sub> powered.

### 1.4.13 Configuration Straps

**Note:** All external pull-down resistors must be connected to V<sub>SS</sub>.

| Signal | Pin(s) | I/O | Buffer Type      | Power Well      | Description  |
|--------|--------|-----|------------------|-----------------|--|
| BADDR  | 100    | I   | IN <sub>TS</sub> | V <sub>DD</sub> | <b>Base Address.</b> Sampled at V <sub>DD</sub> Power-Up reset to determine the base address of the configuration Index-Data register pair, as follows:<br>No pull-down resistor: 2Eh-2Fh<br>10 KΩ <sup>1</sup> external pull-down resistor: 4Eh-4Fh |
| TRIS   | 97     | I   | IN <sub>TS</sub> | V <sub>DD</sub> | <b>TRI-STATE Device.</b> Sampled at V <sub>DD</sub> Power-Up reset to force the device to float all its output and I/O pins, as follows:<br>No pull-down resistor: Pins active<br>10 KΩ <sup>1</sup> external pull-down resistor: Pins floating      |
| CKIN48 | 55     | I   | IN <sub>TS</sub> | V <sub>SB</sub> | <b>CLKIN 48 MHz.</b> Sampled at V <sub>SB</sub> Power-Up reset to determine the presence of the 48 MHz input clock at the CLKIN pin, as follows:<br>No pull-down resistor: No clock<br>10 KΩ external pull-down resistor: 48 MHz clock               |

## 1.0 Signal/Pin Connection and Description (Continued)

| Signal  | Pin(s)      | I/O | Buffer Type      | Power Well      | Description   |
|---------|-------------|-----|------------------|-----------------|---|
| HFCKS   | 88          | I   | IN <sub>TS</sub> | V <sub>SB</sub> | <p><b>High Frequency Clock Selection.</b> Sampled at V<sub>SB</sub> Power-Up reset to determine the high frequency clock selection, as follows:</p> <p>For <math>\overline{\text{CKIN48}}=0</math>:<br/>           No pull-down resistor: 40 MHz<br/>           10 K<math>\Omega</math><sup>1</sup> external pull-down resistor: 10 MHz</p> <p>For <math>\overline{\text{CKIN48}}=1</math>:<br/>           No pull-down resistor: 24 MHz<br/>           10 K<math>\Omega</math><sup>1</sup> external pull-down resistor: 6 MHz</p>  |
| XCNF2-0 | 91, 108, 34 | I   | IN <sub>TS</sub> | V <sub>SB</sub> | <p><b>X-Bus Default Configuration.</b> Sampled at V<sub>SB</sub> Power-Up reset to set the configuration of the X-Bus transactions.</p> <p><b>Pins</b><br/> <b>2 1 0 Functionality</b></p> <p>1 1 x: No BIOS<br/>           1 0 1: 16-bit data BIOS, XSTB0 only<br/>           1 0 0: 16-bit data BIOS, XSTB0 and XSTB1<br/>           0 1 1: 8-bit data BIOS, XA11-4 multiplexed, XRDY disabled<br/>           0 1 0: 8-bit data BIOS, XA11-4 multiplexed, XRDY enabled<br/>           0 0 1: 8-bit data BIOS, XA11-4 direct, XRDY disabled<br/>           0 0 0: 8-bit data BIOS, XA11-4 direct, XRDY enabled</p> <p>Pulled to 1 by internal resistor or set to 0 by external 10 K<math>\Omega</math><sup>1</sup> pull-down resistor.</p> |
| SMBSA   | 48          | I   | IN <sub>TS</sub> | V <sub>SB</sub> | <p><b>SMBus Slave Address.</b> Sampled at V<sub>SB</sub> Power-Up reset to determine the slave address of the device on SMBus, as follows</p> <p>No pull-down resistor: D8h, D9h<br/>           10 K<math>\Omega</math> external pull-down resistor: 60h, 61h</p>   |
| TEST    | 89          | I   | IN <sub>TS</sub> | V <sub>DD</sub> | <p><b>XOR Tree Test Mode.</b> Sampled at V<sub>DD</sub> Power-Up reset to force the device pins into a XOR tree configuration.</p> <p>No pull-down resistor (default): Normal device operation<br/>           10 K<math>\Omega</math><sup>1</sup> external pull-down resistor: Pins configured as XOR tree.</p> <p>When <math>\overline{\text{TEST}}</math> is set to 0 (by an external pull-down resistor), <math>\overline{\text{TRIS}}</math> must be 1 (left unconnected).</p>  |
| CTEST   | 52          | I   | IN <sub>TS</sub> | V <sub>SB</sub> | <p><b>Complementary Test Mode.</b> Sampled at V<sub>SB</sub> Power-Up reset to set the device to Test Mode</p> <p>No pull-down resistor: Normal Operation mode<br/>           10 K<math>\Omega</math> external pull-down resistor: Test Mode</p>  |

1. Because the strap function is multiplexed with the Serial Port pins, a CMOS transceiver device is recommended for Serial Port functionality; in this case, the value of the external pull-down resistor is 10 K $\Omega$ . If, however, a TTL transceiver device is used, the value of the external pull-down resistor must be 470 $\Omega$ , and since the Serial Port pins are not able to drive this load, the external pull-down resistor must be disconnected  $t_{\text{PLV}}$  after V<sub>DD</sub> power-up (see "Reset Timing" on page 27).

### 1.4.14 Testability

| Signal  | Pin(s) | I/O | Buffer Type      | Power Well      | Description   |
|---------|--------|-----|------------------|-----------------|---|
| XOR_OUT | 100    | O   | O <sub>4/8</sub> | V <sub>DD</sub> | <b>XOR Tree Output.</b> All the device pins (except power pins) are internally connected in a XOR tree structure. |

## 1.0 Signal/Pin Connection and Description (Continued)

### 1.4.15 Power and Ground

| Signal            | Pin(s)              | I/O | Buffer Type       | Description   |
|-------------------|---------------------|-----|-------------------|---|
| V <sub>SS</sub>   | 11, 43, 68, 93, 115 | I   | GND               | <b>Ground.</b> Serves for both on-chip logic, output drivers and back-up battery circuit.   |
| V <sub>DD</sub>   | 69, 116             | I   | PWR               | <b>Digital 3.3V Power Supply.</b> Serves as power supply for the legacy peripherals and the LPC Interface.  |
| V <sub>SB</sub>   | 12, 40, 92          | I   | PWR               | <b>Standby Digital 3.3V Power Supply.</b> Used for the SMBus and X-Bus interfaces, the GPIO ports and the clock generator. When active, it also powers the RTC and the SWC.   |
| V <sub>CORF</sub> | 70                  | I/O | PWR               | <b>On-Chip Core Power Converter Filter.</b> Used by the on-chip core power converter which powers the core logic of all the device modules. An external 1 $\mu$ F ceramic filter capacitor must be connected between this pin and V <sub>SS</sub> .               |
| V <sub>BAT</sub>  | 41                  | I   | IN <sub>ULR</sub> | <b>Battery Power Supply.</b> When V <sub>SB</sub> is off, this supply provides battery back-up to the SWC registers, the RTC and the 32 KHz crystal oscillator. The pin is connected to the internal logic through a series resistor for UL-compliant protection. |

## 1.5 INTERNAL PULL-UP AND PULL-DOWN RESISTORS

The signals listed in Table 3 have internal pull-up (PU) and/or pull-down (PD) resistors. The internal resistors are optional for those signals indicated as "Programmable". See Section 2.3 on page 25 for the values of each resistor type.

**Table 3. Internal Pull-Up and Pull-Down Resistors**

| Signal                                     | Pin(s)      | Power Well      | Type               | Comments                  |
|--|-------------|-----------------|--------------------|---------------------------|
| <b>Keyboard and Mouse Controller (KBC)</b> |             |                 |                    |                           |
| P12, P16, P17                              | 121, 75, 66 | V <sub>DD</sub> | PU <sub>30</sub>   |                           |
| <b>SMBus (SMB) Interface</b>               |             |                 |                    |                           |
| SMBCLK                                     | 47          | V <sub>SB</sub> | PU <sub>30</sub>   | Programmable <sup>1</sup> |
| SMBDAT                                     | 46          | V <sub>SB</sub> | PU <sub>30</sub>   | Programmable <sup>1</sup> |
| SMBALERT                                   | 35          | V <sub>SB</sub> | PU <sub>30</sub>   | Programmable <sup>1</sup> |
| <b>Health Monitoring and Control (HMC)</b> |             |                 |                    |                           |
| LMPCIF                                     | 82          | V <sub>SB</sub> | PU <sub>1K25</sub> | Programmable <sup>2</sup> |
| THRMTRIP1,<br>THRMTRIP2                    | 21,<br>22   | V <sub>DD</sub> | PU <sub>30</sub>   |                           |
| VRMTHRM                                    | 83          | V <sub>DD</sub> | PU <sub>30</sub>   |                           |
| <b>System Wake-Up Control (SWC)</b>        |             |                 |                    |                           |
| PWBTIN                                     | 36          | V <sub>SB</sub> | PU <sub>30</sub>   |                           |
| SLBTIN                                     | 35          | V <sub>SB</sub> | PU <sub>30</sub>   |                           |
| PWBTOUT                                    | 49          | V <sub>SB</sub> | PU <sub>30</sub>   | Note <sup>3</sup>         |
| SIOSMI                                     | 37          | V <sub>SB</sub> | PU <sub>30</sub>   |                           |
| SIOSCI                                     | 38          | V <sub>SB</sub> | PU <sub>30</sub>   |                           |

## 1.0 Signal/Pin Connection and Description (Continued)

**Table 3. Internal Pull-Up and Pull-Down Resistors (Continued)**

| Signal   | Pin(s)                        | Power Well           | Type               | Comments                      |
|--|-------------------------------|----------------------|--------------------|-------------------------------|
| $\overline{RI1}$                                 | 101                           | $V_{SB}$             | PU <sub>90</sub>   | Pin can be left Not Connected |
| $\overline{RI2}$                                 | 102                           | $V_{SB}$             | PU <sub>90</sub>   | Pin can be left Not Connected |
| <b>General-Purpose Input/Output (GPIO) Ports</b> |                               |                      |                    |                               |
| GPIO00-04, 06-07                                 | 124-128, 10, 13               | $V_{SB}$ or $V_{DD}$ | PU <sub>30</sub>   | Programmable                  |
| GPIO05   | 82                            | $V_{SB}$             | PU <sub>1K25</sub> | Programmable                  |
| GPIOE10-15                                       | 1-6                           | $V_{SB}$             | PU <sub>30</sub>   | Programmable                  |
|  | 109, 107-103                  |                      |                    |                               |
| GPIOE16-17                                       | 7, 8                          | $V_{SB}$             | PU <sub>30</sub>   | Programmable                  |
| GPIO20-27  | 14-19, 83, 37                 | $V_{SB}$             | PU <sub>30</sub>   | Programmable                  |
| GPIO30-37  | 61-64, 74, 73-71              | $V_{SB}$             | PU <sub>30</sub>   | Programmable                  |
| GPIOE40-47                                       | 21-22, 35, 49, 38, 51, 20, 32 | $V_{SB}$             | PU <sub>30</sub>   | Programmable                  |
| GPIO50-57  | 85-87, 91-89, 80-79           | $V_{SB}$             | PU <sub>30</sub>   | Programmable <sup>4</sup>     |
| GPO60-63   | 54, 48, 45, 55                | $V_{SB}$             | PU <sub>30</sub>   | Programmable                  |
| <b>Strap Configuration</b>                       |                               |                      |                    |                               |
| $\overline{BADDR}$                               | 100                           | $V_{DD}$             | PU <sub>30</sub>   | Strap <sup>5</sup>            |
| $\overline{TRIS}$                                | 97                            | $V_{DD}$             | PU <sub>30</sub>   | Strap <sup>5</sup>            |
| $\overline{CKIN48}$                              | 55                            | $V_{SB}$             | PU <sub>30</sub>   | Strap <sup>6</sup>            |
| $\overline{XCNF2-0}$                             | 91, 108, 34                   | $V_{SB}$             | PU <sub>30</sub>   | Strap <sup>6</sup>            |
| $\overline{SMBSA}$                               | 48                            | $V_{SB}$             | PU <sub>30</sub>   | Strap <sup>6</sup>            |
| $\overline{HFCKS}$                               | 88                            | $V_{SB}$             | PU <sub>30</sub>   | Strap <sup>6</sup>            |
| $\overline{TEST}$                                | 89                            | $V_{DD}$             | PU <sub>30</sub>   | Strap <sup>5</sup>            |
| $\overline{CTEST}$                               | 52                            | $V_{SB}$             | PU <sub>30</sub>   | Strap <sup>6</sup>            |

1. Default at reset: disabled.
2. Default at reset: enabled.
3. Disabled when  $V_{DD}$  is off.
4. Disabled during  $V_{SB}$  Power-Up reset.
5. Active only during  $V_{DD}$  Power-Up reset.
6. Active only during  $V_{SB}$  Power-Up reset.

## 2.0 Device Characteristics

### 2.1 GENERAL DC ELECTRICAL CHARACTERISTICS

#### 2.1.1 Recommended Operating Conditions

| Symbol           | Parameter                     | Min | Typ | Max | Unit |
|------------------|-------------------------------|-----|-----|-----|------|
| V <sub>DD</sub>  | Supply Voltage                | 3.0 | 3.3 | 3.6 | V    |
| V <sub>SB</sub>  | Standby Voltage               | 3.0 | 3.3 | 3.6 | V    |
| V <sub>BAT</sub> | Battery Backup Supply Voltage | 2.4 | 3.0 | 3.6 | V    |
| T <sub>A</sub>   | Operating Temperature         | 0   |     | +70 | °C   |

#### 2.1.2 Absolute Maximum Ratings

Absolute maximum ratings are values beyond which damage to the device may occur. Unless otherwise specified, all voltages are relative to ground.

| Symbol           | Parameter                            | Conditions  | Min               | Max                   | Unit |
|------------------|--------------------------------------|---|-------------------|-----------------------|------|
| V <sub>SUP</sub> | Supply Voltage <sup>1</sup>          |   | -0.5              | +4.1                  | V    |
| V <sub>I</sub>   | Input Voltage                        | All other pins  | -0.5              | 5.5                   | V    |
|                  |                                      | LCLK, LAD3-0, LFRAME, LRESET, SERIRQ, CLKRUN, 32KX1_32KCLKIN        | -0.5              | V <sub>DD</sub> + 0.5 | V    |
| V <sub>O</sub>   | Output Voltage                       | All other pins  | -0.5              | 5.5                   | V    |
|                  |                                      | LAD3-0, LDRQ, SERIRQ, CLKRUN, 32KX2                                 | -0.5              | V <sub>DD</sub> + 0.5 | V    |
| T <sub>STG</sub> | Storage Temperature                  |   | -65               | +165                  | °C   |
| P <sub>D</sub>   | Power Dissipation                    |   |                   | 1                     | W    |
| T <sub>L</sub>   | Lead Temperature Soldering (10 s)    |   |                   | +260                  | °C   |
|                  | ESD Tolerance                        | C <sub>ZAP</sub> = 100 pF<br>R <sub>ZAP</sub> = 1.5 KΩ <sup>2</sup> | 2000              |                       | V    |
| MCRS             | Battery Maximum Safe Reverse Current | V <sub>SB</sub> = 3.63V<br>R <sub>UL</sub> <sup>3</sup> = 1.6KΩ     | 2.27 <sup>4</sup> |                       | mA   |

1. V<sub>SUP</sub> is V<sub>DD</sub>, V<sub>SB</sub> or V<sub>BAT</sub>.

2. Value based on test complying with RAI-5-048-RA human body model ESD testing.

3. Minimum value of internal protection resistor.

4. For batteries with lower MCRS it is necessary to connect a series resistor between the battery and VBAT pin, with resistance:  $R = (3.63V/MCRS) - 1.6 K\Omega$ .

## 2.0 Device Characteristics (Continued)

### 2.1.3 Capacitance

| Symbol           | Parameter                            | Min <sup>2</sup> | Typ <sup>1</sup> | Max <sup>2</sup> | Unit |
|------------------|--------------------------------------|------------------|------------------|------------------|------|
| C <sub>IN</sub>  | Input Pin Capacitance                |                  | 4                | 5                | pF   |
| C <sub>IN1</sub> | Clock Input Capacitance <sup>3</sup> | 5                | 8                | 12               | pF   |
| C <sub>IO</sub>  | I/O Pin Capacitance                  |                  | 8                | 10               | pF   |
| C <sub>O</sub>   | Output Pin Capacitance               |                  | 6                | 8                | pF   |

1. T<sub>A</sub> = 25°C, f = 1 MHz.

2. Not tested. Guaranteed by characterization.

3. LCLK, CLKIN.

### 2.1.4 Power Consumption under Recommended Operating Conditions

| Symbol           | Parameter  | Conditions <sup>1</sup>  | Typ | Max | Unit |
|------------------|--|--|-----|-----|------|
| I <sub>DD</sub>  | V <sub>DD</sub> Average Main Supply Current                                  | V <sub>IL</sub> = 0.5V, V <sub>IH</sub> = 2.4V<br>No Load                        | 14  | 20  | mA   |
| I <sub>DDL</sub> | V <sub>DD</sub> Quiescent Main Supply Current in Low Power Mode <sup>2</sup> | V <sub>IL</sub> = V <sub>SS</sub> , V <sub>IH</sub> = V <sub>DD</sub><br>No Load | 0.5 | 0.8 | mA   |
| I <sub>SB</sub>  | V <sub>SB</sub> Average Main Supply Current                                  | V <sub>IL</sub> = 0.5V, V <sub>IH</sub> = 2.4V<br>No Load                        | 21  | 30  | mA   |
| I <sub>SBL</sub> | V <sub>SB</sub> Quiescent Main Supply Current in Low Power Mode <sup>2</sup> | V <sub>IL</sub> = V <sub>SS</sub> , V <sub>IH</sub> = V <sub>SB</sub><br>No Load | 5   | 8   | mA   |
| I <sub>BAT</sub> | V <sub>BAT</sub> Battery Supply Current                                      | V <sub>DD</sub> , V <sub>SB</sub> = 0V,<br>V <sub>BAT</sub> = 3V                 | 0.9 | 1.5 | μA   |

1. All parameters specified for 0° C ≤ T<sub>A</sub> ≤ 70° C; V<sub>DD</sub> and V<sub>SB</sub> = 3.3V ±10%, unless otherwise specified.

2. All the modules disabled; clock outputs disabled; no LPC or SMBus activity.

### 2.1.5 Voltage Thresholds

| Symbol              | Parameter <sup>1</sup>   | Min <sup>2</sup> | Typ | Max <sup>2</sup> | Unit |
|---------------------|--|------------------|-----|------------------|------|
| V <sub>DDON</sub>   | V <sub>DD</sub> Detected as Power-on                                 | 2.3              | 2.6 | 2.9              | V    |
| V <sub>DDOFF</sub>  | V <sub>DD</sub> Detected as Power-off                                | 2.2              | 2.5 | 2.8              | V    |
| V <sub>DDHY</sub>   | V <sub>DD</sub> Hysteresis (V <sub>DDON</sub> – V <sub>DDOFF</sub> ) | 50               |     |                  | mV   |
| V <sub>SBON</sub>   | V <sub>SB</sub> Detected as Power-on                                 | 2.3              | 2.6 | 2.9              | V    |
| V <sub>SBOFF</sub>  | V <sub>SB</sub> Detected as Power-off                                | 2.2              | 2.5 | 2.8              | V    |
| V <sub>SBHY</sub>   | V <sub>SB</sub> Hysteresis (V <sub>SBON</sub> – V <sub>SBOFF</sub> ) | 50               |     |                  | mV   |
| V <sub>BATDTC</sub> | Battery Detected   | 1.0              |     | 1.2              | V    |
| V <sub>LOWBAT</sub> | Low Battery Voltage  | 1.3              |     | 1.9              | V    |

1. All parameters specified for 0° C ≤ T<sub>A</sub> ≤ 70° C.

2. Not tested. Guaranteed by characterization.

## 2.0 Device Characteristics (Continued)

### 2.2 DC CHARACTERISTICS OF PINS, BY I/O BUFFER TYPES

The following tables summarize the DC characteristics of all device pins described in *Section 1.2 on page 6*. The characteristics describe the general I/O buffer types defined in Table 1 on page 6. For exceptions, refer to Section 2.2.10 on page 24. The DC characteristics of the LPC Interface meet the PCI Local Bus Specification (*Rev 2.2 December 18, 1998*) for 3.3V DC signaling. The DC characteristics of the SMBus Interface meet the SMBus (*Rev 1.1 Dec. 11, 1998*) and SMBus (*Rev 2.0 Aug. 2000*) specifications for on-board devices.

#### 2.2.1 Input, CMOS Compatible with Schmitt Trigger

Symbol:  $I_{NCS}$

| Symbol   | Parameter             | Conditions             | Min              | Max       | Unit    |
|----------|-----------------------|------------------------|------------------|-----------|---------|
| $V_{IH}$ | Input High Voltage    |                        | $0.75 V_{SUP}^1$ | $5.5^2$   | V       |
| $V_{IL}$ | Input Low Voltage     |                        | $-0.5^1$         | 1.1       | V       |
| $V_{HY}$ | Input Hysteresis      |                        | $500^3$          |           | mV      |
| $I_{IL}$ | Input Leakage Current | $0 < V_{IN} < V_{SUP}$ |                  | $\pm 1^4$ | $\mu A$ |

1.  $V_{SUP}$  is  $V_{DD}$ ,  $V_{SB}$  or  $V_{PP}$  according to the input power well.
2. Not tested. Guaranteed by design.
3. Not tested. Guaranteed by characterization.
4. Maximum 10  $\mu A$  for all pins together. Not tested. Guaranteed by characterization.

#### 2.2.2 Input, PCI 3.3V

Symbol:  $I_{NPCI}$

| Symbol     | Parameter             | Conditions            | Min          | Max              | Unit    |
|------------|-----------------------|-----------------------|--------------|------------------|---------|
| $V_{IH}$   | Input High Voltage    |                       | $0.5 V_{DD}$ | $V_{DD} + 0.5^1$ | V       |
| $V_{IL}$   | Input Low Voltage     |                       | $-0.5^1$     | $0.3 V_{DD}$     | V       |
| $I_{IL}^2$ | Input Leakage Current | $0 < V_{IN} < V_{DD}$ |              | $\pm 1^3$        | $\mu A$ |

1. Not tested. Guaranteed by design.
2. Input leakage current includes the output leakage of the bidirectional buffers with TRI-STATE outputs.
3. Maximum 10  $\mu A$  for all pins together. Not tested. Guaranteed by characterization.

#### 2.2.3 Input, SMBus Compatible

Symbol:  $I_{NSM}$

| Symbol     | Parameter             | Conditions            | Min      | Max       | Unit    |
|------------|-----------------------|-----------------------|----------|-----------|---------|
| $V_{IH}$   | Input High Voltage    |                       | 1.4      | $5.5^1$   | V       |
| $V_{IL}$   | Input Low Voltage     |                       | $-0.5^1$ | 0.8       | V       |
| $I_{IL}^2$ | Input Leakage Current | $0 < V_{IN} < V_{SB}$ |          | $\pm 1^3$ | $\mu A$ |

1. Not tested. Guaranteed by design.
2. Input leakage current includes the output leakage of the bidirectional buffers with TRI-STATE outputs.
3. Maximum 10  $\mu A$  for all pins together. Not tested. Guaranteed by characterization.

## 2.0 Device Characteristics (Continued)

### 2.2.4 Input, TTL Compatible

Symbol:  $IN_T$

| Symbol     | Parameter             | Conditions               | Min               | Max              | Unit    |
|------------|-----------------------|--------------------------|-------------------|------------------|---------|
| $V_{IH}$   | Input High Voltage    |                          | 2.0               | 5.5 <sup>1</sup> | V       |
| $V_{IL}$   | Input Low Voltage     |                          | -0.5 <sup>1</sup> | 0.8              | V       |
| $I_{IL}^2$ | Input Leakage Current | $0 < V_{IN} < V_{SUP}^3$ |                   | $\pm 1^4$        | $\mu A$ |

1. Not tested. Guaranteed by design.
2. Input leakage current includes the output leakage of the bidirectional buffers with TRI-STATE outputs.
3.  $V_{SUP}$  is  $V_{DD}$ ,  $V_{SB}$  or  $V_{PP}$  according to the input power well.
4. Maximum 10  $\mu A$  for all pins together. Not tested. Guaranteed by characterization.

### 2.2.5 Input, TTL Compatible with Schmitt Trigger

Symbol:  $IN_{TS}$

| Symbol     | Parameter             | Conditions               | Min               | Max              | Unit    |
|------------|-----------------------|--------------------------|-------------------|------------------|---------|
| $V_{IH}$   | Input High Voltage    |                          | 2.0               | 5.5 <sup>1</sup> | V       |
| $V_{IL}$   | Input Low Voltage     |                          | -0.5 <sup>1</sup> | 0.8              | V       |
| $V_{HY}$   | Input Hysteresis      |                          | 250 <sup>2</sup>  |                  | mV      |
| $I_{IL}^3$ | Input Leakage Current | $0 < V_{IN} < V_{SUP}^4$ |                   | $\pm 1^5$        | $\mu A$ |

1. Not tested. Guaranteed by design.
2. Not tested. Guaranteed by characterization.
3. Input leakage current includes the output leakage of the bidirectional buffers with TRI-STATE outputs.
4.  $V_{SUP}$  is  $V_{DD}$ ,  $V_{SB}$  or  $V_{PP}$  according to the input power well.
5. Maximum 10  $\mu A$  for all pins together. Not tested. Guaranteed by characterization.

### 2.2.6 Output, TTL Compatible Push-Pull Buffer

Symbol:  $O_{p/n}$

Output, TTL Compatible, rail-to-rail Push-Pull buffer that is capable of sourcing  $p$  mA and sinking  $n$  mA

| Symbol   | Parameter           | Conditions             | Min               | Max | Unit |
|----------|---------------------|------------------------|-------------------|-----|------|
| $V_{OH}$ | Output High Voltage | $I_{OH} = -p$ mA       | 2.4               |     | V    |
|          |                     | $I_{OH} = -50$ $\mu A$ | $V_{SUP} - 0.2^1$ |     | V    |
| $V_{OL}$ | Output Low Voltage  | $I_{OL} = n$ mA        |                   | 0.4 | V    |
|          |                     | $I_{OL} = 50$ $\mu A$  |                   | 0.2 | V    |

1.  $V_{SUP}$  is  $V_{DD}$ ,  $V_{SB}$  or  $V_{PP}$  according to the output power well.

## 2.0 Device Characteristics (Continued)

### 2.2.7 Output, Open-Drain Buffer

**Symbol:**  $OD_n$

Output, TTL Compatible Open-Drain output buffer capable of sinking  $n$  mA. Output from these signals is open-drain and is never forced high.

| Symbol   | Parameter          | Conditions            | Min | Max | Unit |
|----------|--------------------|-----------------------|-----|-----|------|
| $V_{OL}$ | Output Low Voltage | $I_{OL} = n$ mA       |     | 0.4 | V    |
|          |                    | $I_{OL} = 50$ $\mu$ A |     | 0.2 | V    |

### 2.2.8 Output, PCI 3.3V

**Symbol:**  $O_{PCI}$

| Symbol   | Parameter           | Conditions               | Min          | Max          | Unit |
|----------|---------------------|--------------------------|--------------|--------------|------|
| $V_{OH}$ | Output High Voltage | $I_{out} = -500$ $\mu$ A | $0.9 V_{DD}$ |              | V    |
| $V_{OL}$ | Output Low Voltage  | $I_{out} = 1500$ $\mu$ A |              | $0.1 V_{DD}$ | V    |

### 2.2.9 Output, Open-Drain, PCI 3.3V

**Symbol:**  $OD_{PCI}$

| Symbol   | Parameter          | Conditions               | Min | Max          | Unit |
|----------|--------------------|--------------------------|-----|--------------|------|
| $V_{OL}$ | Output Low Voltage | $I_{out} = 1500$ $\mu$ A |     | $0.1 V_{DD}$ | V    |

### 2.2.10 Exceptions

- All pins are 5-Volt tolerant except for the pins with PCI ( $IN_{PCI}$ ,  $O_{PCI}$ ) buffer types.
- All pins are back-drive protected except for the pins with PCI ( $IN_{PCI}$ ,  $O_{PCI}$ ) and oscillator ( $O_{OSC}$ ) buffer types.
- The following pins have an internal static pull-up resistor (when enabled) and therefore may have leakage current to  $V_{SUP}$  (when  $V_{IN} = 0$ ): P12, P16, P17, SMBCLK, SMBDAT, SMBALERT, PWBTIN, SLBTIN, PWBTOUT, SIOSMI, SIOSCI, GPIO00-07, GPIOE10-17, GPIO20-27, GPIO30-37, GPIOE40-47, GPO50-57 and GPIO60-63.
- The following strap pins have an internal static pull-up resistor enabled during Power-Up reset and therefore may have leakage current to  $V_{SS}$  (when  $V_{IN} = V_{SUP}$ ): BADDR, TRIS, CKIN48, XCNF2-0, SMBSA, HFCKS, CTEST and TEST.
- $I_{OH}$  is valid for a GPIO pin only when it is not configured as open-drain.

### 2.2.11 Terminology

**Back-Drive Protection.** A pin that is back-drive protected does not sink current into the supply when an input voltage higher than the supply, but below the pin's maximum input voltage, is applied to the pin. This is true even when the supply is inactive. Note that active pull-up resistors and active output buffers are typically not back-drive protected.

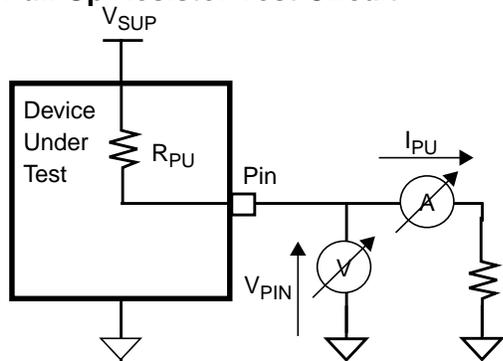
**5-Volt Tolerance.** An input signal that is 5V tolerant can operate with input voltage of up to 5V even though the supply to the device is only 3.3V. The actual maximum input voltage allowed to be supplied to the pin is indicated by the maximum high voltage allowed for the input buffer. Note that some pins have multiple buffers, not all of which are 5V tolerant. In such cases, there is a note that indicates at what conditions a 5V input may be applied to the pin; if there is no note, the low maximum voltage among the buffers is the maximum voltage allowed for the pin.

## 2.0 Device Characteristics (Continued)

### 2.3 INTERNAL RESISTORS

#### DC Test Conditions

##### Pull-Up Resistor Test Circuit



##### Pull-Down Resistor Test Circuit

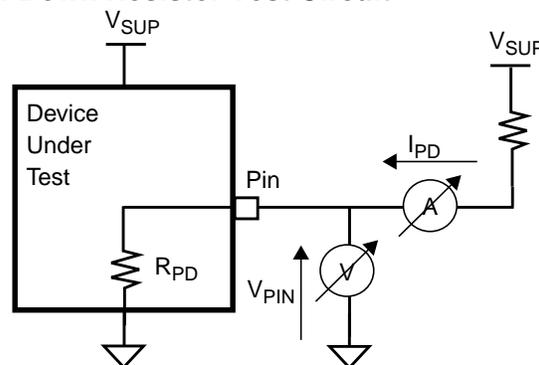


Figure 1. Internal Resistor Test Conditions,  $T_A = 0\text{ }^{\circ}\text{C}$  to  $70\text{ }^{\circ}\text{C}$ ,  $V_{SUP} = 3.3\text{V}$

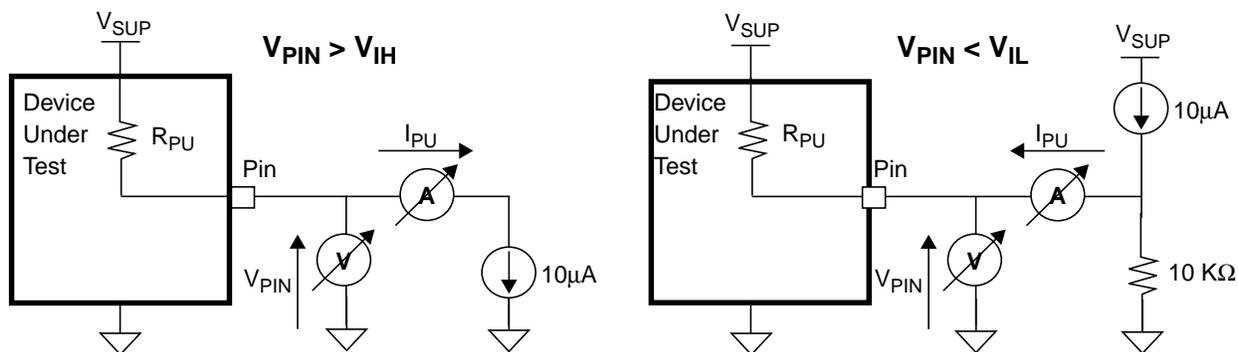


Figure 2. Internal Pull-Up Resistor for Straps,  $T_A = 0\text{ }^{\circ}\text{C}$  to  $70\text{ }^{\circ}\text{C}$ ,  $V_{SUP} = 3.3\text{V}$

Notes for Figures 1 and 2:

- $V_{SUP}$  is  $V_{DD}$  or  $V_{SB}$  according to the pin power well.
- The equivalent resistance of the pull-up resistor is calculated by  $R_{PU} = (V_{SUP} - V_{PIN}) / I_{PU}$ .
- The equivalent resistance of the pull-down resistor is calculated by  $R_{PD} = V_{PIN} / I_{PD}$ .

#### 2.3.1 Pull-Up and Pull-Down Resistors

Symbol:  $PU_{nn}$ ,  $PD_{nn}$

| Symbol   | Parameter                       | Conditions <sup>1</sup>    | Min <sup>2</sup> | Typical | Max <sup>2</sup> | Unit             |
|----------|---------------------------------|----------------------------|------------------|---------|------------------|------------------|
| $R_{PU}$ | Pull-up equivalent resistance   | $V_{PIN} = 0\text{V}$      | $nn-30\%$        | $nn$    | $nn+30\%$        | $\text{K}\Omega$ |
| $R_{PD}$ | Pull-down equivalent resistance | $V_{PIN} = V_{SUP}$        | $nn-30\%$        | $nn$    | $nn+30\%$        | $\text{K}\Omega$ |
|          |                                 | $V_{PIN} = 0.17 V_{SUP}^3$ |                  |         | $nn-50\%$        | $\text{K}\Omega$ |
|          |                                 | $V_{PIN} = 0.8 V_{SUP}^3$  | $nn-48\%$        |         |                  | $\text{K}\Omega$ |

- $T_A = 0\text{ }^{\circ}\text{C}$  to  $70\text{ }^{\circ}\text{C}$ ,  $V_{SUP} = 3.3\text{V}$ .
- Not tested. Guaranteed by characterization.
- For strap pins only.

## 2.0 Device Characteristics (Continued)

### 2.4 PACKAGE THERMAL INFORMATION

Thermal resistance (degrees C/W)  $\Theta_{JA}$  and  $\Theta_{JC}$  values for the PC87427 package are as follows:

Table 4.  $\Theta$  J Values

| Package Type | $\Theta_{JA}$ @0 lfpm | $\Theta_{JA}$ @225 lfpm | $\Theta_{JA}$ @500 lfpm | $\Theta_{JC}$ |
|--------------|-----------------------|-------------------------|-------------------------|---------------|
| 128 PQFP     | 47                    | 35.8                    | 31.1                    | 14.9          |

**Note:** Airflow for  $\Theta_{JA}$  values is measured in linear feet per minute (lfpm).

### 2.5 AC ELECTRICAL CHARACTERISTICS

#### 2.5.1 AC Test Conditions

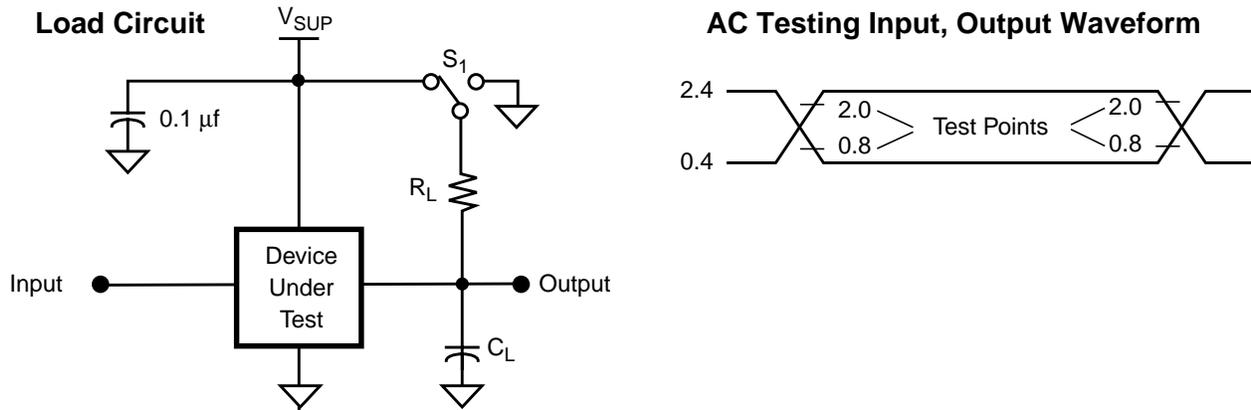


Figure 3. AC Test Conditions,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{SUP} = 3.3\text{V} \pm 10\%$

Notes:

- $V_{SUP}$  is  $V_{DD}$ ,  $V_{SB}$  or  $V_{PP}$  according to the pin power well.
- $C_L = 50$  pF for all output pins except the following pin groups:  
 $C_L = 100$  pF for Serial Port 1, 2 and M (see Section 1.4.4 on page 10) and Floppy Disk Controller (see Section 1.4.9) pins;  
 $C_L = 40$  pF for HFCKOUT pin;  
 $C_L = 400$  pF for SMBus pins (see Section 1.4.2 on page 9);  
 These values include both jig and oscilloscope capacitance.
- $S_1 = \text{Open}$  for push-pull output pins.  
 $S_1 = V_{SUP}$  for high impedance to active low and active low to high impedance transition measurements.  
 $S_1 = \text{GND}$  for high impedance to active high and active high to high impedance transition measurements.  
 $R_L = 1.0$  K $\Omega$  for all the pins.
- For the FDC open-drain interface pins,  $S_1 = V_{DD}$  and  $R_L = 150$   $\Omega$ .

## 2.0 Device Characteristics (Continued)

### 2.5.2 Reset Timing

#### V<sub>SB</sub> Power-Up Reset

| Symbol            | Figure | Description   | Reference Conditions  | Min <sup>1</sup>             | Max <sup>1</sup>         |   |
|-------------------|--------|---|---|------------------------------|--------------------------|---|
| t <sub>LRST</sub> | 5      | Minimum $\overline{\text{LRESET}}$ active time            | V <sub>SB</sub> power-up to end of $\overline{\text{LRESET}}$ | 10 ms                        |                          |   |
| t <sub>IRST</sub> | 4      | Internal Power-Up Reset Time                              | V <sub>SB</sub> power-up to end of internal reset             | Ended by 32 KHz Clock Domain | 17 * t <sub>32KOSC</sub> | t <sub>32KW</sub> + t <sub>32KVAL</sub> <sup>2</sup> + 17 * t <sub>32KOSC</sub> |
|                   | 5      |   | Ended by $\overline{\text{LRESET}}$                           |                              | t <sub>LRST</sub>        |   |
| t <sub>EPLV</sub> | 4, 5   | External strap pull-down resistors, valid time            | Before end of internal reset                                  | t <sub>IRST</sub>            |                          |   |
| t <sub>IPLV</sub> | 4, 5   | Internal strap pull-up resistors, valid time <sup>3</sup> | Before end of internal reset                                  | t <sub>IRST</sub>            |                          |   |

1. Not tested. Guaranteed by design.
2. t<sub>32KW</sub> + t<sub>32KVAL</sub> from V<sub>BAT</sub> power-up to 32 KHz domain toggling if V<sub>SB</sub> and V<sub>BAT</sub> are powered-up together; see "Low Frequency Clock Timing" on page 31.
3. Active only during V<sub>SB</sub> Power-Up reset.

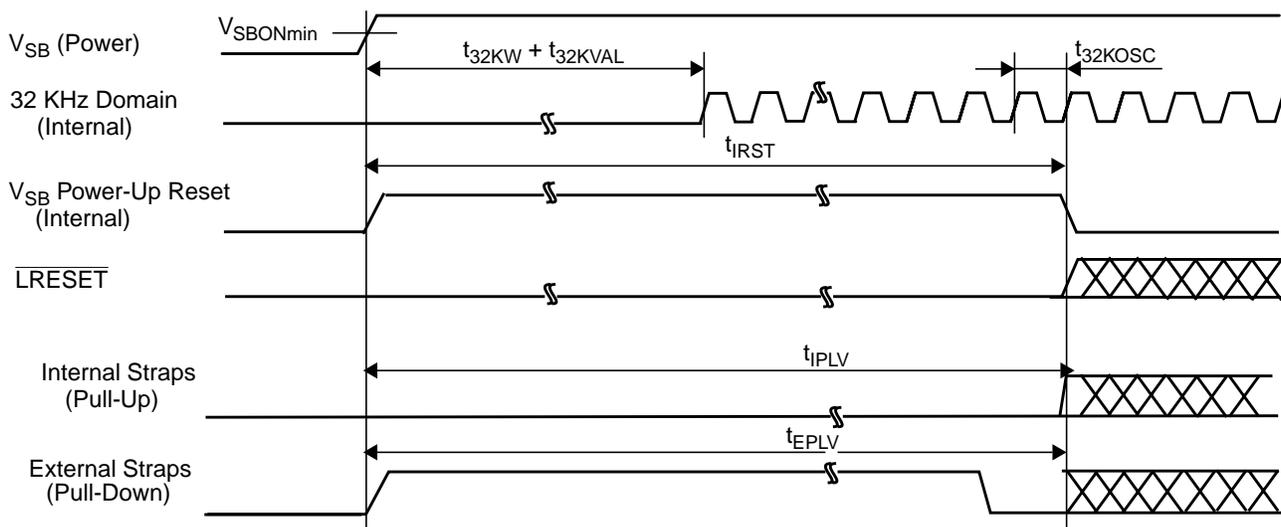


Figure 4. Internal V<sub>SB</sub> Power-Up Reset - Ended by 32 KHz Clock Domain

## 2.0 Device Characteristics (Continued)

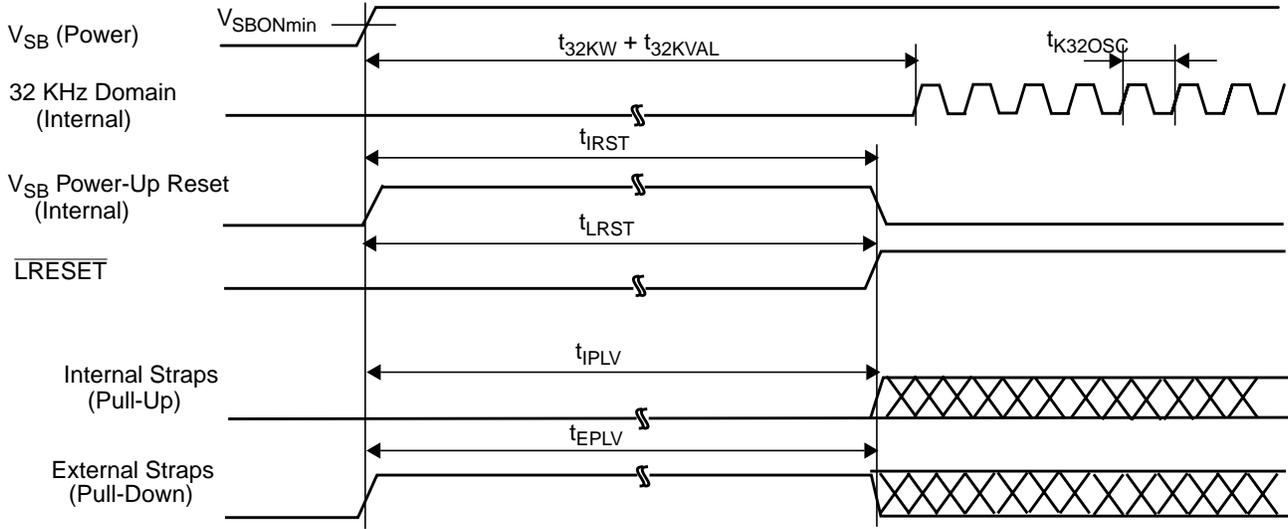


Figure 5. Internal  $V_{SB}$  Power-Up Reset - Ended by  $\overline{LRESET}$

### $V_{DD}$ Power-Up Reset

| Symbol     | Figure | Description   | Reference Conditions                            | Min <sup>1</sup> | Max <sup>1</sup> |
|------------|--------|---|---|------------------|------------------|
| $t_{LRST}$ | 6      | Minimum $\overline{LRESET}$ active time                   | $V_{DD}$ power-up to end of $\overline{LRESET}$ | 10ms             |                  |
| $t_{IRST}$ | 6      | Internal Power-Up reset time                              | $V_{DD}$ power-up to end of internal reset      | $t_{LRST}$       |                  |
| $t_{IPLV}$ | 6      | Internal strap pull-up resistors, valid time <sup>2</sup> | Before end of internal reset                    | $t_{IRST}$       |                  |
| $t_{EPLV}$ | 6      | External strap pull-down resistors, valid time            | Before end of internal reset                    | $t_{IRST}$       |                  |

1. Not tested. Guaranteed by design.
2. Active only during  $V_{DD}$  Power-Up reset.

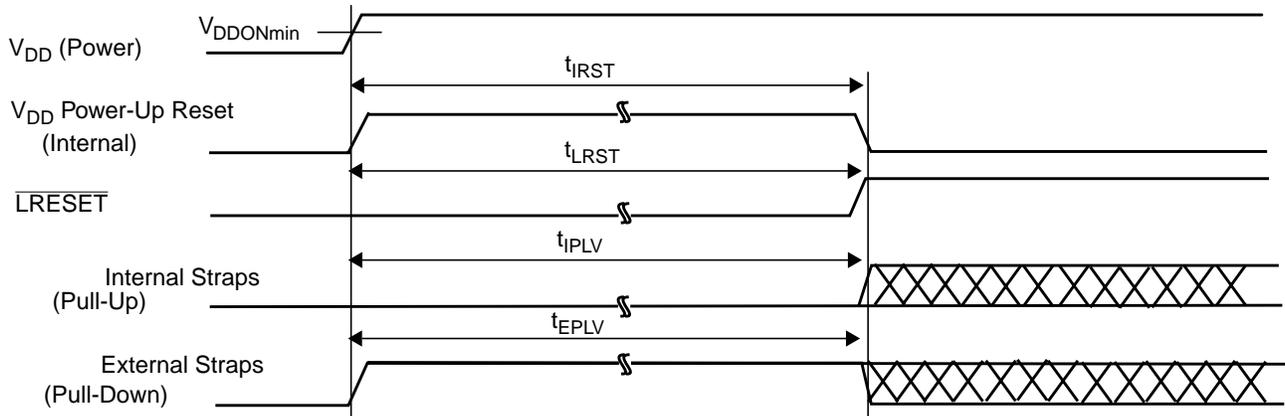


Figure 6. Internal  $V_{DD}$  Power-Up Reset

## 2.0 Device Characteristics (Continued)

### Hardware Reset

| Symbol     | Figure | Description                     | Reference Conditions | Min    | Max |
|------------|--------|---------------------------------|----------------------|--------|-----|
| $t_{WRST}$ | 7      | $\overline{LRESET}$ pulse width |                      | 100 ns |     |

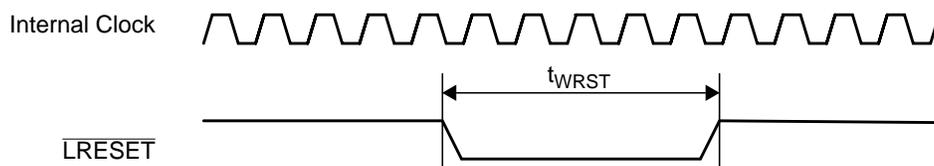


Figure 7. Hardware Reset

## 2.0 Device Characteristics (Continued)

### 2.5.3 Clock Timing

#### High Frequency Clock Timing

| Symbol       | Figure | Clock Input Parameters                 | Reference Conditions                               | CLKIN (48 MHz)    |                       |                   | Units |
|--------------|--------|--|--|-------------------|-----------------------|-------------------|-------|
|              |        |  |  | Min               | Typ                   | Max               |       |
| $t_{CH}$     | 8      | Clock High Pulse Width <sup>1</sup>    |  | 8                 |                       |                   | ns    |
| $t_{CL}$     | 8      | Clock Low Pulse Width <sup>1</sup>     |  | 8                 |                       |                   | ns    |
| $t_{CP}$     | 8      | Clock Period <sup>1</sup> (50%-50%)    |  | 20.2              | 20.83                 | 21.5              | ns    |
| $F_{CK}$     | -      | Clock Frequency                        |  | $F_{CKTYP} - 3\%$ | 48<br>( $F_{CKTYP}$ ) | $F_{CKTYP} + 3\%$ | MHz   |
| $t_{CR}$     | 8      | Clock Rise Time <sup>1</sup> (20%-80%) |  |                   |                       | 2.2 <sup>2</sup>  | ns    |
| $t_{CF}$     | 8      | Clock Fall Time <sup>1</sup> (80%-20%) |  |                   |                       | 2.2 <sup>2</sup>  | ns    |
| $t_{CINW}$   | 9      | Clock Wake-Up Time                     | After $V_{SB} > V_{SBON}$                          |                   |                       | 33                | ms    |
| $t_{CINVAL}$ | 9      | Clock Valid Time <sup>1</sup>          | Clock start toggling to clock within specification | System dependent  |                       |                   |       |

1. Not tested. Guaranteed by design.
2. Recommended value

| Symbol   | Figure | Clock Output Parameter                    | HFCKOUT (48 MHz)                  |                          |                                   | HFCKOUT (40 MHz)                   |                       |                                    | Units |
|----------|--------|---|-----------------------------------|--------------------------|-----------------------------------|------------------------------------|-----------------------|------------------------------------|-------|
|          |        |   | Min                               | Typ                      | Max                               | Min                                | Typ                   | Max                                |       |
| $t_{CH}$ | 8      | Clock High Pulse Width <sup>1,2</sup>     | 8.2                               |                          |                                   | 10.3                               |                       |                                    | ns    |
| $t_{CL}$ | 8      | Clock Low Pulse Width <sup>1,2</sup>      | 8.2                               |                          |                                   | 10.3                               |                       |                                    | ns    |
| $t_{CP}$ | 8      | Clock Period <sup>3</sup><br>(50%-50%)    | $t_{48TYP} - 32K_{TOL}^4 - 50ppm$ | 20.83<br>( $t_{48TYP}$ ) | $t_{48TYP} + 32K_{TOL}^4 + 50ppm$ | $t_{40TYP} - 32K_{TOL}^4 - 150ppm$ | 25<br>( $t_{40TYP}$ ) | $t_{40TYP} + 32K_{TOL}^4 + 150ppm$ | ns    |
| $t_{CR}$ | 8      | Clock Rise Time <sup>2</sup><br>(20%-80%) | $C_L = 15 pF$                     |                          | 2.5                               |                                    | 2.5                   |                                    | ns    |
|          |        |   | $C_L = 40 pF$                     |                          | 5                                 |                                    | 5                     |                                    | ns    |
| $t_{CF}$ | 8      | Clock Fall Time <sup>2</sup><br>(80%-20%) | $C_L = 15 pF$                     |                          | 2.5                               |                                    | 2.5                   |                                    | ns    |
|          |        |   | $C_L = 40 pF$                     |                          | 5                                 |                                    | 5                     |                                    | ns    |

1.  $C_L = 15 pF$ .
2. Not tested. Guaranteed by characterization.
3. Not tested. Guaranteed by design.
4.  $32K_{TOL}$  = tolerance of  $t_{32KCLKIN}$  parameter; see *Low Frequency Clock Timing*.

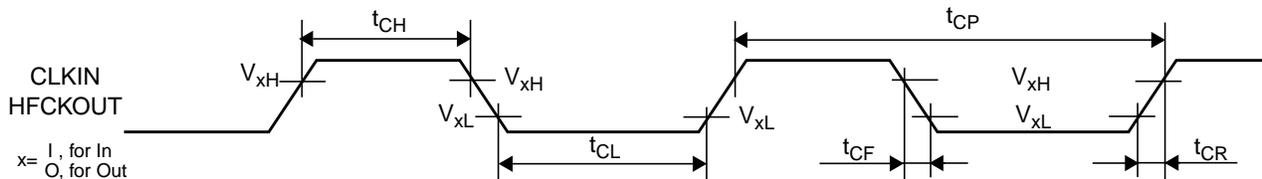


Figure 8. Clock Waveform Timing

## 2.0 Device Characteristics (Continued)

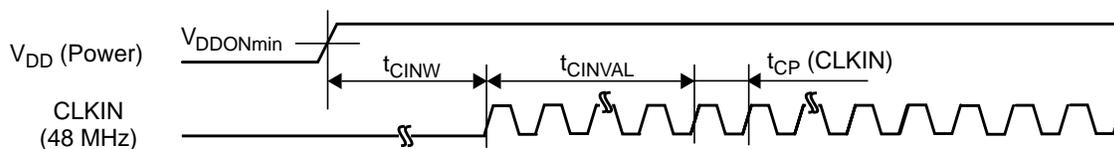


Figure 9. CLKIN Timing

### Low Frequency Clock Timing

| Symbol                       | Figure | Description  | Reference Conditions         | Min                                 | Typ                          | Max                                 | Units   |
|------------------------------|--------|--|------------------------------|-------------------------------------|------------------------------|-------------------------------------|---------|
| Clock Input Timing           |        |  |                              |                                     |                              |                                     |         |
| $t_{32KCLKIN}$               | –      | Required clock period for 32KCLKIN <sup>1</sup>              | From RE to RE of 32KCLKIN.   | 30.5145<br>( $t_{32TYP} - 100ppm$ ) | 30.517578<br>( $t_{32TYP}$ ) | 30.5206<br>( $t_{32TYP} + 100ppm$ ) | $\mu s$ |
| Clock Output Timing          |        |  |                              |                                     |                              |                                     |         |
| $t_{32KOSC}$                 | 10     | Clock period of the internal oscillator <sup>2</sup>         | From RE to RE of LFCKOUT.    |                                     | 30.517578<br>( $t_{32TYP}$ ) |                                     | $\mu s$ |
| $t_{32KW}^+$<br>$t_{32KVAL}$ | 10     | 32K oscillator wake-up time <sup>3</sup>                     | After $V_{BAT} > V_{LOWBAT}$ |                                     |                              | 1                                   | sec     |
| $t_{32KD}$                   | 11     | Internally generated 40/48 MHz clock delay time <sup>3</sup> | After $V_{SB} > V_{SBON}$    |                                     |                              | 33                                  | ms      |

1. Recommended for RTC timekeeping accuracy and for HFCKOUT, LFCKOUT frequency accuracy.
2. Determined by the values of the external crystal circuit components.
3. Not tested. Guaranteed by characterization.

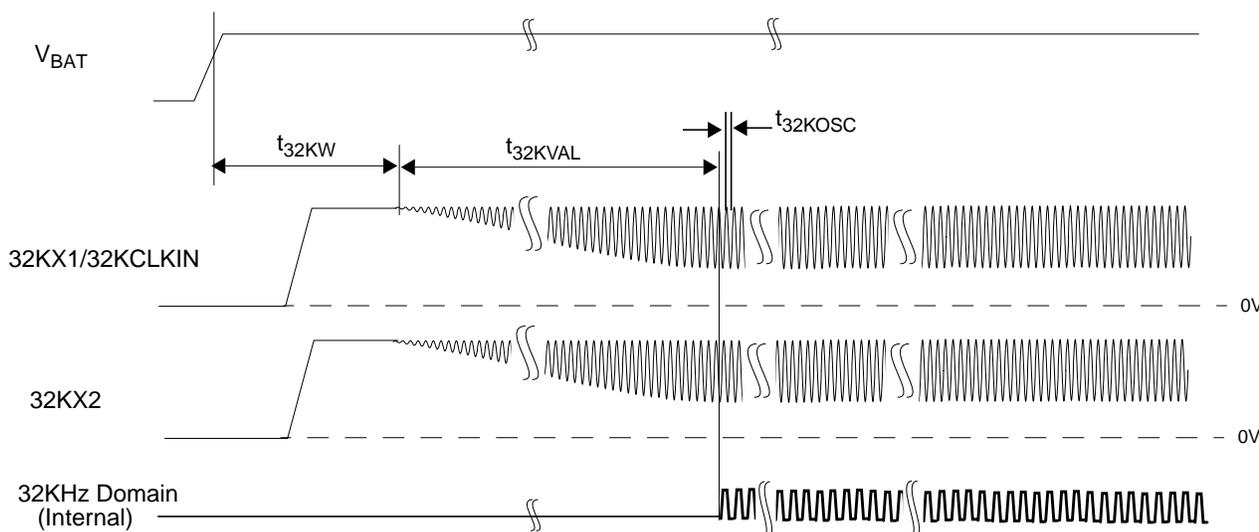


Figure 10. Low Frequency Clock Waveforms

## 2.0 Device Characteristics (Continued)

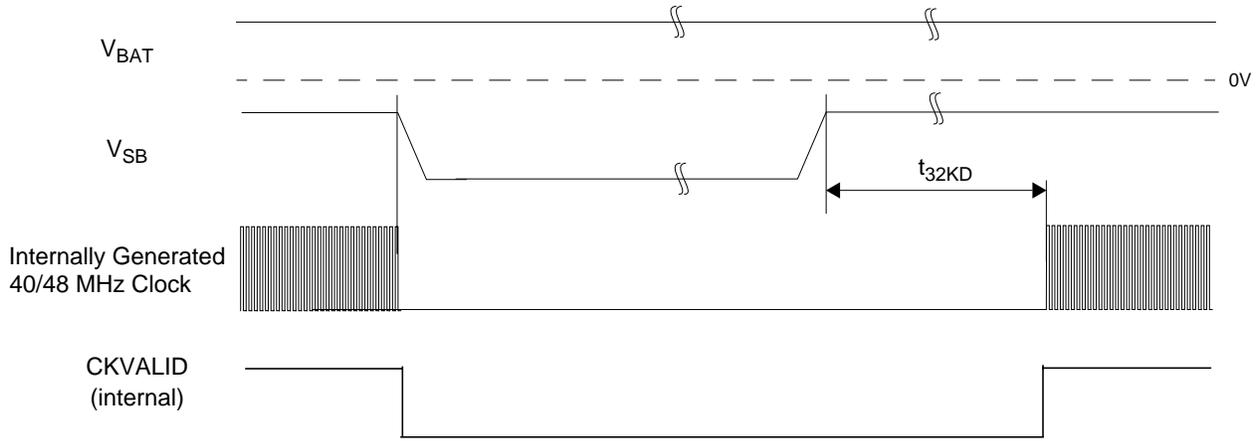


Figure 11. Internal Clock Waveforms

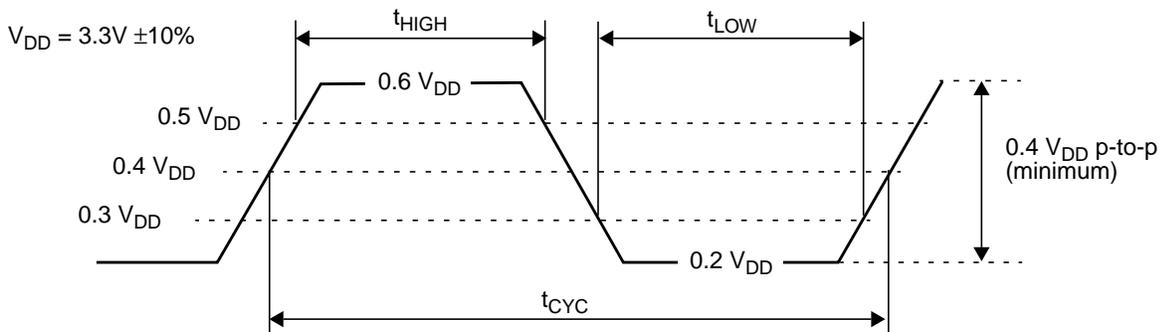
### 2.5.4 LPC Interface Timing

The AC characteristics of the LPC Interface meet the PCI Local Bus Specification (Rev 2.2 December 18, 1998) for 3.3V DC signaling.

#### LCLK and $\overline{\text{LRESET}}$

| Symbol              | Parameter   | Min | Max | Units |
|---------------------|---|-----|-----|-------|
| $t_{\text{CYC}}^1$  | LCLK Cycle Time                                     | 30  |     | ns    |
| $t_{\text{HIGH}}^2$ | LCLK High Time <sup>2</sup>                         | 11  |     | ns    |
| $t_{\text{LOW}}^2$  | LCLK Low Time <sup>2</sup>                          | 11  |     | ns    |
| -                   | LCLK Slew Rate <sup>2,3</sup>                       | 1   | 4   | V/ns  |
| -                   | $\overline{\text{LRESET}}$ Slew Rate <sup>2,4</sup> | 50  |     | mV/ns |

1. The PCI may have any clock frequency between nominal DC and 33 MHz. Device operational parameters at frequencies under 16 MHz are guaranteed by design rather than by testing. The clock frequency may be changed at any time during the operation of the system as long as the clock edges remain "clean" (monotonic) and the minimum cycle high and low times are not violated. The clock may only be stopped in a low state.
2. Not tested. Guaranteed by characterization.
3. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock wavering ( $0.2 V_{\text{DD}}$  to  $0.6 V_{\text{DD}}$ ) as shown below.
4. The minimum  $\overline{\text{LRESET}}$  slew rate applies only to the rising (de-assertion) edge of the reset signal and ensures that system noise cannot make an otherwise monotonic signal appear to bounce in the switching range.

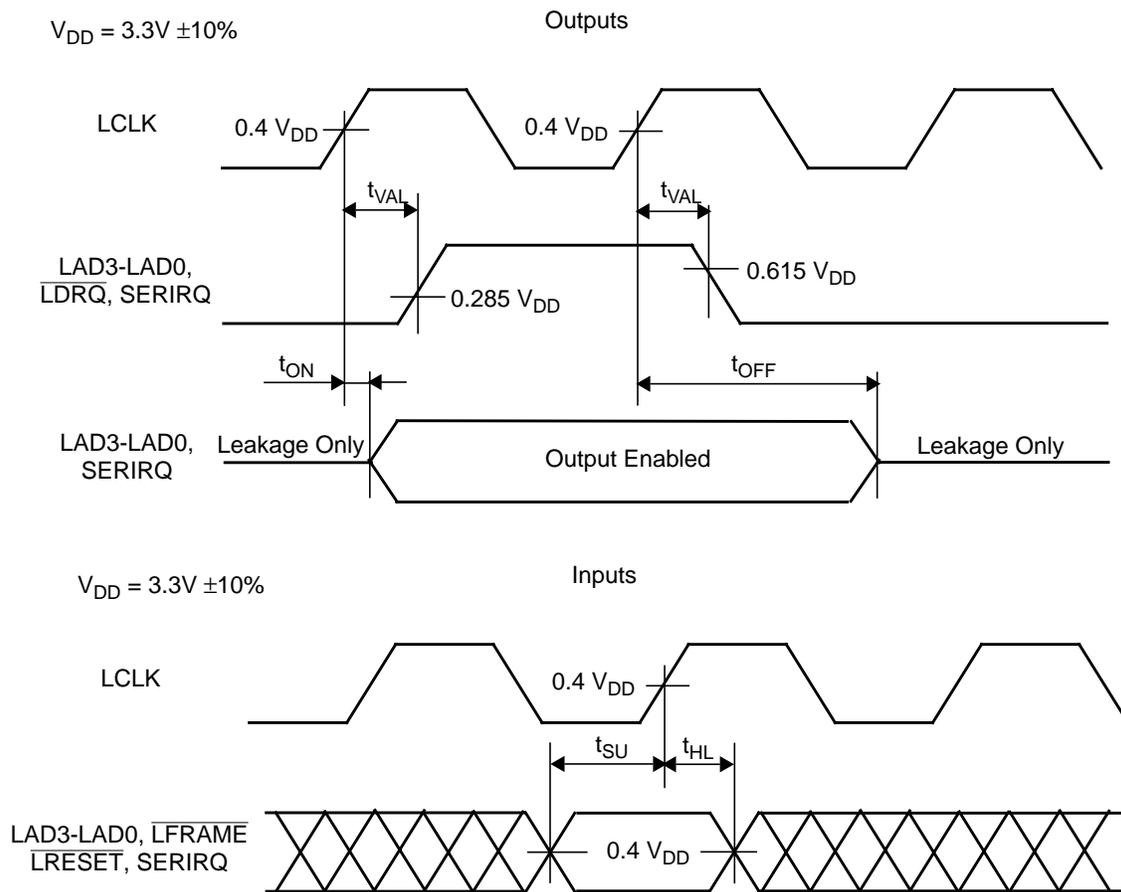


## 2.0 Device Characteristics (Continued)

### SERIRQ and LPC Signals

| Symbol    | Figure | Description           | Reference Conditions | Min            | Max             | Unit |
|-----------|--------|-----------------------|----------------------|----------------|-----------------|------|
| $t_{VAL}$ | Output | Output Valid Delay    | After RE CLK         | 2              | 11              | ns   |
| $t_{ON}$  | Output | Float to Active Delay | After RE CLK         | 2 <sup>1</sup> |                 | ns   |
| $t_{OFF}$ | Output | Active to Float Delay | After RE CLK         |                | 28 <sup>1</sup> | ns   |
| $t_{SU}$  | Input  | Input Setup Time      | Before RE CLK        | 7              |                 | ns   |
| $t_{HL}$  | Input  | Input Hold Time       | After RE CLK         | 0              |                 | ns   |

1. Not tested. Guaranteed by characterization.

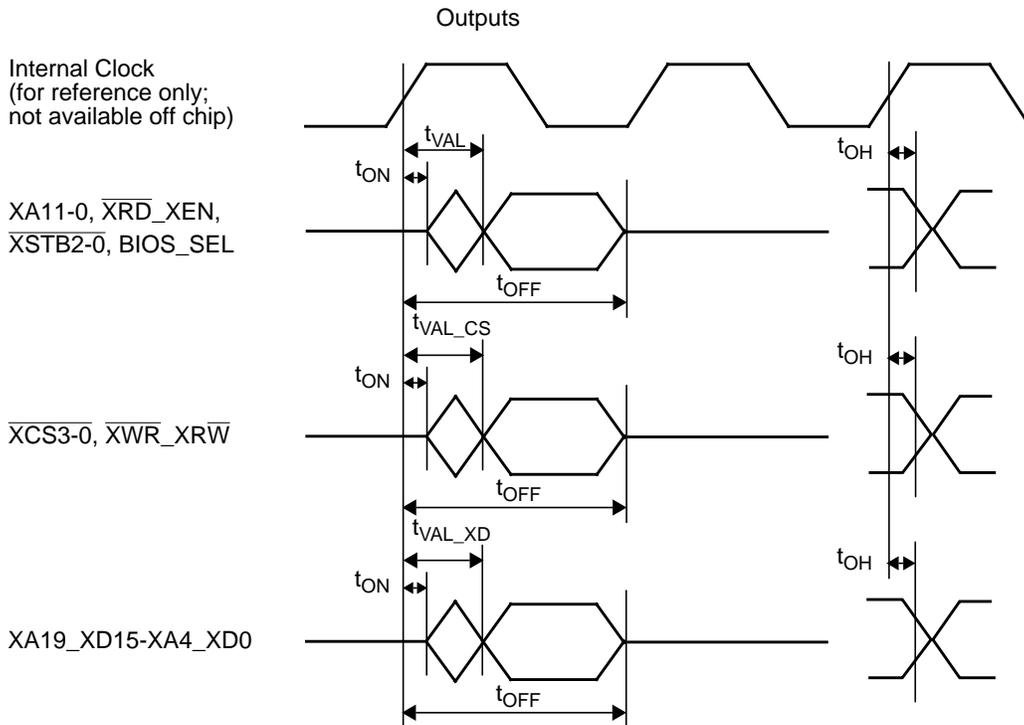


## 2.0 Device Characteristics (Continued)

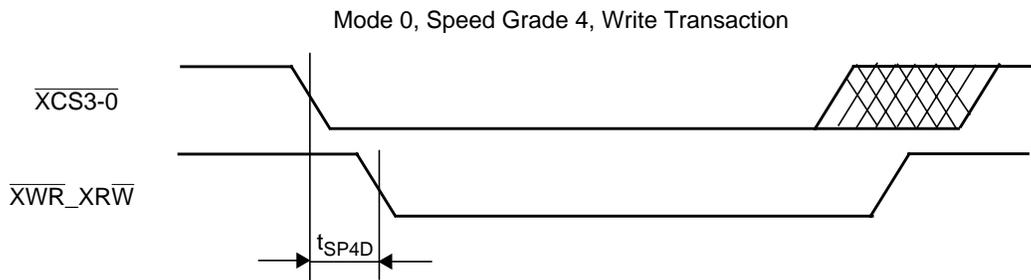
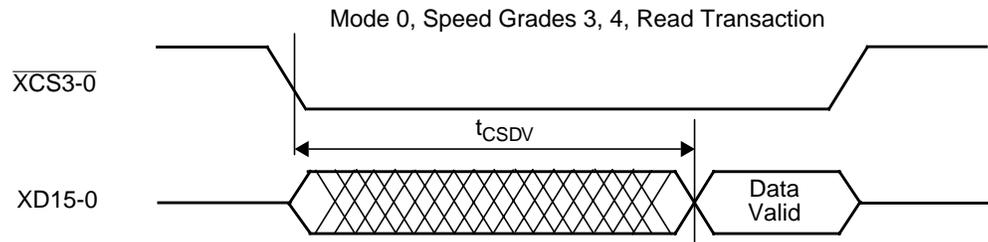
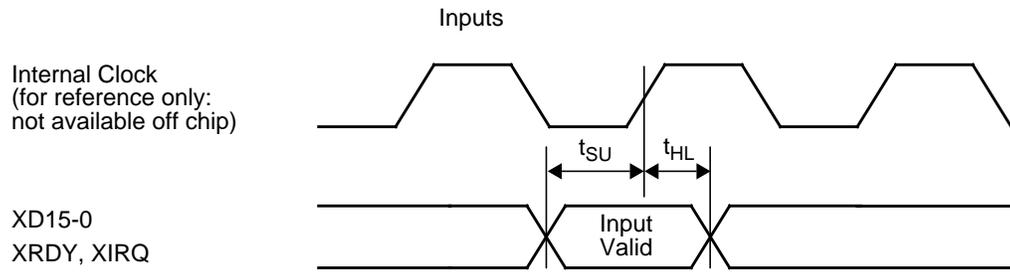
### 2.5.5 X-Bus Extension Timing

| Symbol        | Figure                                      | Description   | Reference Conditions      | Min                   | Max                | Unit |    |
|---------------|---|---|---------------------------|-----------------------|--------------------|------|----|
| $t_{VAL}$     | Outputs                                     | Output Valid Delay  | After RE Internal Clock   | $C_L = 50 \text{ pF}$ | 22 <sup>1</sup>    | ns   |    |
| $t_{VAL\_CS}$ | Outputs                                     | Output Valid Delay for $\overline{XCS3-0}$ , $\overline{XWR\_XR\overline{W}}$ | After RE Internal Clock   | $C_L = 20 \text{ pF}$ | 12 <sup>1</sup>    | ns   |    |
| $t_{VAL\_XD}$ | Outputs                                     | Output Valid Delay for $\overline{XA19\_XD15-XA4\_XD0}$                       | After RE Internal Clock   | $C_L = 20 \text{ pF}$ | 17 <sup>1</sup>    | ns   |    |
|               |   |   |                           | $C_L = 50 \text{ pF}$ | 20 <sup>1</sup>    | ns   |    |
| $t_{ON}$      | Outputs                                     | Float to Active Delay   | After RE Internal Clock   |                       | 0 <sup>2</sup>     | ns   |    |
| $t_{OH}$      | Outputs                                     | Output Hold time  | After RE Internal Clock   |                       | 0 <sup>2</sup>     | ns   |    |
| $t_{OFF}$     | Outputs                                     | Active to Float Delay   | After RE Internal Clock   | $C_L = 50 \text{ pF}$ | 30 <sup>1</sup>    | ns   |    |
| $t_{SU}$      | Inputs                                      | Input Setup Time  | Before RE Internal Clock  |                       | 5 <sup>1</sup>     | ns   |    |
| $t_{HL}$      | Inputs                                      | Input Hold Time   | After RE Internal Clock   |                       | 0 <sup>1</sup>     | ns   |    |
| $t_{CSDV}$    | Mode 0, Speed Grades 3, 4, Read Transaction | Chip Select active to Data Valid  | Read from External Device | $C_L = 20 \text{ pF}$ | 73                 | ns   |    |
|               |   |   |                           | $C_L = 50 \text{ pF}$ | 70                 | ns   |    |
| $t_{SP4D}$    | Mode 0, Speed Grade 4, Write Transaction    | Chip Select active to $\overline{XWR\_XR\overline{W}}$ active delay           | Write to External Device  | $C_L = 20 \text{ pF}$ | - 0.5 <sup>1</sup> | 0.5  | ns |

1. Not tested. Guaranteed by characterization.
2. Not tested. Guaranteed by design.



2.0 Device Characteristics (Continued)



## 2.0 Device Characteristics (Continued)

### 2.5.6 SMBus Timing

| Symbol              | Figure | Description  | Type of Requirement <sup>1</sup> | Min               | Max               | Unit          |
|---------------------|--------|--|----------------------------------|-------------------|-------------------|---------------|
| $t_{\text{SMBR}}$   | 12     | Rise time (SMBCLK and SMBDAT)                                | Input <sup>2</sup>               |                   | 1000 <sup>3</sup> | ns            |
| $t_{\text{SMBF}}$   | 12     | Fall time (SMBCLK and SMBDAT)                                | Input                            |                   | 300 <sup>3</sup>  | ns            |
|                     |        |  | Output <sup>2</sup>              |                   | 250 <sup>4</sup>  | ns            |
| $t_{\text{SMBCKL}}$ | 12     | Clock low period (SMBCLK)                                    | Input                            | 4.7               |                   | $\mu\text{s}$ |
| $t_{\text{SMBCKH}}$ | 12     | Clock high period (SMBCLK)                                   | Input                            | 4                 |                   | $\mu\text{s}$ |
| $t_{\text{SMBCY}}$  | 13     | Clock cycle (SMBCLK)   | Input                            | 10                |                   | $\mu\text{s}$ |
| $t_{\text{SMBDS}}$  | 13     | Data setup time (before clock rising edge)                   | Input                            | 250               |                   | ns            |
|                     |        |  | Output <sup>2</sup>              | 250               |                   | ns            |
| $t_{\text{SMBDH}}$  | 13     | Data hold time (after clock falling edge)                    | Input                            | 0                 |                   | ns            |
|                     |        |  | Output <sup>2</sup>              | 300               |                   | ns            |
| $t_{\text{SMBPS}}$  | 14     | Stop condition setup time (clock before data)                | Input                            | 4                 |                   | $\mu\text{s}$ |
| $t_{\text{SMBSH}}$  | 14     | Start condition hold time (clock after data)                 | Input                            | 4                 |                   | $\mu\text{s}$ |
| $t_{\text{SMBBUF}}$ | 14     | Bus free time between Stop and Start conditions (SMBDAT)     | Input                            | 4.7               |                   | $\mu\text{s}$ |
| $t_{\text{SMBRS}}$  | 15     | Restart condition setup time (clock before data)             | Input                            | 4.7               |                   | $\mu\text{s}$ |
| $t_{\text{SMBRH}}$  | 15     | Restart condition hold time (clock after data)               | Input                            | 4                 |                   | $\mu\text{s}$ |
| $t_{\text{SMBLEX}}$ | -      | Cumulative clock low extend time from Start to Stop (SMBCLK) | Output                           |                   | 25 <sup>3</sup>   | ms            |
| $t_{\text{SMBTO}}$  | -      | Clock low time-out (SMBCLK)                                  | Input                            | 25 <sup>3,5</sup> |                   | ms            |
|                     |        |  | Output                           |                   | 35 <sup>3,6</sup> | ms            |

1. An "Input" type is a value the PC87427 expects from the system; an "Output" type is a value the PC87427 provides to the system.

2. Test conditions:  $R_L = 1 \text{ K}\Omega$  to  $V_{\text{SB}} = 3.3\text{V}$ ,  $C_L = 400 \text{ pF}$  to GND.

3. Not tested. Guaranteed by design.

4. Not tested. Guaranteed by characterization.

5. The PC87427 detects a time-out condition if SMBCLK is held low for more than  $t_{\text{SMBTO}}$ .

6. Upon detection of a time-out condition, the PC87427 resets the SMBus Interface no later than  $t_{\text{SMBTO}}$ .

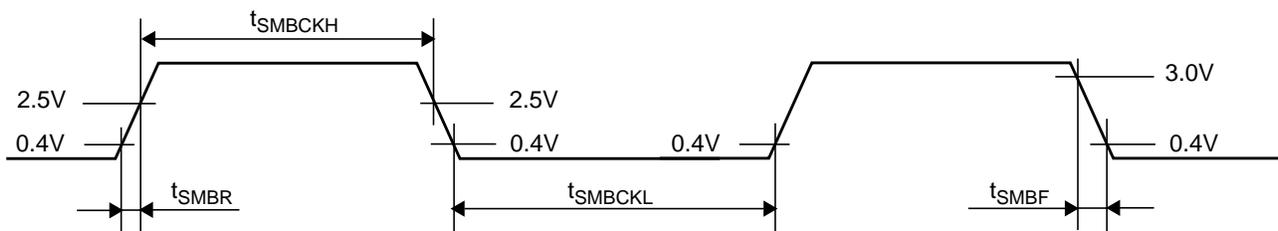


Figure 12. SMBus Signals (SMBCLK and SMBDAT) Rising Time and Falling Time

2.0 Device Characteristics (Continued)

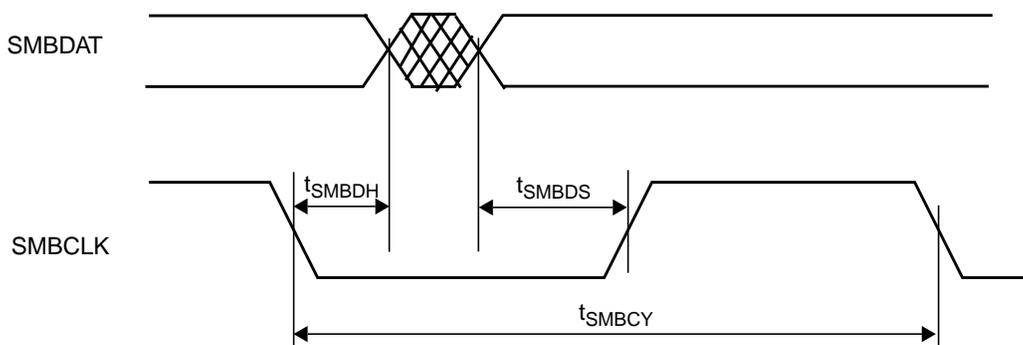


Figure 13. SMBus Data Bit Timing

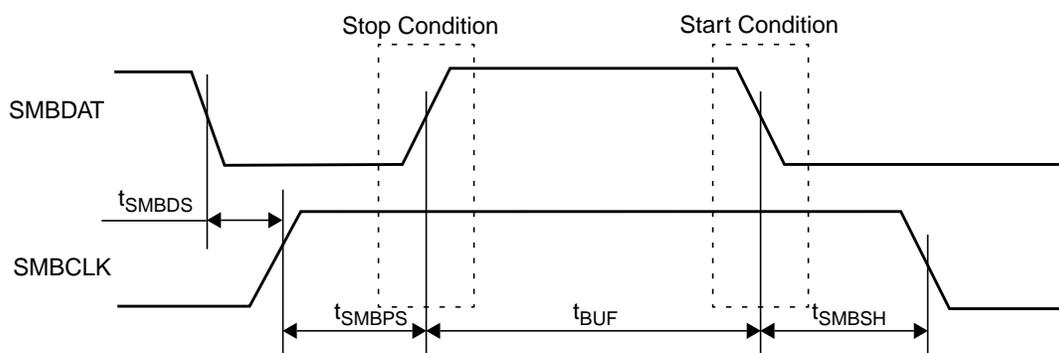


Figure 14. SMBus Start and Stop Condition Timing

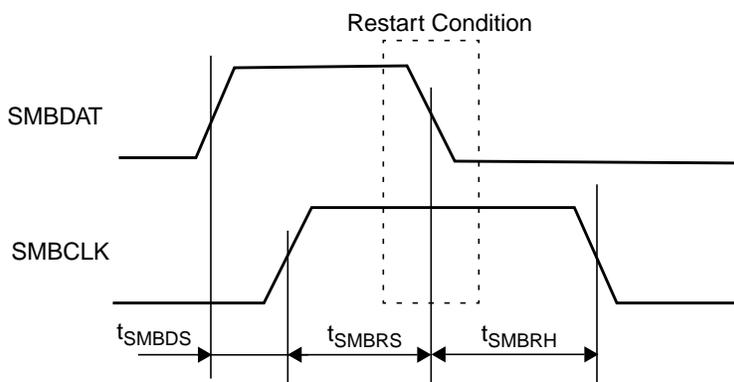


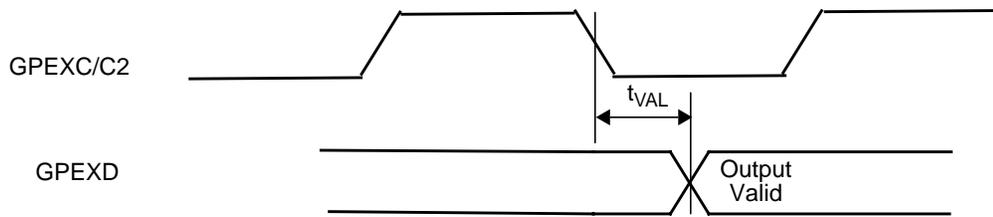
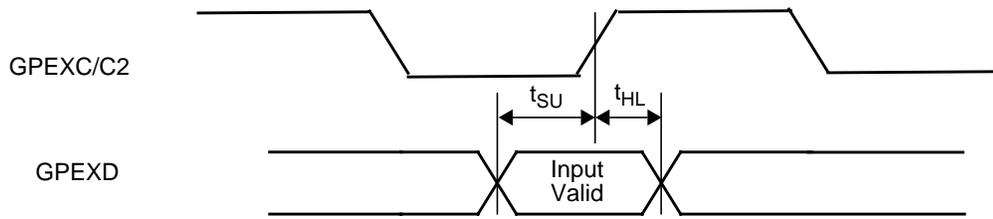
Figure 15. SMBus Restart Condition Timing

## 2.0 Device Characteristics (Continued)

### 2.5.7 GPE Timing

| Symbol    | Figure  | Description        | Reference Conditions                             | Min             | Max            | Unit |
|-----------|---------|--------------------|--|-----------------|----------------|------|
| $t_{VAL}$ | Outputs | Output Valid Delay | After clock falling edge<br>$C_L = 20\text{ pF}$ |                 | 4 <sup>1</sup> | ns   |
| $t_{SU}$  | Inputs  | Input Setup Time   | Before clock rising edge                         | 12 <sup>1</sup> |                | ns   |
| $t_{HL}$  | Inputs  | Input Hold Time    | After clock rising edge                          | 0 <sup>1</sup>  |                | ns   |

1. Not tested. Guaranteed by characterization.



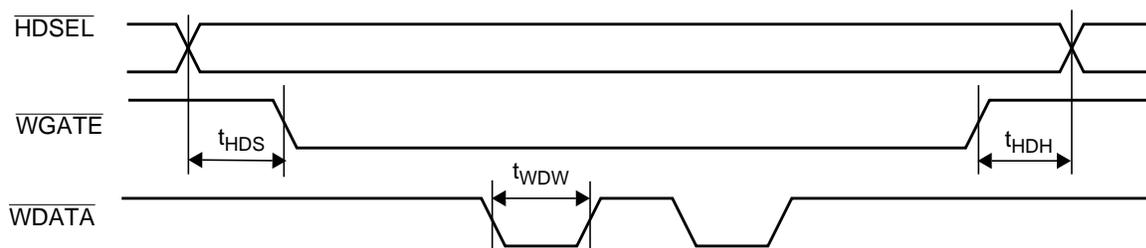
## 2.0 Device Characteristics (Continued)

### 2.5.8 FDC Timing

#### FDC Write Data Timing

| Symbol    | Parameter   | Min   | Max | Unit          |
|-----------|---|---|-----|---------------|
| $t_{HDH}$ | $\overline{HDSEL}$ Hold from $\overline{WGATE}$ Inactive <sup>1</sup> | 100   |     | $\mu\text{s}$ |
| $t_{HDS}$ | $\overline{HDSEL}$ Setup to $\overline{WGATE}$ Active <sup>1</sup>    | 100   |     | $\mu\text{s}$ |
| $t_{WDW}$ | Write Data Pulse Width <sup>1</sup>                                   | See $t_{DRP}$ , $t_{ICP}$ and $t_{WDW}$ values in table below |     |               |

1. Not tested. Guaranteed by design.



$t_{DRP}$   $t_{ICP}$   $t_{WDW}$  Values

| Data Rate | $t_{DRP}$ | $t_{ICP}$            | $t_{ICP}$ Nominal | $t_{WDW}$          | $t_{WDW}$ Minimum | Unit |
|-----------|-----------|----------------------|-------------------|--------------------|-------------------|------|
| 1 Mbps    | 1000      | $6 \times t_{CP}^1$  | 125               | $2 \times t_{ICP}$ | 250               | ns   |
| 500 Kbps  | 2000      | $6 \times t_{CP}^1$  | 125               | $2 \times t_{ICP}$ | 250               | ns   |
| 300 Kbps  | 3333      | $10 \times t_{CP}^1$ | 208               | $2 \times t_{ICP}$ | 375               | ns   |
| 250 Kbps  | 4000      | $12 \times t_{CP}^1$ | 250               | $2 \times t_{ICP}$ | 500               | ns   |

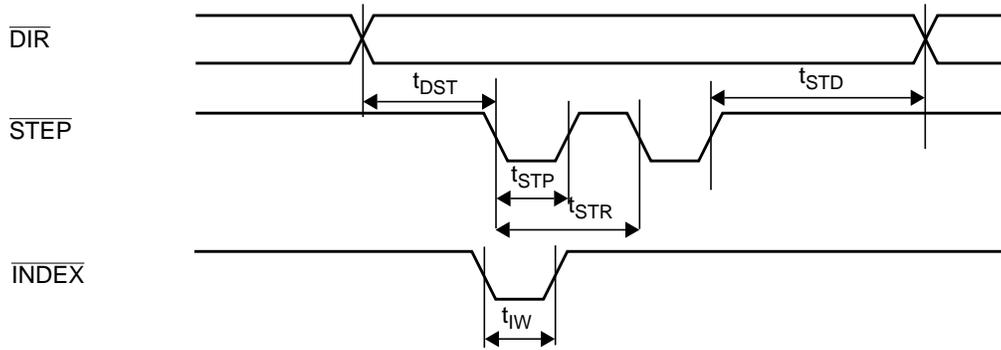
1.  $t_{CP}$  is the clock period defined for CLKIN in *Clock Timing* on page 30.

#### FDC Drive Control Timing

| Symbol    | Parameter   | Min       | Max | Unit          |
|-----------|---|-----------|-----|---------------|
| $t_{DST}$ | $\overline{DIR}$ Setup to $\overline{STEP}$ Active <sup>1</sup> | 6         |     | $\mu\text{s}$ |
| $t_{IW}$  | Index Pulse Width   | 100       |     | ns            |
| $t_{STD}$ | $\overline{DIR}$ Hold from $\overline{STEP}$ Inactive           | $t_{STR}$ |     | ms            |
| $t_{STP}$ | $\overline{STEP}$ Active High Pulse Width <sup>1</sup>          | 8         |     | $\mu\text{s}$ |
| $t_{STR}$ | $\overline{STEP}$ Rate Time <sup>1</sup>                        | 0.5       |     | ms            |

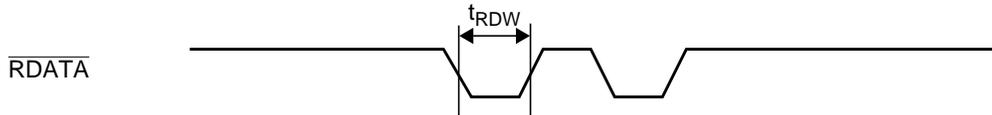
1. Not tested. Guaranteed by design.

## 2.0 Device Characteristics (Continued)



### FDC Read Data Timing

| Symbol    | Parameter             | Min | Max | Unit |
|-----------|-----------------------|-----|-----|------|
| $t_{RDW}$ | Read Data Pulse Width | 50  |     | ns   |



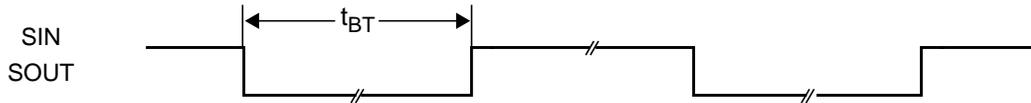
## 2.5.9 Serial Interfaces 1, 2 and M Timing

### Serial Port Data Timing

| Symbol   | Parameter  | Conditions  | Min              | Max              | Unit |
|----------|--|-------------|------------------|------------------|------|
| $t_{BT}$ | Single Bit Time in Serial Interface <sup>1</sup> | Transmitter | $t_{BTN} - 25\%$ | $t_{BTN} + 25\%$ | ns   |
|          |  | Receiver    | $t_{BTN} - 2\%$  | $t_{BTN} + 2\%$  | ns   |

1. Not tested. Guaranteed by design.

2.  $t_{BTN}$  is the nominal bit time in the Serial Interface; it is determined by the setting of the Baud Generator Divisor registers.



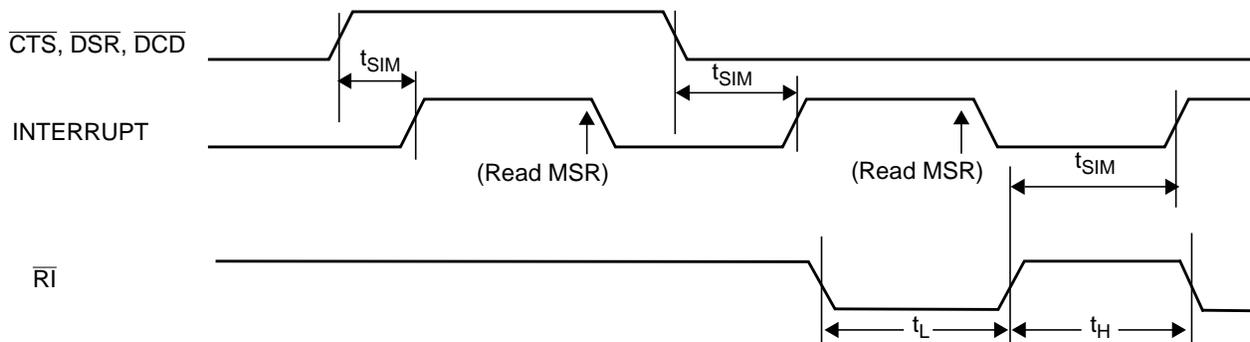
## 2.0 Device Characteristics (Continued)

### Modem Control Timing

| Symbol    | Parameter                                | Min | Max | Unit |
|-----------|--|-----|-----|------|
| $t_L$     | $\overline{RI}$ Low Time <sup>1,2</sup>  | 10  |     | ns   |
| $t_H$     | $\overline{RI}$ High Time <sup>1,2</sup> | 10  |     | ns   |
| $t_{SIM}$ | Delay to Set IRQ from Modem Input        |     | 40  | ns   |

1. Not tested. Guaranteed by characterization

2. This value also applies to  $\overline{RI2,1}$  wake-up detection in the SWC module.



### 2.5.10 SWC Timing

#### Wake-Up Inputs at $V_{SB}$ Power Switching

| Symbol     | Figure | Description                                    | Reference Conditions   | Min                                   | Max                      |
|------------|--------|--|--|---------------------------------------|--------------------------|
| $t_{EWIV}$ | 16     | External Wake-up inputs not valid <sup>1</sup> | At $V_{SB}$ power on, after the 32 KHz Domain is toggling          | $24576 \cdot t_{32KOSC}$ <sup>2</sup> | $32768 \cdot t_{32KOSC}$ |
| $t_{PBOP}$ | 17     | $\overline{PWBTOUT}$ pulse time <sup>1</sup>   | Resume by $\overline{SLPS3}$ , $\overline{SLPS5}$ after Power Fail | $100 \text{ ms}$ <sup>3</sup>         | $100.03 \text{ ms}$      |

1. Not tested. Guaranteed by design.

2.  $t_{32KOSC}$  is the cycle time of the 32 KHz clock domain (see "Low Frequency Clock Timing" on page 31)

3. Except when generated by  $\overline{PWBTIN}$  pulse.

2.0 Device Characteristics (Continued)

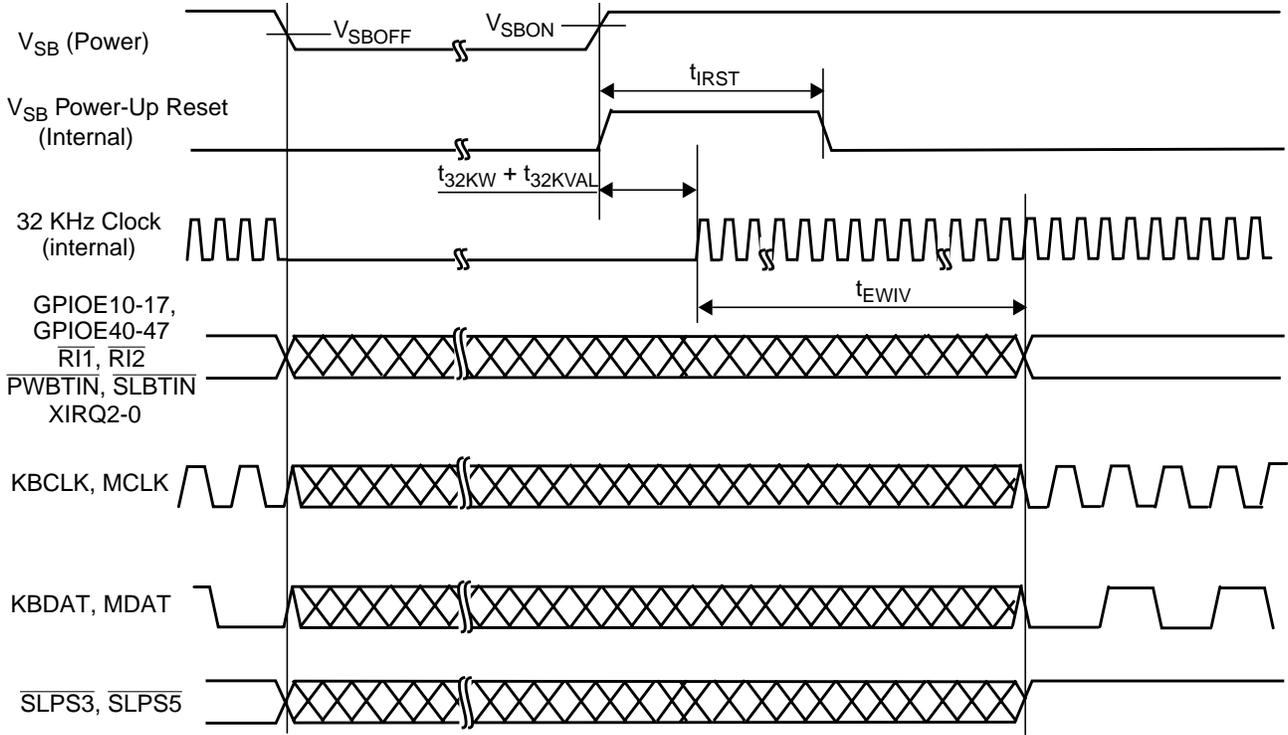


Figure 16. Inputs at  $V_{SB}$  Power Switching (No  $V_{BAT}$ )

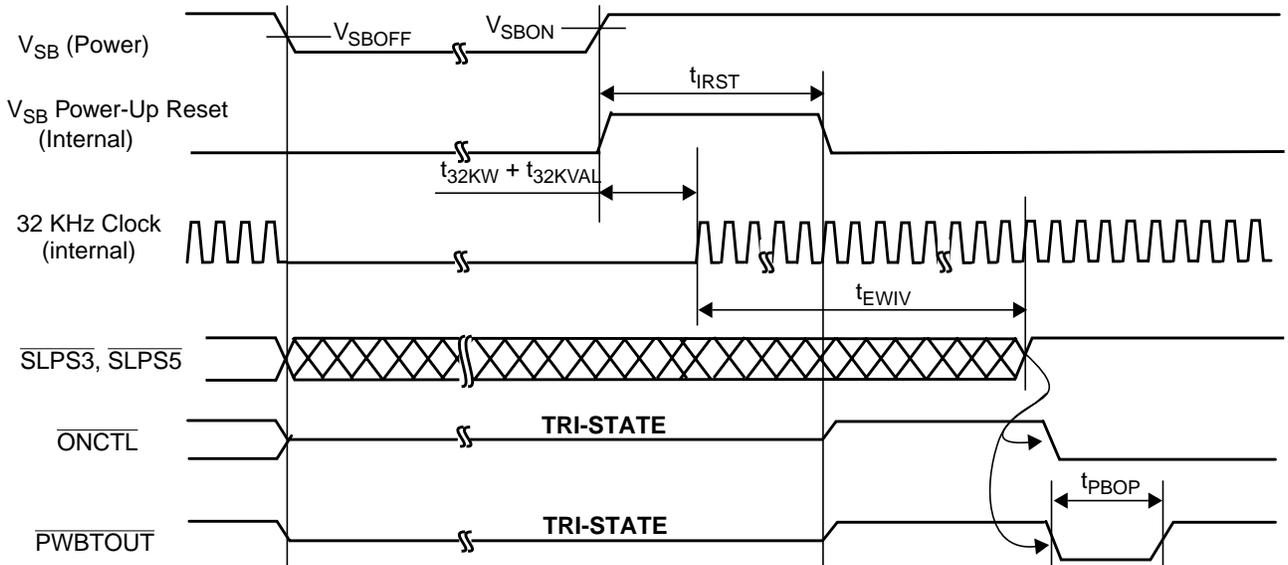


Figure 17. Resume by  $\overline{SLPS3}$ ,  $\overline{SLPS5}$ , After Power Fail (No  $V_{BAT}$ )

## 2.0 Device Characteristics (Continued)

### Wake-Up Inputs at $V_{DD}$ Power Switching

| Symbol     | Figure | Description                                | Reference Conditions                 | Min                                   | Max                      |
|------------|--------|--|--------------------------------------|---------------------------------------|--------------------------|
| $t_{EWIV}$ | 18     | External Wake-up inputs valid <sup>1</sup> | After $V_{DD}$ power On <sup>2</sup> | $24576 \cdot t_{32KOSC}$ <sup>3</sup> | $32768 \cdot t_{32KOSC}$ |

1. Not tested. Guaranteed by design.
2. The 32 KHz clock domain is assumed to be toggling at  $V_{DD}$  power stable.
3.  $t_{32KOSC}$  is the cycle time of the 32 KHz clock domain (see "Low Frequency Clock Timing" on page 31)

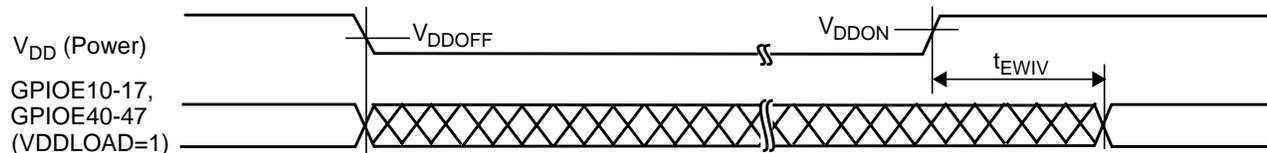


Figure 18. Wake-Up Inputs at  $V_{DD}$  Power Switching

### Power Button Override

| Symbol     | Figure | Description                                   | Reference Conditions             | Min    | Max    |
|------------|--------|---|----------------------------------|--------|--------|
| $t_{PBOV}$ | 19     | Power Button Override <sup>1</sup>            | After $\overline{PWBTIN}$ active | 3.89 s | 3.92 s |
| $t_{OVEX}$ | 19     | Power Button Override Extension <sup>1</sup>  | After the end of $t_{PBOV}$      | 0.2 s  | 0.24 s |
| $t_{PBID}$ | 19     | $\overline{PWBTIN}$ disable time <sup>1</sup> | After a Power-Off event          | 1 s    | 1.25 s |

1. Not tested. Guaranteed by design.

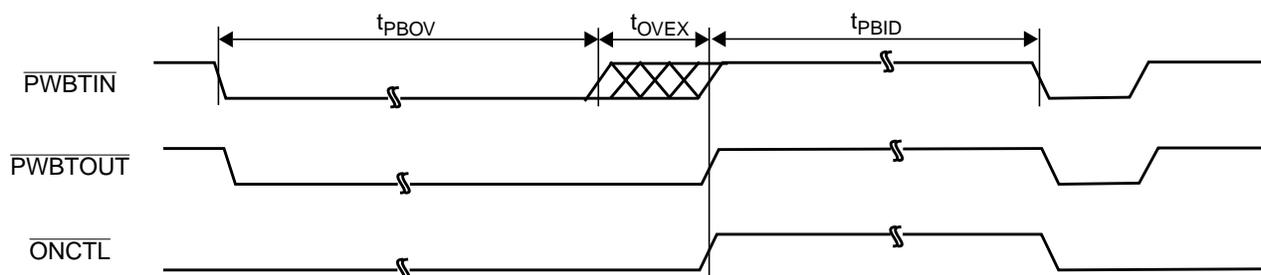


Figure 19. Power Button Override Timing

## 2.0 Device Characteristics (Continued)

### Crowbar

| Symbol      | Figure | Description   | Reference Conditions                                    | Min                | Max               |
|-------------|--------|---|---|--------------------|-------------------|
| $t_{CBTO}$  | 20, 21 | Crowbar Timeout <sup>1</sup>                                    | After $\overline{ONCTL}$ active, or $V_{DD}$ power fall | 0.5 s <sup>2</sup> | 20 s <sup>2</sup> |
| $t_{CBPBO}$ | 20, 21 | Crowbar generated, $\overline{PWBTOUT}$ pulse time <sup>1</sup> | After completion of Crowbar Timeout                     | 4 s                | 4.25 s            |
| $t_{PBID}$  | 20, 21 | $\overline{PWBTIN}$ disable time <sup>1</sup>                   | After a Power-Off event                                 | 1 s                | 1.25 s            |

1. Not tested. Guaranteed by design.
2. Set by CRBAR\_TOUT.

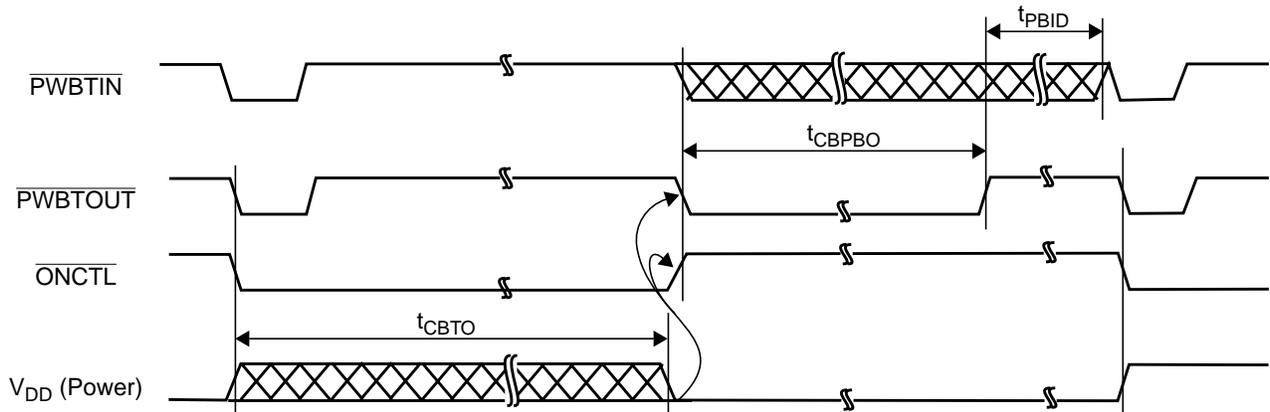


Figure 20. Power-On Crowbar Timing

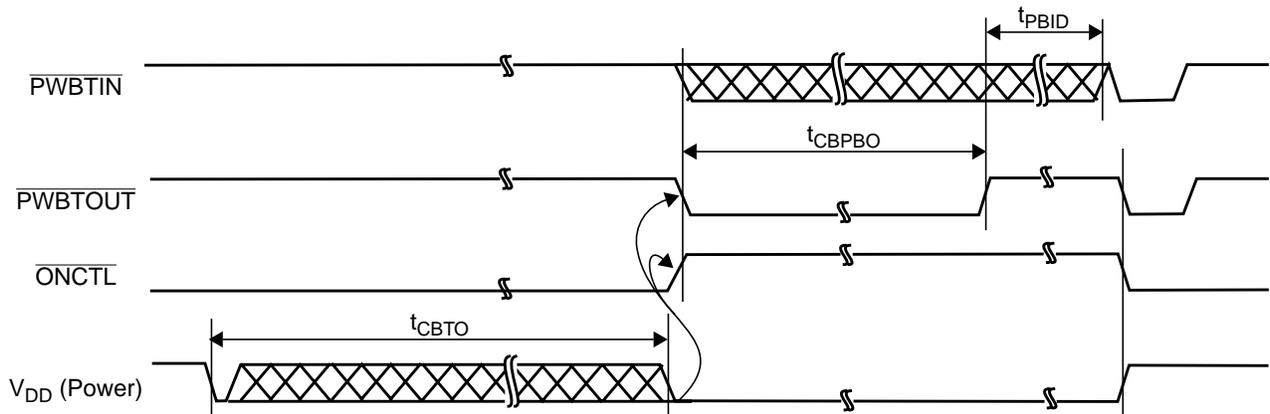


Figure 21. Power-Fall Crowbar Timing

## 2.0 Device Characteristics (Continued)

### System Watchdog Power-Off / ETC

| Symbol     | Figure | Description                                   | Reference Conditions    | Min | Max    |
|------------|--------|---|-------------------------|-----|--------|
| $t_{PBO}$  | 22     | $\overline{PWBTOUT}$ pulse time <sup>1</sup>  |                         | 4 s | 4.25 s |
| $t_{PBID}$ | 22     | $\overline{PWBTIN}$ disable time <sup>1</sup> | After a Power-Off event | 1 s | 1.25 s |

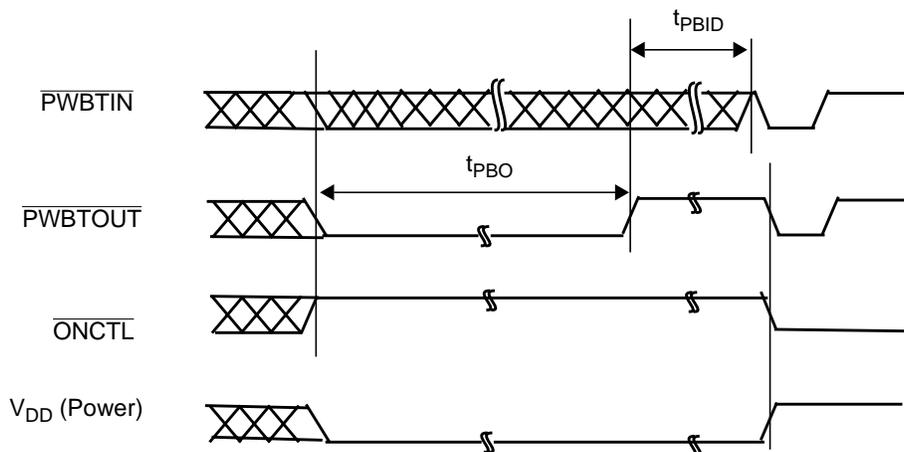
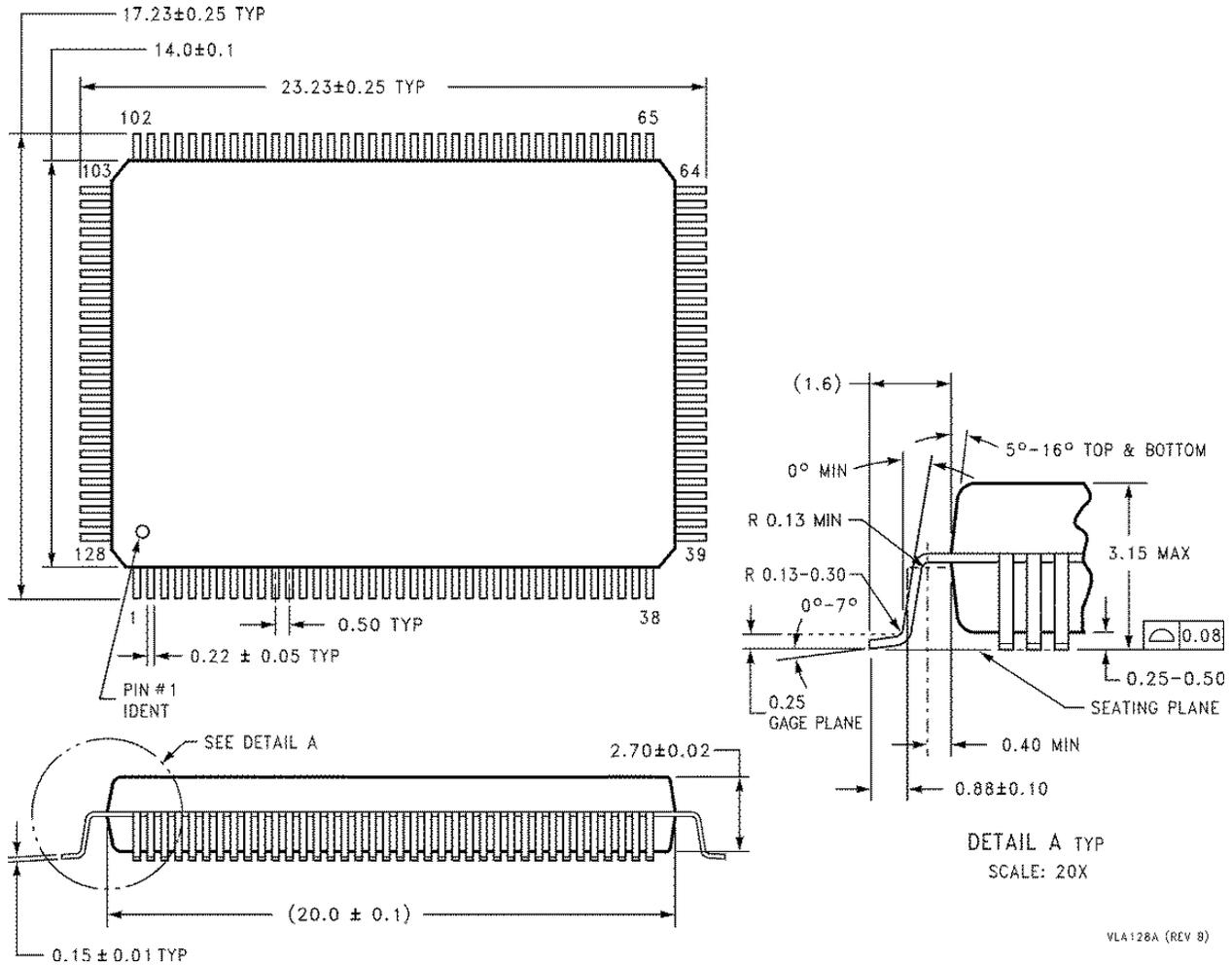


Figure 22. Watchdog Power-Off / ETC Timing

## Physical Dimensions

All dimensions are in millimeters



**Plastic Quad Flatpack (PQFP), JEDEC**  
**Order Number PC87427-xxx/VLA**  
**NS Package Number VLA128A**

VLA128A (REV B)

### LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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