MX86101P

64-BIT HIGH PERFORMANCE GUI ACCELERATOR

1. INTRODUCTION

1-1 FEATURES

- Built-in powerful Graphics Coprocessor perfectly matched to Windows™ operations
  - memory-mapped registers interface to system CPU
  - up to 4K bytes system memory bitmap to screen memory bitmap transfer ports
  - 4/8/15/16/32 packed-pixel color format hardware acceleration
  - Microsoft® Windows™ compatible 256 raster operation
  - 8 x 8 internal pattern map
  - bit block transfer with transparent/opaque capability
  - line draw
  - area fill
  - color expansion
  - rectangular clipping
  - hardware graphic cursor for GUI display modes, with the cursor images stored in display off-screen memory
  - X, Y addressing capability to pixel maps
- 64/32-bit DRAM display memory access.
- 16-bit RAMDAC interface.
- Resolution support up to 1280 x 1024 x 256 non-interlaced, 1024 x 768 x 64K non-interlaced, and 800 x 600 x 16M non-interlaced.
- 32-bit VESA local bus architecture.
- Support of PCI local bus V2.0 specification
  - memory burst cycles
  - configurable display memory base address
  - configurable extended I/O base address
  - relocatable BIOS ROM base address
  - palette snoop operation
- Support of VESA DPMS specifications
- Support of 1MB and 2MB display memory
- Support of various types of DRAM, namely 256K x 4, 256K x 8, 512K x 8, 256K x 16 (1CAS, 2WE) and 256K x 16 (2CAS, 1WE)
- Up to 110 MHz pixel clock
- Up to 68 KHz sweep rate
- Support feature connector
- 208-pin PQFP

1-2 SOFTWARE DRIVERS

- Operating System
  - Microsoft® Windows™ 3.1
  - Microsoft® Windows NT™ 3.1/3.5
  - IBM® OS/2™ 2.1/ T2.1/3.0
- Application Program
  - Autodesk® AutoCAD™ Release 12/11
  - Autodesk® AutoShade™ Ver. 2.0
  - Autodesk® 3D Studio™ Ver.2.0
  - WordPerfect™ 5.0/5.1/6.0
  - Lotus® 123™ 2.x/3.0/3.1
- User-Friendly Utility Program
  - Installation program for application program drivers
  - Windows setup program
  - VESA DPMS setup and Screen-saving Program

1-3 OVERVIEW

The MX86101P is a 64-bit high-performance GUI (Graphics User Interface) Accelerator. With a very cost-effective solution, the MX86101P provides the user a super acceleration and high resolution/color for Windows™ system display. The MX86101P is an ideal solution for both Pentium™ and 486 system.

The MX86101P supports both PCI and VESA local bus. For VL-bus implementation, the MX86101P is a pin-to-pin-compatible upgrade version of the MX86100. For PCI bus implementation, the MX86101P is fully compatible with the PCI Rev. 2.0 specifications.

The MX86101P features a powerful Graphics Coprocessor. Since the Graphics Coprocessor is designed to perfectly matched to Windows™ operation, the MX86101P can achieve extremely high performance in Windows™ environment.

The MX86101P incorporates a 64-bit DRAM bus design with up to 78MHz memory clock rate. This broadens the memory bandwidth tremendously and enlightens the DRAM-access bottleneck. Since the memory clock and the DRAM timing can be programmable, the MX86101P provides much flexibility in DRAM sources. Card makers can just pick up almost any kind of DRAMs available in the market for the MX86101P.

1-4 GENERAL DESCRIPTION

The MX86101P is VLSI implementation of the Windows Accelerator Chip. Besides 100% IBM VGA register-level compatible, this chip is specifically designed for VESA and PCI Local Bus system with improved performance throughput on display.

To improve graphic performance throughput in windows environment, such as Microsoft Windows 3.x, Windows NT, OS/2 2.X, and others, this chip includes a Graphic COProcessor Unit to enhance the drawing functions such as bitblt, draw line, boundary clipping, color expansion. This chip also includes lots of hardware features to let a DRAM-based GUI design compete with VRAM-based GUI's, such as 64-bit DRAM bus interface, 32-bit CPU bus interface, 4 level depths CPU read/write buffer, 16 level depths CRTC read FIFO, graphic H/W cursor, memory mapped coprocessor registers, dual clock display system design.

Operating at dot clock rate up to 110MHz, the MX86101P supports high resolution graphics and alphanumeric display modes for both monochrome and color monitors. With 2M bytes display memory, the MX86101P-based systems can provide the ultra-high graphics resolution of 1280 x 1024 in 256 simultaneous colors at non-interlaced 60Hz, or 1024 x 768 in 64K high colors at non-interlaced 70Hz, or 800 x 600 in 16M true colors at non-interlaced 60Hz.

The MX86101P also allows system designers to select different types of DRAM to implement the display system. DRAM types comprising 256K x 4, 512K x 8, 256K x 16 with 2 CAS 1 WE, and 256K x 16 with 1 CAS 2 WE can be used, but not mixed. With 16 pieces of 256K x 4 DRAMS, we can implement a 2M-byte display system of 64-bit DRAM bus interface. With 4 pieces of 256K x 16 DRAMS, we can implement a 2M-byte display system of 64-bit DRAM bus interface. With 4 pieces of 512K x8 DRAMs, we can implement a 2M-byte display system of 32-bit DRAM bus interface. The MX86101P is also a cost-effective solution for systems with 1M bytes of display memory. For this type of design, we can use 8 pieces of 256K x 4 DRAMs or 2 pieces of 256K x 16 DRAMs to implement a cost-effective 32-bit DRAM bus interface solution.

The MX86101P also implements a 16-bit display pixel out interface to an externally implemented 16-bit RAMDAC. Through this interface, higher refresh rate, resolution and color display modes can be implemented, for instance, 1024 x 768 in 64K high colors at refresh rate of 70Hz.

In short, all of the above features make the MX86101P a very cost competitive product at high-end Windows™ accelerator system with the most outstanding cost/performance ratio.