PRELIMINARY

MX8325-1

MOTHERBOARD CLOCK GENERATOR

FEATURES

- Clock generator for 486, Pentinum™ , and Cryix 6x86 based systems
- Support ISA-, VESA-, and PCI- based designs
- Support independent PCI bus clock and 1/2 CPU clock, and 48 MHz USB clock
- Support 24 MHz clock
- Built-in on-chip one 1 to 3, two 1 to 2 buffers, with minimum pin-to-pin output skew below 500ps
- Under 0.1% CPU clock period change while switching frequency
- Skew-controlled 1/2 CPU and 1X CPU clocks to winthin 500ps
- On-chip loop filter components
- Smooth and glitch-free switching for programmable clock generators
- 28-PIN(300 mil)SOP

FUNCTIONAL DESCRIPTON

The MX8325-1 is a CMOS motherboard clock generator used in portable or desktop computers. The chip includes an oscillator circuitry and three PLLs to provide 14.318 MHz, CPUCLK, 1/2 CPUCLK, PCI bus CLK, and 24 MHz clocks. This chip is built with low skew clock drivers that provide the needed buffering for PCI applications. The desired CPUCLK is selected by S0, S1 and S2. This chip provides selectable 75 MHz, 66.6 MHz, 60 MHz, 55 MHz, 33.3 MHz, 50 MHz, 40 MHz, 33.3 MHz, and 25 MHz CPUCLK. It is suitable for 80486DX, 80486DX2, 80486DX4, 80486S series, Pentium-based and Cyrix 6x86 series designs.

Independent PCI bus clock and 1/2 CPUCLK make this chip mostly suitable for asychronous PCI or synchronous PCI design.

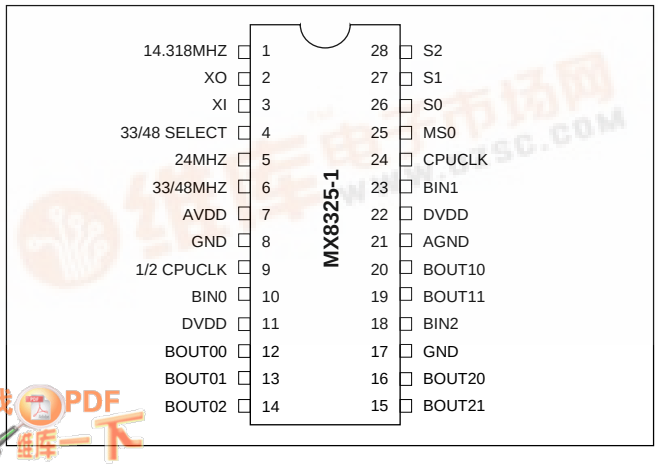
GENERAL DESCRIPTION

There are three PLLs in the MX8325-1 to support smooth transition and glitch-free CPU clock, 24 MHz and PCI bus clock. It can be suited for synchronous PCI design (1/2 CPU clock) and asynchronous PCI design (PCICLK clock). In addition, the MX8325-1 supports one 1-to-3 and two 1-to-2 buffers for motherboard appilications. The output pin-to-pin clock skews of the buffers are controlled below 500 ps. The only external components are a 14.318 MHz crystal and decoupling capacitors.

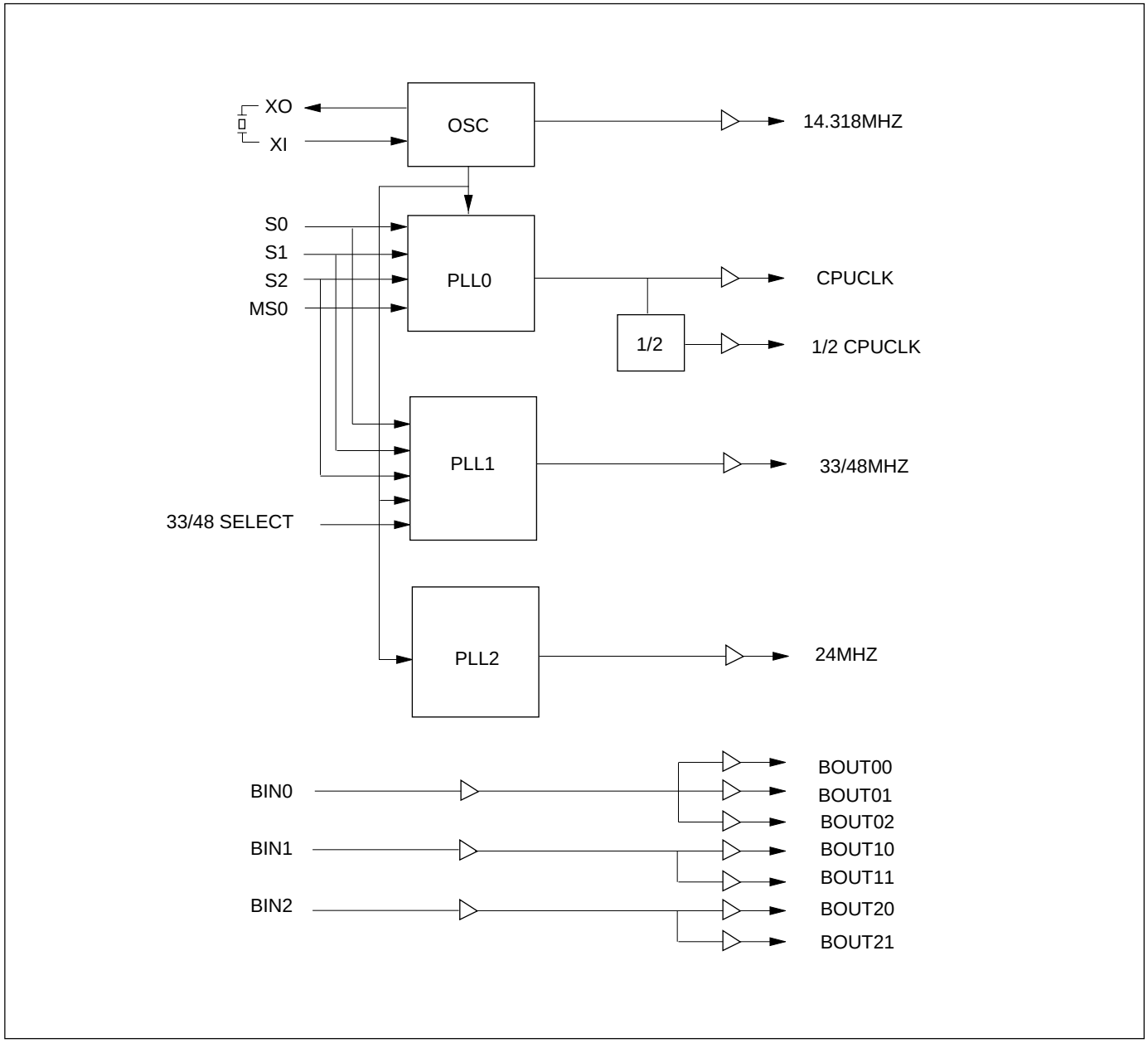
The frequency select pins (S2, S1 and S0) determine the CPU output frequency, which is shown in next page. The CPU clock offers the feature of smooth and glitch-free frequency transition when the frequency modes are changed. The chip meets the 486 and Pentium™ specifications of subseqent clock period changed under 0.1%. The simultaneous 1X and 1/2 CPU clocks offer controlled skew within 500ps (TPY).

PIN CONFIGURATIONS

28 SOP



BLOCK DIAGRAM



PIN DESCRIPTION (For MX8355-03)

SYMBOL	PIN TYPE	PIN NUMBER	DESCRIPTION
14.318MHz	O	1	14.318 MHz output (8mA)
XO	I	2	X'tal output. No connection when clock input
XI	I	3	X'tal input or reference clock input
33/48 SELECT	I	4	33 MHZ/48 MHZ select pin internal pull-high.
24 MHz	O	5	24 MHz clock output (8mA)
33/48 MHZ	O	6	33 or 48 MHZ output depends on pin4.
AVDD	--	7	Analog power supply
GND	--	8	Ground
1/2 CPUCLK	O	9	1/2 CPU clock output (12mA)
BIN0	I	10	Buffer (0) input, internal pull high
DVDD	--	11	Digital power supply
BOUT00	O	12	Buffer (0) output (0)
BOUT01	O	13	Buffer (0) output (1)
BOUT02	O	14	Buffer (0) output (2)
BOUT21	O	15	Buffer (2) output (1)
BOUT20	O	16	Buffer (2) output (0)
DGND	--	17	Digital ground
BIN2	I	18	Buffer (2) input, internal pull high
BOUT11	O	19	Buffer (1) output (1)
BOUT10	O	20	Buffer (1) output (0)
AGND	--	21	Analog ground
DVDD	--	22	Digital power supply
BIN1	I	23	Buffer (1) input, internal pull high
CPUCLK	O	24	CPU clock output (12mA)
MS0	I	25	CPU clock output mode select pin, internal pull high
S0	I	26	CPU clock select pin (0), internal pull high (20mA)
S1	I	27	CPU clock select pin (1), internal pull high (20mA)
S2	I	28	CPU clock select pin (2), internal pull high (20mA)

FREQUENCY TABLE

	MS0=1, 33/48 SELECT=H			MS0=1, 33/48 SELECT=L		
S(2:0)	CPU	1/2 CPUCLK	33/48 MHZ	CPU	1/2 CPUCLK	33/48 MHZ
0	66.6	33.3	33.3	66.6	33.3	48
1	75.0	37.5	33.3	75.0	37.5	48
2	60.0	30.0	33.3	60.0	30.0	48
3	55.0	27.5	33.3	55.0	27.5	48
4	50.0	25	33.3	50.0	25	48
5	40.0	20.0	33.3	40.0	20.0	48
6	33.3	16.65	33.3	33.3	16.65	48
7	25.0	12.5	25.0	25.0	12.5	48

"1" means High.

"0" means Low.

The mode (S (2:0)=(0, 0, 1)) is not supported.

AC/DC CHARACTERISTICS

DC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
DVDD, AVDD	Supply Voltage	4.5	5	5.5	V	
IDD	Supply Current		35		mA	No load, running at 50 MHz
IIH	Input High Current		5		uA	
VOL	Output Low Voltage			0.4	V	IOL=20mA, VDD=5V
VOH	Output High Voltage	2.4			V	IOH=-40mA, VDD=5V
VIL	Input LOW Voltage			0.8	V	for buffers only
VIH	Input High Voltage	2.0			V	for buffers only
RPU	Pull-up Resistor			100K	Ohms	

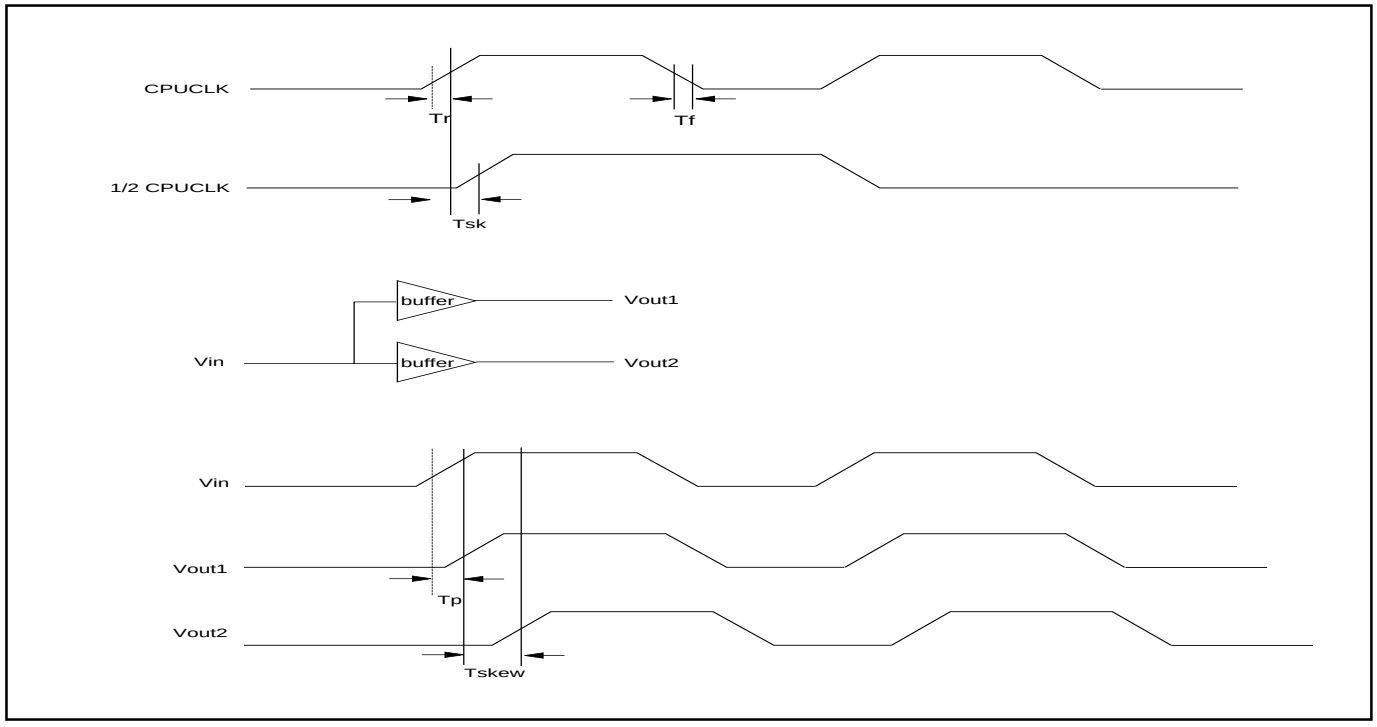
CAPACITANCE TA = 25°C, f = 1.0 MHz (Sampled only)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance		8		pF	
COUT	Output Capacitance		8		pF	

AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Tr	Output Rise Time 0.8V to 2.0V			1.5	ns	25 pF load
Tf	Output Fall Time 2.0V to 0.8V			1.5	ns	25 pF load
Tsk	Clock skew CPU and 1/2 CPU		0.5	1	ns	25 pF load
D_t	Output Duty Cycle	40/60	48/52	60/40	%	25 pF load
Tp	Propagation Delay Bin to Bout	2	3	5	ns	15 pF load Measured at 1.4V
T_{jis}	CPUCLK, 1/2 CPUCLK Out Sigma		250	500	ps	
T_{skew}	Buffer Out skew			500	ps	15 pF load Measured at 1.4V
Fref	Reference Clock Frequency	14.318	14.318	14.318	MHz	

WAVEFORMS

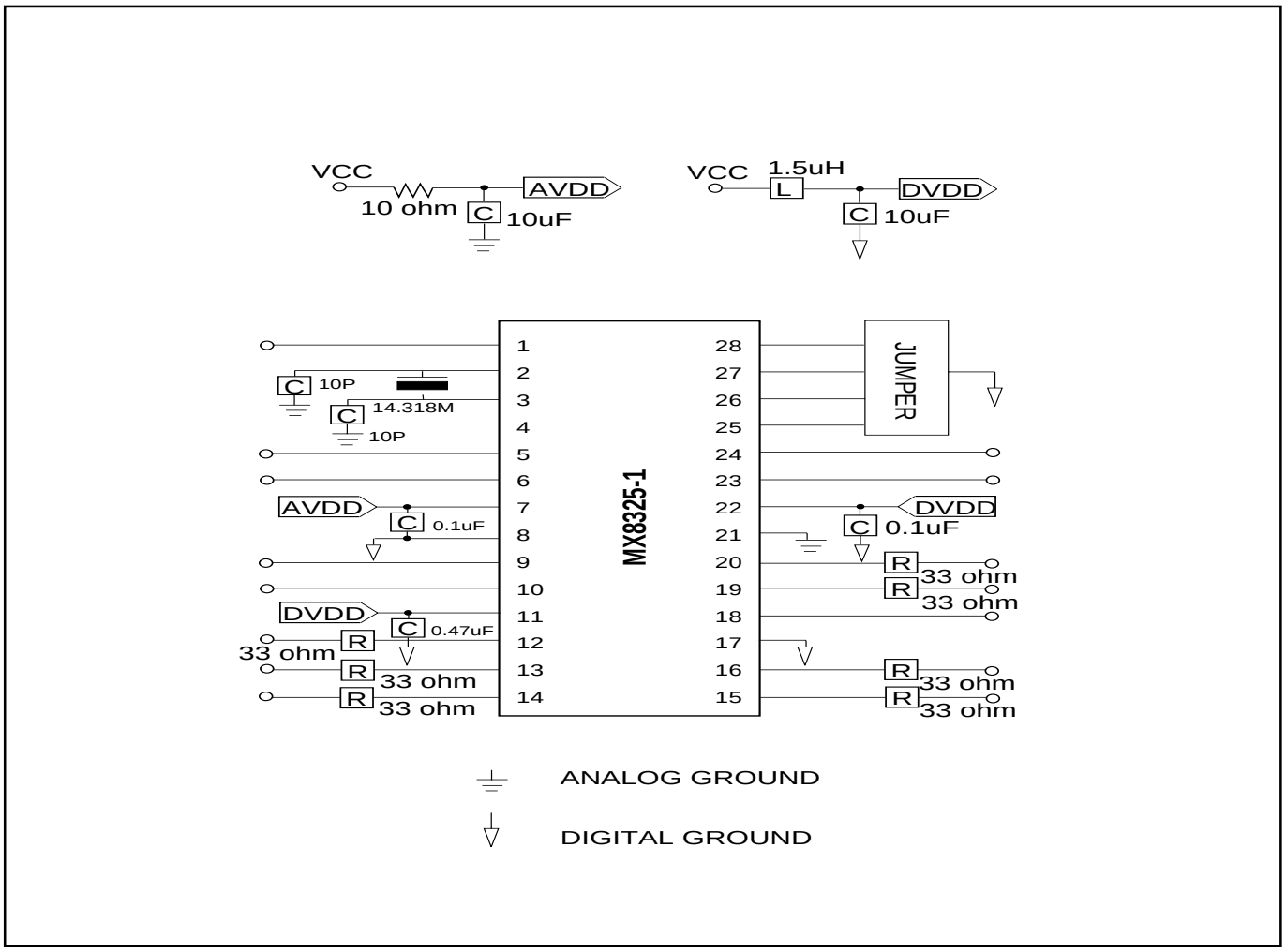


ORDERING INFORMATION

PLASTIC PACKAGE

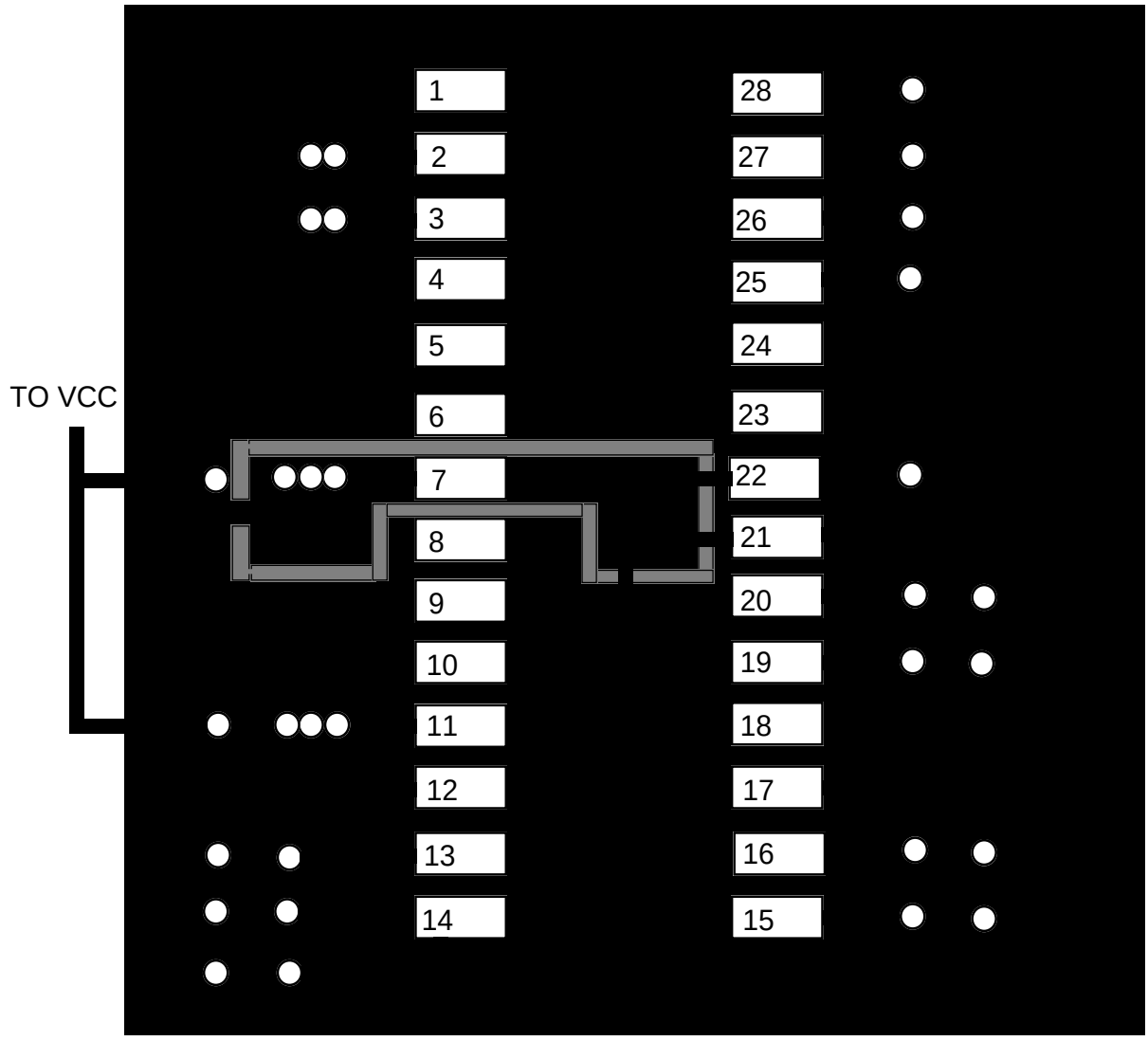
PART NO.	PACKAGE
MX8325-1MC	28-PIN SOP (5V Version)

RECOMMENDED EXTERNAL CIRCUIT



Note : 1. Pin26, pin27, pin28, and pin25 (S0, S1, S2, MS0) are with internal pull high resistor.
2. For 5V and 3.3V mixed application (MX8325-1). If DVDD(pin11 and pin22) is connected to 3.3V power source, and AVDD(pin7) is connected to 5V power source, then all outputs are 3.3V level.

LAYOUT GUIDE



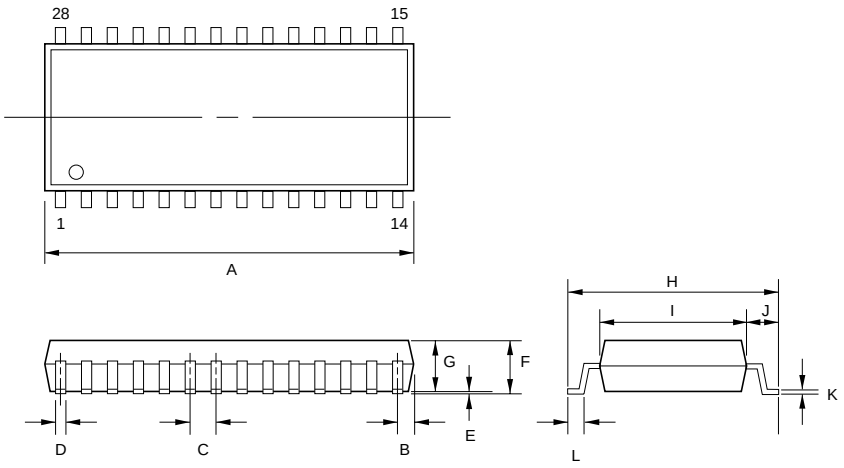
This is the recommended layout guide for the MX8325-1 to maximize the clock performance. The most important feature is the isolated ground plane of the MX8325-1.

The reason it needs an isolated ground plane is explained in the following paragraph. The power supply fluctuation induced from the ripple of switching power supply, and the switching between the heavy circuit activity and little circuit activity on the board will couple into the clock generators and appear as jitters on the clock outputs. To alleviate jitters, special care should be taken on the power source of clock generator to prevent the power source from interacting with the system noise.

28-PIN PLASTIC SOP (300 mil)

ITEM	MILLIMETERS	INCHES
A	17.83	0.702
B	0.66	0.026
C	1.27	0.050
D	0.41	0.061
E	0.20	0.008
F	2.54	0.1
G	2.34	0.092
H	10.31	0.406
I	7.59	0.299
J	1.35	0.053
K	0.25	0.010
L	0.76	0.030

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



MACRONIX INTERNATIONAL CO., LTD

HEADQUARTERS :
TEL : +886-3-578-8888
FAX : +886-3-578-8887

EUROPE OFFICE :
TEL : +32-2-456-8020
FAX : +32-2-456-8021

JAPAN OFFICE :
TEL : +81-44-246-9100
FAX : +81-44-246-9105

SINGAPORE OFFICE :
TEL : +65-747-2309
FAX : +65-748-4090

TAIPEI OFFICE :
TEL : +886-2-2509-3300
FAX : +886-2-2509-2200

MACRONIX AMERICA INC.
TEL : +1-408-453-8088
FAX : +1-408-453-8488

CHICAGO OFFICE :
TEL : +1-847-963-1900
FAX : +1-847-963-1909

http : //www.macronix.com