JUL 1992

MUSIC™ SEMICONDUCTORS

MU9C1880
24-BIT DIRECT COLOR GRAPHICS PALETTE

ADVANCE INFORMATION DRAFT

DISTINCTIVE CHARACTERISTICS

- Combination Look-up table and triple eight-bit Video DAC
- Displays 256 colors from a palette of 256K colors
- Adds 15-, 16-, and 24-bit Direct Color capability to standard VGA controllers
- Direct Color modes display 32K, 64K, or 16M colors
- Pixel-by-pixel mix of 256 Look-up table or 32K Direct colors
- Directly drives double-terminated 75-ohm transmission line
- VGA, Super-VGA, VESA, TIGA™ and 8514/A compatible with enhanced features
- Monitor Sense comparators detect monitor connection
- Setup and Sync for video monitor compatibility
- Asynchronous Microprocessor Interface
- Pixel Replicate™ suppresses display noise when Look-up Table or Mask register accessed during active display time
- Industry-standard 44-pin PLDCC package
- 90-MHz pixel rate
- High-performance CMOS for low power with TTL-compatible inputs

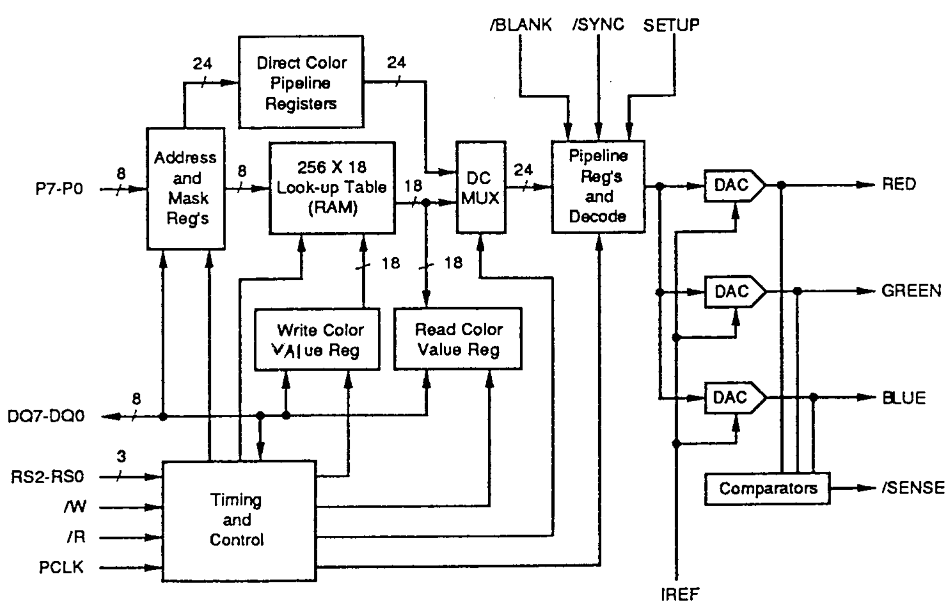
GENERAL DESCRIPTION

The MU9C1880 monolithic Graphics Color Palette includes a 256-word by 18-bit Look-up table, 24-bit Direct Color bypass, three eight-bit Video DACs, and Monitor Sense comparators. The VGA-compatible Look-up table accepts up to eight bits per pixel from a frame buffer and performs a translation into three six-bit values for conversion into Red, Green, and Blue analog signals. Each of the Video DACs can directly drive a double-terminated 75-ohm transmission line.

The MU9C1880 is fully compatible with VGA, Super-VGA, VESA, TIGA™ and 8514/A industry standards while providing many enhanced features. Direct Color operation bypasses the Look-up table to provide 16M (24-bit), 64K (16-bit XGA™), or 32K (15-bit TARGA™) displayable colors. Direct Color data is clocked on two or three consecutive rising edges of the pixel clock, making the MU9C1880 compatible with any VGA controller. Display of Pseudo-color and 15-bit Direct Color data within the same frame is supported. Sync pulses and a Set-up pedestal are available on all three outputs. Monitor Sense comparators permit the detection of color, monochrome, or no monitor connection. The MU9C1880 also incorporates a proprietary Pixel Replicate™ feature that allows Look-up table read and write operations to occur during the active portion of the display.

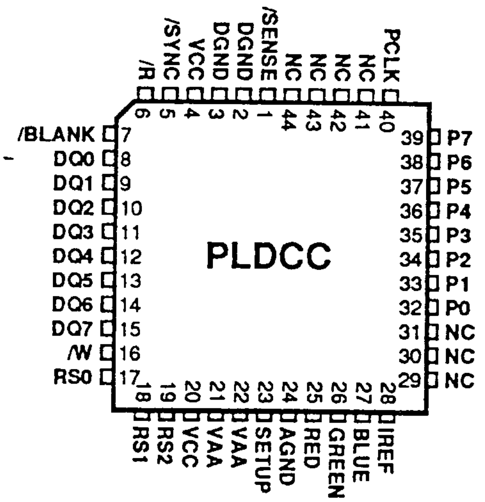
The MU9C1880 accesses its enhanced Direct Color features through an industry-standard key sequence, allowing standard VGA system designs to be upgraded. Available in a 44-pin PLDCC package, it supports the screen resolution and color capability necessary for high-performance Desktop Personal Computer and Desktop Publishing systems.

BLOCK DIAGRAM



June 19, 1992 Rev. 0

MU9C1880 PINOUT DIAGRAM



PIN DESCRIPTIONS

RED, GREEN, BLUE (Video Signal, Output, Analog)

These signals are the outputs of the three video DACs and are capable of driving a double- or single-terminated 75-Ω transmission line directly connected to a suitable monitor or video amplifier.

IREF (Reference Current, Input, Analog)

The IREF pin current sets the full scale output of the Video DACs. This pin must be driven by an external current sink providing a regulated current. This reference current, IREF, is determined by Equation [1], where VFS is the desired full scale DAC output, Ro is the DAC load resistance with a monitor attached, and K is a constant from Table 1.

$$I_{REF}\,[mA] = \frac{V_{FS}\,[mV]}{R_O\,[\Omega] \cdot K} \qquad [1]$$

Pedestal	K (without Sync)	K (with Sync)
0 IRE	2.100	3.008
7.5 IRE	2.270	3.178

Table 1: DAC Full Scale Constants

SETUP (Setup Control, Input, TTL)

The SETUP pin controls the Blanking pedestal. With the SETUP pin HIGH, the /BLANK pin switches a 7.5 IRE Blanking pedestal on and off. With the SETUP pin LOW, the Blanking pedestal is 0 IRE, and the Black Reference level and the Blanking level are the same. The SETUP pin must be connected either HIGH or LOW, and is connected to ground if the Setup function is not desired.

P7-P0 (Pixel Address, Input, TTL)

P7-P0 are the addresses used to reference a color value stored in the Look-up table or the direct DAC values used for conversion to analog video signals. Individual Pixel Address bits are ANDed with the corresponding Mask Register bits before being sent to the Look-up Table. P7-P0 are registered on the rising edge of PCLK. When operating in 15-bit Direct Color mode with the Mode Switch Enable bit (D4) in the Command register set to a logical one, P7 of Byte One (the Mode Switch bit) may be used to switch between Direct Color mode and Pseudo-color mode at pixel rates.

PCLK (Pixel Clock, Rising-edge-active Input, TTL)

The rising edge of PCLK registers the Pixel address (P7-P0) and the /BLANK and /SYNC inputs, transfers data in the internal pipeline, and internally synchronizes the Microprocessor Port signals. P7-P0 data is registered on the rising edge of PCLK. The Pixel Clock period corresponds to one pixel displayed on the monitor in Pseudo-color mode, two pixels in 15- and 16-bit Direct Color modes, and three pixels in 24-bit Direct Color mode.

/BLANK (Blank Control, Active-LOW Input, TTL)

The state of the /BLANK input is registered by the rising edge of PCLK. The /BLANK signal is used for blanking the display during retrace. When /BLANK is HIGH, the DAC outputs reflect their digital input values. When /BLANK is LOW, the DAC outputs are forced to the Blanking level to turn off any display during retrace. /BLANK has the same pipeline delay as P7-P0. In the Direct Color modes, the first PCLK rising edge that /BLANK is HIGH synchronizes the Red data (plus any programmed Red Byte shift) or Byte Zero, after which /BLANK is registered on the same rising edge of PCLK as the Red or Byte Zero data until /BLANK goes LOW again.

/SYNC (Sync Control, Active-LOW Input, TTL)

The state of the /SYNC input is registered by the rising edge of PCLK. The /SYNC signal controls the Sync pulses on the analog outputs. When /SYNC is HIGH, a 40 IRE (Setup = 7.5 IRE) or 43 IRE (Setup = 0 IRE) current source is added to the analog output; when /SYNC is LOW, the current source is switched off. /SYNC has the same pipeline delay as P7-P0. In Direct Color modes, /SYNC is captured on the same rising edge of PCLK as Red or Byte Zero data. Because /SYNC does not affect the /BLANK pin or the DAC input data, it should only be asserted when /BLANK is LOW. The /SYNC pin is grounded if Sync information is not required on the analog outputs.

/SENSE (Monitor Sense, Active-LOW Output, TTL)

The /SENSE pin is LOW if one or more of the Red, Green, or Blue outputs is higher than the internal 335-mV sense threshold.

/R (Read, Active-LOW Input, TTL)

A negative-going pulse on /R controls the DQ7-DQ0 Read cycle. RS2-RS0, registered on the falling edge of /R, determine

PIN DESCRIPTIONS (CONT'D)

the source of the Read Cycle data. The DQ7-DQ0 outputs become valid after the specified access time from the falling edge of /R. The DQ7-DQ0 outputs become high-impedance after the rising edge of /R.

/W (Write, Active-LOW Input, TTL)

A negative-going pulse on /W controls the DQ7-DQ0 Write cycle. RS2-RS0, registered on the falling edge of /W, determine the destination of the Write Cycle data. The DQ7-DQ0 data must meet set-up and hold times referenced to the rising edge of /W.

DQ7-DQ0 (Microprocessor Data Bus, I/O, Three-state TTL)

DQ7-DQ0 transfer data to and from the Microprocessor port. The Color Value registers use only the six low-order bits (DQ5-DQ0); all other registers use all eight bits.

RS2-RS0 (Register Select, Input, TTL)

The states of RS2-RS0 at the beginning of a Microprocessor Port cycle determine the register to be read or written during that cycle as shown in Table 3-6. The beginning of the cycle is initiated by the falling edge of either /R or /W, depending on the type of cycle.

VAA (Analog Power Supply)
AGND (Analog Ground)

The VAA and AGND pins provide the positive power supply and ground, respectively, for the analog portions of the device. They are separated from the VCC and DGND digital supplies to enhance noise margins. VAA and VCC should be tied to the same power plane, and AGND and DGND should be tied to the same ground plane, with appropriate care taken to minimize noise.

VCC (Digital Power Supply)
DGND (Digital Ground)

The VCC and DGND pins provide the positive power supply and ground, respectively, for the digital portions of the device. They are separated from the VAA and AGND analog supplies to enhance noise margins. VAA and VCC should be tied to the same power plane, and AGND and DGND should be tied to the same ground plane, with appropriate care taken to minimize noise.

FUNCTIONAL DESCRIPTION

OPERATIONAL CHARACTERISTICS

The MU9C1880 includes a Video port, Address logic, a 256-word by 18-bit Look-up table (RAM), registers and multiplexers to bypass the Look-up table for Direct Color operation, three eight-bit Video DACs, Monitor Sense comparators, and the logic needed for a Microprocessor interface to access the Mask register, Look-up table and control functions.

Video Port Operation

The Video port includes the Pixel Address (P7-P0), /BLANK, /SYNC, and PCLK pins. The four operational modes are shown in Table 2. The video data is sent to three eight-bit Video DACs, each capable of driving a double-terminated 75-ohm transmission line (75-ohm termination at both ends of the line).

Pseudo-color Mode

Pseudo-color mode provides VGA-compatible Look-up Table operation. P7-P0 are registered on the rising edge of PCLK by the Pixel register. P7-P0 are ANDed with the Mask register, then passed on to the Look-up table RAM as an address. The 18-bit content of this address is transferred to the six MSBs of the three eight-bit Video DACs (the two LSBs are set to zero). Pseudo-color mode is enabled upon power-up and whenever D7 in the Command register is set to zero. The pipeline delay in this mode is four registers (three PCLK cycles).

Command Register								Mode
D7	D6	D5	D4	D3	D2	D1	D0	
0	X	X	X	X	X	X	X	Pseudo-Color
1	0	1	X*	0	0	0	0	15-bit Direct Color (TARGA)
1	0	1	0	0	1	1	0	16-bit Direct Color (XGA)
1	X	0	1	1	1	1	X	24-bit Direct Color

* 0 = Pixel Mode Switch Bit Disabled
1 = Pixel Mode Switch Bit Enabled

Table 2: Operational Modes

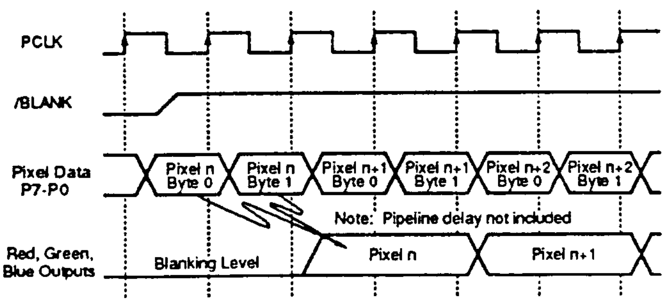


Figure 1: 15- and 16-bit Direct Color Modes

15- and 16-bit Direct Color Modes

The 15- and 16-bit Direct Color modes are enabled by the Command register codes shown in Table 2. These modes, shown in Figure 1, use two PCLK cycles per Direct Color pixel. The multiplexed Pixel Bus data is synchronized by the rising edge of /BLANK: Byte Zero is registered on the first rising edge of PCLK that /BLANK is HIGH, and Byte One is registered on the next rising edge of PCLK. Byte Zero and Byte One continue to alternate on successive rising edges of PCLK until /BLANK goes LOW again. The internal pipeline and the DAC inputs are clocked on the same rising edge of PCLK that registers the

FUNCTIONAL DESCRIPTION (CONT'D)

Pixel Bus	15-bit Byte Zero	15-bit Byte One	16-bit Byte Zero	16-bit Byte One	24-bit Red Byte	24-bit Green Byte	24-bit Blue Byte
P7	G5	Mode*	G4	R7	R7	G7	B7
P6	G4	R7	G3	R6	R6	G6	B6
P5	G3	R6	G2	R5	R5	G5	B5
P4	B7	R5	B7	R4	R4	G4	B4
P3	B6	R4	B6	R3	R3	G3	B3
P2	B5	R3	B5	G7	R2	G2	B2
P1	B4	G7	B4	G6	R1	G1	B1
P0	B3	G6	B3	G5	R0	G0	B0

Rn, Gn and Bn refer to Red, Green and Blue DAC Inputs
(e.g., R7 is the MSB of the Red DAC)
* Pixel Mode Switch Bit

Table 3: Direct Color Pixel Bus Mappings

Byte Zero data; therefore, one pixel is displayed every two PCLK cycles. The pipeline delay is four PCLK cycles.

Table 3 and Table 4 show the relationship between P7-P0 and the inputs of the three DACs for all mappings. The 15-bit Direct Color mode (32K colors) allows any pixel to be either Direct Color or Pseudo-color. This feature is enabled when D4 in the Command register is a logical one. If the Pixel Mode Switch bit (P7 in Byte One) is HIGH, the Look-up Table output data (including address masking) is selected for the Video DACs, otherwise the Direct Color data is selected. Pseudo-color and Direct Color pixels are displayed at the same pixel size and resolution. If D4 in the Command register is a logical zero, all pixels are displayed as Direct Color data independent of state of the Pixel Mode Switch bit, permitting the display of 15-bit Direct Color images that may not have had the 16th bit set to a known state.

24-bit Direct Color Mode

The 24-bit Direct Color mode is enabled by the Command register code shown in Table 2. In this mode, three bytes are read from P7-P0 for every pixel, as shown in Figure 2. The multiplexed Pixel Bus data is synchronized by the rising edge of /BLANK: the Red byte is registered on the first rising edge of PCLK that /BLANK is HIGH (assuming that the Red Byte shift is zero; see below), the Green byte is registered on the next rising edge of PCLK, and the Blue byte on the following rising

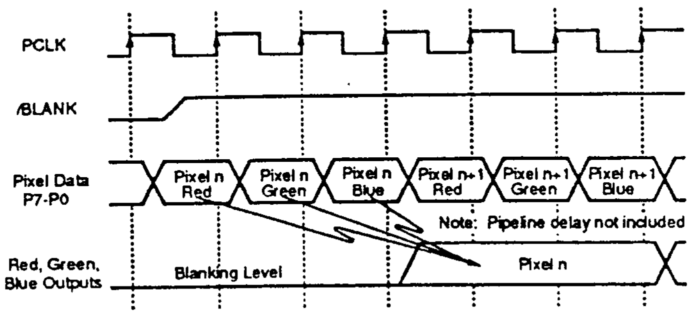


Figure 2: 24-bit Direct Color Mode

edge of PCLK. The Red, Green, and Blue bytes continue in sequence on successive PCLK rising edges until /BLANK goes LOW again. The internal pipeline and the DAC inputs are clocked on the same PCLK rising edge that registers the Red data; therefore, one pixel is displayed every three PCLK cycles. The pipeline delay is six PCLK cycles.

When displaying an overscan border (/BLANK is HIGH and the controller outputs the Overscan register value), the overscan length may cause improper registration of 24-bit Direct Color data. To compensate, the MU9C1880 allows the Red byte position to be shifted one or two PCLK cycles after the first PCLK cycle that /BLANK is HIGH. The shift is set by D6 and D0 in the Command register, as shown in Table 5. With no shift (zero PCLK cycles), the Red byte is registered as explained above and shown in Figure 2. With a shift of one or two PCLK cycles, the Red byte is registered on the second or third PCLK cycle that /BLANK is HIGH, and then every third PCLK cycle thereafter. The DAC outputs are held at the Blanking level for the one or two extra PCLK cycles (after the normal pipeline

Command Register D6	Command Register D0	Red Byte Shift
0	0	0 PCLK cycles
0	1	1 PCLK cycle
1	0	2 PCLK cycles
1	1	Reserved

Table 5: Red Byte Position Shift

DAC Input	Red 15-bit	Red 16-bit	Red 24-bit	Green 15-bit	Green 16-bit	Green 24-bit	Blue 15-bit	Blue 16-bit	Blue 24-bit
7 (MSB)	B1-P6	B1-P7	R-P7	B1-P1	B1-P2	G-P7	B0-P4	B0-P4	B-P7
6	B1-P5	B1-P6	R-P6	B1-P0	B1-P1	G-P6	B0-P3	B0-P3	B-P6
5	B1-P4	B1-P5	R-P5	B0-P7	B1-P0	G-P5	B0-P2	B0-P2	B-P5
4	B1-P3	B1-P4	R-P4	B0-P6	B0-P7	G-P4	B0-P1	B0-P1	B-P4
3	B1-P2	B1-P3	R-P3	B0-P5	B0-P6	G-P3	B0-P0	B0-P0	B-P3
2	0	0	R-P2	0	B0-P5	G-P2	0	0	B-P2
1	0	0	R-P1	0	0	G-P1	0	0	B-P1
0 (LSB)	0	0	R-P0	0	0	G-P0	0	0	B-P0

B0/B1 -- Byte Zero/Byte One for 15- and 16-bit Direct Color Mode
R/G/B -- Red/Green/Blue Byte for 24-bit Direct Color Mode
(e.g.; B1-P6: P6 bit of Byte One; R-P7: P7 of Red Byte)

Table 4: Direct Color DAC Input Mappings

FUNCTIONAL DESCRIPTION (CONT'D)

delay). When /BLANK goes LOW again, all data for the last pixel is properly registered and displayed even if /BLANK is LOW for the Green or Blue byte; the DAC outputs go to the Blanking level only after the last pixel has been displayed for all three PCLK cycles.

/BLANK, SETUP, and /SYNC

The /BLANK (active LOW) input blanks the display during retrace. A LOW level on /BLANK forces the analog outputs to the Blanking level without reference to the data at the DAC inputs. A HIGH level on /BLANK allows the DAC inputs to be converted to analog levels. After being LOW, the first PCLK cycle that /BLANK is HIGH synchronizes the Direct Color mode data.

The Setup pedestal provides a separation between the Blanking level and the Black Reference level, and is selected by the SETUP pin. When the SETUP pin is LOW, the Setup pedestal is 0 IRE and the Blanking level is the same as the Black Reference level. When the SETUP pin is HIGH, the Black and Blanking levels are separated by 7.5 IRE.

The /SYNC (active LOW) input adds composite Sync information to the video outputs. A LOW level on /SYNC turns off a current pedestal, creating a negative Sync pulse. A HIGH level on /SYNC turns on the pedestal and establishes the Blanking level. The Setup current and DAC bit currents are added to this pedestal. /SYNC does not affect any other inputs, and should only be exercised when /BLANK is LOW.

The Sync pedestal is 40 IRE when Setup = 7.5 IRE as established by the NTSC standard. When Setup = 0 IRE, the Sync pedestal is within the tolerance of the 43 IRE Sync pedestal required by the PAL and SECAM standards.

The /BLANK and /SYNC pins are registered on the rising edge of PCLK. For the Direct Color modes, they are registered on the same PCLK cycle as Byte Zero or Red data. The pipeline delays for /BLANK and /SYNC are identical to the delay for P7-P0 for each mode.

Monitor Sense Comparators

The Monitor Sense comparators test the output voltage level against an internally derived 335-mV threshold. The /SENSE output goes LOW if any output exceeds the threshold voltage. The /SENSE output may be read by the host processor, typically through a controller pin dedicated to this purpose. Monitor Sense may be used to detect the presence or absence of color or monochrome monitors or to perform diagnostics. The /SENSE pin should only be read when the DAC outputs are in a predictable state. Note that the /SENSE output may toggle when exercising the /SYNC pin.

Microprocessor Port Operation

The Microprocessor port provides read and write access to the Look-up table's RAM array (256 words of 18 bits), the Mask register, the read-only ID register, and the Command register. Although the external operations of the Video port and Microprocessor port are asynchronous, Microprocessor port

RS2	RS1	RS0	Register
0	0	0	Address Register (RAM Write)
0	0	1	RAM Color Value
0	1	0	Pixel Mask /ID Register†
0	1	1	Address Register (RAM Read)
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Command Register*
1	1	1	Reserved

* Command Register also accessed after four Read cycles to Pixel Mask Register.

† ID register accessed on fourth consecutive Read cycle to Pixel Mask Register.

Table 6: Register Access

transactions destined for the Look-up Table RAM or the Mask register are internally synchronized by PCLK such that only one video cycle is interrupted for each 18-bit read or write of the Look-up table. To avoid noise on the display during this operation, the color data from the previous pixel is repeated (replicated) at the DAC outputs. This Pixel Replicate™ feature allows Look-up Table or Mask register access during the active portion of the display.

INTERNAL REGISTERS

Any internal register listed in Table 6 may be read or written through the Microprocessor port. All registers are a single byte and are read or written in a single Microprocessor Port cycle, except for the RAM Color Value registers which require three Microprocessor Port cycles.

For a Microprocessor Port Write cycle, the states of RS2-RS0 are first set to the desired value. The falling edge of /W registers the state of RS2-RS0. The Microprocessor Data bus signals (DQ7-DQ0) are registered on the rising edge of /W for transfer to the proper byte of the selected register.
When writing to the Look-up Table, the Address register is first initialized by a Write cycle to RS2-0 = 0H. After three bytes have been written to the Color Value Write register, data is transferred to the Look-up Table RAM at the specified address. The Address register is then incremented in anticipation of writing to the next location, allowing sequential blocks of registers to be written.

For a Microprocessor Port Read cycle, RS2-RS0 are set to the desired value and registered on the falling edge of /R. The output data is placed on DQ7-DQ0 until after the rising edge of /R, resulting in the data bus resuming a high-impedance state.

When reading from the Look-up Table, the Address register is initialized with a Write cycle to RS2-0 = 3H. At this point, data is transferred from the selected address to the Color Value Read register, and then the Address register is incremented. After three bytes have been read from the Color Value Read register, data is again transferred from the location selected by the Address register (now pointing to the next address), and the address register is again incremented in anticipation of the next read, allowing sequential blocks of registers to be read.

FUNCTIONAL DESCRIPTION (CONT'D)

	D7	D6	D5	D4	D3	D2	D1	D0
	Direct Color Enable	**Red Byte Position Shift 1**	**Mode Select**	**Mode Switch Enable**	**Mode Select**			**Red Byte Position Shift 0**
0	***P-color***	***0***	***0***	***Disable***	***0***	***0***	***0***	***0***
1	D-color	1	1	Enable	1	1	1	1

Power-on initialized state in ***Bold-italic***

Table 7: Command Register Bit Assignments

(Note: The Bit Assignment table indicates the function or value of each bit when programmed to the state indicated at the left-hand edge of the table. D7 is read and written on DQ7; D0 is read and written on DQ0.)

Mask Register

The eight-bit Mask register allows manipulation of the Pixel addresses. P7-P0 are bit-wise logically ANDed with the contents of this register before being sent to the Look-up table as an address. If the Mask register contains the byte value FFH, then the state of P7-P0 is unaltered. If the Mask register contains 00H, then the Look-up table will be passed 00H. The masking of individual bits may be used to create animation effects on the screen. Mask register operations are internally synchronized to PCLK, allowing unlimited read and write access during any portion of the display.

Address Register

The eight-bit Address register is accessed through one of two register select addresses depending upon the desired action. Separate addresses are provided for reading and writing color values. The Address register auto-increments to allow sequential block transfers of color values without re-programming the Address register.

RAM Color Value

The RAM color values are written through the Write Color Value register (18 bits) and read through the Read Color Value register (18 bits) in three Read or Write cycles. The RAM address of the accessed color value is determined by the Address register. The DQ5-DQ0 pins transfer the six-bit Red field on the first Microprocessor port cycle, the six-bit Green field on the second cycle and the six-bit Blue field on the third. DQ5 corresponds to the DAC MSB, and DQ0 to the LSB. Sequential blocks of color values may be transferred without re-programming the Address register.

Command Register

The Command register (see Table 7) controls the Direct Color features of the MU9C1880. There are two ways to read or write the Command register. The Command register may be directly accessed by setting RS2-0 = 6H. Since some controllers do not support the RS2 pin, the Command register may also be accessed by a key sequence consisting of four consecutive reads of the Mask register address (RS2-0 = 2H; note that the fourth read returns the ID register); the next read or write cycle to the Mask Register address will access the Command register. The Command register continues to be accessible after a read, but not after a write. Any interruption of the key sequence, such as reading a different register or writing any register, will reset an internal access-enable counter, and the key sequence must be restarted from the beginning. After reading the Command register, the access-enable counter should be reset by reading another register unless further access to the Command register is required.

ID Register

The read-only ID register reads back 8EH for the MU9C1880. It may be read from DQ7-DQ0 on the fourth consecutive read from the Pixel Mask Register address. The ID register will always contain both ones and zeroes. After reading the ID register, a read cycle of the Address register should be executed to prevent accidental access of the Command register unless such access is also desired.

APPLICATIONS

SYSTEM APPLICATIONS

The VGA-compatible Look-up table of the MU9C1880 can display up to 256 colors at a time. Each of these colors can be any combination of 64 levels each of Red, Green and Blue. Bypassing the Look-up table allows the display of 32K, 64K, or 16M colors at a time. As a result, color digitized images will look more realistic and the cartoon-like quality that results from limited numbers of colors will be eliminated, making the MU9C1880 particularly well suited to color desk-top publishing and video image-processing applications. Although 15- and 16-bit Direct Color modes do not use the full capability of the eight-bit DACs, it allows the display of a wide range of colors at 800 by 600 pixels with a 1 MB frame buffer. 24-bit Direct Color mode allows color shaded objects to be realistically displayed at resolutions up to 640 by 480 with a 1 MB frame buffer.

When driving analog monochrome (grey-scale) displays, only one DAC output is connected to the single video input of the monitor. The other DAC outputs must be terminated with the equivalent of a single- or double-terminated 75-Ω transmission line (37.5- to 75-Ω resistive load to ground) or tied directly to AGND. If the video frame buffer information is intended to be displayed on a color monitor, the Look-up table can be reprogrammed to provide only the intensity portion of the color information. This technique allows the display of a digitized color frame in monochrome.

The Look-up table also allows pseudo-color image processing techniques, such as density slicing, to be easily implemented on monochrome digitized images. Density slicing is a technique that assigns each grey-scale level in a monochrome image a unique color for display. Small differences in intensity (one bit of the grey scale) are difficult for the eye to differentiate in monochrome, but become readily apparent when assigned unique colors. By changing only the contents of the Look-up table, the displayed image can be transformed from monochrome into color.

CHANGING COLOR MODES

Direct Color modes are enabled by setting the Command register to one of the codes in Table 2, either by a direct write with RS2-0 = 6H or a key sequence. Since this operation would typically be controlled by the host processor at speeds much slower that the video display rate, mode changes are typically done during a blanking interval when /BLANK is LOW.

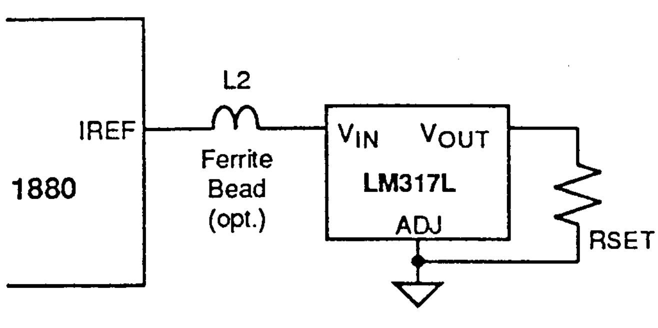


Figure 3: Typical Current Reference

If D4 in the Command register is set to a logical one, 15-bit Direct Color mode can change between Direct Color and Pseudo-color data from pixel to pixel. These changes are controlled through the Video port by the Pixel Mode Switch bit (P7 of Byte One). If the Pixel Mode Switch bit is HIGH, Byte Zero is used as a Look-up Table address (including masking by the Mask register) for a Pseudo-color pixel. If the Pixel Mode Switch bit is LOW, Byte Zero is combined with Byte One to form a Direct Color pixel.

OVERSCAN BORDERS

The MU9C1880 may be used with overscan borders, even in 24-bit Direct Color mode. The overscan border is the area between the bezel and the graphics display area. This border is typically black, and /BLANK is programmed to be LOW until the start of the graphics display area. Most VGA controllers can change the overscan border by programming a color in the Overscan register and setting the width of the border in eight-bit "characters." In 24-bit Direct Color mode, the width of the border in pixels (from /BLANK going HIGH to the start of the graphics display area) may not be divisible by three. If this is the case, the Red Byte shift (D6 and D0 in the Command register) must be used to offset the position of the Red byte one or two PCLK cycles relative to the first PCLK cycle that /BLANK is HIGH, thereby adjusting the MU9C1880's internal logic to match the data stream from the controller. The Red Byte shift also adjusts the DAC blanking, so that all pixels (including overscan pixels) are displayed properly.

Since the controller outputs the same byte for every PCLK cycle of the overscan border, the choices for the border color are limited for the Direct Color modes. In 24-bit Direct Color mode, the Red, Green and Blue values are the same, giving 256 shades of grey from Black to White as possible border colors. 15-bit Direct Color (without the Mode Switch bit) and 16-bit Direct Color modes have a wider range of color choices, limited by the requirement that Byte Zero and Byte One must have the same value. 15-bit Direct Color mode may have a border of any of the 262,144 possible Look-up Table colors by using the Mode Switch bit (P7 in Byte One); the overscan register is set to the address of the Look-up Table (from 80H to FFH) that contains the desired color.

DAC REFERENCE

The MU9C1880 requires an external current sink to set the DAC output levels. Such a reference can easily be built from a minimum of low-cost components, as shown in Figure 3. Better results are obtained if IREF is not capacitively bypassed to VAA; in fact a ferrite bead (L2 in Figure 3) between the IREF pin and the current regulator can reduce high-frequency current variations, and is recommended in noisy environments.

The DAC Reference constants in Table 1 reflect the values for Pseudo-color mode, when only six DAC bits are used. In 15-bit Direct Color mode, the grey scale portion (White to Black) of all three DAC outputs will be 1.6 % lower than Pseudo-color mode. In 16-bit Direct Color mode, the full grey scale output of the Red and Blue DACs will be 1.6 % lower than the Green DAC with all bits on. For 24-bit Direct Color mode, the DAC grey scale will be 1.2 % higher than for Pseudo-color mode.

APPLICATIONS (CONT'D)

PC LAYOUT GUIDELINES

The MU9C1880 must receive power from a noise-free, low-impedance power distribution system. The use of VCC and ground planes is highly recommended. Since one side of the package has the digital supplies (VCC and DGND) and opposite side has the analog supplies (VAA and AGND), high quality 0.01-µF and 100-pF high-frequency ceramic bypass capacitors should be placed on both sides of the package. For maximum PCLK frequencies lower than 30 MHz, 0.1-µF and 1000-pF capacitors should be used instead. In addition, a 4.7-µF tantalum electrolytic capacitor should be placed nearby to help filter low frequency noise. The other TTL and CMOS devices on the PCB should also be capacitively bypassed.

A separate power distribution network is recommended for the MU9C1880 color palettes to ensure a noise-free power supply. One approach is to provide separate power and ground planes for the color palette and its associated analog circuitry, as shown in Figure 4. The separate analog power plane is isolated from the PCB's digital logic supplies by a ferrite bead (L1) and is connected to the VCC and VAA pins on the color palette. A 4.7-µF tantalum electrolytic capacitor to ground (C3) filters low-frequency noise. C2a consists of a pair of ceramic capacitors, as described above, located near VAA and AGND to bypass the analog power and ground pins. C2b is similarly constructed and placed near VCC and DGND to bypass the digital power and ground pins. The analog ground plane isolates digital ground currents from the analog components, and should be separated from the digital ground plane by at least a 1/8-inch (3-mm) gap. The two ground planes should be connected together at a single point (preferably near the PCB's ground connection) by a wide, low-impedance path.

The signal lines connected to the P7-P0, /BLANK, /SYNC, and PCLK inputs must be either very short or terminated to eliminate the possibility of ringing or undershoot that might affect critical timing parameters. The traces for these signals should be led over the digital ground plane and avoid the analog power and ground planes. This device is fabricated in CMOS technology with high-impedance inputs that may not clamp to ground.

To reduce noise, traces connecting external IREF and DAC output circuitry should only be run over the analog ground plane, and should be kept as short as possible. If the distance from the DAC outputs to the Video connector cannot be kept extremely short, the connecting traces should be constructed as 75-Ω microstrip transmission lines. In general, this constraint implies wider traces, but the exact dimensions must be calculated from the board material and construction.

DEVICE HANDLING AND PROTECTION

CMOS devices are subject to a condition known as latch-up. Latch-up can occur when parasitic four-layer devices similar to SCRs are turned on, typically leading to excessive current flow from VCC to ground. If left to continue, this current may cause the bond wires to open and the device to fail catastrophically. Although steps are taken during design to minimize a product's sensitivity to latch-up, additional precautions should be taken by the user. Digital signals that go directly off the board should be terminated with either a 47-Ω series resistor or a 1-KΩ resistor to DGND. If a 1-KΩ resistor to DGND is used, be sure that the output driver connected to that node can pull the inputs above VIH(min) (typically 2.4 mA source current per 1-KΩ pull-down resistor). Either method will greatly increase the latch-up threshold, as well as reduce EMI radiation (which will aid in meeting FCC standards for radiated noise) and improve Electro-static Discharge (ESD) damage protection.

CMOS devices are subject to damage from ESD. To avoid permanent damage from high-energy electrostatic fields, always follow proper handling procedures. Store unused devices in conductive foam, carriers, or tubes. Devices should be handled only at ESD protected workstations (grounded floor mat and work surface) while wearing a grounded wrist strap and anti-static smock. Never insert devices into powered sockets or insert circuit boards into powered edge-connectors.

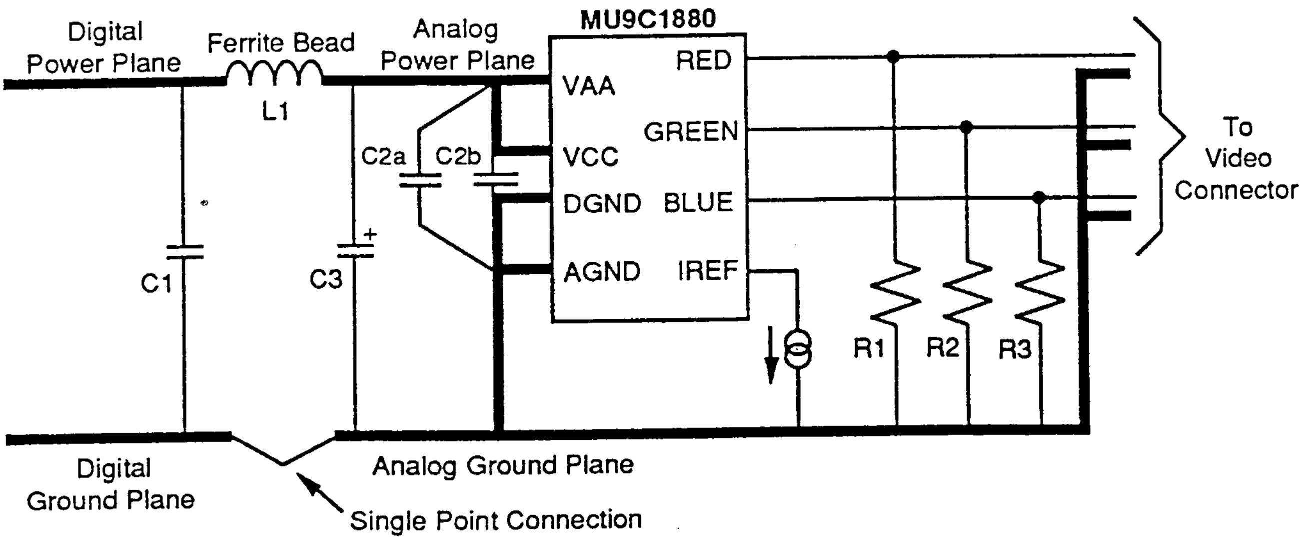


Figure 4: Typical Connection Diagram

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.5 to 7.0 volts
Voltage on all Other Pins	-0.5 to VCC+0.5 Volts (-2.0 Volts for 10 ns at the 50% point; see Figure 8)
Temperature Under Bias	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Maximum Reference Current Magnitude	15 mA
Maximum DAC Output Current Magnitude	50 mA (per Output)
Maximum DC TTL Output Current Magnitude	20 mA (per Output, one at a time, one second duration)

Stresses exceeding the Absolute Maximum Ratings may induce failure. Exposure to absolute maximum ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

All voltages are referenced to DGND.

OPERATING CONDITIONS
(voltages referenced to DGND at the device pins)

Symbol	Parameter	Min	Typical	Max	Units	Notes
V_{CC}	Operating Supply Voltage	4.5	5.0	5.5	Volts	
V_{IH}	Input Voltage Logic "1"	2.0		V_{CC}+0.5	Volts	
V_{IL}	Input Voltage Logic "0"	-0.5		0.8	Volts	-1.0 Volts for 10 ns measured @ 50% amplitude (Fig. 8)
I_{REF}	Reference Current Magnitude	3.5	8.89	10	mA	11
T_A	Ambient Operating Temperature	0		70	°C	Still Air

ELECTRICAL CHARACTERISTICS
(over the Operating Temperature and Voltage ranges)

Symbol	Parameter	Min	Typ	Max	Units	Notes
I_{CC}	Avg. Power Supply Current		120	145	mA	PCLK=90 MHz; 1
V_{TH}	Monitor Sense Comparator Threshold	300	335	370	mV	
V_{OH}	Output Voltage Logic "1"	2.4			Volts	I_{OH}=-5.0 mA
V_{OL}	Output Voltage Logic "0"			0.4	Volts	I_{OL}=5.0 mA
I_{ILK}	Input Leakage Current	-2		2	µA	$V_{DGND} \leq V_{IN} \leq V_{CC}$
I_{OLK}	Leakage Current (DQ7-DQ0)	-10		10	µA	$V_{DGND} \leq V_{IN} \leq V_{CC}$/R≥$V_{IH}$(min)

 DRAFT

ELECTRICAL CHARACTERISTICS (CONT'D)

DAC Parameter Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{IREF}	Voltage on IREF	V_{CC}-3.0		V_{CC}	Volts	11; 3.5 mA≤I_{REF}≤10.0 mA
V_O MAX	Max. Output Voltage			1.5	Volts	10,11; I_O≤20 mA
I_O MAX	Max. Output Current	31			mA	12; V_O≤1.25 Volts
I_{GS}	Grey Scale Current	17.73	18.67	19.60	mA	11; I_{REF} = 8.89 mA
I_{SET}	Setup Current (Blank to Black) Setup = 7.5 IRE Setup = 0 IRE	 1.43 0	 1.51 5	 1.59 50	 mA µA	11; I_{REF} = 8.89 mA
I_{SYNC}	Sync Current (Sync to Blank) /SYNC HIGH /SYNC LOW	 7.66 0	 8.07 5	 8.47 50	 mA µA	11; I_{REF} = 8.89 mA
	Resolution	6 8			bits bits	Pseudo-color Mode 24-bit Direct Color Mode
	Analog Output Full Scale Error			±5	%	2; Ext. I_{REF} = -8.89 mA
	Analog Output Matching			0.5	%	3; measured at I_O =Sync, Blank, Black and White levels
	Integral Nonlinearity			±0.5	LSB	4
	Rise Time (DAC Output)			6	ns	6; 10% to 90%; Load as shown in Fig. 5
	Full Scale Settling Time			12.5	ns	5,6; Load as shown in Fig. 5
	Glitch Energy			40	pV-sec	6; Load as shown in Fig. 5

CAPACITANCE

T_A = 0 to 70 °C; V_{CC} = 5.0 V ± 10%; f = 1.0 MHz

Symbol	Parameter	Max	Notes
C_I	Digital Input	7 pF	6; /R, /W, RS2-0, SETUP, P7-0, PCLK, /BLANK, /SYNC
C_O	Digital Output	7 pF	6; DQ7-0, /SENSE
C_{OA}	Analog Output	TBD pF	6, 9; RED, GREEN, BLUE

SWITCHING TEST CIRCUITS

Figure 5: DAC Switching Test Load

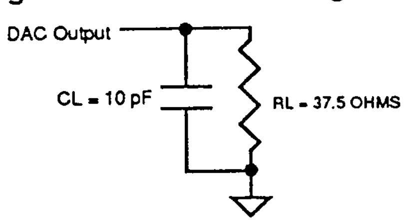


Figure 6: TTL Switching Test Load

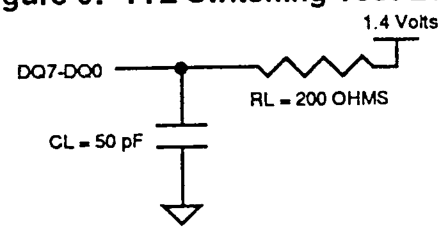


Figure 7: TTL Three-state Test Load

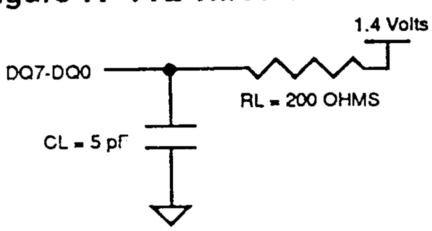
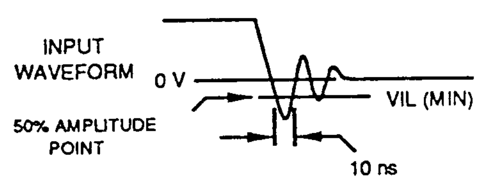


Figure 8: V_{IL} Waveform



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SWITCHING CHARACTERISTICS

AC TEST CONDITIONS

Input Signal Transitions	0.0 to 3.0 Volts
Video Port Signal Rise and Fall Times	≤ 2 ns
Microprocessor Port Signal Rise and Fall Times	≤ 3 ns
Digital Input Timing Reference Level	1.5 Volts
Digital Output Timing Reference Levels	0.8 V and 2.4 V
DAC Switching Test Load	Figure 7
TTL Switching Test Load	Figure 8

VIDEO PORT
Pseudo-color and 15-, 16-, and 24-bit Direct Color Modes

			-90			
No.	Symbol	Parameter	Min	Max	Units	Notes
	f_{MAX}	PCLK Frequency		90	MHz	
1	t_{CHCH}	PCLK Period	11		ns	
2	t_{CLCH}	PCLK LOW	4		ns	
3	t_{CHCL}	PCLK HIGH	4		ns	
4	t_{PVCH}	P7-P0, /BLANK and /SYNC Setup to PCLK HIGH	3		ns	
5	t_{CHPX}	P7-P0, /BLANK, and /SYNC Hold from PCLK HIGH	3		ns	
6	t_{CHAV}	PCLK to DAC Valid	0	25	ns	7,12
6a	Δt_{CHAV}	DAC to DAC Skew		1	ns	6,7
7	t_{AVQV}	DAC Valid to /SENSE Valid		1	µs	6
8	t_{GLGH}	/BLANK LOW	12 x t_{CHCH}		ns	13

MICROPROCESSOR PORT READ CYCLE

			-90			
No.	Symbol	Parameter	Min	Max	Units	Notes
9	t_{RLRH}	Read Pulse Width	50		ns	
10	t_{RHRL1}	Successive Read Interval	3 X t_{CHCH}		ns	
11	t_{RHWL1}	Read to Write	3 X t_{CHCH}		ns	
12	t_{RHRL2}	Color Read to Read	6 X t_{CHCH}		ns	
13	t_{RHWL2}	Color Read to Write	6 X t_{CHCH}		ns	
14	t_{SVRL}	Register Select Setup to /R LOW	10		ns	
15	t_{RLSX}	Register Select Hold from /R LOW	3		ns	
16	t_{RLQV}	Data Access from /R LOW		40	ns	
17	t_{RLQX}	Output Turn-on from /R LOW	3		ns	8
18	t_{RHQX}	Data Hold from /R HIGH	3		ns	
19	t_{RHQZ}	Data Three-state Delay from /R HIGH		20	ns	8

SWITCHING CHARACTERISTICS (CONT'D)

MICROPROCESSOR PORT WRITE CYCLE

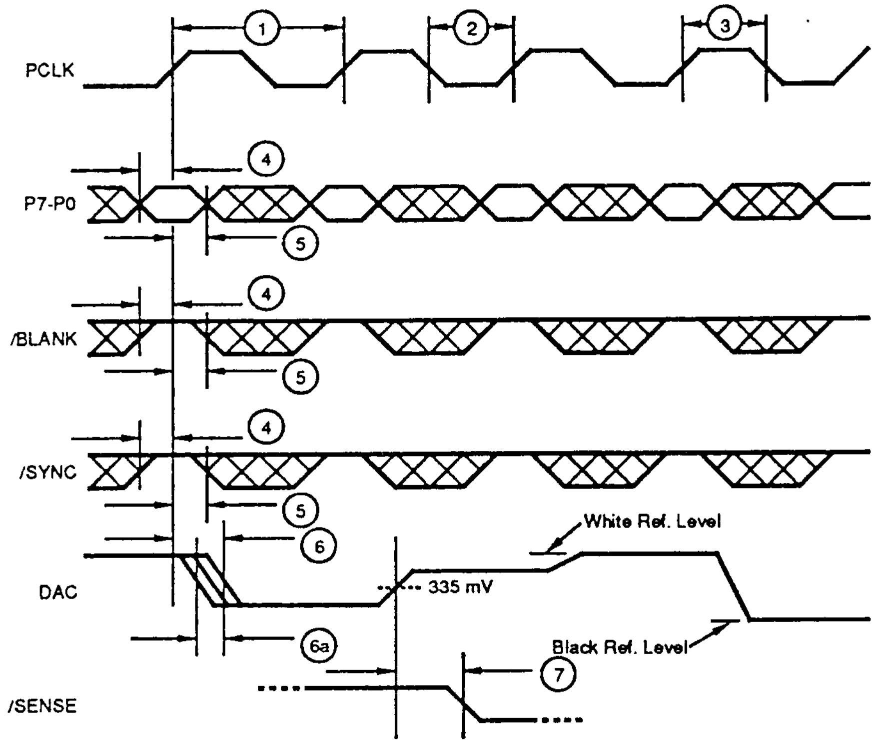
No.	Symbol	Parameter	-90 Min	-90 Max	Units	Notes
20	t_{WLWH}	Write Pulse Width	50		ns	
21	t_{WHWL1}	Successive Write Interval	3 X t_{CHCH}		ns	
22	t_{WHWL2}	Write after Color Write	3 X t_{CHCH}		ns	
23	t_{WHRL1}	Write to Read	3 X t_{CHCH}		ns	
24	t_{WHRL2}	Color Write to Read	3 X t_{CHCH}		ns	
25	t_{WHRL3}	Read after Read Address Write	6 X t_{CHCH}		ns	
26	t_{SVWL}	Register Select Setup to /W LOW	10		ns	
27	t_{WLSX}	Register Select Hold from /W LOW	3		ns	
28	t_{DVWH}	Data Setup to /W HIGH	10		ns	
29	t_{WHDX}	Data Hold from /W HIGH	3		ns	

NOTES

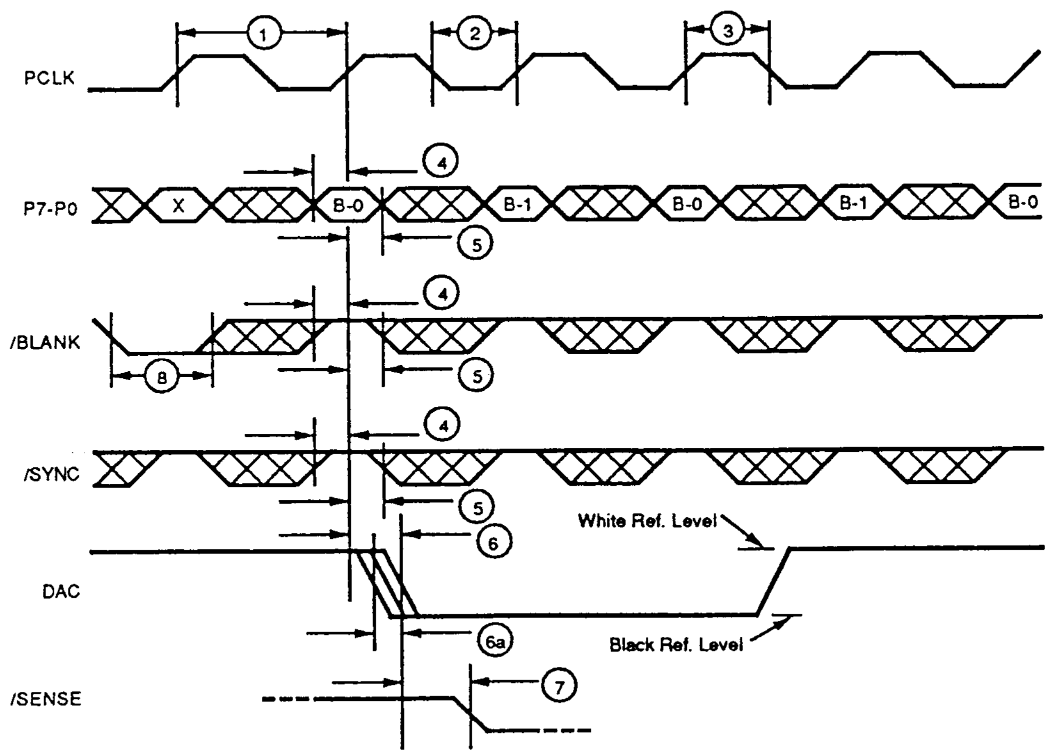
1. ICC is measured with VCC=VCC (max) and tCHCH=tCHCH (min). SETUP=VCC (7.5 IRE). The DAC test load is as shown in Figure 6-1. DQ7-DQ0 are unloaded. IREF = -8.89 mA.
2. Full Scale Error is measured from the value given by the design equation. IREF = -8.89 mA.
3. Measured from the DAC output with the center value. IREF = -8.89 mA.
4. Measured from a straight line between the endpoints in Pseudo-color mode. Monotonicity is guaranteed in all modes.
5. Full Scale Settling Time is measured from a 2% change in output voltage until the output voltage has settled to within ±2% of final value.
6. Guaranteed but not 100% tested.
7. Measured at the 50% point between the starting and ending DAC values.
8. Measured from a ±200 mV change from the steady-state voltage using Test Load as shown in Figure 9.
9. /BLANK≤VIL(MAX) to Disable RED, GREEN, and BLUE Analog outputs.
10. All DAC outputs should be terminated with the equivalent of a single- or double-terminated 75-Ω transmission line (75-Ω or 37.5-Ω resistive load to ground), independent of the number of DAC outputs used. Unused DAC outputs may also be tied directly to AGND or DGND.
11. The IREF pin and analog output pins always source current. This specification shows a current magnitude and ignores the algebraic sign. The typical IREF value (8.89 mA) gives a grey scale output voltage of 700 mV into a 37.5-Ω load (75-Ω local termination in parallel with 75-Ω monitor) with SETUP and /SYNC LOW.
12. Measured from the PCLK transition that causes the DAC to change. The internal pipeline delay from P7-P0 to the DAC output is not included.
13. 15-, 16-, and 24-bit Direct Color modes only.

TIMING DIAGRAMS

VIDEO PORT — PSEUDO-COLOR MODE TIMING

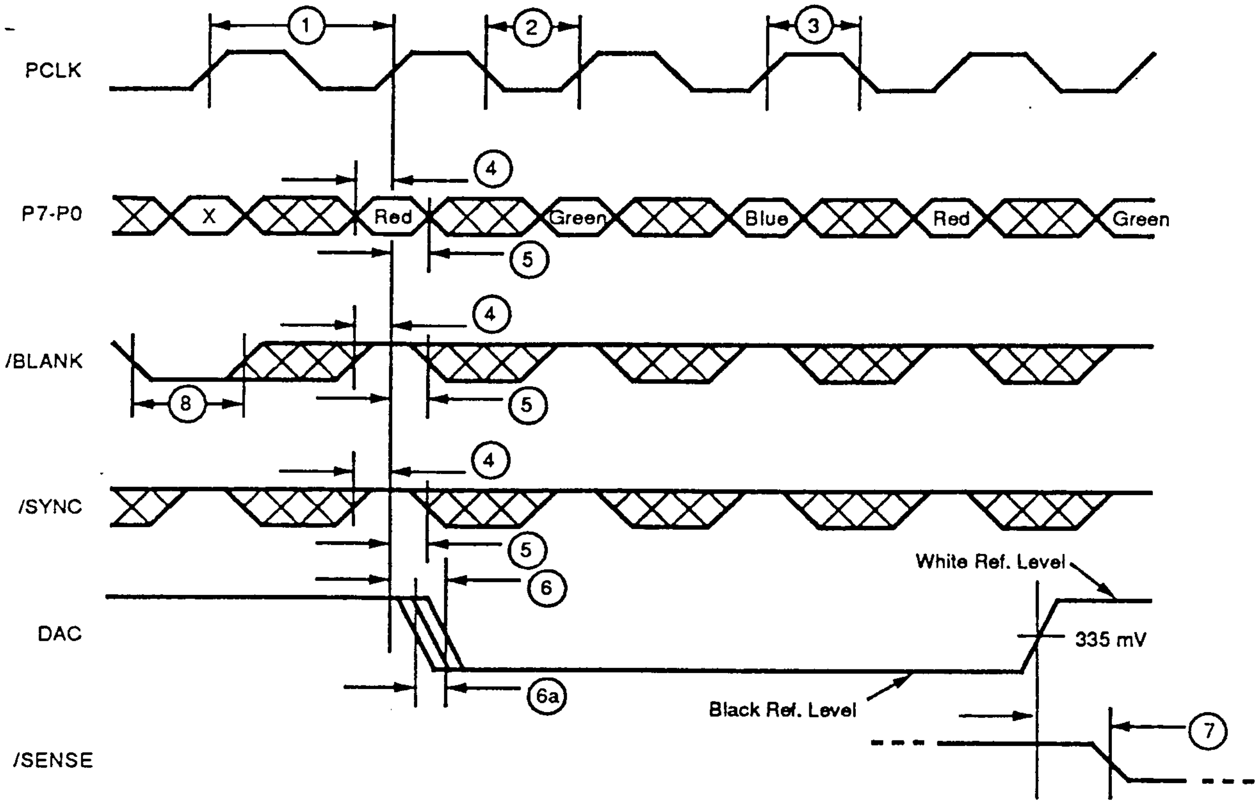


VIDEO PORT — 15- AND 16-BIT DIRECT COLOR MODE

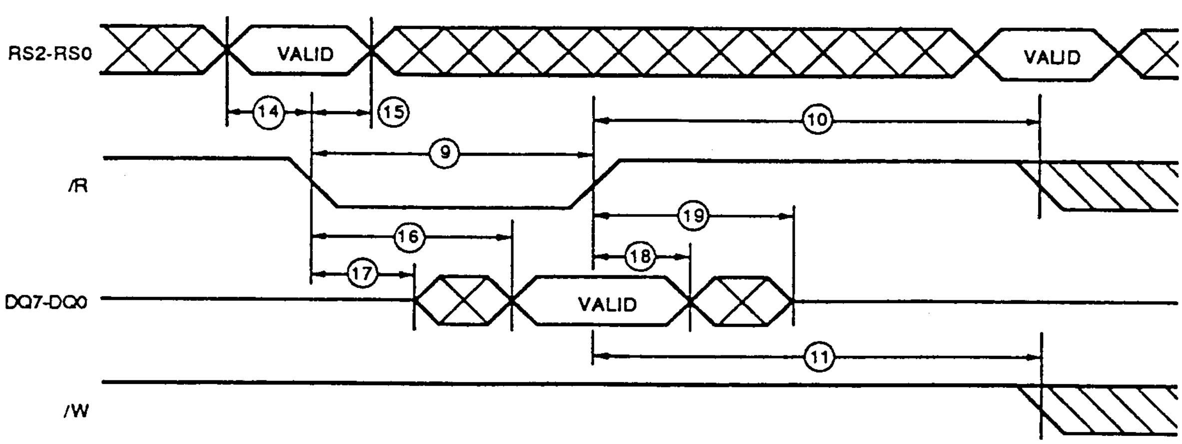


TIMING DIAGRAMS (CONT'D)

VIDEO PORT — 24-BIT DIRECT COLOR MODE

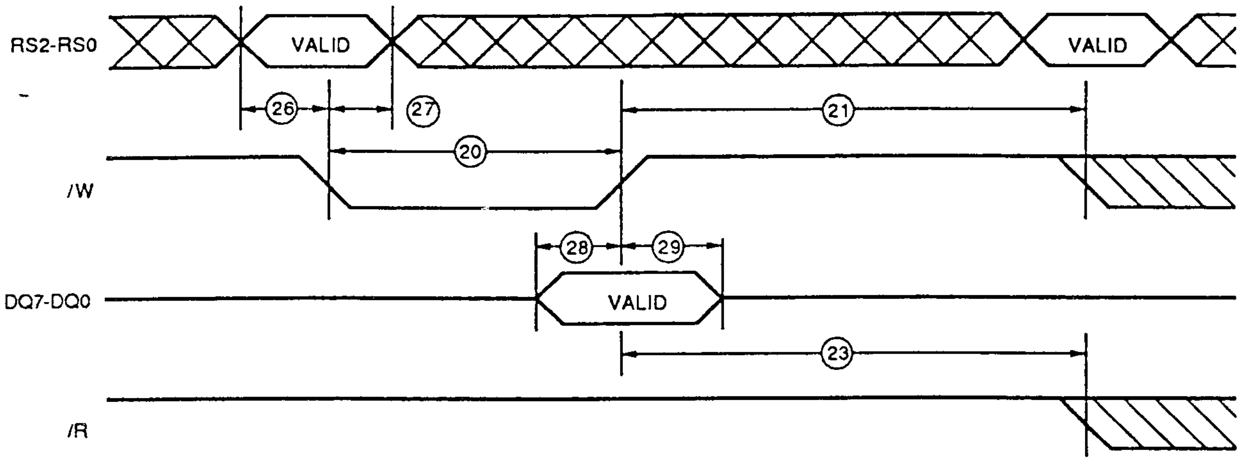


MICROPROCESSOR READ CYCLE

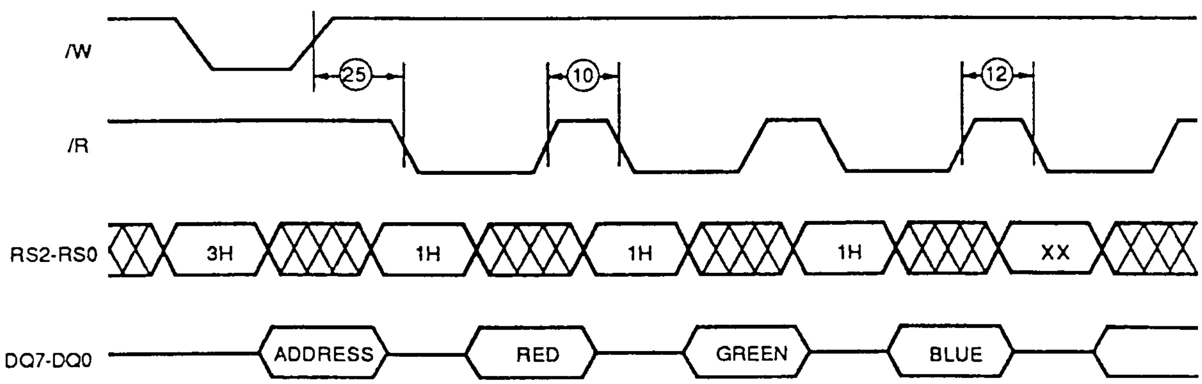


TIMING DIAGRAMS (CONT'D)

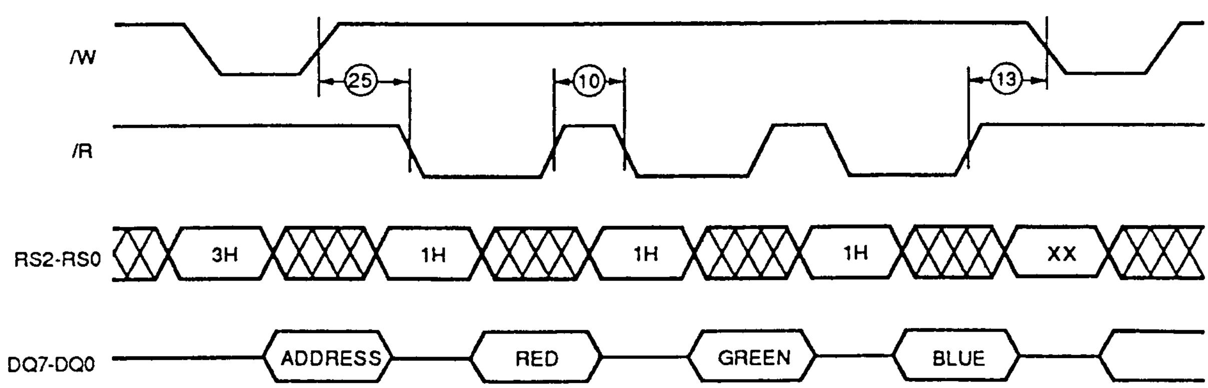
MICROPROCESSOR WRITE CYCLE



COLOR VALUE READ TO READ

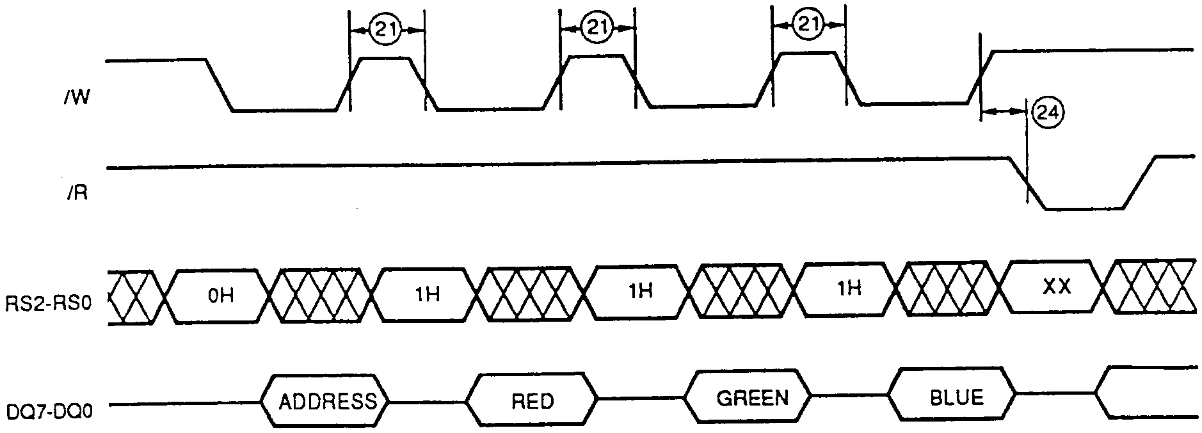


COLOR VALUE READ TO WRITE

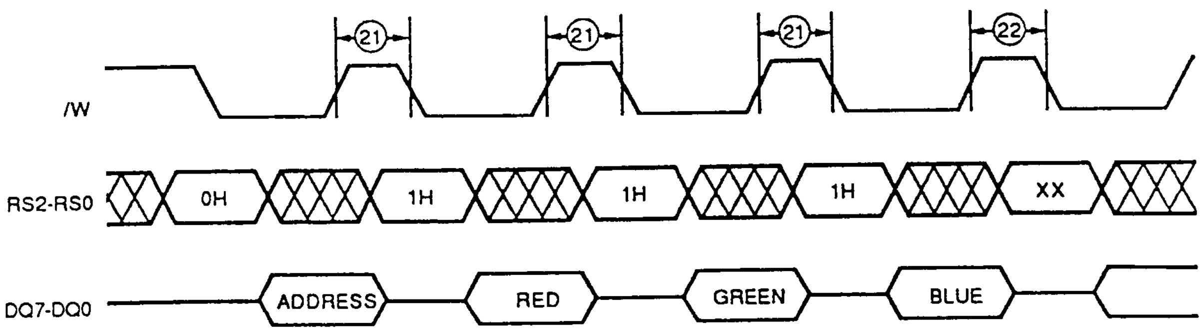


TIMING DIAGRAMS (CONT'D)

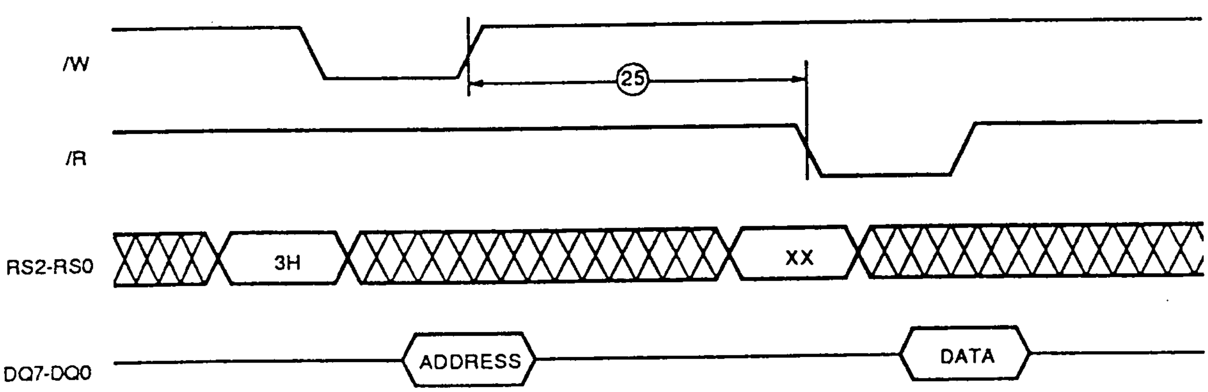
READ AFTER COLOR VALUE WRITE



WRITE AFTER COLOR VALUE WRITE

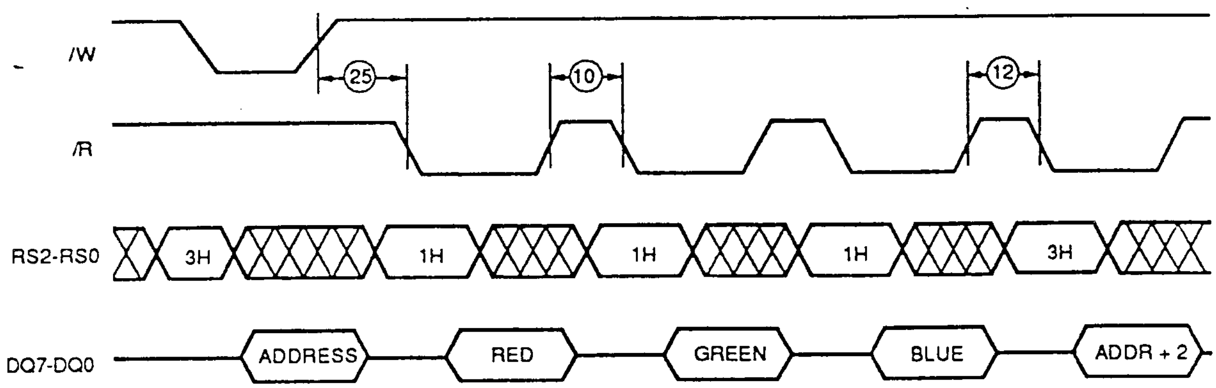


READ AFTER WRITING READ ADDRESS REGISTER

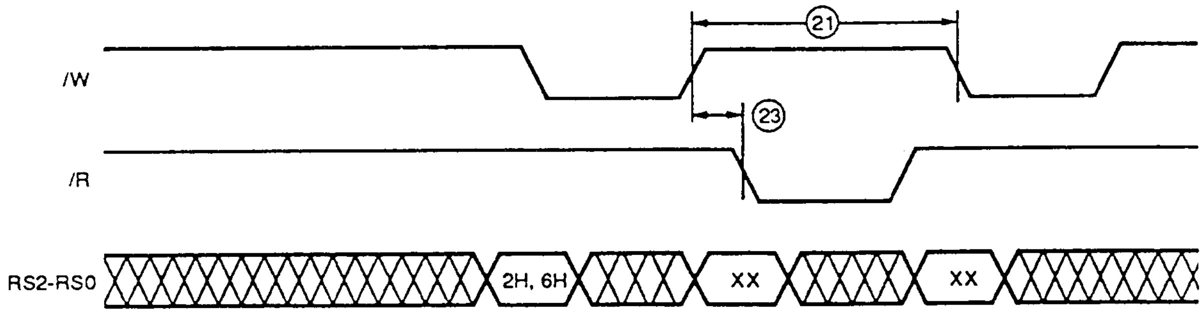


TIMING DIAGRAMS (CONT'D)

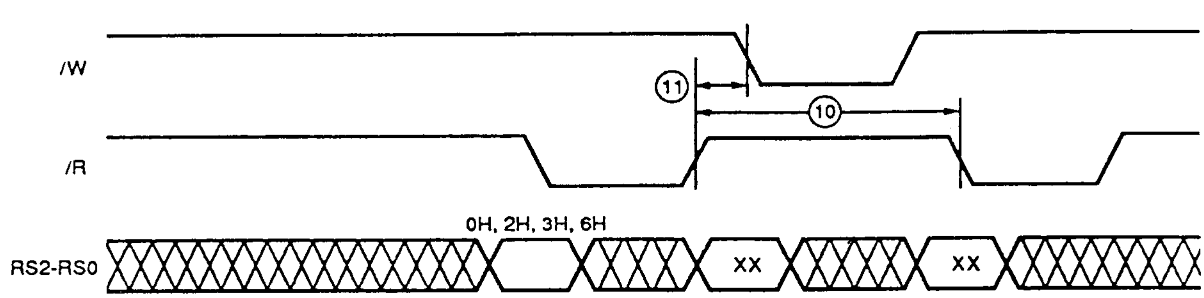
READ COLOR VALUE THEN READ ADDRESS



MASK OR COMMAND REGISTER WRITE TO READ OR WRITE

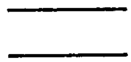


READ FROM COMMAND, MASK OR ADDRESS REGISTER TO READ OR WRITE

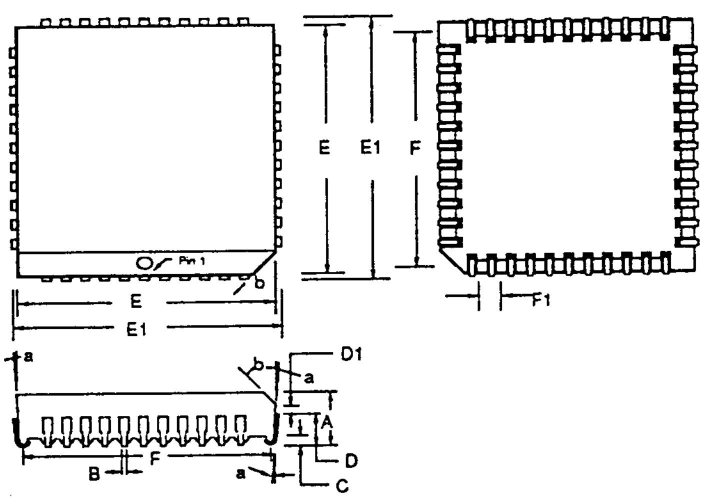


TIMING DIAGRAMS (CONT'D)

KEY

WAVEFORMS	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from H to L	Will be changing from H to L
	May change from L to H	Will be changing from L to H
	Don't care. Any change permitted	Undefined. State unknown
	Does not apply	Center line is high impedance "off state"

PACKAGE OUTLINE



44-PIN PLASTIC LEADED CHIP CARRIER

Lead Count	Dim A	Dim B	Dim C	Dim D	Dim D1	Dim E	Dim. E1	Dim. F	Dim. F1	Dim. a	Dim. b		
44	.170 / .176	.017 TYP	.033 / .043	.098 TYP	.050 TYP	.650 / .656	.685 / .695	.620 / .626	.050 TYP	3° / 6°	45° TYP		

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ORDERING INFORMATION

PART NUMBER	SPEED	REFERENCE	PACKAGE	TEMPERATURE RANGE
MU9C1880-90DC	90MHz	CURRENT	44-PIN PLDCC	0-70°C

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