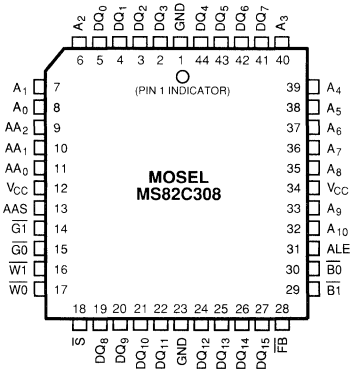
2 x 2K x 16 Cache Data RAM

FEATURES

- Supports 16 bit wide 80286 and 32 bit wide 80386 system cache data requirements directly.
- High speed access supports 16/20/25 MHz 80386 systems.
- On-board x16 SRAM organized as 2 sets of 2K x 16.
- On-board address latches support pipelined accesses with no external components.
- Easliy supports 2-way and 4-way set associative cache subsystems.
- Supports both pipelined and non-pipelined cycles.
- 16 bit bi-directional data path.
- Built-in alternate address multiplexer allows quick word selection during line replacement.
- Interfaces directly with Intel 82385, Chips & Technologies 82C307/82C327 and other cache controllers.
- Significantly reduces board real estate required for cache data storage.
- Packaged in JEDEC standard 44 terminal PLCC.

PIN CONFIGURATIONS



DESCRIPTION

The MOSEL 82C308 is a high performance CMOS static RAM optimized for use as cache subsystem data buffers in 80386 and 80286 systems. The device has a full 16 bit wide bi-directional data path, and is configured as 2 banks of 2K x 16 memory. This configuration offers significant design, density and power advantages over designs using traditional RAM architectures in caches for these systems.

The MS82C308 is available with fast address access times down to 35ns (max), and with very fast output enable times (12ns max.), and supports 80386 systems up to 25 MHz. The MS82C308 contains all the logic on-board to interface directly with the Intel 82385, Chips & Technologies 82C307/82C327 and other cache controllers. Its' on-board address latches allow it to support both pipelined and non-pipelined memory accesses. An additional on-board alternate address multiplexer is provided to allow fast selection or words during line replacement.

For a 32 bit 80386 system with a 16KB cache, only 2 devices are needed. For a 32 bit 80386 system with a full 32KB cache, only 4 MS82C308 devices are needed, replacing the standard requirement of 16 4K x 4 SRAMS and additional discrete logic. This offers a significant reduction in board real estate, power, cost and capacitive loading.

The MS82C308 is manufactured in MOSEL's high performance CMOS process and operates from a single 5V power supply. All inputs and outputs are TTL compatible. The device is supplied in a space saving JEDEC standard 44 terminal PLCC package.

6

SPEED SELECTION

80386 SPEED	RECOMMENDED MS82C308
16MHz	–55
20MHz	–45
25MHz	–35

PIN DESCRIPTIONS

A_0 - A_{10} Address Inputs

These 11 address inputs select one of the 2048 16-bit words in each RAM bank.

AA_0 - AA_2 Alternate Address Inputs

These 3 alternate address inputs are used to select words within the same page. They are used in conjuction with AAS.

AAS Alternate Address Select

This pin is active high. When LOW, address inputs A_0-A_2 will be input to the array; when HIGH, alternate address inputs AA_0-AA_2 will be input to the array.

ALE Address Latch Enable

This active HIGH pin controls the internal transparent latches on pins A_0-A_{11}. When ALE is HIGH the latch is transparent and the inputs on the address pins are applied to the memory array. On the falling edge of ALE the current input states of pins A_0-A_{11} are latched and remain applied to the memory array until ALE returns to the active HIGH state.

$\overline{G0}$ Output Enable 0 Input
$\overline{G1}$ Output Enable 1 Input

These output enables are active LOW. $\overline{G}_0$ active will enable data output from Bank 0, while $\overline{G}_1$ will enable data output from Bank 1. These two pins can not both be active simultaneously. The DQ pins will be in the high-impedance state when deselected.

$\overline{S}$ Chip Select Input

This pin is active low. The DQ pins will be in the high-impedance state when deselected.

$\overline{B0}$ Byte Enable 0 Input
$\overline{B1}$ Byte Enable 1 Input

These pins are active LOW. During a write operation, these pins select whether the upper or lower byte of the addressed 16-bit word will be written.

$\overline{FB}$ Force Byte Enable Input

This pin is active LOW. If the $\overline{FB}$ pin is active during a write operation, both the upper and low bytes of the addressed 16-bit word will be written.

$\overline{W0}$ Write Enable 0 Input
$\overline{W1}$ Write Enable 1 Input

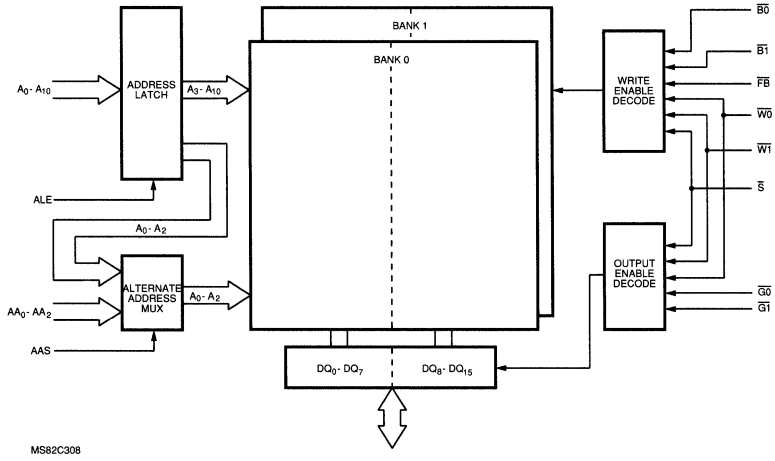
The chip is selected and either byte enable input or the force byte enable input is active, bring a write enable pin active will cause the data present on the DQ pins to be written into the selected bank.

DQ_0-DQ_{15} Data Input/Output Ports

These 16 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply
GND Ground

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The MS82C308 is a high performance CMOS static RAM intended for use as a data buffer in caches for 80386 or 80286 systems. A two byte wide data path is provided for use in 16 and 32 bit systems. The array is configured as two banks to allow a fast output enable to be generated by a search of the cache directory concurrent with the data buffer access. It replaces four 4K x 4 or 2K x 8 chips and several TTL MSI and SSI chips with a small footprint 44 pin PLCC. In addition, power, cost and capacitive loading are significantly reduced.

Two chips are needed for a 32 bit 80386 system with a 16KB cache while a single chip can be used to implement and 8KB 80286 cache. The arrays could be doubled to implement a 4-way set associative system if desired.

For a 32 bit 80386 system with a full 32KB cache, four MS82C308 chips would be needed. The cache depth can be expanded as desired. For example, for a system with a 64KB cache, 8 MS82C308's are needed.

Address Latch

An on-board address latch is used to store the address directly from the 80386 local address bus. Two different modes of operations (pipelined cycle vs. non-pipelined cycle) are possible in an 80386 based system. The transparent address latch is enabled by the ALE pin. In non-pipelined accesses, the address will change during the ALE cycle. In pipelined accesses the address will change before the rising edge of ALE.

The access time in non-pipelined cycles will be determined by address access time, while it will be measured from the rising edge of ALE in pipe-lined cycles.

Alternate Address Multiplexer

A 3 bit multiplexer is provided to allow selection of words within the same block of 2, 4 or 8 words. This is necessary in cache systems when the line or sub-line (unit of memory that is replaced) is greater than one word.

RAM Array

The RAM is logically configured as two banks of 2K words of 2 bytes. Both banks are always accessed simultaneously; the two output enables are used to select which word is outputted to the data bus.

Output Enable Decode

Two $\overline{G}$ inputs are provided, one for each bank. $\overline{G0}$ will gate the data from first bank and $\overline{G1}$ will gate the data from second bank. If either of the two write enable signals are active, the output enable signals will be overridden to prevent the 82C308 from driving the bus. Two $\overline{G}$'s ($\overline{G0}$ and $\overline{G1}$) inputs can not be active at the same time. Otherwise, undetermined results would appear at the 16 data outputs.

Write Enable Decode

Two $\overline{W}$ inputs are provided, one for each bank. When either of the write enables are asserted, the array outputs are disabled to prevent driver conflicts. Individual byte enables are provided that control the writes in either or both of the two bytes of the 82C308. The $\overline{FB}$ input is provided to allow forcing both byte write enables during a move-in (fetch) operation. This eliminates the external gating of write enable required in a store-in cache implementation.

Array Expansion

A chip select input ($\overline{S}$) is provided to allow for expansion of the cache array in the vertical (more words) dimension. The access time from chip select is less than the address to data time to allow for external decoding circuitry.

Set Associativity

While the MS82C308 is intended to be used in a two-way set associative cache implementation, it is very simple to increase the size of the cache by increasing the associativity to 4 or more ways by paralleling MS82C308's (2 for 4 way, 4 for 8 way, etc).

TRUTH TABLE

	INPUTS										OUTPUTS		FUNCTION
	ALE	AAS	$\overline{G0}$	$\overline{G1}$	$\overline{S}$	$\overline{B0}$	$\overline{B1}$	$\overline{FB}$	$\overline{W0}$	$\overline{W1}$	DQ_0-DQ_7	DQ_8-DQ_{15}	
1	X	X	X	X	H	X	X	X	X	X	HI-Z	HI-Z	Deselected
2	X	X	H	H	L	H	H	H	H	H	HI-Z	HI-Z	Outputs Disabled
3	L	X	–	–	–	–	–	–	–	–	–	–	Address Latch Enabled
4	H	X	–	–	–	–	–	–	–	–	–	–	Address Latch Transparent
5	X	H	–	–	–	–	–	–	–	–	–	–	Alternate Address Selected
6	H	X	L	H	L	H	H	H	H	H	D_{OUT}	D_{OUT}	Read Current Address (Bank 0)
7	H	X	H	L	L	H	H	H	H	H	D_{OUT}	D_{OUT}	Read Current Address (Bank 1)
8	L	L	L	H	L	H	H	H	H	H	D_{OUT}	D_{OUT}	Read Latched Address (Bank 0)
9	L	L	H	L	L	H	H	H	H	H	D_{OUT}	D_{OUT}	Read Latched Address (Bank 1)
10	X	H	L	H	L	H	H	H	H	H	D_{OUT}	D_{OUT}	Read Alternate Address (Bank 0)
11	X	H	H	L	L	H	H	H	H	H	D_{OUT}	D_{OUT}	Read Alternate Address (Bank 1)
12	H	X	X	X	L	L	H	H	L	H	D_{IN}	HI-Z	Write to Lower Byte of Current Address (Bank 0)
13	H	X	X	X	L	H	L	H	L	H	HI-Z	D_{IN}	Write to Upper Byte of Current Address (Bank 0)
14	H	X	X	X	L	L	L	H	L	H	D_{IN}	D_{IN}	Write to Both Bytes of Current Address (Bank 0)
15	H	X	X	X	L	X	X	L	L	H	D_{IN}	D_{IN}	Write to Both Bytes of Current Address (Bank 0)
16	H	X	X	X	L	L	H	H	H	L	D_{IN}	HI-Z	Write to Lower Byte of Current Address (Bank 1)
17	H	X	X	X	L	H	L	H	H	L	HI-Z	D_{IN}	Write to Upper Byte of Current Address (Bank 1)
18	H	X	X	X	L	L	L	H	H	L	D_{IN}	D_{IN}	Write to Both Bytes of Current Address (Bank 1)
19	H	X	X	X	L	X	X	L	H	L	D_{IN}	D_{IN}	Write to Both Bytes of Current Address (Bank 1)
20	L	L	X	X	L	L	H	H	L	H	D_{IN}	HI-Z	Write to Lower Byte of Latched Address (Bank 0)
21	L	L	X	X	L	H	L	H	L	H	HI-Z	D_{IN}	Write to Upper Byte of Latched Address (Bank 0)
22	L	L	X	X	L	L	L	H	L	H	D_{IN}	D_{IN}	Write to Both Bytes of Latched Address (Bank 0)
23	L	L	X	X	L	X	X	L	L	H	D_{IN}	D_{IN}	Write to Both Bytes of Latched Address (Bank 0)
24	X	H	X	X	L	L	H	H	L	H	D_{IN}	HI-Z	Write to Lower Byte of Alternate Address (Bank 0)
25	X	H	X	X	L	H	L	H	L	H	HI-Z	D_{IN}	Write to Upper Byte of Alternate Address (Bank 0)
26	X	H	X	X	L	L	L	H	L	H	D_{IN}	D_{IN}	Write to Both Bytes of Alternate Address (Bank 0)
27	X	H	X	X	L	X	X	L	L	H	D_{IN}	D_{IN}	Write to Both Bytes of Alternate Address (Bank 0)
28	L	L	X	X	L	L	H	H	H	L	D_{IN}	HI-Z	Write to Lower Byte of Latched Address (Bank 1)
29	L	L	X	X	L	H	L	H	H	L	HI-Z	D_{IN}	Write to Upper Byte of Latched Address (Bank 1)
30	L	L	X	X	L	L	L	H	H	L	D_{IN}	D_{IN}	Write to Both Bytes of Latched Address (Bank 1)
31	L	L	X	X	L	X	X	L	H	L	D_{IN}	D_{IN}	Write to Both Bytes of Latched Address (Bank 1)
32	X	H	X	X	L	L	H	H	H	L	D_{IN}	HI-Z	Write to Lower Byte of Alternate Address (Bank 1)
33	X	H	X	X	L	H	L	H	H	L	HI-Z	D_{IN}	Write to Upper Byte of Latched Address (Bank 1)
34	X	H	X	X	L	L	L	H	H	L	D_{IN}	D_{IN}	Write to Both Bytes of Alternate Address (Bank 1)
35	X	H	X	X	L	X	X	L	H	L	D_{IN}	D_{IN}	Write to Both Bytes of Alternate Address (Bank 1)

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITION	UNIT
V_{TERM}	Terminal Voltage with Repect to GND	–0.5 to +7.0	V
t_{BIAS}	Temperature Under Bias	–10 to +125	°C
t_{STG}	Storage Temperature	–60 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0°C to + 70°C	5V ± 5%

DC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MIN.	TYP. [1]	MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage[2][3]		–0.5	–	0.8	V
V_{IH}	Guaranteed Input High Voltage[2]		2.0	–	6.0	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0Vto V_{CC}	–	–	2	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\overline{G0}$ = V_{IH}, $\overline{G1}$ = V_{IH}, V_{IN} = 0V toV_{CC}	–	–	10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 8mA	–	–	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = – 4mA	2.4	–	–	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max, $\overline{G0}$ = V_{IL} or $\overline{G1}$ = V_{IL}, $\overline{S}$ = V_{IL} $I_{I/O}$ = 0mA, F = F_{MAX}[4]	–	–	150	mA

NOTES:
1. Typical characteristics are at V_{CC} = 5.0V, t_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. $V_{IL(MIN)}$ = –3.0 for pulse width < 20ns.
4. F_{MAX} = $1/t_{RC}$

CAPACITANCE[1] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{DQ}	Input/Output Capacitance	V_{DQ} = 0V	8	pF

1. This parameter is guaranteed and not tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5 ns
Input and Output Timing Reference Level	1.5V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOADS AND WAVEFORMS

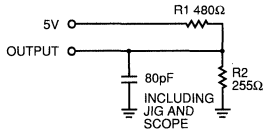


Figure 1a

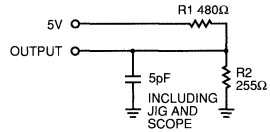


Figure 1b

Equivalent to:

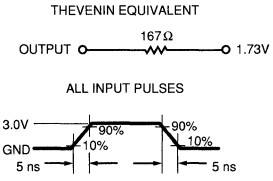


Figure 2

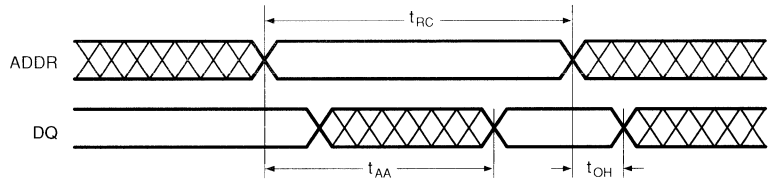
AC ELECTRICAL CHARACTERISTICS (over the operating range)
READ CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	MS82C308-35			MS82C308-45			MS82C308-55			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t_{AVAX}	t_{RC}	Read Cycle Time	35		–	45		–	55		–	ns
t_{AVQV}	t_{AA}	Address Access Time			35			45			55	ns
t_{SLQV}	t_{ACS}	Chip Select Access Time			25			35			45	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid			12			15			18	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output Low Z	2		10	2		15	2		20	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	2		15	2		15	2		15	ns
t_{SLQX}	t_{CLZ}	Chip Select to Output in Low Z	2		10	2		15	2		20	ns
t_{SHQZ}	t_{CHZ}	Chip Deselect to Output in High Z	0		20	0		20	0		20	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change	5		–	5		–	5		–	ns
	t_{CPWH}	ALE Width High	10		–	12		–	15		–	ns
	t_{CPWL}	ALE Width Low	10		–	12		–	15		–	ns
	t_{AS}	Address Latch Setup Time	3		–	3		–	3		–	ns
	t_{AH}	Address Latch Hold Time	5		–	5		–	5		–	ns
	t_{AALE}	Access Time from ALE	–		45	–		55	–		55	ns
	t_{SAA}	AAS to Alternate Address Setup Time	3		–	3		–	3		–	ns
	t_{AAA}	Access Time from AAS or Alternate Address	–		35	–		35	–		35	ns
	t_{OHAA}	Output Hold from AA, AAS Change	3		–	3		–	3		–	ns

SWITCHING WAVEFORMS (READ CYCLE)

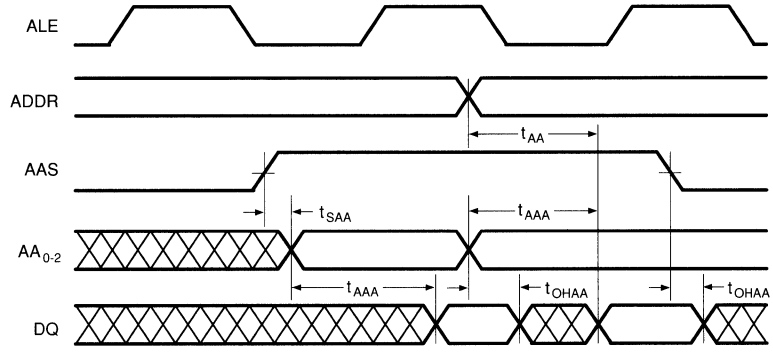
READ CYCLE 1[1,2,3,4,5]

ADDRESS ACCESS TIME - NON-PIPELINE



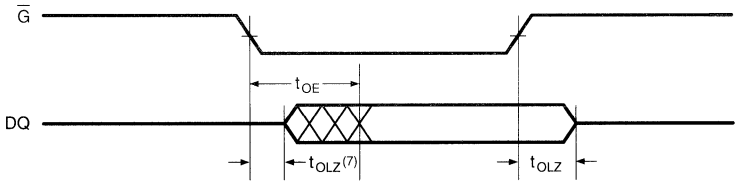
READ CYCLE 2[1,3,4]

ALTERNATE ADDRESS ACCESS



READ CYCLE 3[1,3,6]

OUTPUT ENABLE ACCESS

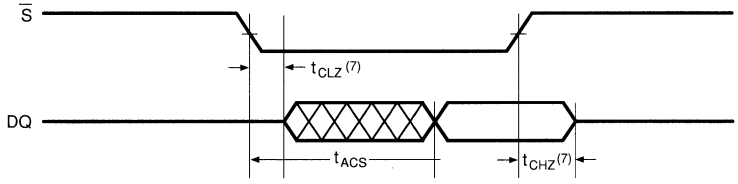


6

SWITCHING WAVEFORMS (READ CYCLE)

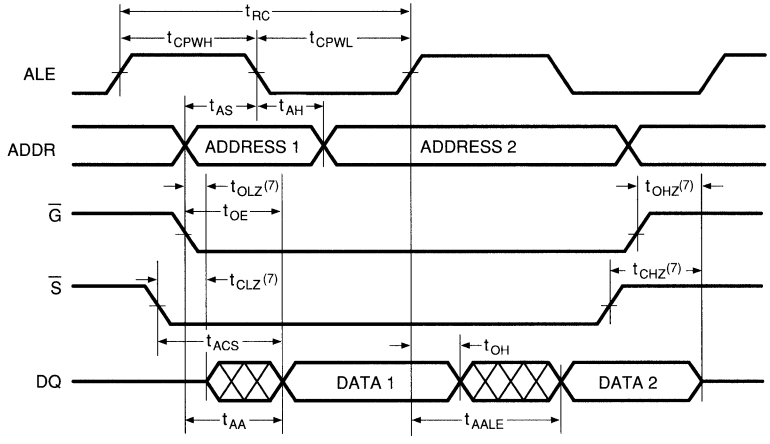
READ CYCLE 4[1,4,6]

CHIP SELECT ACCESS



READ CYCLE 5[1]

PIPELINED



NOTES:
1. $\overline{W0}$, $\overline{W1}$ and $\overline{FB}$ are high during all read cycles.
2. ALE must be high during non-pipelined cycles.
3. Device is continuously selected: $\overline{S} = V_{IL}$.
4. Output is continuously enabled: either $\overline{G0} = V_{IL}$ or $\overline{G1} = V_{IL}$ (but not both).
5. AAS may not change during cycle.
6. Address must be valid sufficiently before $\overline{G}$ or $\overline{S}$ transition low to ensure address access specification not violated.
7. Transition is measured ± 500 mV from steady state with C_L = 5pF as shown in Figure 1b on page 6. This parameter is guaranteed and not 100% tested.

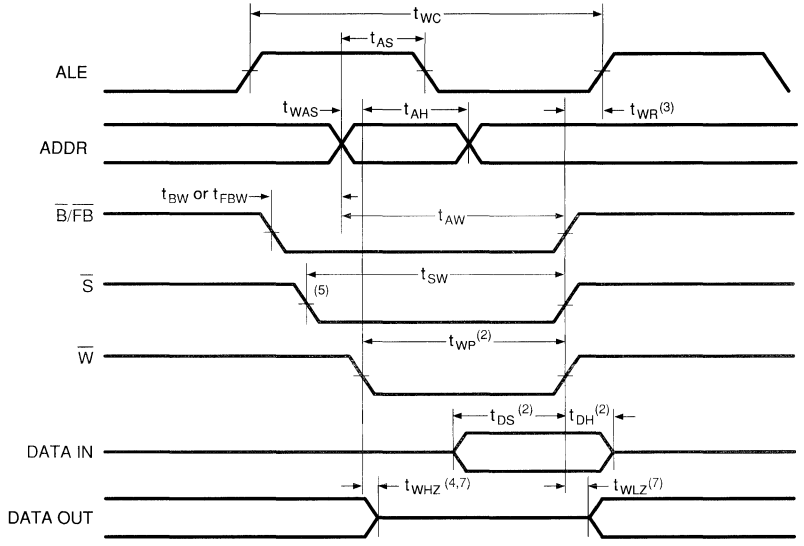
AC ELECTRICAL CHARACTERISTICS (over the operating range)

WRITE CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	MS82C308-35			MS82C308-45			MS82C308-55			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t_{AVAX}	t_{WC}	Write Cycle Time	35	–		45	–		55	–		ns
t_{WLWH}	t_{WP}	Write Pulse Width	20	–		20	–		25	–		ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	2		15	2		15	2		15	ns
t_{WHQL}	t_{WLZ}	Write to Output in Low Z	2		15	2		15	2		15	ns
t_{DVWH}	t_{DS}	Data Setup Time	8	–		10	–		10	–		ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	3	–		5	–		5	–		ns
	t_{AS}	Address Latch Setup Time	3	–		3	–		3	–		ns
	t_{AH}	Address Latch Hold Time	5	–		5	–		5	–		ns
t_{AVWL}	t_{WAS}	Address to Write Setup Time	3	–		5	–		5	–		ns
	t_{SAA}	AAS to Alternate Address Setup Time	3	–		3	–		3	–		ns
	t_{WAAS}	Alt Address Setup Time	6	–		6	–		6	–		ns
	t_{WAAH}	Alt Address Hold Time	2	–		2	–		2	–		ns
	t_{BW}	Byte Enable to Write Pulse Setup	0	–		0	–		0	–		ns
	t_{FW}	Force Byte Enable to Write Pulse Setup	0	–		0	–		0	–		ns
	t_{AW}	Address Valid to End of Wtrite	30	–		35	–		40	–		ns
t_{SLWH}	t_{SW}	Chip Select to Wtrite Pulse End	20	–		25	–		30	–		ns
t_{WHAX}	t_{WR}	Write Recovery Time	2	–		2	–		2	–		ns

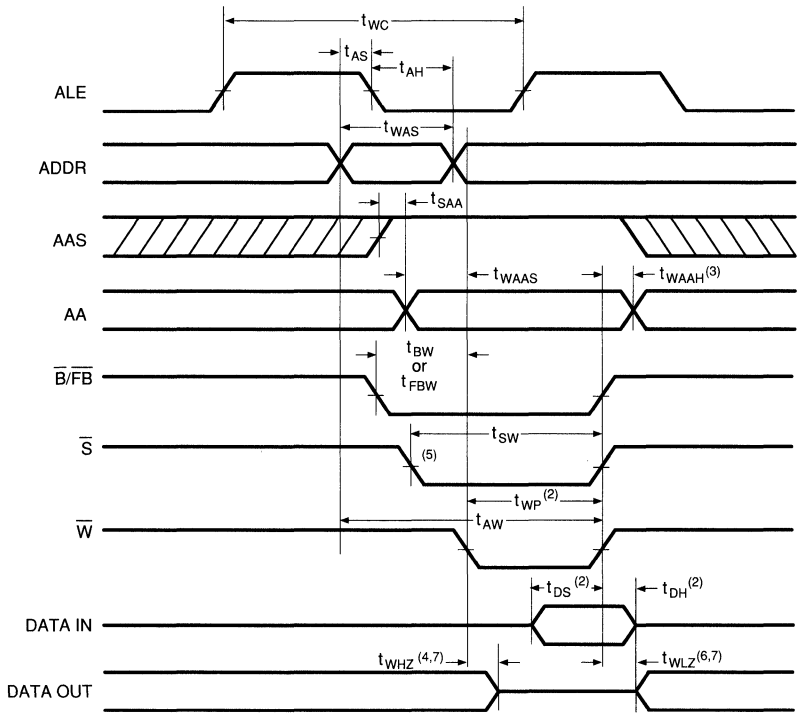
SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 1[1]



SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 2[1]



NOTES:
1. $\overline{W}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{B}$ or $\overline{FB}$ low, $\overline{S}$ low and $\overline{W}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. t_{WR} or t_{WAAH} is measured from the earlier of $\overline{B}$ or $\overline{FB}$, or $\overline{S}$ or $\overline{W}$ going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied
5. If the $\overline{S}$ low transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ transition, outputs remain in a high impedance state.
6. D_{OUT} is the same phase of write data of this write cycle.
7. Transition is measured ± 500 mV from steady state with C_L = 5pF as shown in Figure 1b on page 6. This parameter is guaranteed and not 100% tested.

ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER [1]	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
35	MS82C308-35JC	J44-1	0°C to +70°C
45	MS82C308-45JC		0°C to +70°C
55	MS82C308-55JC		0°C to +70°C