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## **MEC5035-Aurora** Product Customer Specification-ODM

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## **Legacy Free Mobile Embedded Flash ARC EC Base Component with BC-Link**

**Revision 0.61 (08/31/2007)**

### **ORDER NUMBER(S):**

**MEC5035-xx for 128 pin, XVTQFP package**

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## Chapter 1 MEC5035 Features

- 3.3V Operation
- ACPI Compliant
- LPC Interface
  - LPC I/O Cycle decoded
- VTR (standby) and VBAT (Power Planes)
  - Low Standby Current in Sleep Mode
- Configuration Register Set
  - Compatible with ISA Plug-and-Play Standard
  - EC-Programmable Base Address
- ARC-625D Embedded Controller (EC)
  - 192KB plus 2KB single cycle Embedded Flash Closely Coupled instruction memory
  - 4KB Single Cycle 32-bit wide dual-ported SRAM, accessible as both Closely Coupled Data Memory and Instruction Memory
  - Maskable Interrupt controller with 32 interrupts
  - Maskable Hardware Wake-Up Events
  - Idle and sleep modes
  - J-TAG Debug Port
  - MCU Serial Debug Port
- Embedded Flash
  - Size 192KB, 32-bit access, 35ns access time, 1k cycles endurance
  - Programmable by LPC, EC, JTAG interfaces
  - Flash security enhancements
    - Bonding pad implementation
    - Secure Battery secret storage
    - 4K Boot Block protection
    - Direct JTAG and direct LPC-protected (2) pages at or near top of memory for password protection
- Legacy Support
  - Fast GATEA20 & Fast CPU\_RESET
- Four System to EC Message Interfaces
  - 8042 Style Host Interface
  - Mailbox Registers Interface
    - Thirty-two 8-Bit scratch registers
    - Two Register Mailbox Command Interface
    - Two Register SMI Source Interface
  - ACPI Embedded Controller Interface
    - Three instances
    - 1 or 4 Byte Data transfer capable
  - ACPI Power Management Interface
    - SCI Event-Generating Functions
- Battery Backed Resources
  - Power-Fail Status Register
  - 32KHz clock generator
  - 1 Week Wakeup timer
  - Power Switch Interface
  - Vbat backed 64 byte memory
- Two EC based SMBus 2.0 Host Controllers
  - EC SMBus Host Interface Logic Allows Master or Slave Operation
  - Controllers are Fully Operational on Standby Power
  - I2C Compatibility Mode
  - Collision Detect Hardware (Multi-Master Support).
  - 400Khz SMB capability
  - Scalable input clock (16MHz in current MEC5035 definition).
  - 10 Ports multiplexed to single Controller/ 4 Ports multiplexed to single Controller
- Three independent Hardware Driven PS/2 Ports
  - Fully functional on Main and/or Suspend Power
  - PS/2 edge Wake Capable
- 101 General Purpose I/O Pins

**Product Customer Specification-ODM**

- 8 GPIO Pass-Through Port (GPTP)
- Total 3 LED's
  - Numerous different blink rates (including all MEC5025 blink rates)
  - Breathing LED output
  - Operate when EC is in sleep state
- Four Programmable 16-bit Timers
- Two Hibernation Timer
  - Programmable wake-up from 0.5ms to 128 minutes
- System Watch Dog Timer (WDT)
- SMSC BC-Link Interconnection Bus
  - Three High Speed Bus Masters Controllers (HSBCM)
  - One LowSpeed Bus Masters Controllers (LSBCM)
- EC General Purpose Serial Peripheral Interface (ECGP-SPI)
  - 3-pin Full Duplex serial communication interface
  - Flexible clock rates
  - SPI Burst capable
- FAN Support
  - Three Programmable Pulse-Width Modulator Outputs
    - Multiple Clock Rates
    - 16-Bit ON & 16-Bit OFF Counters
  - Three Fan Tachometer Inputs
  - One additional Programmable Pulse-Width Modulator Output
- Two pin debug Port with standard 16550 register interface
  - Accessible from both Host and EC
  - Programmable Input/output pin Polarity Inversion
  - Programmable Main power or standby power functionality
- Resistor/Capacitor Identification Detection (RC\_ID)
  - Single pin interface to external inexpensive RC circuit
  - Replacement for multiple GPIO's
  - Provides 8 quantized states on one pin
- Integrated Standby Power Reset Generator
- Clock Generator
  - 32.768KHz-input clock
  - operational on Suspend Power
  - Programmable Clock Power Management Control & Distribution
  - Primary output 64 Mhz  $\pm 2\%$  Accuracy and various divisors
- 128 Pin XVTQFP package

## 1.1 MEC5035 Features Revision History

This revision history shows the changes made to this chapter.

**Table 1.1 MEC5035 Features Chapter Revision History**

"REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See [Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History," on page 539.](#)

| #  | REV# IN SPEC | DATE          | SECTION/FIGURE/ENTRY | CORRECTION                                                    |
|----|--------------|---------------|----------------------|---------------------------------------------------------------|
| 1. | 0.4          | 2007-04Apr-16 | 16-bit timers        | Removed reference to counter since Tin/Tout is not connected. |
| 2. |              |               | 4K SRAM              | SRAM is dual ported not switched.                             |
| 3. |              |               | GPIO                 | Increase # of GPIO's to actual count=101.                     |
| 4. |              |               | RCID                 | change from TBD to 8 quantized states                         |



**Table 1.1 MEC5035 Features Chapter Revision History**

| “REV# IN SPEC” column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, “MEC5035 Product Customer Specification-ODM Revision History,” on page 539.</a> |              |            |                            |                                                                                                                    |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------------|----------------------------|--------------------------------------------------------------------------------------------------------------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE       | SECTION/FIGURE/ENTRY       | CORRECTION                                                                                                         |
| 5.                                                                                                                                                                                                                                          | 0.61         | 2007-08-15 | Programmable 16-bit Timers | Changed instances from 3 to 4.                                                                                     |
| 6.                                                                                                                                                                                                                                          | 0.61         | 2007-08-31 | SMB                        | — Removed Exceeds 8 Ports multiplexed to single Controller / One Controller dedicated to a single port requirement |



## Chapter 2 General Description

The MEC5035 is the EC Base Component of a multi-device Advanced I/O Controller system. In this architecture the MEC5035 is matched with up to four Companion components. Communication between the base and companion is accomplished using the [SMSC BC-Link Master](#) in the MEC5035 via the SMSC BC-Link protocol as described in [Chapter 32, "SMSC BC-Link Master," on page 510](#) and [SMSC BC-Link \(TM\) Specification, Revision 1.02, dated September 05, 2007](#).

The MEC5035 is the EC Base Component of a split-architecture Advanced I/O Controller system. In this architecture, the MEC5035 is paired with High Speed SMSC BC-Link Companion Components; (such as the SMSC ECE5018 Commercial Companion or the ECE5011 Consumer Companion) and Low Speed SMSC BC-Link Components (such as the SMSC ECE1077 KBD Scan Extension.)

### 2.1 EC Base Component

The MEC5035 is a fully integrated EC Base Component that incorporates an high-performance [ARC 625D Embedded Controller](#) with a 192KB [Embedded Flash Subsystem](#), an [8042 Emulated Keyboard Controller](#), a [General Purpose Serial Peripheral Interface \(GP-SPI\)](#), a three-port [PS/2 Device Interface](#), a 2-pin [Two Pin Serial Port \(UART\)](#) accessible to both the LPC-host and EC two multi-port [SMB Device Interfaces](#), a Serial IRQ Peripheral Interface, a three-port [ACPI Embedded Controller Interface](#) with four data byte enhancement, a [GPIO Interface](#) including eight [GPIO Pass-Through Ports](#), Watch-Dog Timer, Hibernation Timer, a 16-Bit Timer Interface, Mailbox Registers Interface, a three-pin Fan Tachometer Interface with high and low fan speed threshold detection, PCI Clock Run Support, four independently programmable Pulse-Width Modulators, maskable hardware Wake-Up Events and four BC Interconnect Bus interfaces.

A detailed MEC5035 Block Diagram is shown the following figure.

The MEC5035 is directly powered by two separate suspend supply planes (VBAT and VTR) and senses a third runtime power plane (VCC) to provide "instant on" and system power management functions (see [Section 4.5, "Power Configuration," on page 96](#)). The MEC5035 also contains an the EC System Power Management Interface supports low-power states and can drive state changes as a result of hardware Wake-Up Events as defined by the MEC5035 Wake Interface. ACPI-related functions are supported by the EC System Power Management Interface through the SCI Interface. MEC5035 VBAT battery-backed resources includes a Power Switch Interface, [Week Alarm Interface](#) and 64 bytes of VBAT-backed RAM accessible by the EC only.

Each of the MEC5035 logical device I/O addresses can be programmed through internal configuration registers. The MEC5035 configuration register set is compatible with the [Plug and Play ISA Specification, Version 1.0a, Intel Corp. and Microsoft Corp., May 5, 1994](#) and provides the functionality needed to support Microsoft Windows operating systems. The legacy host Super I/O Configuration and alternate Super I/O Configuration decode ranges comply with the [Intel Low Pin Count Specification, Revision 1.0, September 29, 1997](#). The Super I/O Configuration decode ranges are relocatable above 0x100 by EC control and/or by host access. Full 16-bit I/O runtime register address decoding is supported and there are 15 configurable IRQ options for each logical device.

The MEC5035 also defines a Software Development System Interface that includes an MCU Serial Debug Port, an EC accessible UART that can operate at 115.2K baud, and a JTAG interface.

## 2.2 Embedded Controller

## 2.3 Block Diagram

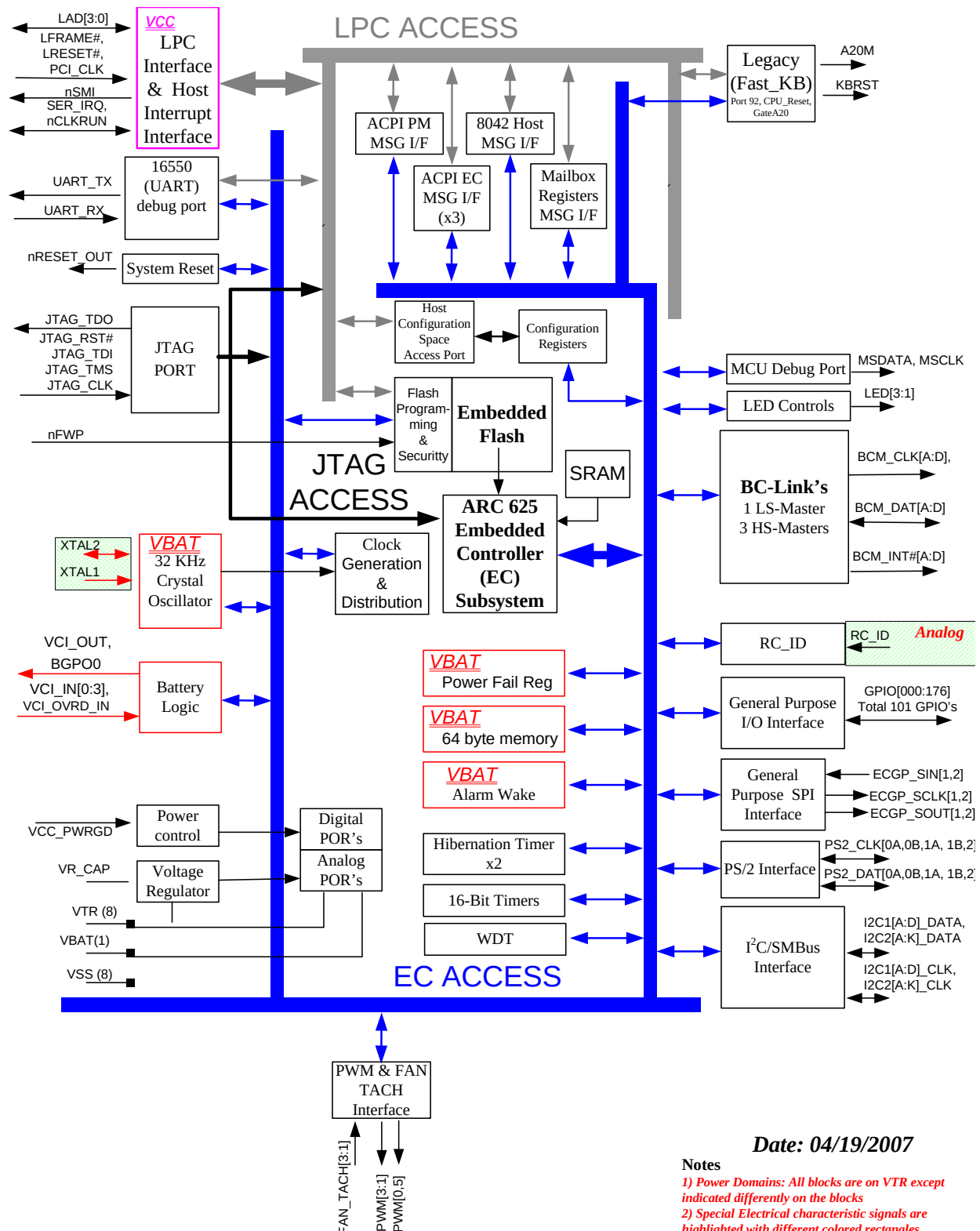




Figure 2.1 MEC5035 Block Diagram

## 2.4 General Description Revision History

This revision history shows the changes made to this chapter.

**Table 2.1 General Description Chapter Revision History**

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History," on page 539.</a> |              |            |                      |                                                                               |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------------|----------------------|-------------------------------------------------------------------------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE       | SECTION/FIGURE/ENTRY | CORRECTION                                                                    |
| 1.                                                                                                                                                                                                                                          | 0.04         | 04/19/2007 | All<br>Block Diagram | Major general description addition added<br>TBD's removed<br>Added SRAM block |
| 2.                                                                                                                                                                                                                                          |              |            |                      |                                                                               |
| 3.                                                                                                                                                                                                                                          |              |            |                      |                                                                               |
| 4.                                                                                                                                                                                                                                          |              |            |                      |                                                                               |



## Chapter 3 Pinout and Pin Description

The MEC5035 is available in 128 XVTQFP Package.

### 3.1 Dell Signal Convention

Dell Motherboard signal names differ from SMSC Signal names for the signals listed in [Table 3.1](#). SMSC signal names are used for the remainder of this document. This list is not meant to be all encompassing; there may be other Dell motherboard signal names that do not correspond to SMSC Signal naming conventions.

**Table 3.1 Dell Mother Signal/SMSC Signal Naming Convention non-concordance**

|    | MEC5035 pin | Dell Signal Name          | SMSC Signal Name             |
|----|-------------|---------------------------|------------------------------|
| 1  | 1           | POWER_SW_IN3#/GPIO000     | VCI_IN3#/GPIO000             |
| 2  | 9           | GPIO007/I2C1D_DATA/EMCLK2 | GPIO007/I2C1D_DATA/PS2_CLK0B |
| 3  | 10          | GPIO010/I2C1D_CLK/EMDAT2  | GPIO010/I2C1D_CLK/PS2_DAT0B  |
| 4  | 67          | GPIO101/SPI_CLK           | GPIO101/ECGP_SCLK            |
| 5  | 68          | GPIO102/SPI_DOUT          | GPIO102/ECGP_SOUT            |
| 6  | 69          | GPIO103/SPI_DIN           | GPIO103/ECGP_SIN             |
| 7  | 70          | GPIO104/LPC_TX            | GPIO104/UART_TX              |
| 8  | 71          | GPIO105/LPC_RX            | GPIO105/UART_RX              |
| 9  | 75          | GPIO110/IMCLK             | GPIO110/PS2_CLK2/GPTP-IN6    |
| 10 | 76          | GPIO111/IMDAT             | GPIO111/PS2_DAT2/GPTP-OUT6   |
| 11 | 77          | GPIO112/KCLK1             | GPIO112/PS2_CLK1A            |
| 12 | 78          | GPIO113/KDAT1             | GPIO113/PS2_DAT1A            |
| 13 | 79          | GPIO114/EMCLK1            | GPIO114/PS2_CLK0A            |
| 14 | 80          | GPIO115/EMDAT1            | GPIO115/PS2_DAT0A            |
| 15 | 81          | GPIO116/EC_2pin debug_DAT | GPIO116/MSDATA               |
| 16 | 82          | GPIO117/EC_2pin debug_CLK | GPIO117/MSCLK                |
| 17 | 111         | GPIO154/I2C1C_DATA/KDAT2  | GPIO154/I2C1C_DATA/PS2_CLK1B |
| 18 | 112         | GPIO155/I2C1C_CLK/KCLK2   | GPIO155/I2C1C_CLK/PS2_DAT1B  |
| 19 | 119         | POWER_SW_IN2#/GPIO161     | VCI_IN2#/GPIO161             |
| 20 | 120         | ALWON                     | VCI_OUT                      |
| 21 | 126         | POWER_SW_IN1#/GPIO162     | VCI_IN1#/GPIO162             |
| 22 | 127         | POWER_SW_IN0#/GPIO163     | VCI_IN0#/GPIO163             |
| 23 | 128         | ACAV_IN/GPIO164           | VCI_OVRD_IN/GPIO164          |





## 3.2 SMSC Pin Configuration

Table 3.2 Pin Configuration

| 128<br>XVTQFP<br>Pin # | Na m e                                | 128<br>XVTQFP<br>Pin # | Na m e                   | 128<br>XVTQFP<br>Pin # | Na m e                          | 128<br>XVTQFP<br>Pin # | Na m e                                         |
|------------------------|---------------------------------------|------------------------|--------------------------|------------------------|---------------------------------|------------------------|------------------------------------------------|
| 1                      | VCI_IN3#                              | 33                     | GPIO040/GPTP-OUT3        | 65                     | VTR[3]                          | 97                     | GPIO141/I2C1F_DATA<br>/I2C2B_DATA              |
| 2                      | GPIO001                               | 34                     | GPIO041                  | 66                     | GPIO100/nEC_SCI                 | 98                     | GPIO142/I2C1F_CLK<br>/I2C2B_CLK                |
| 3                      | GPIO002                               | 35                     | GPIO042/BCM_C_INT#       | 67                     | GPIO101/ECGP_SCLK               | 99                     | GPIO143/I2C1E_DATA                             |
| 4                      | VTR[7]                                | 36                     | GPIO043/BCM_C_DATA       | 68                     | GPIO102/ECGP_SOUT               | 100                    | GPIO144/I2C1E_CLK                              |
| 5                      | GPIO003/I2C1A_DATA                    | 37                     | GPIO044/BCM_C_CLK        | 69                     | GPIO103/ECGP_SIN                | 101                    | VSS_RO                                         |
| 6                      | GPIO004/I2C1A_CLK                     | 38                     | GPIO045/LSBCM_D_IN<br>T# | 70                     | GPIO104/UART_TX                 | 102                    | GPIO145/JTAG_TDI                               |
| 7                      | GPIO005/I2C1B_DATA                    | 39                     | GPIO046/LSBCM_D_DATA     | 71                     | GPIO105/UART_RX                 | 103                    | GPIO146/JTAG_TDO                               |
| 8                      | GPIO006/I2C1B_CLK                     | 40                     | GPIO047/LSBCM_D_CLK      | 72                     | GPIO106/nRESET_OUT              | 104                    | VTR[6]                                         |
| 9                      | GPIO007<br>/I2C1D_DATA<br>/PS2_CLK0B  | 41                     | GPIO050/FAN_TACH1        | 73                     | GPIO107                         | 105                    | GPIO147/I2C1J_DATA<br>/I2C2C_DATA<br>/JTAG_CLK |
| 10                     | GPIO010/I2C1D_CLK<br>/PS2_DATA0B      | 42                     | GPIO051/FAN_TACH2        | 74                     | VSS[3]                          | 106                    | GPIO150/I2C1J_CLK<br>/I2C2C_CLK<br>/JTAG_TMS   |
| 11                     | GPIO011/nSMI                          | 43                     | GPIO052/FAN_TACH3        | 75                     | GPIO110/PS2_CLK2<br>/GPTP-IN6   | 107                    | JTAG_RST#                                      |
| 12                     | GPIO012<br>/I2C1H_DATA<br>/I2C2D_DATA | 44                     | VTR[2]                   | 76                     | GPIO111/PS2_DATA2<br>/GPTP-OUT6 | 108                    | GPIO151/GPTP-IN4                               |
| 13                     | GPIO013/I2C1H_CLK<br>/I2C2D_CLK       | 45                     | GPIO053/PWM0             | 77                     | GPIO112/PS2_CLK1A               | 109                    | GPIO152/GPTP-OUT4                              |
| 14                     | GPIO014/GPTP-IN7                      | 46                     | GPIO054/PWM1             | 78                     | GPIO113/PS2_DATA1A              | 110                    | GPIO153/LED3                                   |
| 15                     | GPIO015/GPTP-OUT7                     | 47                     | GPIO055/PWM2             | 79                     | GPIO114/PS2_CLK0A               | 111                    | GPIO154<br>/I2C1C_DATA<br>/PS2_CLK1B           |
| 16                     | GPIO016/GPTP-IN8                      | 48                     | GPIO056/PWM3             | 80                     | GPIO115/PS2_DATA0A              | 112                    | GPIO155/I2C1C_CLK<br>/PS2_DATA1B               |
| 17                     | GPIO017/GPTP-OUT8                     | 49                     | VCC_PWRGD                | 81                     | GPIO116/MSDATA                  | 113                    | VSS[5]                                         |
| 18                     | GPIO020                               | 50                     | GPIO060/KBRST            | 82                     | GPIO117/MSCLK                   | 114                    | GPIO156/LED1                                   |
| 19                     | GPIO021/RC_ID                         | 51                     | VSS[2]                   | 83                     | VTR[4]                          | 115                    | GPIO157/LED2                                   |
| 20                     | VSS[7]                                | 52                     | VTR[8]                   | 84                     | GPIO120                         | 116                    | VTR[5]                                         |
| 21                     | VTR[1]                                | 53                     | VSS[8]                   | 85                     | GPIO121/BCM_A_INT#              | 117                    | GPIO160/32KHZ_OUT                              |
| 22                     | VR_CAP[1]                             | 54                     | GPIO061/LPCPD#           | 86                     | GPIO122/BCM_A_DATA              | 118                    | BGPO0                                          |
| 23                     | GPIO022/BCM_B_CLK                     | 55                     | LDRQ#                    | 87                     | GPIO123/BCM_A_CLK               | 119                    | VCI_IN2#                                       |
| 24                     | GPIO023/BCM_B_DATA                    | 56                     | SER_IRQ                  | 88                     | VSS[4]                          | 120                    | VCI_OUT                                        |
| 25                     | GPIO024/BCM_B_INT#                    | 57                     | LRESET#                  | 89                     | GPIO124/GPTP-OUT5               | 121                    | VBAT                                           |
| 26                     | VSS[1]                                | 58                     | PCI_CLK                  | 90                     | GPIO125/GPTP-IN5                | 122                    | XTAL1                                          |
| 27                     | GPIO025/UART_CLK                      | 59                     | LFRAME#                  | 91                     | GPIO126                         | 123                    | nFWP                                           |
| 28                     | GPIO026/GPTP-IN1                      | 60                     | LAD0                     | 92                     | GPIO127/A20M                    | 124                    | XTAL2                                          |
| 29                     | GPIO027/GPTP-OUT1                     | 61                     | LAD1                     | 93                     | GPIO130/I2C2A_DATA              | 125                    | AGND                                           |
| 30                     | GPIO030/GPTP-IN2                      | 62                     | LAD2                     | 94                     | GPIO131/I2C2A_CLK               | 126                    | VCI_IN1#                                       |
| 31                     | GPIO031/GPTP-OUT2                     | 63                     | LAD3                     | 95                     | GPIO132/I2C1G_DATA              | 127                    | VCI_IN0#                                       |
| 32                     | GPIO032/GPTP-IN3                      | 64                     | CLKRUN#                  | 96                     | GPIO140/I2C1G_CLK               | 128                    | VCI_OVRD_IN                                    |

### 3.3 128 XVTQFP package

#### Pin Define

The symbol same as 71.05035.00G  
9/26 confirm Joseph CC Hsu #6560

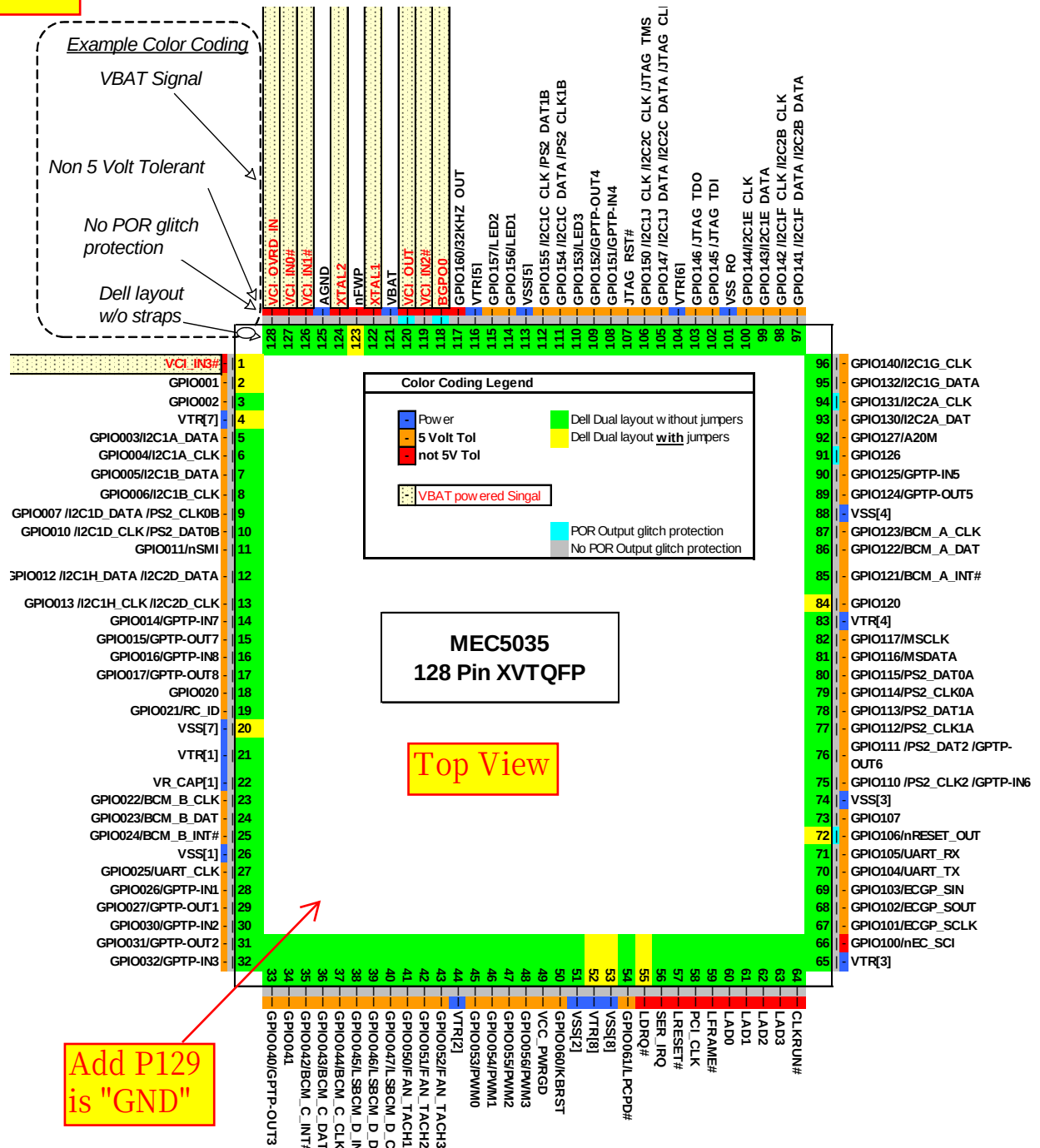


Figure 3.1 128 XVTQFP Package Configuration

### 3.4 Pin Description

The following tables describe the pin functions. See [Section 3.6, "Notes from tables in this chapter,"](#) on page 64 for notes referenced in the tables in this section.

Table 3.3 HOST INTERFACE

| HOST INTERFACE  |             |                                                                  | (13 PINS) |
|-----------------|-------------|------------------------------------------------------------------|-----------|
| 128 VTQFP Pin # | Signal Name | Description                                                      | Notes     |
| 56              | SER_IRQ     | Serial IRQ                                                       | Note2     |
| 55              | LDRQ#       | LPC Encoded DMA request                                          | Note2     |
| 57              | LRESET#     | LPC Reset. LRESET# is the same as the system PCI reset,          |           |
| 58              | PCI_CLK     | PCI Clock                                                        |           |
| 59              | LFRAME#     | Frame signal. Indicates start of new cycle and termination of    |           |
| 60              | LAD0        | LPC address/data bus. Multiplexed command, address and data bus. | Note2     |
| 61              | LAD1        |                                                                  |           |
| 62              | LAD2        |                                                                  |           |
| 63              | LAD3        |                                                                  |           |
| 64              | CLKRUN#     | PCI Clock Control                                                |           |
| 66              | nEC_SCI     | Power Management Event                                           | Note2     |
| 54              | LPCPD#      | The LPC Bus Powerdown Signal.                                    |           |
| 11              | nSMI        | SMI Output                                                       |           |
|                 |             |                                                                  |           |
|                 |             |                                                                  |           |
|                 |             |                                                                  |           |

Table 3.4 BC-Link Interface

| BC-Link         |              |                          | (12 PINS) |
|-----------------|--------------|--------------------------|-----------|
| 128 VTQFP Pin # | Signal Name  | Description              | Notes     |
| 87              | BCM_A_CLK    | BC-Link Master clock     |           |
| 86              | BCM_A_DAT    | BC-Link Master data I/O  | Note3     |
| 85              | BCM_A_INT#   | BC-Link Master interrupt |           |
| 23              | BCM_B_CLK    | BC-Link Master clock     |           |
| 24              | BCM_B_DAT    | BC-Link Master data I/O  | Note3     |
| 25              | BCM_B_INT#   | BC-Link Master interrupt |           |
| 37              | BCM_C_CLK    | BC-Link Master clock     |           |
| 36              | BCM_C_DAT    | BC-Link Master data I/O  | Note3     |
| 35              | BCM_C_INT#   | BC-Link Master interrupt |           |
| 38              | LSBCM_D_INT# | BC-Link Master clock     |           |
| 39              | LSBCM_D_DAT  | BC-Link Master data I/O  | Note3     |
| 40              | LSBCM_D_CLK  | BC-Link Master interrupt |           |
|                 |              |                          |           |

Table 3.5 Clock Interface



| Master Clock          |             |                          | (3 PINS) |
|-----------------------|-------------|--------------------------|----------|
| 128<br>VTQFP<br>Pin # | Signal Name | Description              | Notes    |
| 122                   | XTAL1       | 32.768kHz Crystal Input  |          |
| 124                   | XTAL2       | 32.768kHz Crystal Output |          |
| 117                   | 32KHZ_OUT   | 32.768kHz Digital Output |          |

Table 3.6 Fan &amp; Tachometer

| FAN PWM & TACHOMETER  |             |             | (7 PINS) |
|-----------------------|-------------|-------------|----------|
| 128<br>VTQFP<br>Pin # | Signal Name | Description | Notes    |
| 41                    | FAN_TACH1   |             |          |
| 42                    | FAN_TACH2   |             |          |
| 43                    | FAN_TACH3   |             |          |
| 45                    | PWM0        |             |          |
| 46                    | PWM1        |             |          |
| 47                    | PWM2        |             |          |
| 48                    | PWM3        |             |          |
|                       |             |             |          |
|                       |             |             |          |

See [APPLICATION NOTE: on page 478](#) for PWM pins

Table 3.7 GPIO Interface

| General Purpose Input/Output |                                                                              |                                          | (20 PINS) |
|------------------------------|------------------------------------------------------------------------------|------------------------------------------|-----------|
| 128<br>VTQFP<br>Pin #        | Signal Name                                                                  | Description                              | Notes     |
|                              | <b>101 GPIO's See Multiplexing Tables below in this chapter for details.</b> |                                          |           |
| 19                           | RC_ID                                                                        | RC Identification Detection/             |           |
| 67                           | ECGP_SCLK                                                                    | General Purpose SPI Clock                |           |
| 69                           | ECGP_SIN                                                                     | General Purpose SPI Input                |           |
| 68                           | ECGP_SOUT                                                                    | General Purpose SPI Output               |           |
| 28                           | GPTP-IN1                                                                     | General Purpose Pass Through Port Input  |           |
| 30                           | GPTP-IN2                                                                     |                                          |           |
| 32                           | GPTP-IN3                                                                     |                                          |           |
| 108                          | GPTP-IN4                                                                     |                                          |           |
| 90                           | GPTP-IN5                                                                     |                                          |           |
| 75                           | GPTP-IN6                                                                     |                                          |           |
| 14                           | GPTP-IN7                                                                     |                                          |           |
| 16                           | GPTP-IN8                                                                     |                                          |           |
| 29                           | GPTP-OUT1                                                                    | General Purpose Pass Through Port Output |           |
| 31                           | GPTP-OUT2                                                                    |                                          |           |
| 33                           | GPTP-OUT3                                                                    |                                          |           |
| 109                          | GPTP-OUT4                                                                    |                                          |           |
| 89                           | GPTP-OUT5                                                                    |                                          |           |
| 76                           | GPTP-OUT6                                                                    |                                          |           |
| 15                           | GPTP-OUT7                                                                    |                                          |           |
| 17                           | GPTP-OUT8                                                                    |                                          |           |

Table 3.8 JTAG Interface

| JTAG Interface        |             |                              | (5 PINS)       |
|-----------------------|-------------|------------------------------|----------------|
| 128<br>VTQFP<br>Pin # | Signal Name | Description                  | Notes          |
| 105                   | JTAG_CLK    | JTAG Test Clock              | Note9          |
| 107                   | JTAG_RST#   | JTAG Test Reset (active low) | Note8<br>Note9 |
| 102                   | JTAG_TDI    | JTAG Test Data In            | Note9          |
| 103                   | JTAG_TDO    | JTAG Test Data Out           | Note9          |
| 106                   | JTAG_TMS    | JTAG Test Mode Select        | Note9          |
|                       |             |                              |                |

Table 3.9 MISC Interface

| MISC Interface  |             |                                 | (17 PINS) |
|-----------------|-------------|---------------------------------|-----------|
| 128 VTQFP Pin # | Signal Name | Description                     | Notes     |
| 92              | A20M        | KBD GATEA20 Output              |           |
| 50              | KBRST       | CPU_RESET                       |           |
| 114             | LED1        | LED output                      |           |
| 115             | LED2        | LED output                      |           |
| 110             | LED3        | LED output                      |           |
| 82              | MSCLK       | SMSC Proprietary EC debug port  | Note4     |
| 81              | MSDATA      | SMSC Proprietary EC debug port  | Note4     |
| 27              | UART_CLK    | UART CLK input                  |           |
| 71              | UART_RX     | UART RX Input                   |           |
| 70              | UART_TX     | UART TX Output                  | Note6     |
| 49              | VCC_PWRGD   | System Main Power Indication    |           |
| 19              | RC_ID       | RC Identification Detection     |           |
| 67              | ECGP_SCLK   | General Purpose SPI Clock       |           |
| 68              | ECGP_SOUT   | General Purpose SPI Output      |           |
| 69              | ECGP_SIN    | General Purpose SPI Input       |           |
| 123             | nFWP        | (Boot) Flash Write Protect      |           |
| 72              | nRESET_OUT  | EC-driven External System Reset |           |
|                 |             |                                 |           |

Table 3.10 PS/2 Interface

| PS/2 Interface  |             |                  | (10 PINS) |
|-----------------|-------------|------------------|-----------|
| 128 VTQFP Pin # | Signal Name | Description      | Notes     |
| 9               | PS2_CLK0B   | PS/2 clock ouput | Note11    |
| 10              | PS2_DAT0B   | PS/2 data        | Note11    |
| 75              | PS2_CLK2    | PS/2 clock ouput |           |
| 76              | PS2_DAT2    | PS/2 data        |           |
| 77              | PS2_CLK1A   | PS/2 clock ouput | Note11    |
| 78              | PS2_DAT1A   | PS/2 data        | Note11    |
| 79              | PS2_CLK0A   | PS/2 clock ouput | Note11    |
| 80              | PS2_DAT0A   | PS/2 data        | Note11    |
| 111             | PS2_CLK1B   | PS/2 clock ouput | Note11    |
| 112             | PS2_DAT1B   | PS/2 data        | Note11    |
|                 |             |                  |           |
|                 |             |                  |           |



Table 3.11 Power Switch Interface

| Dell Power Switch Interface |             |                                            | (7 PINS) |
|-----------------------------|-------------|--------------------------------------------|----------|
| 128<br>VTQFP<br>Pin #       | Signal Name | Description                                | Notes    |
| 128                         | VCI_OVRD_IN | Input can cause wakeup or interrupt event. | Note5    |
| 120                         | VCI_OUT     | OUTPUT from combinational logic and/or EC  |          |
| 118                         | BGPO0       | VCC0 driven GPO.                           |          |
| 127                         | VCI_IN0#    | Input can cause wakeup or interrupt event. | Note36   |
| 126                         | VCI_IN1#    | Input can cause wakeup or interrupt event. |          |
| 119                         | VCI_IN2#    | Input can cause wakeup or interrupt event. |          |
| 1                           | VCI_IN3#    | Input can cause wakeup or interrupt event. |          |
|                             |             |                                            |          |

Table 3.12 SMBus Interface





| SMBus Interface       |             |                                 | (28 PINS) |
|-----------------------|-------------|---------------------------------|-----------|
| 128<br>VTQFP<br>Pin # | Signal Name | Description                     | Notes     |
| 6                     | I2C1A_CLK   | SMBus Controller 1 Port A Clock |           |
| 5                     | I2C1A_DATA  | SMBus Controller 1 Port A Data  |           |
| 8                     | I2C1B_CLK   | SMBus Controller 1 Port B Clock |           |
| 7                     | I2C1B_DATA  | SMBus Controller 1 Port B Data  |           |
| 112                   | I2C1C_CLK   | SMBus Controller 1 Port C Clock |           |
| 111                   | I2C1C_DATA  | SMBus Controller 1 Port C Data  |           |
| 10                    | I2C1D_CLK   | SMBus Controller 1 Port D Clock |           |
| 9                     | I2C1D_DATA  | SMBus Controller 1 Port D Data  |           |
| 100                   | I2C1E_CLK   | SMBus Controller 1 Port E Clock |           |
| 99                    | I2C1E_DATA  | SMBus Controller 1 Port E Data  |           |
| 98                    | I2C1F_CLK   | SMBus Controller 1 Port F Clock |           |
| 97                    | I2C1F_DATA  | SMBus Controller 1 Port F Data  |           |
| 96                    | I2C1G_CLK   | SMBus Controller 1 Port G Clock |           |
| 95                    | I2C1G_DATA  | SMBus Controller 1 Port G Data  |           |
| 13                    | I2C1H_CLK   | SMBus Controller 1 Port H Clock |           |
| 12                    | I2C1H_DATA  | SMBus Controller 1 Port H Data  |           |
| 106                   | I2C1J_CLK   | SMBus Controller 1 Port J Clock |           |
| 105                   | I2C1J_DATA  | SMBus Controller 1 Port J Data  |           |
| 103                   | I2C1K_CLK   | SMBus Controller 1 Port K Clock |           |
| 102                   | I2C1K_DATA  | SMBus Controller 1 Port K Data  |           |
| 94                    | I2C2A_CLK   | SMBus Controller 2 Port A Clock |           |
| 93                    | I2C2A_DAT   | SMBus Controller 2 Port A Data  |           |
| 98                    | I2C2B_CLK   | SMBus Controller 2 Port B Clock |           |
| 97                    | I2C2B_DATA  | SMBus Controller 2 Port B Data  |           |
| 106                   | I2C2C_CLK   | SMBus Controller 2 Port C Clock |           |
| 105                   | I2C2C_DATA  | SMBus Controller 2 Port C Data  |           |
| 13                    | I2C2D_CLK   | SMBus Controller 2 Port D Clock |           |
| 12                    | I2C2D_DATA  | SMBus Controller 2 Port D Data  |           |

Table 3.13 Power Interface

| Power           |             |                                                     | (19 PINS) |
|-----------------|-------------|-----------------------------------------------------|-----------|
| 128 VTQFP Pin # | Signal Name | Description                                         | Notes     |
| 125             | AGND        | VBAT associated ground                              |           |
| 121             | VBAT        | VBAT supply                                         |           |
| 22              | VR_CAP[1]   | Capacitor Connection for Internal Voltage Regulator |           |
| 26              | VSS[1]      | VTR associated ground                               |           |
| 51              | VSS[2]      | VTR associated ground                               |           |
| 74              | VSS[3]      | VTR associated ground                               |           |
| 88              | VSS[4]      | VTR associated ground                               |           |
| 113             | VSS[5]      | VTR associated ground                               |           |
| 20              | VSS[7]      | VTR associated ground                               |           |
| 53              | VSS[8]      | VTR associated ground                               |           |
| 101             | VSS_RO      | VTR associated ground used for ring oscillator.     |           |
| 21              | VTR[1]      | VTR supply                                          |           |
| 44              | VTR[2]      | VTR supply                                          |           |
| 65              | VTR[3]      | VTR supply                                          |           |
| 83              | VTR[4]      | VTR supply                                          |           |
| 116             | VTR[5]      | VTR supply                                          |           |
| 104             | VTR[6]      | VTR supply                                          |           |
| 4               | VTR[7]      | VTR supply                                          |           |
| 52              | VTR[8]      | VTR supply                                          |           |

### 3.5 Pin Signal Function Multiplexing

This section describes the Multiplexing of Signal Pin Functions on the pins of the MEC5035. Signal Pin Functions are selected by the individual pin's [Pin Control Register](#). The [Pin Control Register](#) also controls all wakeup and interrupt events from the signal pins. See [Section 17.8.1, "Pin Control Register," on page 376](#) for programming control of multiplexing.

See [Section 3.6, "Notes from tables in this chapter," on page 64](#) for notes referenced in the tables in this section and in addition [Section 3.7, "General System/Layout pin Issues," on page 66](#).

Pin functions that exhibits power domain emulation have a different power supply designation in the "emulated pwr" column than "PWR" column of the Multiplexing Table[1:16] below. See [Section 3.7.1, "Pin Default State Through Power Transitions," on page 66](#) and [Section 3.7.2, "Alternate Function Pin State Through Power Transitions," on page 67](#) for description of Signal Pin Function States through Power Transitions.

#### "VCC" POWER DOMAIN EMULATION

Pin Signal Functions that exhibit "[VCC" power domain emulation](#)" are documented in the [Multiplexing Tables\[1:16\]](#) as PWR = VTR and emulated pwr = VCC. The System Runtime Supply power is not connected to the MEC5035. The VCC\_PWRGD signal is used to indicate when power is applied to the System Runtime Supply. All Pin Signal Functions that exhibit "[VCC" power domain emulation](#)" are powered by VTR and controlled by the VCC\_PWRGD signal input. "[VCC" power domain emulation](#)" Pin Signal Functions are tri-stated when VCC\_PWRGD is inactive and are functional when VCC\_PWRGD is active.

### "VTR" POWER DOMAIN EMULATION

Pin Signal Functions that exhibit "VTR" power domain emulation are documented in the [Multiplexing Tables\[1:16\]](#) as PWR = VBAT and emulated pwr = VTR. All Pin Signal Functions that exhibit "VTR" power domain emulation are powered by VBAT and controlled by the internal VTR POR. "VTR" power domain emulation Pin Signal Functions are tristated when VTR power is not applied and are functional when VTR power is applied.

## 3.5.1 Multiplexing Tables[1:16]

**Table 3.14 Multiplexing Table (1 of 16)**

| 128 pins<br>MEC5035 | MUX     | Signal     | Buffer Type   | PWR  | emulated<br>pwr | Notes |
|---------------------|---------|------------|---------------|------|-----------------|-------|
| 1                   | Default | VC1_IN3#   | I             | VBAT | VBAT            | Note5 |
| 1                   | Alt 1   |            |               |      |                 |       |
| 1                   | Alt 2   |            |               |      |                 |       |
| 1                   | Alt 3   |            |               |      |                 |       |
| 2                   | Default | GPIO001    | (I/O/OD)-8ma  | VTR  | VTR             |       |
| 2                   | Alt 1   |            |               |      |                 |       |
| 2                   | Alt 2   |            |               |      |                 |       |
| 2                   | Alt 3   |            |               |      |                 |       |
| 3                   | Default | GPIO002    | (I/O/OD)-8ma  | VTR  | VTR             |       |
| 3                   | Alt 1   |            |               |      |                 |       |
| 3                   | Alt 2   |            |               |      |                 |       |
| 3                   | Alt 3   |            |               |      |                 |       |
| 4                   | Default | VTR[7]     | PWR           | PWR  | PWR             |       |
| 4                   | Alt 1   |            |               |      |                 |       |
| 4                   | Alt 2   |            |               |      |                 |       |
| 4                   | Alt 3   |            |               |      |                 |       |
| 5                   | Default | GPIO003    | (I/O/OD)-12ma | VTR  | VTR             |       |
| 5                   | Alt 1   | I2C1A_DATA | (I/OD)-12ma   | VTR  | VTR             |       |
| 5                   | Alt 2   |            |               |      |                 |       |
| 5                   | Alt 3   |            |               |      |                 |       |
| 6                   | Default | GPIO004    | (I/O/OD)-12ma | VTR  | VTR             |       |
| 6                   | Alt 1   | I2C1A_CLK  | (I/OD)-12ma   | VTR  | VTR             |       |
| 6                   | Alt 2   |            |               |      |                 |       |
| 6                   | Alt 3   |            |               |      |                 |       |
| 7                   | Default | GPIO005    | (I/O/OD)-12ma | VTR  | VTR             |       |
| 7                   | Alt 1   | I2C1B_DATA | (I/OD)-12ma   | VTR  | VTR             |       |
| 7                   | Alt 2   |            |               |      |                 |       |
| 7                   | Alt 3   |            |               |      |                 |       |
| 8                   | Default | GPIO006    | (I/O/OD)-12ma | VTR  | VTR             |       |
| 8                   | Alt 1   | I2C1B_CLK  | (I/OD)-12ma   | VTR  | VTR             |       |
| 8                   | Alt 2   |            |               |      |                 |       |
| 8                   | Alt 3   |            |               |      |                 |       |



## Product Customer Specification-ODM

Table 3.15 Multiplexing Table (2 of 16)

| 128 pins<br>MEC5035 | MUX     | Signal     | Buffer Type   | PWR | emulated<br>pwr | Notes  |
|---------------------|---------|------------|---------------|-----|-----------------|--------|
| 9                   | Default | GPIO007    | (I/O/OD)-12ma | VTR | VTR             |        |
| 9                   | Alt 1   | I2C1D_DATA | (I/OD)-12ma   | VTR | VTR             |        |
| 9                   | Alt 2   | PS2_CLK0B  | (I/OD)-12ma   | VTR | VTR             | Note11 |
| 9                   | Alt 3   |            |               |     |                 |        |
| 10                  | Default | GPIO010    | (I/O/OD)-12ma | VTR | VTR             |        |
| 10                  | Alt 1   | I2C1D_CLK  | (I/OD)-12ma   | VTR | VTR             |        |
| 10                  | Alt 2   | PS2_DAT0B  | (I/OD)-12ma   | VTR | VTR             | Note11 |
| 10                  | Alt 3   |            |               |     |                 |        |
| 11                  | Default | GPIO011    | (I/O/OD)-12ma | VTR | VTR             |        |
| 11                  | Alt 1   | nSMI       | OD-12ma       | VTR | VTR             |        |
| 11                  | Alt 2   |            |               |     |                 |        |
| 11                  | Alt 3   |            |               |     |                 |        |
| 12                  | Default | GPIO012    | (I/O/OD)-12ma | VTR | VTR             |        |
| 12                  | Alt 1   | I2C1H_DATA | (I/OD)-12ma   | VTR | VTR             |        |
| 12                  | Alt 2   | I2C2D_DATA | (I/OD)-12ma   | VTR | VTR             |        |
| 12                  | Alt 3   |            |               |     |                 |        |
| 13                  | Default | GPIO013    | (I/O/OD)-12ma | VTR | VTR             |        |
| 13                  | Alt 1   | I2C1H_CLK  | (I/OD)-12ma   | VTR | VTR             |        |
| 13                  | Alt 2   | I2C2D_CLK  | (I/OD)-12ma   | VTR | VTR             |        |
| 13                  | Alt 3   |            |               |     |                 |        |
| 14                  | Default | GPIO014    | (I/O/OD)-8ma  | VTR | VTR             |        |
| 14                  | Alt 1   | GPTP-IN7   | I-8ma         | VTR | VTR             |        |
| 14                  | Alt 2   |            |               |     |                 |        |
| 14                  | Alt 3   |            |               |     |                 |        |
| 15                  | Default | GPIO015    | (I/O/OD)-8ma  | VTR | VTR             |        |
| 15                  | Alt 1   | GPTP-OUT7  | (O/OD)-8ma    | VTR | VTR             |        |
| 15                  | Alt 2   |            |               |     |                 |        |
| 15                  | Alt 3   |            |               |     |                 |        |
| 16                  | Default | GPIO016    | (I/O/OD)-8ma  | VTR | VTR             |        |
| 16                  | Alt 1   | GPTP-IN8   | I-8ma         | VTR | VTR             |        |
| 16                  | Alt 2   |            |               |     |                 |        |
| 16                  | Alt 3   |            |               |     |                 |        |



Table 3.16 Multiplexing Table (3 of 16)

| 128 pins<br>MEC5035 | MUX     | Signal    | Buffer Type   | PWR | emulated<br>pwr | Notes |
|---------------------|---------|-----------|---------------|-----|-----------------|-------|
| 17                  | Default | GPIO017   | (I/O/OD)-8ma  | VTR | VTR             |       |
| 17                  | Alt 1   | GPTP-OUT8 | (O/OD)-8ma    | VTR | VTR             |       |
| 17                  | Alt 2   |           |               |     |                 |       |
| 17                  | Alt 3   |           |               |     |                 |       |
| 18                  | Default | GPIO020   | (I/O/OD)-8ma  | VTR | VTR             |       |
| 18                  | Alt 1   |           |               |     |                 |       |
| 18                  | Alt 2   |           |               |     |                 |       |
| 18                  | Alt 3   |           |               |     |                 |       |
| 19                  | Default | GPIO021   | (I/O/OD)-12ma | VTR | VTR             |       |
| 19                  | Alt 1   | RC_ID     | (I/OD)-12ma   | VTR | VTR             |       |
| 19                  | Alt 2   |           |               |     |                 |       |
| 19                  | Alt 3   |           |               |     |                 |       |
| 20                  | Default | VSS[7]    | PWR           | PWR | PWR             |       |
| 20                  | Alt 1   |           |               |     |                 |       |
| 20                  | Alt 2   |           |               |     |                 |       |
| 20                  | Alt 3   |           |               |     |                 |       |
| 21                  | Default | VTR[1]    | PWR           | PWR | PWR             |       |
| 21                  | Alt 1   |           |               |     |                 |       |
| 21                  | Alt 2   |           |               |     |                 |       |
| 21                  | Alt 3   |           |               |     |                 |       |
| 22                  | Default | VR_CAP[1] | PWR           | PWR | PWR             |       |
| 22                  | Alt 1   |           |               |     |                 |       |
| 22                  | Alt 2   |           |               |     |                 |       |
| 22                  | Alt 3   |           |               |     |                 |       |
| 23                  | Default | GPIO022   | (I/O/OD)-16ma | VTR | VTR             |       |
| 23                  | Alt 1   | BCM_B_CLK | O-16ma        | VTR | VTR             |       |
| 23                  | Alt 2   |           |               |     |                 |       |
| 23                  | Alt 3   |           |               |     |                 |       |
| 24                  | Default | GPIO023   | (I/O/OD)-16ma | VTR | VTR             |       |
| 24                  | Alt 1   | BCM_B_DAT | IO-16ma       | VTR | VTR             | Note3 |
| 24                  | Alt 2   |           |               |     |                 |       |
| 24                  | Alt 3   |           |               |     |                 |       |



Table 3.17 Multiplexing Table (4 of 16)

| 128 pins<br>MEC5035 | MUX     | Signal     | Buffer Type   | PWR | emulated<br>pwr | Notes |
|---------------------|---------|------------|---------------|-----|-----------------|-------|
| 25                  | Default | GPIO024    | (I/O/OD)-16ma | VTR | VTR             |       |
| 25                  | Alt 1   | BCM_B_INT# | I-16ma        | VTR | VTR             |       |
| 25                  | Alt 2   |            |               |     |                 |       |
| 25                  | Alt 3   |            |               |     |                 |       |
| 26                  | Default | VSS[1]     | PWR           | PWR | PWR             |       |
| 26                  | Alt 1   |            |               |     |                 |       |
| 26                  | Alt 2   |            |               |     |                 |       |
| 26                  | Alt 3   |            |               |     |                 |       |
| 27                  | Default | GPIO025    | (I/O/OD)-8ma  | VTR | VTR             |       |
| 27                  | Alt 1   | UART_CLK   | I-8ma         | VTR | VTR             |       |
| 27                  | Alt 2   |            |               |     |                 |       |
| 27                  | Alt 3   |            |               |     |                 |       |
| 28                  | Default | GPIO026    | (I/O/OD)-8ma  | VTR | VTR             |       |
| 28                  | Alt 1   | GPTP-IN1   | I-8ma         | VTR | VTR             |       |
| 28                  | Alt 2   |            |               |     |                 |       |
| 28                  | Alt 3   |            |               |     |                 |       |
| 29                  | Default | GPIO027    | (I/O/OD)-8ma  | VTR | VTR             |       |
| 29                  | Alt 1   | GPTP-OUT1  | (O/OD)-8ma    | VTR | VTR             |       |
| 29                  | Alt 2   |            |               |     |                 |       |
| 29                  | Alt 3   |            |               |     |                 |       |
| 30                  | Default | GPIO030    | (I/O/OD)-8ma  | VTR | VTR             |       |
| 30                  | Alt 1   | GPTP-IN2   | I-8ma         | VTR | VTR             |       |
| 30                  | Alt 2   |            |               |     |                 |       |
| 30                  | Alt 3   |            |               |     |                 |       |
| 31                  | Default | GPIO031    | (I/O/OD)-8ma  | VTR | VTR             |       |
| 31                  | Alt 1   | GPTP-OUT2  | (O/OD)-8ma    | VTR | VTR             |       |
| 31                  | Alt 2   |            |               |     |                 |       |
| 31                  | Alt 3   |            |               |     |                 |       |
| 32                  | Default | GPIO032    | (I/O/OD)-8ma  | VTR | VTR             |       |
| 32                  | Alt 1   | GPTP-IN3   | I-8ma         | VTR | VTR             |       |
| 32                  | Alt 2   |            |               |     |                 |       |
| 32                  | Alt 3   |            |               |     |                 |       |



Table 3.18 Multiplexing Table (5 of 16)

| 128 pins<br>MEC5035 | MUX     | Signal       | Buffer Type   | PWR | emulated<br>pwr | Notes |
|---------------------|---------|--------------|---------------|-----|-----------------|-------|
| 33                  | Default | GPIO040      | (I/O/OD)-8ma  | VTR | VTR             |       |
| 33                  | Alt 1   | GPTP-OUT3    | (O/OD)-8ma    | VTR | VTR             |       |
| 33                  | Alt 2   |              |               |     |                 |       |
| 33                  | Alt 3   |              |               |     |                 |       |
| 34                  | Default | GPIO041      | (I/O/OD)-8ma  | VTR | VTR             |       |
| 34                  | Alt 1   |              |               |     |                 |       |
| 34                  | Alt 2   |              |               |     |                 |       |
| 34                  | Alt 3   |              |               |     |                 |       |
| 35                  | Default | GPIO042      | I-8ma         | VTR | VTR             |       |
| 35                  | Alt 1   | BCM_C_INT#   | I-8ma         | VTR | VTR             |       |
| 35                  | Alt 2   |              |               |     |                 |       |
| 35                  | Alt 3   |              |               |     |                 |       |
| 36                  | Default | GPIO043      | I-16ma        | VTR | VTR             |       |
| 36                  | Alt 1   | BCM_C_DAT    | I/O-16ma      | VTR | VTR             | Note3 |
| 36                  | Alt 2   |              |               |     |                 |       |
| 36                  | Alt 3   |              |               |     |                 |       |
| 37                  | Default | GPIO044      | (I/O/OD)-16ma | VTR | VTR             |       |
| 37                  | Alt 1   | BCM_C_CLK    | O-16ma        | VTR | VTR             |       |
| 37                  | Alt 2   |              |               |     |                 |       |
| 37                  | Alt 3   |              |               |     |                 |       |
| 38                  | Default | GPIO045      | I-8ma         | VTR | VTR             |       |
| 38                  | Alt 1   | LSBCM_D_INT# | I-8ma         | VTR | VTR             |       |
| 38                  | Alt 2   |              |               |     |                 |       |
| 38                  | Alt 3   |              |               |     |                 |       |
| 39                  | Default | GPIO046      | I-8ma         | VTR | VTR             |       |
| 39                  | Alt 1   | LSBCM_D_DAT  | I/O-8ma       | VTR | VTR             | Note3 |
| 39                  | Alt 2   |              |               |     |                 |       |
| 39                  | Alt 3   |              |               |     |                 |       |
| 40                  | Default | GPIO047      | I-8ma         | VTR | VTR             |       |
| 40                  | Alt 1   | LSBCM_D_CLK  | O-8ma         | VTR | VTR             |       |
| 40                  | Alt 2   |              |               |     |                 |       |
| 40                  | Alt 3   |              |               |     |                 |       |

Table 3.19 Multiplexing Table (6 of 16)

| 128 pins<br>MEC5035 | MUX     | Signal    | Buffer Type   | PWR | emulated<br>pwr | Notes |
|---------------------|---------|-----------|---------------|-----|-----------------|-------|
| 41                  | Default | GPIO050   | (I/O/OD)-8ma  | VTR | VTR             |       |
| 41                  | Alt 1   | FAN_TACH1 | I-8ma         | VTR | VTR             |       |
| 41                  | Alt 2   |           |               |     |                 |       |
| 41                  | Alt 3   |           |               |     |                 |       |
| 42                  | Default | GPIO051   | (I/O/OD)-8ma  | VTR | VTR             |       |
| 42                  | Alt 1   | FAN_TACH2 | I-8ma         | VTR | VTR             |       |
| 42                  | Alt 2   |           |               |     |                 |       |
| 42                  | Alt 3   |           |               |     |                 |       |
| 43                  | Default | GPIO052   | (I/O/OD)-8ma  | VTR | VTR             |       |
| 43                  | Alt 1   | FAN_TACH3 | I-8ma         | VTR | VTR             |       |
| 43                  | Alt 2   |           |               |     |                 |       |
| 43                  | Alt 3   |           |               |     |                 |       |
| 44                  | Default | VTR[2]    | PWR           | PWR | PWR             |       |
| 44                  | Alt 1   |           |               |     |                 |       |
| 44                  | Alt 2   |           |               |     |                 |       |
| 44                  | Alt 3   |           |               |     |                 |       |
| 45                  | Default | GPIO053   | (I/O/OD)-12ma | VTR | VTR             |       |
| 45                  | Alt 1   | PWM0      | (O/OD)-12ma   | VTR | VTR             |       |
| 45                  | Alt 2   |           |               |     |                 |       |
| 45                  | Alt 3   |           |               |     |                 |       |
| 46                  | Default | GPIO054   | (I/O/OD)-12ma | VTR | VTR             |       |
| 46                  | Alt 1   | PWM1      | (O/OD)-12ma   | VTR | VTR             |       |
| 46                  | Alt 2   |           |               |     |                 |       |
| 46                  | Alt 3   |           |               |     |                 |       |
| 47                  | Default | GPIO055   | (I/O/OD)-12ma | VTR | VTR             |       |
| 47                  | Alt 1   | PWM2      | (O/OD)-12ma   | VTR | VTR             |       |
| 47                  | Alt 2   |           |               |     |                 |       |
| 47                  | Alt 3   |           |               |     |                 |       |
| 48                  | Default | GPIO056   | (I/O/OD)-12ma | VTR | VTR             |       |
| 48                  | Alt 1   | PWM3      | (O/OD)-12ma   | VTR | VTR             |       |
| 48                  | Alt 2   |           |               |     |                 |       |
| 48                  | Alt 3   |           |               |     |                 |       |





Table 3.20 Multiplexing Table (7 of 16)

| 128 pins<br>MEC5035 | MUX     | Signal    | Buffer Type  | PWR | emulated<br>pwr | Notes          |
|---------------------|---------|-----------|--------------|-----|-----------------|----------------|
| 49                  | Default | VCC_PWRGD | I            | VTR | VTR             | Note5          |
| 49                  | Alt 1   |           |              |     |                 |                |
| 49                  | Alt 2   |           |              |     |                 |                |
| 49                  | Alt 3   |           |              |     |                 |                |
| 50                  | Default | GPIO060   | (I/O/OD)-8ma | VTR | VTR             |                |
| 50                  | Alt 1   | KBRST     | OD-8ma       | VTR | VCC             |                |
| 50                  | Alt 2   |           |              |     |                 |                |
| 50                  | Alt 3   |           |              |     |                 |                |
| 51                  | Default | VSS[2]    | PWR          | PWR | PWR             |                |
| 51                  | Alt 1   |           |              |     |                 |                |
| 51                  | Alt 2   |           |              |     |                 |                |
| 51                  | Alt 3   |           |              |     |                 |                |
| 52                  | Default | VTR[8]    | PWR          | PWR | PWR             |                |
| 52                  | Alt 1   |           |              |     |                 |                |
| 52                  | Alt 2   |           |              |     |                 |                |
| 52                  | Alt 3   |           |              |     |                 |                |
| 53                  | Default | VSS[8]    | PWR          | PWR | PWR             |                |
| 53                  | Alt 1   |           |              |     |                 |                |
| 53                  | Alt 2   |           |              |     |                 |                |
| 53                  | Alt 3   |           |              |     |                 |                |
| 54                  | Default | GPIO061   | (I/O/OD)-8ma | VTR | VTR             |                |
| 54                  | Alt 1   | LPCPD#    | I-8ma        | VTR | VCC             |                |
| 54                  | Alt 2   |           |              |     |                 |                |
| 54                  | Alt 3   |           |              |     |                 |                |
| 55                  | Default | LDRQ#     | PCI_O        | VTR | VCC             | Note5<br>Note7 |
| 55                  | Alt 1   |           |              |     |                 |                |
| 55                  | Alt 2   |           |              |     |                 |                |
| 55                  | Alt 3   |           |              |     |                 |                |
| 56                  | Default | SER_IRQ   | PCI_IO       | VTR | VCC             | Note5<br>Note7 |
| 56                  | Alt 1   |           |              |     |                 |                |
| 56                  | Alt 2   |           |              |     |                 |                |
| 56                  | Alt 3   |           |              |     |                 |                |



Table 3.21 Multiplexing Table (8 of 16)

| 128 pins<br>MEC5035 | MUX     | Signal  | Buffer Type | PWR | emulated<br>pwr | Notes          |
|---------------------|---------|---------|-------------|-----|-----------------|----------------|
| 57                  | Default | LRESET# | PCI_I       | VTR | VCC             | Note5<br>Note7 |
| 57                  | Alt 1   |         |             |     |                 |                |
| 57                  | Alt 2   |         |             |     |                 |                |
| 57                  | Alt 3   |         |             |     |                 |                |
| 58                  | Default | PCI_CLK | PCI_ICLK    | VTR | VCC             | Note5<br>Note7 |
| 58                  | Alt 1   |         |             |     |                 |                |
| 58                  | Alt 2   |         |             |     |                 |                |
| 58                  | Alt 3   |         |             |     |                 |                |
| 59                  | Default | LFRAME# | PCI_I       | VTR | VCC             | Note5<br>Note7 |
| 59                  | Alt 1   |         |             |     |                 |                |
| 59                  | Alt 2   |         |             |     |                 |                |
| 59                  | Alt 3   |         |             |     |                 |                |
| 60                  | Default | LAD0    | PCI_IO      | VTR | VCC             |                |
| 60                  | Alt 1   |         |             |     |                 |                |
| 60                  | Alt 2   |         |             |     |                 |                |
| 60                  | Alt 3   |         |             |     |                 |                |
| 61                  | Default | LAD1    | PCI_IO      | VTR | VCC             |                |
| 61                  | Alt 1   |         |             |     |                 |                |
| 61                  | Alt 2   |         |             |     |                 |                |
| 61                  | Alt 3   |         |             |     |                 |                |
| 62                  | Default | LAD2    | PCI_IO      | VTR | VCC             |                |
| 62                  | Alt 1   |         |             |     |                 |                |
| 62                  | Alt 2   |         |             |     |                 |                |
| 62                  | Alt 3   |         |             |     |                 |                |
| 63                  | Default | LAD3    | PCI_IO      | VTR | VCC             |                |
| 63                  | Alt 1   |         |             |     |                 |                |
| 63                  | Alt 2   |         |             |     |                 |                |
| 63                  | Alt 3   |         |             |     |                 |                |
| 64                  | Default | CLKRUN# | PCI_OD      | VTR | VCC             | Note5<br>Note7 |
| 64                  | Alt 1   |         |             |     |                 |                |
| 64                  | Alt 2   |         |             |     |                 |                |
| 64                  | Alt 3   |         |             |     |                 |                |

Table 3.22 Multiplexing Table (9 of 16)

| 128 pins<br>MEC5035 | MUX     | Signal     | Buffer Type   | PWR | emulated<br>pwr | Notes |
|---------------------|---------|------------|---------------|-----|-----------------|-------|
| 65                  | Default | VTR[3]     | PWR           | PWR | PWR             |       |
| 65                  | Alt 1   |            |               |     |                 |       |
| 65                  | Alt 2   |            |               |     |                 |       |
| 65                  | Alt 3   |            |               |     |                 |       |
| 66                  | Default | GPIO100    | IO8/IOD8      | VTR | VTR             |       |
| 66                  | Alt 1   | nEC_SCI    | PCI_OD        | VTR | VTR             | Note1 |
| 66                  | Alt 2   |            |               |     |                 |       |
| 66                  | Alt 3   |            |               |     |                 |       |
| 67                  | Default | GPIO101    | (I/O/OD)-8ma  | VTR | VTR             |       |
| 67                  | Alt 1   | ECGP_SCLK  | O-8ma         | VTR | VTR             |       |
| 67                  | Alt 2   |            |               |     |                 |       |
| 67                  | Alt 3   |            |               |     |                 |       |
| 68                  | Default | GPIO102    | (I/O/OD)-8ma  | VTR | VTR             |       |
| 68                  | Alt 1   | ECGP_SOUT  | (I/O/OD)-8ma  | VTR | VTR             |       |
| 68                  | Alt 2   |            |               |     |                 |       |
| 68                  | Alt 3   |            |               |     |                 |       |
| 69                  | Default | GPIO103    | (I/O/OD)-8ma  | VTR | VTR             |       |
| 69                  | Alt 1   | ECGP_SIN   | (I/O/OD)-8ma  | VTR | VTR             |       |
| 69                  | Alt 2   |            |               |     |                 |       |
| 69                  | Alt 3   |            |               |     |                 |       |
| 70                  | Default | GPIO104    | (I/O/OD)-12ma | VTR | VTR             |       |
| 70                  | Alt 1   | UART_TX    | O-12ma        | VTR | (VTR/VCC)       | Note6 |
| 70                  | Alt 2   |            |               |     |                 |       |
| 70                  | Alt 3   |            |               |     |                 |       |
| 71                  | Default | GPIO105    | (I/O/OD)-8ma  | VTR | VTR             |       |
| 71                  | Alt 1   | UART_RX    | I-8ma         | VTR | VTR             | Note6 |
| 71                  | Alt 2   |            |               |     |                 |       |
| 71                  | Alt 3   |            |               |     |                 |       |
| 72                  | Default | GPIO106    | (I/O/OD)-8ma  | VTR | VTR             |       |
| 72                  | Alt 1   | nRESET_OUT | O-8ma         | VTR | VTR             |       |
| 72                  | Alt 2   |            |               |     |                 |       |
| 72                  | Alt 3   |            |               |     |                 |       |



Table 3.23 Multiplexing Table (10 of 16)

| 128 pins<br>MEC5035 | MUX     | Signal    | Buffer Type   | PWR | emulated<br>pwr | Notes  |
|---------------------|---------|-----------|---------------|-----|-----------------|--------|
| 73                  | Default | GPIO107   | (I/O/OD)-8ma  | VTR | VTR             |        |
| 73                  | Alt 1   |           |               |     |                 |        |
| 73                  | Alt 2   |           |               |     |                 |        |
| 73                  | Alt 3   |           |               |     |                 |        |
| 74                  | Default | VSS[3]    | PWR           | PWR | PWR             |        |
| 74                  | Alt 1   |           |               |     |                 |        |
| 74                  | Alt 2   |           |               |     |                 |        |
| 74                  | Alt 3   |           |               |     |                 |        |
| 75                  | Default | GPIO110   | (I/O/OD)-16ma | VTR | VTR             |        |
| 75                  | Alt 1   | PS2_CLK2  | (I/OD)-16ma   | VTR | VTR             |        |
| 75                  | Alt 2   | GPTP-IN6  | I-16ma        | VTR | VTR             |        |
| 75                  | Alt 3   |           |               |     |                 |        |
| 76                  | Default | GPIO111   | (I/O/OD)-16ma | VTR | VTR             |        |
| 76                  | Alt 1   | PS2_DAT2  | (I/OD)-16ma   | VTR | VTR             |        |
| 76                  | Alt 2   | GPTP-OUT6 | (O/OD)-16ma   | VTR | VTR             |        |
| 76                  | Alt 3   |           |               |     |                 |        |
| 77                  | Default | GPIO112   | (I/O/OD)-12ma | VTR | VTR             |        |
| 77                  | Alt 1   | PS2_CLK1A | (I/O/OD)-12ma | VTR | VTR             | Note11 |
| 77                  | Alt 2   |           |               |     |                 |        |
| 77                  | Alt 3   |           |               |     |                 |        |
| 78                  | Default | GPIO113   | (I/O/OD)-12ma | VTR | VTR             |        |
| 78                  | Alt 1   | PS2_DAT1A | (I/O/OD)-12ma | VTR | VTR             | Note11 |
| 78                  | Alt 2   |           |               |     |                 |        |
| 78                  | Alt 3   |           |               |     |                 |        |
| 79                  | Default | GPIO114   | (I/O/OD)-12ma | VTR | VTR             |        |
| 79                  | Alt 1   | PS2_CLK0A | (I/OD)-12ma   | VTR | VTR             | Note11 |
| 79                  | Alt 2   |           |               |     |                 |        |
| 79                  | Alt 3   |           |               |     |                 |        |
| 80                  | Default | GPIO115   | (I/O/OD)-12ma | VTR | VTR             |        |
| 80                  | Alt 1   | PS2_DAT0A | (I/OD)-12ma   | VTR | VTR             | Note11 |
| 80                  | Alt 2   |           |               |     |                 |        |
| 80                  | Alt 3   |           |               |     |                 |        |



Table 3.24 Multiplexing Table (11 of 16)

| 128 pins<br>MEC5035 | MUX     | Signal     | Buffer Type   | PWR | emulated<br>pwr | Notes |
|---------------------|---------|------------|---------------|-----|-----------------|-------|
| 81                  | Default | GPIO116    | (I/O/OD)-16ma | VTR | VTR             |       |
| 81                  | Alt 1   | MSDATA     | O-16ma        | VTR | VTR             | Note4 |
| 81                  | Alt 2   |            |               |     |                 |       |
| 81                  | Alt 3   |            |               |     |                 |       |
| 82                  | Default | GPIO117    | (I/O/OD)-16ma | VTR | VTR             |       |
| 82                  | Alt 1   | MSCLK      | O-16ma        | VTR | VTR             | Note4 |
| 82                  | Alt 2   |            |               |     |                 |       |
| 82                  | Alt 3   |            |               |     |                 |       |
| 83                  | Default | VTR[4]     | PWR           | PWR | PWR             |       |
| 83                  | Alt 1   |            |               |     |                 |       |
| 83                  | Alt 2   |            |               |     |                 |       |
| 83                  | Alt 3   |            |               |     |                 |       |
| 84                  | Default | GPIO120    | (I/O/OD)-8ma  | VTR | VTR             |       |
| 84                  | Alt 1   |            |               |     |                 |       |
| 84                  | Alt 2   |            |               |     |                 |       |
| 84                  | Alt 3   |            |               |     |                 |       |
| 85                  | Default | GPIO121    | I-8ma         | VTR | VTR             |       |
| 85                  | Alt 1   | BCM_A_INT# | I-8ma         | VTR | VTR             |       |
| 85                  | Alt 2   |            |               |     |                 |       |
| 85                  | Alt 3   |            |               |     |                 |       |
| 86                  | Default | GPIO122    | I-16ma        | VTR | VTR             |       |
| 86                  | Alt 1   | BCM_A_DAT  | IO-16ma       | VTR | VTR             | Note3 |
| 86                  | Alt 2   |            |               |     |                 |       |
| 86                  | Alt 3   |            |               |     |                 |       |
| 87                  | Default | GPIO123    | I-16ma        | VTR | VTR             |       |
| 87                  | Alt 1   | BCM_A_CLK  | O-16ma        | VTR | VTR             |       |
| 87                  | Alt 2   |            |               |     |                 |       |
| 87                  | Alt 3   |            |               |     |                 |       |
| 88                  | Default | VSS[4]     | PWR           | PWR | PWR             |       |
| 88                  | Alt 1   |            |               |     |                 |       |
| 88                  | Alt 2   |            |               |     |                 |       |
| 88                  | Alt 3   |            |               |     |                 |       |



Table 3.25 Multiplexing Table (12 of 16)

| 128 pins<br>MEC5035 | MUX     | Signal     | Buffer Type   | PWR | emulated<br>pwr | Notes |
|---------------------|---------|------------|---------------|-----|-----------------|-------|
| 89                  | Default | GPIO124    | (I/O/OD)-8ma  | VTR | VTR             |       |
| 89                  | Alt 1   | GPTP-OUT5  | (O/OD)-8ma    | VTR | VTR             |       |
| 89                  | Alt 2   |            |               |     |                 |       |
| 89                  | Alt 3   |            |               |     |                 |       |
| 90                  | Default | GPIO125    | (I/O/OD)-8ma  | VTR | VTR             |       |
| 90                  | Alt 1   | GPTP-IN5   | I-8ma         | VTR | VTR             |       |
| 90                  | Alt 2   |            |               |     |                 |       |
| 90                  | Alt 3   |            |               |     |                 |       |
| 91                  | Default | GPIO126    | (I/O/OD)-8ma  | VTR | VTR             |       |
| 91                  | Alt 1   |            |               |     |                 |       |
| 91                  | Alt 2   |            |               |     |                 |       |
| 91                  | Alt 3   |            |               |     |                 |       |
| 92                  | Default | GPIO127    | (I/O/OD)-8ma  | VTR | VTR             |       |
| 92                  | Alt 1   | A20M       | O-8ma         | VTR | VCC             |       |
| 92                  | Alt 2   |            |               |     |                 |       |
| 92                  | Alt 3   |            |               |     |                 |       |
| 93                  | Default | GPIO130    | (I/O/OD)-12ma | VTR | VTR             |       |
| 93                  | Alt 1   | I2C2A_DAT  | (I/OD)-12ma   | VTR | VTR             |       |
| 93                  | Alt 2   |            |               |     |                 |       |
| 93                  | Alt 3   |            |               |     |                 |       |
| 94                  | Default | GPIO131    | (I/O/OD)-12ma | VTR | VTR             |       |
| 94                  | Alt 1   | I2C2A_CLK  | (I/OD)-12ma   | VTR | VTR             |       |
| 94                  | Alt 2   |            |               |     |                 |       |
| 94                  | Alt 3   |            |               |     |                 |       |
| 95                  | Default | GPIO132    | (I/O/OD)-12ma | VTR | VTR             |       |
| 95                  | Alt 1   | I2C1G_DATA | (I/OD)-12ma   | VTR | VTR             |       |
| 95                  | Alt 2   |            |               |     |                 |       |
| 95                  | Alt 3   |            |               |     |                 |       |
| 96                  | Default | GPIO140    | (I/O/OD)-12ma | VTR | VTR             |       |
| 96                  | Alt 1   | I2C1G_CLK  | (I/OD)-12ma   | VTR | VTR             |       |
| 96                  | Alt 2   |            |               |     |                 |       |
| 96                  | Alt 3   |            |               |     |                 |       |

Table 3.26 Multiplexing Table (13 of 16)

| 128 pins<br>MEC5035 | MUX     | Signal     | Buffer Type   | PWR | emulated<br>pwr | Notes |
|---------------------|---------|------------|---------------|-----|-----------------|-------|
| 97                  | Default | GPIO141    | (I/O/OD)-12ma | VTR | VTR             |       |
| 97                  | Alt 1   | I2C1F_DATA | (I/OD)-12ma   | VTR | VTR             |       |
| 97                  | Alt 2   | I2C2B_DATA | (I/OD)-12ma   | VTR | VTR             |       |
| 97                  | Alt 3   |            |               |     |                 |       |
| 98                  | Default | GPIO142    | (I/O/OD)-12ma | VTR | VTR             |       |
| 98                  | Alt 1   | I2C1F_CLK  | (I/OD)-12ma   | VTR | VTR             |       |
| 98                  | Alt 2   | I2C2B_CLK  | (I/OD)-12ma   | VTR | VTR             |       |
| 98                  | Alt 3   |            |               |     |                 |       |
| 99                  | Default | GPIO143    | (I/O/OD)-12ma | VTR | VTR             |       |
| 99                  | Alt 1   | I2C1E_DATA | (I/OD)-12ma   | VTR | VTR             |       |
| 99                  | Alt 2   |            |               |     |                 |       |
| 99                  | Alt 3   |            |               |     |                 |       |
| 100                 | Default | GPIO144    | (I/O/OD)-12ma | VTR | VTR             |       |
| 100                 | Alt 1   | I2C1E_CLK  | (I/OD)-12ma   | VTR | VTR             |       |
| 100                 | Alt 2   |            |               |     |                 |       |
| 100                 | Alt 3   |            |               |     |                 |       |
| 101                 | Default | VSS_RO     | PWR           | PWR | PWR             |       |
| 101                 | Alt 1   |            |               |     |                 |       |
| 101                 | Alt 2   |            |               |     |                 |       |
| 101                 | Alt 3   |            |               |     |                 |       |
| 102                 | Default | GPIO145    | (I/O/OD)-12ma | VTR | VTR             |       |
| 102                 | Alt 1   | I2C1K_DATA | (I/OD)-12ma   | VTR | VTR             |       |
| 102                 | Alt 2   | JTAG_TDI   | I-12ma        | VTR | VTR             | Note9 |
| 102                 | Alt 3   |            |               |     |                 |       |
| 103                 | Default | GPIO146    | (I/O/OD)-12ma | VTR | VTR             |       |
| 103                 | Alt 1   | I2C1K_CLK  | (I/OD)-12ma   | VTR | VTR             |       |
| 103                 | Alt 2   | JTAG_TDO   | O-12ma        | VTR | VTR             | Note9 |
| 103                 | Alt 3   |            |               |     |                 |       |
| 104                 | Default | VTR[6]     | PWR           | PWR | PWR             |       |
| 104                 | Alt 1   |            |               |     |                 |       |
| 104                 | Alt 2   |            |               |     |                 |       |
| 104                 | Alt 3   |            |               |     |                 |       |



Table 3.27 Multiplexing Table (14 of 16)

| 128 pins<br>MEC5035 | MUX     | Signal     | Buffer Type   | PWR | emulated<br>pwr | Notes          |
|---------------------|---------|------------|---------------|-----|-----------------|----------------|
| 105                 | Default | GPIO147    | (I/O/OD)-12ma | VTR | VTR             |                |
| 105                 | Alt 1   | I2C1J_DATA | (I/OD)-12ma   | VTR | VTR             |                |
| 105                 | Alt 2   | I2C2C_DATA | (I/OD)-12ma   | VTR | VTR             |                |
| 105                 | Alt 3   | JTAG_CLK   | I-12ma        | VTR | VTR             | Note9          |
| 106                 | Default | GPIO150    | (I/O/OD)-12ma | VTR | VTR             |                |
| 106                 | Alt 1   | I2C1J_CLK  | (I/OD)-12ma   | VTR | VTR             |                |
| 106                 | Alt 2   | I2C2C_CLK  | (I/OD)-12ma   | VTR | VTR             |                |
| 106                 | Alt 3   | JTAG_TMS   | I-12ma        | VTR | VTR             | Note9          |
| 107                 | Default | JTAG_RST#  | I-8ma         | VTR | VTR             | Note8<br>Note9 |
| 107                 | Alt 1   |            |               |     |                 |                |
| 107                 | Alt 2   |            |               |     |                 |                |
| 107                 | Alt 3   |            |               |     |                 |                |
| 108                 | Default | GPIO151    | (I/O/OD)-8ma  | VTR | VTR             |                |
| 108                 | Alt 1   | GPTP-IN4   | I-8ma         | VTR | VTR             |                |
| 108                 | Alt 2   |            |               |     |                 |                |
| 108                 | Alt 3   |            |               |     |                 |                |
| 109                 | Default | GPIO152    | (I/O/OD)-8ma  | VTR | VTR             |                |
| 109                 | Alt 1   | GPTP-OUT4  | (O/OD)-8ma    | VTR | VTR             |                |
| 109                 | Alt 2   |            |               |     |                 |                |
| 109                 | Alt 3   |            |               |     |                 |                |
| 110                 | Default | GPIO153    | (I/O/OD)-16ma | VTR | VTR             |                |
| 110                 | Alt 1   | LED3       | (O/OD)-16ma   | VTR | VTR             |                |
| 110                 | Alt 2   |            |               |     |                 |                |
| 110                 | Alt 3   |            |               |     |                 |                |
| 111                 | Default | GPIO154    | (I/O/OD)-12ma | VTR | VTR             |                |
| 111                 | Alt 1   | I2C1C_DATA | (I/OD)-12ma   | VTR | VTR             |                |
| 111                 | Alt 2   | PS2_CLK1B  | (I/OD)-12ma   | VTR | VTR             | Note11         |
| 111                 | Alt 3   |            |               |     |                 |                |
| 112                 | Default | GPIO155    | (I/O/OD)-12ma | VTR | VTR             |                |
| 112                 | Alt 1   | I2C1C_CLK  | (I/OD)-12ma   | VTR | VTR             |                |
| 112                 | Alt 2   | PS2_DAT1B  | (I/OD)-12ma   | VTR | VTR             | Note11         |
| 112                 | Alt 3   |            |               |     |                 |                |



Table 3.28 Multiplexing Table (15 of 16)

| 128 pins<br>MEC5035 | MUX     | Signal    | Buffer Type   | PWR  | emulated<br>pwr | Notes |
|---------------------|---------|-----------|---------------|------|-----------------|-------|
| 113                 | Default | VSS[5]    | PWR           | PWR  | PWR             |       |
| 113                 | Alt 1   |           |               |      |                 |       |
| 113                 | Alt 2   |           |               |      |                 |       |
| 113                 | Alt 3   |           |               |      |                 |       |
| 114                 | Default | GPIO156   | (I/O/OD)-16ma | VTR  | VTR             |       |
| 114                 | Alt 1   | LED1      | (IO/IOD)-16ma | VTR  | VTR             |       |
| 114                 | Alt 2   |           |               |      |                 |       |
| 114                 | Alt 3   |           |               |      |                 |       |
| 115                 | Default | GPIO157   | (I/O/OD)-16ma | VTR  | VTR             |       |
| 115                 | Alt 1   | LED2      | (O/OD)-16ma   | VTR  | VTR             |       |
| 115                 | Alt 2   |           |               |      |                 |       |
| 115                 | Alt 3   |           |               |      |                 |       |
| 116                 | Default | VTR[5]    | PWR           | PWR  | PWR             |       |
| 116                 | Alt 1   |           |               |      |                 |       |
| 116                 | Alt 2   |           |               |      |                 |       |
| 116                 | Alt 3   |           |               |      |                 |       |
| 117                 | Default | GPIO160   | (I/O/OD)-8ma  | VTR  | VTR             |       |
| 117                 | Alt 1   | 32KHZ_OUT | O-8ma         | VTR  | VTR             |       |
| 117                 | Alt 2   |           |               |      |                 |       |
| 117                 | Alt 3   |           |               |      |                 |       |
| 118                 | Default | BGPO0     | O-8ma         | VBAT | VBAT            |       |
| 118                 | Alt 1   |           |               |      |                 |       |
| 118                 | Alt 2   |           |               |      |                 |       |
| 118                 | Alt 3   |           |               |      |                 |       |
| 119                 | Default | VCI_IN2#  | I             | VBAT | VBAT            | Note5 |
| 119                 | Alt 1   |           |               |      |                 |       |
| 119                 | Alt 2   |           |               |      |                 |       |
| 119                 | Alt 3   |           |               |      |                 |       |
| 120                 | Default | VCI_OUT   | O-8ma         | VBAT | VBAT            |       |
| 120                 | Alt 1   |           |               |      |                 |       |
| 120                 | Alt 2   |           |               |      |                 |       |
| 120                 | Alt 3   |           |               |      |                 |       |

Table 3.29 Multiplexing Table (16 of 16)

| 128 pins<br>MEC5035 | MUX     | Signal      | Buffer Type | PWR  | emulated<br>pwr | Notes |
|---------------------|---------|-------------|-------------|------|-----------------|-------|
| 121                 | Default | VBAT        | PWR         | PWR  | PWR             |       |
| 121                 | Alt 1   |             |             |      |                 |       |
| 121                 | Alt 2   |             |             |      |                 |       |
| 121                 | Alt 3   |             |             |      |                 |       |
| 122                 | Default | XTAL1       | ICLK        | VBAT | VBAT            |       |
| 122                 | Alt 1   |             |             |      |                 |       |
| 122                 | Alt 2   |             |             |      |                 |       |
| 122                 | Alt 3   |             |             |      |                 |       |
| 123                 | Default | nFWP        | I           | VBAT | VTR             |       |
| 123                 | Alt 1   |             |             |      |                 |       |
| 123                 | Alt 2   |             |             |      |                 |       |
| 123                 | Alt 3   |             |             |      |                 |       |
| 124                 | Default | XTAL2       | OCLK        | VBAT | VBAT            |       |
| 124                 | Alt 1   |             |             |      |                 |       |
| 124                 | Alt 2   |             |             |      |                 |       |
| 124                 | Alt 3   |             |             |      |                 |       |
| 125                 | Default | AGND        | PWR         | PWR  | PWR             |       |
| 125                 | Alt 1   |             |             |      |                 |       |
| 125                 | Alt 2   |             |             |      |                 |       |
| 125                 | Alt 3   |             |             |      |                 |       |
| 126                 | Default | VCI_IN1#    | I           | VBAT | VBAT            | Note5 |
| 126                 | Alt 1   |             |             |      |                 |       |
| 126                 | Alt 2   |             |             |      |                 |       |
| 126                 | Alt 3   |             |             |      |                 |       |
| 127                 | Default | VCI_IN0#    | I           | VBAT | VBAT            | Note5 |
| 127                 | Alt 1   |             |             |      |                 |       |
| 127                 | Alt 2   |             |             |      |                 |       |
| 127                 | Alt 3   |             |             |      |                 |       |
| 128                 | Default | VCI_OVRD_IN | I           | VBAT | VBAT            | Note5 |
| 128                 | Alt 1   |             |             |      |                 |       |
| 128                 | Alt 2   |             |             |      |                 |       |
| 128                 | Alt 3   |             |             |      |                 |       |

## 3.6 Notes from tables in this chapter

|              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Note1</b> | The nEC_SCI Signal Pin Function can be controlled by hardware and ARC software. The nEC_SCI Signal Pin Function can drive either the ACPI Run-time GPE Chipset input or the Wake GPE Chipset input. Depending how the nEC_SCI Signal Pin Function is used, other ACPI-related SCI functions may be best supplied by other general purpose outputs that can be configured as open-drain drivers.                                                                                                        |
| <b>Note2</b> | These pins require an external weak pull-up resistors of 10k-100k ohms.                                                                                                                                                                                                                                                                                                                                                                                                                                |
| <b>Note3</b> | A pull-up is not needed on this BC-Link DATA pin as long as the voltage remains above the logic-high threshold during the second turnaround cycle.                                                                                                                                                                                                                                                                                                                                                     |
| <b>Note4</b> | This pin may require a weak pull-up.                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| <b>Note5</b> | This pin has EC wakeup and interrupt capability controlled by the corresponding Pin Control Register. A GPIO assignment is documented in the GPIO chapter to provide interrupt and wakeup capability. The GPIO assignment is not documented in the Pinout and Pin Description Chapter because it should not be used for I/O. See Detailed Pin Muxing Assignments section in the GPIO chapter and lookup this pin and see the associated note.                                                          |
| <b>Note6</b> | The two pin debug port UART can be used as a Host or EC. This pin can be VCC protected or not VCC portected under program control by the POWER bit in the Configuration Select Register in Host configuration space (also accessible by the EC).                                                                                                                                                                                                                                                       |
| <b>Note7</b> | This pin has no internal pullup or pulldown capability. The PU/PD Enable Bits in the associated Pin Control Registser has no effect. This pin has no input hysteresis; therefore, signals with slow rise and fall times (usecs) will retrigger interrupts.                                                                                                                                                                                                                                             |
| <b>Note8</b> | The JTAG_RST# pin needs to be asserted during VTR power-up. For example, an external 0.1 $\mu$ F Capacitor to ground and a 10K resistor to VTR can meet this requirement. The RC values are system dependent: care should be taken by the system board designer to insure that during VTR power up that JTAG_RST# is asserted for a longer time then the VTR rise time due to system capacitive loading. See Reset Section in the JTAG Chapter for more detailed decription of JTAG_RST# requirements. |



## Product Customer Specification-ODM

|               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Note9</b>  | When the JTAG_RST# pin is deasserted (logic'1'), the JTAG_TDI, JTAG_TDO, JTAG_CLK, JTAG_TMS signal functions in the JTAG interface are unconditionally routed to the JTAG signal functions; the Pin Control register for these pins has no effect. When the JTAG_RST# pin is asserted (logic'0'), the JTAG_TDI, JTAG_TDO, JTAG_CLK, JTAG_TMS signal functions in the JTAG interface are not routed to the interface and the Pin Control Register for these pins controls the muxing. The pin control registers can not route the JTAG interface to the pins. System Board Designer should terminate this pin in all functional state using jumpers and pull-up or pull down resistors, etc . |
| <b>Note10</b> | All VBAT powered pins with GPIO's on then have only one direction selected by the default signal function. The associated GPIO input register, output register bits are not connected to the pin. Only the Interrupt Detection field in the associated pin control register function is functional; the remainder of the bits in the pin control register has no effect.                                                                                                                                                                                                                                                                                                                     |
| <b>Note11</b> | PS/2 ports ending with signal functions ending with "A" or "B" are muxed to a single controller. Only one set of clock and data are intended to used at a time (either "A" or "B") not both. The unused port segment should have its associated pin control register's, Mux Control Field programmed away from the PS2 controller.                                                                                                                                                                                                                                                                                                                                                           |
| <b>Note12</b> | Most GPIO's are (I/O/OD). See Multiplexing tables below and associated notes for specific exceptions.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| <b>Note13</b> | GPIO assignments on this pin is present only to provide interrupt and wakeup capability. This is provided by the Interrupt Detection field in the Pin Control register. The Mux control field in the Pin Control Register should <b>not</b> be set to '00' = GPIO or undesirable results may occur.                                                                                                                                                                                                                                                                                                                                                                                          |



This section addresses general pin signal issues that typical need to be addressed at the system and board level.

The Power State and Power State Transitions in this table are defined in [Chapter 4, Power, Clocks and Resets](#). Behavior assumes no specific programming to change pin state. All GPIO's default pins have the same behavior described in [Table 3.30](#) as generically as GPIOXXX.

### Table 3.30 Pin Default State Through Power Transitions

[illegible]

**Note 3.2** See "VCC" power domain emulation and "VTR" power domain emulation on page 48



Table 3.32 Non 5 Volt Tolerant Signal Buffers

|    | MEC5035 pin | Non 5 Volt Tolerant Signal |
|----|-------------|----------------------------|
| 1  | 1           | VCI_IN3#                   |
| 2  | 55          | LDRQ#                      |
| 3  | 56          | SER_IRQ                    |
| 4  | 57          | LRESET#                    |
| 5  | 58          | PCI_CLK                    |
| 6  | 59          | LFRAME#                    |
| 7  | 60          | LAD0                       |
| 8  | 61          | LAD1                       |
| 9  | 62          | LAD2                       |
| 10 | 63          | LAD3                       |
| 11 | 64          | CLKRUN#                    |
| 12 | 66          | GPIO100/nEC_SCI            |
| 14 | 117         | GPIO160/32KHZ_OUT          |
| 15 | 118         | BGPO0                      |
| 16 | 119         | VCI_IN2#                   |
| 17 | 120         | VCI_OUT                    |
| 18 | 122         | XTAL1                      |
| 19 | 123         | nFWP                       |
| 20 | 124         | XTAL2                      |
| 21 | 126         | VCI_IN1#                   |
| 22 | 127         | VCI_IN0#                   |
| 23 | 128         | VCI_OVRD_IN                |
|    |             |                            |

**Table 3.33 POR Output Glitch Protection**

|   | <b>MEC5035<br/>pin</b> | <b>POR Glitch Protection</b> |
|---|------------------------|------------------------------|
| 1 | 72                     | <b>GPIO106/nRESET_OUT</b>    |
| 2 | 91                     | <b>GPIO126</b>               |
| 3 | 94                     | <b>GPIO131/I2C2A_CLK</b>     |
| 4 | 118                    | <b>BGPO0</b>                 |
| 5 | 120                    | <b>VCI_OUT</b>               |



### 3.8 Package Outline

The geometry same as 71.05035.00G  
9/26 confirm Joseph CC Hsu #6560

## Dimension

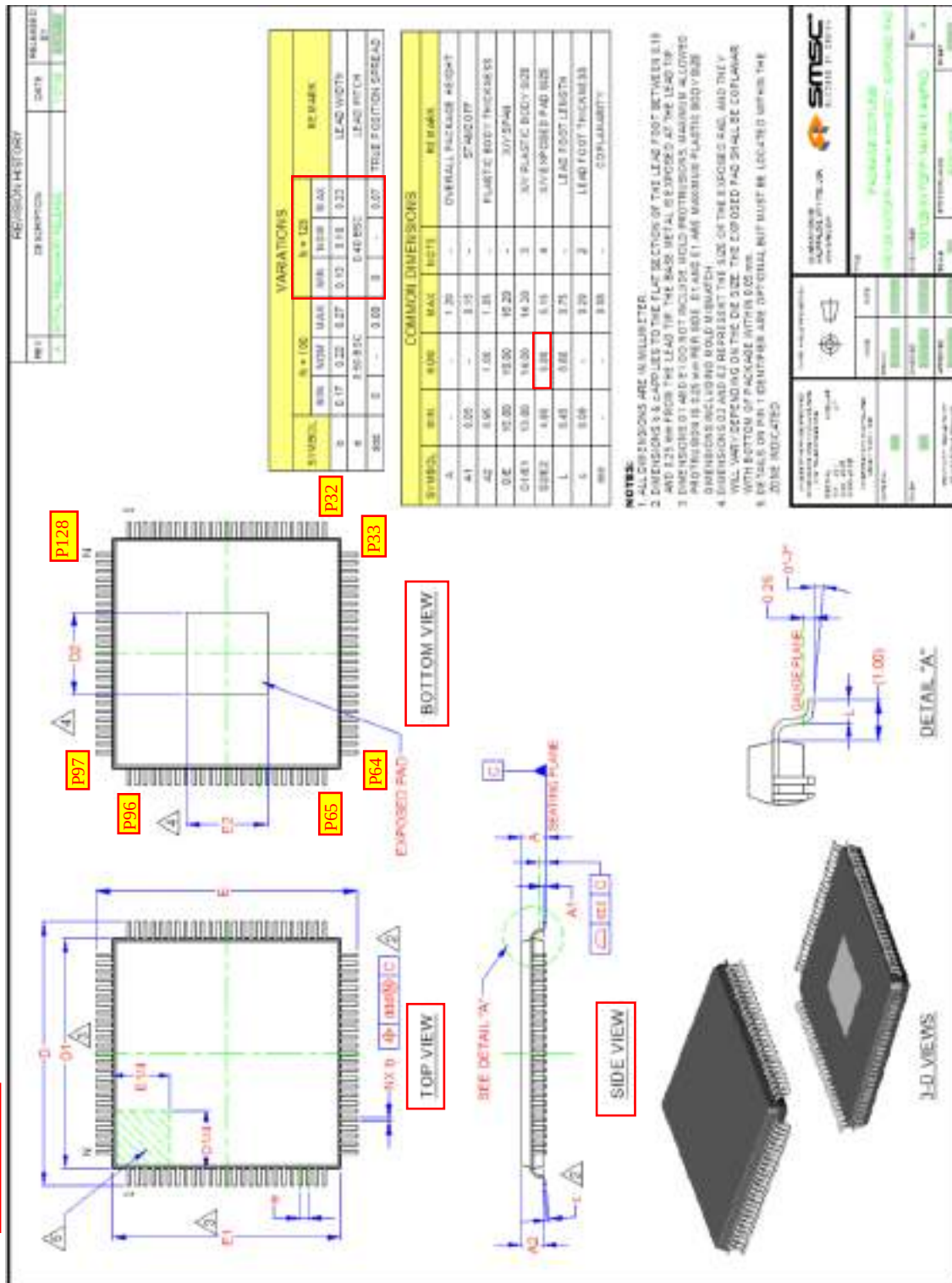


**Figure 3.3 128 Pin XVTQFP 14x14x1.4 mm Body with exposed pad**



### 3.9 Pinout and Pin Description Revision History

This revision history shows the changes made to this chapter.

**Table 3.34 Pinout and Pin Description Chapter Revision History**

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History," on page 539. |              |            |                                                                                                                                                                                                                                                                                                            |                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| #                                                                                                                                                                                                                           | REV# IN SPEC | DATE       | SECTION/FIGURE/ENTRY                                                                                                                                                                                                                                                                                       | CORRECTION                                                                                                                                                                                                                                                                                                                                                                                                        |
| 1.                                                                                                                                                                                                                          | 0.4          | 04/17/2007 | <p>Table 3.20 on page 54</p> <p>Section 3.5, "Pin Signal Function Multiplexing," on page 47</p> <p>Section 3.7.1, "Pin Default State Through Power Transitions," on page 66</p> <p>Section 3.6, "Notes from tables in this chapter," on page 64</p>                                                        | <p>Added note12 to pin 49 , VCC_PWRGD signal</p> <p>Added excel notes to Section 3.6, "Notes from tables in this chapter," on page 64.</p> <p>Corrected emulated pwr pin 21, 93 &amp; 94, buffer type pin 105 &amp; 106 and buffer type pin 105 &amp; 106. Corrected excel formula error: replaced "0" with "reserved" pin 34, 58, 59.</p> <p>Added section.</p> <p>Added Note13 about UART VTR/VCC function.</p> |
| 2.                                                                                                                                                                                                                          | 0.4          | 05/03/2007 | <p>"VCC" power domain emulation on page 47</p> <p>"VTR" power domain emulation on page 48</p> <p>Section 3.7, "General System/Layout pin Issues," on page 66</p>                                                                                                                                           | <p>Added New General System/Layout pin Issues section. Consolidated POR Glitch table, 5 Volt tolerant, Default Pin State Through Power Transitions, and Pin Notes.</p> <p>Added Alternate Function Pin State Through Power Transitions and described emulated buffers. Removed notes captured by new/reorganized section: Note[1,2,5,8,11].</p>                                                                   |
| 3.                                                                                                                                                                                                                          | 0.5          | 05/17/2007 | <p>Table 3.2, "Pin Configuration," on page 39</p> <p>Figure 3.1 128 XVTQFP Package Configuration on page 40</p>                                                                                                                                                                                            | <p>Remove "Warning: This figure is for pin count calculation only and is not final. Do not use for layout.</p>                                                                                                                                                                                                                                                                                                    |
| 4.                                                                                                                                                                                                                          | 0.5          | 05/23/2007 | <p>Table 3.32, "Non 5 Volt Tolerant Signal Buffers," on page 68</p>                                                                                                                                                                                                                                        | <p>Pin 73 GPIO107 removed from list.</p>                                                                                                                                                                                                                                                                                                                                                                          |
| 5.                                                                                                                                                                                                                          | 0.6          | 07/09/2007 | <p>Section 3.5, "Pin Signal Function Multiplexing," on page 47 &amp; Section 3.6, "Notes from tables in this chapter," on page 64</p> <p>Table 3.1, "Dell Mother Signal/SMSC Signal Naming Convention non-concordance," on page 38</p> <p>Section 3.6, "Notes from tables in this chapter," on page 64</p> | <p>Added note 7 to indicate the PCI buffers do not have internal pullup/pulldown resistors. Effects pins 55-59 &amp; 64.</p> <p>GPIO octal numbering corrected pin 111 &amp; above in Table 3.1. to make consistent with the remainder of the document.</p> <p>Added Note8 about adding RC ckt to JTAG_RST#.</p>                                                                                                  |

**Table 3.34 Pinout and Pin Description Chapter Revision History**

"REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See [Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History," on page 539.](#)

| #  | REV# IN SPEC | DATE       | SECTION/FIGURE/ENTRY                                                                                                                           | CORRECTION                                                                                                                                                                 |
|----|--------------|------------|------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6. | 0.61         | 08/29/2007 | <a href="#">Section 3.5, "Pin Signal Function Multiplexing," on page 47 &amp; Section 3.6, "Notes from tables in this chapter," on page 64</a> | Updated pin note 7 to indicate the PCI buffers have no internal Hysteresis and can retrigger interrupts. Effects pins 55-59 & 64.                                          |
| 7. | 0.61         | 8/31/2007  | <a href="#">Table 3.12, "SMBus Interface," on page 45</a><br><a href="#">Section 3.5, "Pin Signal Function Multiplexing," on page 47</a>       | Added visabilty of SMBus ports 2B, 2C & 2D Functional Singnals<br>I2C2B_CLK, I2C2B_DATA, I2C2C_CLK,<br>I2C2C_DATA, I2C2D_CLK, I2C2D_DATA on pins 98, 97, 106, 105, 13, 12. |



## Chapter 4 Power, Clocks and Resets

### 4.1 General Description

The [Power, Clocks and Resets](#) chapter includes descriptions of the MEC5035 [Clock Generator](#), [Power Configuration](#) and [Reset Interface](#). The [Clock Generator](#), in addition to describing clock sources, also features a [Generic Block Clocking Model](#), [Block Clocking and Reset Requirements Summary](#) and a [Power Management Interface](#). The [Reset Interface](#) description includes internal and external reset sources, as well as descriptions of an internal [1.8V Regulator](#) and [Power Mux](#). Other descriptions in this chapter include [References](#), a [Port List](#), [Interrupt Interface](#) and a [Registers Interface](#).

The Power Configuration, Clock Generator and Reset circuits have the following features:

#### 4.1.1 Power Configuration

- Description of [Power Supplies and Clocks ACPI Context](#).
- Enumerated [Power Supply Configurations](#).
- [Power-Up Sequence](#) Definition.
- [1.8V Regulator](#).
- [Power Mux](#).

#### 4.1.2 Clock Generator

- Three Asynchronous Clock Sources: [64.52 MHz Ring Oscillator](#), [32.768 KHz Crystal Oscillator](#) and [PCI\\_CLK](#).
- Efficient Logic Design to Minimize Power Consumption.
- Independent EC-driven [Power Management Interface](#).
- [64.52 MHz Ring Oscillator](#) Optimized for 115.2K baud 16C550A UART Support.
- [Generic Block Clocking Model](#).
- EC-accessible [Registers Interface](#).

#### 4.1.3 Reset Interface

- [VTR](#) and [VBAT](#) Reset Signaling ([VTRGD](#), [VBAT\\_POR](#), [nSYS\\_RST](#), [nEC\\_RST](#)).
- [VCC](#) Reset Signaling ([VCC Power Good](#)).
- [Watch-Dog Timer Forced Reset](#).
- [Interrupt Interface](#).
- [Strapping Options](#).

### 4.2 References

1. Advanced Configuration and Power Interface Specification, Revision 1.0b, February 2, 1999.
2. Intel® 82801DBM I/O Controller Hub 4 Mobile (ICH4-M), Datasheet, Order Number: 252337-001, Intel Corp., January 2003.
3. PCI Mobile Design Guide, Version 1.1, PCI-SIG, December 18, 1998.

### 4.3 Port List

The [Port List](#) shown in [Table 4.1](#) is preliminary and subject to change.



Table 4.1 Power, Clocks and Resets Port List

| SIGNAL NAME                   | DIRECTION    | SOURCE                                             | DESTINATION                                                                                                         | DESCRIPTION                                                                                                                                                                                                                                                                                                          |
|-------------------------------|--------------|----------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ARC_CLK_DISABLE               | Input        | External - Embedded Controller Core (EC)           | Internal - <a href="#">EC Power State Controls</a>                                                                  | Indication for the <a href="#">Power Management Interface</a> (see <a href="#">Section 4.4.7 on page 84</a> ) that an EC Sleep instruction has occurred and the processor is sleeping or halted.                                                                                                                     |
| SLEEP_STATE                   | Output       | Internal - <a href="#">EC Power State Controls</a> | Internal - <a href="#">64.52 MHz Ring Oscillator Control</a> and External Functions as Needed.                      | System Sleeping State status indicator as described in <a href="#">Section 4.4.7.4.2, "EC Power State Controls," on page 88</a> .                                                                                                                                                                                    |
| SLEEP_FLAG                    | Output       | <a href="#">Clock Control Register</a>             | Internal - <a href="#">64.52 MHz Ring Oscillator Control, Block Sleep Enables</a> and External Functions as Needed. | Sleep indicator from the <a href="#">Clock Control Register</a> . See also <a href="#">Section 4.4.7.4.2, "EC Power State Controls," on page 88</a> and <a href="#">Section 4.4.7.4.4, "Block Sleep Enables," on page 91</a> .                                                                                       |
| PCI_CLK                       | Input        | External                                           | Internal Test Functions                                                                                             | 33 MHz PCI Clock Input (also TEST_CLK_IN).                                                                                                                                                                                                                                                                           |
| LRESET#                       | Input        | External                                           | Internal                                                                                                            | PCI Reset. See <a href="#">Section 4.6.9, "LPC RESET," on page 102</a> .                                                                                                                                                                                                                                             |
| XTAL1                         | Input        | External                                           | Internal - <a href="#">32.768 KHz Crystal Oscillator</a>                                                            | <a href="#">32.768 KHz Crystal Oscillator</a> crystal input pin.                                                                                                                                                                                                                                                     |
| XTAL2                         | Output/Input | External                                           | Internal - <a href="#">32.768 KHz Crystal Oscillator</a>                                                            | <a href="#">32.768 KHz Crystal Oscillator</a> crystal output/single-ended clock source input pin (see <a href="#">XOSEL</a> ).                                                                                                                                                                                       |
| WAKE                          | Input        | External                                           | Internal - <a href="#">Wake Interface</a>                                                                           | Aggregated Wake indicator from the <a href="#">EC Interrupt Aggregator on page 304</a> for the <a href="#">Power Management Interface</a> (see <a href="#">Section 4.4.7 on page 84</a> ). The EC can determine the state of the WAKE signal using WAKE bit in the <a href="#">PCR Status and Control Register</a> , |
| WDT_ALRT                      | Input        | External                                           | Internal - <a href="#">Reset Interface</a>                                                                          | Causes a <a href="#">Watch-Dog Timer Forced Reset</a> as described in <a href="#">Section 4.6.10 on page 103</a> .                                                                                                                                                                                                   |
| XOSEL                         | Output       | Internal                                           | Internal - <a href="#">32.768 KHz Crystal Oscillator</a> and other functions as needed.                             | <a href="#">Clock Enable Register</a> bit D0, used to select a single-ended external input for the <a href="#">32.768 KHz Crystal Oscillator</a> ( <a href="#">Section , "XOSEL," on page 117</a> ).                                                                                                                 |
| ALL_BLOCK_SLEEPENABLE_OUTPUTS | Output       | Internal - <a href="#">Block Sleep Enables</a>     | External - Sleep-able Blocks                                                                                        | To all blocks as defined in <a href="#">Section 4.7.5, "Block Sleep Enable Registers," on page 110</a> . See also <a href="#">Section 4.4.7.4.4, "Block Sleep Enables," on page 91</a>                                                                                                                               |

**Table 4.1 Power, Clocks and Resets Port List (continued)**

| SIGNAL NAME                                                                                                                                                                                                                 | DIRECTION  | SOURCE                                                                             | DESTINATION                                                                  | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                        |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|------------------------------------------------------------------------------------|------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MCLK,<br>EC_BUS_CLK_EN,<br>LPC_BUS_CLK_EN,<br>MCLK_DIV2_EN,<br>MCLK_DIV4_EN,<br>MCLK_DIV8_EN,<br>MCLK_DIV16_EN,<br>MCLK_DIV32_EN,<br>MCLK_DIV64_EN,<br>MCLK_DIV128_EN,<br>MCLK_DIV640_EN,<br>MCLK_DIV64_EN_HST,<br>X32K_CLK | Output     | Internal -<br>Ring<br>Oscillator<br>Sourced<br>Clocking and<br>32K Clock<br>Domain | External                                                                     | See <a href="#">Section 4.4.8, "Ring Oscillator Sourced Clocking,"</a> on page 93 and <a href="#">Section 4.4.9, "32K Clock Domain,"</a> on page 95.                                                                                                                                                                                                                                               |
| 32KHZ_OUT                                                                                                                                                                                                                   | Output     | Internal                                                                           | External                                                                     | Off-Chip 32.768KHz Oscillator Output (see <a href="#">Section , "32KHz OUTPUT,"</a> on page 105).                                                                                                                                                                                                                                                                                                  |
| ALL BLOCK<br>"CLOCK<br>REQUIRED"<br>STATUS BITS                                                                                                                                                                             | Input      | External -<br>Sleep-able<br>Blocks                                                 | Internal - <a href="#">64.52<br/>MHz Ring<br/>Oscillator<br/>Control</a>     | see <a href="#">Section 4.7.6, "Clock Required Status Registers,"</a> on page 112.                                                                                                                                                                                                                                                                                                                 |
| nSIO_RESET                                                                                                                                                                                                                  | Output     | Internal                                                                           | Internal/<br>External                                                        | EC-driven SIO Reset and External System Reset (nRESET_OUT-See <a href="#">Table 3.9, "MISC Interface,"</a> on page 44). (see <a href="#">Section , "iRESET OUT,"</a> on page 109).                                                                                                                                                                                                                 |
| VCC_PWRGD                                                                                                                                                                                                                   | Input      | External                                                                           | Internal - <a href="#">Host<br/>Clock Domain</a>                             | VCC Power Good Input. See <a href="#">Section 4.4.8.4, "Host Clock Domain,"</a> on page 94 and <a href="#">Section 4.6.8, "VCC Power Good,"</a> on page 102. The EC can determine the state of the <a href="#">VCC_PWRGD</a> signal using <a href="#">VCC_PWRGD</a> bit in the <a href="#">PCR Status and Control Register</a> . See also <a href="#">Section 4.6.9, "LPC RESET,"</a> on page 102. |
| VCC_PWRGD_<br>BUFF                                                                                                                                                                                                          | Output     | Internal                                                                           | External - Pad<br>Buffers                                                    | Buffered <a href="#">VCC_PWRGD</a> output used to tri-state VCC-related Pads.                                                                                                                                                                                                                                                                                                                      |
| PCR_INT                                                                                                                                                                                                                     | Output     | Internal                                                                           | External ( <a href="#">EC<br/>Interrupt<br/>Aggregator on<br/>page 304</a> ) | see <a href="#">Section 4.9, "Interrupt Interface,"</a> on page 117.                                                                                                                                                                                                                                                                                                                               |
| FLASH_PGM                                                                                                                                                                                                                   | Input      | External                                                                           | Internal -<br><a href="#">Power-Fail and<br/>Reset Status<br/>Register</a>   | see <a href="#">Section , "FLASH,"</a> on page 116.                                                                                                                                                                                                                                                                                                                                                |
| LPC_RST#                                                                                                                                                                                                                    | Output     | Internal                                                                           | External (LPC<br>Interface)                                                  | see <a href="#">Section 4.6.9, "LPC RESET,"</a> on page 102.                                                                                                                                                                                                                                                                                                                                       |
| VTR                                                                                                                                                                                                                         | Power Well | External                                                                           | –                                                                            | Suspend Supply                                                                                                                                                                                                                                                                                                                                                                                     |
| VBAT                                                                                                                                                                                                                        | Power Well | External                                                                           | –                                                                            | Battery Supply                                                                                                                                                                                                                                                                                                                                                                                     |
| VSS                                                                                                                                                                                                                         | Power Well | External                                                                           | –                                                                            | Digital Ground                                                                                                                                                                                                                                                                                                                                                                                     |
| AGND                                                                                                                                                                                                                        | Power Well | External                                                                           | –                                                                            | Analog Ground for the <a href="#">32.768 KHz<br/>Crystal Oscillator</a> .                                                                                                                                                                                                                                                                                                                          |
| VTR_1.8                                                                                                                                                                                                                     | Power Well | Internal                                                                           | –                                                                            | Output of the internal 1.8 V regulator (see <a href="#">Section 4.6.6, "1.8V Regulator,"</a> on page 101).                                                                                                                                                                                                                                                                                         |



Table 4.1 Power, Clocks and Resets Port List (continued)

| SIGNAL NAME | DIRECTION  | SOURCE   | DESTINATION           | DESCRIPTION                                                                                                                                                 |
|-------------|------------|----------|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VTR1.8_BAT  | Power Well | Internal | –                     | Output of the internal <a href="#">Power Mux</a> for VBAT-backed logic (see <a href="#">Section 4.6.7, "Power Mux,"</a> on page 101).                       |
| nSYS_RST    | Output     | Internal | Internal/<br>External | Synchronized VTR Power Good ( <a href="#">Section 4.6.4, "nSYS_RST,"</a> on page 101).                                                                      |
| nEC_RST     | Output     | Internal | Internal/<br>External | Stretched nSYS_RST used for EC reset and <a href="#">Strapping Options</a> (see <a href="#">Section 4.6, "Reset Interface,"</a> on page 99).                |
| VBAT_POR    | Output     | Internal | Internal/<br>External | VBAT Power On Reset ( <a href="#">Section 4.6.3, "VBAT_POR,"</a> on page 100)                                                                               |
| VR_CAP      | Power Well | Internal | –                     | Capacitor Connection for Internal Voltage Regulator (4.7μF ±20%, ESR 2 Ohms, max.) (see also <a href="#">Section 4.6.6, "1.8V Regulator,"</a> on page 101). |

## 4.4 Clock Generator

### 4.4.1 Overview

The MEC5035 [Clock Generator](#) includes three clock sources as illustrated in [Figure 4.1](#): the [64.52 MHz Ring Oscillator](#), [32.768 KHz Crystal Oscillator](#) and the PCI Clock ([PCI\\_CLK](#) in [Table 4.1](#)). The relationship of these clock sources to the system power supplies is described in [Section 4.4.2, "Power Supplies and Clocking,"](#) on page 78; their relationship to the ACPI power states is described in [Section 4.5.1, "Power Supplies and Clocks ACPI Context,"](#) on page 96.

[Ring Oscillator Sourced Clocking](#) includes [Programmable Clock Domains](#), a [Fixed Clock Domain](#) and a [Host Clock Domain](#). The output from the [32.768 KHz Crystal Oscillator](#) defines a [32K Clock Domain](#). A [Block Clocking and Reset Requirements Summary](#) is included in [Section 4.4.6](#) on page 82.

The [Clock Generator](#) also includes the definition of a [Generic Block Clocking Model](#) that provides the foundation for a [Power Management Interface](#). This interface defines several [EC Controlled Dynamic Power States](#) that can influence power consumption at the block level and within the [Clock Generator](#).

The [Clock Generator](#) includes an EC accessible [Registers Interface](#) and support for an ATE test mode to drive all system clocking from the [PCI\\_CLK](#) input.



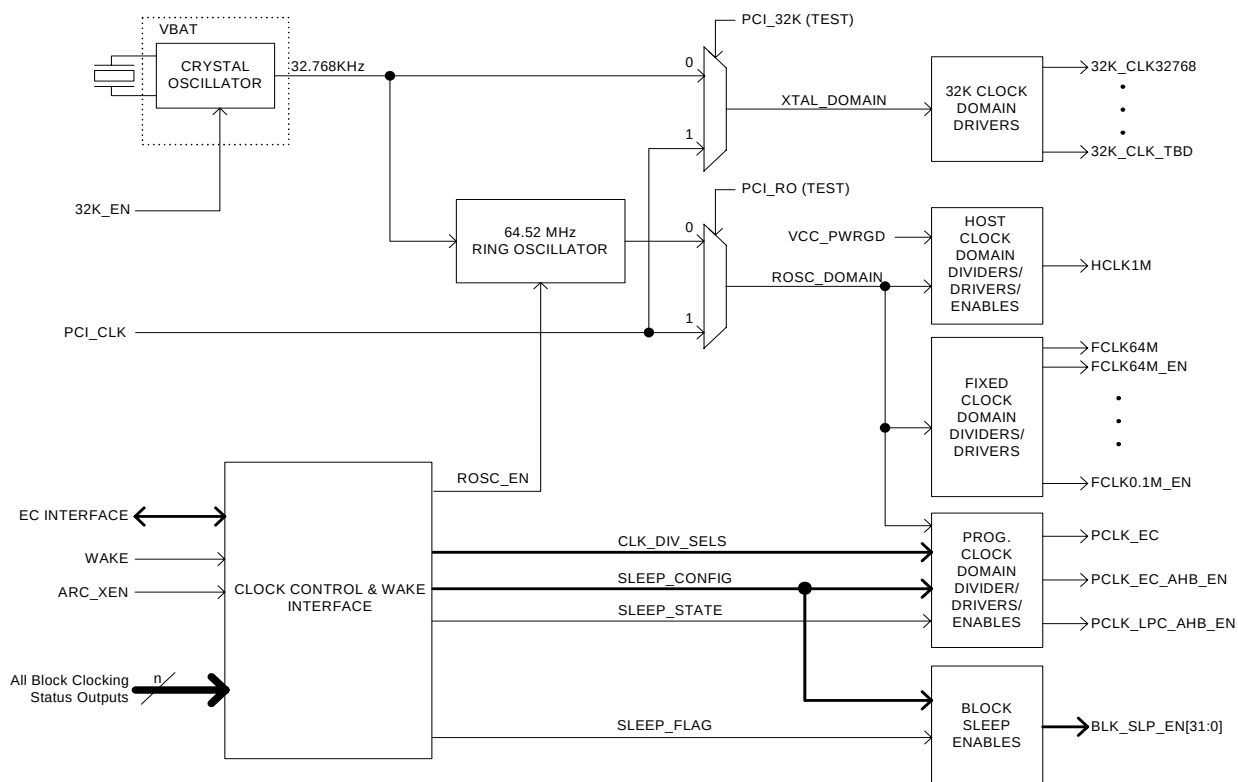


Figure 4.1 Clock Generator Block Diagram

## 4.4.2 Power Supplies and Clocking

Table 4.2 illustrates clocking capabilities versus power supply availability. For more information, see Section 4.5, "Power Configuration," on page 96.

Table 4.2 Clocks vs. Power Supplies

| POWER SUPPLY STATES (Note 4.1) |     |     | CLOCKS    |                      |                      |                      |
|--------------------------------|-----|-----|-----------|----------------------|----------------------|----------------------|
| VBAT                           | VTR | VCC | PCI CLOCK | 32K XTAL             | 32K EXTERNAL         | RING OSC.            |
| OFF                            | OFF | OFF | OFF       | OFF                  | OFF                  | OFF                  |
| ON                             | OFF | OFF |           | ON/OFF<br>(Note 4.2) | ON/OFF<br>(Note 4.4) | ON/OFF<br>(Note 4.3) |
| ON                             | ON  | OFF |           |                      |                      |                      |
| ON                             | ON  | ON  | ON/OFF    |                      |                      |                      |

**Note 4.1** power supply states not illustrated in Table 4.2 are undefined (see also Section 4.5, "Power Configuration," on page 96).

**Note 4.2** this is true only after the EC asserts the 32K\_EN bit in the Clock Enable Register.

**Note 4.3** there is accuracy adjustment latency as described in Section 4.4.3, "64.52 MHz Ring Oscillator," on page 79. The 64.52 MHz Ring Oscillator can be disabled using the Power Management Interface.



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**Note 4.4** an external single-ended 32.768Hz clock source may be [VTR](#) or [VBAT](#) powered. Note that higher than normal [VBAT](#) current may occur when [VTR](#) transitions from unpowered to powered if the switching threshold on the external single-ended 32.768Hz clock source is different than the internal [Power Mux](#) switch threshold.

### 4.4.3 64.52 MHz Ring Oscillator

The MEC5035 [Clock Generator](#) includes a high-accuracy, low power, low start-up latency [64.52 MHz Ring Oscillator](#). The [64.52 MHz Ring Oscillator](#) is always enabled except in the [SYSTEM DEEPEST SLEEP](#) state when the [64.52 MHz Ring Oscillator](#) is stopped by hardware as described in [Section 4.4.7, "Power Management Interface," on page 84](#). The [64.52 MHz Ring Oscillator](#) start-up time  $t_{ADJ}$  is shown in [Table 4.3](#).

Without correction or when the [32.768 KHz Crystal Oscillator](#) is not running, the accuracy of the [64.52 MHz Ring Oscillator](#) is  $\pm 50\%$  (min.). When the [64.52 MHz Ring Oscillator](#) is enabled and the [32.768 KHz Crystal Oscillator](#) is running, the accuracy of the [64.52 MHz Ring Oscillator](#) is automatically corrected by hardware from  $\pm 50\%$  to  $\pm 2\%$  using a free-running iterative algorithm (see a description of the [FREQ LOCK](#) bit in the [PCR Status and Control Register](#) and the [SAA](#) bit in the [Clock Control Register](#)). The  $t_{ADJ}$  time is shown in [Table 4.3](#).

The [64.52 MHz Ring Oscillator](#) is reset by [VTRGD](#) as described in [Section 4.6, "Reset Interface," on page 99](#).

**Table 4.3 64.52 MHz Ring Oscillator Timing Parameters**

| PARAMETERS                                                                      | SYMBOL    | MIN  | TYP | MAX                             | UNITS   |
|---------------------------------------------------------------------------------|-----------|------|-----|---------------------------------|---------|
| Adjustment Delay to $\pm 2\%$ Accuracy                                          | $t_{ADJ}$ | 0.03 | -   | TBD( <a href="#">Note 4.5</a> ) | ms      |
| <a href="#">64.52 MHz Ring Oscillator</a> Start-up Delay ( $\pm 50\%$ accuracy) | $t_{SU}$  |      |     | 6                               | $\mu s$ |

**Note 4.5** when the [32.768 KHz Crystal Oscillator](#) is configured for use with a crystal (i.e., [XOSEL](#) is '0'), the [32.768 KHz Crystal Oscillator](#) start-up time must be added to the  $t_{ADJ}$  time in [Table 4.3](#) when the [32K\\_EN](#) is asserted (see [32K\\_EN](#) description in [Section , "32K\\_EN," on page 117](#)).

### 4.4.4 32.768 KHz Crystal Oscillator

The [32.768 KHz Crystal Oscillator](#) provides a stable timebase for the [64.52 MHz Ring Oscillator](#) and a clock source for the [32K Clock Domain](#). The [XOSEL](#) bit configures the [32.768 KHz Crystal Oscillator](#) to use either a single-ended 32.768 KHz clock input or a 32.768 KHz crystal as described in [Section , "XOSEL," on page 117](#).

The [32.768 KHz Crystal Oscillator](#) is controlled by the [32K\\_EN](#) bit in the [Clock Enable Register](#) (see [Section 4.8.2, "Clock Enable Register," on page 117](#)). When [XOSEL](#) is not asserted and [32K\\_EN](#) is asserted, there is a start-up delay ( $t_{SU}$ ) for the [32.768 KHz Crystal Oscillator](#) as shown in [Table 4.4](#).

The clocks sourced by the [32.768 KHz Crystal Oscillator](#) in the [32K Clock Domain](#) operate as described in [Table 4.15, "Typical MEC5035 Clocks vs. ACPI Power States"](#) (see [Section 4.5.1, "Power Supplies and Clocks ACPI Context," on page 96](#).

**Table 4.4 32.768 KHz Crystal Oscillator Timing Parameters**

| PARAMETERS                                                   | SYMBOL   | MIN | TYP | MAX | UNITS |
|--------------------------------------------------------------|----------|-----|-----|-----|-------|
| <a href="#">32.768 KHz Crystal Oscillator</a> Start-up Delay | $t_{SU}$ |     |     | 5   | sec.  |

Table 4.4 32.768 KHz Crystal Oscillator Timing Parameters (continued)

| PARAMETERS                                                       | SYMBOL | MIN | TYP | MAX | UNITS |
|------------------------------------------------------------------|--------|-----|-----|-----|-------|
| 32.768 KHz Crystal Oscillator/Single-ended Clock Source Accuracy | Acc    | TBD | TBD | TBD | TBD   |

## 4.4.5 Generic Block Clocking Model

### 4.4.5.1 Overview

The [Generic Block Clocking Model](#) defines the block [Clock Gating](#) interface that is assumed by the [Clock Generator](#) for all of the MEC5035 internal blocks identified in the [Block Sleep Enable Registers](#). [Components](#) of this model are illustrated in [Figure 4.2](#) and described in [Section 4.4.5.2](#). The response of this model to the actions of the [Power Management Interface](#) is described in [Section 4.4.5.3, "Behavior," on page 81](#).

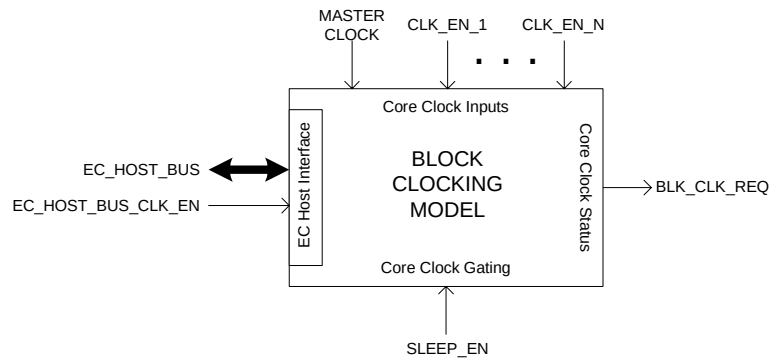


Figure 4.2 Generic Block Clocking Model Illustration

### 4.4.5.2 Components

As shown in [Figure 4.2](#) the external interface for the [Generic Block Clocking Model](#) includes an EC (or other available bus master) host interface, core clock Inputs (which may be clocks or clock enables), a logical core clock gating control and a core clock status output. Not shown in [Figure 4.2](#) is the internal interface for the [Generic Block Clocking Model](#) that includes a block enable bit and may also include a block idle status indicator. Each of the [Generic Block Clocking Model](#) internal and external interface elements and operational states are described in [Table 4.5](#).

When firmware de-asserts the internal block enable bit the block is disabled and in a minimum power consumption state. Depending on the implementation, the host may need to guarantee that the block is not in use before the internal enable bit is de-asserted because it may also function as a reset. Transitions to a minimum block power consumption state while the internal enable bit remains asserted may be requested by the [Power Management Interface](#) using an external sleep enable input (see also [Section 4.4.5.3, "Behavior," on page 81](#)). In both cases (i.e., when the block is disabled or sleeping), the core clock required status indicator output (BLK\_CLK\_REQ in [Figure 4.2](#)) is de-asserted.

When firmware asserts the internal block enable and the external sleep enable input is not asserted, or the external sleep enable input is asserted but the internal idle indicator is not asserted, the block is operational and in a maximum power consumption state. In both of these cases, the core clock required status indicator output is asserted.

Table 4.5 Generic Block Clocking Model Components

| INTERNAL<br>ENABLE<br>BIT<br>(Note 4.7) | EXTERNAL<br>SLEEP_EN<br>INPUT<br>(Note 4.8) | BLOCK<br>IDLE<br>STATUS | CORE<br>CLOCK<br>REQUIRED<br>STATUS<br>OUTPUT<br>(Note 4.6) | STATE                 | POWER   | DESCRIPTION                                                                                                                                                                                                                                                                                |
|-----------------------------------------|---------------------------------------------|-------------------------|-------------------------------------------------------------|-----------------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0                                       | X                                           | X                       | 0                                                           | DISABLED              | MINIMUM | Block is disabled by firmware and the core clock is not needed and gated 'off' internally. Note: it may be up to the host to guarantee that the block is not in use before the internal enable bit is asserted because the internal enable may also function as a reset when not asserted. |
| 1                                       | 0                                           | NOT IDLE                | 1                                                           | FULL<br>POWER         | MAXIMUM | The full power state identifies the block normal operation mode where the block is neither disabled by firmware nor commanded to sleep by the <a href="#">Power Management Interface</a> .                                                                                                 |
|                                         |                                             | IDLE                    |                                                             |                       |         |                                                                                                                                                                                                                                                                                            |
|                                         | 1                                           | NOT IDLE                | 0                                                           | PREPARING<br>TO SLEEP | MINIMUM | A sleep command has been asserted but the core clock is still required because the block is not idle.                                                                                                                                                                                      |
|                                         |                                             | IDLE                    |                                                             | SLEEPING              |         | A sleep command has been asserted, the block is idle and the core clocks are stopped.                                                                                                                                                                                                      |

**Note 4.6** the "Block Clock Required Status Output" (BLK\_CLK\_REQ in [Figure 4.2](#)) only reflects the core clock requirement; i.e. independent of the host interface clock enable (EC\_HOST\_BUS\_CLK\_EN in [Figure 4.2](#)). The MEC5035 [Generic Block Clocking Model](#) assumes that the block may not remain operational without the host interface clock enable which will not be stopped unless the [64.52 MHz Ring Oscillator](#) is disabled (see [Section 4.4.7, "Power Management Interface," on page 84](#)). The "Clock Required Status" for each block can be seen in the [Clock Required Status Registers](#).

**Note 4.7** the internal enable bit (not shown in [Figure 4.2](#)) is accessible through the EC Host Interface shown in [Figure 4.2](#) and provides a reset to each block. Typically, as soon as the internal enable bit is de-asserted, the block may be immediately reset and held in the lowest power consumption state.

**Note 4.8** The external sleep enables are configured using the [Block Sleep Enables](#) as described in [Section 4.4.7.4.4, "Block Sleep Enables," on page 91](#).

#### 4.4.5.3 Behavior

The affects of the [Power Management Interface](#) on the block sleep [Behavior](#) as a result of transitions on the sleep enable input are ignored when the block is disabled. Blocks are typically disabled following a power-on reset ([Figure 4.3](#)).

When a block is enabled, a sleep state request as a result of a transition on the sleep enable input must not adversely affect block operation; e.g., by performing illegal operations on an external circuit or corrupting transaction data. As a result, there may be transition latency from the running state to the sleeping state, depending on the nature of the block and its operational state as defined by an internal block 'idle' indicator when the sleep enable is asserted. It is possible that a block may never enter the sleeping state if the block does not idle before the sleep enable input is de-asserted as a result of a wake event.

Once a block enters the sleeping state, internal clocks are gated 'off' and the block is inactive; i.e., outputs are static and the block cannot respond to transitions on inputs, except as defined by the [Wake Interface](#). The transition from the sleeping state to the running state can only occur once the system clocks are running and the sleep enable input is de-asserted.

As described in [Section 4.4.5.2, "Components"](#), transitions from the running state or the preparing to sleep state to the disabled state may occur without latency depending on the implementation (not shown in [Figure 4.3](#)). Transitions from the sleeping state to the disabled state are undefined when the [64.52 MHz Ring Oscillator](#) is stopped. Transitions from the sleeping state to the disabled state can occur without latency when the [64.52 MHz Ring Oscillator](#) is running (also not shown in [Figure 4.3](#)).

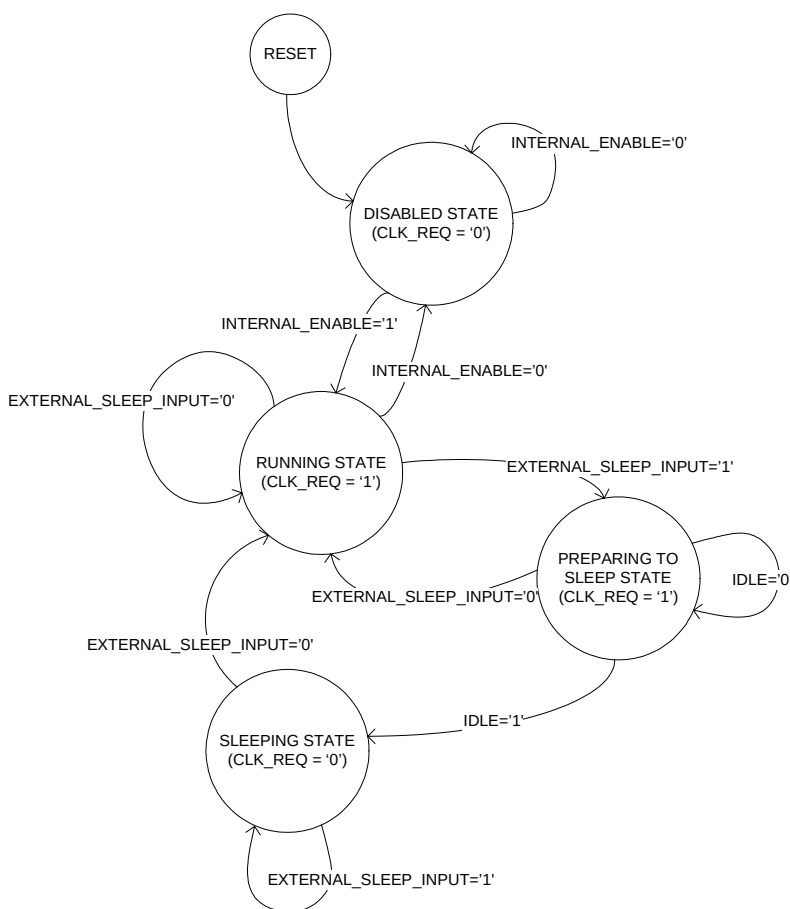


Figure 4.3 Generic Block Clocking Model Clock Gating State Diagram Example

## 4.4.6 Block Clocking and Reset Requirements Summary

The [Block Clocking and Reset Requirements Summary](#) shown in [Table 4.6](#) includes clocking requirements as defined by [Section 4.4.8, "Ring Oscillator Sourced Clocking,"](#) on page 93 and [Section 4.4.9, "32K Clock Domain,"](#) on page 95, relevant MEC5035 clock sources used, the required ACPI



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state support and the relationship of the block to the [Power Management Interface](#). [Table 4.6](#) also includes reset requirements as defined in [Section 4.6, "Reset Interface,"](#) on page 99.

The values shown in [Table 4.6](#) are preliminary and subject to change.

Table 4.6 Block Clocking and Reset Requirements Summary

| BLOCK NAME                     | CLOCKS                                                                                                                                                                                                                      | ACPI States  | CLOCK SOURCE                                                            | Dynamic Clock Gating? (Note 4.9) | RESETS                                                                                      | DESCRIPTION                                                                                                                                                                                                                              |
|--------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|-------------------------------------------------------------------------|----------------------------------|---------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LPC Interface                  | MCLK,<br>LPC_BUS_CLK_EN, PCI_CLK                                                                                                                                                                                            | S0-S1        | PCI_CLK,<br>64.52 MHz Ring Oscillator                                   | YES                              | nSYS_RST,<br>LPC RESET                                                                      | Independent Clock Domain; LPC Interface is gated by VCC_PWRGD to prevent back-drive.                                                                                                                                                     |
| EC CORE                        | MCLK,<br>EC_BUS_CLK_EN                                                                                                                                                                                                      | S0-S5        | 64.52 MHz Ring Oscillator                                               | NO                               | nEC_RST                                                                                     | The EC and its subordinate bridges are all driven by the System Clock. The System Clock is programmable as described in the <a href="#">EC Clock Divider Register</a> . NOTE: The EC should be able to sense VCC_PWRGD (Interrupt/wake). |
| EC_AHB                         | MCLK,<br>EC_BUS_CLK_EN                                                                                                                                                                                                      | S0-S5        | 64.52 MHz Ring Oscillator                                               | NO                               | nSYS_RST                                                                                    | These clock enables only stop when the 64.52 MHz Ring Oscillator is stopped.                                                                                                                                                             |
| LPC_AHB                        | MCLK,<br>LPC_BUS_CLK_EN                                                                                                                                                                                                     | S0-S5        | 64.52 MHz Ring Oscillator                                               | NO                               | nSYS_RST                                                                                    |                                                                                                                                                                                                                                          |
| 64.52 MHz Ring Oscillator      | —                                                                                                                                                                                                                           | S0-S5        | 32.768 KHz Crystal Oscillator                                           | YES                              | VTRGD                                                                                       | Clock source for Ring Oscillator Sourced Clocking.                                                                                                                                                                                       |
| 32.768 KHz Crystal Oscillator  | —                                                                                                                                                                                                                           | G0,<br>S0-S5 | —                                                                       | NO                               | VBAT_POR                                                                                    | Can use an external clock source.                                                                                                                                                                                                        |
| 64-Byte Memory Bank            | MCLK,<br>EC_BUS_CLK_EN                                                                                                                                                                                                      | G0,<br>S0-S5 | 64.52 MHz Ring Oscillator                                               | NO                               | nSYS_RST,<br>VBAT_POR                                                                       |                                                                                                                                                                                                                                          |
| VBAT-Powered Control Interface | MCLK,<br>EC_BUS_CLK_EN                                                                                                                                                                                                      |              | 64.52 MHz Ring Oscillator                                               | NO                               | nSYS_RST,<br>VBAT_POR                                                                       |                                                                                                                                                                                                                                          |
| PWM 1                          | MCLK,                                                                                                                                                                                                                       | S0-S5        | 64.52 MHz Ring Oscillator                                               | YES                              | nSYS_RST                                                                                    |                                                                                                                                                                                                                                          |
| PWM 2                          | MCLK_DIV640_EN,                                                                                                                                                                                                             |              |                                                                         |                                  |                                                                                             |                                                                                                                                                                                                                                          |
| PWM 3                          | EC_BUS_CLK_EN                                                                                                                                                                                                               |              |                                                                         |                                  |                                                                                             |                                                                                                                                                                                                                                          |
| PWM 4                          |                                                                                                                                                                                                                             |              |                                                                         |                                  |                                                                                             |                                                                                                                                                                                                                                          |
| Tachometer 1                   | MCLK,                                                                                                                                                                                                                       | S0-S5        | 64.52 MHz Ring Oscillator                                               | YES                              | nSYS_RST                                                                                    |                                                                                                                                                                                                                                          |
| Tachometer 2                   | MCLK_DIV640_EN,                                                                                                                                                                                                             |              |                                                                         |                                  |                                                                                             |                                                                                                                                                                                                                                          |
| Tachometer 3                   | EC_BUS_CLK_EN                                                                                                                                                                                                               |              |                                                                         |                                  |                                                                                             |                                                                                                                                                                                                                                          |
| SMBus 1                        | MCLK,                                                                                                                                                                                                                       | S0-S5        | 64.52 MHz Ring Oscillator                                               | YES                              | nSYS_RST                                                                                    |                                                                                                                                                                                                                                          |
| SMBus 2                        | MCLK_DIV8_EN,<br>EC_BUS_CLK_EN                                                                                                                                                                                              |              |                                                                         |                                  |                                                                                             |                                                                                                                                                                                                                                          |
| 16-Bit Counter/Timer 0         | MCLK,                                                                                                                                                                                                                       | S0-S5        | 64.52 MHz Ring Oscillator                                               | YES                              | nSYS_RST                                                                                    |                                                                                                                                                                                                                                          |
| 16-Bit Counter/Timer 1         | MCLK_DIV2_EN,                                                                                                                                                                                                               |              |                                                                         |                                  |                                                                                             |                                                                                                                                                                                                                                          |
| 16-Bit Counter/Timer 2         | MCLK_DIV4_EN,                                                                                                                                                                                                               |              |                                                                         |                                  |                                                                                             |                                                                                                                                                                                                                                          |
| 16-Bit Counter/Timer 3         | MCLK_DIV8_EN,<br>MCLK_DIV16_EN,<br>MCLK_DIV32_EN,<br>MCLK_DIV64_EN,<br>MCLK_DIV128_EN,<br>EC_BUS_CLK_EN                                                                                                                     |              |                                                                         |                                  |                                                                                             |                                                                                                                                                                                                                                          |
| Master BC Link 1               | MCLK,                                                                                                                                                                                                                       | S0-S5        | 64.52 MHz Ring Oscillator                                               | YES                              | nSYS_RST                                                                                    | Master BC Links                                                                                                                                                                                                                          |
| Master BC Link 2               | EC_BUS_CLK_EN                                                                                                                                                                                                               |              |                                                                         |                                  |                                                                                             |                                                                                                                                                                                                                                          |
| Master BC Link 3               |                                                                                                                                                                                                                             |              |                                                                         |                                  |                                                                                             |                                                                                                                                                                                                                                          |
| Master BC Link 4               |                                                                                                                                                                                                                             |              |                                                                         |                                  |                                                                                             |                                                                                                                                                                                                                                          |
| JTAG                           | MCLK,<br>EC_BUS_CLK_EN                                                                                                                                                                                                      | S0-S5        | 64.52 MHz Ring Oscillator,<br>External (EC CLOCK/4 max.)                | NO                               | nSYS_RST                                                                                    | JTAG clock is externally sourced and is asynchronous to EC clock. The EC clock is required to drive the EC host interface for JTAG access to the EC registers and for the JTAG memory access bus master.                                 |
| Week Timer                     | MCLK,<br>EC_BUS_CLK_EN,<br>X32K_CLK                                                                                                                                                                                         | G0,<br>S0-S5 | 64.52 MHz Ring Oscillator,<br>32.768 KHz Crystal Oscillator             | NO                               | nSYS_RST,<br>VBAT_POR                                                                       | Required accuracy ~10 sec./day; VBAT driven logic controlled by Switched Power Mux.                                                                                                                                                      |
| Power, Clocks and Resets       | MCLK,<br>MCLK_DIV2_EN,<br>MCLK_DIV4_EN,<br>MCLK_DIV8_EN,<br>MCLK_DIV16_EN,<br>MCLK_DIV32_EN,<br>MCLK_DIV64_EN,<br>MCLK_DIV128_EN,<br>MCLK_DIV640_EN,<br>MCLK_DIV64_EN_HST,<br>EC_BUS_CLK_EN,<br>LPC_BUS_CLK_EN,<br>X32K_CLK | G0,<br>S0-S5 | PCI_CLK,<br>64.52 MHz Ring Oscillator,<br>32.768 KHz Crystal Oscillator | YES                              | nSYS_RST,<br>VBAT_POR,<br>VTRGD,<br>nEC_RST,<br>LPC RESET,<br>VCC Power Good,<br>nSIO_RESET | Represents all clock sources, clock controls and resets. <a href="#">Reset Interface</a> includes input from <a href="#">Watch-Dog Timer</a> .                                                                                           |
| RC ID Interface                | MCLK,<br>MCLK_DIV4_EN,<br>MCLK_DIV8_EN,<br>EC_BUS_CLK_EN                                                                                                                                                                    | S0-S5        | 64.52 MHz Ring Oscillator                                               | YES                              | nSYS_RST                                                                                    |                                                                                                                                                                                                                                          |
| Legacy Port Functions          | MCLK,<br>MCLK_DIV64_EN_HST,<br>EC_BUS_CLK_EN                                                                                                                                                                                | S0-S1        | 64.52 MHz Ring Oscillator                                               | YES                              | nSYS_RST,<br>LPC RESET,<br>nSIO_RESET                                                       | PORT92, CPU_RESET, GATEA20 (8042)                                                                                                                                                                                                        |
| Watch-Dog Timer                | MCLK,<br>EC_BUS_CLK_EN,<br>X32K_CLK                                                                                                                                                                                         | S0-S5        | 64.52 MHz Ring Oscillator,<br>32.768 KHz Crystal Oscillator             | NO                               | nSYS_RST                                                                                    |                                                                                                                                                                                                                                          |
| Hibernation Timer 1            | MCLK,                                                                                                                                                                                                                       | S0-S5        | 64.52 MHz Ring Oscillator,                                              | NO                               | nSYS_RST                                                                                    | Can be used as wake timers.                                                                                                                                                                                                              |
| Hibernation Timer 2            | EC_BUS_CLK_EN,<br>X32K_CLK                                                                                                                                                                                                  |              | 32.768 KHz Crystal Oscillator                                           |                                  |                                                                                             |                                                                                                                                                                                                                                          |

**Table 4.6 Block Clocking and Reset Requirements Summary (continued)**

|                          |                                          |       |                                                             |     |                         |                                                |
|--------------------------|------------------------------------------|-------|-------------------------------------------------------------|-----|-------------------------|------------------------------------------------|
| SPI Peripheral Interface | MCLK,<br>MCLK_DIV32_EN,<br>EC_BUS_CLK_EN | S0-S5 | 64.52 MHz Ring Oscillator                                   | YES | nSYS_RST                |                                                |
| GPIO                     | MCLK,<br>EC_BUS_CLK_EN                   | S0-S5 | 64.52 MHz Ring Oscillator                                   | NO  | nSYS_RST                | No clocks needed for asynchronous wake events. |
| LED Interface            | MCLK,<br>EC_BUS_CLK_EN,<br>X32K_CLK      | S0-S5 | 64.52 MHz Ring Oscillator,<br>32.768 KHz Crystal Oscillator | NO  | nSYS_RST                | There are three LEDs in this interface.        |
| ACPI EC INTERFACE        | MCLK,<br>EC_BUS_CLK_EN,<br>PCI_CLK       | S0-S1 | 64.52 MHz Ring Oscillator,<br>PCI_CLK                       | NO  | nSYS_RST                | There are three ports in this interface.       |
| 8042 KBD INTERFACE       |                                          |       |                                                             | NO  | nSYS_RST                | There is one port in this interface.           |
| MAILBOX INTERFACE        |                                          |       |                                                             | NO  | nSYS_RST                | There is one port in this interface.           |
| PS/2 Interface 1         | MCLK,<br>MCLK_DIV32_EN,<br>EC_BUS_CLK_EN | S0-S5 | 64.52 MHz Ring Oscillator                                   | YES | nSYS_RST                | Only Requires "edge" for wake events.          |
| PS/2 Interface 2         |                                          |       |                                                             |     |                         |                                                |
| PS/2 Interface 3         |                                          |       |                                                             |     |                         |                                                |
| MCU Serial Debug Port    | MCLK,<br>EC_BUS_CLK_EN                   | S0-S5 | 64.52 MHz Ring Oscillator                                   | YES | nSYS_RST                |                                                |
| KBD SCAN INTERFACE       | MCLK,<br>EC_BUS_CLK_EN                   | S0-S5 | 64.52 MHz Ring Oscillator                                   | NO  | nSYS_RST                |                                                |
| EC INTERRUPT INTERFACE   | MCLK,<br>EC_BUS_CLK_EN                   | S0-S5 | 64.52 MHz Ring Oscillator                                   | NO  | nSYS_RST                |                                                |
| Flash Interface          | MCLK,<br>EC_BUS_CLK_EN                   | S0-S5 | 64.52 MHz Ring Oscillator                                   | YES | nSYS_RST                | Intrinsic power management controls, also.     |
| 16C550A UART             | MCLK,<br>EC_BUS_CLK_EN                   | S0-S5 | 64.52 MHz Ring Oscillator                                   | YES | nSYS_RST,<br>nSIO_RESET | Can be driven by the LPC host or the EC.       |

**Note 4.9** "YES" in this column means that blocks include [Block Sleep Enables](#) in the [Block Sleep Enable Registers](#) and status bits in the [Clock Required Status Registers](#); "NO" means that blocks are not affected by the [Power Management Interface](#).

## 4.4.7 Power Management Interface

### 4.4.7.1 Overview

The MEC5035 includes several features to help minimize power consumption, the most intrinsic of which is the application of advanced gate-level low-power design techniques. The EC can also establish the upper run-time power consumption limit by asserting individual internal block enables (i.e., as described in the [Generic Block Clocking Model](#)) only for functions that are absolutely required during normal operation. Finally, the EC can also dynamically minimize power consumption by modulating clocks at the block level and within the [Clock Generator](#) using the [Clock Gating](#) feature of the [Power Management Interface](#).

**APPLICATION NOTE:** implementing dynamic power management using individual internal block enables alone is complicated by the fact that, depending on the block implementation, block enables may also perform a reset function.

There are [6 EC Controlled Dynamic Power States](#) as described in [Section 4.4.7.2](#). These states are achieved using [Clock Gating](#) as described in [Section 4.4.7.4 on page 88](#), which can also affect the [64.52 MHz Ring Oscillator](#).

Running and sleeping are the two basic operational modes when considering dynamic power management as defined by this interface ([Figure 4.4](#)). Transitions between these modes are deliberate and persistent. For example, to exit the full power state the EC must issue a sleep command as described in [Section 4.4.7.4.3, "EC Controlled Sleep State Activation," on page 89](#). Exiting sleep states requires the [Wake Interface](#).

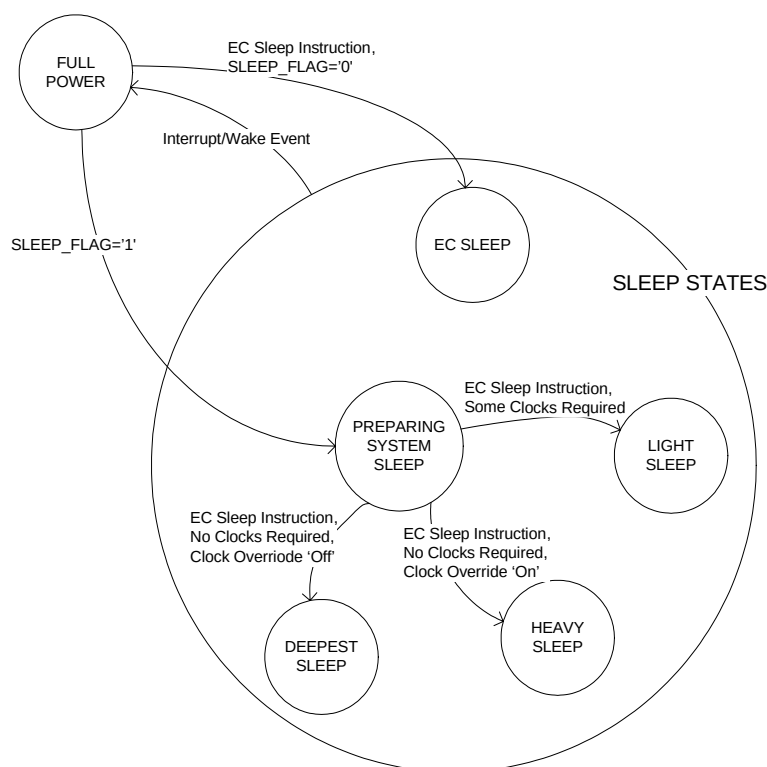


Figure 4.4 Mode Transitions for Dynamic Power Management

#### 4.4.7.2 EC CONTROLLED DYNAMIC POWER STATES

Table 4.7 illustrates the [EC Controlled Dynamic Power States](#) that can be achieved using the [Clock Gating](#) feature of [Power Management Interface](#). The [EC Controlled Dynamic Power States](#) closely mirror the system power states defined by the [Generic Block Clocking Model](#), but 1) redefine the “preparing to sleep” state to include the affects of the EC sleep state, 2) define additional implementation-specific sleep states that affect [Wake Interface](#) latency and 3) indicate the aggregated response of all the MEC5035 power-managed blocks. Typically, the higher the state number in [Table 4.7](#), the greater the system power savings. Traversing the [EC Controlled Dynamic Power States](#) requires the [SLEEP\\_FLAG](#), [ARC\\_CLK\\_DISABLE](#) signal, [WAKE](#) signal, the [ROSC\\_SLP\\_OVRD](#) bit, the [Block Sleep Enable Registers](#) and the [Clock Required Status Registers](#).

See [Section 33.3, “Power Consumption,” on page 522](#) for characterization current values

Table 4.7 EC Controlled Dynamic Power States

| STATE | <a href="#">SLEEP_FLAG</a><br>( <a href="#">Note 4.10</a> ) | <a href="#">ARC_CLK_DISABLE</a><br>( <a href="#">Note 4.11</a> ) | GLOBAL<br>BLOCK<br>CLOCK<br>STATUS<br>( <a href="#">Note 4.12</a> ) | RING<br>OSC.<br>SLEEP<br>OVRD.<br>( <a href="#">Note 4.13</a> ) | STATE<br>NAME | DESCRIPTION                                                                                                      |
|-------|-------------------------------------------------------------|------------------------------------------------------------------|---------------------------------------------------------------------|-----------------------------------------------------------------|---------------|------------------------------------------------------------------------------------------------------------------|
| 1.    | 0                                                           | 0                                                                | X                                                                   | X                                                               | FULL<br>POWER | The system is running. This is the highest power consumption state.                                              |
| 2.    | 0                                                           | 1                                                                | X                                                                   | X                                                               | EC SLEEP      | EC has executed a sleep instruction. The rest of the system is unaffected by the <a href="#">EC SLEEP</a> state. |



Table 4.7 EC Controlled Dynamic Power States (continued)

| STATE | SLEEP_FLAG<br>(Note 4.10) | ARC_CLK_DISABLE<br>(Note 4.11) | GLOBAL BLOCK CLOCK STATUS<br>(Note 4.12) | RING OSC. SLEEP OVRD.<br>(Note 4.13) | STATE NAME             | DESCRIPTION                                                                                                                                                                                                                                                                                                       |
|-------|---------------------------|--------------------------------|------------------------------------------|--------------------------------------|------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3.    | 1                         | 0                              | X                                        | X                                    | PREPARING SYSTEM SLEEP | Sleep commands issued to all sleep-enabled blocks (see <a href="#">Section 4.4.7.4.3, "EC Controlled Sleep State Activation,"</a> on page 89). The EC can return to the <b>FULL POWER</b> state from <b>PREPARING SYSTEM SLEEP</b> by de-asserting ('0') <b>SLEEP_FLAG</b> (see also <a href="#">Note 4.14</a> ). |
| 4.    | 1                         | 1                              | Clock Required                           | X                                    | SYSTEM LIGHT SLEEP     | System is in a sleeping mode but the <b>64.52 MHz Ring Oscillator</b> must remain operating because one or more blocks require a clock.                                                                                                                                                                           |
| 5.    | 1                         | 1                              | Clock Not Required                       | 1                                    | SYSTEM HEAVY SLEEP     | System is in a sleeping mode and no blocks require the clock but the <b>64.52 MHz Ring Oscillator</b> must remain operating because the EC decided to limit start-up latency by preventing the <b>64.52 MHz Ring Oscillator</b> from turning off.                                                                 |
| 6.    | 1                         | 1                              | Clock Not Required                       | 0                                    | SYSTEM DEEPEST SLEEP   | System is in a sleeping mode, no blocks require the clock and the <b>64.52 MHz Ring Oscillator</b> is stopped. This is the lowest possible power consumption state that can be achieved using the <a href="#">Power Management Interface</a> .                                                                    |

**Note 4.10** **SLEEP\_FLAG** is bit D1 in the [Clock Control Register](#).

**Note 4.11** the **ARC\_CLK\_DISABLE** signal is described in [Table 4.1, "Power, Clocks and Resets Port List,"](#) on page 75.

**Note 4.12** includes the sum of all the "Core Clock Required Status" outputs defined in the [Generic Block Clocking Model](#) and aggregated in the [Clock Required Status Registers](#).

**Note 4.13** this column refers to the **ROSC\_SLP\_OVRD** bit in the [Clock Control Register](#).

**Note 4.14** In the **PREPARING SYSTEM SLEEP** state when the sleep enable to a block is asserted, EC register accesses to that block are undefined and should be avoided.

#### 4.4.7.3 64.52 MHz Ring Oscillator Control

The **64.52 MHz Ring Oscillator** can only be controlled by the EC using the [Power Management Interface](#). As illustrated in [Figure 4.5](#) and described in [Table 4.8](#), the **64.52 MHz Ring Oscillator** remains running whenever a single block "Core Clock Required Status" output is asserted, the **ROSC\_SLP\_OVRD** is asserted, **SLEEP\_STATE** is not asserted, or when **WAKE** is asserted. The **64.52 MHz Ring Oscillator** will only stop when all block "Core Clock Required Status" outputs and the **ROSC\_SLP\_OVRD** are not asserted, **WAKE** is not asserted and **SLEEP\_STATE** is asserted.

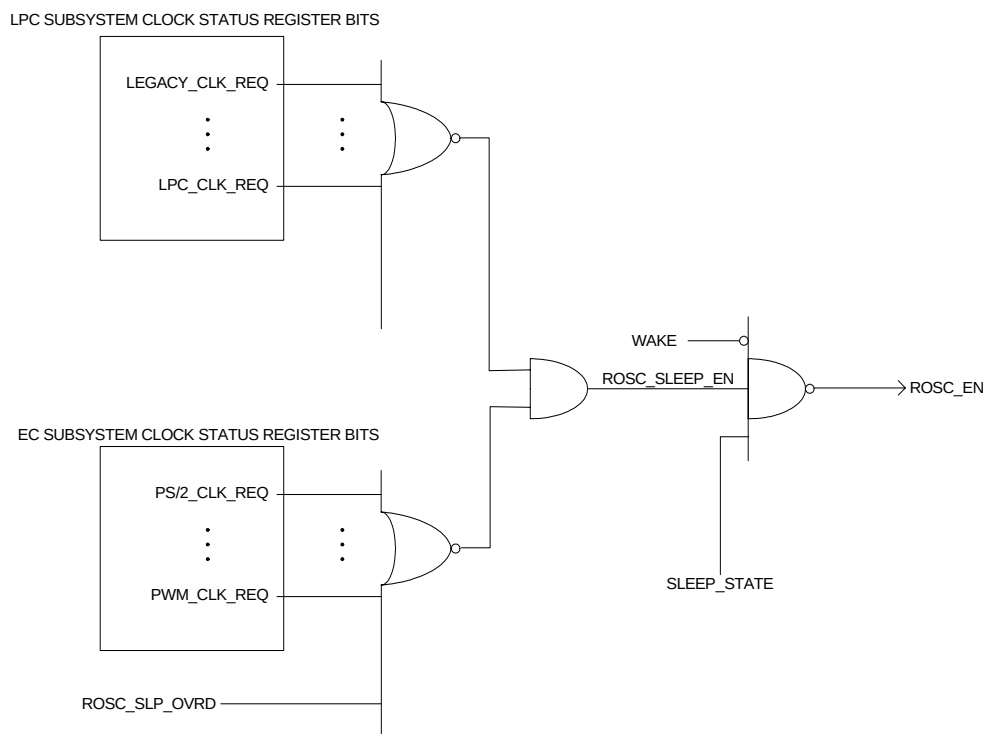


Figure 4.5 64.52 MHz Ring Oscillator Controls

Table 4.8 ROSC\_EN Control

| ROSC_SLEEP_ENBL<br>E<br>(Note 4.15) | SLEEP_STAT<br>E (Note 4.16) | WAKE<br>(Note 4.17) | ROSC_EN<br>(Note 4.18) | DESCRIPTION                                                                                                                                                                                                                                                    |
|-------------------------------------|-----------------------------|---------------------|------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0                                   | X                           | X                   | 1                      | The 64.52 MHz Ring Oscillator is always enabled ("on") when at least one block requires the clock or the EC has overridden the 64.52 MHz Ring Oscillator sleep state using the ROSC_SLP_OVRD bit in the Clock Control Register.                                |
| X                                   | 0                           | X                   |                        | The 64.52 MHz Ring Oscillator is always enabled ("on") when SLEEP_STATE is not asserted.                                                                                                                                                                       |
| X                                   | X                           | 1                   |                        | The 64.52 MHz Ring Oscillator is always enabled ("on") when WAKE is asserted.                                                                                                                                                                                  |
| 1                                   | 1                           | 0                   | 0                      | 64.52 MHz Ring Oscillator is disabled ("off") when SLEEP_STATE is asserted, all blocks do not require the 64.52 MHz Ring Oscillator, the EC has not overridden the 64.52 MHz Ring Oscillator sleep state using the ROSC_SLP_OVRD bit and WAKE is not asserted. |

**Note 4.15** ROSC\_SLEEP\_ENABLE is illustrated in Figure 4.5 and indicates the status of all the "Core Clock Required Status" outputs defined in the Generic Block Clocking Model and

aggregated in the [Clock Required Status Registers](#) and the [ROSC\\_SLP\\_OVRD](#) bit. For a description of the [ROSC\\_SLP\\_OVRD](#) signal, see [Section](#) on page 105.

**Note 4.16** see [Section 4.4.7.4.2, "EC Power State Controls,"](#) on page 88 and [Table 4.1](#) for a description of the [SLEEP\\_STATE](#) signal.

**Note 4.17** see [Section 4.4.7.5, "Wake Interface,"](#) on page 92 and [Table 4.1](#) for a description of the [WAKE](#) signal.

**Note 4.18** [ROSC\\_EN](#) is the [64.52 MHz Ring Oscillator](#) enable control illustrated in [Figure 4.5](#).

#### 4.4.7.4 Clock Gating

##### 4.4.7.4.1 OVERVIEW

Power savings using the [Power Management Interface](#) comes from [Clock Gating](#) as described above and in the subsections that follow. The magnitude of the power savings depends on the configuration of the [Block Sleep Enables](#), the [ROSC\\_SLP\\_OVRD](#) bit in the [Clock Control Register](#) and the operational status of the individual block as defined by the [Clock Required Status Registers](#).

##### 4.4.7.4.2 EC POWER STATE CONTROLS

Assuming [WAKE](#) is not asserted, when the [SLEEP\\_FLAG](#) bit in the [Clock Control Register](#) is asserted by the EC (see also [Section 4.4.7.4.3, "EC Controlled Sleep State Activation"](#)), a sleep command is sent to all blocks that are configured for sleep as defined by the [Block Sleep Enables](#). [Clock Gating](#) occurs at the block level following the sleep command depending on the state of the block clocking requirement (see [Section 4.7.6, "Clock Required Status Registers,"](#) on page 112).

Once the [SLEEP\\_FLAG](#) bit is asserted, [Clock Gating](#) can only occur within the [Clock Generator](#) when the [ARC\\_CLK\\_DISABLE](#) signal (see [Table 4.1, "Power, Clocks and Resets Port List,"](#) on page 75) is asserted, at which time the [SLEEP\\_STATE](#) signal that can affect [64.52 MHz Ring Oscillator Control](#) is asserted ([Table 4.9](#)). Timing for the [EC Power State Controls](#) is defined in [Figure 4.6](#) and [Table 4.10](#).

If [WAKE](#) is asserted when [EC Controlled Sleep State Activation](#) is attempted, the [64.52 MHz Ring Oscillator](#) will remain enabled, the [SLEEP\\_FLAG](#) will be automatically de-asserted by hardware as described in [Section 4.4.7.5, "Wake Interface,"](#) on page 92 and an EC interrupt will occur (not shown in [Table 4.9](#)).

**Table 4.9 EC Power State Controls Description**

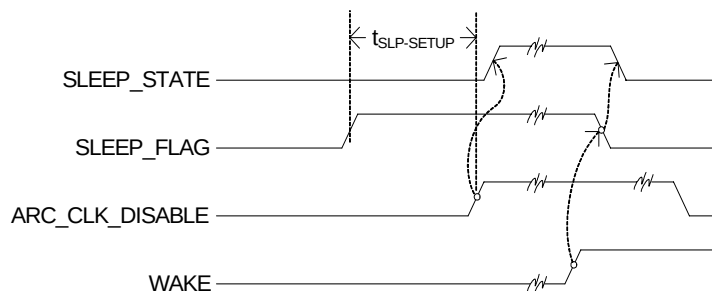
| <a href="#">ARC_CLK_DISABLE</a><br>( <a href="#">Note 4.11</a> ) | <a href="#">SLEEP_FLAG</a><br>( <a href="#">Note 4.10</a> ) | <a href="#">SLEEP_STATE</a><br>( <a href="#">Note 4.20</a> ) | <b>STATES</b><br>( <a href="#">Note 4.19</a> ) | <b>DESCRIPTION</b>                                                                                                                                                                                                                                                                                                                                                                                                   |
|------------------------------------------------------------------|-------------------------------------------------------------|--------------------------------------------------------------|------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0                                                                | 0                                                           | 0                                                            | <a href="#">FULL POWER</a>                     | –                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 0                                                                | 1                                                           | 0                                                            | <a href="#">PREPARING SYSTEM SLEEP</a>         | <a href="#">SLEEP_FLAG</a> has been asserted by the EC which asserts sleep enables to blocks that have been enabled for sleeping; i.e., clocks in these blocks are turning 'off' in this state. The EC and the <a href="#">64.52 MHz Ring Oscillator</a> clock remain active. The <a href="#">PREPARING SYSTEM SLEEP</a> state may represent a lower than <a href="#">FULL POWER</a> system power consumption state. |

**Table 4.9 EC Power State Controls Description (continued)**

| ARC_CLK_DISABLE<br>(Note 4.11) | SLEEP_FLAG<br>(Note 4.10) | SLEEP_STATE<br>(Note 4.20) | STATES<br>(Note 4.19)                                              | DESCRIPTION                                                                                                                                                                                                                                  |
|--------------------------------|---------------------------|----------------------------|--------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1                              | 0                         | 0                          | EC SLEEP                                                           | The Clock Generator is unaffected in the EC SLEEP state. The EC SLEEP state may or may not represent a lower system power state than the PREPARING SYSTEM SLEEP state depending on the Block Sleep Enables and the system operational state. |
| 1                              | 1                         | 1                          | SYSTEM LIGHT SLEEP,<br>SYSTEM HEAVY SLEEP,<br>SYSTEM DEEPEST SLEEP | The 64.52 MHz Ring Oscillator may be stopped as described in Section 4.4.7.3, "64.52 MHz Ring Oscillator Control," on page 86 and in Table 4.7.                                                                                              |

**Note 4.19** see the system state definitions in Table 4.7, "EC Controlled Dynamic Power States," on page 85.

**Note 4.20** SLEEP\_STATE affects the 64.52 MHz Ring Oscillator as described in Section 4.4.7.3, "64.52 MHz Ring Oscillator Control," on page 86 and appears in Table 4.1, "Power, Clocks and Resets Port List," on page 75.

**Figure 4.6 EC Power State Controls Timing****Table 4.10 EC Power State Controls Timing Parameters**

| PARAMETERS              | SYMBOL                 | MIN | TYP | MAX | UNITS    |
|-------------------------|------------------------|-----|-----|-----|----------|
| System Sleep Setup Time | $t_{\text{SLP-SETUP}}$ | 1   | —   | —   | EC Clock |

#### 4.4.7.4.3 EC CONTROLLED SLEEP STATE ACTIVATION

##### OVERVIEW

EC Controlled Sleep State Activation depends upon the assertion of the ARC\_CLK\_DISABLE signal which occurs when the EC executes a sleep instruction. The dynamic sleep states that can be achieved through EC Controlled Sleep State Activation in part depend on the state of the SLEEP\_FLAG in the Clock Control Register as defined in the sections below, "Entering and Exiting EC Sleep State" and "Entering and Exiting System Sleep States."

In all cases, EC Controlled Sleep State Activation should not be attempted when the WAKE bit in the PCR Status and Control Register is asserted. Simultaneous assertions of WAKE and EC Controlled

Sleep State Activation immediately terminate system sleeps states as defined in Section 4.4.7.5, "Wake Interface," on page 92.

#### ENTERING AND EXITING EC SLEEP STATE

As illustrated in Table 4.7, "EC Controlled Dynamic Power States," on page 85, transitions to the EC SLEEP state occur when the ARC\_CLK\_DISABLE signal is asserted while the SLEEP\_FLAG in the Clock Control Register is not asserted ('0'). The EC SLEEP state is terminated when an interrupt to the EC occurs, as described in Section 4.4.7.5, "Wake Interface," on page 92. Entering and Exiting EC Sleep State from the EC firmware perspective is illustrated in Figure 4.7.

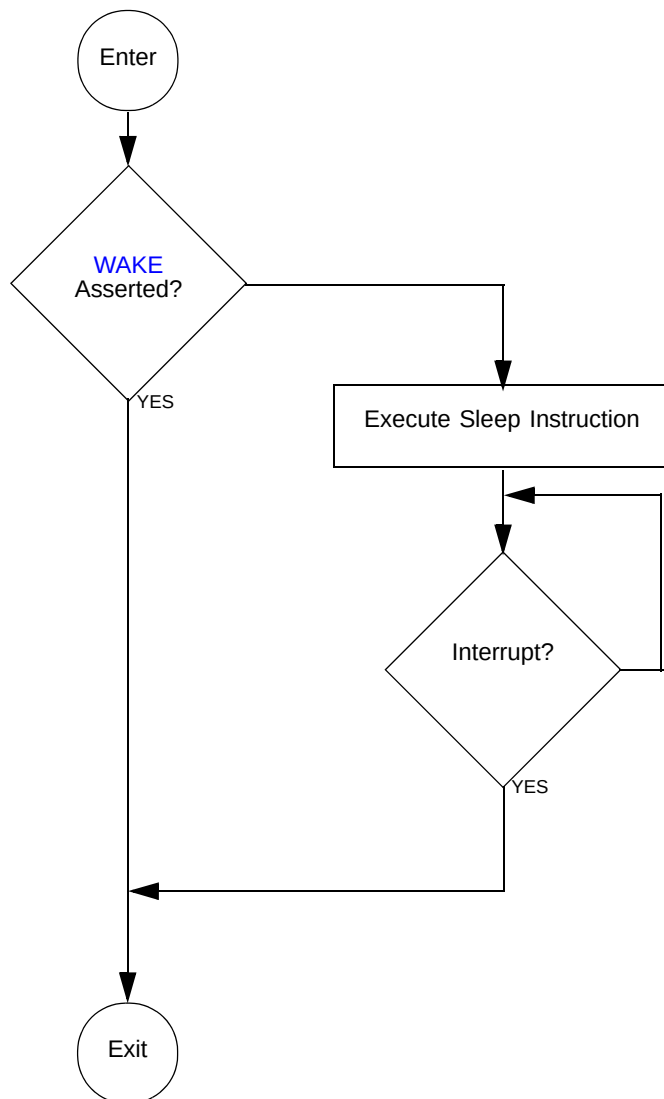


Figure 4.7 Firmware Flow for Entering and Exiting the EC SLEEP State

#### ENTERING AND EXITING SYSTEM SLEEP STATES

As illustrated in Table 4.7, "EC Controlled Dynamic Power States," on page 85, transitions to the system sleep states (i.e., sleep states other than EC SLEEP) occur when the ARC\_CLK\_DISABLE signal is asserted while the SLEEP\_FLAG in the Clock Control Register is asserted ('1'). These states include SYSTEM LIGHT SLEEP, SYSTEM HEAVY SLEEP and SYSTEM DEEPEST SLEEP.

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The system sleep states are terminated when a wake event occurs as described in [Section 4.4.7.5, "Wake Interface,"](#) on page 92. Entering and Exiting System Sleep States from the EC firmware perspective is illustrated in [Figure 4.8](#).

Note that as described in [Section 4.4.7.2, "EC Controlled Dynamic Power States,"](#) on page 85, the [PREPARING SYSTEM SLEEP](#) state in [Table 4.7](#) occurs as soon as the [SLEEP\\_FLAG](#) is asserted, independent of the state of [ARC\\_CLK\\_DISABLE](#). The EC can optionally interrogate the [Clock Required Status Registers](#) to estimate the depth of the sleep state, for example, before executing a sleep instruction (not shown in [Figure 4.8](#)). The EC can return to the [FULL POWER](#) state from the [PREPARING SYSTEM SLEEP](#) state at any time before executing a sleep instruction by de-asserting the [SLEEP\\_FLAG](#).

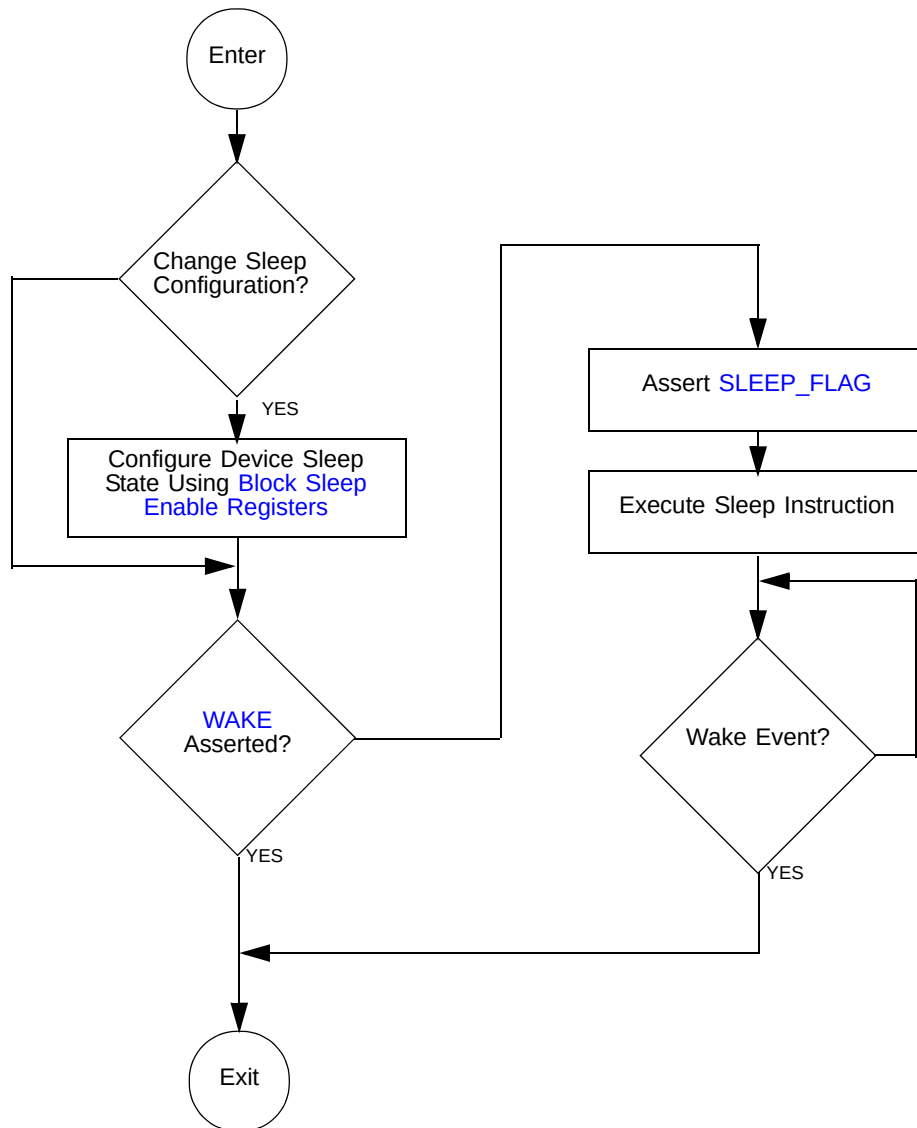


**Figure 4.8 Firmware Flow for Entering and Exiting Lowest Power EC-Controlled System Sleep States**

#### 4.4.7.4.4 BLOCK SLEEP ENABLES

The [Block Sleep Enables](#) allow the EC firmware to determine which blocks will receive sleep commands as a result of [EC Controlled Sleep State Activation](#) (see [Entering and Exiting System Sleep States](#) on page 90). The [Block Sleep Enables](#) are configured using the [Block Sleep Enable Registers](#) (see [Section 4.7.5](#) on page 110) and behave as illustrated in [Figure 4.9](#) and [Table 4.11](#). There are

two **Block Sleep Enable Registers**: the **EC Blocks Sleep Enables Register** (see [Section 4.7.5.2 on page 111](#)) and the **LPC Blocks Sleep Enables Register** ([Section 4.7.5.1 on page 110](#)).

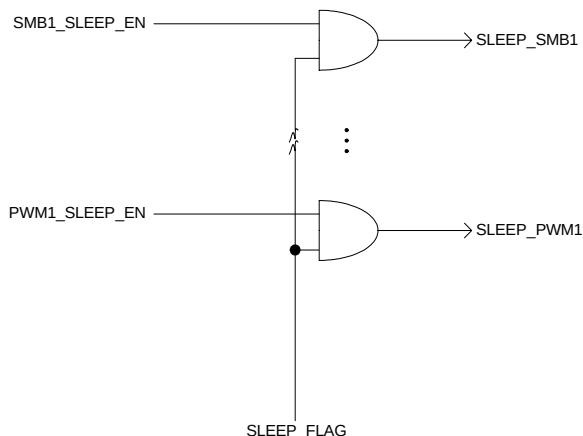


**Figure 4.9 Block Sleep Enables Example**

**Table 4.11 Block Sleep Enables Definition**

| <b>SLEEP ENABLE</b><br>( <a href="#">Note 4.21</a> ) | <b>SLEEP_FLAG</b><br>( <a href="#">Note 4.10</a> ) | <b>BLOCK SLEEP_EN SIGNAL</b><br>( <a href="#">Note 4.22</a> ) | <b>DESCRIPTION</b>                                                                                                                                                |
|------------------------------------------------------|----------------------------------------------------|---------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0                                                    | 0                                                  | 0                                                             | Block not enabled for sleep, system is in <b>FULL POWER</b> or <b>EC SLEEP</b> state.                                                                             |
|                                                      | 1                                                  |                                                               | Block not enabled for sleep, system is in <b>PREPARING SYSTEM SLEEP</b> or <b>SYSTEM LIGHT SLEEP</b> state.                                                       |
| 1                                                    | 0                                                  | 1                                                             | Block enabled for sleep, system is in <b>FULL POWER</b> or <b>EC SLEEP</b> state.                                                                                 |
|                                                      | 1                                                  |                                                               | Block enabled for sleep, system is in <b>PREPARING SYSTEM SLEEP</b> , <b>SYSTEM LIGHT SLEEP</b> , <b>SYSTEM HEAVY SLEEP</b> or <b>SYSTEM DEEPEST SLEEP</b> state. |

**Note 4.21** sleep enable for a single block as defined in [Section 4.7.5, "Block Sleep Enable Registers," on page 110](#).

**Note 4.22** **Clock Generator** sleep enable output signal to a single block (SLEEP\_EN) as defined in the [Generic Block Clocking Model](#).

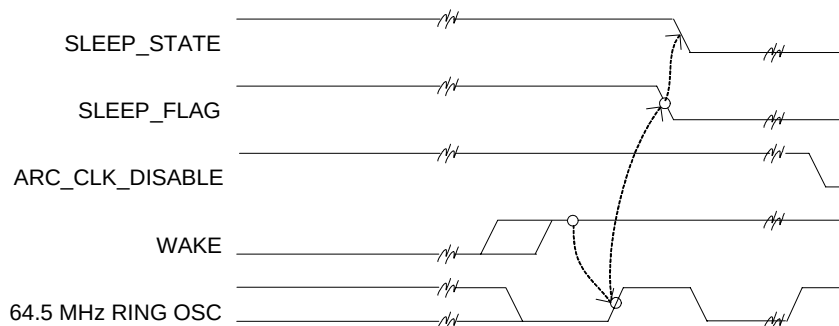
#### 4.4.7.5 Wake Interface

The **Wake Interface** terminates the sleep states illustrated in [Table 4.7, "EC Controlled Dynamic Power States," on page 85](#) and includes interrupts to the EC to transition from the **EC SLEEP** state, as well as wake events that can restart the **64.52 MHz Ring Oscillator** and terminate the **SYSTEM LIGHT SLEEP**, **SYSTEM HEAVY SLEEP** and **SYSTEM DEEPEST SLEEP** states.

The **WAKE** signal shown in [Table 4.1, "Power, Clocks and Resets Port List," on page 75](#) is the only required input to the **Clock Generator** for the **Wake Interface**. EC interrupts, although technically part of the **Wake Interface**, are external to the **Power, Clocks and Resets** function and are not illustrated in this definition. The minimum pulse-width for wake events is characterized in [Note 17.2 on page 373](#).

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When the **WAKE** signal is asserted while a dynamic system sleep state is enabled, the **SLEEP\_FLAG** in the **Clock Control Register** is automatically de-asserted by hardware within the first one or two clocks that occur when the **64.52 MHz Ring Oscillator** is re-enabled as illustrated in **Figure 4.10**. As described in **Section 4.4.7.4.2, "EC Power State Controls," on page 88** and in **Section 4.4.7.4.3, "EC Controlled Sleep State Activation," on page 89**, system sleep states are essentially ignored if the **SLEEP\_STATE** signal and the **WAKE** signal are simultaneously asserted.

**Figure 4.10 Wake Interface Timing****4.4.8 Ring Oscillator Sourced Clocking****4.4.8.1 Overview**

**Ring Oscillator Sourced Clocking** includes all of the **Fixed Clock Domain**, **Host Clock Domain** and **Programmable Clock Domains** that are derived from the **64.52 MHz Ring Oscillator**. **Ring Oscillator Sourced Clocking** remains active as long as the **64.52 MHz Ring Oscillator** is running (see **Section 4.4.7.3, "64.52 MHz Ring Oscillator Control," on page 86**).

The distribution of **Ring Oscillator Sourced Clocking** throughout the MEC5035 is illustrated in **Table 4.6, "Block Clocking and Reset Requirements Summary," on page 83**. All **Ring Oscillator Sourced Clocking** and **32K Clock Domain** clocking is summarized in **Table 4.12**.

**Table 4.12 All Clock Generator Output Ports Summary**

| SYMBOL         | TYPE<br>(CLOCK OR<br>ENABLE) | FREQUENCY    | REFERENCE                                                              |
|----------------|------------------------------|--------------|------------------------------------------------------------------------|
| MCLK           | CLOCK                        | 64.52 MHz    | <a href="#">Section 4.4.3, "64.52 MHz Ring Oscillator," on page 79</a> |
| EC_BUS_CLK_EN  | ENABLE                       | Programmable | <a href="#">Section 4.4.8.2.1, "EC Bus Clock," on page 94</a>          |
| LPC_BUS_CLK_EN | ENABLE                       | Programmable | <a href="#">Section 4.4.8.2.2, "LPC Bus Clock," on page 94</a>         |



**Table 4.12 All Clock Generator Output Ports Summary (continued)**

| SYMBOL            | TYPE<br>(CLOCK OR<br>ENABLE) | FREQUENCY  | REFERENCE                                                  |
|-------------------|------------------------------|------------|------------------------------------------------------------|
| MCLK_DIV2_EN      | ENABLE                       | 32.26 MHz  | Section 4.4.8.3, "Fixed Clock Domain," on page 94          |
| MCLK_DIV4_EN      | ENABLE                       | 16.13 MHz  |                                                            |
| MCLK_DIV8_EN      | ENABLE                       | 8.06 MHz   |                                                            |
| MCLK_DIV16_EN     | ENABLE                       | 4.03 MHz   |                                                            |
| MCLK_DIV32_EN     | ENABLE                       | 2.02 MHz   |                                                            |
| MCLK_DIV64_EN     | ENABLE                       | 1.01 MHz   |                                                            |
| MCLK_DIV128_EN    | ENABLE                       | 504 KHz    |                                                            |
| MCLK_DIV640_EN    | ENABLE                       | 101 KHz    | Section 4.4.8.4, "Host Clock Domain," on page 94           |
| MCLK_DIV64_EN_HST | ENABLE                       | 1.01 MHz   |                                                            |
| X32K_CLK          | CLOCK                        | 32.768 KHz | Section 4.4.4, "32.768 KHz Crystal Oscillator," on page 79 |

#### 4.4.8.2 Programmable Clock Domains

##### 4.4.8.2.1 EC BUS CLOCK

The [EC Bus Clock](#) ([EC\\_BUS\\_CLK\\_EN](#)) is a programmable clock that is derived from the [EC Clock Divider Register](#) as described in [Section 4.7.2 on page 106](#).

##### 4.4.8.2.2 LPC BUS CLOCK

The [LPC Bus Clock](#) ([LPC\\_BUS\\_CLK\\_EN](#)) is a programmable clock that is derived from the [LPC\\_AHB Clock Divider Register](#) as described in [Section 4.7.3 on page 107](#).

#### 4.4.8.3 Fixed Clock Domain

The [Fixed Clock Domain](#) represents non-programmable clocks that are derived from the [64.52 MHz Ring Oscillator](#). The [Fixed Clock Domain](#) outputs as shown in [Table 4.12](#) are [MCLK](#), [MCLK\\_DIV2\\_EN](#), [MCLK\\_DIV4\\_EN](#), [MCLK\\_DIV8\\_EN](#), [MCLK\\_DIV16\\_EN](#), [MCLK\\_DIV32\\_EN](#), [MCLK\\_DIV64\\_EN](#), [MCLK\\_DIV128\\_EN](#), and [MCLK\\_DIV640\\_EN](#).

#### 4.4.8.4 Host Clock Domain

The [Host Clock Domain](#) includes clocking for the [Legacy Port Functions](#). [Host Clock Domain](#) clock gating is controlled by [VCC\\_PWRGD](#) such that when [VCC\\_PWRGD](#) is not asserted ('0'), clocks in the [Host Clock Domain](#) are 'off.'

When [VCC\\_PWRGD](#) is asserted ('1') clocks in the [Host Clock Domain](#) are 'on' and the [Legacy Port Functions](#) may be affected by the [EC Controlled Dynamic Power States](#) as described in [Section 4.4.7, "Power Management Interface," on page 84](#).

The [Host Clock Domain](#) output as shown in [Table 4.12](#) is [MCLK\\_DIV64\\_EN\\_HST](#).



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## 4.4.9 32K Clock Domain

### 4.4.9.1 Overview

The **32K Clock Domain** represents all of the clocking derived from the **32.768 KHz Crystal Oscillator**. The output of the **32.768 KHz Crystal Oscillator** is synchronized to the **64.52 MHz Ring Oscillator** as described below in [Section 4.4.9.2, "Synchronization," on page 95](#).

The **32K Clock Domain** remains active as long as the **32.768 KHz Crystal Oscillator** is running (see [Section , "32K\\_EN," on page 117](#)). The blocks driven by the **32K Clock Domain** are summarized in [Table 4.13](#) and are not affected by **Clock Gating** in the **Power Management Interface**. Typically, blocks driven by the **32K Clock Domain** can generate wake events, even when the **64.52 MHz Ring Oscillator** is disabled.

### 4.4.9.2 Synchronization

The **32K Clock Domain X32K\_CLK** output is synchronized to the **64.52 MHz Ring Oscillator**. **Synchronization** is disabled under three conditions: 1) when the **64.52 MHz Ring Oscillator** is disabled (e.g., in the **SYSTEM DEEPEST SLEEP** state or during a test mode) and 2) when **VTRGD** is not asserted (see [Section 4.6.2, "VTRGD," on page 99](#)).

Note that the output of the **32.768 KHz Crystal Oscillator** that is applied to the **64.52 MHz Ring Oscillator** is not synchronized.

### 4.4.9.3 Summary

The distribution of the **32K Clock Domain** throughout the MEC5035 is illustrated in [Table 4.6, "Block Clocking and Reset Requirements Summary," on page 83](#) and in [Table 4.13](#), below.

**Table 4.13 32K Clock Domain Driven Blocks**

| BLOCK NAME ( <a href="#">Note 4.40</a> )     | BLOCK CROSS REFERENCE                                                                               |
|----------------------------------------------|-----------------------------------------------------------------------------------------------------|
| Week Timer                                   | <a href="#">Chapter 21, "Week Alarm Interface," on page 404</a>                                     |
| Watch-Dog Timer                              | <a href="#">Chapter 19, "Watchdog Timer Interface," on page 390</a>                                 |
| Hibernation Timer 1                          | <a href="#">Chapter 20, "Hibernation Timer," on page 399</a>                                        |
| Hibernation Timer 2                          | <a href="#">Chapter 20, "Hibernation Timer," on page 399</a>                                        |
| LED Interface                                | <a href="#">Chapter 27, "LED," on page 470</a>                                                      |
| <a href="#">Watch-Dog Timer Forced Reset</a> | <a href="#">Section 4.6.10, "Watch-Dog Timer Forced Reset," on page 103.</a>                        |
| <a href="#">64.52 MHz Ring Oscillator</a>    | <a href="#">Section 4.4.3, "64.52 MHz Ring Oscillator," on page 79 (<a href="#">Note 4.23</a>).</a> |

**Note 4.23** [Synchronization](#) as described in [Section 4.4.9.2](#) does not apply to the output of the **32.768 KHz Crystal Oscillator** that is applied to the **64.52 MHz Ring Oscillator**.

## 4.5 Power Configuration

### 4.5.1 Power Supplies and Clocks ACPI Context

The MEC5035 is influenced by three separate power planes, [VBAT](#), [VTR](#), and VCC, as described in [Table 4.14](#). The [VBAT](#) and [VTR](#) power planes provide power directly to the MEC5035 through the [VBAT](#) and [VTR](#) pins shown in [Table 4.1, "Power, Clocks and Resets Port List"](#). The MEC5035 senses the VCC power state using the [VCC\\_PWRGD](#) input pin. The [VBAT](#), [VTR](#), and VCC power sequencing requirements are as follows (see also [Section 4.5.3, "Power-Up Sequence," on page 98](#)):

1. VCC power can be applied simultaneously with or after [VTR](#) power.
2. [VTR](#) power can be applied simultaneously with or after [VBAT](#).

The typical relationships of the MEC5035 power supplies to the system power states is shown below in [Table 4.14](#). The distribution of the MEC5035 power supplies to the various functional blocks is illustrated in [Figure 2.1 MEC5035 Block Diagram on page 36](#)

The typical relationships of the MEC5035 clocks to the system power states is shown below in [Table 4.15](#). Descriptions of the various clock domains can be found in [Section 4.4, "Clock Generator," on page 77](#).

**Table 4.14 Typical MEC5035 Power Supplies vs. ACPI Power States**

| SUPPLY NAME          | ACPI POWER STATE |          |          |          |               |               | DESCRIPTION                                                                                                                                                                      |
|----------------------|------------------|----------|----------|----------|---------------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                      | S0 (FULL ON)     | S1 (POS) | S3 (STR) | S4 (STD) | S5 (SOFT OFF) | G3 (MECH OFF) |                                                                                                                                                                                  |
| <a href="#">VBAT</a> | ON               | ON       | ON       | ON       | ON            | ON            | MEC5035 V <sub>BAT</sub> Well Supply (assuming a <a href="#">TYPE 2</a> configuration as described in <a href="#">Section 4.5.2, "Power Supply Configurations," on page 97</a> ) |
| <a href="#">VTR</a>  | ON               | ON       | ON       | ON/OFF   | ON/OFF        | OFF           | MEC5035 Suspend Supply. ( <a href="#">Note 4.24</a> )                                                                                                                            |
| VCC                  | ON               | ON       | OFF      | OFF      | OFF           | OFF           | MEC5035 Runtime Supply ( <a href="#">Note 4.25</a> )                                                                                                                             |

**Note 4.24** [VTR](#) availability in S4 - S5 may depend, for example, on whether AC power is available.

**Note 4.25** the MEC5035 senses the VCC power state using the [VCC\\_PWRGD](#) input pin; i.e., VCC power is not directly applied to this device.

**Table 4.15 Typical MEC5035 Clocks vs. ACPI Power States**

| CLOCK NAME                                   | ACPI POWER STATE |          |          |          |               |               | DESCRIPTION                                                                                                                                                                                                          |
|----------------------------------------------|------------------|----------|----------|----------|---------------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                              | S0 (FULL ON)     | S1 (POS) | S3 (STR) | S4 (STD) | S5 (SOFT OFF) | G3 (MECH OFF) |                                                                                                                                                                                                                      |
| <a href="#">32K Clock Domain</a> (XOSEL='1') | ON               | ON       | ON       | ON       | ON            | OFF/ ON       | When <a href="#">XOSEL</a> = '1' and the XTAL2 pin is driven, for example, by an Intel ICH4M SUSCLK, the <a href="#">32K Clock Domain</a> is running whenever RSMRST is not asserted. (see <a href="#">Ref[2]</a> ). |

Table 4.15 Typical MEC5035 Clocks vs. ACPI Power States (continued)

| CLOCK NAME                                        | ACPI POWER STATE   |             |             |             |                     |                     | DESCRIPTION                                                                                                                                                                                                                         |
|---------------------------------------------------|--------------------|-------------|-------------|-------------|---------------------|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                   | S0<br>(FULL<br>ON) | S1<br>(POS) | S3<br>(STR) | S4<br>(STD) | S5<br>(SOFT<br>OFF) | G3<br>(MECH<br>OFF) |                                                                                                                                                                                                                                     |
| 32K Clock Domain<br>(XOSEL='0')                   | ON                 | ON          | ON          | ON          | ON                  | ON                  | When XOSEL = '0' and a 32.768KHz crystal is connected between the XTAL1 and XTAL2 pins, the 32K Clock Domain is running whenever VBAT is fully powered except following a VBAT_POR as described in Section , "32K_EN," on page 117. |
| Host Clock Domain                                 | ON                 | ON          | OFF         | OFF         | OFF                 | OFF                 | The Host Clock Domain is gated by the MEC5035 runtime supply (VCC) as described in Section 4.4.8.4, "Host Clock Domain," on page 94.                                                                                                |
| PCI_CLK                                           | ON/OFF             | ON/OFF      | OFF         | OFF         | OFF                 | OFF                 | 33MHz LPC Bus clock input powered by the MEC5035 runtime supply (VCC). (Note 4.26)                                                                                                                                                  |
| Programmable Clock Domains and Fixed Clock Domain | ON/OFF             | ON/OFF      | ON/OFF      | OFF/ON      | OFF/ON              | OFF                 | These clocks are powered by the MEC5035 suspend supply (VTR) but may start and stop as described in Section 4.4.7, "Power Management Interface," on page 84. (see also Note 4.24)                                                   |

**Note 4.26** the PCI\_CLK can start and stop in S0/S1 as defined in Ref[3].

## 4.5.2 Power Supply Configurations

There are two acceptable types of MEC5035 power supply configuration that fundamentally differ based on the need for a backup battery connection to VBAT.

### 4.5.2.1 TYPE 1

TYPE 1 configurations do not use a VBAT backup battery connection. Power supply requirements for TYPE 1 configurations are as follows: VBAT is tied to VSS and VTR is connected to the suspend supply as described in Section 4.5.1, "Power Supplies and Clocks ACPI Context".

In this configuration some internal components that utilize the VBAT power plane are switched internally to VTR using a Power Mux when VTRpower is applied according to the internal VTRGD signal (see also Section 4.6.7, "Power Mux," on page 101).

In TYPE 1 configurations, the VBAT-Powered Control Interface cannot be used to power-on an unpowered system and firmware must provide defaults for all VBAT-powered registers following each VBAT\_POR.

#### 4.5.2.2 TYPE 2

TYPE 2 configurations use an un-switched VBAT backup battery connection. Power supply requirements for TYPE 2 configurations are as follows: VBAT is connected to an un-switched backup battery and VTR is connected to the suspend supply as described in Section 4.5.1, "Power Supplies and Clocks ACPI Context".

In this configuration some internal components that utilize the VBAT power plane are switched internally to VTR using a Power Mux when VTR power is applied as described in Section 4.6.7, "Power Mux," on page 101.

In TYPE 2 configurations, the VBAT-Powered Control Interface can be used to power-on an unpowered system.

### 4.5.3 Power-Up Sequence

Table 4.16 summarizes the MEC5035 Power-Up Sequence. For information regarding the typical relationships of the MEC5035 power supplies to the system power states see Section 4.5, "Power Configuration," on page 96.

**Table 4.16 Power-up Sequence**

|    | VBAT | VTR | VCC | Reset Interface                                            | DESCRIPTION                                                                                                                                                                                                            |
|----|------|-----|-----|------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1. | OFF  | OFF | OFF | —                                                          | MEC5035 fully unpowered                                                                                                                                                                                                |
| 2. | ON   | OFF | OFF | —                                                          | 32.768 KHz Crystal Oscillator may be disabled as described in Section 4.6.3, "VBAT_POR," on page 100.                                                                                                                  |
| 3. | ON   | ON  | OFF | VBAT_POR,<br>VTRGD,<br>nSYS_RST,<br>nEC_RST,<br>nSIO_RESET | VBAT-powered registers may be reset as described in Section 4.6.3, "VBAT_POR," on page 100. VTR-powered registers and blocks reset (nSYS_RST). EC held in reset as described in Section 4.6.5, "nEC_RST," on page 101. |
|    |      |     |     |                                                            | nSIO_RESET asserted.                                                                                                                                                                                                   |
|    |      |     |     |                                                            | 64.52 MHz Ring Oscillator enabled.                                                                                                                                                                                     |
|    |      |     |     |                                                            | EC begins code execution following a delay as described in Section 4.6.5, "nEC_RST," on page 101.                                                                                                                      |
| 4. | ON   | ON  | ON  | VCC_PWRGD,<br>nSIO_RESET                                   | Registers affected by VCC_PWRGD are reset (Note 4.27)                                                                                                                                                                  |
|    |      |     |     |                                                            | Firmware de-asserts nSIO_RESET as described in Section , "iRESET OUT," on page 109.                                                                                                                                    |

**Note 4.27** for VTR-powered on-chip registers that are reset by VCC\_PWRGD, it is important that firmware not write to any of these registers until 1 ms following the assertion of VCC\_PWRGD ('1').

## 4.6 Reset Interface

### 4.6.1 Overview

The primary function of the [Reset Interface](#) ([Figure 4.28](#)) is to generate [VTR](#) and [VBAT](#) reset signaling; including, [VTRGD](#), [VBAT\\_POR](#), [nSYS\\_RST](#), [nEC\\_RST](#) and [Watch-Dog Timer Forced Reset](#). The [Reset Interface](#) also includes a section regarding the [1.8V Regulator](#). There is other VCC-related [Reset Interface](#) functionality not shown in [Figure 4.28](#) that is described [Section 4.6.8, "VCC Power Good,"](#) on page 102 and [Section 4.6.9, "LPC RESET,"](#) on page 102.

Also included in the [Reset Interface](#) are descriptions of the [Power Mux](#) and [Strapping Options](#). These are related [Power, Clocks and Resets](#) functions that are illustrated in [Figure 4.28](#), but are not described anywhere else in this chapter.

The relationship of the [Reset Interface](#) to the MEC5035 functional blocks is illustrated in [Table 4.6, "Block Clocking and Reset Requirements Summary,"](#) on page 83.

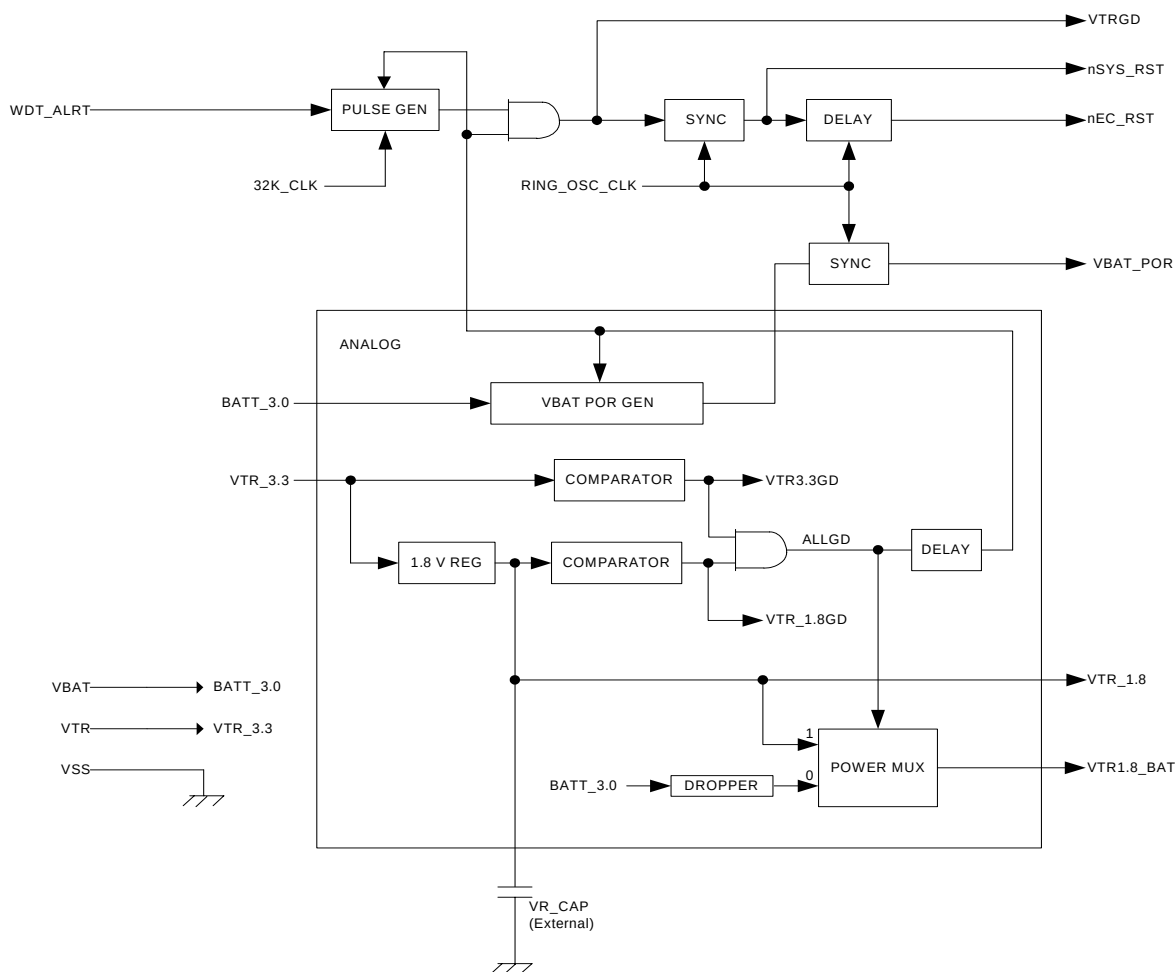


Figure 4.28 Reset Interface Block Diagram

### 4.6.2 VTRGD

[VTRGD](#) ([Figure 4.28](#)) is the reset signal for the [64.52 MHz Ring Oscillator](#) and the source for [nSYS\\_RST](#) and [nEC\\_RST](#).

As shown in [Figure 4.28](#), [Figure 4.29](#) and in [Table 4.17](#), [VTRGD](#) is asserted following a delay after the [VTR](#) and [VTR\\_1.8](#) power supplies exceed preset voltage thresholds. [VTRGD](#) is de-asserted as soon

as either the **VTR** or **VTR\_1.8** power supplies drop below these thresholds (see [Figure 4.31 VTR Power-Down Timing](#) on page 100).

**VTRGD** can also be asserted as a result of a [Watch-Dog Timer Forced Reset](#) as described in [Section 4.6.10, "Watch-Dog Timer Forced Reset,"](#) on page 103.

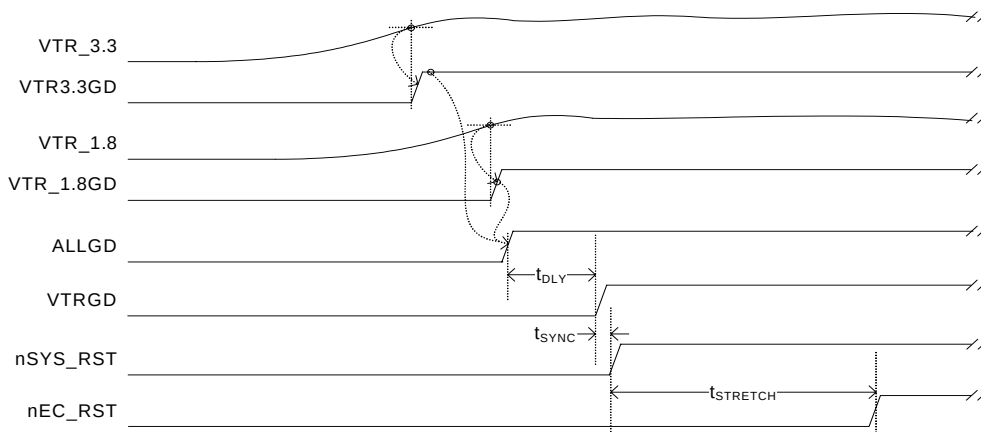


**Figure 4.29 VTR Power-Up Timing**

**Table 4.17 VTR Power-Up Timing**

| PARAMETERS                 | SYMBOL        | MIN | TYP | MAX | UNITS                            | NOTES                     |
|----------------------------|---------------|-----|-----|-----|----------------------------------|---------------------------|
| <b>VTRGD</b> Delay Time    | $t_{DLY}$     |     | 360 |     | $\mu\text{s}$                    |                           |
| <b>nSYS_RST</b> Delay Time | $t_{SYNC}$    | 2   | —   | 3   | 64.52 MHz Ring Oscillator Clocks | <a href="#">Note 4.30</a> |
| <b>nEC_RST</b> Delay Time  | $t_{STRETCH}$ | 10  | 20  | 40  | ms                               |                           |

**Note 4.30** this interval is determined using a [Fixed Clock Domain](#) from the 64.52 MHz Ring Oscillator.

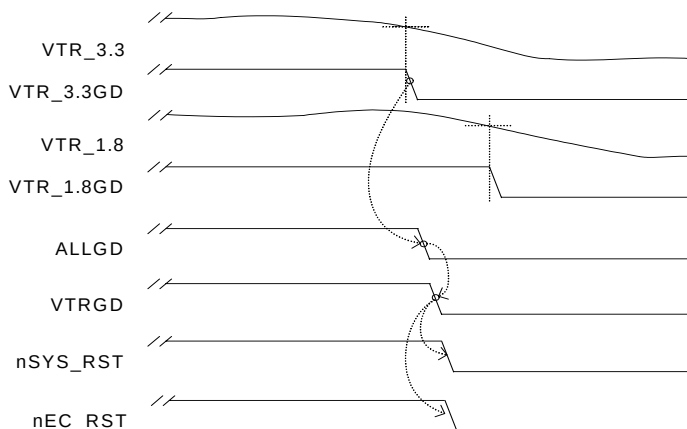


**Figure 4.31 VTR Power-Down Timing**

### 4.6.3 VBAT\_POR

**VBAT\_POR** is a pulse that is asserted at the rising edge of **VTRGD** ([Figure 4.29](#)) if the coin cell is replaced, or the **VBAT** voltage falls below 1.25 V nominal while **VTRGD** is not asserted ('0'). Note



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that the [32.768 KHz Crystal Oscillator](#) is stopped if the coin cell is replaced, or the [VBAT](#) voltage falls below 1.25 V nominal while [VTRGD](#) is not asserted. No action is taken if the coin cell is replaced, or the [VBAT](#) voltage falls below 1.25 V nominal while [VTRGD](#) is asserted

[VBAT\\_POR](#) is used as described throughout this specification to reset registers and functional device blocks. [VBAT\\_POR](#) events are registered in the [Power-Fail and Reset Status Register](#).

### 4.6.4 nSYS\_RST

[nSYS\\_RST](#) is [VTRGD](#) synchronized to the [64.52 MHz Ring Oscillator](#) (Figure 4.29). Note that [VTRGD](#) and [nSYS\\_RST](#) have the same logical sense (uninverted); however, because of nomenclature, the asserted states are opposite. Note that [VTRGD](#) is defined in [Section 4.6.2, "VTRGD," on page 99](#).

[nSYS\\_RST](#) is de-asserted as defined in [Figure 4.29, "VTR Power-Up Timing"](#) and in [Table 4.17](#). [nSYS\\_RST](#) can also be asserted as a result of a [Watch-Dog Timer Forced Reset](#) as described in [Section 4.6.10, "Watch-Dog Timer Forced Reset," on page 103](#). [nSYS\\_RST](#) is asserted as soon as either the [VTR](#) or [VTR\\_1.8](#) power supplies drop below preset voltage thresholds (see [Figure 4.31 VTR Power-Down Timing on page 100](#)).

[nSYS\\_RST](#) is the reset signal for all [VTR](#)-powered blocks except for the [64.52 MHz Ring Oscillator](#) and the Embedded Controller. [nSYS\\_RST](#) also affects the [VBAT-Powered Control Interface](#) as described in [Table 22.2, "VCI Output Truth Table," on page 412](#).

### 4.6.5 nEC\_RST

[nEC\\_RST](#) is a delayed version of [nSYS\\_RST](#) that is used to reset the Embedded Controller and for [Strapping Options](#) as described in [Section 4.6.11, "Strapping Options," on page 103](#).

[nEC\\_RST](#) is de-asserted as defined in [Figure 4.29, "VTR Power-Up Timing"](#) and in [Table 4.17](#). [nEC\\_RST](#) can also be asserted as a result of a [Watch-Dog Timer Forced Reset](#) as described in [Section 4.6.10, "Watch-Dog Timer Forced Reset," on page 103](#). Like [nSYS\\_RST](#), [nEC\\_RST](#) is asserted as soon as either the [VTR](#) or [VTR\\_1.8](#) power supplies drop below preset voltage thresholds (see [Figure 4.31 VTR Power-Down Timing on page 100](#)).

### 4.6.6 1.8V Regulator

The [1.8V Regulator](#) generates the MEC5035 core power well. As illustrated in [Figure 4.28](#), the input to the [1.8V Regulator](#) is [VTR](#), the output is [VTR\\_1.8](#) (see also [Table 4.1](#)). The [1.8V Regulator](#) is not used when [VTR](#) is inactive, as described in [Section 4.6.7, "Power Mux" below](#).

The stability of the [1.8V Regulator](#) amplifier depends on an external capacitor, [VR\\_CAP](#) as described in [Table 4.1](#). The choice of capacitor can be either ceramic or low ESR tantalum. Ceramics are the recommended choice due to their superior AC performance (below 100mΩ ESR), but X5R dielectrics should be used to prevent greater than 20% capacitance variation over temperature and voltage. Low ESR tantalum capacitors will work but care should be taken because the ESR can vary 2x at low temperatures.

### 4.6.7 Power Mux

To guarantee the highest reliability and lowest possible power consumption, the [Power Mux](#) switches between the [1.8V Regulator](#) and a level-shifted [VBAT](#) voltage to produce the 1.8V internal supply for [VBAT](#)-backed logic ([VTR1.8\\_BAT](#) in [Table 4.1](#)).

[Power Mux](#) switching depends on the voltage level of the [1.8V Regulator](#) and the [VTR](#) supply. As illustrated in [Figure 4.28](#), the [Power Mux](#) selects the [1.8V Regulator](#) after the [VTR](#) and the [VTR\\_1.8](#) power supplies exceed preset voltage thresholds. The [Power Mux](#) selects the [VBAT](#) supply as soon as either the [VTR](#) or [VTR\\_1.8](#) power supplies drop below these thresholds (see [Figure 4.31 VTR Power-Down Timing on page 100](#)).



Note that the **Power Mux** only switches 1.8 volts. To guarantee minimum **VBAT** power consumption for 3.3V **VBAT** powered outputs when **VTR** is fully powered, supply switching from **VBAT** to **VTR** must be done externally.

#### 4.6.8 VCC Power Good

**VCC Power Good** is defined by the **VCC\_PWRGD** input pin (Table 4.1). **VCC\_PWRGD** is also synchronized to the **64.52 MHz Ring Oscillator** and used for the functions shown in Table 4.19.

The **VCC\_PWRGD** input must always be driven to a '1' or a '0,' even when VCC is 0 V. The minimum **VCC\_PWRGD** pulse width (high and low) is shown below in Table 4.18.

**Table 4.18 VCC\_PWRGD Input Timing**

| PARAMETERS                   | SYMBOL             | MIN | TYP | MAX | UNITS | NOTES |
|------------------------------|--------------------|-----|-----|-----|-------|-------|
| <b>VCC_PWRGD</b> Pulse Width | t <sub>VPGPW</sub> | TBD | –   | –   | ms    |       |

**Table 4.19 Functions Affected by VCC Power Good**

| NAME              | REFERENCE                                                                                     |
|-------------------|-----------------------------------------------------------------------------------------------|
| Host Clock Domain | see Section 4.4.8.4, "Host Clock Domain," on page 94.                                         |
| LPC RESET         | Section 4.6.9, "LPC RESET," on page 102.                                                      |
| nSIO_RESET        | Section , "iRESET OUT," on page 109.                                                          |
| VCC_PWRGD_BUFF    | Table 4.1, "Power, Clocks and Resets Port List," on page 75.                                  |
| VCC PWRGD         | Section , "VCC PWRGD," on page 109.                                                           |
| VCC Straps        | Section 4.6.11.1.2, "VCC Straps," on page 103 (Note: VCC Straps are not used in this design). |

#### 4.6.9 LPC RESET

**LPC RESET** (**LPC\_RST#** in Table 4.1) is defined by **VCC\_PWRGD**, **LRESET#** and **VTRGD** as illustrated in Table 4.20. **LPC RESET** only affects logic that is driven by **PCI\_CLK**.

**Table 4.20 LPC RESET Definition**

| VCC_PWRGD<br>(Note 4.32) | LRESET#<br>(Note 4.33) | VTRGD<br>(Note 4.34) | LPC RESET<br>(Note 4.35) |
|--------------------------|------------------------|----------------------|--------------------------|
| 0                        | X                      | X                    | 0                        |
| 1                        |                        | 0                    | Undefined                |
|                          | 0                      | 1                    | 0                        |
|                          | 1                      |                      | 1                        |

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**Note 4.32** this is the [Table 4.1 VCC\\_PWRGD](#) input.

**Note 4.33** this is the [Table 4.1 LRESET#](#) input. The EC can determine the state of the [LRESET#](#) input using registers in [Table 5.8, "LPC Bus Monitor Register,"](#) on page 133.

**Note 4.34** see [Section 4.6.2, "VTRGD,"](#) on page 99.

**Note 4.35** [LPC RESET](#) is the [Table 4.1 LPC\\_RST#](#) output. The trailing edge of [LPC\\_RST#](#) is synchronized to the [PCI\\_CLK](#) in [Table 4.1](#).

## 4.6.10 Watch-Dog Timer Forced Reset

A [Watch-Dog Timer Forced Reset](#) ([Figure 4.36](#)) occurs when the [WDT\\_ALRT](#) input ([Table 4.1](#)) is asserted ('1'). As shown in [Figure 4.36](#), [VTRGD](#) is de-asserted ('0') and [nSYS\\_RST](#) and [nEC\\_RST](#) are asserted ('0') when [WDT\\_ALRT](#) is asserted. The [VTRGD](#) reset time ( $t_{RST}$ ) is determined by the [32.768 KHz Crystal Oscillator](#) as shown in [Table 4.21](#). Following the [VTRGD](#) reset time, the [nSYS\\_RST](#) Delay Time ( $t_{SYNC}$ ) and the [nEC\\_RST](#) Delay Time ( $t_{STRETCH}$ ) are determined using the [64.52 MHz Ring Oscillator](#) as described in [Figure 4.29](#) and [Table 4.17](#).

Note that analog reset signal functions are not shown in [Figure 4.36](#) because it is assumed that the power supplies are fully powered and stable during a [Watch-Dog Timer Forced Reset](#).

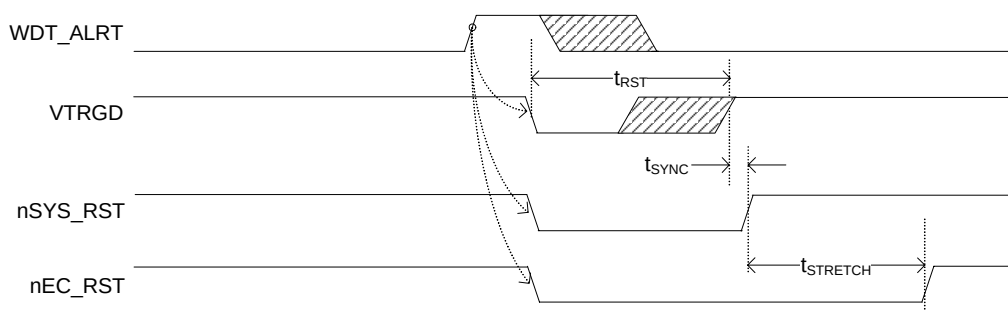


**Figure 4.36 Watch-Dog Timer Forced Reset Timing**

**Table 4.21 Watch-Dog Timer Forced Reset Timing**

| PARAMETERS                          | SYMBOL        | MIN                                                                  | TYP | MAX | UNITS                                                      |
|-------------------------------------|---------------|----------------------------------------------------------------------|-----|-----|------------------------------------------------------------|
| <a href="#">VTRGD</a> Reset Time    | $t_{RST}$     | 1                                                                    | –   | 2   | <a href="#">32.768 KHz Crystal Oscillator</a> Clock Cycles |
| <a href="#">nSYS_RST</a> Delay Time | $t_{SYNC}$    | (see <a href="#">Table 4.17, "VTR Power-Up Timing,"</a> on page 100) |     |     |                                                            |
| <a href="#">nEC_RST</a> Delay Time  | $t_{STRETCH}$ |                                                                      |     |     |                                                            |

## 4.6.11 Strapping Options

### 4.6.11.1 Definitions

#### 4.6.11.1.1 VTR STRAPS

[VTR Straps](#) are configured on pins where the direction default of the pin is 'output.' [VTR Straps](#) are sampled on the active edge of [nEC\\_RST](#).

#### 4.6.11.1.2 VCC STRAPS

[VCC Straps](#) are configured on pins where the direction default of the pin is 'output.' [VCC Straps](#) are sampled on the active edge of [VCC\\_PWRGD](#). Typically, [VCC Straps](#) are only used on devices without a VTR-powered EC.

#### 4.6.11.2 Applications

There are currently no [Strapping Options](#) required for the MEC5035.

## 4.7 Registers Interface

The [Power, Clocks and Resets](#) registers are located in two address ranges with two Base Address as indicated in [Table 4.22](#). See [Note 7.3 on page 168](#).

**Table 4.22 Power, Clocks and Resets Interface Base Address Table**

| Power, Clocks and Resets BLOCKS                        | LDN FROM<br>( <a href="#">Table 7.3 on page 168</a> ) | AHB BASE ADDRESS         |
|--------------------------------------------------------|-------------------------------------------------------|--------------------------|
| <a href="#">Power, Clock &amp; Reset (VTR PWR'ed)</a>  | 32h                                                   | <a href="#">F0_C800h</a> |
| <a href="#">Power, Clock &amp; Reset (VBAT PWR'ed)</a> | 33h                                                   | <a href="#">F0_CC00h</a> |

[Table 4.23](#) is a register summary for the [Power, Clock & Reset \(VTR PWR'ed\)](#) registers. This is a duplication of [Table 4.23 on page 104](#). Please use [Table 4.23 on page 104](#) and it links for the [Power, Clock & Reset \(VTR PWR'ed\)](#) registers.

[Table 4.24](#) is a register summary for the [Power, Clock & Reset \(VBAT PWR'ed\)](#) registers. these registers are defined in this chapter in [Table 4.24](#).

Each EC address is indicated as an SPB Offset from its AHB base address as indicated in [Table 4.22](#).

The following tables summarize the registers allocated for each Instance. The offset field in the following table is the offset from the Embedded Controller (EC) Base Address.

**Table 4.23 Power, Clocks and Resets VTR-Powered Registers Summary**

| OFFSET<br>(HEX)<br>( <a href="#">Note 4.37</a> ) | REGISTER NAME                                             | ACCESS | SIZE<br>(BITS) | PAGE<br>REFERENCE   |
|--------------------------------------------------|-----------------------------------------------------------|--------|----------------|---------------------|
| 0                                                | <a href="#">EC Clock Divider Register</a>                 | R/W    | 8              | <a href="#">106</a> |
| 4                                                | <a href="#">LPC_AHB Clock Divider Register</a>            | R/W    | 8              | <a href="#">107</a> |
| 8                                                | <a href="#">PCR Status and Control Register</a>           | R      | 8              | <a href="#">108</a> |
| C                                                | <a href="#">Clock Control Register</a>                    | R/W    | 8              | <a href="#">105</a> |
| 10                                               | <a href="#">LPC Blocks Sleep Enables Register</a>         | R/W    | 8              | <a href="#">110</a> |
| 14                                               | <a href="#">EC Blocks Sleep Enables Register</a>          | R/W    | 24             | <a href="#">111</a> |
| 18                                               | <a href="#">LPC Blocks Clock Required Status Register</a> | R      | 8              | <a href="#">113</a> |
| 1C                                               | <a href="#">EC Blocks Clock Required Status Register</a>  | R      | 24             | <a href="#">114</a> |
| 20                                               | <a href="#">OSC_ID Register</a>                           | R      | 8              | <a href="#">114</a> |
| 24                                               | Reserved                                                  | R      | 32             | —                   |

**Note 4.37** all register addresses are naturally aligned on 32-bit boundaries. Offsets for registers that are smaller than 32 bits are reserved and must not be used for any other purpose.

**Table 4.24 Power, Clocks and Resets VBAT-Powered Registers Summary**

| OFFSET<br>(HEX)<br>(Note 4.37) | REGISTER NAME                                        | ACCESS | SIZE<br>(BITS) | PAGE<br>REFERENCE   |
|--------------------------------|------------------------------------------------------|--------|----------------|---------------------|
| 0                              | <a href="#">Power-Fail and Reset Status Register</a> | R/W    | 8              | <a href="#">115</a> |
| 4                              | <a href="#">Clock Enable Register</a>                | R/W    | 8              | <a href="#">117</a> |

#### 4.7.1 Clock Control Register

**Table 4.25 Clock Control Register**

| HOST ADDRESS | N/A      |    |    | N/A   |                 |                   | HOST SIZE           |          |
|--------------|----------|----|----|-------|-----------------|-------------------|---------------------|----------|
| EC OFFSET    | 0Ch      |    |    | 8-bit |                 |                   | EC SIZE             |          |
| POWER        | VTR      |    |    | 05h   |                 |                   | nSYS_RST<br>DEFAULT |          |
| BUS          | EC SPB   |    |    |       |                 |                   |                     |          |
| BIT          | D7       | D6 | D5 | D4    | D3              | D2                | D1                  | D0       |
| HOST TYPE    | –        | –  | –  | –     | –               | –                 | –                   | –        |
| EC TYPE      | R        | R  | R  | R/W   | R/W             | R/W               | R/W                 | R        |
| BIT NAME     | Reserved |    |    | SAA   | 32KHz<br>OUTPUT | ROSC_SLP<br>_OVRD | SLEEP_<br>FLAG      | Reserved |

##### SLEEP\_FLAG

The [SLEEP\\_FLAG](#) affects the system power state as described in [Section 4.4.7.2, "EC Controlled Dynamic Power States," on page 85](#). The [SLEEP\\_FLAG](#) is R/W. EC firmware asserts [SLEEP\\_FLAG](#) ('1'), which is then typically de-asserted ('0') by hardware as described in [Section 4.4.7.5, "Wake Interface," on page 92](#).

##### ROSC\_SLP\_OVRD

The EC can prevent the start-up time of the [64.52 MHz Ring Oscillator](#) from affecting system latency by using the [64.52 MHz Ring Oscillator](#) Sleep Override bit ([ROSC\\_SLP\\_OVRD](#)). As illustrated in [Figure 4.5](#), during normal operation when [ROSC\\_SLP\\_OVRD](#) is asserted ('1' default), the [64.52 MHz Ring Oscillator](#) will always remain enabled. When [ROSC\\_SLP\\_OVRD](#) is not asserted ('0'), the [64.52 MHz Ring Oscillator](#) can be stopped as described in [Section 4.4.7.3, "64.52 MHz Ring Oscillator Control," on page 86](#).

##### 32KHz OUTPUT

The [32KHz OUTPUT](#) bit controls the MEC5035 [32KHz\\_OUT](#) signal function ([Table 4.1](#)). When [32KHz OUTPUT](#) is de-asserted '0,' the 32KHz output clock is disabled and the [32KHz\\_OUT](#) signal function is driven low. When [32KHz OUTPUT](#) is asserted, the 32KHz output clock is enabled. The [32KHz OUTPUT](#) bit is R/W and disabled by default following [VTRGD](#).

## SAA

When asserted ('1'), the Stop Auto-Adjust bit (**SAA**) disables automatic frequency correction of the **64.52 MHz Ring Oscillator**. When **SAA** is not asserted ('0') (default), the **64.52 MHz Ring Oscillator** operates normally as defined in [Section 4.4.3 on page 79](#).

Note that when **SAA** is asserted voltage and temperature variations can adversely affect the frequency of the **64.52 MHz Ring Oscillator**. To guarantee the accuracy of the **64.52 MHz Ring Oscillator** as defined in [Section 4.4.3](#), the **SAA** bit must not be asserted.

**APPLICATION NOTE:** note that the **FREQ LOCK** function as described in [Section , "FREQ LOCK," on page 110](#) is undefined when the **SAA** bit is asserted.

## 4.7.2 EC Clock Divider Register

### 4.7.2.1 Overview

The **EC Clock Divider Register** ([Table 4.27](#)) contains the **EC\_CLK\_DIV** bits that are used to program the EC clock and the EC\_AHB clock enable frequency as described in [Section , "EC\\_CLK\\_DIV," on page 107](#).

In the MEC5035, the highest available frequency that can be programmed using the **EC Clock Divider Register** is 32.25 MHz (**EC\_CLK\_DIV** = 2), the lowest is 252.9 KHz (**EC\_CLK\_DIV** = 255). As shown in [Table 4.26](#), normal operation is only guaranteed for **EC\_CLK\_DIV** values 03h - FFh. See [Section 14.3, "EC Clocking," on page 269](#) for a description of EC clocking.

**Table 4.26 EC\_CLK\_DIV PROGRAMMING BEHAVIOR**

| <b>EC_CLK_DIV</b> | <b>FREQUENCY (MHZ)</b> | <b>FLASH ACCESS ALLOWED</b> | <b>DESCRIPTION</b>                                                    |
|-------------------|------------------------|-----------------------------|-----------------------------------------------------------------------|
| 00h - 01h         | NO CHANGE              | –                           | Reserved. Writes to the <b>EC Clock Divider Register</b> are ignored. |
| 02h               | 32.25                  | NO                          | Only access to SRAM or AHB registers is possible.                     |
| 03h - FFh         | 21.5 – 0.253           | YES                         | Normal Operation.                                                     |

**Table 4.27** EC Clock Divider Register

|              |            |     |     |       |     |     |                     |     |
|--------------|------------|-----|-----|-------|-----|-----|---------------------|-----|
| HOST ADDRESS | N/A        |     |     | N/A   |     |     | HOST SIZE           |     |
| EC OFFSET    | 00h        |     |     | 8-bit |     |     | EC SIZE             |     |
| POWER        | VTR        |     |     | 08h   |     |     | nSYS_RST<br>DEFAULT |     |
| BUS          | EC SPB     |     |     |       |     |     |                     |     |
| BIT          | D7         | D6  | D5  | D4    | D3  | D2  | D1                  | D0  |
| HOST TYPE    | –          | –   | –   | –     | –   | –   | –                   | –   |
| EC TYPE      | R/W        | R/W | R/W | R/W   | R/W | R/W | R/W                 | R/W |
| BIT NAME     | EC_CLK_DIV |     |     |       |     |     |                     |     |

**EC\_CLK\_DIV**

The [EC\\_CLK\\_DIV](#) bits contain the binary encoded divider that determines the EC clock and EC\_AHB clock enable frequency. Valid [EC\\_CLK\\_DIV](#) values are 02h - FFh. The [EC\\_CLK\\_DIV](#) default is 08h (8 MHz). Writing a '00h' or a '01h' to the [EC Clock Divider Register](#) has no affect.

When the [EC\\_CLK\\_DIV](#) is greater than '01h,' the EC clock and EC\_AHB clock enable frequency (F) is calculated using the equation in [Figure 4.38](#), where MCLK is the undivided output of the [64.52 MHz Ring Oscillator](#) and DIV is the [EC\\_CLK\\_DIV](#) value programmed into the [EC Clock Divider Register](#).

$$F = \frac{MCLK}{DIV}$$

**Figure 4.38** [EC\\_CLK\\_DIV](#) Equation

**APPLICATION NOTE:** to support EC traffic to the LPC Subsystem, the EC\_AHB clock frequency must be equal to or less than the LPC\_AHB clock frequency.

**APPLICATION NOTE:** the JTAG clock can't be higher than 1/2 the EC clock as defined by the [EC Clock Divider Register](#).

## 4.7.3 LPC\_AHB Clock Divider Register

### 4.7.3.1 Overview

The [LPC\\_AHB Clock Divider Register](#) ([Table 4.29](#)) contains the [LPC\\_AHB\\_CLK\\_DIV](#) bits that are used to program the LPC\_AHB clock enable frequency as described in [Section , "LPC\\_AHB\\_CLK\\_DIV," on page 108](#).

In the MEC5035, the highest available frequency that can be programmed using the [LPC\\_AHB Clock Divider Register](#) is 64.52 MHz ([LPC\\_AHB\\_CLK\\_DIV](#) = 1), the lowest is 4.3 MHz ([LPC\\_AHB\\_CLK\\_DIV](#) = Fh). As shown in [Table 4.28](#), normal operation is only guaranteed for [LPC\\_AHB\\_CLK\\_DIV](#) values 01h - 0Fh.

**Table 4.28 LPC\_AHB\_CLK\_DIV PROGRAMMING BEHAVIOR**

| LPC_AHB_CLK_DIV | FREQUENCY (MHZ) | DESCRIPTION                                                                         |
|-----------------|-----------------|-------------------------------------------------------------------------------------|
| 00h             | NO CHANGE       | Reserved. Writes to the <a href="#">LPC_AHB Clock Divider Register</a> are ignored. |
| 01h - 0Fh       | 64.52 – 4.30    | Normal Operation.                                                                   |

**Table 4.29 LPC\_AHB Clock Divider Register**

|              |          |    |    |    |                 |     |     |                     |  |
|--------------|----------|----|----|----|-----------------|-----|-----|---------------------|--|
| HOST ADDRESS | N/A      |    |    |    | N/A             |     |     | HOST SIZE           |  |
| EC OFFSET    | 04h      |    |    |    | 8-bit           |     |     | EC SIZE             |  |
| POWER        | VTR      |    |    |    | 01h             |     |     | nSYS_RST<br>DEFAULT |  |
| BUS          | EC SPB   |    |    |    |                 |     |     |                     |  |
| BIT          | D7       | D6 | D5 | D4 | D3              | D2  | D1  | D0                  |  |
| HOST TYPE    | –        | –  | –  | –  | –               | –   | –   | –                   |  |
| EC TYPE      | R        | R  | R  | R  | R/W             | R/W | R/W | R/W                 |  |
| BIT NAME     | Reserved |    |    |    | LPC_AHB_CLK_DIV |     |     |                     |  |

#### LPC\_AHB\_CLK\_DIV

The [LPC\\_AHB\\_CLK\\_DIV](#) is the binary encoded divider that determines the LPC\_AHB clock enable frequency. Valid [LPC\\_AHB\\_CLK\\_DIV](#) values are 01h - 0Fh. The [LPC\\_AHB\\_CLK\\_DIV](#) default is 01h. Writing a '00h' to the [LPC\\_AHB Clock Divider Register](#) has no affect.

When the [LPC\\_AHB\\_CLK\\_DIV](#) is greater than '00h,' the LPC\_AHB clock enable frequency (F) is calculated using the same equation as for the [EC\\_CLK\\_DIV](#) (Figure 4.38), where MCLK is the undivided output of the [64.52 MHz Ring Oscillator](#) and DIV is the [LPC\\_AHB\\_CLK\\_DIV](#) value. When the [LPC\\_AHB\\_CLK\\_DIV](#) is '01h,' the LPC\_AHB clock frequency (F) is the undivided output of the [64.52 MHz Ring Oscillator](#).

**APPLICATION NOTE:** to support EC traffic to the LPC Subsystem, the EC\_AHB clock frequency must be equal to or less than the LPC\_AHB clock frequency.

#### 4.7.4 PCR Status and Control Register

The [Power, Clocks and Resets](#) Status and Control Register contains the [VCC PWRGD](#) and [WAKE](#) status bits and other controls as illustrated in [Table 4.30](#).



Table 4.30 PCR Status and Control Register

| HOST ADDRESS | N/A      |      |           |            | N/A        |          | HOST SIZE        |          |
|--------------|----------|------|-----------|------------|------------|----------|------------------|----------|
| EC OFFSET    | 08h      |      |           |            | 8-bit      |          | EC SIZE          |          |
| POWER        | VTR      |      |           |            | 00XX_XX1Xb |          | nSYS_RST DEFAULT |          |
| BUS          | EC SPB   |      |           |            |            |          |                  |          |
| BIT          | D7       | D6   | D5        | D4         | D3         | D2       | D1               | D0       |
| HOST TYPE    | –        | –    | –         | –          | –          | –        | –                | –        |
| EC TYPE      | R        | R    | R         | R/W        | R          | R        | R                | R        |
| BIT NAME     | Reserved | WAKE | FREQ LOCK | iRESET OUT | Reserved   | Reserved | VCC PWRGD        | Reserved |

**VCC PWRGD**

The **VCC PWRGD** bit reflects the state of the synchronized **VCC\_PWRGD** input pin (see [Section 4.6.8, "VCC Power Good,"](#) on page 102). The **VCC PWRGD** pin can generate an either-edge interrupt as described in the note associated with the **VCC PWRGD** signal in [Section 17.4, "Detailed Pin Muxing assignments,"](#) on page 367.

**iRESET OUT**

The **iRESET OUT** bit is used by firmware to control the **nSIO\_RESET** signal function ([Table 4.1](#)). **nSIO\_RESET** is also the source for the **nRESET\_OUT** signal function ([Table 3.9, "MISC Interface,"](#) on page 44). Firmware can program the state of **iRESET OUT** except when the **VCC PWRGD** bit is not asserted ('0'), in which case **iRESET OUT** is 'don't care' and **nSIO\_RESET** is asserted ('0') ([Table 4.31](#)). In all other cases, the **nSIO\_RESET** signal function is always the inverse of the **iRESET OUT** bit.

**APPLICATION NOTE:** it should be noted that when the **iRESET OUT** bit is asserted ('1') the internal **nSIO\_RESET** is asserted even if the **nRESET\_OUT** pin is configured as an alternate function.

Table 4.31 iRESET OUT BIT BEHAVIOR

| VCC PWRGD | iRESET OUT | nSIO_RESET | RESET STATE (INTERNAL/EXTERNAL) | DESCRIPTION                                                                                                     |
|-----------|------------|------------|---------------------------------|-----------------------------------------------------------------------------------------------------------------|
| 0         | X          | 0          | ASSERTED                        | The <b>iRESET OUT</b> bit does not affect the state of <b>nSIO_RESET</b> when <b>VCC PWRGD</b> is not asserted. |
| 1         | 1          | 1          | NOT ASSERTED                    | The <b>iRESET OUT</b> bit can only be written by firmware when <b>VCC PWRGD</b> is asserted.                    |
|           | 0          |            |                                 |                                                                                                                 |



## FREQ LOCK

**FREQ LOCK** is asserted ('1') when the [32.768 KHz Crystal Oscillator](#) is stable and the accuracy of the [64.52 MHz Ring Oscillator](#) is within the tightest tolerance described in [Table 4.3, "64.52 MHz Ring Oscillator Timing Parameters," on page 79](#).

## WAKE

The **WAKE** bit reflects the state of the **WAKE** input to the [Power, Clocks and Resets](#) block as defined in [Table 4.1, "Power, Clocks and Resets Port List," on page 75](#). When **WAKE** is asserted ('1'), a wake event is pending; when **WAKE** is not asserted ('0'), there are no active wake events or interrupts. The **WAKE** bit is used by the EC as defined in [Section 4.4.7.4.3, "EC Controlled Sleep State Activation," on page 89](#).

## 4.7.5 Block Sleep Enable Registers

The [Block Sleep Enables](#) identified in the [Block Sleep Enable Registers](#) are described below in [Section 4.7.5.1, "LPC Blocks Sleep Enables Register"](#) and [Section 4.7.5.2, "EC Blocks Sleep Enables Register"](#). The behavior of the [Block Sleep Enables](#) is described in [Section 4.4.7.4.4, "Block Sleep Enables," on page 91](#).

### 4.7.5.1 LPC Blocks Sleep Enables Register

**Table 4.32 LPC Blocks Sleep Enables Register**

| HOST ADDRESS | N/A      |    |    |    | N/A    |      |     | HOST SIZE           |  |
|--------------|----------|----|----|----|--------|------|-----|---------------------|--|
| EC OFFSET    | 10h      |    |    |    | 8-bit  |      |     | EC SIZE             |  |
| POWER        | VTR      |    |    |    | 00h    |      |     | nSYS_RST<br>DEFAULT |  |
| BUS          | EC SPB   |    |    |    |        |      |     |                     |  |
| BIT          | D7       | D6 | D5 | D4 | D3     | D2   | D1  | D0                  |  |
| HOST TYPE    | –        | –  | –  | –  | –      | –    | –   | –                   |  |
| EC TYPE      | R        | R  | R  | R  | R      | R/W  | R/W | R/W                 |  |
| BIT NAME     | Reserved |    |    |    | LEGACY | UART | LPC | Reserved            |  |

**Note 4.39** All writes to the [LPC Blocks Sleep Enables Register](#) should clear bit[0] to '0'.

**Table 4.33 LPC Blocks Sleep Enables Register Bit Names**

| BIT NAME | BLOCK NAME (Note 4.40) | BLOCK CROSS REFERENCE                                                 |
|----------|------------------------|-----------------------------------------------------------------------|
| LPC      | LPC Interface          | <a href="#">Chapter 5, "Host Interface," on page 120</a>              |
| UART     | 16C550A UART           | <a href="#">Chapter 12, "Two Pin Serial Port (UART)," on page 224</a> |
| LEGACY   | Legacy Port Functions  | <a href="#">Section 10.10, "Legacy Support," on page 201</a>          |
| Reserved | —                      | —                                                                     |

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**Note 4.40** the blocks listed in this table are referenced in [Table 4.6, "Block Clocking and Reset Requirements Summary,"](#) on page 83.

## 4.7.5.2 EC Blocks Sleep Enables Register

Table 4.34 EC Blocks Sleep Enables Register

| HOST ADDRESS | N/A    |       |       |       | N/A      |       |       | HOST SIZE           |  |
|--------------|--------|-------|-------|-------|----------|-------|-------|---------------------|--|
| EC OFFSET    | 14h    |       |       |       | 24-bit   |       |       | EC SIZE             |  |
| POWER        | VTR    |       |       |       | 00_0000h |       |       | nSYS_RST<br>DEFAULT |  |
| BUS          | EC SPB |       |       |       |          |       |       |                     |  |
| BIT          | D23    | D22   | D21   | D20   | D19      | D18   | D17   | D16                 |  |
| HOST TYPE    | –      | –     | –     | –     | –        | –     | –     | –                   |  |
| EC TYPE      | R/W    | R/W   | R/W   | R/W   | R/W      | R/W   | R/W   | R/W                 |  |
| BIT NAME     | FLASH  | SPI_P | SMB2  | SMB1  | PWM4     | PWM3  | PWM2  | PWM1                |  |
| BIT          | D15    | D14   | D13   | D12   | D11      | D10   | D9    | D8                  |  |
| HOST TYPE    | –      | –     | –     | –     | –        | –     | –     | –                   |  |
| EC TYPE      | R/W    | R/W   | R/W   | R/W   | R/W      | R/W   | R/W   | R/W                 |  |
| BIT NAME     | PS2_3  | PS2_2 | PS2_1 | MBCL4 | MBCL3    | MBCL2 | MBCL1 | TACH3               |  |
| BIT          | D7     | D6    | D5    | D4    | D3       | D2    | D1    | D0                  |  |
| HOST TYPE    | –      | –     | –     | –     | –        | –     | –     | –                   |  |
| EC TYPE      | R/W    | R/W   | R/W   | R/W   | R/W      | R/W   | R/W   | R/W                 |  |
| BIT NAME     | TACH2  | TACH1 | MSDP  | RC_ID | C/T3     | C/T2  | C/T1  | C/T0                |  |

Table 4.35 EC Blocks Sleep Enables Register Bit Names

| BIT NAME | BLOCK NAME (Note 4.40) | BLOCK CROSS REFERENCE                                             |
|----------|------------------------|-------------------------------------------------------------------|
| C/T0     | 16-Bit Counter/Timer 0 | <a href="#">Chapter 26, "16-Bit Timer Interface," on page 457</a> |
| C/T1     | 16-Bit Counter/Timer 1 | <a href="#">Chapter 26, "16-Bit Timer Interface," on page 457</a> |
| C/T2     | 16-Bit Counter/Timer 2 | <a href="#">Chapter 26, "16-Bit Timer Interface," on page 457</a> |
| C/T3     | 16-Bit Counter/Timer 3 | <a href="#">Chapter 26, "16-Bit Timer Interface," on page 457</a> |

**Table 4.35 EC Blocks Sleep Enables Register Bit Names (continued)**

| <b>BIT NAME</b> | <b>BLOCK NAME (Note 4.40)</b> | <b>BLOCK CROSS REFERENCE</b>                                                    |
|-----------------|-------------------------------|---------------------------------------------------------------------------------|
| RC_ID           | RC ID Interface               | Chapter 25, "RC Identification Detection (RC_ID)," on page 446                  |
| MSDP            | MCU Serial Debug Port         | Chapter 18, "Serial Debug Port," on page 386                                    |
| TACH1           | Tachometer 1                  | Chapter 29, "TACH Monitor," on page 486                                         |
| TACH2           | Tachometer 2                  | Chapter 29, "TACH Monitor," on page 486                                         |
| TACH3           | Tachometer 3                  | Chapter 29, "TACH Monitor," on page 486                                         |
| MBCL1           | Master BC Link 1              | Chapter 32, "SMSC BC-Link Master," on page 510                                  |
| MBCL2           | Master BC Link 2              | Chapter 32, "SMSC BC-Link Master," on page 510                                  |
| MBCL3           | Master BC Link 3              | Chapter 32, "SMSC BC-Link Master," on page 510                                  |
| MBCL4           | Master BC Link 4              | Chapter 32, "SMSC BC-Link Master," on page 510                                  |
| PS2_1           | PS/2 Interface 1              | Chapter 30, "PS/2 Device Interface," on page 496                                |
| PS2_2           | PS/2 Interface 2              | Chapter 30, "PS/2 Device Interface," on page 496                                |
| PS2_3           | PS/2 Interface 3              | Chapter 30, "PS/2 Device Interface," on page 496                                |
| PWM1            | PWM 1                         | Chapter 28, "PWM Controller," on page 478                                       |
| PWM2            | PWM 2                         | Chapter 28, "PWM Controller," on page 478                                       |
| PWM3            | PWM 3                         | Chapter 28, "PWM Controller," on page 478                                       |
| PWM4            | PWM 4                         | Chapter 28, "PWM Controller," on page 478                                       |
| SMB1            | SMBus 1                       | Chapter 31, "SMB Device Interface," on page 506                                 |
| SMB2            | SMBus 2                       | Chapter 31, "SMB Device Interface," on page 506                                 |
| SPI_P           | SPI Peripheral Interface      | Chapter 24, "General Purpose Serial Peripheral Interface (GP-SPI)," on page 419 |
| FLASH           | Flash Interface               | Chapter 15, "Embedded Flash Subsystem," on page 276                             |
| Reserved        | —                             | —                                                                               |

#### 4.7.6 Clock Required Status Registers

The [Clock Required Status Registers](#) indicates the core clock status per block as defined in [Section 4.4.5, "Generic Block Clocking Model,"](#) on page 80 and enumerated in the [Block Clocking and Reset Requirements Summary](#). Like the [Block Sleep Enable Registers](#), there are two [Clock Required Status Registers](#): the [LPC Blocks Clock Required Status Register](#) and the [EC Blocks Clock Required Status Register](#).

**Product Customer Specification-ODM**

When a bit in the [Clock Required Status Registers](#) is asserted ('1'), the block is enabled and requires that the [64.52 MHz Ring Oscillator](#) remain running as defined in [Section 4.4.7.4.2, "EC Power State Controls,"](#) on page 88.

When a bit in the [Clock Required Status Registers](#) is not asserted ('0'), the block is either not enabled as defined in the [Generic Block Clocking Model](#), or has been commanded to sleep and no longer requires the [64.52 MHz Ring Oscillator](#).

**4.7.6.1 LPC Blocks Clock Required Status Register****Table 4.36** [LPC Blocks Clock Required Status Register](#)

| HOST ADDRESS | N/A      |    |    |    | N/A    |      |     | HOST SIZE           |  |
|--------------|----------|----|----|----|--------|------|-----|---------------------|--|
| EC OFFSET    | 18h      |    |    |    | 8-bit  |      |     | EC SIZE             |  |
| POWER        | VTR      |    |    |    | 0Xh    |      |     | nSYS_RST<br>DEFAULT |  |
| BUS          | EC SPB   |    |    |    |        |      |     |                     |  |
| BIT          | D7       | D6 | D5 | D4 | D3     | D2   | D1  | D0                  |  |
| HOST TYPE    | –        | –  | –  | –  | –      | –    | –   | –                   |  |
| EC TYPE      | R        | R  | R  | R  | R      | R    | R   | R                   |  |
| BIT NAME     | Reserved |    |    |    | LEGACY | UART | LPC | Reserved            |  |

**Note 4.41** Bit[0] in the [LPC Blocks Clock Required Status Register](#) may change state.

#### 4.7.6.2 EC Blocks Clock Required Status Register

**Table 4.37** EC Blocks Clock Required Status Register

| HOST ADDRESS | N/A    |       |       |       | N/A      |       |       | HOST SIZE           |  |
|--------------|--------|-------|-------|-------|----------|-------|-------|---------------------|--|
| EC OFFSET    | 1Ch    |       |       |       | 24-bit   |       |       | EC SIZE             |  |
| POWER        | VTR    |       |       |       | XX_XXXXh |       |       | nSYS_RST<br>DEFAULT |  |
| BUS          | EC SPB |       |       |       |          |       |       |                     |  |
| BIT          | D23    | D22   | D21   | D20   | D19      | D18   | D17   | D16                 |  |
| HOST TYPE    | –      | –     | –     | –     | –        | –     | –     | –                   |  |
| EC TYPE      | R      | R     | R     | R     | R        | R     | R     | R                   |  |
| BIT NAME     | FLASH  | SPI_P | SMB2  | SMB1  | PWM4     | PWM3  | PWM2  | PWM1                |  |
| BIT          | D15    | D14   | D13   | D12   | D11      | D10   | D9    | D8                  |  |
| HOST TYPE    | –      | –     | –     | –     | –        | –     | –     | –                   |  |
| EC TYPE      | R      | R     | R     | R     | R        | R     | R     | R                   |  |
| BIT NAME     | PS2_3  | PS2_2 | PS2_1 | MBCL4 | MBCL3    | MBCL2 | MBCL1 | TACH3               |  |
| BIT          | D7     | D6    | D5    | D4    | D3       | D2    | D1    | D0                  |  |
| HOST TYPE    | –      | –     | –     | –     | –        | –     | –     | –                   |  |
| EC TYPE      | R      | R     | R     | R     | R        | R     | R     | R                   |  |
| BIT NAME     | TACH2  | TACH1 | MSDP  | RC_ID | C/T3     | C/T2  | C/T1  | C/T0                |  |

#### 4.7.7 OSC\_ID Register

The [OSC\\_ID Register](#) (Table 4.38) contains the [FOUNDRY](#), [FOUNDRY](#) and [SHRINK](#) identification codes for the [64.52 MHz Ring Oscillator](#).



Table 4.38 OSC\_ID Register

| HOST ADDRESS | N/A     |    |    |    | N/A     |    |        | HOST SIZE         |  |
|--------------|---------|----|----|----|---------|----|--------|-------------------|--|
| EC OFFSET    | 20h     |    |    |    | 8-bit   |    |        | EC SIZE           |  |
| POWER        | VTR     |    |    |    | XXh     |    |        | HARDWIRED DEFAULT |  |
| BUS          | EC SPB  |    |    |    |         |    |        |                   |  |
| BIT          | D7      | D6 | D5 | D4 | D3      | D2 | D1     | D0                |  |
| HOST TYPE    | –       | –  | –  | –  | –       | –  | –      | –                 |  |
| EC TYPE      | R       | R  | R  | R  | R       | R  | R      | R                 |  |
| BIT NAME     | FOUNDRY |    |    |    | FOUNDRY |    | SHRINK |                   |  |

**SHRINK**

The 2-bit [SHRINK](#) register represents the hard-coded [64.52 MHz Ring Oscillator](#) shrink factor.

**FOUNDRY**

The 2-bit [FOUNDRY](#) register represents the hard-coded [64.52 MHz Ring Oscillator](#) foundry code.

**BLOCK\_REVISION**

The 4-bit [FOUNDRY](#) register represents the hard-coded [64.52 MHz Ring Oscillator](#) block revision number.

## 4.8 VBAT Powered Registers

### 4.8.1 Power-Fail and Reset Status Register

#### 4.8.1.1 Overview

The [Power-Fail and Reset Status Register](#) ([Table 4.39](#)) collects and retains the [VBAT RST](#), [FLASH](#) and [WDT](#) event status when [VTR](#) is unpowered. Asserted events can cause interrupts as described in [Section 4.9, "Interrupt Interface," on page 117](#).

**Table 4.39 Power-Fail and Reset Status Register**

| HOST ADDRESS | N/A         |       |      | N/A      |    |    | HOST SIZE           |    |
|--------------|-------------|-------|------|----------|----|----|---------------------|----|
| EC OFFSET    | 00h         |       |      | 8-bit    |    |    | EC SIZE             |    |
| POWER        | VBAT        |       |      | 1XXX000b |    |    | VBAT_POR<br>DEFAULT |    |
| BUS          | EC SPB      |       |      |          |    |    |                     |    |
| BIT          | D7          | D6    | D5   | D4       | D3 | D2 | D1                  | D0 |
| HOST TYPE    | –           | –     | –    | –        | –  | –  | –                   | –  |
| EC TYPE      | R/WC        | R/WC  | R/WC | R/WC     | R  | R  | R                   | R  |
| BIT NAME     | VBAT<br>RST | FLASH | WDT  | Reserved |    |    |                     |    |

#### WDT

The **WDT** bit is asserted ('1') following a [Watch-Dog Timer Forced Reset](#) as described in [Section 4.6.10, "Watch-Dog Timer Forced Reset," on page 103](#). To clear the **WDT** bit EC firmware must write a '1' to this bit; writing a '0' to the **WDT** bit has no affect.

#### FLASH

The **FLASH** bit is set to '1' by hardware when **FLASH\_PGM** in [Table 4.1, "Power, Clocks and Resets Port List," on page 75](#) is asserted. **FLASH\_PGM** is asserted when the [Embedded Flash Subsystem](#) is placed in [Program Mode](#) or [Erase Mode](#). To clear the **FLASH** bit EC firmware must write a '1' to this bit; writing a '0' to the **FLASH** bit has no affect.

#### VBAT RST

The **VBAT RST** bit is set to '1' by hardware when a **VBAT\_POR** is detected. This is the register default value. To clear **VBAT RST** EC firmware must write a '1' to this bit; writing a '0' to **VBAT RST** has no affect.

## 4.8.2 Clock Enable Register

Table 4.40 Clock Enable Register

|              |          |    |    |       |    |    |                  |       |
|--------------|----------|----|----|-------|----|----|------------------|-------|
| HOST ADDRESS | N/A      |    |    | N/A   |    |    | HOST SIZE        |       |
| EC OFFSET    | 04h      |    |    | 8-bit |    |    | EC SIZE          |       |
| POWER        | VBAT     |    |    | 00h   |    |    | VBAT_POR DEFAULT |       |
|              |          |    |    | N/A   |    |    | nSYS_RST DEFAULT |       |
| BUS          | EC SPB   |    |    |       |    |    |                  |       |
| BIT          | D7       | D6 | D5 | D4    | D3 | D2 | D1               | D0    |
| HOST TYPE    | –        | –  | –  | –     | –  | –  | –                | –     |
| EC TYPE      | R        | R  | R  | R     | R  | R  | R/W              | R/W   |
| BIT NAME     | Reserved |    |    |       |    |    | 32K_EN           | XOSEL |

### XOSEL

When the External Oscillator Select bit (XOSEL) is asserted ('1'), the 32.768 KHz Crystal Oscillator is driven by a single-ended 32.768 KHz clock source connected to the XTAL2 pin.

When XOSEL is not asserted ('0') (default), the 32.768 KHz Crystal Oscillator requires a 32.768 KHz parallel resonant crystal connected between the XTAL1 and XTAL2 pins. See also Table 4.15, "Typical MEC5035 Clocks vs. ACPI Power States," on page 96.

**APPLICATION NOTE:** the XOSEL bit should be correctly configured by firmware before the 32K\_EN bit is asserted.

### 32K\_EN

The 32K\_EN bit controls the 32.768 KHz Crystal Oscillator as defined in Table 4.41. The 32K\_EN bit is de-asserted ('0') by default on a VBAT\_POR (see also Section 4.6.3 on page 100). The 32K\_EN bit is unaffected by nSYS\_RST.

Table 4.41 32K\_EN Bit

| 32K_EN | 32.768 KHz Crystal Oscillator | DESCRIPTION                                                        |
|--------|-------------------------------|--------------------------------------------------------------------|
| 0      | OFF                           | VBAT_POR default.                                                  |
| 1      | ON                            | The 32.768 KHz Crystal Oscillator can only be enabled by firmware. |

## 4.9 Interrupt Interface

The Power, Clocks and Resets Interrupt Interface inputs include the VBAT\_RST, FLASH and WDT status bits in the Power-Fail and Reset Status Register. The Interrupt Interface output is PCR\_INT in Table 4.1, "Power, Clocks and Resets Port List," on page 75. The corresponding bit in the EC Interrupt Aggregator is bit PFR in IRQ31 Source Register.



Whenever any [Interrupt Interface](#) input is asserted, [PCR\\_INT](#) is asserted; when all [Interrupt Interface](#) inputs are not asserted, [PCR\\_INT](#) is not asserted. [PCR\\_INT](#) may be masked as described in [Chapter 16, "EC Interrupt Aggregator,"](#) on page 304.

## 4.10 [Power, Clocks and Resets](#) Revision History

This revision history shows the changes made to this chapter.

**Table 4.42 [Power, Clocks and Resets](#) Chapter Revision History**

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History,"</a> on page 539. |              |            |                                                                                                                                                                                                  |                                                                                                                                                                                                               |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE       | SECTION/FIGURE/ENTRY                                                                                                                                                                             | CORRECTION                                                                                                                                                                                                    |
| 1.                                                                                                                                                                                                                                          | 0.4          | 5/10/2007  | <a href="#">Section 4.6.8, "VCC Power Good,"</a> on page 102                                                                                                                                     | Removed: " <a href="#">VCC_PWRGD</a> input levels are $V_{IL} = V_{SS} \pm 400$ mV and $V_{IH} = V_{TR} \pm 400$ mV."                                                                                         |
| 2.                                                                                                                                                                                                                                          | 0.5          | 6/05/2007  | All<br><br><a href="#">Section 4.4.9.2, "Synchronization,"</a> on page 95<br><br><a href="#">Section 4.6.4, "nSYS_RST,"</a> on page 101<br><a href="#">Section 4.6.5, "nEC_RST,"</a> on page 101 | Replace <a href="#">ARC_XEN</a> signal with <a href="#">ARC_CLK_DISABLE</a><br><br>Removed condition "when the <a href="#">WDT_ALRT</a> signal is asserted."<br><br>Corrected "assertion/de-assertion" sense. |
| 3.                                                                                                                                                                                                                                          | 0.6          | 07/30/2008 | <a href="#">Section 4.4.7.2, "EC Controlled Dynamic Power States,"</a> on page 85                                                                                                                | Added xref to <a href="#">Section 33.3, "Power Consumption,"</a> on page 522.                                                                                                                                 |
| 4.                                                                                                                                                                                                                                          |              |            |                                                                                                                                                                                                  |                                                                                                                                                                                                               |



## Chapter 5 Host Interface

### 5.1 General Description

#### 5.1.1 Overview

The host processor communicates with the MEC5035 via the [LPC Bus Interface](#). The host processor communicates through a series of read/write registers in the MEC5035. Register access is accomplished through programmed I/O or DMA LPC transfer cycles. All I/O transfer cycles are 8 bits wide. DMA transfer cycles can be 16-bit or 8-bit wide.

The Logical Devices physically located in the MEC5035 are identified in [Table 7.2, "Host Logical Devices on MEC5035," on page 167](#) and [Table 6.1, "Basechip Logical Devices," on page 140](#). The base addresses of logical devices with registers located in LPC I/O space, including the Keyboard Controller, can be moved via the configuration registers located in the LPC Interface Configuration Register Space.

All configuration register access for the MEC5035 basechip and associated companions are accessed indirectly through the LPC I/O Configuration Register Port (IOCR-Port.) The default I/O address is 2Eh and 2Fh, but the IOCR-Port can be relocated by either the host or the EC. Detailed description of the MEC5035 Configuration Space is in [Chapter 6, "Logical Device Configuration," on page 140](#).

All LPC transactions that are claimed by the MEC5035 are mapped by the LPC interface to an address in the MEC5035's AHB address space. All these addresses can also be accessed by the Embedded Controller in the MEC5035.

**Table 5.1 Targets of LBC cycles claimed by the MEC5035**

| TARGET                             | ACRONYM          | DESCRIPTIONS                                                                                           | LPC TYPES           |
|------------------------------------|------------------|--------------------------------------------------------------------------------------------------------|---------------------|
| LPC IO Configuration Register Port | <b>IOCR-Port</b> | Standard LPC 2Eh/2Fh Port which permits BIOS access. This port can be relocated by the ARC.            | I/O                 |
| Basechip Logical Devices           | <b>BLD</b>       | Targets physically located in the MEC5035.<br>The Keyboard Controller Interface uses a Port at 60h/64h | DMA & I/O           |
| Basechip Configuration Register    | <b>BCR</b>       | 256 byte space per Logical Device accessed by BIOS through the IOCR-Port.                              | I/O through CR-Port |

#### 5.1.2 Block Diagram

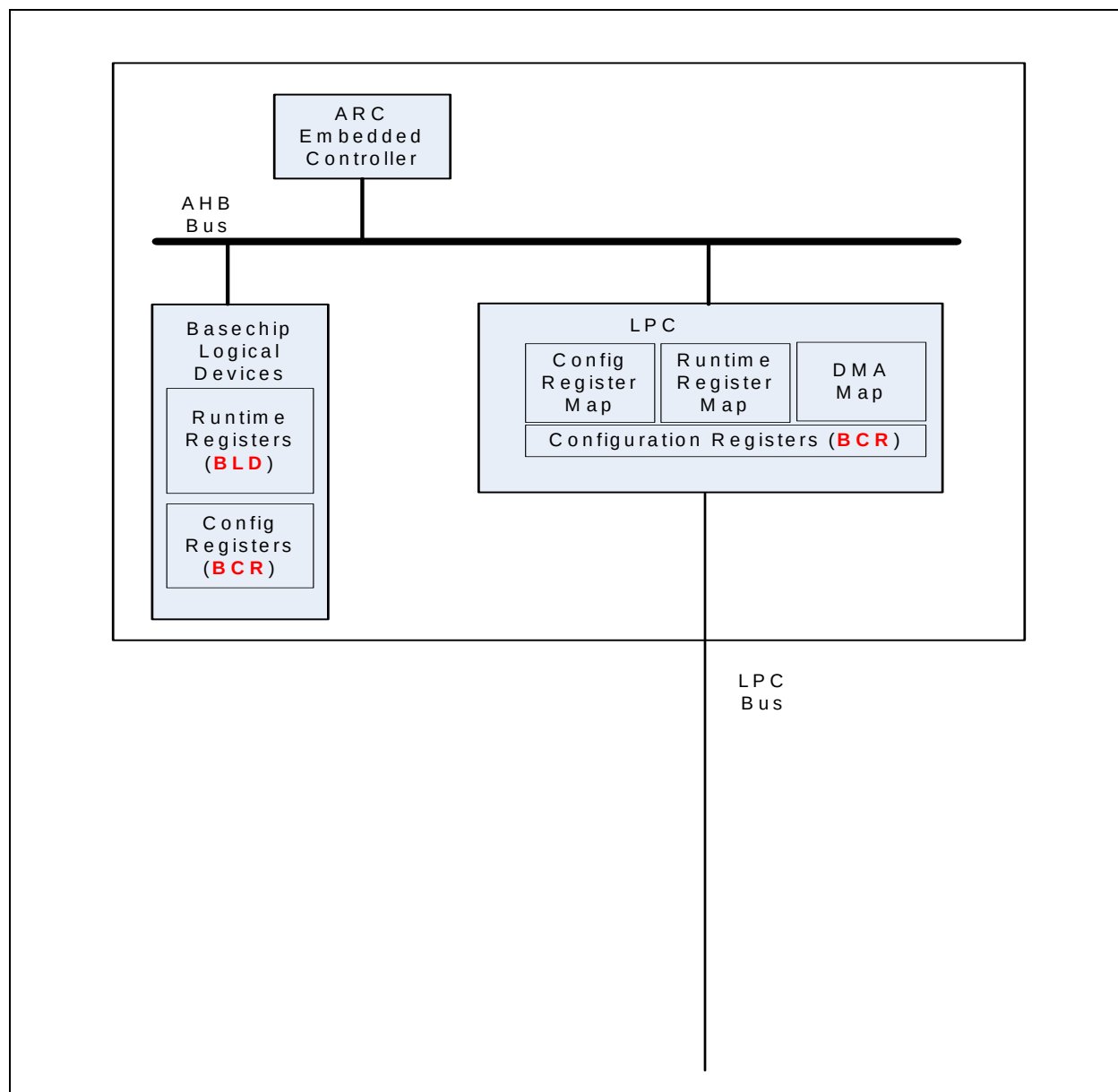


Figure 5.1 LPC Interface in MEC5035

## 5.2 Power, Clocks and Resets

### 5.2.1 Power Domain

This block is powered by VTR. Although the block is not powered by VCC, the block is also controlled by VCC\_PWRGD. When VCC\_PWRGD is de-asserted, the LPC bus pins are placed in the same state they assume when VTR is off. LAD[3:0] and SERIRQ are tri-stated, LDRQ# is pulled high, CLKRUN# is unpowered and LFRAME#, LRESET# and LPCPD# are gated high; see [Table 5.2, "LPC Bus Pin Behavior on Reset," on page 124](#). The LPC block is also placed in a minimal power state.

See [Section 4.5, "Power Configuration," on page 96](#) for details on power domains.

## 5.2.2 Clocks

[LPC Logical Device Configuration Registers](#) and [LPC Logical Device EC-only Registers](#) in this block are clocked by the [LPC Bus Clock](#). The LPC interface itself is clocked by the [PCI\\_CLK](#) clock input.

The clock rate of the [LPC Bus Clock](#) is set by the [EC Clock Divider Register](#) described on [page 106](#). In normal operation the [EC Clock Divider Register](#) should be set to 01h, so that the LPC bus runs at the 64.52MHz [MCLK](#) rate.

See [Section 4.4, "Clock Generator," on page 77](#) for details on clocks.

## 5.2.3 Resets

This block is affected by [nSYS\\_RST](#), [VCC Power Good](#) and [LPC RESET](#).

The assertion of [nSYS\\_RST](#) resets the LPC state machine and all registers to their default values. The AHB Master state machine is also reset to its default value.

[VCC Power Good](#) going low resets the LPC state machine. The AHB Master interface that is part of the Host Interface will go to its idle state. Any transaction that is active on the AHB Master when the VCC POR occurs will be terminated in such a way that the AHB subsystem will not be locked up.

The assertion of [LPC RESET#](#) resets the LPC state machine but does not otherwise affect register values. An interrupt to the EC will be generated on either edge of [LRESET#](#). See [Section 5.5, "Host Interrupts to EC," on page 125](#)

See [Section 4.6, "Reset Interface," on page 99](#) for details on reset.

## 5.3 LPC Logical Device

The LPC Logical Device structure is illustrated in [Figure 5.1, "LPC Interface in MEC5035"](#).

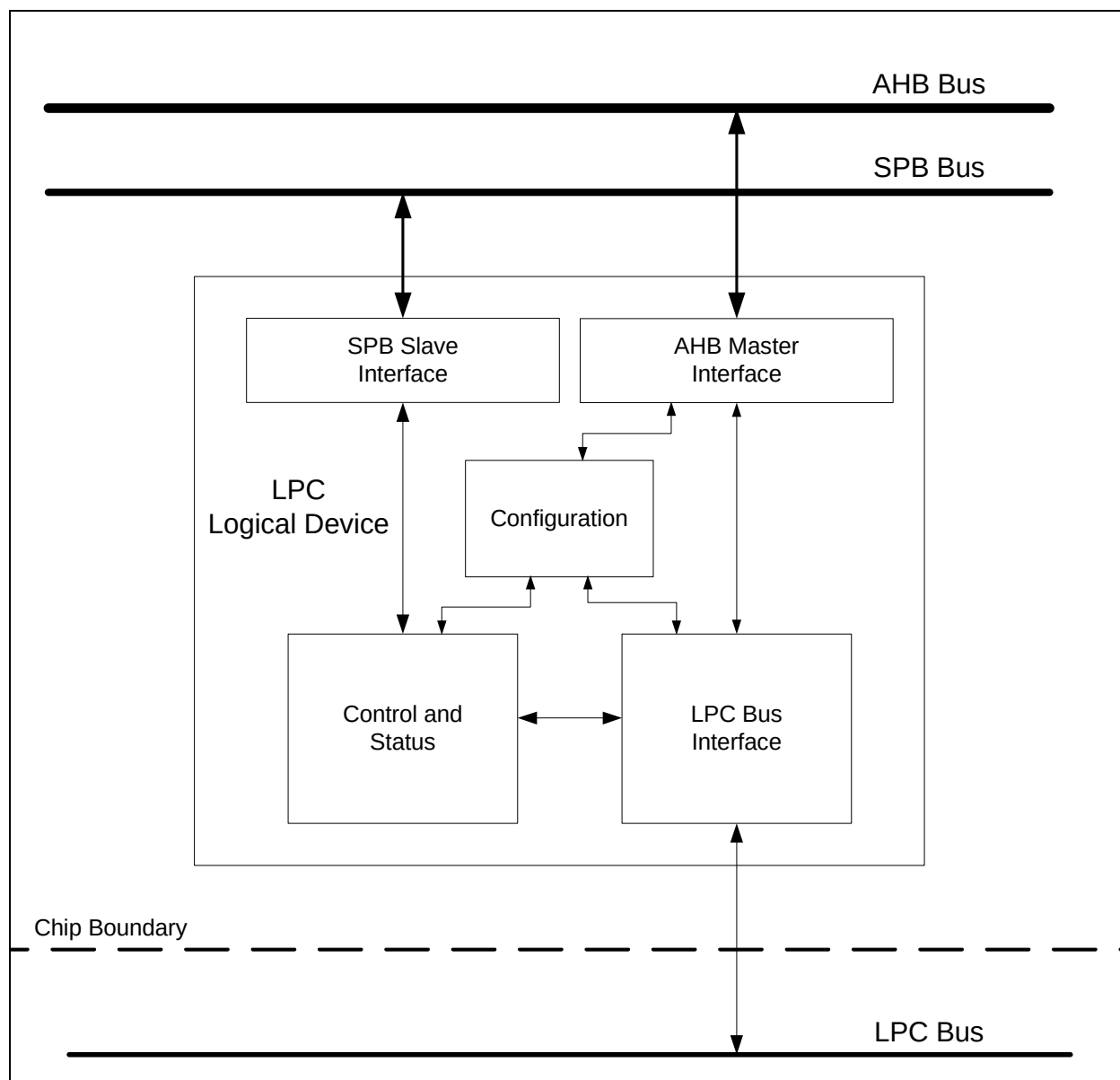


Figure 5.2

The LPC Logical Device is directly connected to two internal buses, the 32-bit AHB as well as the SPB. The SPB interface is 32-bits. In addition, it is connected to the external LPC bus.

Host accesses to [Configuration Registers](#) for each Logical Device on the MEC5035 are managed by a Configuration block described in [Chapter 6, "Logical Device Configuration," on page 140](#). Configuration registers are accessed through the LPC IO Configuration Register Port. The LPC Logical Device translates the Configuration address to an AHB address and the Host LPC access is converted into an AHB transaction inside the MEC5035.

Host I/O accesses to [Configuring Runtime Register Addresses](#) as well as LPC DMA accesses are converted directly to AHB accesses. The LPC address is translated by the LPC Bus Interface to an AHB address inside the MEC5035 and the access becomes an access on the AHB bus.

### 5.3.1 LPC Bus Interface

The MEC5035 communicates with the host over a Low Pin Count (LPC) interface. The LPC interface uses 3.3V signaling. For detailed specifications, see the *Intel Low Pin Count Specification* and the *PCI Local Bus Specification*, Section 4.2.2. The LPC Bus Interface is listed in [Table 3.3, "HOST INTERFACE," on page 41](#)

The following cycle types are supported by the LPC Bus protocol.

- 8-bit I/O Read
- 8-bit I/O Write
- 8-bit DMA Read (for Logical Devices which support 8-bit DMA)
- 8-bit DMA Write (for Logical Devices which support 8-bit DMA)
- 16-bit DMA Read (for Logical Devices which support 16-bit DMA)
- 16-bit DMA Write (for Logical Devices which support 16-bit DMA)

LPC transactions that access registers located on the basechip will require a minimum of two wait SYNCs on the LPC bus. The number of SYNCs may be larger if the AHB bus is in use by the embedded controller, or if the data referenced by the host is not present in a MEC5035 register. The MEC5035 always uses Long Wait SYNCs, rather than Short Wait SYNCs, when responding to an LPC bus request.

[Table 5.2, "LPC Bus Pin Behavior on Reset"](#), shows the behavior of LPC outputs and input/outputs under reset conditions. See [Section 3.7.1, "Pin Default State Through Power Transitions," on page 66](#) for more complete Power transition pin state description.

**Table 5.2 LPC Bus Pin Behavior on Reset**

| Pins     | VTR POR<br>(nSYS_RST) | VCC POR            | LPCPD#<br>Asserted | LRESET#<br>Asserted |
|----------|-----------------------|--------------------|--------------------|---------------------|
| LAD[3:0] | Tri-state             | Tri-state          | Tri-State          | Tri-State           |
| LDRQ#    | Tri-state             | De-asserted (high) | De-asserted (high) | De-asserted (high)  |
| SERIRQ   | Tri-state             | Tri-state          | Tri-State          | Tri-State           |
| CLKRUN#  | Tri-state             | Tri-state          | Tri-State          | Tri-State           |

### 5.3.2 LPC I/O Cycles

LPC 8-bit I/O Read cycles and 8-bit I/O Write cycles are mapped directly to addresses in the MEC5035 AHB address space. The mapping will be to the range FF\_0000h through FF\_FFFFh. For information on how addresses map between the LPC bus and the MEC5035, see [Chapter 7, "Bus Hierarchy," on page 162](#) and [Chapter 6, "Logical Device Configuration," on page 140](#). For a list of all Configuration Registers accessible to the Host, see [Chapter 6, "Logical Device Configuration," on page 140](#).

### 5.3.3 LPC Firmware Hub and Memory Cycles

The MEC5035 does not support LPC Firmware Hub cycles and LPC Memory cycles on the LPC Bus.

### 5.3.4 LPC DMA Cycles

There are no DMA peripherals on the MEC5035.



### 5.3.5 .Wait SYNC's on LPC

LPC cycles, with targets physically located in the MEC5035 basechip, are completed with no more than **two** LPC Long WAIT SYNC's

## 5.4 LPC Bus Configuration

The mapping from LPC Bus cycles to AHB read/write cycles is managed by the LPC Logical Device. The mapping is defined by a series of configuration registers which are defined in [Chapter 6, "Logical Device Configuration," on page 140](#), in [Section 5.4, "LPC Bus Configuration," on page 125](#).

## 5.5 Host Interrupts to EC

The LRESET# reset signal and the LPCPD# power down signal can be used to generate EC interrupts and wake-up events. The edge detection of the interrupt and wake events are controlled by their associated [Pin Control Register on page 376](#). The interrupts are routed to the LRESET# and LPCPD# bits in the [IRQ15 Source Register on page 332](#).

The LPC Logical Device can generate an additional interrupt to the EC when a Host access is mapped to the AHB bus. Bit LPC\_AHB\_ERR in the [Host Bus Error Register](#) is set when an LPC-sourced AHB bus access causes an error; it is also routed to the LPC\_AHB\_ERR bit in the [IRQ15 Source Register on page 332](#). For details see [Section 5.10.2, "Host Bus Error Register," on page 134](#).

## 5.6 EC Interrupts to Host

The Embedded Controller can send an interrupt to the Host on any Serial Interrupt Request channel using the [EC SIRIRQ Register](#) in conjunction with the [SERIRQ Configuration Registers](#).

## 5.7 LPC Clock Run and LPC Power Down Behavior

The LPCPD# signal (see the *Intel Low Pin Count Specification*, Section 8.1) and the CLKRUN# signal (see the *Intel Low Pin Count Specification*, Section 8.2) are implemented in the MEC5035.

### 5.7.1 Using LPCPD#

The MEC5035 must tolerate the LPCPD# signal going active and then inactive again without LRESET# going active. This is a requirement for notebook power management functions.

The *LPC Bus Specification, Rev. 1.0*, Section 8.2 states that "After LPCPD# goes back inactive, the LPC I/F will always be reset using LRST#". This text must be qualified for mobile systems where it is possible that when exiting a "light" sleep state (ACPI S1, APM POS), LPCPD# may be asserted but the LPC Bus power may not be removed, in which case LRESET# will not occur. When exiting a "deeper" sleep state (ACPI S3-S5, APM STR, STD, soft-off), LRESET# will occur.

The LPCPD# pin is implemented as a "local" powergood for the LPC bus in the MEC5035. It is not to be used as a global powergood for the chip. It is used to minimize the LPC power dissipation. It should be used to reset the LPC block and hold it in reset.

Prior to going to a low-power state, the system asserts the LPCPD# signal. LPCPD# goes active at least 30 microseconds prior to the LCLK signal stopping low and power being shut to the other LPC interface signals. Upon recognizing LPCPD# active, there are no further transactions on the LPC interface. The MEC5035 drives the LDRQ# signal low or tri-state, and does so until LPCPD# goes active. This prevents the MEC5035 from driving the signals high into a potentially powered-down host.



Upon recognizing LPCPD# inactive, The MEC5035 drives LDRQ0# high.

## 5.7.2 Using CLKRUN#

CLKRUN# is used to indicate the PCI clock status as well as to request that a stopped clock be started. See [Figure 5.3 CLKRUN# System Implementation Example on page 127](#), an example of a typical system implementation using CLKRUN#.

The CLKRUN# signal in the MEC5035 also supports the LPC nLDRQ DMA protocol since PCI clock is also required to drive the nLDRQ signal active (See [Section 6.7.1, "DMA Configuration Registers," on page 148](#)). If an interrupt or DMA occurs while the PCI clock is stopped, CLKRUN# must be asserted before the interrupt or DMA can be serviced.

PCI Clock Run Support can be enabled and disabled using the [Bit\[2\] SerIRQ Mode](#) in the [Device Mode](#) register, Global Configuration Register 24h (see [Table 6.16, "Chip-Level \(Global\) Control/Configuration Registers," on page 158](#)). When the [Bit\[2\] SerIRQ Mode](#) is '0,' Serial IRQs are disabled, the CLKRUN# pin is disabled, and the affects of Interrupt and DMA requests on CLKRUN# are ignored. When the [Bit\[2\] SerIRQ Mode](#) is '1,' Serial IRQs are enabled, the CLKRUN# pin is enabled, and the CLKRUN# support related to Interrupts and DMA requests as described in the section below is enabled.

The CLKRUN# pin is an open drain output and input. Refer to the *PCI Mobile Design Guide Rev 1.0* for a description of the CLKRUN# function. If CLKRUN# is sampled "high", the PCI clock is stopped or stopping. If CLKRUN# is sampled "low", the PCI clock is starting or started (running). CLKRUN# in the MEC5035 supports both Serial IRQ and LPC DMA cycles.

### 5.7.2.1 CLKRUN# Support for Serial IRQ Cycle

If a device in the MEC5035 asserts or de-asserts an interrupt and CLKRUN# is sampled "high", the MEC5035 can request the restoration of the clock by asserting the CLKRUN# signal asynchronously ([Table 5.3](#)). The MEC5035 holds CLKRUN# low until it detects two rising edges of the clock. After the second clock edge, the MEC5035 must disable the open drain driver ([Figure 5.4](#)).

The MEC5035 must not assert CLKRUN# if it is already driven low by the central resource; i.e., the PCI CLOCK GENERATOR in [Figure 5.3](#). The MEC5035 will not assert CLKRUN# under any conditions if the Serial IRQs are disabled.

The MEC5035 must not assert CLKRUN# unless the line has been de-asserted for two successive clocks; i.e., before the clock was stopped ([Figure 5.4](#)).

### 5.7.2.2 CLKRUN# Support for LPC DMA Cycle

If a device in the MEC5035 requests DMA service while the PCI clock is stopped, CLKRUN# must be asserted to restart the PCI clock so that the nLDRQ signal may be asserted (See [Table 5.3](#)). The MEC5035 will not assert CLKRUN# under any conditions if the SerIRQ\_Mode bit is inactive ("0").

If a device in the MEC5035 asserts a DMA request and CLKRUN# is sampled "high", the MEC5035 holds CLKRUN# low until it detects two rising edges of the PCI clock. After the second clock edge, the MEC5035 must disable the CLKRUN# open-drain driver (See [Figure 5.4](#)).

The MEC5035 will not assert CLKRUN# if it is already driven low by the central resource; i.e., the PCI CLOCK GENERATOR. The MEC5035 also will not assert CLKRUN# unless the signal has been de-asserted for two successive clocks; i.e., before the clock was stopped.

Table 5.3 MEC5035 CLKRUN# Function

| SIRQ_MODE<br>(BIT 2 OF GR24) | INTERNAL INTERRUPT<br>OR DMA REQUEST | CLKRUN# | ACTION         |
|------------------------------|--------------------------------------|---------|----------------|
| 0                            | X                                    | X       | None           |
| 1                            | NO CHANGE                            | X       | None           |
|                              | CHANGE (Note 5.1)                    | 0       | None           |
|                              | CHANGE (Note 5.1)                    | 1       | Assert CLKRUN# |

**Note 5.1** “Change” means either-edge change on any or all parallel IRQs routed to the Serial IRQ block. “Assertion” means assertion of DMA request by a device in the MEC5035. The “change” detection logic must run asynchronously to the PCI Clock and regardless of the Serial IRQ mode; i.e., “continuous” or “quiet”.

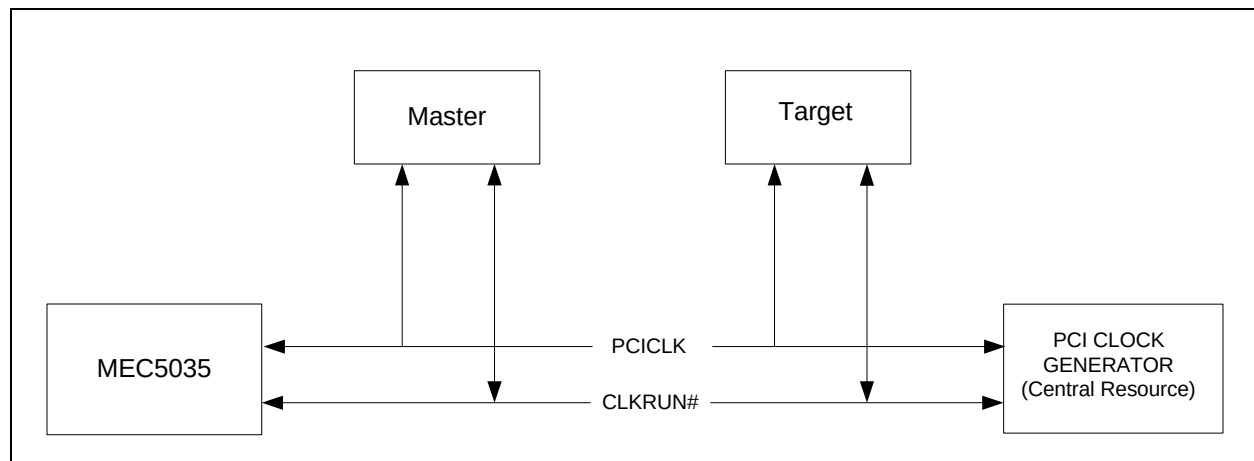


Figure 5.2 CLKRUN# System Implementation Example

Figure 5.3 CLKRUN# System Implementation Example

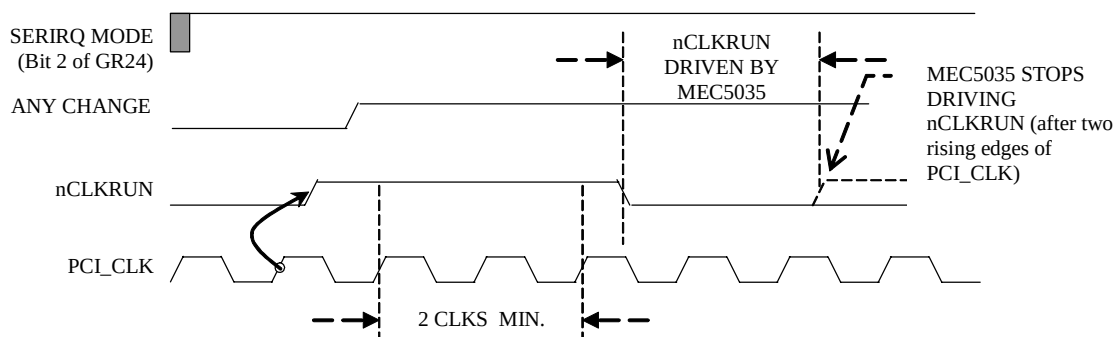


Figure 5.4 Clock Start Illustration

**Notes:**

- The signal “ANY CHANGE” is the same as “CHANGE/ASSERTION” in [Table 5.3](#).
- The MEC5035 must continually monitor the state of CLKRUN# to maintain the PCI Clock until an active “any IRQ change” condition has been transferred to the host in a Serial IRQ cycle or “any DRQ assertion” condition has been transferred to the host in a DMA cycle. For example, if “any IRQ change or DRQ assertion” is asserted before CLKRUN# is de-asserted (not shown in [Figure 5.4](#)), the MEC5035 must assert CLKRUN# as needed until the Serial IRQ cycle or DMA cycle has completed.

## 5.8 Using Serial Interrupts

The MEC5035 will support the serial interrupt scheme, which is adopted by several companies, to transmit interrupt information to the system. The serial interrupt scheme adheres to the *Serial IRQ Specification for PCI Systems Version 6.0*.

**TIMING DIAGRAMS for IRQSER CYCLE**

PCICLK = 33 MHz\_IN pin

IRQSER = SIRQ pin

Start Frame timing with source sampled a low pulse on IRQ1

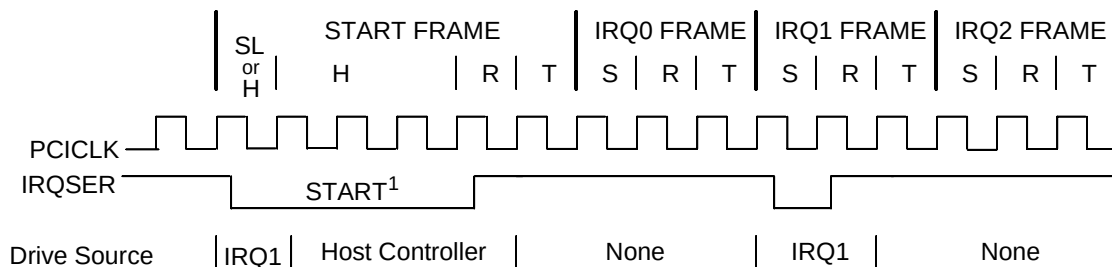


**Figure 5.5 Serial Interrupts Waveform "Start Frame"**

H=Host Control      SL=Slave Control      R=Recovery      T=Turn-around      S=Sample

Start Frame pulse can be 4-8 clocks wide.

Stop Frame Timing with Host using 17 IRQSER sampling period

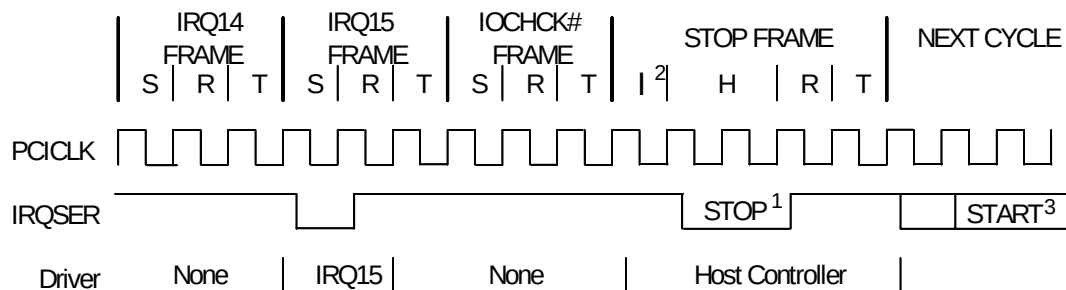


**Figure 5.6 Serial Interrupt Waveform "Stop Frame"**



H=Host Control

R=Recovery

T=Turn-around

S=Sample

I= Idle

Stop pulse is two clocks wide for Quiet mode, three clocks wide for Continuous mode.

There may be none, one, or more Idle states during the Stop Frame.

The next IRQSER cycle's Start Frame pulse may or may not start immediately after the turn-around clock of the Stop Frame.

### 5.8.1 SERIRQ Mode Bit Function

**Table 5.4 SERIRQ\_EN Configuration Control**

| CR25 BIT[2] | NAME      | DESCRIPTION                  |
|-------------|-----------|------------------------------|
| 0           | SERIRQ_EN | Serial IRQ Disabled          |
| 1           |           | Serial IRQ Enabled (Default) |

#### 5.8.1.1 IRQSER Cycle Control

There are two modes of operation for the IRQSER Start Frame.

##### Quiet (Active) Mode

Any device may initiate a Start Frame by driving the IRQSER low for one clock, while the IRQSER is Idle. After driving low for one clock, the IRQSER must immediately be tri-stated without at any time driving high. A Start Frame may not be initiated while the IRQSER is active. The IRQSER is Idle between Stop and Start Frames. The IRQSER is active between Start and Stop Frames. This mode of operation allows the IRQSER to be Idle when there are no IRQ/Data transitions which should be most of the time.

Once a Start Frame has been initiated, the host controller will take over driving the IRQSER low in the next clock and will continue driving the IRQSER low for a programmable period of three to seven clocks. This makes a total low pulse width of four to eight clocks. Finally, the host controller will drive the IRQSER back high for one clock then tri-state.

Any IRQSER Device (i.e., The MEC5035) which detects any transition on an IRQ/Data line for which it is responsible must initiate a Start Frame in order to update the host controller unless the IRQSER is already in an IRQSER Cycle and the IRQ/Data transition can be delivered in that IRQSER Cycle.

##### Continuous (Idle) Mode

Only the Host controller can initiate a Start Frame to update IRQ/Data line information. All other IRQSER agents become passive and may not initiate a Start Frame. IRQSER will be driven low for four to eight clocks by host controller. This mode has two functions. It can be used to stop or idle the IRQSER or the host controller can operate IRQSER in a continuous mode by initiating a Start Frame at the end of every Stop Frame.

An IRQSER mode transition can only occur during the Stop Frame. Upon reset, IRQSER bus is defaulted to continuous mode, therefore only the host controller can initiate the first Start Frame. Slaves must continuously sample the Stop Frames pulse width to determine the next IRQSER Cycle's mode.

##### IRQSER Data Frame

Once a Start Frame has been initiated, the MEC5035 will watch for the rising edge of the Start Pulse and start counting IRQ/Data Frames from there. Each IRQ/Data Frame is three clocks: Sample phase, Recovery phase, and Turn-around phase. During the sample phase, the MEC5035 must drive the

IRQSER (SIRQ pin) low, if and only if, its last detected IRQ/Data value was low. If its detected IRQ/Data value is high, IRQSER must be left tri-stated. During the recovery phase, the MEC5035 must drive the SERIRQ high, if and only if, it had driven the IRQSER low during the previous sample phase. During the turn-around phase, the MEC5035 must tri-state the SERIRQ. The MEC5035 drives the IRQSER line low at the appropriate sample point if its associated IRQ/Data line is low, regardless of which device initiated the start frame.

The Sample phase for each IRQ/Data follows the low to high transition of the Start Frame pulse by a number of clocks equal to the IRQ/Data Frame times three, minus one e.g. The IRQ5 Sample clock is the sixth IRQ/Data Frame, then the sample phase is  $\{(6 \times 3) - 1 = 17\}$  the seventeenth clock after the rising edge of the Start Pulse.

**Table 5.5 IRQSER Sampling Periods**

| IRQSER PERIOD | SIGNAL SAMPLED | # OF CLOCKS PAST START |
|---------------|----------------|------------------------|
| 1             | Not Used       | 2                      |
| 2             | IRQ1           | 5                      |
| 3             | nSMI/IRQ2      | 8                      |
| 4             | IRQ3           | 11                     |
| 5             | IRQ4           | 14                     |
| 6             | IRQ5           | 17                     |
| 7             | IRQ6           | 20                     |
| 8             | IRQ7           | 23                     |
| 9             | IRQ8           | 26                     |
| 10            | IRQ9           | 29                     |
| 11            | IRQ10          | 32                     |
| 12            | IRQ11          | 35                     |
| 13            | IRQ12          | 38                     |
| 14            | IRQ13          | 41                     |
| 15            | IRQ14          | 44                     |
| 16            | IRQ15          | 47                     |

The SIRQ data frame will now support IRQ2 from a logical device; previously IRQSER Period 3 was reserved for use by the System Management Interrupt (nSMI). When using Period 3 for IRQ2, the user should mask off the MEC5035's SMI via the ESMI Mask Register. Likewise, when using Period 3 for nSMI, the user should not configure any logical devices as using IRQ2.

IRQSER Period 14 is used to transfer IRQ13. Each Logical devices will have IRQ13 as a choice for their primary interrupt.

#### Stop Cycle Control

Once all IRQ/Data Frames have completed, the host controller will terminate IRQSER activity by initiating a Stop Frame. Only the host controller can initiate the Stop Frame. A Stop Frame is indicated when the IRQSER is low for two or three clocks. If the Stop Frame's low time is two clocks, then the next IRQSER cycle's sampled mode is the Quiet mode; and any IRQSER device may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse. If the Stop Frame's



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low time is three clocks, then the next IRQSER cycle's sampled mode is the continuous mode, and only the host controller may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse.

### Latency

Latency for IRQ/Data updates over the IRQSER bus in bridge-less systems with the minimum IRQ/Data Frames of 17 will range up to 96 clocks (3.84 $\mu$ S with a 25 MHz PCI Bus or 2.88 $\mu$ S with a 33 MHz PCI Bus). If one or more PCI to PCI Bridge is added to a system, the latency for IRQ/Data updates from the secondary or tertiary buses will be a few clocks longer for synchronous buses, and approximately double for asynchronous buses.

### EOI/ISR Read Latency

Any serialized IRQ scheme has a potential implementation issue related to IRQ latency. IRQ latency could cause an EOI or ISR Read to precede an IRQ transition that it should have followed. This could cause a system fault. The host interrupt controller is responsible for ensuring that these latency issues are mitigated. The recommended solution is to delay EOIs and ISR Reads to the interrupt controller by the same amount as the IRQSER Cycle latency in order to ensure that these events do not occur out of order.

### AC/DC Specification Issue

All IRQSER agents must drive/sample IRQSER synchronously related to the rising edge of the PCI bus clock. The IRQSER (SIRQ) pin uses the electrical specification of the PCI bus. Electrical parameters will follow the PCI Specification Section 4, sustained tri-state.

### Reset and Initialization

The IRQSER bus uses LRESET as its reset signal and follows the PCI bus reset mechanism. The IRQSER pin is tri-stated by all agents while LRESET is active. With reset, IRQSER slaves and bridges are put into the (continuous) Idle mode. The host controller is responsible for starting the initial IRQSER cycle to collect system's IRQ/Data default values. The system then follows with the Continuous/Quiet mode protocol (Stop Frame pulse width) for subsequent IRQSER cycles. It is the host controller's responsibility to provide the default values to the 8259's and other system logic before the first IRQSER cycle is performed. For IRQSER system suspend, insertion, or removal application, the host controller should be programmed into Continuous (IDLE) mode first. This is to guarantee the IRQSER bus is in Idle state before the system configuration changes.

## 5.9 LPC Logical Device Configuration Registers

The configuration registers in the LPC Logical Device are described in [Chapter 6, "Logical Device Configuration," on page 140](#). These registers control the activity of all the Logical Devices in the MEC5035. The [Activate Register](#) controls the LPC device itself. The Host can shut down the LPC Logical Device by clearing the Activate bit, but it cannot restart the LPC interface, since once the LPC interface is inactive the Host has no access to any registers on the MEC5035. The Embedded Controller can set or clear the Activate bit at any time.

**Table 5.6 Activate Register**

|             |            |    |    |       |    |    |                     |          |
|-------------|------------|----|----|-------|----|----|---------------------|----------|
| HOST OFFSET | BYTE0: 30h |    |    | 8-bit |    |    | HOST SIZE           |          |
| EC ADDRESS  | FF_3330h   |    |    | 8-bit |    |    | EC SIZE             |          |
| POWER       | VTR        |    |    | 00b   |    |    | nSYS_RST<br>DEFAULT |          |
| BUS         | LPC SPB    |    |    |       |    |    |                     |          |
| BYTE0 BIT   | D7         | D6 | D5 | D4    | D3 | D2 | D1                  | D0       |
| HOST TYPE   | R          | R  | R  | R     | R  | R  | R                   | R/W      |
| EC TYPE     | R          | R  | R  | R     | R  | R  | R                   | R/W      |
| BIT NAME    | Reserved   |    |    |       |    |    |                     | Activate |

#### ACTIVATE

When this bit is 1, the LPC Logical Device is powered and functional.

When this bit is 0, the logical device is powered down and inactive. Except for the [Activate Register](#) itself, clocks to the block are gated and the LPC Logical Device will permit the ring oscillator to be shut down (see [Section 5.10.4, "EC Clock Control Register," on page 137](#)). LPC bus output pads will be tri-stated. Serial IRQ activation is separately controlled by the [Device Mode](#) register in the [Chip-Level \(Global\) Control/Configuration Registers](#).

**APPLICATION NOTE:** The [Activate](#) bit in the [Activate Register](#) should not be written '0' to by the Host over LPC.

## 5.10 LPC Logical Device EC-only Registers

[Table 5.7, "LPC EC-only Registers"](#) summarizes the registers in the Host Interface block that are only accessible by the EC. In addition to these registers, the Host Interface also contains Configuration registers, described in [Chapter 6, "Logical Device Configuration," on page 140](#).

**Table 5.7 LPC EC-only Registers**

| AHB ADDRESS | NAME                                      | VTR POR (nSYS_RST) DEFAULT |
|-------------|-------------------------------------------|----------------------------|
| FF_3100h    | Reserved                                  | 0000_0000h                 |
| FF_3104h    | <a href="#">LPC Bus Monitor Register</a>  | 0000_0000h                 |
| FF_3108h    | <a href="#">Host Bus Error Register</a>   | 0000_0000h                 |
| FF_310Ch    | <a href="#">EC SIRIRQ Register</a>        | 0000_0000h                 |
| FF_3110h    | <a href="#">EC Clock Control Register</a> | 0000_0000h                 |

Because their addresses are in the part of the LPC Logical Device address frame that is not addressable from the LPC bus, the following registers are accessible only to the EC.

## 5.10.1 LPC Bus Monitor Register

Table 5.8 LPC Bus Monitor Register

|               |          |     |     |        |    |     |                  |              |
|---------------|----------|-----|-----|--------|----|-----|------------------|--------------|
| HOST OFFSET   | N/A      |     |     | N/A    |    |     | HOST SIZE        |              |
| EC ADDRESS    | FF_3104h |     |     | 32-bit |    |     | EC SIZE          |              |
| POWER         | VTR      |     |     | 00h    |    |     | nSYS_RST DEFAULT |              |
| BUS           | LPC SPB  |     |     |        |    |     |                  |              |
| BYTE[3:1] BIT | D31      | D30 | D29 | ...    |    | D10 | D9               | D8           |
| HOST TYPE     | -        | -   | -   | -      | -  | -   | -                | -            |
| EC TYPE       | R        | R   | R   | R      | R  | R   | R                | R            |
| BIT NAME      | Reserved |     |     |        |    |     |                  |              |
| BYTE0 BIT     | D7       | D6  | D5  | D4     | D3 | D2  | D1               | D0           |
| HOST TYPE     | -        | -   | -   | -      | -  | -   | -                | -            |
| EC TYPE       | R        | R   | R   | R      | R  | R   | R                | R            |
| BIT NAME      | Reserved |     |     |        |    |     | LRESET_Status    | LPCPD_Status |

### LPCPD\_STATUS

This bit reflects the state of the LPCPD# input pin. The LPCPD\_Status is the inverse of the LPCPD# pin (see [Section 5.7, "LPC Clock Run and LPC Power Down Behavior,"](#) on page 125).

When the LPCPD\_Status bit is '0b', the LPCPD# input pin is de-asserted (that is, the pin has the value '1b'). When the LPCPD\_Status bit is '1b', the LPCPD# input pin is asserted (that is, the pin has the value '0b').

An interrupt to the EC will be generated on either edge of LPCPD#. See [Section 5.5, "Host Interrupts to EC,"](#) on page 125

### LRESET\_STATUS

This bit reflects the state of the LRESET# input pin. The LRESET\_Status is the inverse of the LRESET# pin (see [Section 5.2.3, "Resets,"](#) on page 122).

When the LRESET\_Status bit is '0b', the LRESET# input pin is de-asserted (that is, the pin has the value '1b'). When the LRESET\_Status bit is '1b', the LRESET# input pin is asserted (that is, the pin has the value '0b').

An interrupt to the EC will be generated on either edge of LRESET#. See [Section 5.5, "Host Interrupts to EC,"](#) on page 125



## 5.10.2 Host Bus Error Register

Table 5.9 Host Bus Error Register

|             |                     |          |         |            |             |              |                     |             |
|-------------|---------------------|----------|---------|------------|-------------|--------------|---------------------|-------------|
| HOST OFFSET | N/A                 |          |         | N/A        |             |              | HOST SIZE           |             |
| EC ADDRESS  | FF_3108h            |          |         | 32-bit     |             |              | EC SIZE             |             |
| POWER       | VTR                 |          |         | 0000_0000h |             |              | nSYS_RST<br>DEFAULT |             |
| BUS         | LPC SPB             |          |         |            |             |              |                     |             |
| BYTE3 BIT   | D31                 | D30      | D29     | D28        | D27         | D26          | D25                 | D24         |
| HOST TYPE   | -                   | -        | -       | -          | -           | -            | -                   | -           |
| EC TYPE     | R                   | R        | R       | R          | R           | R            | R                   | R           |
| BIT NAME    | ErrorAddress[23:16] |          |         |            |             |              |                     |             |
| BYTE2 BIT   | D23                 | D22      | D21     | D20        | D19         | D18          | D17                 | D16         |
| HOST TYPE   | -                   | -        | -       | -          | -           | -            | -                   | -           |
| EC TYPE     | R                   | R        | R       | R          | R           | R            | R                   | R           |
| BIT NAME    | ErrorAddress[15:8]  |          |         |            |             |              |                     |             |
| BYTE1 BIT   | D15                 | D14      | D13     | D12        | D11         | D10          | D9                  | D8          |
| HOST TYPE   | -                   | -        | -       | -          | -           | -            | -                   | -           |
| EC TYPE     | R                   | R        | R       | R          | R           | R            | R                   | R           |
| BIT NAME    | ErrorAddress[7:0]   |          |         |            |             |              |                     |             |
| BYTE0 BIT   | D7                  | D6       | D5      | D4         | D3          | D2           | D1                  | D0          |
| HOST TYPE   | -                   | -        | -       | -          | -           | -            | -                   | -           |
| EC TYPE     | R                   | R/WC     | R/WC    | R/WC       | R/WC        | R/WC         | R/W                 | R/WC        |
| BIT NAME    | Reserved            | Reserved | DMA Err | Config Err | Runtime Err | BAR_Conflict | En_AHB_Err          | LPC_AHB_Err |

### LPC\_AHB\_ERR

This bit can be used to generate an EC interrupt. It is set whenever either a BAR conflict or an AHB bus error occurs as a result of an LPC access. Once set, it remains set until cleared by being written with a 1.

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When this bit is 0, only a BAR conflict, which occurs when two BARs match the same LPC I/O address, will cause **LPC\_AHB\_ERR** to be set. When this bit is 1, AHB bus errors will also cause **LPC\_AHB\_ERR** to be set.

**BAR\_CONFLICT**

This bit is set to 1 whenever a BAR conflict occurs on an LPC address. A Bar conflict occurs when more than one BAR matches the address during of an LPC cycle access. Once this bit is set, it remains set until cleared by being written with a 1.

**RUNTIME\_ERR**

This bit is set to 1 whenever **En\_AHB\_ERR** is 1 and an LPC I/O access causes an AHB bus error. This error will only occur if a BAR is misconfigured. Once set, it remains set until cleared by being written with a 1.

**CONFIG\_ERR**

This bit is set to 1 whenever **En\_AHB\_ERR** is 1 and an LPC Configuration access causes an AHB bus error. Once set, it remains set until cleared by being written with a 1.

**DMA\_ERR**

This bit is set to 1 whenever **En\_AHB\_ERR** is 1 and an LPC DMA access causes an AHB bus error. Once set, it remains set until cleared by being written with a 1.

**ERRORADDRESS**

This 24-bit field captures the 24-bit AHB address of every LPC transaction whenever the bit **LPC\_AHB\_ERR** in this register is 0. When **LPC\_AHB\_ERR** is 1 this register is not updated but retains its previous value. When bus errors occur this field saves the address of the first address that caused an error.

### 5.10.3 EC SERIRQ Register

**Table 5.10 EC SIRIRQ Register**

|               |          |     |     |            |    |     |                  |        |
|---------------|----------|-----|-----|------------|----|-----|------------------|--------|
| HOST OFFSET   | N/A      |     |     | N/A        |    |     | HOST SIZE        |        |
| EC ADDRESS    | FF_310Ch |     |     | 32-bit     |    |     | EC SIZE          |        |
| POWER         | VTR      |     |     | 0000_0000h |    |     | nSYS_RST DEFAULT |        |
| BUS           | LPC SPB  |     |     |            |    |     |                  |        |
| BYTE[3:1] BIT | D31      | D30 | D29 | ...        |    | D10 | D9               | D8     |
| HOST TYPE     | -        | -   | -   | -          | -  | -   | -                | -      |
| EC TYPE       | R        | R   | R   | R          | R  | R   | R                | R      |
| BIT NAME      | Reserved |     |     |            |    |     |                  |        |
| BYTE0 BIT     | D7       | D6  | D5  | D4         | D3 | D2  | D1               | D0     |
| HOST TYPE     | -        | -   | -   | -          | -  | -   | -                | -      |
| EC TYPE       | R        | R   | R   | R          | R  | R   | R                | R/W    |
| BIT NAME      | Reserved |     |     |            |    |     |                  | EC_IRQ |

#### EC\_IRQ

If the LPC Logical Device is selected as the source for a Serial Interrupt Request by an Interrupt Configuration register (see [Section 6.8, "SERIRQ Interrupts," on page 150](#)), this bit is used as the interrupt source.

## 5.10.4 EC Clock Control Register

Table 5.11 EC Clock Control Register

|               |          |     |     |            |    |     |                  |     |
|---------------|----------|-----|-----|------------|----|-----|------------------|-----|
| HOST OFFSET   | N/A      |     |     | N/A        |    |     | HOST SIZE        |     |
| EC ADDRESS    | FF_3110h |     |     | 32-bit     |    |     | EC SIZE          |     |
| POWER         | VTR      |     |     | 0000_0000h |    |     | nSYS_RST DEFAULT |     |
| BUS           | LPC SPB  |     |     |            |    |     |                  |     |
| BYTE[3:1] BIT | D31      | D30 | D29 | ...        |    | D10 | D9               | D8  |
| HOST TYPE     | -        | -   | -   | -          | -  | -   | -                | -   |
| EC TYPE       | R        | R   | R   | R          | R  | R   | R                | R   |
| BIT NAME      | Reserved |     |     |            |    |     |                  |     |
| BYTE0 BIT     | D7       | D6  | D5  | D4         | D3 | D2  | D1               | D0  |
| HOST TYPE     | -        | -   | -   | -          | -  | -   | -                | -   |
| EC TYPE       | R        | R   | R   | R          | R  | R   | R/W              | R/W |
| BIT NAME      | Reserved |     |     |            |    |     | Clock_Control    |     |

### CLOCK\_CONTROL

This field controls when the host interface will permit the internal ring oscillator to be shut down. The choices are as follows:

- 0h:** The host interface will permit the ring oscillator to be shut down if the LPCPD# signal is asserted (sampled low)
- 1h:** The host interface will permit the ring oscillator to be shut down if the CLKRUN# signals "CLOCK STOP" and there are no pending serial interrupt request or DMA requests from devices associated with the MEC5035. The CLKRUN# signals "CLOCK STOP" by CLKRUN# being high for 5 LPCCLK's after the raising edge of CLKRUN#.
- 2h:** The host interface will permit the ring oscillator to be shut down after the completion of every LPC transaction. It will require the ring oscillator as soon as a START field appears on the LPC bus. This mode may cause an increase in the time to respond to LPC transactions if the ring oscillator has to turn on and adjust its speed after the LPC transaction arrives at the MEC5035
- 3h:** The ring oscillator is not permitted to shut down as long as the host interface is active

When the [Activate](#) bit in the [Activate Register on page 132](#) is 0, the Host Interface will permit the ring oscillator to be shut down and the [Clock\\_Control](#) Field is ignored. The [Clock\\_Control](#) Field only effects the Host Interface when the [Activate](#) bit in the [Activate Register](#) is 1.

## 5.11 Host Interface Revision History

This revision history shows the changes made to this chapter.

**Table 5.12 Host Interface Chapter Revision History**

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History," on page 539.</a> |              |            |                                                                                                          |                                                                                                                                                                                                                                                                                                                            |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------------|----------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE       | SECTION/FIGURE/ENTRY                                                                                     | CORRECTION                                                                                                                                                                                                                                                                                                                 |
| 1.                                                                                                                                                                                                                                          | 0.4          | 04/30/2007 | Global<br><br><a href="#">Clock_Control on page 137</a><br><a href="#">Activate on page 132</a>          | <ul style="list-style-type: none"> <li>Remove references top FWM/ MEM cycles. Not implemented.</li> <li>Replace VTR POR with <a href="#">nSYS_RST</a>.</li> <li>Replace nPCIRST with LRESET# 2x</li> <li>Activate bit =0 unconditionally asserts clk_en. CLOCK STOP defined for CLKRUN#</li> <li>Added section.</li> </ul> |
| 2.                                                                                                                                                                                                                                          | 0.4          | 04/30/2007 | <a href="#">Section 5.3.1, "LPC Bus Interface," on page 124</a><br><a href="#">Table 5.2 on page 124</a> | LDRQ pin tristated between <a href="#">nSYS_RST</a> & VCC_PWRGD assertion.                                                                                                                                                                                                                                                 |
| 3.                                                                                                                                                                                                                                          |              |            |                                                                                                          |                                                                                                                                                                                                                                                                                                                            |
| 4.                                                                                                                                                                                                                                          |              |            |                                                                                                          |                                                                                                                                                                                                                                                                                                                            |



## Chapter 6 Logical Device Configuration

### 6.1 Description

The Configuration of the MEC5035 is very flexible and is based on the configuration architecture implemented in typical Plug-and-Play components.

The MEC5035 is designed for motherboard designs in which the resources required by their components are known. With its flexible resource allocation architecture, the MEC5035 allows the BIOS to assign resources at POST.

### 6.2 Location of Configuration Registers

Configuration Registers for Logical Devices accessible by the Host are located on the LPC SPB in the address range FF\_0000h through FF\_FFFFh. All Configuration Registers are located at addresses where address bits 9 and 8 are both '1b' (that is, at offsets 300h through 3FFh from the base of a 1KB address frame). Configuration registers are accessible by the Embedded Controller with 8-bit, 16-bit or 32-bit accesses. The Host can access the registers only with 8-bit accesses.

The Configuration Registers for the LPC Logical Device are located on the LPC SPB in the address range FF\_3300h through FF\_33F0h. The Global Configuration Registers are located within the Global Configuration Logical Device.

### 6.3 Basechip Logical Devices

Logical devices described in this section are peripherals that are located on the MEC5035 basechip and are accessible to the Host over the LPC bus.

Each logical device on the MEC5035 can have a set of Runtime Register and a set of Configuration Registers. The distinction between Runtime and Configuration registers is that the Host can access Runtime Registers by a direct I/O address, while it can only access Configuration Registers through a configuration port. The Embedded Controller (EC) can access all Configuration Registers and all Runtime Registers directly. The Logical Device Numbers for the Logical Devices resident in the MEC5035 are listed in [Table 6.14, "MEC5035 Configuration Register Map," on page 154.](#)

**Table 6.1 Basechip Logical Devices**

| Logical Device Number | Logical Device                             | Logical Device CR Map on <a href="#">Table 6.14</a> |
|-----------------------|--------------------------------------------|-----------------------------------------------------|
| 0h                    | <a href="#">Mailbox Interface</a>          | <a href="#">on page 154</a>                         |
| 1h                    | <a href="#">Keyboard Controller (8042)</a> | <a href="#">on page 154</a>                         |
| 2h                    | <a href="#">ACPI EC Channel 1</a>          | <a href="#">on page 154</a>                         |
| 3h                    | <a href="#">ACPI EC Channel 2</a>          | <a href="#">on page 154</a>                         |
| 4h                    | <a href="#">ACPI EC Channel 3</a>          | <a href="#">on page 154</a>                         |
| 5h                    | <a href="#">ACPI PM1</a>                   | <a href="#">on page 154</a>                         |
| 6h                    | <a href="#">UART</a>                       | <a href="#">on page 154</a>                         |
| 7h                    | <a href="#">Legacy (Fast KB)</a>           | <a href="#">on page 155</a>                         |
| Ch                    | <a href="#">LPC Interface</a>              | <a href="#">on page 155</a>                         |

**Table 6.1 Basechip Logical Devices**

| Logical Device Number | Logical Device       | Logical Device CR Map on Table 6.14 |
|-----------------------|----------------------|-------------------------------------|
| Eh                    | Embedded Flash       | on page 156                         |
| 3Fh                   | Global Configuration | on page 156                         |

Each Companion device may have an additional 16 Logical Devices; Configuration Registers for these Logical Devices are described in the specifications for each Companion.

All Configuration and Runtime Registers in the MEC5035 have an assigned AHB address between FF 0000h and FF FFFFh. Configuration and Runtime Registers in Companion devices are assigned AHB addresses between FE\_0000h and FE\_FFFFh. The EC can issue reads and writes to any register in that AHB address range. The EC can access 8-bit registers with 8-bit reads and writes, 16-bit registers with either 8-bit or 16-bit reads and writes and 32-bit registers with 8-bit, 16-bit and 32-bit reads and writes.

The Host can only access a subset of the AHB address space, and within that space all registers are treated as 8-bit registers, although a register may be implemented as a 32-bit register and accessible to the EC as a 32-bit register. The Host accesses registers in the FF\_0000h through FF\_FFFFh range through LPC I/O cycles. I/O cycles are mapped according to rules described in [Section 6.5, on page 142](#), [Section 6.6, on page 144](#) and [Section 6.7, on page 148](#).

## 6.4 Registers

The [Host Interface](#) has its own Logical Device Number and Base Address as indicated in [Table 6.2](#). The Host LPC I/O addresses for the [Logical Device Configuration](#) are selected via a Base Address Register. LPC access to configuration registers is through the Host Access Configuration Port.

The [Logical Device Configuration](#) also has a [Global Configuration](#) block which has a separate Logical Device Number and Base Address Register as indicated in [Table 6.2](#). The Base Address Register for the [Global Configuration](#) has only one writable bit, the Valid Bit, since the only I/O accessible Register has a fixed address.

[Table 6.3](#) is a register summary for the [LPC Interface](#) block and [Table 6.16, "Chip-Level \(Global\) Control/Configuration Registers," on page 158](#) is a register summary for the [Global Configuration](#) block.

**Table 6.2 Host Interface Base Address Table**

| Host Interface BLOCKS | LDN FROM (Table 7.2 on page 167) | AHB BASE ADDRESS |
|-----------------------|----------------------------------|------------------|
| LPC Interface         | Ch                               | FF_3000h         |
| Global Configuration  | 3Fh                              | FF_FC00h         |

**Note:** The Host LPC I/O addresses for this instance are selected via a Base Address Register (see [Section 6.6.2, on page 144](#)). LPC access to configuration registers is through the Host Access Configuration Port (see [Section 6.5.1, on page 142](#).)

[Table 6.3](#) is a register summary for the [Host Access Port](#) block. The LPC I/O address for each Run-Time Register is described below as an offset from its Base Address Register. Each EC address is indicated as an SPB Offset from its AHB base address. Each Configuration register access through



the [Host Access Port](#) address via its LDN indicated in [Table 6.2 on page 141](#) and its [Host Access Port](#) index which is described as “Host Config Index” in the tables below.

**Table 6.3 Host Access Port Register Summary**

| PORT NAME   | HOST I/O ACCESS |            |           | EC INTERFACE |           |         | NOTES |
|-------------|-----------------|------------|-----------|--------------|-----------|---------|-------|
|             | HOST I/O INDEX  | SPB OFFSET | HOST TYPE | SPB OFFSET   | BYTE LANE | EC TYPE |       |
| CONFIG PORT | 00h             | 00h        | W         |              |           |         |       |
| INDEX PORT  | 00h             | 00h        | R/W       |              |           |         |       |
| DATA PORT   | 01h             | 01h        | R/W       |              |           |         |       |

**Note:** The EC does not have access to the [Host Access Port](#); however, the EC can access registers with AHB addresses.

## 6.5 Configuration Registers

### 6.5.1 Host Access Port

The Host can access Configuration Registers through a port described in [Section 6.5.2, on page 142](#). Host accesses are limited to 8 bits. There are 48 8-bit Global Configuration Registers (at offsets 00h through 2Fh), plus up to 208 8-bit registers associated with each Logical Device. The Logical Device is selected with the [Logical Device Number](#) Register (Global Configuration Register 07h). The INDEX PORT is used to select a specific logical device register. These registers are then accessed through the DATA PORT. The Logical Device registers are accessible only when the device is in the Configuration State.

Only two states are defined (Run and Configuration). In the Run State, the chip will always be ready to enter the Configuration State.

The desired configuration registers are accessed in two steps:

- Write the index of the [Logical Device Number](#) Configuration Register (i.e., 07h) to the INDEX PORT and then write the number of the desired logical device to the DATA PORT
- Write the address of the desired configuration register within the logical device to the INDEX PORT and then write or read the configuration register through the DATA PORT.

**Note:** If accessing the Global Configuration Registers, step (a) is not required.

**Note:** Any write to an undefined or reserved Configuration register is terminated normally on the LPC bus without any modification of state in the basechip or Companion device. Any read to an undefined or reserved Configuration register returns FFh.

### 6.5.2 Primary Configuration Address Decoder

The logical devices are configured through three Configuration Access Ports (CONFIG, INDEX and DATA). The BIOS uses these ports to initialize the logical devices at POST ([Table 6.4](#)).

The Base Address of the Configuration Access Ports is determined by the BAR that corresponds to Logical Device Ch, the [LPC Interface](#). This is the first BAR in the table, at AHB address FF\_3360h. The Configuration Access Port BAR is unique in that an LPC I/O access that matches this BAR does not directly generate an AHB read or write. Instead, the Device and Frame values in the BAR indicates that the LPC I/O should be handled locally in the LPC Logical Device.

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The Configuration map will issue an AHB read or write, the results of which will be used to complete the LPC access.

**Table 6.4 MEC5035 Configuration Access Ports**

| PORT NAME   | RELATIVE ADDRESS                            | TYPE       | PORT NAME   |
|-------------|---------------------------------------------|------------|-------------|
| CONFIG PORT | Configuration Access Ports Base Address + 0 | Write      | CONFIG PORT |
| INDEX PORT  | Configuration Access Ports Base Address + 0 | Read/Write | INDEX PORT  |
| DATA PORT   | Configuration Access Ports Base Address + 1 |            | DATA PORT   |

**6.5.2.1 Entering the Configuration State**

The INDEX and DATA ports are effective only when the chip is in the Configuration State. The device enters the Configuration State when the Config Entry Key is successfully written to the CONFIG PORT.

**Config Entry Key = < 55h>**

**6.5.2.2 Exiting the Configuration State**

The device exits the Configuration State when the following Config Exit Key is successfully written to the CONFIG PORT address.

**Config Exit Key = < AAh>**

**6.5.2.3 Read Accessing Configuration Port**

The data read from the Configuration Port is undefined when not in the Configuration State. Writing the Config Entry Key puts the chip in the Configuration State. Once in the Configuration State, reading the Configuration Port will return the last value written to the Configuration Index. If no value was written the Configuration Port reads 00h.

**6.5.3 Configuration Sequence Example**

To program the configuration registers, the following sequence must be followed:

1. Enter Configuration State
2. Program the Configuration Registers
3. Exit Configuration State.

The following is an example of a configuration program in Intel 8086 assembly language.

```

;-----
; ENTER CONFIGURATION STATE
;-----
MOV DX, CONFIG_PORT_BASE_ADDRESS
MOV AX, 055H ; Config Entry Key
OUT DX, AL

;-----
; CONFIGURE BASE ADDRESS,
; LOGICAL DEVICE 8
;-----
MOV DX, CONFIG_PORT_BASE_ADDRESS
MOV AL, 07H
OUT DX, AL ; Point to LD# Config Reg
MOV DX, CONFIG_PORT_BASE_ADDRESS+1
MOV AL, 08H
OUT DX, AL ; Point to Logical Device 8
;
MOV DX, CONFIG_PORT_BASE_ADDRESS
MOV AL, 60H

```

```
OUT DX,AL ; Point to BASE ADDRESS REGISTER
MOV DX, CONFIG_PORT_BASE_ADDRESS+1
MOV AL, 02H
OUT DX,AL ; Update BASE ADDRESS REGISTER
;-----
; EXIT CONFIGURATION STATE
;-----
MOV DX, CONFIG_PORT_BASE_ADDRESS
MOV AX, 0AAH ; Config Exit Key
OUT DX,AL.
```

## 6.5.4 Configuration Register Address Mapping

The INDEX PORT defines 256 bytes for configuration. The first 48 of these bytes are Global Configuration registers, which reside in the first 48 bytes of the Configuration part of the address frame for Logical Device 3Fh. Values of INDEX greater than 48 map into registers that are specific to the Logical Device specified in the Global Configuration Logical Device Number Register 7h. These registers reside in upper 20 bytes of the Logical Device address frame. See [Section 6.10.2](#), on [page 153](#) for details.

## 6.6 Configuring Runtime Register Addresses

### 6.6.1 Runtime Registers

Runtime Registers are registers that are accessible to the Host within the Host I/O address space. These Host I/O accesses are all mapped into the MEC5035 AHB address space onto devices located on the LPC SPB. Runtime registers all reside within the first 256 bytes of a 1KB Logical Device address frame. The Host accesses these registers with 8-bit LPC I/O accesses. Each 8-bit I/O address is mapped into an 8-bit address in the AHB address space, so the first 256 bytes of the Logical Device frame can accommodate 256 LPC Runtime Registers per Logical Device. The Host I/O addresses are determined by a block of [Base Address Registers](#) located in the LPC Logical Device. The Embedded Controller can access all the Runtime Registers as well, using loads and stores to full AHB addresses.

### 6.6.2 Base Address Registers

Each Logical Device has a Base Address Register (BAR). These BARs are located in blocks of Configuration Registers in Logical Device 0Ch, in the AHB address range FF\_3360h through FF\_3384h. On every LPC bus I/O access all Base Address Registers are checked in parallel and if any matches the LPC I/O address the MEC5035 claims the bus cycle.

**Note:** Software should insure that no two BARs map the same LPC I/O address. If two BARs do map to the same address, the [BAR\\_Conflict](#) bit in the [Host Bus Error Register](#) on [page 134](#) is set when an LPC access targeting the BAR Conflict address. An EC interrupt can be generated.

Each BAR is 32 bits wide. The format of each BAR is summarized in [Table 6.5, "Base Address Register Format"](#). An LPC I/O request is translated by the BAR into an 8-bit read or write transaction on the AHB bus. The 16-bit LPC I/O address is translated into a 24-bit AHB address.

The Base Address Register Table is itself part of the AHB address space. It resides in the Configuration quadrant of Logical Device 20h, the LPC bus interface.

**Table 6.5 Base Address Register Format**

| BYTE3 BIT | D31                                      | D30    | D29   | D28 | D27 | D26 | D25 | D24 |
|-----------|------------------------------------------|--------|-------|-----|-----|-----|-----|-----|
| BIT NAME  | LPC Host Address, most significant bits  |        |       |     |     |     |     |     |
| BYTE2 BIT | D23                                      | D22    | D21   | D20 | D19 | D18 | D17 | D16 |
| BIT NAME  | LPC Host Address, least significant bits |        |       |     |     |     |     |     |
| BYTE1 BIT | D15                                      | D14    | D13   | D12 | D11 | D10 | D9  | D8  |
| BIT NAME  | Valid                                    | Device | Frame |     |     |     |     |     |
| BYTE0 BIT | D7                                       | D6     | D5    | D4  | D3  | D2  | D1  | D0  |
| BIT NAME  | Reserved                                 | Mask   |       |     |     |     |     |     |

**MASK**

These 7 bits are used to mask off address bits in the address match between an LPC I/O address and the Host Address field of the BARs, as described in [Section 6.6.3, "Mapping LPC I/O Addresses"](#). A block of up to 128 8-bit registers can be assigned to one base address.

**FRAME**

These 6 bits are used to specify a logical device frame number within a bus. This field is multiplied by 400h to provide the frame address within the peripheral bus address. If [DEVICE](#) is 0, then the logical device is located on the MEC5035 and all 6 bits are used for the frame number. In the MEC5035 Frame values for frames corresponding to logical devices that are not present on the MEC5035 are invalid.

**DEVICE**

This bit combined with [FRAME](#) constitute the Logical Device Number. DEVICE identifies the physical location of the logical device. If this bit is 0, the logical device is located on the MEC5035 and the AHB address is on the local AHB bus. This bit should always be set to 0.

**VALID**

If this bit is 1, the BAR is valid and will participate in LPC matches. If it is 0 this BAR is ignored

**HOST\_ADDRESS**

These 16 bits are used to match LPC I/O addresses

## 6.6.3 Mapping LPC I/O Addresses

A Base Address Register will match an LPC I/O address, and thus the MEC5035 will claim the LPC bus cycle, if the following relation holds:

$$(\text{LPC Address} \& \sim \text{BAR.MASK}) == (\text{BAR.LPC\_Address} \& \sim \text{BAR.MASK}) \\ \& \& (\text{BAR.Valid} == 1)$$

If one of the BARs match, the LPC cycle will be claimed and the LPC request will be translated to an AHB address according to the following formulae:

DEVICE = 0:

AHB Address = FF\_000h | (BAR.Frame<<10) | (LPC\_Address & BAR.MASK)

The formulae are illustrated in Figure 6.1, "LPC BAR Mapping":

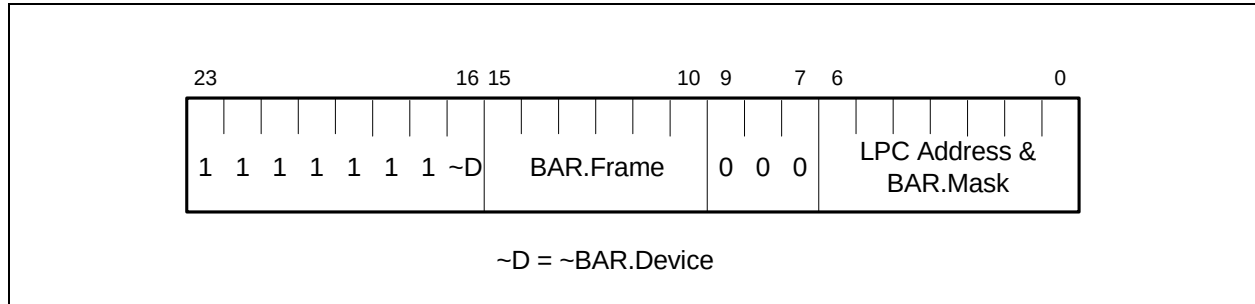


**Figure 6.1 LPC BAR Mapping**

When matching LPC I/O addresses, the MEC5035 ignores address bits that correspond to '1b' bits in the MASK field. When forming the AHB address from the LPC I/O address, the LPC I/O address bits that correspond to the '1b' bits in the MASK are passed through to the AHB address. For example, the Keyboard Controller (9042 Interface) Base Address Register has 60h in the LPC Address field, the Frame field is 01h, and the MASK field is 04h. Because of the single '1b' bit in MASK, the BAR will match LPC I/O patterns in the form '00000000011000hb', so both 60h and 64h will be matched and claimed by the MEC5035. When forming the AHB address, the Frame number 01h will be put in bit positions 15 through 10 and concatenated with FF\_0000h, to form the Keyboard Controller Frame base address of FF\_0400h. If the Host reads from address 60h, a read access will be initiated to AHB address FF\_0400h (the base address OR'd with bit 2 from 60h). If the Host reads from address 64h, a read access will be initiated to AHB address FF\_0404h (again, bit 2 from the LPC I/O address is OR'd into the AHB address).

As another example, if a standard 16550 UART was located at LPC I/O address 238h, then the UART Receive buffer would appear at address 238h and the Line Status register at 23Dh. If the BAR for the UART was set to 0238\_8047h, then the UART will be matched at I/O address 238h, the UART is located on the basechip in Logical Device 6h, the UART is enabled and the UART device includes 8 registers. The Receive buffer would map to AHB address FF\_1800h and the Line Status register would map to AHB address FF\_1805h.

## 6.6.4 Base Address Register Table

Table 6.6, "Base Address Registers Default Values", lists the Base Address Registers for all logical devices on the MEC5035 base chip. The BAR EC Offsets are relative to the base address of the LPC Logical Device, which is located at AHB address FF\_3000h. The columns to the right of the heavy line show the field definitions for the default values listed in the column labeled "Reset Default". Shaded fields in Table 6.6 are read-only. .

The EC can read and write the BAR table entries with 32-bit, 16-bit or 8-bit accesses. The Host accesses the BAR table using 8-bit reads and writes.

**Note:** The BAR at offset 360h associated with the LPC Interface is different in that LPC I/O accesses that are claimed by this BAR does not translate directly into a AHB addresses. Addresses that are claimed by this BAR, the Configuration Port BAR, are used to manage Configuration Registers. These accesses are described in Section 6.5, on page 142. This BAR is also special in that a byte write to offset 362h (bits[7:0] of the LPC Host Address field) does not directly write into the BAR. Instead, the byte is held in a buffer. A byte write to offset 363h will both write the byte at offset 363h and will copy the buffer into offset 362h. This is done to insure



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that the 16-bit LPC Host Address field of the Configuration Port BAR is always completely updated in one cycle.

Table 6.6 Base Address Registers Default Values

| BAR EC OFFSET | LPC OFFSET | RESET DEFAULT | LPC I/O ADDRESS | VALID | DEVICE | FRAME | MASK | DESCRIPTION                                                              |
|---------------|------------|---------------|-----------------|-------|--------|-------|------|--------------------------------------------------------------------------|
| 360h          | 60h        | 002E_0C01h    | 002Eh           | 0     | 0      | C     | 1    | Logical Device 0Ch: LPC Interface (Configuration Port)                   |
| 364h          | 64h        | 0000_0001h    | 0000h           | 0     | 0      | 0     | 1    | Logical Device 00h: Mailbox Register I/F                                 |
| 368h          | 68h        | 0060_0104h    | 0000h           | 0     | 0      | 1     | 4    | Logical Device 01h: Keyboard Controller (8042 Interface)                 |
| 36Ch          | 6Ch        | 0062_0207h    | 0062h           | 0     | 0      | 2     | 4    | Logical Device 02h: ACPI EC Interface 1 (See <a href="#">Note 6.2.</a> ) |
| 370h          | 70h        | 0062_0307h    | 0062h           | 0     | 0      | 3     | 7    | Logical Device 03h: ACPI EC Interface 2 (See <a href="#">Note 6.3</a> )  |
| 374h          | 74h        | 0062_0407h    | 0062h           | 0     | 0      | 4     | 7    | Logical Device 04h: ACPI EC Interface 3 (See <a href="#">Note 6.3</a> )  |
| 378h          | 78h        | 0000_0507h    | 0000h           | 0     | 0      | 5     | 7    | Logical Device 05h: ACPI PM1 Interface                                   |
| 37Ch          | 7Ch        | 0000_0607h    | 0000h           | 0     | 0      | 6     | 7    | Logical Device 06h: UART                                                 |
| 380h          | 80h        | 0092_0700h    | 0092h           | 0     | 0      | 7     | 0    | Logical Device 07h: Legacy (GATEA20) I/F                                 |
| 384h          | 84h        | 0000_0E04h    | 0000h           | 0     | 0      | E     | 4    | Logical Device 0Eh: Embedded Flash Interface                             |

**Note 6.2** In order to avoid address conflict with the [Keyboard Controller \(8042\)](#) LDN 1h at legacy at LPC I/O address 60h/64h, only [ACPI EC Channel 1](#) LDN 2h at AHB base address [FF\\_0800h](#) should be located at the legacy LPC I/O address 62h/66h. When operating both the [Keyboard Controller \(8042\)](#) and [ACPI EC Channel 1](#) at legacy LPC I/O addresses 60h/62h/64h/66h, the Mask value in [ACPI EC Channel 1](#) BAR should be programmed to 4h and the [ACPI EC Channel 1](#), [EC\\_Cx\\_Byte Count Register](#), [Byte Count](#) on [page 187](#) should remain 0. To utilize the [ACPI EC Channel 1](#) in [Non Legacy Operation](#) the [ACPI EC Channel 1](#) BAR must be placed on LPC I/O 8 byte boundary. (See [Section 9.5](#), on [page 186](#)). Only bits[3:0] in the Mask field of [ACPI EC Channel 1](#) BAR are programmable, bits[6:4] are read-only '000'.

**Note 6.3** The [ACPI EC Channel 2](#) & [ACPI EC Channel 3](#) LDN 3h & 4h can not be located at the the legacy LPC I/O address 62h/66h. The [ACPI EC Channel 2](#) & [ACPI EC Channel 3](#) BAR's must be placed on LPC I/O 8 byte boundaries.

## 6.7 DMA

LPC DMA cycles are mapped to AHB memory addresses by the LPC Logical Device. The addresses reference FIFOs that are associated with the DMA. FIFO addresses are restricted to 32-bit aligned addresses (that is, addresses that are divisible by 4). Configuration for DMA Device access is described in [Section 6.7.1, on page 148](#).

### 6.7.1 DMA Configuration Registers

The MEC5035 will claim an LPC DMA request if the requested channel is listed as valid in the [Table 6.7, "DMA Configuration Register Map"](#). A channel is claimed if the [DMA Configuration Register Format](#) that corresponds to the channel maps to a Logical Device. In order to execute the DMA operation, the MEC5035 translates the DMA access into a bus read or write of the FIFO that corresponds to channel in question. The address of a DMA FIFO will always be one of the first 16 32-aligned addresses within the DMA quadrant of a Logical Device frame.

The mapping in the [DMA Configuration Register Map](#) is used both for mapping LPC DMA I/O requests from the Host to Logical Devices, as well as for mapping DMA requests from Logical Devices to the LPC Bus LDRQ# DMA request signal.

The Host can access the DMA Configuration registers with 8-bit accesses. The EC can access the DMA Configuration registers as four 32-bit registers, eight 16-bit registers or sixteen 8-bit registers.

The mapping of DMA devices into the AHB address space is shown in Figure 6.4, "DMA Address Mapping":

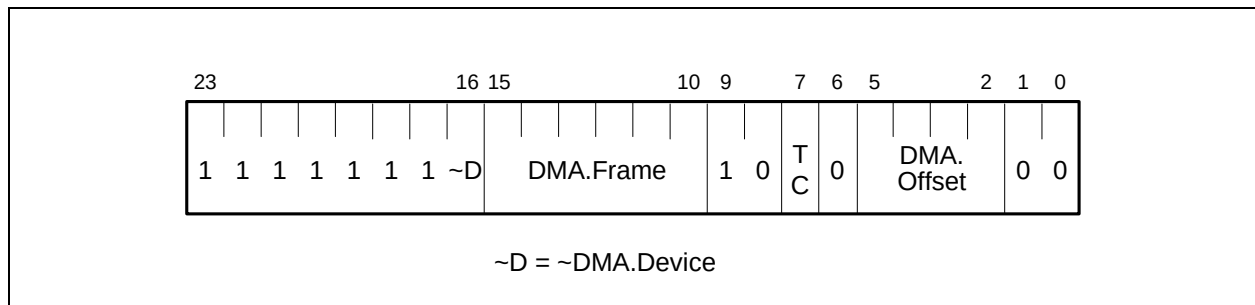


**Figure 6.4 DMA Address Mapping**

**Table 6.7 DMA Configuration Register Map**

| ADDRESS  | TYPE | RESET | CONFIGURATION REGISTER NAME |
|----------|------|-------|-----------------------------|
| FF_3350h | R/W  | 0000h | DMA Channel 0               |
| FF_3352h | R/W  | 0000h | DMA Channel 1               |
| FF_3354h | R/W  | 0000h | DMA Channel 2               |
| FF_3356h | R/W  | 0000h | DMA Channel 3               |
| FF_3358h | R    | 0000h | DMA Channel 4 (Reserved)    |
| FF_335Ah | R/W  | 0000h | DMA Channel 5               |
| FF_335Ch | R/W  | 0000h | DMA Channel 6               |

**Table 6.7 DMA Configuration Register Map (continued)**

| ADDRESS  | TYPE | RESET | CONFIGURATION REGISTER NAME |
|----------|------|-------|-----------------------------|
| FF_335Eh | R/W  | 0000h | DMA Channel 7               |

**Note 6.5** DMA Channel 4 is reserved in the MEC5035. LPC Host cycles with DMA channel 4 asserted will be unclaimed by the MEC5035.

**Table 6.8 DMA Configuration Register Format**

| BYTE1 BIT | D15   | D14    | D13   | D12 | D11    | D10 | D9 | D8 |
|-----------|-------|--------|-------|-----|--------|-----|----|----|
| BIT NAME  | Valid | Device | Frame |     |        |     |    |    |
| BYTE0 BIT | D7    | D6     | D5    | D4  | D3     | D2  | D1 | D0 |
| BIT NAME  | Event |        |       |     | Offset |     |    |    |

**OFFSET**

These 4 bits select which register within the Logical Device address space are to be used for this DMA. The 4 addresses correspond to the following address offsets:

|     |        |
|-----|--------|
| 0h: | +200h  |
| 1h: | +204h  |
| 2h: | +208h  |
| 3h: | +20Ch  |
| 4h: | +210h  |
| 5h: | +214h  |
| 6h: | +218h  |
| 7h: | +21Ch  |
| 8h: | +220h  |
| 9h: | +224h. |
| Ah: | +228h  |
| Bh: | +22Ch  |
| Ch: | +230h  |
| Dh: | +234h  |
| Eh: | +238h  |
| Fh: | +23Ch  |

**EVENT**

If **DEVICE** is 0, the DMA Request for this channel is sourced from the MEC5035 Logical Device identified by **FRAME** and this field is ignored.

**FRAME**

These 6 bits are used to a logical device frame number within a bus. This field is multiplied by 400h to provide the frame address within the peripheral bus address. If **DEVICE** is 0, then the logical device is located on the MEC5035 and all 6 bits are used for the frame number. In the MEC5035 Frame values greater than 0Ah are invalid, since there are only 11 logical devices accessible to the Host.



## DEVICE

This bit combined with [FRAME](#) constitute the Logical Device Number. DEVICE identifies the physical location of the logical device. If this bit is 0, the logical device is located on the MEC5035 and the AHB address is on the local AHB bus. This field should always be 0.

## VALID

If this bit is 1, the DMA Channel is active on the MEC5035. If it is 0 this DMA Channel is ignored.

## 6.8 SERIRQ Interrupts

The MEC5035 can route Logical Device interrupts onto SIRQ stream frames IRQ[0:15]. Routing is controlled by the SIRQ Interrupt Configuration Registers. There is one SIRQ Interrupt Configuration Register for each accessible SIRQ Frame (IRQ); all 16 registers are listed in [Table 6.9, "SIRQ Interrupt Configuration Register Map"](#). Each SIRQ Interrupt Configuration Register controls a series of multiplexors which route to a single Logical Device interrupt as illustrated in [Figure 6.7 SIRQ Routing Internal Logical Devices on page 152](#). The format for each SIRQ Interrupt Configuration Register is described in [Table 6.10](#). Each Logical Device can have up to two LPC SERIRQ interrupts. When the MEC5035 is polled by the host, each SIRQ frame routes the level of the Logical Device interrupt (selected by the corresponding SIRQ Interrupt Configuration Register) to the SIRQ stream. See

**Note:** Two Logical Devices cannot share a Serial IRQ.

The SIRQ Interrupt Configuration Register The Host can access the Interrupt Configuration registers with 8-bit accesses. The EC can access the Interrupt Configuration registers as four 32-bit registers, eight 16-bit registers or sixteen 8-bit registers.

**Note:** An interrupt is deactivated by setting an entry in the [SIRQ Interrupt Configuration Register Map](#) to FFh, which is the default reset value.

### 6.8.1 SERIRQ Configuration Registers

**Table 6.9 SIRQ Interrupt Configuration Register Map**

| ADDRESS  | TYPE | RESET | CONFIGURATION REGISTER NAME |
|----------|------|-------|-----------------------------|
| FF_3340h | R/W  | FFh   | IRQ0                        |
| FF_3341h | R/W  | FFh   | IRQ1                        |
| FF_3342h | R/W  | FFh   | IRQ2 (nSMI)                 |
| FF_3343h | R/W  | FFh   | IRQ3                        |
| FF_3344h | R/W  | FFh   | IRQ4                        |
| FF_3345h | R/W  | FFh   | IRQ5                        |
| FF_3346h | R/W  | FFh   | IRQ6                        |
| FF_3347h | R/W  | FFh   | IRQ7                        |
| FF_3348h | R/W  | FFh   | IRQ8                        |
| FF_3349h | R/W  | FFh   | IRQ9                        |
| FF_334Ah | R/W  | FFh   | IRQ10                       |

**Table 6.9 SIRQ Interrupt Configuration Register Map (continued)**

| ADDRESS  | TYPE | RESET | CONFIGURATION REGISTER NAME |
|----------|------|-------|-----------------------------|
| FF_334Bh | R/W  | FFh   | IRQ11                       |
| FF_334Ch | R/W  | FFh   | IRQ12                       |
| FF_334Dh | R/W  | FFh   | IRQ13                       |
| FF_334Eh | R/W  | FFh   | IRQ14                       |
| FF_334Fh | R/W  | FFh   | IRQ15                       |

**Note 6.6** The SIRQ Interrupt Configuration Registers are though the [Host Access Port](#) as 8-bit accesses. The EC can access the SIRQ Interrupt Configuration Registers as 32-bit, 16-bit across 8-bit boundary or as individual 8-bit accesses.

**Table 6.10 SIRQ Interrupt Configuration Register Format**

| BYTE0 BIT | D7     | D6     | D5    | D4 | D3 | D2 | D1 | D0 |
|-----------|--------|--------|-------|----|----|----|----|----|
| BIT NAME  | Select | Device | Frame |    |    |    |    |    |

**FRAME**

When combined with [DEVICE](#), these six bits select the Logical Device as the source for the interrupt.

This field defaults to 3Fh

**Note:** The LPC Logical Device (Logical Device Number 0Ch) can be used by the Embedded Controller to generate a Serial Interrupt Request to the Host under software control.

**DEVICE**

This bit combined with [FRAME](#) constitute the Logical Device Number of the interrupt source. [DEVICE](#) identifies the physical location of the logical device. If this bit is 0, the logical device is located on the MEC5035.

This field defaults to 1.

**SELECT**

If this bit is 0, the first interrupt signal from the Logical Device is selected for the SERIRQ vector. If this bit is 1, the second interrupt signal from the Logical Device is selected. The KYBD controller is the only Logical Devices on the MEC5035 which has a second interrupt signal. For all other Logical Devices this field is ignored.

This field defaults to 1.

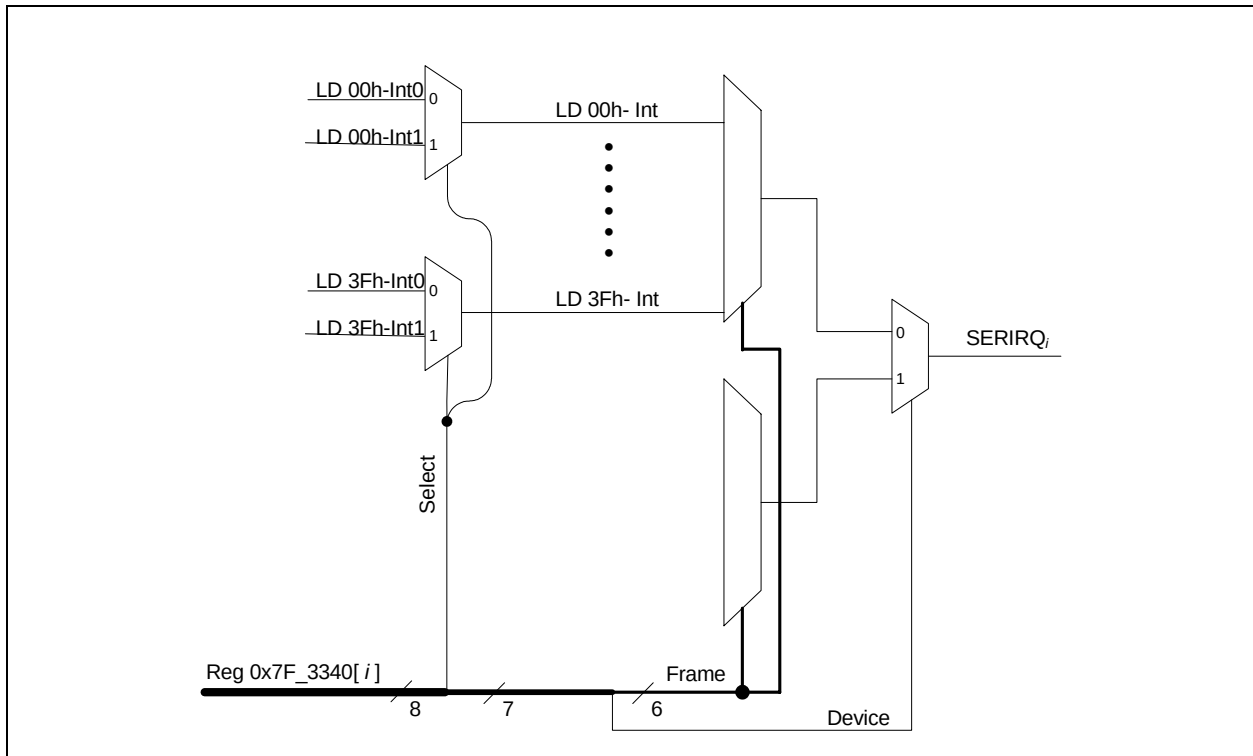


Figure 6.7 SIRQ Routing Internal Logical Devices

#### 6.8.1.1 MEC5035 SIRQ Routing

Table 6.11 MEC5035 Logical Device SIRQ Routing

| SIRQ INTERRUPT CONFIGURATION REGISTER |        |       |                                                               |
|---------------------------------------|--------|-------|---------------------------------------------------------------|
| SELECT                                | DEVICE | FRAME | LOGICAL DEVICE INTERRUPT SOURCE                               |
| 0                                     | 0      | 0     | MailBox SIRQ - See <a href="#">Section 8.3.1, on page 173</a> |
| 1                                     | 0      | 0     | SMI - <a href="#">Section 8.3.1, on page 173</a>              |
| 0                                     | 0      | 1     | Keyboard SIRQ - <a href="#">Section 10.4.1, on page 193</a>   |
| 1                                     | 0      | 1     | Mouse SIRQ - <a href="#">Section 10.4.1, on page 193</a>      |
| 0                                     | 0      | 6     | UART SIRQ - <a href="#">Section 12.3.1, on page 227</a>       |

## 6.9 Configuration Register Reset Conditions

There are two reset conditions that will cause Configuration Registers on the MEC5035 to reset to default values. A reset can be caused by a VTR Power On Reset condition or a VCC-Powergood Power on Reset condition. In addition, firmware running on the Embedded Controller can set all Configuration Registers to a default condition. The Host can request that the Configuration Registers be reset through a request to the Embedded Controller sent via the Mailbox interface.

## 6.10 Logical Device Configuration/Control Registers

A separate set of control and configuration registers exist for each Logical Device and is selected with the Logical Device # Register (07h). The Logical Devices are listed in [Table 6.1, "Basechip Logical Devices," on page 140](#), and the registers within each Logical Device are listed in [Section 6.10.2, on page 153](#).

### 6.10.1 Logical Device Activation

Many Logical Devices have a register, called Activate, that is used to activate the Logical Device. When a Logical Device is inactive, it is powered down and will not respond to an AHB request. The format for the Activate Register is shown in [Table 6.12, "Activate Register"](#). The Activate Register for the LPC Logical Device is shown in [Table 5.6, "Activate Register," on page 132](#).

**Table 6.12 Activate Register**

|             |                   |    |    |    |       |    |    |                     |  |
|-------------|-------------------|----|----|----|-------|----|----|---------------------|--|
| HOST OFFSET | BYTE0: 30h        |    |    |    | 8-bit |    |    | HOST SIZE           |  |
| EC OFFSET   | Frame offset 330h |    |    |    | 8-bit |    |    | EC SIZE             |  |
| POWER       | VTR               |    |    |    | 00b   |    |    | nSYS_RST<br>DEFAULT |  |
| BUS         | LPC SPB           |    |    |    |       |    |    |                     |  |
| BYTE0 BIT   | D7                | D6 | D5 | D4 | D3    | D2 | D1 | D0                  |  |
| HOST TYPE   | R                 | R  | R  | R  | R     | R  | R  | R/W                 |  |
| EC TYPE     | R                 | R  | R  | R  | R     | R  | R  | R/W                 |  |
| BIT NAME    | Reserved          |    |    |    |       |    |    | Activate            |  |

#### ACTIVATE

When this bit is 1, the logical device is powered and functional. When this bit is 0, the logical device is powered down and inactive.

### 6.10.2 Configuration Register Map

The MEC5035 Configuration register map is shown in [Table 6.14, "MEC5035 Configuration Register Map"](#). Logical Device numbers are in hexadecimal. All Logical Devices are accessible by both the Host and the EC. Logical Devices between 00h and 3Fh are located on the basechip.

The EC has access to all Configuration Registers and all Global Control registers directly on the AHB bus. The address of a Global Control register is 7F FF00h+*offset*, where *offset* is the offset listed in Column 2 of [Table 6.16, "Chip-Level \(Global\) Control/Configuration Registers"](#). The other Configuration Registers are accessible at the INDEX ([Table 6.14, Column 1](#)) plus the AHB Address Base ([Table 6.13, "Configuration Register AHB Mapping"](#), Column 2). LDN is the Logical Device Number.

**Note:** The Global Configuration Registers are the first 48 bytes of the configuration space Logical Device 3Fh.

Table 6.13 Configuration Register AHB Mapping

| Logical Device Range | AHB Address Base               |
|----------------------|--------------------------------|
| 00h - 3Fh            | FF_0300h + (LDN << 10)         |
| 40h - 7Fh            | FE_0300h + ((LDN - 40h) << 10) |

The Configuration Register address mapping is illustrated in:

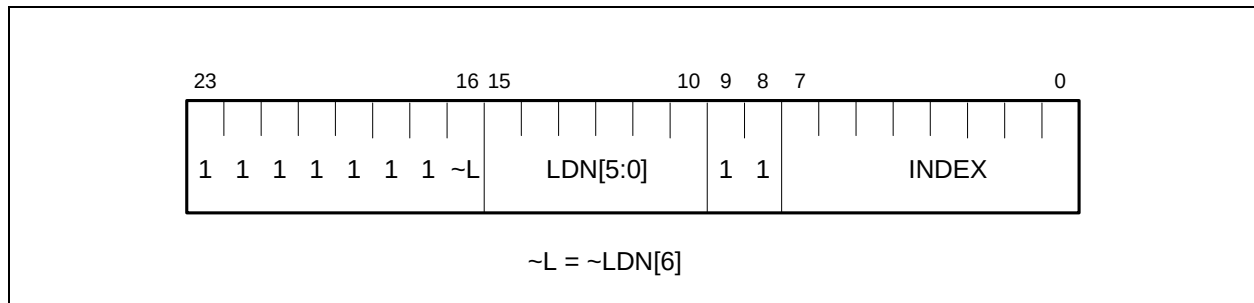


Figure 6.1 Configuration Register Mapping

Table 6.14 MEC5035 Configuration Register Map

| LPC<br>CR<br>INDEX                                                                                                             | AHB<br>OFFSET | TYPE<br><a href="#">Note 6.2</a> | RESET <a href="#">Note 6.3</a>  | CONFIGURATION REGISTER<br>NAME    |
|--------------------------------------------------------------------------------------------------------------------------------|---------------|----------------------------------|---------------------------------|-----------------------------------|
| Configuration Registers for LDN 0h ( <a href="#">Mailbox Interface</a> ) at AHB base address <a href="#">FF_0000h</a>          |               |                                  |                                 |                                   |
| -                                                                                                                              | -             | -                                | -                               | None                              |
| Configuration Registers for LDN 1h ( <a href="#">Keyboard Controller (8042)</a> ) at AHB base address <a href="#">FF_0400h</a> |               |                                  |                                 |                                   |
| 30h                                                                                                                            | 330h          | R/W                              | 00h on <a href="#">nSYS_RST</a> | <a href="#">Activate Register</a> |
| Configuration Registers for LDN 2h ( <a href="#">ACPI EC Channel 1</a> ) at AHB base address <a href="#">FF_0800h</a>          |               |                                  |                                 |                                   |
| -                                                                                                                              | -             | -                                | -                               | None                              |
| Configuration Registers for LDN 3h ( <a href="#">ACPI EC Channel 2</a> ) at AHB base address <a href="#">FF_0C00h</a>          |               |                                  |                                 |                                   |
| -                                                                                                                              | -             | -                                | -                               | None                              |
| Configuration Registers for LDN 4h ( <a href="#">ACPI EC Channel 3</a> ) at AHB base address <a href="#">FF_1000h</a>          |               |                                  |                                 |                                   |
| -                                                                                                                              | -             | -                                | -                               | None                              |
| Configuration Registers for LDN 5h ( <a href="#">ACPI PM1</a> ) at AHB base address <a href="#">FF_1400h</a>                   |               |                                  |                                 |                                   |
| -                                                                                                                              | -             | -                                | -                               | None                              |
| Configuration Registers for LDN 6h ( <a href="#">UART</a> ) at AHB base address <a href="#">FF_1800h</a>                       |               |                                  |                                 |                                   |

**Table 6.14 MEC5035 Configuration Register Map (continued)**

| LPC CR INDEX                                                                              | AHB OFFSET | TYPE<br>Note 6.2 | RESET Note 6.3    | CONFIGURATION REGISTER NAME                          |
|-------------------------------------------------------------------------------------------|------------|------------------|-------------------|------------------------------------------------------|
| 30h                                                                                       | 330h       | R/W              | 00h on nSYS_RST   | Activate Register                                    |
| F0h                                                                                       | 3F0h       | R/W              | 00h on nSYS_RST   | Configuration Select Register                        |
| <b>Configuration Registers for LDN 7h (Legacy (Fast KB)) at AHB base address FF_1C00h</b> |            |                  |                   |                                                      |
| 30h                                                                                       | 330h       | R/W              | 00h on nSYS_RST   | PORT92 Enable Register                               |
| <b>Configuration Registers for LDN Ch (LPC Interface) at AHB base address FF_3000h</b>    |            |                  |                   |                                                      |
| 30h                                                                                       | 330h       | R/W              | 00h on nSYS_RST   | Activate Register                                    |
| 40h                                                                                       | 340h       | R/W              | FFh on nSIO_RESET | SIRQ IRQ0 Configuration Register                     |
| 41h                                                                                       | 341h       | R/W              | FFh on nSIO_RESET | SIRQ IRQ1 Configuration Register                     |
| 42h                                                                                       | 342h       | R/W              | FFh on nSIO_RESET | SIRQ IRQ2 (nSMI) Configuration Register              |
| 43h                                                                                       | 343h       | R/W              | FFh on nSIO_RESET | SIRQ IRQ3 Configuration Register                     |
| 44h                                                                                       | 344h       | R/W              | FFh on nSIO_RESET | SIRQ IRQ4 Configuration Register                     |
| 45h                                                                                       | 345h       | R/W              | FFh on nSIO_RESET | SIRQ IRQ5 Configuration Register                     |
| 46h                                                                                       | 346h       | R/W              | FFh on nSIO_RESET | SIRQ IRQ6 Configuration Register                     |
| 47h                                                                                       | 347h       | R/W              | FFh on nSIO_RESET | SIRQ IRQ7 Configuration Register                     |
| 48h                                                                                       | 348h       | R/W              | FFh on nSIO_RESET | SIRQ IRQ8 Configuration Register                     |
| 49h                                                                                       | 349h       | R/W              | FFh on nSIO_RESET | SIRQ IRQ9 Configuration Register                     |
| 4Ah                                                                                       | 34Ah       | R/W              | FFh on nSIO_RESET | SIRQ IRQ10 Configuration Register                    |
| 4Bh                                                                                       | 34Bh       | R/W              | FFh on nSIO_RESET | SIRQ IRQ11 Configuration Register                    |
| 4Ch                                                                                       | 34Ch       | R/W              | FFh on nSIO_RESET | SIRQ IRQ12 Configuration Register                    |
| 4Dh                                                                                       | 34Dh       | R/W              | FFh on nSIO_RESET | SIRQ IRQ13 Configuration Register                    |
| 4Eh                                                                                       | 34Eh       | R/W              | FFh on nSIO_RESET | SIRQ IRQ14 Configuration Register                    |
| 4Fh                                                                                       | 34Fh       | R/W              | FFh on nSIO_RESET | SIRQ IRQ15 Configuration Register                    |
| 50h                                                                                       | 350h       | R/W              | 00h on nSIO_RESET | DMA Channel 0, LSB Configuration Register            |
| 51h                                                                                       | 351h       | R/W              | 00h on nSIO_RESET | DMA Channel 0, MSB Configuration Register            |
| 52h                                                                                       | 352h       | R/W              | 00h on nSIO_RESET | DMA Channel 1, LSB Configuration Register            |
| 53h                                                                                       | 353h       | R/W              | 00h on nSIO_RESET | DMA Channel 1, MSB Configuration Register            |
| 54h                                                                                       | 354h       | R/W              | 00h on nSIO_RESET | DMA Channel 2, LSB Configuration Register            |
| 55h                                                                                       | 355h       | R/W              | 00h on nSIO_RESET | DMA Channel 2, MSB Configuration Register            |
| 56h                                                                                       | 356h       | R/W              | 00h on nSIO_RESET | DMA Channel 3, LSB Configuration Register            |
| 57h                                                                                       | 357h       | R/W              | 00h on nSIO_RESET | DMA Channel 3, MSB Configuration Register            |
| 58h                                                                                       | 358h       | R/W              | 00h on nSIO_RESET | DMA Channel 4 (Reserved), LSB Configuration Register |

Table 6.14 MEC5035 Configuration Register Map (continued)

| LPC CR INDEX                                                                                   | AHB OFFSET                | TYPE<br>Note 6.2 | RESET Note 6.3           | CONFIGURATION REGISTER NAME                               |
|------------------------------------------------------------------------------------------------|---------------------------|------------------|--------------------------|-----------------------------------------------------------|
| 59h                                                                                            | 359h                      | R/W              | 00h on nSIO_RESET        | DMA Channel 4 (Reserved), MSB Configuration Register      |
| 5Ah                                                                                            | 35Ah                      | R/W              | 00h on nSIO_RESET        | DMA Channel 5, LSB Configuration Register                 |
| 5Bh                                                                                            | 35Bh                      | R/W              | 00h on nSIO_RESET        | DMA Channel 5, MSB Configuration Register                 |
| 5Ch                                                                                            | 35Ch                      | R/W              | 00h on nSIO_RESET        | DMA Channel 6, LSB Configuration Register                 |
| 5Dh                                                                                            | 35Dh                      | R/W              | 00h on nSIO_RESET        | DMA Channel 6, MSB Configuration Register                 |
| 5Eh                                                                                            | 35Eh                      | R/W              | 00h on nSIO_RESET        | DMA Channel 7, LSB Configuration Register                 |
| 5Fh                                                                                            | 35Fh                      | R/W              | 00h on nSIO_RESET        | DMA Channel 7, MSB Configuration Register                 |
| 60h - 63h                                                                                      | FF_3360h                  | R/W / R          | 002E_0C01h on nSIO_RESET | BAR for Configuration Port                                |
| 64h - 67h                                                                                      | FF_3364h                  | R/W / R          | 0000_0001h on nSIO_RESET | BAR for Mailbox                                           |
| 68h - 6Bh                                                                                      | FF_3368h                  | R/W / R          | 0060_0104h on nSIO_RESET | BAR for 8042/Keyboard Interface                           |
| 6C - 6F                                                                                        | FF_336Ch                  | R/W / R          | 0062_0204h on nSIO_RESET | BAR for ACPI EC Interface 1<br>(See Note 6.2 on page 147) |
| 70h - 73h                                                                                      | FF_3370h                  | R/W / R          | 0062_0307h on nSIO_RESET | BAR for ACPI EC Interface 2<br>(See Note 6.3 on page 147) |
| 74h - 7Fh                                                                                      | FF_3374h                  | R/W / R          | 0062_0407h on nSIO_RESET | BAR for ACPI EC Interface 3<br>(See Note 6.3 on page 147) |
| 78h - 7Bh                                                                                      | FF_3378h                  | R/W / R          | 0000_0507h on nSIO_RESET | BAR for ACPI PM1 Interface                                |
| 7Ch - 7Fh                                                                                      | FF_337Ch                  | R/W / R          | 0000_0607h on nSIO_RESET | BAR for UART                                              |
| 80h - 83h                                                                                      | FF_3380h                  | R/W / R          | 0092_0700h on nSIO_RESET | BAR for Legacy (Fast KYBD) Interface                      |
| 84h - 87h                                                                                      | FF_3384h                  | R/W / R          | 0000_0E04h on nSIO_RESET | BAR for Embedded Flash Interface                          |
| <b>Configuration Registers for LDN Eh (Embedded Flash) at AHB base address FF_3800h</b>        |                           |                  |                          |                                                           |
| -                                                                                              | -                         | -                | -                        | None                                                      |
| <b>Configuration Registers for LDN 3Fh (Global Configuration) at AHB base address FF_FC00h</b> |                           |                  |                          |                                                           |
| 00h - 02h                                                                                      | FF_FF00h<br>-<br>FF_FF02h | -                |                          | Reserved                                                  |
| 03H                                                                                            | FF_FF03                   | -                | -                        | SMSC Reserved                                             |
| 04h - 06h                                                                                      | FF_FF04h<br>-<br>FF_FF06h | -                | 00h on nSIO_RESET        | Reserved                                                  |

**Table 6.14 MEC5035 Configuration Register Map (continued)**

| LPC CR INDEX        | AHB OFFSET                | TYPE<br><a href="#">Note 6.2</a> | RESET <a href="#">Note 6.3</a>    | CONFIGURATION REGISTER NAME                                                                     |
|---------------------|---------------------------|----------------------------------|-----------------------------------|-------------------------------------------------------------------------------------------------|
| <a href="#">07h</a> | FF_FF07h                  | R/W                              | -                                 | <a href="#">Logical Device Number</a>                                                           |
| 08h - 1Fh           | FF_FF08h<br>-<br>FF_FF1Fh | -                                | 46h<br>hardwired                  | Reserved                                                                                        |
| <a href="#">20h</a> | FF_FF20h                  | R                                | Current Revision<br>hardwired     | <a href="#">Device ID</a>                                                                       |
| <a href="#">21h</a> | FF_FF21h                  | R                                | N/A                               | <a href="#">Device Revision</a> A read-only register which provides device revision information |
| 22h– 23h            | FF_FF22h<br>-<br>FF_FF23h | -                                | 04h on <a href="#">nSIO_RESET</a> | SMSC Reserved                                                                                   |
| <a href="#">24h</a> | FF_FF24h                  | R/W                              | 00h                               | <a href="#">Device Mode</a>                                                                     |
| 25h – 2Fh           | FF_FF25h<br>-<br>FF_FF2Fh | -                                |                                   | SMSC Reserved                                                                                   |

**Note 6.2** R/W / R means that some parts of a register are read/write and some parts are read-only

**Note 6.3** Resets are defined in [Chapter 4, Power, Clocks and Resets: nSYS\\_RST on page 101](#) and [nSIO\\_RESET on page 76](#).

## 6.11 Chip-Level (Global) Control/Configuration Registers [00h - 2Fh]

The chip-level (global) registers reside in Logical Device 3Fh at AHB addresses FF\_FF00h through FF\_FF2Fh. All unimplemented registers and bits ignore writes and return zero when read. The global registers are accessed in the configuration address range [00h - 2Fh] in all Logical Devices. There is no Activate associated with Logical Device 3Fh: the Global Configuration Registers are always accessible.

As with all Configuration Registers, the INDEX PORT is used to select a Global Configuration Register in the chip. The DATA PORT is then used to access the selected register.

The Host can access all the Global Configuration registers at the offsets listed in [Table 6.16, "Chip-Level \(Global\) Control/Configuration Registers"](#) through the INDEX PORT and the DATA PORT. The EC can access all these registers at the listed offsets from the AHB Base Address shown in [Table 6.15, "Global Configuration Register Base Address"](#).

**Table 6.15 Global Configuration Register Base Address**

| Logical Device Range | AHB Address Base |
|----------------------|------------------|
| 3FH                  | FF_FC00          |

The EC can access all these registers at the addresses listed in [Table 6.14, "MEC5035 Configuration Register Map," on page 154](#).



**Table 6.16 Chip-Level (Global) Control/Configuration Registers**

| REGISTER                               | OFFSET    | DESCRIPTION                                                                                                                                                                                                                                  |
|----------------------------------------|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>CHIP (GLOBAL) CONTROL REGISTERS</b> |           |                                                                                                                                                                                                                                              |
| Reserved                               | 00h-03h   | Reserved, Writes are ignored, reads return 0.                                                                                                                                                                                                |
| Reserved                               | 04h - 06h | Reserved - Writes are ignored, reads return 0.                                                                                                                                                                                               |
| Logical Device Number                  | 07h       | A write to this register selects the current logical device. This allows access to the control and configuration registers for each logical device.<br><b>Note:</b> The Activate command operates only on the selected logical device.       |
| Reserved                               | 08h - 1Fh | Reserved - Writes are ignored, reads return 0.                                                                                                                                                                                               |
| Device ID<br>Hard Wired                | 20h       | A read-only register which provides device identification:<br>Bits[7:0] = 46h                                                                                                                                                                |
| Device Revision<br>Hard Wired          | 21h       | A read-only register which provides device revision information.<br>Bits[7:0] = current revision when read                                                                                                                                   |
| Reserved                               | 22h - 23h | Reserved - Writes are ignored, reads return 0.                                                                                                                                                                                               |
| Device Mode                            | 24h       | Bit [1:0] Reserved – writes ignored, reads return “0”.<br>Bit[2] SerIRQ Mode<br>( <a href="#">Note 6.4</a> )<br>= 0: Serial IRQ Disabled.<br>= 1: Serial IRQ Enabled<br>(Default).<br>Bit [7:3] Reserved – writes ignored, reads return “0”. |
| Reserved                               | 25h - 27h | Reserved - Writes are ignored, reads return 0.                                                                                                                                                                                               |
| Test Register                          | 28h       | SMSC Test Mode Register, Reserved for SMSC                                                                                                                                                                                                   |
| Test Register                          | 29h       | SMSC Test Mode Register, Reserved for SMSC                                                                                                                                                                                                   |
| Reserved                               | 2Ah - 2Bh | Reserved - Writes are ignored, reads return 0.                                                                                                                                                                                               |
| Test Register                          | 2Ch       | SMSC Test Mode Register, Reserved for SMSC                                                                                                                                                                                                   |
| Test Register                          | 2Dh       | SMSC Test Mode Register, Reserved for SMSC                                                                                                                                                                                                   |
| Test Register                          | 2Eh       | SMSC Test Mode Register, Reserved for SMSC                                                                                                                                                                                                   |
| Test Register                          | 2Fh       | SMSC Test Mode Register, Reserved for SMSC                                                                                                                                                                                                   |

**Note 6.4** The SerIRQ Mode bit controls the SER\_IRQ pin, the CLKRUN# pin and the affects of LPC DMA requests on CLKRUN# (See [Section 5.7](#), on [page 125](#) and [Section 5.8](#), on [page 128](#)).



## 6.12 Logical Device Configuration Revision History

This revision history shows the changes made to this chapter.

**Table 6.17 Logical Device Configuration Chapter Revision History**

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History," on page 539.</a> |              |      |                                                                                                                                                                                                                                                                                                       |                                                                                                                                                                                                                                                                                                                                                                     |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE | SECTION/FIGURE/ENTRY                                                                                                                                                                                                                                                                                  | CORRECTION                                                                                                                                                                                                                                                                                                                                                          |
| 1.                                                                                                                                                                                                                                          |              |      | <a href="#">Configuration Registers for LDN Ch (LPC Interface) at AHB base address FF_3000h on page 155</a><br><br><a href="#">DMA Channel 4 (Reserved) on page 148</a><br><a href="#">Note 6.5 on page 149</a><br><br><a href="#">Table 6.14 on page 154</a><br><a href="#">Note 6.3 on page 157</a> | Remove spec conflict all DMA Configuration Register default to 00.<br><a href="#">DMA Channel 4 (Reserved)</a> read-only Bug 251<br><br>address FF_3358h is read only 0000.<br>DMA Chan 4 not claimed by MEC5035.<br><br>Define all resets in CR space. In LDN Ch Activate reg is <a href="#">nSYS_RST</a> and every other register is <a href="#">nSIO_RESET</a> . |
| 2.                                                                                                                                                                                                                                          |              |      |                                                                                                                                                                                                                                                                                                       |                                                                                                                                                                                                                                                                                                                                                                     |
| 3.                                                                                                                                                                                                                                          |              |      | <a href="#">Table 6.6 on page 147</a><br><a href="#">Note 6.2 on page 147</a><br><a href="#">Note 6.3 on page 147</a><br><a href="#">Table 6.14 on page 154</a><br><br><a href="#">Table 6.14 on page 154</a><br><br><a href="#">Section 6.8, "SERIRQ Interrupts," on page 150</a>                    | The ACPI EC Channel 1 BAR at AHB address FF_336Ch default value is changed to 0062_0204h. Further, the Mask field in the BAR should be changed from a fixed value to a variable value.<br><br>The Embedded Flash Interface BAR at AHB address FF_3384h default value is changed to 0000_0E04h.<br><br>Rewritten for clarity: no design changes                      |
| 4.                                                                                                                                                                                                                                          |              |      |                                                                                                                                                                                                                                                                                                       |                                                                                                                                                                                                                                                                                                                                                                     |





## Chapter 7 Bus Hierarchy

### 7.1 General Description

All devices on the MEC5035 are maintained in a common address space. All communication with on-chip functions is through registers that have addresses in this common address space. The ARC Embedded Controller (EC) can reference all devices through the address space, while the Host can only reference a subset.

### 7.2 Block Diagram

[Figure 7.1 Bus Hierarchy on page 163](#) shows, in graphic form, the inter connectivity of devices on the MEC5035, including the EC, the principal lower buses and most of the peripherals.

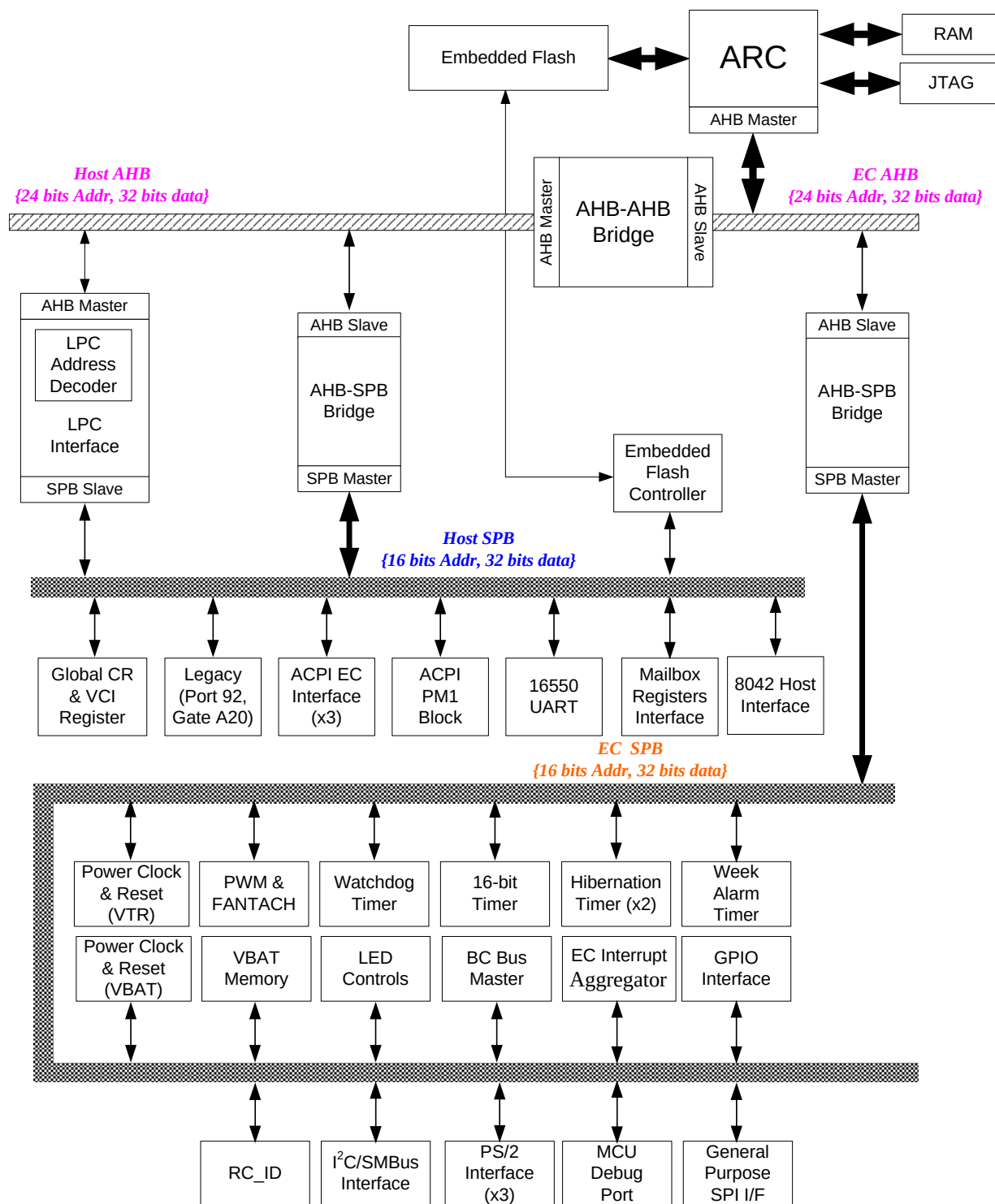


Figure 7.1 Bus Hierarchy

## 7.3 Address Space

The ARC EC has a 24-bit address space. Addresses in the lower half of the range, 0h through 7F\_FFFFh, can be used for both instruction access and data access. The address range 0h through 4\_FFFFh (which includes the 192KB Flash Memory Array and an additional 2KB Flash Info Block) is

mapped to the [Embedded Flash Subsystem](#). Addresses in the range 80\_0000h through 80\_0FFFh are mapped to the Closely Coupled Data Memory. These memories are shown in [Figure 7.1](#). Software can change the address mapping so that the Closely Coupled Data Memory is mapped to 6\_0000h through 6\_0FFFh, where it can be used for both instructions and data, and the [Embedded Flash Subsystem](#) becomes accessible only through a register interface. Addresses greater or equal to 80\_1000h are propagated through the AHB interface on the ARC processor. References, by either the EC or the Host via the LPC bus, to addresses that are not mapped to any device register or memory will cause a bus error; see [Section 7.4.3, "AHB Bus Errors," on page 170](#).

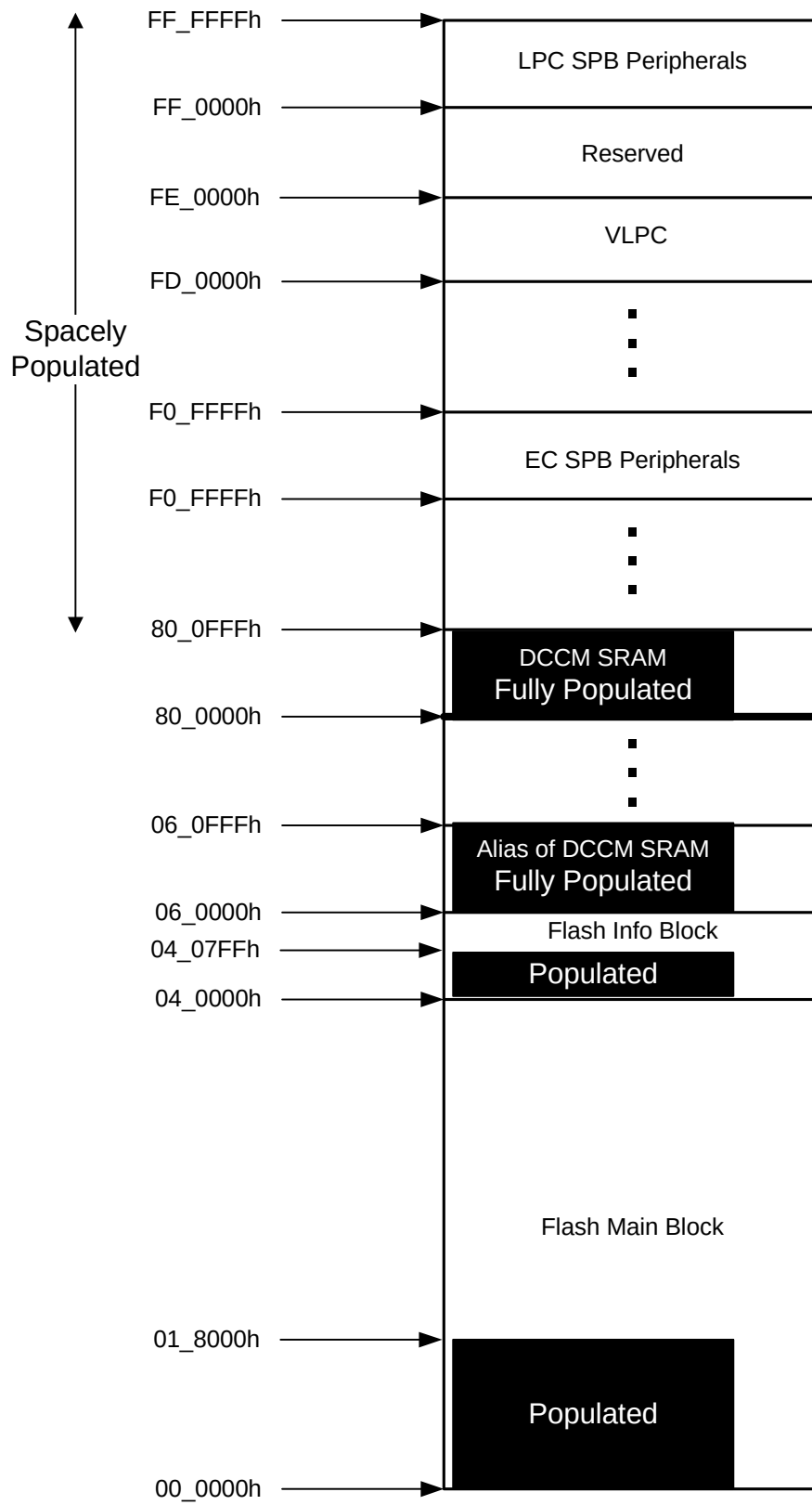
### 7.3.1 ARC Address Space

The [ARC Address Space](#) is illustrated in [Figure 7.1, "Bus Hierarchy"](#). [EC Instruction Memory](#) occupies the lower half of the address space, 00\_0000h through 7F\_FFFFh. The ARC processor can only execute instructions that are located in the Instruction Memory portion of the address space. Only a portion of the Instruction space is populated.

The upper half of the address space is used solely for data references. The region contains a general-purpose [EC Data Memory](#) SRAM, as well as the address space of the two SPB peripheral buses.

The contents of the Instruction memory can be read and written by the ARC processor through regular load and store instructions. However, there may be a one cycle instruction fetch penalty whenever a data load or store instruction to Instruction memory is executed.

## Product Customer Specification-ODM





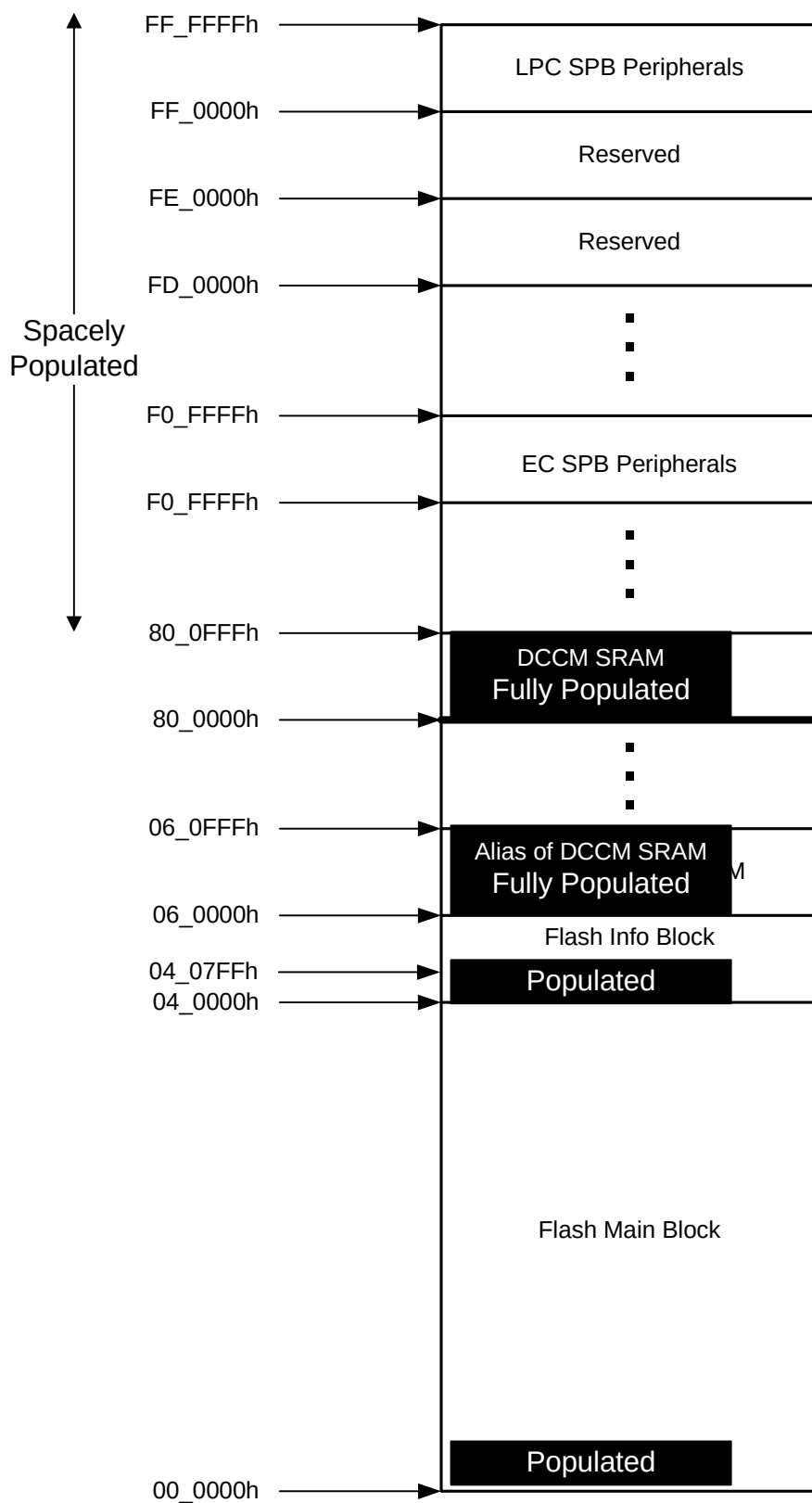


Figure 7.2 MEC5035 EC Memory Map



## 7.3.2 AHB Address Space

The components on the AHB subsystem and the two SPB bridges define a set of addresses that are accessible by the EC. This address space is shown in [Table 7.1, "MEC5035 AHB Address Space"](#). As shown in the table, the Host can access much of the address space, but not all.

**Table 7.1 MEC5035 AHB Address Space**

| ADDRESS RANGE       | DEVICE              | ACCESSIBLE BY EC | ACCESSIBLE BY HOST                 |
|---------------------|---------------------|------------------|------------------------------------|
| F0_0000h - F0_FFFFh | ARC-only SPB Bridge | Yes              | No                                 |
| FF_0000h - FF_FFFFh | LPC SPB Bridge      | Yes              | Yes (limited by LPC interface map) |

Each 64KB address space of an SPB Bridge is divided into 1KB Frames. Peripherals are grouped into Logical Devices; each Logical Device corresponds to a 1KB Frame. Logical Devices addressable by the Host are listed in [Table 7.2, "Host Logical Devices on MEC5035"](#). The 1KB Address Frame of a Host Logical Device is divided into four subregions, as described in [Section 7.4.2, "Address Framing," on page 169](#)

**Table 7.2 Host Logical Devices on MEC5035**

| Logical Device Number | Logical Devices            | AHB Address of Frame | Runtime Registers | Configuration Registers | EC-only Registers |
|-----------------------|----------------------------|----------------------|-------------------|-------------------------|-------------------|
| 0h                    | Mailbox Interface          | FF_0000h             | yes               | yes                     | yes               |
| 1h                    | Keyboard Controller (8042) | FF_0400h             | yes               | yes                     | no                |
| 2h                    | ACPI EC Channel 1          | FF_0800h             | yes               | yes                     | no                |
| 3h                    | ACPI EC Channel 2          | FF_0C00h             | yes               | yes                     | no                |
| 4h                    | ACPI EC Channel 3          | FF_1000h             | yes               | yes                     | no                |
| 5h                    | ACPI PM1                   | FF_1400h             | yes               | yes                     | no                |
| 6h                    | UART                       | FF_1800h             | yes               | yes                     | no                |
| 7h                    | Legacy (Fast KB)           | FF_1C00h             | yes               | yes                     | no                |
| Ch                    | LPC Interface              | FF_3000h             | no                | yes                     | yes               |
| Eh                    | Embedded Flash Interface   | FF_3800h             | yes               | yes                     | yes               |
| 3Fh                   | Global Configuration       | FF_FC00h             | no                | no                      | yes               |

The 64KB address space of the ARC-only SPB Bridge is divided into 1KB Frames. Peripherals are grouped into Logical Devices; each Logical Device corresponds to a 1KB Frame. These EC Logical Devices addressable by the ARC-only are listed in [Table 7.3, "EC Logical Devices on MEC5035"](#). Multiple instantiations of the same block are in a single 1KB Frame. Each instantiation is separated by 128 bytes.

**Note 7.3** All VBAT powered registers are in a Single 1KB Frame separated by 128 bytes (see [Table 7.3](#), Logical Device Number 33h.)

**Note 7.4** The [VBAT-Powered Control Interface](#) is in the Global Configuration Logical Device, Host Logical Device Number 3Fh, in EC-only space (see [Section 7.4.2, "Address Framing," on page 169](#)).

Note that the ARC-only SPB Bridge address space uses the terminology of Logical Device; however, there is no host access to these blocks.

**Table 7.3 EC Logical Devices on MEC5035**

| Logical Device Number | AHB Address for Base of Frame | Logical Devices                    | Notes                    |
|-----------------------|-------------------------------|------------------------------------|--------------------------|
| 0h                    | F0_0000h                      | Hibernation Timer                  |                          |
| 1h                    | F0_0400h                      | Watchdog Timer                     |                          |
| 2h                    | F0_0800h                      | Reserved                           |                          |
| 3h                    | F0_0C00h                      | 16-bit Timer                       |                          |
| 4h                    | F0_1000h                      | RC ID                              |                          |
| 5h                    | F0_1400h                      | BC Bus Master                      |                          |
| 6h                    | F0_1800h                      | SMBus                              |                          |
| 7h                    | F0_1C00h                      | General Purpose SPI Peripheral     |                          |
| 8h - 15h              | F0_2000h - F0_4FFFh           | Reserved                           |                          |
| 16h                   | F0_5800h                      | PWM                                |                          |
| 17h                   | F0_5C00h                      | TACH                               |                          |
| 18h - 20h             | F0_6000h - F0_83FFh           | Reserved                           |                          |
| 21h                   | F0_8400h                      | LED                                |                          |
| 22h                   | F0_8800h                      | PS/2                               |                          |
| 23h                   | F0_8C00h                      | MCU Debug Port                     |                          |
| 24h - 2Fh             | F0_9000h - F0_BCFFh           | Reserved                           |                          |
| 30h                   | F0_C000h                      | EC Interrupt Aggregator            |                          |
| 31h                   | F0_C400h                      | GPIOs                              |                          |
| 32h                   | F0_C800h                      | Power, Clock & Reset (VTR PWR'ed)  |                          |
| 33h                   | F0_CC00h                      | Power, Clock & Reset (VBAT PWR'ed) | <a href="#">Note 7.3</a> |
|                       | F0_CC80h                      | Week Alarm Timer                   |                          |
|                       | F0_CD00h                      | VBAT Backed Memory                 |                          |
| 35h - 3Fh             | F0_D400h - F0_FFFFh           | Reserved                           |                          |

## 7.4 AHB Buses

Addresses and internal buses in the MEC5035 are compatible with ARM Limited's *Advanced Microprocessor Bus Architecture* (AMBA), as specified in *AMBA™ Specification (Rev 2.0)*, 1999.

As seen in [Figure 7.1 Bus Hierarchy on page 163](#), there are two separate AHB buses, the EC AHB and the Host AHB. The first has one master, the EC, and two slaves, while the second has two masters, the LPC interface and the AHB-AHB bridge, and three slaves. The bus connections are summarized in [Table 7.4, "MEC5035 AHB Buses"](#) and can be seen in [Figure 7.1](#).

**Table 7.4 MEC5035 AHB Buses**

| AHB BUS  | MASTER INTERFACES               | SLAVE INTERFACES                |
|----------|---------------------------------|---------------------------------|
| EC AHB   | EC                              | EC SPB bridge<br>AHB-AHB bridge |
| Host AHB | LPC Interface<br>AHB-AHB bridge | LPC SPB bridge<br>SPI bridge    |

The AHB-to-AHB bridge is a one-way device: addresses generated on the EC AHB can be propagated to the Host AHB bus, but addresses on the Host AHB bus cannot be propagated to the EC AHB bus. This is the reason that the Host is restricted from accessing the address range F0\_0000h to F0\_FFFFh (the address range of the EC SPB bridge). The bridge maps address from FD\_0000h through FF\_FFFFh. Multi-word block transfers on the EC AHB (for example, the 16-byte memory fetch to fill a cache line) are converted by the bridge into a series of sequential 4-byte transfers.

Both the EC and the LPC interface can have at most one outstanding AHB bus request at one time. On the Host AHB, the LPC interface always has priority over the AHB-AHB bridge. Both AHB buses support byte, halfword and word AHB transfers. The only Burst mode supported on the EC AHB is an incrementing burst of 4 beats of 4 bytes per beat. Burst mode is not supported on the Host AHB. AHB bus locking or early burst termination are not supported.

### 7.4.1 Bus Clocking

The Host AHB runs at the MEC5035 system clock rate of 64.52 MHz. The bus clock and the bus arbiter will be shut down when there are no transactions active on the bus. The bus clock and arbiter will be restarted as soon as an address is acquired from the LPC bus, or when an EC AHB bus transaction is mapped, via the AHB-to-AHB bridge, to the address space of the Host AHB. The EC AHB clock can be programmed to run at any of the available rates between 250KHz and 21.5MHz; see [Chapter 4, "Power, Clocks and Resets," on page 74](#). The EC bus clock is shut down when the EC is idle.

If the Host AHB clock is idle when an LPC transaction arrives at the LPC interface, the LPC interface will restart the AHB bus clock and arbiter early enough so that as soon as an I/O address is translated to an AHB address the I/O transaction can be placed on the AHB without delay. If the I/O address is not claimed by the MEC5035 then the LPC interface will drop its bus request. If the EC is not requesting the Host AHB at the same time, the Host AHB bus clock will again shut down.

### 7.4.2 Address Framing

The EC can directly address all peripherals on the MEC5035. The Host, by contrast, is restricted in what it can address. The Host accesses the MEC5035 through the LPC bus, using I/O cycles, Memory Cycles and Firmware Hub cycles (see [Chapter 5, "Host Interface," on page 120](#)). These cycles are mapped into the MEC5035 address space accessible by the LPC interface.

The mapping function forces some of the address bits to preset values, as shown in [Table 7.5, "LPC to MEC5035 Address Mapping"](#). This mapping has the effect of creating four contiguous 256-byte regions: LPC I/O, EC-only, LPC DMA and LPC Configuration. Together, the four regions create a 1024

byte “frame” for each logical device that is accessible to the Host. There is therefore a maximum of 64 Logical Devices, each with a 1KB frame, located on the basechip.

LPC I/O cycles for Runtime Registers are mapped into the first 256 bytes of the 1024 byte frame. Each byte of LPC I/O space is mapped to a 4-byte word in the 1024 byte frame, so at most 64 bytes of LPC I/O space per logical device can be used as Runtime Registers (which map into 256 bytes of MEC5035 address space). Configuration Registers, which are accessed through a Configuration portal typically located at addresses 2Eh and 2Fh in the LPC I/O space, are restricted to the highest 256 bytes of the 1024 byte frame.

DMA FIFO addresses are restricted to offsets between 200h and 2FFh within a Logical Device frame. In addition, DMA FIFO addresses are restricted to 32-bit aligned addresses, that is, address bits [1:0] are both 0. The low 10 bits of a DMA FIFO are thus in the form ‘10xxxxxx00b’.

LPC Firmware Hub cycles and LPC Memory cycles are mapped into the address range 80\_0000h to FF\_FFFFh. This range is mapped into the off-chip SPI Flash memory.

Because the EC does not require the mapping mechanism required for translating LPC Runtime Registers, Configuration Registers and DMA channels, it accesses each 1KB frame uniformly. All Logical Devices located on the EC-only AHB (those in the address range F0\_0000h through F0\_FFFFh) have a flat, 1KB frame.

For details on LPC address mapping to the MEC5035 address space, see [Chapter 5, "Host Interface," on page 120](#).

**Table 7.5 LPC to MEC5035 Address Mapping**

| TYPE OF ACCESS                                                              | ADDRESS BIT MAPPING                                                                    |
|-----------------------------------------------------------------------------|----------------------------------------------------------------------------------------|
| LPC I/O Access<br>Runtime Registers                                         | Address bits[9:8] = 00b<br>Address bits[1:0] = 00b<br>Address bits[23:10] set from map |
| No LPC Access<br>EC-only registers                                          | Address bits[9:8] = 01b                                                                |
| LPC I/O Access through Configuration Access Port<br>Configuration Registers | Address bits[9:8] = 11b<br>Address bits[23:10] set from map                            |
| LPC DMA Access                                                              | Address bits[9:8] = 10b<br>Address bits[23:10] set from map                            |

### 7.4.3 AHB Bus Errors

AHB bus requests by both the Host, through the LPC bus, and the EC, can be terminated with an AHB bus error. The handling of bus errors by the EC is described in the *ARCompact™ Instruction Set Architecture: Programmer's Reference*.

Bus errors may be caused by:

- EC I/O requests that lie outside the range of the Data Closely Coupled Memory, the EC SPB or the AHB-AHB bridge
- I/O requests to either the Host SPB or the EC SPB that map to a non-existent Logical Device
- I/O requests to an invalid register address within a valid Logical Device on either the EC SPB or the Host SPB

## 7.5 SMSC Peripheral Buses (SPB)

The SMSC Peripheral Bus (SPB) is a byte-addressable bus with a 16-bit address space and a 32-bit data path. All accesses must be aligned to the data-size boundaries. The SPB supports 32-bit, 16-bit

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and 8-bit accesses. All peripheral accesses are 32-bits wide, so that if a peripheral cannot transfer more than 8 bits of a register in one I/O access, register addresses should all be on 32-bit boundaries even though the upper bits (bits 31 through 8) are always zero. The SPB will not assemble a 32-bit word out of multiple 8-bit accesses.

SPB transfers take two cycles, so that a read or write on the AHB to a register on the SPB will take a total of three cycles. The SPB contains an 8-bit word address, four byte lane strobes and up to 64 logical device select strobes. Data on the SPB read and write buses are always 32-bit aligned, with the byte strobes indicating which byte lane or lanes should be active during a transaction. An SPB peripheral must steer bytes, based on the byte strobes, to the correct byte lane.

There are two SPB bridges forwarded to two SPB (busses):

*LPC SPB*

The LPC SPB address range is FF\_0000h through FF\_FFFFh

*EC SPB*

The EC SPB address range is F0\_0000h through F0\_FFFFh

The SPB bridges claim all addresses within their 64KB address space. If an AHB master attempts to access an address within an SPB bridge address space that is not assigned to a Logical Device, the master's access will be terminated with a bus error. In addition, an access to an invalid address within a valid Logical Device will be terminated with a bus error.

## 7.6 Bus Hierarchy Revision History

This revision history shows the changes made to this chapter.

**Table 7.6 Bus Hierarchy Chapter Revision History**

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History," on page 539.</a> |              |           |                                                      |                                                                                                                                                                                                                           |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|-----------|------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE      | SECTION/FIGURE/ENTRY                                 | CORRECTION                                                                                                                                                                                                                |
| 1.                                                                                                                                                                                                                                          |              |           | <a href="#">Table 7.2 &amp; Table 7.3</a>            | LDN= EC 3F changed to reserved.<br>Renamed LD's: "EC Interrupt Aggregator" Embedded Flash Controller, GPSPI Promulgated elsewhere in spec via xref.                                                                       |
| 2.                                                                                                                                                                                                                                          |              |           | <a href="#">Figure 7.1 Bus Hierarchy on page 163</a> | Added JTAG interface<br>Breakout PCR VTR & VBAT<br>Renamed GPSPI, Embedded Flash Controller<br>Added Global CR & VCi Reg<br>Removed duplicate "Interrupt reg" & VBAT logic<br>Added instances to PS/2 & Hibernation timer |
| 3.                                                                                                                                                                                                                                          |              |           |                                                      |                                                                                                                                                                                                                           |
| 4.                                                                                                                                                                                                                                          | 0.6          | 7/26/2007 | <a href="#">Figure 7.1, "Bus Hierarchy"</a>          | Added indication of "populated" Flash & SRAM.                                                                                                                                                                             |

## Chapter 8 MailBox Register Interface

### 8.1 General Description

The [MailBox Register Interface](#) provides a standard run-time mechanism for the host to communicate with the Embedded Controller (EC) and other logical components in the MEC5035. Block Diagram. The Mailbox Registers Interface includes a total of 36 index-addressable 8-bit registers and a [Mailbox Registers Interface Host Access Port](#). Thirty-two of 36 index-addressable 8-bit registers are EC Mailbox registers. The [Mailbox Registers Interface Host Access Port](#) consists of two 8-bit run-time registers that occupy two addresses in the HOST I/O space. The [Mailbox Registers Interface Host Access Port](#) is used by the host to access the 36 index-addressable 8-bit registers.

**Note:** In this specification, host access to registers in the Mailbox Registers Interface through the host access port are identified by the prefix MBX in front of a hexadecimal index address.

#### 8.1.1 Block Diagram

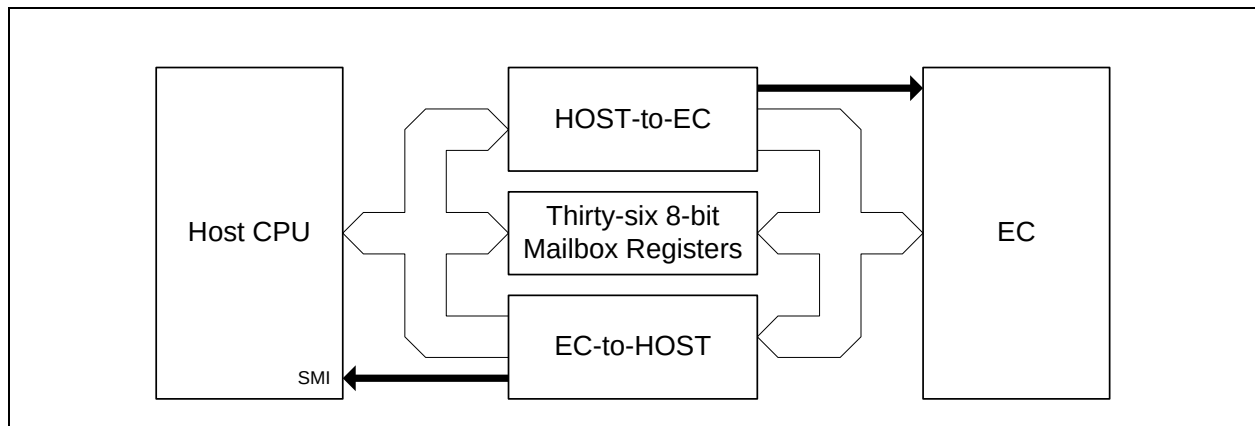


Figure 8.1 MailBox Block Diagram

### 8.2 Power, Clocks and Reset

#### 8.2.1 Power Domain

This block is powered by the VTR power supply.

See [Section 4.5, "Power Configuration," on page 96](#) for details on power domains.

#### 8.2.2 Clocks

This block has one clock input, the [LPC Bus Clock](#).

See [Section 4.4, "Clock Generator," on page 77](#) for details on clocks.

#### 8.2.3 Reset

This block is reset when [nSYS\\_RST](#) is asserted.

In addition the [MBX\\_INDEX Register](#) & [MBX\\_DATA Register](#) are reset when [VCC\\_PWRGD](#) Signal Pin function is deasserted.

See [Section 4.6, "Reset Interface," on page 99](#) for details on reset.

## 8.3 Interrupts

The [MailBox Register Interface](#) can generate an interrupt event for the HOST-to-EC events. See [HOST-to-EC Mailbox Register on page 178](#). The interrupt source is routed onto the [MBX](#) bit in the [IRQ17 Source Register](#) and is a level, active high signal.

### 8.3.1 MailBox Register Interface (LDN 0h) SIRQ Routing

The [MailBox Register Interface](#) can generate a SIRQ event for the EC-to-HOST EC events. See [HOST-to-EC Mailbox Register on page 178](#). This interrupt is routed to the SIRQ block (see [SERIRQ Configuration Registers on page 150](#)). For this interrupt, the [SELECT on page 151](#) is cleared to '0' in the Interrupt Configuration Register for the selected SIRQ frame.

The [MailBox Register Interface](#) can generate a SMI event from the [SMI Interrupt Source Register on page 179](#). The SMI event can be routed to any frame in the SIRQ stream and to the nSMI pin. To enable SMI routing to the SIRQ stream, the bit [SELECT on page 151](#) is set to '1' in the Interrupt Configuration Register for the selected SIRQ frame. The SMI event can be routed to nSMI pin by selecting the nSMI signal function in the associated [Pin Control Register on page 376](#).

The SMI event produces a standard active low on the serial IRQ stream and active low on the open drain nSMI pin. See [Figure 8.1 Mailbox SIRQ and SMI routing on page 173](#).

See [Section 6.8.1, "SERIRQ Configuration Registers," on page 150](#).

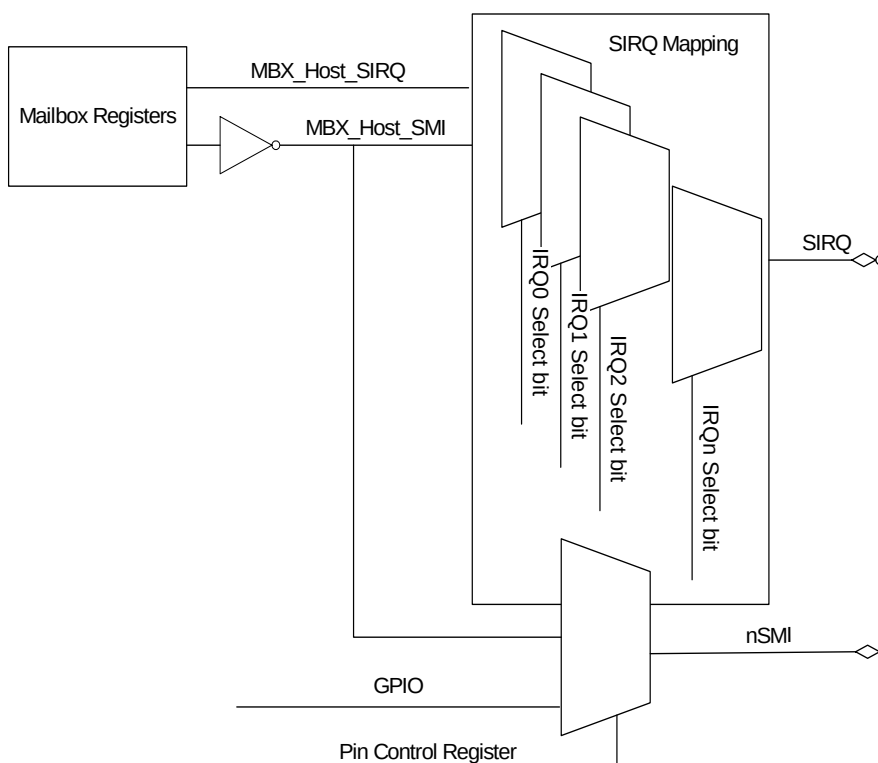


Figure 8.1 Mailbox SIRQ and SMI routing

## 8.4 Registers

The [MailBox Register Interface](#) has its own Logical Device Number, and Base Address as indicated in [Table 8.1](#). The Host LPC I/O addresses for the [MailBox Register Interface](#) are selected via a Base



Address Register (see [Section 6.6.2, "Base Address Registers," on page 144](#)). LPC access to configuration registers is through Host Access Configuration Port (see [Section 6.5.1, "Host Access Port," on page 142](#).)

[Table 8.2](#) is a register summary for the [MailBox Register Interface](#) block.

**Table 8.1 MailBox Register Interface Base Address Table**

| <a href="#">MailBox Register Interface</a><br>INSTANCE | LDN<br>FROM<br>( <a href="#">Table 7.2</a><br>on<br>page 167) | AHB BASE ADDRESS |
|--------------------------------------------------------|---------------------------------------------------------------|------------------|
| <a href="#">Mailbox Interface</a>                      | 0h                                                            | FF_0000h         |

**Note:** The Host LPC I/O addresses for this instance is selected via a Base Address Register (see [Section 6.6.2, "Base Address Registers," on page 144](#)). LPC access to configuration registers is through the Host Access Configuration Port (see [Section 6.5.1, "Host Access Port," on page 142](#).)

The [Table 8.2](#) is a register summary for one instance of the [MailBox Register Interface](#). The LPC I/O address for each Run-Time Register is described below as an offset from its Base Address Register. Each EC address is indicated as an SPB Offset from its AHB base address. Each Configuration register is accessed through the [Host Access Port](#) is via its LDN indicated in [Table 8.1 on page 174](#) and its [Host Access Port](#) index which is described as "Host Config Index" in the tables below.



Table 8.2 MailBox Register Interface Register Summary

|     |                                               | HOST I/O ACCESS      |            |                           | EC INTERFACE |           |                           | NOTES                    |
|-----|-----------------------------------------------|----------------------|------------|---------------------------|--------------|-----------|---------------------------|--------------------------|
|     | REGISTER NAME                                 | HOST I/O INDEX       | SPB OFFSET | HOST TYPE                 | SPB OFFSET   | BYTE LANE | EC TYPE                   |                          |
|     | <a href="#">MBX_INDEX Register</a>            | 00h                  | 00h        | R/W                       | -            | -         | -                         |                          |
|     | <a href="#">MBX_DATA Register</a>             | 01h                  | 01h        | R/W                       | -            | -         | -                         |                          |
|     |                                               | <b>MAILBOX INDEX</b> |            |                           |              |           |                           |                          |
| 1.  | <a href="#">HOST-to-EC Mailbox Register</a>   | MBX 00h              | -          | R/W                       | 100h         | 0         | R/WC                      | <a href="#">Note 8.2</a> |
| 2.  | <a href="#">EC-to-Host Mailbox Register</a>   | MBX 01h              | -          | R/WC                      | 104h         | 0         | R/W                       | <a href="#">Note 8.3</a> |
| 3.  | <a href="#">SMI Interrupt Source Register</a> | MBX 02h              | -          | <a href="#">Table 8.7</a> | 108h         | 0         | <a href="#">Table 8.7</a> |                          |
| 4.  | <a href="#">SMI Interrupt Mask Register</a>   | MBX 03H              | -          | R/W                       | 10Ch         | 0         | R/W                       |                          |
| 5.  | <b>Mailbox register [0]</b>                   | MBX10h               | -          | R/W                       | 110h         | 0         | R/W                       |                          |
| 6.  | <b>Mailbox register [1]</b>                   | MBX11h               | -          |                           |              | 1         |                           |                          |
| 7.  | <b>Mailbox register [2]</b>                   | MBX12h               | -          |                           |              | 2         |                           |                          |
| 8.  | <b>Mailbox register [3]</b>                   | MBX13h               | -          |                           |              | 3         |                           |                          |
| 9.  | <b>Mailbox register [4]</b>                   | MBX14h               | -          | R/W                       | 114h         | 0         | R/W                       |                          |
| 10. | <b>Mailbox register [5]</b>                   | MBX15h               | -          |                           |              | 1         |                           |                          |
| 11. | <b>Mailbox register [6]</b>                   | MBX16h               | -          |                           |              | 2         |                           |                          |
| 12. | <b>Mailbox register [7]</b>                   | MBX17h               | -          |                           |              | 3         |                           |                          |
| 13. | <b>Mailbox register [8]</b>                   | MBX18h               | -          | R/W                       | 118h         | 0         | R/W                       |                          |
| 14. | <b>Mailbox register [9]</b>                   | MBX19h               | -          |                           |              | 1         |                           |                          |
| 15. | <b>Mailbox register [A]</b>                   | MBX1Ah               | -          |                           |              | 2         |                           |                          |
| 16. | <b>Mailbox register [B]</b>                   | MBX1Bh               | -          |                           |              | 3         |                           |                          |
| 17. | <b>Mailbox register [C]</b>                   | MBX1Ch               | -          | R/W                       | 11Ch         | 0         | R/W                       |                          |
| 18. | <b>Mailbox register [D]</b>                   | MBX1Dh               | -          |                           |              | 1         |                           |                          |
| 19. | <b>Mailbox register [E]</b>                   | MBX1Eh               | -          |                           |              | 2         |                           |                          |
| 20. | <b>Mailbox register [F]</b>                   | MBX1Fh               | -          |                           |              | 3         |                           |                          |
| 21. | <b>Mailbox register [10]</b>                  | MBX20h               | -          | R/W                       | 120h         | 0         | R/W                       |                          |
| 22. | <b>Mailbox register [11]</b>                  | MBX21h               | -          |                           |              | 1         |                           |                          |
| 23. | <b>Mailbox register [12]</b>                  | MBX22h               | -          |                           |              | 2         |                           |                          |
| 24. | <b>Mailbox register [13]</b>                  | MBX23h               | -          |                           |              | 3         |                           |                          |

**Table 8.2 MailBox Register Interface Register Summary**

|     | REGISTER NAME         | HOST I/O ACCESS |            |           | EC INTERFACE |           |         | NOTES |
|-----|-----------------------|-----------------|------------|-----------|--------------|-----------|---------|-------|
|     |                       | HOST I/O INDEX  | SPB OFFSET | HOST TYPE | SPB OFFSET   | BYTE LANE | EC TYPE |       |
| 25. | Mailbox register [14] | MBX24h          | -          | R/W       | 124h         | 0         | R/W     |       |
| 26. | Mailbox register [15] | MBX25h          | -          |           |              | 1         |         |       |
| 27. | Mailbox register [16] | MBX26h          | -          |           |              | 2         |         |       |
| 28. | Mailbox register [17] | MBX27h          | -          |           |              | 3         |         |       |
| 29. | Mailbox register [18] | MBX28h          | -          | R/W       | 128h         | 0         | R/W     |       |
| 30. | Mailbox register [19] | MBX29h          | -          |           |              | 1         |         |       |
| 31. | Mailbox register [1A] | MBX2Ah          | -          |           |              | 2         |         |       |
| 32. | Mailbox register [1B] | MBX2Bh          | -          |           |              | 3         |         |       |
| 33. | Mailbox register [1C] | MBX2Ch          | -          | R/W       | 12Ch         | 0         | R/W     |       |
| 34. | Mailbox register [1D] | MBX2Dh          | -          |           |              | 1         |         |       |
| 35. | Mailbox register [1E] | MBX2Eh          | -          |           |              | 2         |         |       |
| 36. | Mailbox register [1F] | MBX2Fh          | -          |           |              | 3         |         |       |

**Note 8.2** Interrupt is cleared when read by the EC.

**Note 8.3** Interrupt is cleared when read by the host.

### 8.4.1 Mailbox Registers Interface Host Access Port

The Mailbox registers access port is two runtime registers that occupy two addresses in the Host I/O space: [MBX\\_INDEX Register](#) & [MBX\\_DATA Register](#).

To access a Mailbox register once the Mailbox Registers Interface Base Address has been initialized, write the Mailbox register index address to the MBX Index port and read or write the Mailbox register data from the MBX data port.

See [Table 8.2, "MailBox Register Interface Register Summary," on page 175.](#)

### 8.4.2 Mailbox Control Registers

Mailbox Register, HOST-to-EC, and Mailbox Register, EC-to-HOST, are specifically designed to pass commands between the host and the EC ([Figure 8.1 on page 172](#)). If enabled, these registers can generate interrupts.

Mailbox Register and Mailbox Register are not dual-ported, so the HOST BIOS and Keyboard BIOS must be designed to properly share these registers. When the host performs a write of the HOST-to-EC mailbox register, an interrupt will be generated and seen by the EC if unmasked. When the EC writes FF to the HOST-to-EC mailbox register, resets the register to 00h, providing a simple means for the EC to inform the host that an operation has been completed.

When the EC writes the EC-to-HOST mailbox register, an SMI may be generated and seen by the host if unmasked. When the Host CPU writes FFh to the EC-to-HOST mailbox register, the EC-to-HOST register resets to 00h, providing a simple means for the host to inform that EC that an operation has been completed.



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**PROGRAMMER'S NOTE:** The protocol used to pass commands back and forth through the Mailbox Registers Interface is left to the System designer. SMSC can provide an application example of working code in which the host uses the Mailbox registers to gain access to all of the EC registers.

## 8.5 Registers

### 8.5.1 Mailbox Index register

Table 8.3 MBX\_INDEX Register

|             |            |     |     |     |            |     |                                                |     |  |
|-------------|------------|-----|-----|-----|------------|-----|------------------------------------------------|-----|--|
| HOST OFFSET | 00h        |     |     |     | 8-Bit      |     | HOST SIZE                                      |     |  |
| EC OFFSET   | NA         |     |     |     |            |     | EC SIZE                                        |     |  |
| POWER       | VTR        |     |     |     | 00h<br>00h |     | nSYS_RST DEFAULT<br>&<br>VCC_PWRGD DEASSERTION |     |  |
| BUS         | LPC SPB    |     |     |     |            |     |                                                |     |  |
| BYTE0 BIT   | D7         | D6  | D5  | D4  | D3         | D2  | D1                                             | D0  |  |
| HOST TYPE   | R/W        | R/W | R/W | R/W | R/W        | R/W | R/W                                            | R/W |  |
| EC TYPE     | -          | -   | -   | -   | -          | -   | -                                              | -   |  |
| BIT NAME    | INDEX[7:0] |     |     |     |            |     |                                                |     |  |

### 8.5.2 Mailbox Data register

Table 8.4 MBX\_DATA Register

|             |           |     |     |     |            |     |                                                |     |  |
|-------------|-----------|-----|-----|-----|------------|-----|------------------------------------------------|-----|--|
| HOST OFFSET | 01        |     |     |     | 8-Bit      |     | HOST SIZE                                      |     |  |
| EC OFFSET   | NA        |     |     |     |            |     | EC SIZE                                        |     |  |
| POWER       | VTR       |     |     |     | 00h<br>00h |     | nSYS_RST DEFAULT<br>&<br>VCC_PWRGD DEASSERTION |     |  |
| BUS         | LPC SPB   |     |     |     |            |     |                                                |     |  |
| BYTE0 BIT   | D7        | D6  | D5  | D4  | D3         | D2  | D1                                             | D0  |  |
| HOST TYPE   | R/W       | R/W | R/W | R/W | R/W        | R/W | R/W                                            | R/W |  |
| EC TYPE     | -         | -   | -   | -   | -          | -   | -                                              | -   |  |
| BIT NAME    | DATA[7:0] |     |     |     |            |     |                                                |     |  |

### 8.5.3 HOST-to-EC Mailbox Register

Table 8.5 HOST-to-EC Mailbox Register

| HOST OFFSET | MBX_00h           |      |      | 8-Bit |      |      | HOST SIZE           |      |
|-------------|-------------------|------|------|-------|------|------|---------------------|------|
| EC OFFSET   | 100h              |      |      | 8-Bit |      |      | EC SIZE             |      |
| POWER       | VTR               |      |      | 00h   |      |      | nSYS_RST<br>DEFAULT |      |
| BUS         | LPC SPB           |      |      |       |      |      |                     |      |
| BYTE0 BIT   | D7                | D6   | D5   | D4    | D3   | D2   | D1                  | D0   |
| HOST TYPE   | R/W               | R/W  | R/W  | R/W   | R/W  | R/W  | R/W                 | R/W  |
| EC TYPE     | R/WC              | R/WC | R/WC | R/WC  | R/WC | R/WC | R/WC                | R/WC |
| BIT NAME    | HOST_EC_MBOX[7:0] |      |      |       |      |      |                     |      |

#### HOST\_EC\_MBOX[7:0]

If enabled, an interrupt to the EC marked by the [MBX](#) bit in the [IRQ17 Source Register](#) will be generated whenever the Host writes this register.

This register is cleared when written with FFh.

### 8.5.4 EC-to-Host Mailbox Register

Table 8.6 EC-to-Host Mailbox Register

|             |                   |      |      |       |      |      |                     |      |
|-------------|-------------------|------|------|-------|------|------|---------------------|------|
| HOST OFFSET | MBX_01h           |      |      | 8-Bit |      |      | HOST SIZE           |      |
| EC OFFSET   | 104h              |      |      | 8-Bit |      |      | EC SIZE             |      |
| POWER       | VTR               |      |      | 00h   |      |      | nSYS_RST<br>DEFAULT |      |
| BUS         | LPC SPB           |      |      |       |      |      |                     |      |
| BYTE0 BIT   | D7                | D6   | D5   | D4    | D3   | D2   | D1                  | D0   |
| HOST TYPE   | R/WC              | R/WC | R/WC | R/WC  | R/WC | R/WC | R/WC                | R/WC |
| EC TYPE     | R/W               | R/W  | R/W  | R/W   | R/W  | R/W  | R/W                 | R/W  |
| BIT NAME    | EC_HOST_MBOX[7:0] |      |      |       |      |      |                     |      |

#### EC\_HOST\_MBOX[7:0]

An EC write to this register will set bit [EC\\_WR](#) in the [SMI Interrupt Source Register](#) to '1b'. If enabled, setting bit [EC\\_WR](#) to '1b' generates a Host SMI.

This register is cleared when written with FFh.

## 8.5.5 SMI Interrupt Source Register

**Table 8.7** SMI Interrupt Source Register

| HOST OFFSET | MBX_02h     |      |      | 8-Bit |      |      | HOST SIZE           |       |
|-------------|-------------|------|------|-------|------|------|---------------------|-------|
| EC OFFSET   | 108h        |      |      | 8-Bit |      |      | EC SIZE             |       |
| POWER       | VTR         |      |      | 00h   |      |      | nSYS_RST<br>DEFAULT |       |
| BUS         | LPC SPB     |      |      |       |      |      |                     |       |
| BYTE0 BIT   | D7          | D6   | D5   | D4    | D3   | D2   | D1                  | D0    |
| HOST TYPE   | R/WC        | R/WC | R/WC | R/WC  | R/WC | R/WC | R/WC                | R     |
| EC TYPE     | R/W         | R/W  | R/W  | R/W   | R/W  | R/W  | R/W                 | -     |
| BIT NAME    | EC_SWI[6:0] |      |      |       |      |      |                     | EC_WR |

### EC\_WR

This bit is set autonomously when the [EC-to-Host Mailbox Register](#) has been written. An SMI to the Host is generated when any bit in this register ([EC\\_WR](#) or any bit in [EC\\_SWI\[6:0\]](#)) is '1b' and the corresponding bit in the [SMI Interrupt Mask Register](#) register is '1b'.

This bit is automatically cleared by a read of the [EC-to-Host Mailbox Register](#). The bit is also cleared when written with a '1b', by either the Host or the EC.

### EC\_SWI[6:0]

The EC can generate an SMI to the Host by writing any non-zero value to this field.

Each bit in this field is cleared when written with a '1b'.

## 8.5.6 SMI Interrupt Mask Register

**Table 8.8 SMI Interrupt Mask Register**

| HOST OFFSET | MBX_03h        |     |     |     | 8-Bit |     |     | HOST SIZE           |  |
|-------------|----------------|-----|-----|-----|-------|-----|-----|---------------------|--|
| EC OFFSET   | 10Ch           |     |     |     | 8-Bit |     |     | EC SIZE             |  |
| POWER       | VTR            |     |     |     | 00h   |     |     | nSYS_RST<br>DEFAULT |  |
| BUS         | LPC SPB        |     |     |     |       |     |     |                     |  |
| BYTE0 BIT   | D7             | D6  | D5  | D4  | D3    | D2  | D1  | D0                  |  |
| HOST TYPE   | R/W            | R/W | R/W | R/W | R/W   | R/W | R/W | R/W                 |  |
| EC TYPE     | R/W            | R/W | R/W | R/W | R/W   | R/W | R/W | R/W                 |  |
| BIT NAME    | EC_SWI_EN[6:0] |     |     |     |       |     |     | EC_WR_EN            |  |

### EC\_WR\_EN

If this bit is '1b', bit [EC\\_WR](#) in the [SMI Interrupt Source Register](#) is enabled.

### EC\_SWI\_EN[6:0]

Each bit that is set to '1b' in this field enables the corresponding bit in the [EC\\_SWI\[6:0\]](#) field in the [SMI Interrupt Source Register](#).

## 8.6 MailBox Register Interface Revision History

This revision history shows the changes made to this chapter.

**Table 8.9 MailBox Register Interface Chapter Revision History**

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History,"</a> on <a href="#">page 539</a> . |              |            |                                                                                                                             |                                                             |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------------|-----------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------|
| #                                                                                                                                                                                                                                                            | REV# IN SPEC | DATE       | SECTION/FIGURE/ENTRY                                                                                                        | CORRECTION                                                  |
| 1.                                                                                                                                                                                                                                                           | 0.4          | 05/10/2007 | <a href="#">Section 8.2.3, "Reset,"</a> on <a href="#">page 172</a> , <a href="#">Table 8.3</a> & <a href="#">Table 8.4</a> | Replace VCC POR with <a href="#">VCC_PWRGD</a> deassertion. |
| 2.                                                                                                                                                                                                                                                           |              |            |                                                                                                                             |                                                             |
| 3.                                                                                                                                                                                                                                                           |              |            |                                                                                                                             |                                                             |
| 4.                                                                                                                                                                                                                                                           |              |            |                                                                                                                             |                                                             |





## Chapter 9 ACPI Embedded Controller Interface

### 9.1 General Description

The [ACPI Embedded Controller Interface](#) is a Host/EC Message Interface. The ACPI defines the standard hardware and software communications interface between the OS and an embedded controller. This interface allows the OS to support a standard driver that can directly communicate with the embedded controller, allowing other drivers within the system to communicate with and use the EC resources; for example, Smart Battery and AML code

The [ACPI Embedded Controller Interface](#) also provides a four byte data interface which is a superset of the standard [ACPI Embedded Controller Interface](#) one byte data interface. The [ACPI Embedded Controller Interface](#) defaults to the standard one byte interface.

The [ACPI Embedded Controller Interface](#) features:

- Three Independent Interfaces
- Considered as Channel
- Each Channel is associated with a Logical Device Number
- Standard one data byte interface
- Four byte interface superset

#### 9.1.1 Block Diagram

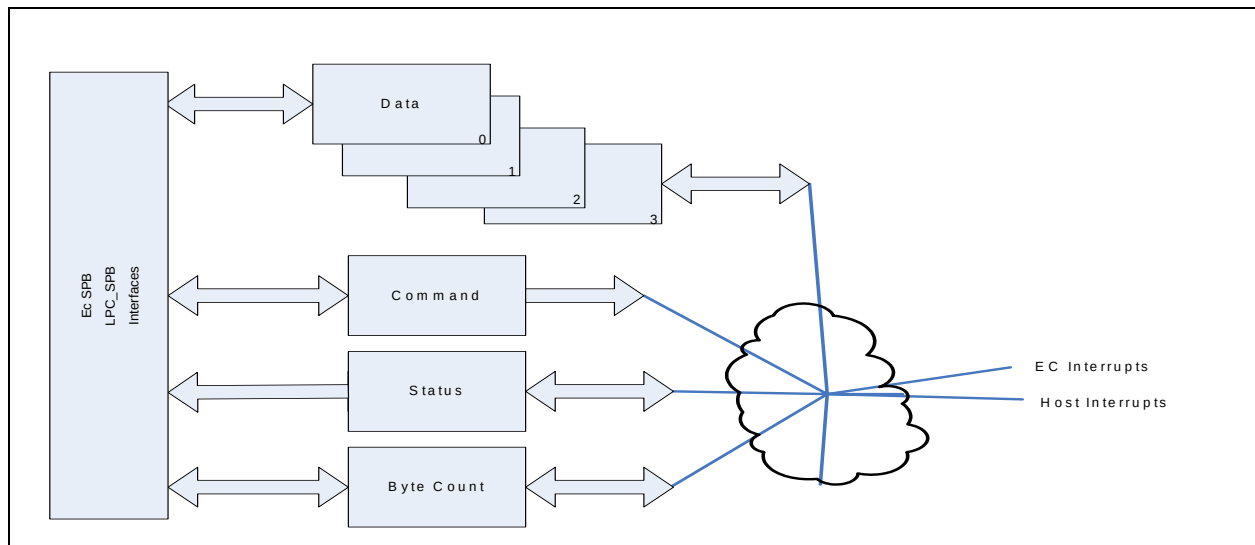


Figure 9.1 [ACPI Embedded Controller Interface](#) Block Diagram (Single Channel)

### 9.2 Power, Clocks and Reset

#### 9.2.1 Power Domain

This block is powered by the VTR Power Supply.

See [Section 4.5, "Power Configuration,"](#) on page 96 for details on power domains.

## 9.2.2 Clocks

This block has one clock input, the [LPC Bus Clock](#).

See [Section 4.4, "Clock Generator," on page 77](#) for details on clocks.

## 9.2.3 Reset

This block is reset on a [nSYS\\_RST](#).

See [Section 4.6, "Reset Interface," on page 99](#) for details on reset.

## 9.3 Interrupts

Each [ACPI Embedded Controller Interface](#) can generate an EC\_OBF interrupt when the OBF in the [EC\\_Cx\\_STATUS Register](#) is cleared and an EC\_IBF interrupt when the IBF in the [EC\\_Cx\\_STATUS Register](#) is set. The interrupt source is routed onto bits [5:0] of the [IRQ24 Source Register](#), and is a level, active high signal.

**Note 9.1** An SCI or SMI event can be tracked by Host/EC firmware via the SCI\_EVT & SMI\_EVT Bits in the [EC\\_Cx\\_STATUS Register on page 185](#); however, the [ACPI Embedded Controller Interface](#) does not generate a SCI or SMI events directly. SMI events are generated in the [SMI Interrupt Source Register on page 179](#) of the [MailBox Register Interface](#). SCI events are generated by the [ACPI PM1 Block Interface on page 212](#). (See [Section 11.3.1, "SCI Interrupts to the Host," on page 212](#))

## 9.4 Registers

There are three instances of [ACPI Embedded Controller Interface](#) block implemented in the MEC5035 enumerated as 1, 2, 3.

Each instance of the [ACPI Embedded Controller Interface](#) has its own Logical Device Number, and Base Address as indicated in [Table 9.1](#).

**Table 9.1** [ACPI Embedded Controller Interface](#) Base Address Table

| <a href="#">ACPI Embedded Controller Interface</a><br>INSTANCE | LDN<br>FROM<br>( <a href="#">Table 7.2</a><br>on<br>page 167) | AHB BASE ADDRESS         |
|----------------------------------------------------------------|---------------------------------------------------------------|--------------------------|
| ACPI_EC 1                                                      | 2h                                                            | <a href="#">FF_0800h</a> |
| ACPI_EC 2                                                      | 3h                                                            | <a href="#">FF_0C00h</a> |
| ACPI_EC 3                                                      | 4h                                                            | <a href="#">FF_1000h</a> |

**Note 9.2** The Host LPC I/O addresses for each instance is selected via a Base Address Register (see [Section 6.6.2, "Base Address Registers," on page 144](#)). LPC access to configuration registers is through the Host Access Configuration Port (see [Section 6.5.1, "Host Access Port," on page 142](#).)

The [Table 9.2](#) is a register summary for one instance of the [ACPI Embedded Controller Interface](#). The LPC I/O address for each Run-Time Register is described below as an offset from its Base Address Register. Each EC address is indicated as an SPB Offset from its AHB base address. Each configuration register access through the [Host Access Port](#) is via its LDN indicated in [Table 9.1 on page 183](#) and its [Host Access Port](#) index which is described as "Host Config Index" in the tables below.

**Table 9.2 ACPI Embedded Controller Interface Register Summary**

| REGISTER NAME                | HOST I/O ACCESS   |               |              | CMD<br>Note<br>9.3 | EC INTERFACE  |              |            | NOTES    |
|------------------------------|-------------------|---------------|--------------|--------------------|---------------|--------------|------------|----------|
|                              | HOST I/O<br>INDEX | SPB<br>OFFSET | HOST<br>TYPE |                    | SPB<br>OFFSET | BYTE<br>LANE | EC<br>TYPE |          |
| EC_Cx_DATA 0<br>Register     | 00h               | 00h           | R/W          | 0                  | 100h          | 0            | R/W        |          |
| EC_Cx_DATA 1<br>Register     | 01h               | 01h           | R/W          | 0                  |               | 1            | R/W        |          |
| EC_Cx_DATA 2<br>Register     | 02h               | 02h           | R/W          | 0                  |               | 2            | R/W        |          |
| EC_Cx_DATA 3<br>Register     | 03h               | 03h           | R/W          | 0                  |               | 3            | R/W        |          |
| EC_Cx_COMMAND<br>Register    | 04h               | 04h           | W            | 1                  | 100h          | 0            | R          | Note 9.4 |
| EC_Cx_STATUS<br>Register     | 04h               | 04h           | R            | 0                  | 104h          | 0            | R/W        |          |
| EC_Cx_Byte Count<br>Register | 05h               | 05h           | R            | 0                  | 105h          | 0            | R          |          |
| Reserved                     | 06h               | 06h           | R            | n/a                | 106h          | 0            | R          | Note 9.5 |
| Reserved                     | 07h               | 07h           | R            | n/a                | 107h          | 0            | R          |          |

**Note 9.3** CMD is bit D3 in the EC\_Cx\_STATUS Register.

**Note 9.4** See Section 9.4.3, "EC\_Cx\_COMMAND Register," on page 186 for description of host access and data flow to EC.

**Note 9.5** This reserved register is claimed by the block. Reads return data value of 00h and writes have no effect.

### 9.4.1 Run-Time Registers

ACPI Embedded Controller Interface contains three registers: EC\_Cx\_COMMAND Register, EC\_Cx\_STATUS Register, and EC\_Cx\_DATA. The standard ACPI Embedded Controller Interface registers occupy two addresses in the Host I/O space (Table 9.2).

The EC\_Cx\_DATA and EC\_Cx\_COMMAND registers appear as a single 8-bit data register in the EC. The CMD bit in the EC\_Cx\_STATUS register is used by the EC to discriminate commands from data written by the host to the ECI. CMD is controlled by hardware: host writes to the EC\_Cx\_DATA register clear the CMD bit; host writes to the EC\_Cx\_COMMAND register set the CMD bit.

### 9.4.2 EC\_Cx\_STATUS Register

The EC\_Cx\_STATUS Register indicates the state of the Embedded Controller Interface of Channel x. To the host, the EC\_Cx\_STATUS Register is read-only. To the EC, some bits in the EC\_Cx\_STATUS Register are read-only (Table 9.3). These bits are controlled by hardware. The EC software controlled bits in the EC\_Cx\_STATUS Register are read/write.



Table 9.3 EC\_Cx\_STATUS Register

|                |         |                         |                         |       |     |     |                     |     |
|----------------|---------|-------------------------|-------------------------|-------|-----|-----|---------------------|-----|
| HOST I/O INDEX | 04h     |                         |                         | 8-bit |     |     | HOST SIZE           |     |
| EC OFFSET      | 104h    |                         |                         | 8-bit |     |     | EC SIZE             |     |
| POWER          | VTR     |                         |                         | 00h   |     |     | nSYS_RST<br>DEFAULT |     |
| BUS            | LPC SPB |                         |                         |       |     |     |                     |     |
| BYTE0 BIT      | D7      | D6                      | D5                      | D4    | D3  | D2  | D1                  | D0  |
| HOST TYPE      | R       |                         |                         |       |     |     |                     |     |
| EC TYPE        | R/W     | R/W                     | R/W                     | R/W   | R   | R/W | R                   | R   |
| BIT NAME       | UD      | SMI<br>EVT <sup>−</sup> | SCI<br>EVT <sup>−</sup> | BURST | CMD | UD  | IBF                 | OBF |

**Note 9.6** The UD bits are User-Defined. UD bits are maintained by EC software, only.

#### OBF

The Output Buffer Full (OBF) flag is set when the EC writes a byte of data into the data port ([EC\\_Cx\\_DATA 0 Register](#)).

Once the host reads the status byte and sees the OBF flag set, the host reads the data port to get the byte of data that the EC has written.

Once the host reads the data, the OBF flag is automatically cleared by hardware. An EC\_OBF interrupt signals the EC that the data has been read by the host and the EC is free to write more data to the [EC\\_Cx\\_DATA 0 Register](#) register.

The EC\_OBF interrupt is generated whenever the OBF bit in the [EC\\_Cx\\_STATUS Register](#) register is reset. See [Section 9.3, "Interrupts," on page 183](#).

#### IBF

The Input Buffer Full (IBF) flag is set when the host has written a byte of data to the command or data port.

An EC\_IBF interrupt signals the EC that there is data available. Once the EC reads the status byte and sees the IBF flag set, the EC reads the data port to get the byte of data that the host has written.

Once the EC reads the data, the IBF flag is automatically cleared by hardware. The EC must then generate a software interrupt to alert the host that the data has been read and that the host is free to write more data to the ECI as needed. See [Section 9.3, "Interrupts," on page 183](#).

#### CMD

The CMD bit is set when the [EC\\_Cx\\_DATA 0 Register](#) register contains a command byte; the CMD bit is cleared when the [EC\\_Cx\\_DATA 0 Register](#) contains a data byte.

The CMD bit is controlled by hardware: host writes to the [EC\\_Cx\\_DATA 0 Register](#) register clear CMD; host writes to the [EC\\_Cx\\_COMMAND Register](#) set CMD.

The CMD bit allows the embedded controller to differentiate the start of a command sequence from a data byte write operation.

**BURST**

The BURST bit is set when the EC is in Burst Mode for polled command processing; the BURST bit is cleared when the EC is in Normal mode for interrupt-driven command processing.

The BURST bit is an EC-maintained software flag that indicates the embedded controller has received the Burst Enable command from the host, has halted normal processing, and is waiting for a series of commands to be sent from the host. Burst Mode allows the OS or system management handler to quickly read and write several bytes of data at a time without the overhead of SCIs between commands.

**Note 9.7** The BURST bit is maintained by EC software, only.

**SCI\_EVT**

The SCI Event flag is set by software when an SCI event is pending; i.e., the EC is requesting an SCI query; SCI Event flag is clear when no SCI events are pending.

The SCI Event bit is an EC-maintained software flag that is set when the embedded controller has detected an internal event that requires operating system attention. The EC sets SCI Event before generating an SCI to the OS.

**Note 9.8** The SCI Event bit is maintained by EC software, only. See [Note 9.1 on page 183](#).

**SMI\_EVT**

The SMI Event flag is set when an SMI event is pending; i.e., the EC is requesting an SMI query; SMI Event flag is cleared when no SMI events are pending.

The SMI Event bit is an EC-maintained software flag that is set when the embedded controller has detected an internal event that requires system management interrupt handler attention. The EC sets SMI Event before generating an SMI.

**Note 9.9** The SMI Event flag bit is maintained by EC software, only. See [Note 9.1 on page 183](#).

### 9.4.3 EC\_Cx\_COMMAND Register

The [EC\\_Cx\\_COMMAND Register](#) is a write-only register that allows the host to issue commands to the embedded controller.

Writes to the [EC\\_Cx\\_COMMAND Register](#) are latched in the EC data register and the IBF is set in the [EC\\_Cx\\_STATUS Register](#). Writes to the [EC\\_Cx\\_COMMAND Register](#) also set the CMD bit in the [EC\\_Cx\\_STATUS Register](#).

### 9.4.4 EC\_Cx\_DATA 0 Register

The [EC\\_Cx\\_DATA 0 Register](#) is a read/write register that allows the host to issue data arguments to the embedded controller and allows the OS to read data returned by the embedded controller.

## 9.5 Non Legacy Operation

This mode adds three additional Data Registers: [EC\\_Cx\\_DATA 1 Register](#), [EC\\_Cx\\_DATA 2 Register](#), and [EC\\_Cx\\_DATA 3 Register](#).

The [Byte Count](#) controls the operation of the IBF and OBF including EC\_IBF and EC\_OBF interrupts. Bits[3:0] of the register contain the byte flags. These are set when data is written to the corresponding Data register and cleared when the corresponding data register is read.

Bits[5:4], the Bytes Used field, indicates how many bytes are to be transferred. This field is defaulted to 1 which supports legacy mode. The values for these bits are:

- 00 Byte 0 (default legacy)
- 10 Bytes 0 and 1

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11 Bytes 0,1, and 2

11 Bytes 0,1,2, and 3r

**Note 9.10** All other values are reserved and resort to the default value

Bits[3:0], the Bytes Written field, indicates how many bytes have been written. This may be used to insure completion of expected data transfers.

**9.5.1 Byte Count****Table 9.4 EC\_Cx\_Byte Count Register**

|             |                |                |          |    |                           |                           |                           |                           |  |
|-------------|----------------|----------------|----------|----|---------------------------|---------------------------|---------------------------|---------------------------|--|
| HOST OFFSET | 05h            |                |          |    | 8-bit                     |                           |                           | HOST SIZE                 |  |
| EC OFFSET   | 105h           |                |          |    | 8-bit                     |                           |                           | EC SIZE                   |  |
| POWER       | VTR            |                |          |    | 00h                       |                           |                           | nSYS_RST<br>DEFAULT       |  |
| BUS         | LPC SPB        |                |          |    |                           |                           |                           |                           |  |
| BYTE0 BIT   | D7             | D6             | D5       | D4 | D3                        | D2                        | D1                        | D0                        |  |
| HOST TYPE   | R/W            | R/W            | R        | R  | R                         |                           |                           |                           |  |
| EC TYPE     | R/W            | R/W            | R        | R  | R                         |                           |                           |                           |  |
| BIT NAME    | Byte 1<br>Used | Byte 0<br>Used | Reserved |    | Data<br>Byte 3<br>Written | Data<br>Byte 2<br>Written | Data<br>Byte 1<br>Written | Data<br>Byte 0<br>Written |  |

**Table 9.5 Control of IBF**

|                       | CMD | DATA<br>BYTE 0<br>BIT[0] | DATA<br>BYTE 1<br>BIT[1] | DATA<br>BYTE 2<br>BIT[2] | DATA<br>BYTE 3<br>BIT[3] | IBF | BYTES<br>USED[7:6] |
|-----------------------|-----|--------------------------|--------------------------|--------------------------|--------------------------|-----|--------------------|
| Host Writes<br>CMD    | ↑   | ↑                        | 0                        | 0                        | 0                        | ↑   | 00b<br>Legacy      |
| EC Reads<br>CMD       | ↓   | ↓                        | 0                        | 0                        | 0                        | ↓   |                    |
| Host Writes<br>Data 0 | 0   | ↑                        | 0                        | 0                        | 0                        | ↑   | 00b<br>Legacy      |
| EC Reads<br>Data 0    | 0   | ↓                        | 0                        | 0                        | 0                        | ↓   |                    |

**Table 9.5 Control of IBF**

|                       | CMD | DATA<br>BYTE 0<br>BIT[0] | DATA<br>BYTE 1<br>BIT[1] | DATA<br>BYTE 2<br>BIT[2] | DATA<br>BYTE 3<br>BIT[3] | IBF | BYTES<br>USED[7:6] |
|-----------------------|-----|--------------------------|--------------------------|--------------------------|--------------------------|-----|--------------------|
| Host Writes<br>Data 0 | 0   | ↑                        | 0                        | 0                        | 0                        | 0   | 01b                |
| Host Writes<br>Data 1 | 0   | 1                        | ↑                        | 0                        | 0                        | ↑   |                    |
| EC Reads<br>Data 0    | 0   | ↓                        | 1                        | 0                        | 0                        | 1   |                    |
| EC Reads<br>Data 1    | 0   | 0                        | ↓                        | 0                        | 0                        | ↓   |                    |
| Host Writes<br>Data 0 | 0   | ↑                        | 0                        | 0                        | 0                        | 0   | 10b                |
| Host Writes<br>Data 1 | 0   | 1                        | ↑                        | 0                        | 0                        | 0   |                    |
| Host Writes<br>Data 2 | 0   | 1                        | 1                        | ↑                        | 0                        | ↑   |                    |
| EC Reads<br>Data 0    | 0   | ↓                        | 1                        | 1                        | 0                        | 1   |                    |
| EC Reads<br>Data 1    | 0   | 0                        | ↓                        | 1                        | 0                        | 1   |                    |
| EC Reads<br>Data 2    | 0   | 0                        | 0                        | ↓                        | 0                        | ↓   |                    |
| Host Writes<br>Data 0 | 0   | ↑                        | 0                        | 0                        | 0                        | 0   | 11b                |
| Host Writes<br>Data 1 | 0   | 1                        | ↑                        | 0                        | 0                        | 0   |                    |
| Host Writes<br>Data 2 | 0   | 1                        | 1                        | ↑                        | 0                        | 0   |                    |
| Host Writes<br>Data 3 | 0   | 1                        | 1                        | 1                        | ↑                        | ↑   |                    |
| EC Reads<br>Data 0    | 0   | ↓                        | 1                        | 1                        | 1                        | 1   |                    |
| EC Reads<br>Data 1    | 0   | 0                        | ↓                        | 1                        | 1                        | 1   |                    |
| EC Reads<br>Data 2    |     | 0                        | 0                        | ↓                        | 1                        | 1   |                    |
| EC Reads<br>Data 3    | 0   | 0                        | 0                        | 0                        | ↓                        | ↓   |                    |



Table 9.6 Control of OBF

|                      | CMD | DATA<br>BYTE 0<br>BIT[0] | DATA<br>BYTE 1<br>BIT[1] | DATA<br>BYTE 2<br>BIT[2] | DATA<br>BYTE 3<br>BIT[3] | OBF | BYTE<br>COUNT[7:6] |
|----------------------|-----|--------------------------|--------------------------|--------------------------|--------------------------|-----|--------------------|
| EC Writes<br>Data 0  | 0   | ↑                        | 0                        | 0                        | 0                        | ↑   | 00b<br>Legacy      |
| Host Reads<br>Data 0 | 0   | ↓                        | 0                        | 0                        | 0                        | ↓   |                    |
| EC Writes<br>Data 0  | 0   | ↑                        | 0                        | 0                        | 0                        | 0   | 01b                |
| EC Writes<br>Data 1  | 0   | 1                        | ↑                        | 0                        | 0                        | ↑   |                    |
| Host Reads<br>Data 0 | 0   | ↓                        | 1                        | 0                        | 0                        | 1   |                    |
| Host Reads<br>Data 1 | 0   | 0                        | ↓                        | 0                        | 0                        | ↓   |                    |
| EC Writes<br>Data 0  | 0   | ↑                        | 0                        | 0                        | 0                        | 0   | 10b                |
| EC Writes<br>Data 1  | 0   | 1                        | ↑                        | 0                        | 0                        | 0   |                    |
| EC Writes<br>Data 2  | 0   | 1                        | 1                        | ↑                        | 0                        | ↑   |                    |
| Host Reads<br>Data 0 | 0   | ↓                        | 1                        | 1                        | 0                        | 1   |                    |
| Host Reads<br>Data 1 | 0   | 0                        | ↓                        | 1                        | 0                        | 1   |                    |
| Host Reads<br>Data 2 | 0   | 0                        | 0                        | ↓                        | 0                        | ↓   |                    |
| EC Writes<br>Data 0  | 0   | ↑                        | 0                        | 0                        | 0                        | 0   | 11b                |
| EC Writes<br>Data 1  | 0   | 1                        | ↑                        | 0                        | 0                        | 0   |                    |
| EC Writes<br>Data 2  | 0   | 1                        | 1                        | ↑                        | 0                        | 0   |                    |
| EC Writes<br>Data 3  | 0   | 1                        | 1                        | 1                        | ↑                        | ↑   |                    |
| Host Reads<br>Data 0 | 0   | ↓                        | 1                        | 1                        | 1                        | 1   |                    |
| Host Reads<br>Data 1 | 0   | 0                        | ↓                        | 1                        | 1                        | 1   |                    |
| Host Reads<br>Data 2 |     | 0                        | 0                        | ↓                        | 1                        | 1   |                    |
| Host Reads<br>Data 3 | 0   | 0                        | 0                        | 0                        | ↓                        | ↓   |                    |



## 9.5.2 EC\_Cx\_DATA 1 Register

The [EC\\_Cx\\_DATA 1 Register](#) is a read/write register that allows the host to issue data arguments to the embedded controller and allows the OS to read data returned by the embedded controller.

## 9.5.3 EC\_Cx\_DATA 2 Register

The [EC\\_Cx\\_DATA 2 Register](#) is a read/write register that allows the host to issue data arguments to the embedded controller and allows the OS to read data returned by the embedded controller.

## 9.5.4 EC\_Cx\_DATA 3 Register

The [EC\\_Cx\\_DATA 3 Register](#) is a read/write register that allows the host to issue data arguments to the embedded controller and allows the OS to read data returned by the embedded controller.

## 9.6 ACPI Embedded Controller Interface Revision History

This revision history shows the changes made to this chapter.

**Table 9.7** [ACPI Embedded Controller Interface](#) Chapter Revision History

| “REV# IN SPEC” column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, “MEC5035 Product Customer Specification-ODM Revision History,”</a> on page 539. |              |           |                                                                                                                                                                                                                  |                                                                                                                                                                                                                                         |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE      | SECTION/FIGURE/ENTRY                                                                                                                                                                                             | CORRECTION                                                                                                                                                                                                                              |
| 1.                                                                                                                                                                                                                                          | 0.4          | 4/20/2007 | <a href="#">Table 9.4, “EC_Cx_Byte Count Register,”</a> on page 187<br><br><a href="#">Table 9.2, “ACPI Embedded Controller Interface Register Summary,”</a> on page 184<br><a href="#">Note 9.5</a> on page 184 | <ul style="list-style-type: none"> <li>Default value of <a href="#">EC_Cx_Byte Count Register</a> is 0.</li> <li>Added reserved registers at offset 6h &amp; 7h to insure cover full range of LPC access when BAR mask = 7h.</li> </ul> |
| 2.                                                                                                                                                                                                                                          |              |           |                                                                                                                                                                                                                  |                                                                                                                                                                                                                                         |
| 3.                                                                                                                                                                                                                                          |              |           |                                                                                                                                                                                                                  |                                                                                                                                                                                                                                         |
| 4.                                                                                                                                                                                                                                          |              |           |                                                                                                                                                                                                                  |                                                                                                                                                                                                                                         |



# Chapter 10 8042 Emulated Keyboard Controller

## 10.1 General Description

The MEC5035 keyboard controller uses the EC to produce a superset of the features provided by the industry-standard 8042 keyboard controller. The [8042 Emulated Keyboard Controller](#) is Host/EC Message Interface with hardware assists to emulate 8042 behavior and provide Legacy GATEA20 support.

### 10.1.1 Features

- Legacy Keyboard Support
- Emulated 8042 Operation
- Port 92 Legacy A20M Support

### 10.1.2 Block Diagram

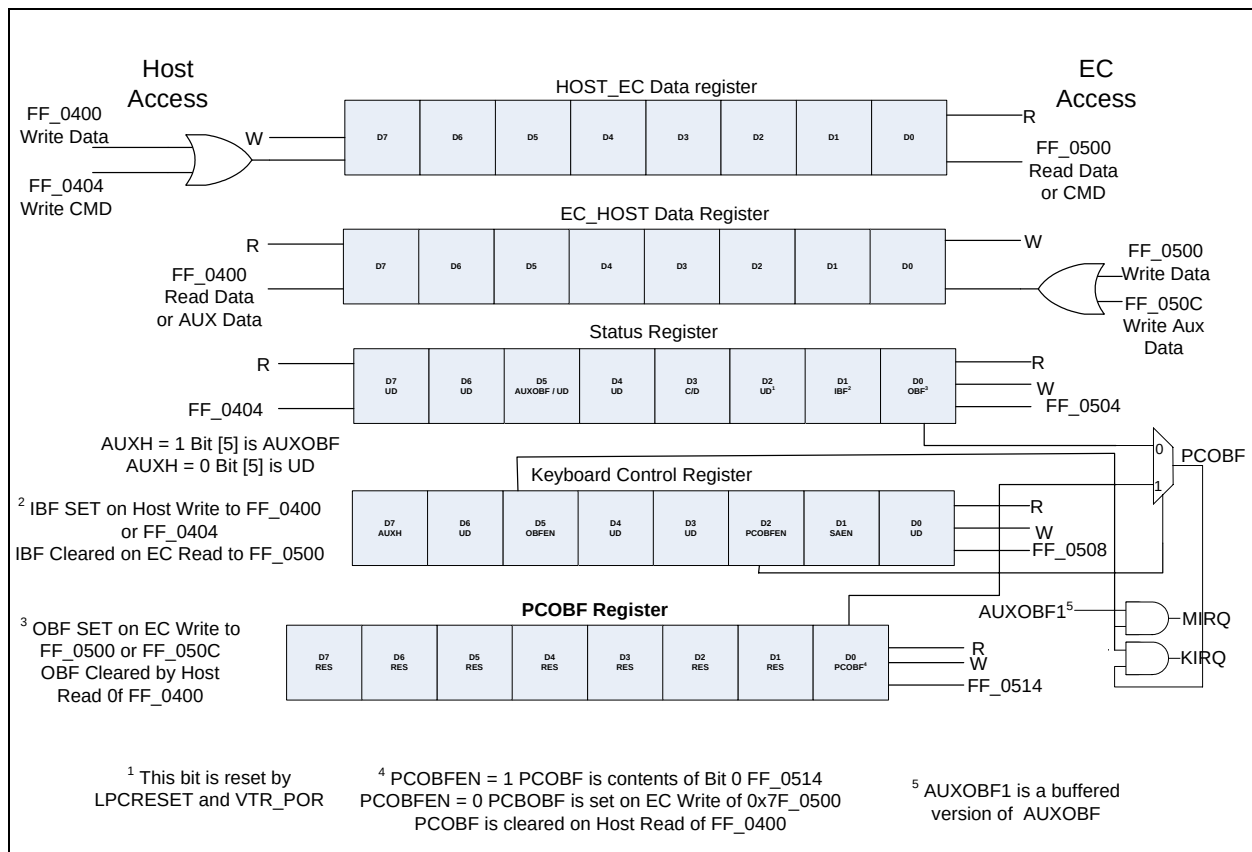


**Figure 10.1 Block Diagram of 8042 Emulated Keyboard Controller**

### 10.1.3 Block Diagram Signal List

**Table 10.1 8042 Emulated Keyboard Controller Signal List**

| SIGNAL NAME | DIRECTION | DESCRIPTION                                                                            |
|-------------|-----------|----------------------------------------------------------------------------------------|
| EC_IBF      | Output    | Interrupt generated by the host writing either data or command to the data register    |
| EC_OBF      | Output    | Interrupt generated by the host reading either data or aux data from the data register |
| KIRQ        | Output    | Routed to the Host SIRQ                                                                |
| MIRQ        | Output    | Routed to the Host SIRQ                                                                |

## 10.2 Power, Clocks and Reset

### 10.2.1 Power Domain

This block is powered by VTR.

See [Section 4.5, "Power Configuration," on page 96](#) for details on power domains.

### 10.2.2 Clocks

This block has four clock inputs: [LPC Bus Clock](#), 1MHz ([MCLK\\_DIV32\\_EN](#)) clock source. [LPC Bus Clock](#) is used to the accessible and clock the registers in this block. The 1MHz [Host Clock Domain](#) is used to clock the counter in the CPU\_RESET circuitry.

See [Section 4.4, "Clock Generator," on page 77](#) for details on clocks.

## 10.3 Power On Reset

This block is reset on a [nSYS\\_RST](#) and [nSIO\\_RESET](#). On a reset, all Register are reset to 00h and the state machines are set to idle.

See [Section 4.6, "Reset Interface," on page 99](#) for details on reset.

## 10.4 Interrupts

The [8042 Emulated Keyboard Controller](#) can generate an [KBD\\_OBF](#) interrupt when the [OBF](#) bit in the [Keyboard Status Read Register](#) is cleared and an [KBD\\_IBF](#) interrupt when the [IBF](#) bit in the [Keyboard Status Read Register](#) is set. The interrupt source is routed onto the [IRQ23 Source Register](#), and are level, active high signals.

### 10.4.1 8042 Emulated Keyboard Controller (LDN 1h) SIRQ Routing

The [8042 Emulated Keyboard Controller](#) can generate two SIRQ events for the EC-to-HOST EC events: [KIRQ](#) & [MIRQ](#). For the [KIRQ](#) interrupt the Interrupt Configuration Register, [SELECT](#) on [page 151](#) is cleared to '0' and for [MIRQ](#) the Interrupt Configuration Register, [SELECT](#) is set to '1'.

See [Chapter 6, Logical Device Configuration, Section 6.8, "SERIRQ Interrupts," on page 150](#).

## 10.5 Instance Description

There are two blocks defined in this chapter: [8042 MSG Interface](#) and the [Port92-Legacy](#). The MEC5035 has one instance of each block.

## 10.6 Registers

The [8042 Emulated Keyboard Controller](#) has a [8042 MSG Interface](#) block which has its own Logical Device Number, and Base Address as indicated in [Table 10.2](#). The Host LPC I/O addresses for the [8042 MSG Interface](#) is selected via Base Address Register (see [Section 6.6.2, "Base Address Registers," on page 144](#)). LPC access to configuration registers is through Host Access Configuration Port (see [Section 6.5.1, "Host Access Port," on page 142](#).)

The [8042 Emulated Keyboard Controller](#) also has a [Port92-Legacy](#) block which has a separate Logical Device Number and Base Address Register as indicated in [Table 10.2](#). The Base Address Register for the [Port92-Legacy](#) has only one writable bit, the Valid Bit, since the only I/O accessible Register has a fixed address.

[Table 10.3](#) is a register summary for the [8042 MSG Interface](#) block and [Table 10.14 on page 202](#) is a register summary for the [Port92-Legacy](#) block.

**Table 10.2 8042 Emulated Keyboard Controller Base Address Table**

| <a href="#">8042 Emulated Keyboard Controller BLOCKS</a> | <b>LDN FROM<br/>(<a href="#">Table 7.2 on page 167</a>)</b> | <b>AHB BASE ADDRESS</b>  |
|----------------------------------------------------------|-------------------------------------------------------------|--------------------------|
| <b>8042 MSG Interface</b>                                | 1h                                                          | <a href="#">FF_0400h</a> |
| <b>Port92-Legacy</b>                                     | 7h                                                          | <a href="#">FF_1C00h</a> |

**Note 10.1** The Host LPC I/O addresses for this instance is selected via a Base Address Register (see [Section 6.6.2, "Base Address Registers," on page 144](#)). LPC access to configuration registers is through the Host Access Configuration Port (see [Section 6.5.1, "Host Access Port," on page 142](#).)

[Table 10.3](#) is a register summary for the [8042 MSG Interface](#) block. The LPC I/O address for each Run-Time Register is described below as an offset from its Base Address Register. Each EC address is indicated as an SPB Offset from its AHB base address. Each Configuration register access through the [Host Access Port](#) is via its LND indicated in [Table 10.2 on page 194](#) and its [Host Access Port](#) index which is described as "Host Config Index" in the tables below.



Table 10.3 8042 MSG Interface Register Summary

| REGISTER NAME                        | HOST I/O ACCESS    |            |           | CMD<br>Note<br>10.2 | EC INTERFACE |           |         | NOTES |
|--------------------------------------|--------------------|------------|-----------|---------------------|--------------|-----------|---------|-------|
|                                      | HOST I/O INDEX     | SPB OFFSET | HOST TYPE |                     | SPB OFFSET   | BYTE LANE | EC TYPE |       |
| HOST_EC<br>Data/CMD Register         | 00h                | 00h        | W         | 0                   | 100h         | 0         | R       |       |
|                                      | 04h                | 04h        |           | 1                   |              | 0         | R       |       |
| EC_HOST<br>Data/AUX Data<br>Register | 00h                | 00h        | R         | 0                   | 100h         | 0         | W       |       |
|                                      |                    |            |           | 0                   | 10Ch         | 0         |         |       |
| Keyboard Status<br>Read Register     | 04h                | 04h        | R         | 0                   | 104h         | 3         | R/W     |       |
| PCOBF Register                       | -                  | -          | -         | 0                   | 114h         | 0         | R/W     |       |
| Keyboard Control<br>Register         | -                  | -          | -         | 0                   | 108h         | 0         | R/W     |       |
|                                      | HOST ACCESS        |            |           | N/A                 | EC INTERFACE |           |         |       |
| REGISTER NAME                        | HOST CONFIG. INDEX | SPB OFFSET | HOST TYPE |                     | EC OFFSET    | BYTE LANE | EC TYPE |       |
| Activate Register                    | 30h                | 330h       | R/W       |                     | 330h         | 0         | R/W     |       |

**Note 10.2** CMD is bit D3 in the [Keyboard Status Read Register](#).

**Note 10.3** All Registers listed in [Table 10.3](#) are powered by VTR and reset by [nSYS\\_RST](#).

## 10.7 8042 MSG Interface Configuration Registers

### 10.7.1 Activate Register

**Table 10.4 8042 MSG Interface Activate Register**

|                   |          |    |    |    |       |    |    |                     |  |
|-------------------|----------|----|----|----|-------|----|----|---------------------|--|
| HOST CONFIG INDEX | 330h     |    |    |    | 8-bit |    |    | HOST SIZE           |  |
| EC OFFSET         | NA       |    |    |    | 8-bit |    |    | EC SIZE             |  |
| POWER             | VTR      |    |    |    | 00h   |    |    | nSYS_RST<br>DEFAULT |  |
| BUS               | LPC SPB  |    |    |    |       |    |    |                     |  |
| BYTE3 BIT         | D7       | D6 | D5 | D4 | D3    | D2 | D1 | D0                  |  |
| HOST TYPE         | R        |    |    |    |       |    |    | R/W                 |  |
| EC TYPE           | -        | -  | -  | -  | -     | -  | -  | -                   |  |
| BIT NAME          | Reserved |    |    |    |       |    |    | Activate            |  |

#### ACTIVATE

0=1MHz Clock to the CPU\_REST block is disabled, ONLY if the PGEN is not active  
1=1MHz Clock to the CPU\_REST block is enabled

## 10.8 8042 MSG Interface Runtime Registers

### 10.8.1 HOST\_EC Data / CMD Register

This is an 8-bit HOST write-only register. When written with Data, the **C/D** status bit of the status register is cleared to zero and the **IBF** bit is set.

When written with a command, the **C/D** status bit of the status register is set to one and the **IBF** bit is set to a 1.

**Table 10.5 HOST\_EC Data/CMD Register**

|                |                         |    |    |       |    |    |                     |    |
|----------------|-------------------------|----|----|-------|----|----|---------------------|----|
| HOST I/O INDEX | 00h Data<br>04h Command |    |    | 8-bit |    |    | HOST SIZE           |    |
| EC OFFSET      | 100h                    |    |    | 8-bit |    |    | EC SIZE             |    |
| POWER          | VTR                     |    |    | 00h   |    |    | nSYS_RST<br>DEFAULT |    |
| BUS            | LPC SPB                 |    |    |       |    |    |                     |    |
| BYTE3 BIT      | D7                      | D6 | D5 | D4    | D3 | D2 | D1                  | D0 |
| HOST TYPE      | W                       | W  | W  | W     | W  | W  | W                   | W  |
| EC TYPE        | R                       | R  | R  | R     | R  | R  | R                   | R  |
| BIT NAME       | Data                    |    |    |       |    |    |                     |    |

### 10.8.2 EC\_HOST Data / AUX Data Register

This is an 8-bit read-only register. When read, by the HOST, the **PCOBF** and/or **AUXOBF** interrupts are cleared and the **OBF** flag in the status register is cleared.

**Table 10.6 EC\_HOST Data/AUX Data Register**

|                |                            |    |    |    |       |    |    |                     |  |
|----------------|----------------------------|----|----|----|-------|----|----|---------------------|--|
| HOST I/O INDEX | 00h                        |    |    |    | 8-bit |    |    | HOST SIZE           |  |
| EC OFFSET      | 100h Data or 10Ch Aux Data |    |    |    | 8-bit |    |    | EC SIZE             |  |
| POWER          | VTR                        |    |    |    | 00h   |    |    | nSYS_RST<br>DEFAULT |  |
| BUS            | LPC SPB                    |    |    |    |       |    |    |                     |  |
| BYTE3 BIT      | D7                         | D6 | D5 | D4 | D3    | D2 | D1 | D0                  |  |
| HOST TYPE      | R                          | R  | R  | R  | R     | R  | R  | R                   |  |
| EC TYPE        | W                          | W  | W  | W  | W     | W  | W  | W                   |  |
| BIT NAME       | Data                       |    |    |    |       |    |    |                     |  |

### 10.8.3 Keyboard Status Read

This is an 8 bit read only register. Refer to the description of the Status Register (EC OFFSET 104h) for more information.



Table 10.7 Keyboard Status Read Register

|                |         |     |         |       |     |                 |                     |     |
|----------------|---------|-----|---------|-------|-----|-----------------|---------------------|-----|
| HOST I/O INDEX | 4h      |     |         | 8-bit |     |                 | HOST SIZE           |     |
| EC OFFSET      | 104h    |     |         | 8-bit |     |                 | EC SIZE             |     |
| POWER          | VTR     |     |         | 00h   |     |                 | nSYS_RST<br>DEFAULT |     |
| BUS            | LPC SPB |     |         |       |     |                 |                     |     |
| BYTE3 BIT      | D7      | D6  | D5      | D4    | D3  | D2              | D1                  | D0  |
| HOST TYPE      | R       | R   | R       | R     | R   | R               | R                   | R   |
| EC TYPE        | R/W     | R/W | R/W     | R/W   | R   | R/W             | R                   | R   |
| BIT NAME       | UD      | UD  | AUX-OBF | UD    | C/D | UD <sup>1</sup> | IBF                 | OBF |

This register is read-only for the Host and read/write by the EC. The EC cannot write to bits 0, 1, or 3 of the Status register.

#### UD<sup>1</sup>

Read/Write by EC. These bits are user-definable. This bit is reset to '0' when LRESET# pin signal function is asserted. See [Table 3.3, "HOST INTERFACE," on page 41](#).

#### UD

Read/Write by EC. These bits are user-definable.

#### C/D

Command Data - This bit specifies whether the input data register contains data or a command ("0" = data, "1" = command). During a host command write operation, this bit is set to "1", during a host data write operation, this bit is set to "0".

#### IBF

Input Buffer Full - This flag is set to "1" whenever the host system writes data or a command into the [HOST\\_EC Data/CMD Register](#). Setting this flag activates the EC's [EC\\_IBF](#) interrupt if enabled. When the EC reads the [HOST\\_EC Data / CMD Register](#), this bit is automatically reset and the interrupt is cleared.

#### OBF

The Output Buffer Full (OBF) bit is set when the EC writes a byte of Data or AUX Data into the [EC\\_HOST Data / AUX Data Register](#). When the host reads the data, the [OBF](#) bit is automatically cleared by hardware and a [EC\\_OBF](#) interrupt is generated.

#### AUXOBF

Auxiliary Output Buffer Full - This flag is set to "1" whenever the EC writes AUX Data into [EC\\_HOST Data / AUX Data Register](#). This flag is reset to "0" whenever the EC writes into the Data into [EC\\_HOST Data / AUX Data Register](#).

**Table 10.8 PCOBF Register**

| HOST OFFSET | NA       |    |    |    |    |    | 8-bit | HOST SIZE           |
|-------------|----------|----|----|----|----|----|-------|---------------------|
| EC OFFSET   | 114h     |    |    |    |    |    | 8-bit | EC SIZE             |
| POWER       | VTR      |    |    |    |    |    | 00h   | nSYS_RST<br>DEFAULT |
| BUS         | LPC SPB  |    |    |    |    |    |       |                     |
| BYTE3 BIT   | D7       | D6 | D5 | D4 | D3 | D2 | D1    | D0                  |
| HOST TYPE   | -        | -  | -  | -  | -  | -  | -     | -                   |
| EC TYPE     | R        |    |    |    |    |    |       | R/W                 |
| BIT NAME    | Reserved |    |    |    |    |    |       | PCOBF               |

**Note 10.4** Refer to the [PCOBF Description](#) for information on this register. This is a “1” bit register (bits 1-7=0 on read)

## 10.9 EC-to-Host Keyboard Communication

The EC can write to the [EC\\_HOST Data/AUX Data Register](#) via EC OFFSET 100h or EC OFFSET 10Ch (Aux Host Data) respectively. A write to either of these addresses automatically sets bit 0 ([OBF](#)) in the Status register. A write to EC OFFSET 100h also sets [PCOBF](#). A write to EC OFFSET 10Ch also sets [AUXOBF](#). See [Table 10.9](#).

**Table 10.9 Host-Interface Flags**

| EC ADDRESS           | FLAG                                                  |
|----------------------|-------------------------------------------------------|
| EC OFFSET 100h (R/W) | <a href="#">PCOBF</a> (KIRQ) output signal goes high  |
| EC OFFSET 10Ch (W)   | <a href="#">AUXOBF</a> (MIRQ) output signal goes high |

The [HOST\\_EC Data / CMD Register](#) and [EC\\_HOST Data / AUX Data Register](#) are each 8 bits wide. A write to this 8 bit register by the EC will load the [EC\\_HOST Data / AUX Data Register](#), set the [OBF](#) flag and set the [PCOBF](#) output if enabled.

**Note 10.5** Refer to the [PCOBF](#) and [Keyboard Status Read Register](#) descriptions for more information.

### 10.9.1 PCOBF Description

(The following description assumes that OBFEN = 1 in [Keyboard Control Register on page 201](#)); PCOBF is gated onto KIRQ. The KIRQ signal is a system interrupt which signifies that the EC has written to the KBD Data Read register via EC OFFSET100h. On power-up, PCOBF is reset to 0. PCOBF will normally reflect the status of writes to EC OFFSET 100h, if PCOBFEN (bit 2 of Configuration register “0”) = “0”. (KIRQ is normally selected as IRQ1 for keyboard support). PCOBF is cleared by hardware on a HOST read of the [EC\\_HOST Data / AUX Data Register](#)

Additional flexibility has been added which allows firmware to directly control the PCOBF output signal, independent of data transfers to the host-interface data output register. This feature allows the

MEC5035 to be operated via the host “polled” mode. This firmware control is active when PCOBFEN = 1 and firmware can then bring PCOBF high by writing a “1” to the LSB of the 1 bit data register, PCOBF, at EC OFFSET 114h. The firmware must also clear this bit by writing a “0” to the LSB of the 1 bit data register at EC OFFSET 114h.

The PCOBF register is also readable; bits 1-7 will return a “0” on the read back. The value read back on bit 0 of the register always reflects the present value of the PCOBF output. If PCOBFEN = 1, then this value reflects the output of the firmware latch at EC OFFSET 114h. If PCOBFEN = 0, then the value read back reflects the in-process status of write cycles to EC OFFSET 100h (i.e., if the value read back is high, the host interface output data register has just been written to). If OBFEN=0, then KIRQ is driven inactive (low).

## 10.9.2 AUXOBF1 Description

(The following description assumes that OBFEN = 1 in [Keyboard Control Register on page 201](#)); This bit is multiplexed onto MIRQ. The AUXOBF1/MIRQ signal is a system interrupt which signifies that the EC has written to the [EC\\_HOST Data / AUX Data Register](#).

On power-up, after nSYS\_RST, AUXOBF1 is reset to 0. AUXOBF1 will normally reflects the status of writes to EC OFFSET 10Ch. (MIRQ is normally selected as IRQ12 for mouse support). AUXOBF1 is cleared by hardware on a read of the Host Data Register. If OBFEN=0, then KIRQ is driven inactive (low).

**Table 10.10 Status and Interrupt Behavior of Writing to Output Data Register**

|                   | HOST I/F STATUS REGISTER BITS |          |         |         |
|-------------------|-------------------------------|----------|---------|---------|
| Write to Register | AUXOBF (D5)                   | OBF (D0) | OBFEN=0 | OBFEN=1 |
| EC OFFSET 100h    | 0                             | 1        | KIRQ=0  | KIRQ=1  |
| EC OFFSET 10Ch    | 1                             | 1        | MIRQ=0  | MIRQ=1  |

**Table 10.11 OBFEN and PCOBFEN Effects on KIRQ**

| OBFEN | PCOBFEN |                                 |
|-------|---------|---------------------------------|
| 0     | X       | KIRQ is inactive and driven low |
| 1     | 0       | KIRQ = PCOBF@EC OFFSET 100h     |
| 1     | 1       | KIRQ = PCOBF@EC OFFSET 114h     |

**Table 10.12 OBFEN and AUXH Effects on MIRQ**

| OBFEN | AUXH |                                                                       |
|-------|------|-----------------------------------------------------------------------|
| 0     | X    | MIRQ is inactive and driven low                                       |
| 1     | 0    | MIRQ = PCOBF@EC OFFSET 10Ch; Status Register D5 = User Defined        |
| 1     | 1    | MIRQ = PCOBF@EC OFFSET 10Ch; Status Register D5 = Hardware Controlled |

### 10.9.2.1 Keyboard Control

**Table 10.13 Keyboard Control Register**

|             |         |     |       |       |     |             |                     |     |
|-------------|---------|-----|-------|-------|-----|-------------|---------------------|-----|
| HOST OFFSET | NA      |     |       | 8-bit |     |             | HOST SIZE           |     |
| EC OFFSET   | 108h    |     |       | 8-bit |     |             | EC SIZE             |     |
| POWER       | VTR     |     |       | 00h   |     |             | nSYS_RST<br>DEFAULT |     |
| BUS         | LPC SPB |     |       |       |     |             |                     |     |
| BYTE3 BIT   | D7      | D6  | D5    | D4    | D3  | D2          | D1                  | D0  |
| HOST TYPE   | -       | -   | -     | -     | -   | -           | -                   | -   |
| EC TYPE     | R/W     | R/W | R/W   | R/W   | R/W | R/W         | R/W                 | R/W |
| BIT NAME    | AUXH    | UD  | OBFEN | UD    | UD  | PCOBF<br>EN | SAEN                | UD  |

#### UD

user defined bit

#### AUXH

Aux in Hardware; when high, [AUXOBF](#) of the status register is set in hardware by a write to EC OFFSET 10Ch. When low, [AUXOBF](#) of the status register is a user defined bit (UD) and R/W.

#### OBFFEN

When set, [PCOBF](#) is gated onto KIRQ and [AUXOBF1](#) is gated onto MIRQ. When low, KIRQ and MIRQ are driven low. Software should not change this bit when [OBF](#) of the status register is equal to 1.

#### PCOBFEN

When high, [PCOBF](#) reflects whatever value was written to the [PCOBF](#) firmware latch assigned to 114h. When low, [PCOBF](#) reflects the status of writes to EC OFFSET 100h (the output data register).

#### SAEN

Software-assist enable. When set to "1," [SAEN](#) allows control of the [GATEA20](#) signal via firmware. If [SAEN](#) is reset to '0', [GATEA20](#) corresponds to either the last host-initiated control of [GATEA20](#) or the firmware write to EC OFFSETs 118h or 11Ch.

## 10.10 Legacy Support

## 10.11 Port92-Legacy Registers

The [Table 10.14](#) is a register summary for the [Port92-Legacy](#) block. The LPC I/O address of the [PORT92 Register](#) is fixed. Each EC address is indicated as an SPB Offset from its AHB base address listed for the [Port92-Legacy](#) block in [Table 10.2, "8042 Emulated Keyboard Controller Base Address Table," on page 194](#). Each Configuration register access through the [Host Access Port](#) address via its LND indicated in [Table 10.2 on page 194](#) and its [Host Access Port](#) index which is described as "Host Config Index" in the tables below.

Table 10.14 Port92-Legacy Support Register Summary

|                          | HOST I/O ACCESS    |            |           | EC INTERFACE |           |         | NOTES |
|--------------------------|--------------------|------------|-----------|--------------|-----------|---------|-------|
| REGISTER NAME            | HOST I/O ADDRESS   | SPB OFFSET | HOST TYPE | SPB OFFSET   | BYTE LANE | EC TYPE |       |
| GATEA20 Control Register | -                  | -          | -         | 100h         | 0         | R       |       |
| SETGA20L Register        | -                  | -          | -         | 108h         | 0         | W       |       |
| RSTGA20L Register        | -                  | -          | -         | 10Ch         | 0         | W       |       |
| PORT92 Register          | 92h                | 000h       | R/W       | 000h         | 0         | R/W     |       |
|                          | HOST ACCESS        |            |           | EC INTERFACE |           |         |       |
| REGISTER NAME            | HOST CONFIG. INDEX | SPB OFFSET | HOST TYPE | SPB OFFSET   | BYTE LANE | EC TYPE |       |
| PORT92 Enable Register   | 30h                | 3F0h       | R/W       | 330h         | 0         | R/W     |       |

**Note 10.6** CMD is bit D3 in the [Keyboard Status Read Register](#).

All Registers listed in [Table 10.14](#) are powered by VTR and reset by nSYS\_RST except the [PORT92 Register](#) which is powered by VTR and reset by nSIO\_RESET (See [Section , "iRESET OUT," on page 109](#)).

## 10.12 Configuration Registers

### 10.12.1 Port 92 Enable

The MEC5035 supports LPC I/O writes to port 92h as a quick alternate mechanism for generating a CPU\_RESET pulse or controlling the state of [GATEA20](#).

**Table 10.15 PORT92 Enable Register**

|                   |          |    |    |    |       |    |    |                     |  |
|-------------------|----------|----|----|----|-------|----|----|---------------------|--|
| HOST CONFIG INDEX | 30h      |    |    |    | 8-bit |    |    | HOST SIZE           |  |
| EC OFFSET         | 330h     |    |    |    | 8-bit |    |    | EC SIZE             |  |
| POWER             | VTR      |    |    |    | 00h   |    |    | nSYS_RST<br>DEFAULT |  |
| BUS               | LPC SPB  |    |    |    |       |    |    |                     |  |
| BYTE3 BIT         | D7       | D6 | D5 | D4 | D3    | D2 | D1 | D0                  |  |
| HOST TYPE         | R        |    |    |    |       |    |    | R/W                 |  |
| EC TYPE           | -        | -  | -  | -  | -     | -  | -  | -                   |  |
| BIT NAME          | Reserved |    |    |    |       |    |    | P92_EN              |  |

## 10.13 Runtime registers

### 10.13.1 Port 92

The MEC5035 supports LPC I/O writes to port HOST I/O address 92h as a quick alternate mechanism for generating a CPU\_RESET pulse or controlling the state of [GATEA20](#).

The [PORT92 Register](#) resides at HOST I/O address 92h and is used to support the alternate reset (ALT\_RST#) and alternate [GATEA20](#) (ALT\_A20) functions. This register defaults to 00h on assertion of [nSIO\\_RESET](#) (See [Section , "iRESET OUT," on page 109](#)).

Setting the Port92 Enable bit ([PORT92 Enable Register](#)) enables the Port92h Register. When Port92 is disabled, by clearing the Port92 Enable bit, then access to this register is completely disabled (I/O writes to host 92h are ignored and I/O reads float the system data bus SD[7:0]).

**Table 10.16 PORT92 Register**

|                  |          |    |    |       |    |    |                           |               |
|------------------|----------|----|----|-------|----|----|---------------------------|---------------|
| HOST I/O ADDRESS | 0092h    |    |    | 8-bit |    |    | HOST SIZE                 |               |
| EC OFFSET        | 00h      |    |    | 8-bit |    |    | EC SIZE                   |               |
| POWER            | VTR      |    |    | 00h   |    |    | nSIO_RESET DEFAULT        |               |
| BUS              | LPC SPB  |    |    |       |    |    |                           |               |
| BYTE3 BIT        | D7       | D6 | D5 | D4    | D3 | D2 | D1                        | D0            |
| HOST TYPE        | R        |    |    |       |    |    | R/W                       | R/W           |
| EC TYPE          | -        | -  | -  | -     | -  | -  | -                         | -             |
| BIT NAME         | Reserved |    |    |       |    |    | ALT_GATE A20 <sup>−</sup> | ALT_CPU_RESET |

#### ALT\_CPU\_RESET

This bit provides an alternate means to generate a CPU\_RESET pulse. The CPU\_RESET output provides a means to reset the system CPU to effect a mode switch from Protected Virtual Address Mode to the Real Address Mode. This provides a faster means of reset than is provided through the EC keyboard controller. Writing a “1” to this bit will cause the ALT\_RST# internal signal to pulse (active low) for a minimum of 6μs after a delay of 14μs. Before another ALT\_RST# pulse can be generated, this bit must be written back to “0”.

#### ALT\_GATEA20

This bit provides an alternate means for system control of the MEC5035 GATEA20 pin.

0=ALT\_A20 is driven low  
1=ALT\_A20 is driven high

When Port 92 is enabled, writing a 0 to bit 1 of the [PORT92 Register](#) forces ALT\_A20 low. ALT\_A20 low drives GATEA20 low, if A20 from the keyboard controller is also low. When Port 92 is enabled, writing a 1 to bit 1 of the [PORT92 Register](#) forces ALT\_A20 high. ALT\_A20 high drives GATEA20 high regardless of the state of A20 from the keyboard controller.

### 10.13.2 GATE A20

The MEC5035 contains on-chip logic support for the [GATEA20](#) hardware speed-up feature. [GATEA20](#) is part of the control required to mask address line A20 to emulate 8086 addressing.

In addition to the ability for the host to control the [GATEA20](#) output signal directly, a configuration bit called “SAEN” (Software Assist Enable, bit 1 of [Keyboard Control Register](#) is provided; when set, SAEN allows firmware to control the [GATEA20](#) output.

When SAEN is set, a 1 bit register assigned to EC OFFSET110h controls the [GATEA20](#) output. The register bit allocation is shown in [Table 10.13](#).

**Note 10.7** Refer to the [GATEA20 Control](#) description for information on this register. This is a one bit register (Bits 1-7=0 on read)

### 10.13.3 GATEA20 Control

**Table 10.17 GATEA20 Control Register**

|                    |           |           |           |           |           |           |           |                             |
|--------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------------------------|
| <b>HOST OFFSET</b> | NA        |           |           |           |           |           | 8-bit     | <b>HOST SIZE</b>            |
| <b>EC OFFSET</b>   | 100h      |           |           |           |           |           | 8-bit     | <b>EC SIZE</b>              |
| <b>POWER</b>       | VTR       |           |           |           |           |           | 00h       | <b>nSYS_RST<br/>DEFAULT</b> |
| <b>BUS</b>         | LPC SPB   |           |           |           |           |           |           |                             |
| <b>BYTE3 BIT</b>   | <b>D7</b> | <b>D6</b> | <b>D5</b> | <b>D4</b> | <b>D3</b> | <b>D2</b> | <b>D1</b> | <b>D0</b>                   |
| <b>HOST TYPE</b>   | -         | -         | -         | -         | -         | -         | -         | -                           |
| <b>EC TYPE</b>     | R         |           |           |           |           |           |           | R/W                         |
| <b>BIT NAME</b>    | Reserved  |           |           |           |           |           |           | GATEA20                     |

#### GATEA20

Writing a “0” into bid GATEA20 causes the [GATEA20](#) output to go low, and vice versa.

Host control and firmware control of [GATEA20](#) affect two separate register elements. Read back of [GATEA20](#) through the use of EC OFFSET 110h reflects the present state of the [GATEA20](#) output signal: if [SAEN](#) is set, the value read back corresponds to the last firmware-initiated control of [GATEA20](#); if [SAEN](#) is reset, the value read back corresponds to the last host-initiated control of [GATEA20](#).

Host control of the [GATEA20](#) output is provided by the hardware interpretation of the “[GATEA20](#) sequence” (see [Table 10.18](#)). The foregoing description assumes that the [SAEN](#) configuration bit is reset.

When the MEC5035 receives a “D1” command followed by data (via the host interface), the on-chip hardware copies the value of data bit 1 in the received data field to the [GATEA20](#) host latch. At no time during this host-interface transaction will [PCOBF](#) or the [IBF](#) flag (bit 1) in the [Keyboard Status Read Register](#) be activated; for example, this host control of [GATEA20](#) is transparent to firmware, with no consequent degradation of overall system performance. [Table 10.18](#) details the possible [GATEA20](#) sequences and the MEC5035 responses.

On [VCC\\_POR](#), [GATEA20](#) will be set.

An additional level of control flexibility is offered via a memory-mapped synchronous set and reset capability. Any data written to EC OFFSET 118h causes the [GATEA20](#) host latch to be set; any data written to EC OFFSET 11Ch causes it to be reset. This control mechanism should be used with caution. It was added to augment the “normal” control flow as described above, not to replace it. Since the host and the firmware have asynchronous control capability of the host latch via this mechanism, a potential conflict could arise. Therefore, after using the EC OFFSET 118h and EC OFFSET 11Ch addresses, firmware should read back the [GATEA20](#) status via EC OFFSET 110h (with [SAEN](#) = 0) to confirm the actual [GATEA20](#) response.



**Table 10.18 GATEA20 Command/Data Sequence Examples**

| DATA BYTE        | R/W              | D[0:7]               | IBF FLAG         | GATEA20          | COMMENTS                     |
|------------------|------------------|----------------------|------------------|------------------|------------------------------|
| 1<br>0<br>1      | W<br>W<br>W      | D1<br>DF<br>FF       | 0<br>0<br>0      | Q<br>1<br>1      | GATEA20 Turn-on Sequence     |
| 1<br>0<br>1      | W<br>W<br>W      | D1<br>DD<br>FF       | 0<br>0<br>0      | Q<br>0<br>0      | GATEA20 Turn-off Sequence    |
| 1<br>1<br>0<br>1 | W<br>W<br>W<br>W | D1<br>D1<br>DF<br>FF | 0<br>0<br>0<br>0 | Q<br>Q<br>1<br>1 | GATEA20 Turn-on Sequence(*)  |
| 1<br>1<br>0<br>1 | W<br>W<br>W<br>W | D1<br>D1<br>DD<br>FF | 0<br>0<br>0<br>0 | Q<br>Q<br>0<br>0 | GATEA20 Turn-off Sequence(*) |
| 1<br>1<br>1      | W<br>W<br>W      | D1<br>XX**<br>FF     | 0<br>1<br>1      | Q<br>Q<br>Q      | Invalid Sequence             |

**Note 10.8**

- All examples assume that the SAEN configuration bit is 0.
- "Q" indicates the bit remains set at the previous state.
- \*Not a standard sequence.
- \*\*XX = Anything except D1.
- If multiple data bytes, set IBF and wait at state 0. Let the software know something unusual happened.
- For data bytes, only D[1] is used; all other bits are don't care.



Table 10.19 SETGA20L Register

|             |         |    |    |    |       |    |    |                     |  |
|-------------|---------|----|----|----|-------|----|----|---------------------|--|
| HOST OFFSET | NA      |    |    |    | 8-bit |    |    | HOST SIZE           |  |
| EC OFFSET   | 108h    |    |    |    | 8-bit |    |    | EC SIZE             |  |
| POWER       | VTR     |    |    |    | 00h   |    |    | nSYS_RST<br>DEFAULT |  |
| BUS         | LPC SPB |    |    |    |       |    |    |                     |  |
| BYTE3 BIT   | D7      | D6 | D5 | D4 | D3    | D2 | D1 | D0                  |  |
| HOST TYPE   | -       | -  | -  | -  | -     | -  | -  | -                   |  |
| EC TYPE     | W       |    |    |    |       |    |    |                     |  |
| BIT NAME    |         |    |    |    |       |    |    |                     |  |

**Note 10.9** Refer to the [GATEA20](#) Hardware Speed-up description for information on this register. A write to this register sets [GATEA20](#).

Table 10.20 RSTGA20L Register

|             |         |    |    |    |       |    |    |                     |  |
|-------------|---------|----|----|----|-------|----|----|---------------------|--|
| HOST OFFSET | NA      |    |    |    | 8-bit |    |    | HOST SIZE           |  |
| EC OFFSET   | 10Ch    |    |    |    | 8-bit |    |    | EC SIZE             |  |
| POWER       | VTR     |    |    |    | 00h   |    |    | nSYS_RST<br>DEFAULT |  |
| BUS         | LPC SPB |    |    |    |       |    |    |                     |  |
| BYTE3 BIT   | D7      | D6 | D5 | D4 | D3    | D2 | D1 | D0                  |  |
| HOST TYPE   | -       | -  | -  | -  | -     | -  | -  | -                   |  |
| EC TYPE     | W       |    |    |    |       |    |    |                     |  |
| BIT NAME    |         |    |    |    |       |    |    |                     |  |

**Note 10.10** Refer to the [GATEA20](#) Hardware Speed-up description for information on this register. A write to this register re-sets [GATEA20](#).

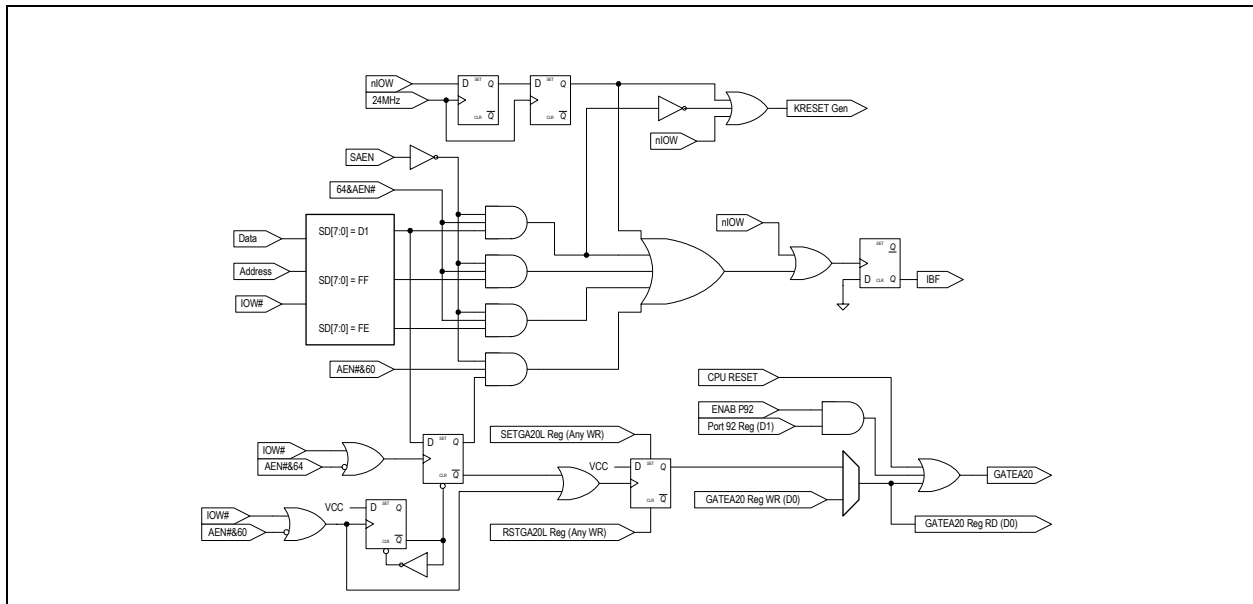


**Figure 10.2 GATEA20 Implementation Diagram**

**Note 10.11** Host Commands (FF, FE, & D1) do not cause IBF. The method of blocking IBF in [Figure 10.2](#) is the nIOW not being asserted when FF, FE, & D1 Host commands are written”.

The hardware [GATEA20](#) state machine returns to state S1 from state S2 when CMD = D1 ([Figure 10.3](#)).

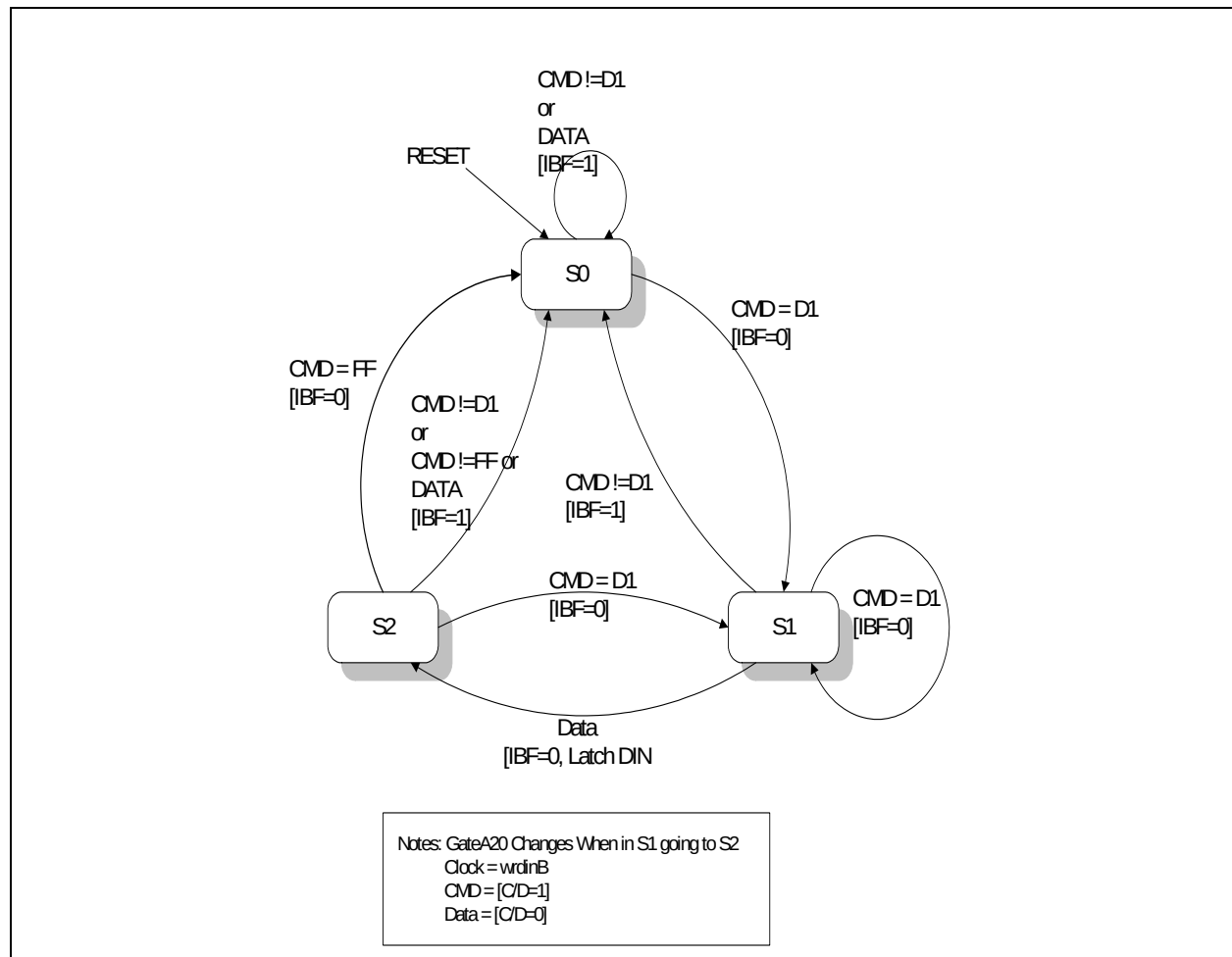


Figure 10.3 GATEA20 State Machine

## 10.14 CPU\_RESET Hardware Speed-Up

The [ALT\\_CPU\\_RESET](#) bit generates, under program control, the ALT\_RST# signal, which provides an alternate, means to drive the MEC5035 CPU\_RESET pin which in turn is used to reset the Host CPU. The ALT\_RST# signal is internally NANDed together with the KBDRESET# pulse from the KRESET Speed up logic to provide an alternate software means of resetting the host CPU.

**Note 10.12** Before another ALT\_RST# pulse can be generated, [ALT\\_CPU\\_RESET](#) must be cleared to "0" either by an [nSIO\\_RESET](#) (See [Section , "iRESET OUT," on page 109](#)) or by a write to the [PORT92 Register](#) with bit 0 = "0". A ALT\_RST# pulse is not generated in the event that the [ALT\\_CPU\\_RESET](#) bit is cleared and set before the prior ALT\_RESET# pulse has completed.

**Note 10.13** This function is qualified by the SLP\_EN signal or the [Activate](#) bit. If either of these signals goes to '0', then the 1MHz clocks source is disabled if the PGEN is not currently active. See [EC Blocks Sleep Enables Register Bit Names on page 111](#) & [Section 4.4.7.4.4, "Block Sleep Enables," on page 91](#).

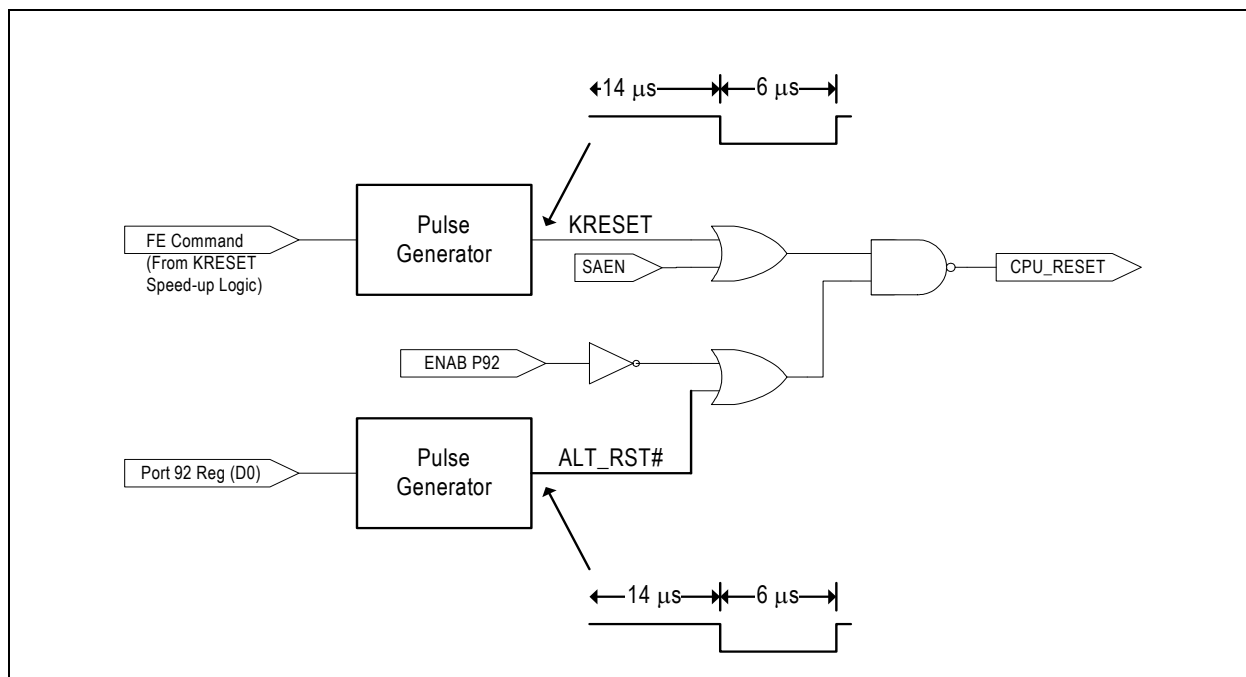


**Figure 10.4 CPU\_RESET Implementation Diagram**

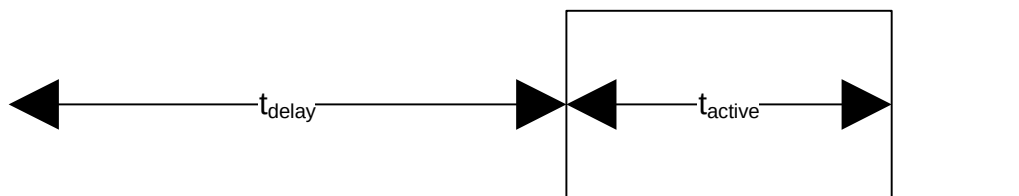


**Figure 10.14 CPU\_RESET timing**

**Table 10.21 CPU\_RESET Timing Parameters**

| NAME               | DESCRIPTION                 | MIN | TYP | MAX  | UNITS         |
|--------------------|-----------------------------|-----|-----|------|---------------|
| $t_{\text{delay}}$ | Delay prior to active pulse | 14  | 15  | 15.5 | $\mu\text{s}$ |
| $t_{\text{delay}}$ | Delay prior to active pulse | 6   | 8   | 8.5  | $\mu\text{s}$ |

**Note 10.15** Figure 10.14 & Table 10.21 refers to Figure 10.4 in which CPU\_RESET is the inverse of ALT\_RST# & KRESET.

## 10.15 8042 Emulated Keyboard Controller Revision History

This revision history shows the changes made to this chapter.

**Table 10.22 8042 Emulated Keyboard Controller Chapter Revision History**

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History," on page 539.</a> |              |            |                                                                                                                                                                                                                                                                                                                                                                                                                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE       | SECTION/FIGURE/ENTRY                                                                                                                                                                                                                                                                                                                                                                                                 | CORRECTION                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 1.                                                                                                                                                                                                                                          |              | 04/23/2007 | <a href="#">Figure 10.4 CPU_RESET Implementation Diagram on page 210</a><br><a href="#">Figure 10.14 Table 10.21, Note 10.15, Note 10.11 on page 208</a><br><br><a href="#">Table 10.17, "GATEA20 Control Register," on page 205</a><br><br><a href="#">Table 10.14 on page 202</a><br><a href="#">Table 10.17 on page 205</a><br><a href="#">Table 10.19 on page 207</a><br><a href="#">Table 10.20 on page 207</a> | <ul style="list-style-type: none"> <li>■ Change AND gate to NAND gate</li> <li>■ Added to Clarify CPU_RESET requirements</li> <li>■ Host Commands (FF, FE, &amp; D1) do not cause IBF.</li> <li>■ Change default from 0h to 1h.</li> <li>■ Change <a href="#">GATEA20 Control Register</a>, <a href="#">SETGA20L Register</a>, <a href="#">RSTGA20L Register</a> AHB address offsets from 110h, 118h, &amp; 11Ch to 100h, 108h, &amp; 10Ch.</li> </ul> |
| 2.                                                                                                                                                                                                                                          |              |            |                                                                                                                                                                                                                                                                                                                                                                                                                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 3.                                                                                                                                                                                                                                          |              |            |                                                                                                                                                                                                                                                                                                                                                                                                                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 4.                                                                                                                                                                                                                                          |              |            |                                                                                                                                                                                                                                                                                                                                                                                                                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

## Chapter 11 ACPI PM1 Block Interface

### 11.1 General Description

The MEC5035 supports ACPI as described in this section. These features comply with the ACPI Specification, Revision 1.0, through a combination of hardware and EC software.

The MEC5035 implements the ACPI fixed registers but includes only those bits that apply to the power button sleep button and RTC alarm events. The ACPI [WAK\\_ SLP\\_TYPx](#), and [SLP\\_](#) bits are also supported.

### 11.2 Power, Clocks and Reset

#### 11.2.1 Power Domain

This block is powered by VTR

See [Section 4.5, "Power Configuration," on page 96](#) for details on power domains.

#### 11.2.2 Clocks

This block has one clock input, the [LPC Bus Clock](#).

See [Section 4.4, "Clock Generator," on page 77](#) for details on clocks.

#### 11.2.3 Power On Reset

This block is reset on a [nSYS\\_RST](#). After [nSYS\\_RST](#) is asserted, all registers are set to '0'.

See [Section 4.6, "Reset Interface," on page 99](#) for details on reset.

### 11.3 Interrupts

#### 11.3.1 SCI Interrupts to the Host

The functions described in the following sub-sections can generate a SCI event on the EC\_SCI# pin. In the MEC5035, an SCI event is considered the same as an ACPI wakeup or runtime event. The EC can also generate a SCI on the EC\_SCI# pin by setting the [EC\\_SCI\\_](#) bit in the [EC\\_SCI# Pin Interface on page 220](#).

#### 11.3.2 Interrupts to the EC

An Interrupt is generated to the EC on [PM1\\_CTL2](#) bit of [IRQ13 Source Register](#) by the Host writing to [Power Management 1 Control Register 2 \(PM1\\_CNTRL 2\)](#)

An Interrupt is generated to the EC on [PM1\\_EN2](#) bit of [IRQ13 Source Register](#) by the Host writing to [Power Management 1 Enable Register 2 \(PM1\\_EN 2\)](#)

An Interrupt is generated to the EC on [PM1\\_STS2](#) bit of [IRQ13 Source Register](#) by the Host writing to [Power Management 1 Status Register 2 \(PM1\\_STS 2\)](#)

### 11.3.3 ACPI PM1 Block SCI Event-Generating Functions

#### 11.3.3.1 Power Button with Override

The power button has a status and an enable bit in the PM1\_BLK of registers to provide an SCI upon the button press. The status bit is software Read/Writable by the EC; the enable bit is Read-only by the EC. It also has a status and enable bit in the PM1\_BLK of registers to indicate and control the power button override (fail-safe) event. These bits are not required by ACPI. The power button override event status bit is software Read/Writable by the EC; the enable bit is software read-only by the EC. The enable bit for the override event is located at bit 1 in the [Power Management 1 Control Register 2 \(PM1\\_CNTRL 2\)](#).

The [PWRBTN\\_](#) bit is set by the Host to enable the generation of an SCI due to the power button event. The status bit is set by the EC when it generates a power button event and is cleared by the Host writing a '1' to this bit (writing a '0' has no effect); it can also be cleared by the EC. If the enable bit is set, the EC will generate an SCI power management event.

#### 11.3.3.2 Sleep Button

The sleep button has a status and an enable bit in the PM1\_BLK of registers to provide an SCI upon the button press. The status bit is software Read/Writable by the EC; the enable bit is Read-only by the EC.

The [SLPBTN\\_](#) bit is set by the Host to enable the generation of an SCI due to the sleep button event. The status bit is set by the EC when it generates a sleep button event and is cleared by the Host writing a '1' to this bit (writing a '0' has no effect); it can also be cleared by the EC. If the enable bit is set, the EC will generate an SCI power management event.

#### 11.3.4 RTC Alarm

The ACPI specification requires that the RTC alarm generate a hardware wake-up event from the sleeping state. The RTC alarm can be enabled as an SCI event and its status can be determined through bits in the PM1\_BLK of registers. The status bit is software Read/Writable by the EC; the enable bit is Read-only by the EC.

The [RTC\\_](#) bit is set by the Host to enable the generation of an SCI due to the RTC alarm event. The status bit is set by the EC when the RTC generates an alarm event and is cleared by the Host writing a '1' to this bit (writing a '0' has no effect); it can also be cleared by the EC. If the enable bit is set, the 8051 will generate an SCI power management event.

## 11.4 Registers

Each instance of the [ACPI PM1 Block Interface](#) has its own Logical Device Number, and Base Address as indicated in [Table 11.1](#).

**Table 11.1** [ACPI PM1 Block Interface](#) Base Address Table

| <a href="#">ACPI PM1 Block Interface</a><br>INSTANCE | LDN | AHB BASE ADDRESS         |
|------------------------------------------------------|-----|--------------------------|
| <a href="#">ACPI PM1 Block Interface</a>             | 5h  | <a href="#">FF_1400h</a> |

The ACPI register model consists of a number of fixed register blocks that perform designated functions. A register block consists of a number of registers that perform Status, Enable and Control functions. The ACPI specification deals with events (which have an associated interrupt status and enable bits, and sometimes an associated control function) and control features. The status registers



illustrate what defined function is requesting ACPI interrupt services (SCI). Any status bit in the ACPI specification has the following attributes:

Status bits are only set through some defined hardware or EC event.

Unless otherwise noted, status bits are cleared by the system writing a “1” to that bit position, and upon [nSYS\\_RST](#). Writing a ‘0’ has no effect.

Status bits only generate interrupts while their associated bit in the enable register is set.

Function bit positions in the status register have the same bit position in the enable register (there are exceptions to this rule, special status bits have no enables).

Note that this implies that if the respective enable bit is reset and the hardware event occurs, the respective status bit is set; however no interrupt is generated until the enable bit is set. This allows software to test the state of the event (by examining the status bit) without necessarily generating an interrupt. There are a special class of status bits that have no respective enable bit, these are called out specifically, and the respective enable bit in the enable register is marked as reserved for these special cases.

The enable registers allow the setting of the status bit to generate an interrupt (under EC control). As a general rule, there is an enable bit in the enable register for every status bit in the status register. The control register provides special controls for the associated event, or special control features that are not associated with an interrupt event. The order of a register block is the status registers, followed by enable registers, followed by control registers.

The registers in the MEC5035 [ACPI PM1 Block Interface](#) occupy eight addresses in the host I/O space and are specified as offsets from the ACPI PM1 Block base address ([Table 11.1](#)).

**Table 11.2 ACPI PM1 Block Interface Register Summary**

| REGISTER NAME                                                       | HOST ACCESS    |            |           | EC ACCESS  |           |         | NOTES                                                   |
|---------------------------------------------------------------------|----------------|------------|-----------|------------|-----------|---------|---------------------------------------------------------|
|                                                                     | HOST I/O INDEX | SPB OFFSET | HOST TYPE | SPB OFFSET | BYTE LANE | EC TYPE |                                                         |
| <a href="#">Power Management 1 Status Register 1 (PM1_STS) 1</a>    | 0h             | 00h        | R         | 100h       | 0         | R       |                                                         |
| <a href="#">Power Management 1 Status Register 2 (PM1_STS) 2</a>    | 1h             | 01h        | R/WC      | 101h       | 1         | R/W     | <a href="#">Table 11.4</a><br><a href="#">Note 11.4</a> |
| <a href="#">Power Management 1 Enable Register 1 (PM1_EN) 1</a>     | 2h             | 02h        | R         | 102h       | 2         | R       |                                                         |
| <a href="#">Power Management 1 Enable Register 2 (PM1_EN) 2</a>     | 3h             | 03h        | R/W       | 103h       | 3         | R       | <a href="#">Table 11.6</a><br><a href="#">Note 11.5</a> |
| <a href="#">Power Management 1 Control Register 1 (PM1_CNTRL) 1</a> | 4h             | 04h        | R         | 104h       | 0         | R       |                                                         |
| <a href="#">Power Management 1 Control Register 2 (PM1_CNTRL) 2</a> | 5h             | 05h        | R/W       | 105h       | 1         | R       | <a href="#">Table 11.8</a><br><a href="#">Note 11.6</a> |
| <a href="#">Power Management 2 Control Register 1 (PM2_CNTRL) 1</a> | 6h             | 06h        | R         | 106h       | 2         | R       | <a href="#">Note 11.2</a>                               |

Table 11.2 ACPI PM1 Block Interface Register Summary

| REGISTER NAME                                       | HOST ACCESS    |            |           | EC ACCESS  |           |         | NOTES     |
|-----------------------------------------------------|----------------|------------|-----------|------------|-----------|---------|-----------|
|                                                     | HOST I/O INDEX | SPB OFFSET | HOST TYPE | SPB OFFSET | BYTE LANE | EC TYPE |           |
| Power Management 2 Control Register 2 (PM2_CNTRL 2) | 7h             | 07h        | R         | 107h       | 3         | R       | Note 11.2 |
| EC_PM_STS Register                                  | -              | -          | -         | 110h       | 0         | R/W     |           |
| REGISTER NAME                                       | HOST ACCESS    |            |           | EC ACCESS  |           |         | NOTES     |
|                                                     | HOST I/O INDEX | SPB OFFSET | HOST TYPE | SPB OFFSET | BYTE LANE | EC TYPE |           |

**Note 11.1** Byte 0 of this register is reserved

**Note 11.2** These registers return '0' when read, writes have no effect

#### 11.4.1 Power Management 1 Status 1 (PM1\_STS 1)

Table 11.3 Power Management 1 Status Register 1 (PM1\_STS) 1

| HOST OFFSET | 0h       |    |    | 8-bit |    |    | HOST SIZE           |    |
|-------------|----------|----|----|-------|----|----|---------------------|----|
| EC OFFSET   | 100h     |    |    |       |    |    | EC SIZE             |    |
| POWER       | VTR      |    |    | 00h   |    |    | nSYS_RST<br>DEFAULT |    |
| BUS         | LPC SPB  |    |    |       |    |    |                     |    |
| BYTE0 BIT   | D7       | D6 | D5 | D4    | D3 | D2 | D1                  | D0 |
| HOST TYPE   | R        | R  | R  | R     | R  | R  | R                   | R  |
| EC TYPE     | R        | R  | R  | R     | R  | R  | R                   | R  |
| BIT NAME    | Reserved |    |    |       |    |    |                     |    |

#### RESERVED

Reserved bits return '0' when read.

## 11.4.2 Power Management 1 Status 2 (PM1\_STS 2)

**Table 11.4 Power Management 1 Status Register 2 (PM1\_STS 2)**

| HOST OFFSET | 1h      |          |    |    | 8-bit        |         | HOST SIZE           |            |
|-------------|---------|----------|----|----|--------------|---------|---------------------|------------|
| EC OFFSET   | 101h    |          |    |    |              |         | EC SIZE             |            |
| POWER       | VTR     |          |    |    | 00h          |         | nSYS_RST<br>DEFAULT |            |
| BUS         | LPC SPB |          |    |    |              |         |                     |            |
| BYTE0 BIT   | D7      | D6       | D5 | D4 | D3           | D2      | D1                  | D0         |
| HOST TYPE   | R/WC    | R        | R  | R  | R/WC         | R/WC    | R/WC                | R/WC       |
| EC TYPE     | R/W     | R        | R  | R  | R/W          | R/W     | R/W                 | R/W        |
| BIT NAME    | WAK_STS | Reserved |    |    | PWRBTNOR_STS | RTC_STS | SLPBTN_STS          | PWRBTN_STS |

**Note 11.3** These bits are set/cleared by the EC directly i.e., writing '1' sets the bit and writing '0' clears it. These bits can also be cleared by the Host software writing a one to this bit position and by nSYS\_RST. Writing a 0 by the Host has no effect.

**Note 11.4** An interrupt (PM1\_CTL2) is generated to the EC when the Host writes to this register.

### PWRBTN\_STS

This bit can be set or cleared by the EC to simulate a Power button status if the power is controlled by the EC. The Host writing a one to this bit can also clear this bit. The EC must generate the associated SCI interrupt under software control.

### SLPBTN\_STS

This bit can be set or cleared by the EC to simulate a Sleep button status if the sleep state is controlled by the EC. The Host writing a one to this bit can also clear this bit. The EC must generate the associated SCI interrupt under software control.

### RTC\_STS

This bit can be set or cleared by the EC to simulate a RTC status. The Host writing a one to this bit can also clear this bit. The EC must generate the associated SCI interrupt under software control.

### PWRBTNOR\_STS

This bit can be set or cleared by the EC to simulate a Power button override event status if the power is controlled by the EC. The Host writing a one to this bit can also clear this bit. The EC must generate the associated hardware event under software control.

### WAK\_STS

This bit can be set or cleared by the EC. The Host writing a one to this bit can also clear this bit.

### 11.4.3 Power Management 1 Enable 1 (PM1\_EN 1)

**Table 11.5 Power Management 1 Enable Register 1 (PM1\_EN 1)**

|             |          |    |    |       |    |    |                     |    |
|-------------|----------|----|----|-------|----|----|---------------------|----|
| HOST OFFSET | 02h      |    |    | 8-bit |    |    | HOST SIZE           |    |
| EC OFFSET   | 102h     |    |    |       |    |    | EC SIZE             |    |
| POWER       | VTR      |    |    | 00h   |    |    | nSYS_RST<br>DEFAULT |    |
| BUS         | LPC SPB  |    |    |       |    |    |                     |    |
| BYTE0 BIT   | D7       | D6 | D5 | D4    | D3 | D2 | D1                  | D0 |
| HOST TYPE   | R        | R  | R  | R     | R  | R  | R                   | R  |
| EC TYPE     | R        | R  | R  | R     | R  | R  | R                   | R  |
| BIT NAME    | Reserved |    |    |       |    |    |                     |    |

#### RESERVED

Reserved bits return '0' when read.

### 11.4.4 Power Management 1 Enable 2 (PM1\_EN 2)

**Table 11.6 Power Management 1 Enable Register 2 (PM1\_EN 2)**

|             |          |    |    |    |       |        |           |                  |  |
|-------------|----------|----|----|----|-------|--------|-----------|------------------|--|
| HOST OFFSET | 03h      |    |    |    | 8-bit |        |           | HOST SIZE        |  |
| EC OFFSET   | 103h     |    |    |    |       |        |           | EC SIZE          |  |
| POWER       | VTR      |    |    |    | 00h   |        |           | nSYS_RST DEFAULT |  |
| BUS         | LPC SPB  |    |    |    |       |        |           |                  |  |
| BYTE0 BIT   | D7       | D6 | D5 | D4 | D3    | D2     | D1        | D0               |  |
| HOST TYPE   | R        | R  | R  | R  | R     | R/W    | R/W       | R/W              |  |
| EC TYPE     | R        | R  | R  | R  | R     | R      | R         | R                |  |
| BIT NAME    | Reserved |    |    |    |       | RTC_EN | SLPBTN_EN | PWRBTN_EN        |  |

**Note 11.5** An interrupt (PM1\_EN2) is generated to the EC when the Host writes to this register.

#### PWRBTN\_EN

This bit can be read or written by the Host. It can be read by the EC.

### SLPBTN\_EN

This bit can be read or written by the Host. It can be read by the EC.

### RTC\_EN

This bit can be read or written by the Host. It can be read by the EC.

## 11.4.5 Power Management 1 Control 1 (PM1\_CNTRL 1)

**Table 11.7 Power Management 1 Control Register 1 (PM1\_CNTRL 1)**

| HOST OFFSET | 04h      |    |    |    | 8-bit |    |    | HOST SIZE           |  |
|-------------|----------|----|----|----|-------|----|----|---------------------|--|
| EC OFFSET   | 104h     |    |    |    |       |    |    | EC SIZE             |  |
| POWER       | VTR      |    |    |    | 00h   |    |    | nSYS_RST<br>DEFAULT |  |
| BUS         | LPC SPB  |    |    |    |       |    |    |                     |  |
| BYTE0 BIT   | D7       | D6 | D5 | D4 | D3    | D2 | D1 | D0                  |  |
| HOST TYPE   | R        | R  | R  | R  | R     | R  | R  | R                   |  |
| EC TYPE     | R        | R  | R  | R  | R     | R  | R  | R                   |  |
| BIT NAME    | Reserved |    |    |    |       |    |    |                     |  |

### RESERVED

Reserved bits return '0' when read.

## 11.4.6 Power Management 1 Control 2 (PM1\_CNTRL 2)

**Table 11.8 Power Management 1 Control Register 2 (PM1\_CNTRL 2)**

| HOST OFFSET | 5h       |    |        | 8-bit    |    |    | HOST SIZE        |          |
|-------------|----------|----|--------|----------|----|----|------------------|----------|
| EC OFFSET   | 105h     |    |        |          |    |    | EC SIZE          |          |
| POWER       | VTR      |    |        | 00h      |    |    | nSYS_RST DEFAULT |          |
| BUS         | LPC SPB  |    |        |          |    |    |                  |          |
| BYTE0 BIT   | D7       | D6 | D5     | D4       | D3 | D2 | D1               | D0       |
| HOST TYPE   | R        | R  | W      | R/W      |    |    | R/W              | R/W      |
| EC TYPE     | R        | R  | R/WC   | R        |    |    | R                | R        |
| BIT NAME    | Reserved |    | SLP_EN | SLP_TYPx |    |    | PWRBTNOR_EN      | Reserved |

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**Note 11.6** An interrupt ([PM1\\_CTL2](#)) is generated to the EC when the Host writes to this register.

**PWRBTNOR\_EN**

This bit can be set or cleared by the Host, read by the EC.

**SLP\_TYPx**

These bits can be set or cleared by the Host, read by the EC.

**SLP\_EN**

Refer to [Table 11.9, "SLP\\_ Definition"](#)

**Table 11.9 SLP\_ Definition**

| HOST / EC | R/W   | DESCRIPTION                                               |
|-----------|-------|-----------------------------------------------------------|
| Host      | Read  | Always reads 0                                            |
|           | Write | Writing a 0 has no effect,<br>Writing a 1 sets this bit   |
| EC        | Read  | Reads the value of the bit                                |
|           | Write | Writing a 0 has no effect,<br>Writing a 1 clears this bit |

**11.4.7 Power Management 2 Control 1 (PM2\_CNTRL 1)****Table 11.10 Power Management 2 Control Register 1 (PM2\_CNTRL 1)**

| HOST OFFSET | 06h      |    |    |    | 8-bit |    |    | HOST SIZE           |  |
|-------------|----------|----|----|----|-------|----|----|---------------------|--|
| EC OFFSET   | 106h     |    |    |    |       |    |    | EC SIZE             |  |
| POWER       | VTR      |    |    |    | 00h   |    |    | nSYS_RST<br>DEFAULT |  |
| BUS         | LPC SPB  |    |    |    |       |    |    |                     |  |
| BYTE0 BIT   | D7       | D6 | D5 | D4 | D3    | D2 | D1 | D0                  |  |
| HOST TYPE   | R        | R  | R  | R  | R     | R  | R  | R                   |  |
| EC TYPE     | R        | R  | R  | R  | R     | R  | R  | R                   |  |
| BIT NAME    | Reserved |    |    |    |       |    |    |                     |  |

**RESERVED**

Reserved bits return '0' when read.

## 11.4.8 Power Management 2 Control 2 (PM2\_CNTRL 2)

**Table 11.11 Power Management 2 Control Register 2 (PM2\_CNTRL 2)**

|             |          |    |    |    |       |    |    |                     |  |
|-------------|----------|----|----|----|-------|----|----|---------------------|--|
| HOST OFFSET | 07h      |    |    |    | 8-bit |    |    | HOST SIZE           |  |
| EC OFFSET   | 107h     |    |    |    |       |    |    | EC SIZE             |  |
| POWER       | VTR      |    |    |    | 00h   |    |    | nSYS_RST<br>DEFAULT |  |
| BUS         | LPC SPB  |    |    |    |       |    |    |                     |  |
| BYTE0 BIT   | D7       | D6 | D5 | D4 | D3    | D2 | D1 | D0                  |  |
| HOST TYPE   | R        | R  | R  | R  | R     | R  | R  | R                   |  |
| EC TYPE     | R        | R  | R  | R  | R     | R  | R  | R                   |  |
| BIT NAME    | Reserved |    |    |    |       |    |    |                     |  |

### RESERVED

Reserved bits return '0' when read.

## 11.5 EC\_SCI# Pin Interface

The EC\_SCI# pin logic hardware is shown below in [Figure 11.1](#).

Any or all of the [PWRBTN](#), [SLPBTN\\_STS](#), and [RTC](#) bits in the [Power Management 1 Status Register 2 \(PM1\\_STS 2\)](#) can assert the EC\_SCI# pin if enabled by the [PWRBTN](#), [SLPBTN](#), and [RTC](#) bits in the PM1\_EN 2 register.

The [EC\\_SCI](#) bit can assert the EC\_SCI# pin at any time, without being enabled. The [EC\\_SCI](#) bit is located in the [EC\\_PM\\_STS Register](#).

The [EC\\_SCI](#) bit is in the MEC5035 and is read/write by the EC. If the [EC\\_SCI](#) bit is "1", an interrupt is generated on the EC\_SCI# pin.

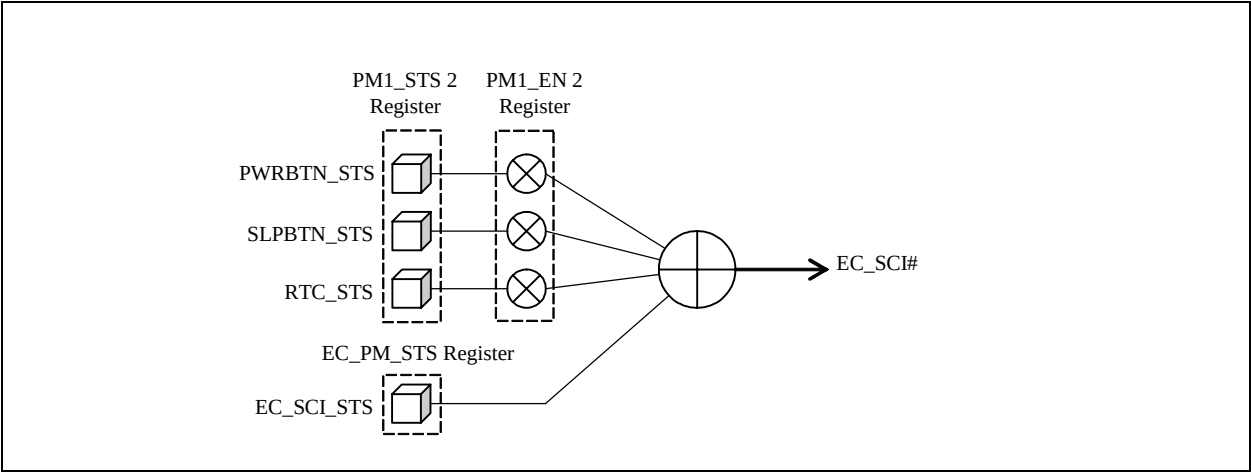


Figure 11.1 Hardware EC\_SCI# Interface

11.5.1 EC\_PM\_STS Register

Table 11.12 EC\_PM\_STS Register

| HOST OFFSET |         |     |     |     |     |     | HOST SIZE |                     |
|-------------|---------|-----|-----|-----|-----|-----|-----------|---------------------|
| EC OFFSET   | 110h    |     |     |     |     |     | 8-bit     | EC SIZE             |
| POWER       | VTR     |     |     |     |     |     | 00h       | nSYS_RST<br>DEFAULT |
| BUS         | LPC SPB |     |     |     |     |     |           |                     |
| BYTE0 BIT   | D7      | D6  | D5  | D4  | D3  | D2  | D1        | D0                  |
| HOST TYPE   | -       | -   | -   | -   | -   | -   | -         | -                   |
| EC TYPE     | R/W     | R/W | R/W | R/W | R/W | R/W | R/W       | R/W                 |
| BIT NAME    | UD[6:0] |     |     |     |     |     |           | EC_SCI_STS          |

EC\_SCI\_STS

If the EC\_SCI\_ bit is “1”, an interrupt is generated on the EC\_SCI# pin.

UD[6:0]

User-defined bits. This bits do not generate an interrupt.





## 11.6 ACPI PM1 Block Interface Revision History

This revision history shows the changes made to this chapter.

**Table 11.13** ACPI PM1 Block Interface Chapter Revision History

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History," on page 539.</a> |              |      |                      |            |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------|----------------------|------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE | SECTION/FIGURE/ENTRY | CORRECTION |
| 1.                                                                                                                                                                                                                                          |              |      |                      |            |
| 2.                                                                                                                                                                                                                                          |              |      |                      |            |
| 3.                                                                                                                                                                                                                                          |              |      |                      |            |
| 4.                                                                                                                                                                                                                                          |              |      |                      |            |



## Chapter 12 Two Pin Serial Port (UART)

### 12.1 General Description

The MEC5035 incorporates one full function UART. The UART is compatible with the 16450, the 16450 ACE registers and the 16C550A. The UART performs serial-to-parallel conversion on received characters and parallel-to-serial conversion on transmit characters. The data rates are independently programmable from 115.2K baud down to 50 baud. The character options are programmable for 1 start; 1, 1.5 or 2 stop bits; even, odd, sticky or no parity; and prioritized interrupts. The UART contains a programmable baud rate generator that is capable of dividing the input clock or crystal by a number from 1 to 65535. The UART is also capable of supporting the MIDI data rate. Refer to the Configuration Registers for information on disabling, powerdown and changing the base address of the UART. The interrupt from a UART is enabled by programming OUT2 of the UART to a logic "1". OUT2 being a logic "0" disables that UART's interrupt. The UART is accessible by both the Host and the EC.

#### 12.1.1 Features

- Programmable word length, stop bits and parity
- Programmable baud rate generator
- Interrupt generator
- Loop-back mode
- Interface registers
- 16-byte Transmit FIFO
- 16-byte Receive FIFO
- Multiple clock sourcesX
- VTR & VCC operation
- Pin Polarity control
- Low power sleep mode

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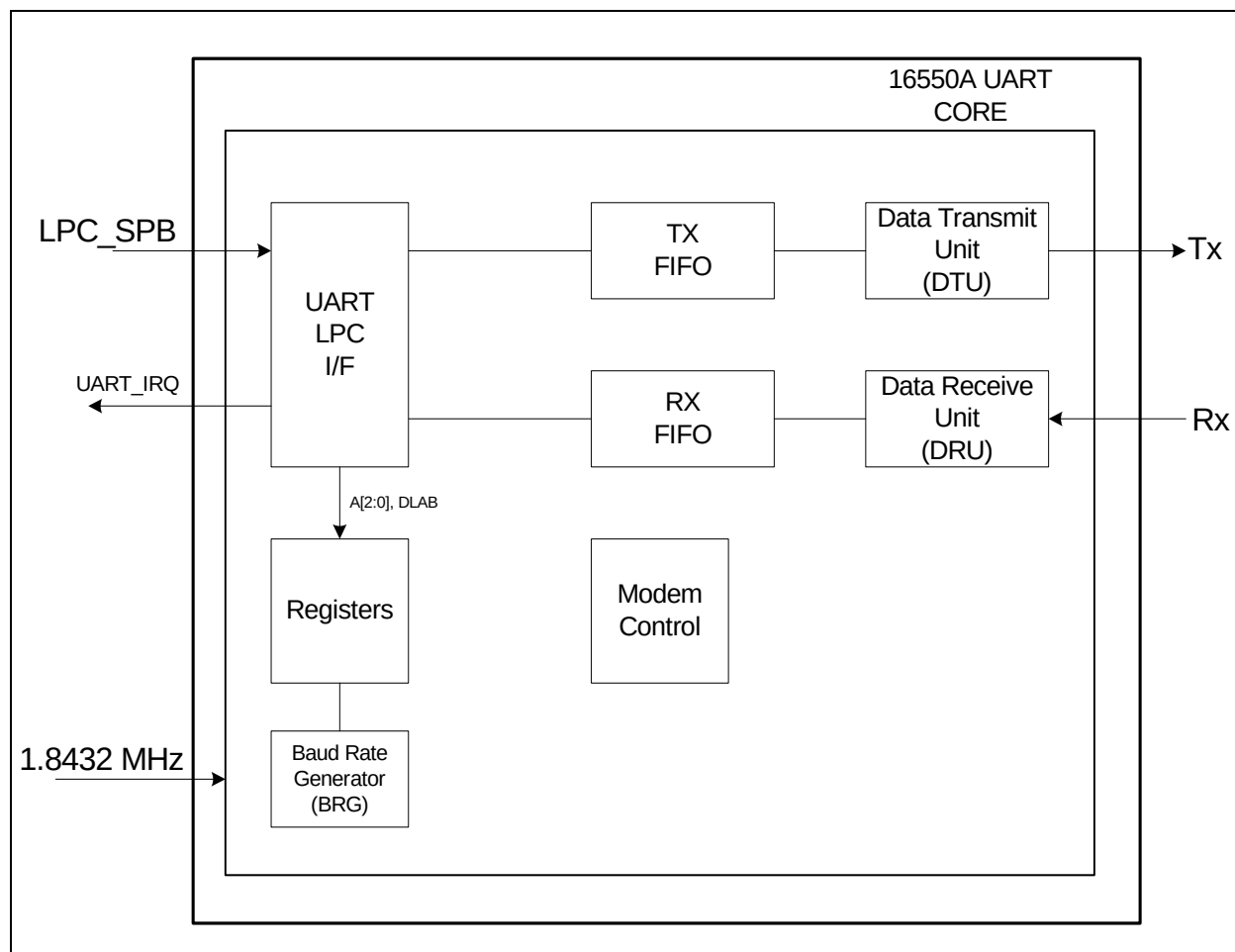
**12.1.2 Block Diagram**

Figure 12.1 Serial Port (UART) Block Diagram

**12.1.3 Block Diagram Signal List**

Table 12.1 Serial Port (UART) Register Interface Port List

| SIGNAL NAME | DIRECTION | DESCRIPTION                          |
|-------------|-----------|--------------------------------------|
| UART_INT    | Output    | Host Interrupt routed to SERIRQ      |
| EC IF       | I/O Bus   | Bus used for register access         |
| CPU_CLOCK   | Input     | Block operating clock                |
| UART_RX     | Input     | UART Receive data pin                |
| UART_TX     | Output    | UART Transmit data pin               |
| UART_CLK    | Input     | UART Alternate clock pin (1.8462MHz) |
| nSYS_RST    | input     | VTR POR reset                        |
| nSIO_RESET  | input     | VCC POR reset                        |

## 12.2 Power, Clocks and Reset

### 12.2.1 Power Domain

This block is powered by the VTR Power Supply.

See [Section 4.5, "Power Configuration," on page 96](#) for details on power domains.

### 12.2.2 Clocks

.Registers in this block are clocked by the [LPC Bus Clock](#). Baud rates are derived from [MCLK](#), either directly or after dividing the master clock down to 1.8432MHz.

See [Section 4.4, "Clock Generator," on page 77](#) for details on clocks.

### 12.2.3 Reset

[Table 12.2](#) details the effect of [nSYS\\_RST](#) or [nSIO\\_RESET](#) on each of the runtime registers of the Serial Port.

**Table 12.2 Reset Function Table**

| REGISTER/SIGNAL               | RESET CONTROL             | RESET STATE                      |
|-------------------------------|---------------------------|----------------------------------|
| Interrupt Enable Register     | RESET                     | All bits low                     |
| Interrupt Identification Reg. |                           | Bit 0 is high; Bits 1 - 7 low    |
| FIFO Control                  |                           | All bits low                     |
| Line Control Reg.             |                           |                                  |
| MODEM Control Reg.            |                           |                                  |
| Line Status Reg.              |                           | All bits low except 5, 6 high    |
| MODEM Status Reg.             |                           | Bits 0 - 3 low; Bits 4 - 7 input |
| TXD1, TXD2                    |                           | High                             |
| INTRPT (RCVR errs)            | RESET/Read LSR            | Low                              |
| INTRPT (RCVR Data Ready)      | RESET/Read RBR            |                                  |
| INTRPT (THRE)                 | RESET/ReadIIR/Write THR   |                                  |
| OUT2B                         | RESET                     | High                             |
| RTSB                          |                           |                                  |
| DTRB                          |                           |                                  |
| OUT1B                         |                           |                                  |
| RCVR FIFO                     | RESET/<br>FCR1*FCR0/_FCR0 | All Bits Low                     |
| XMIT FIFO                     | RESET/<br>FCR1*FCR0/_FCR0 |                                  |

The Runtime register can be configured to be reset on either [nSYS\\_RST](#) or [nSIO\\_RESET](#). The [POWER](#) bit in the [Configuration Select Register](#) controls which reset effects the runtime registers. The

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Refer to [Table 12.2](#) for effected registers and [Chapter 4, Power, Clocks and Resets](#) for definitions of [nSYS\\_RST](#) on page 101 or [nSIO\\_RESET](#) on page 76

See [Section 4.6, "Reset Interface,"](#) on page 99 for details on reset.

## 12.3 Interrupts

The [Two Pin Serial Port \(UART\)](#) can generate an interrupt event. The interrupt source is routed onto the [UART\\_RX](#) bit in the [IRQ17 Source Register](#), and is a level, active high signal.

### 12.3.1 Two Pin Serial Port (UART) (LDN 6h) SIRQ Routing

The [Two Pin Serial Port \(UART\)](#) can generate a SIRQ event to the Host. See the [Interrupt Enable Register \(IER\)](#) on page 231 and the [Interrupt Identification Register \(IIR\)](#) on page 233. This interrupt is routed to the SIRQ block (see [SERIRQ Configuration Registers](#) on page 150)

## 12.4 Registers

The [Two Pin Serial Port \(UART\)](#) registers are located on the Host SPB.

Each instance of the [Two Pin Serial Port \(UART\)](#) has its own Logical Device Number, and Base Address as indicated in [Table 12.3](#).

**Table 12.3** [Two Pin Serial Port \(UART\)](#) Base Address Table

| Two Pin Serial Port (UART) INSTANCE | LDN FROM<br>( <a href="#">Table 7.2</a> on page 167) | AHB BASE ADDRESS         |
|-------------------------------------|------------------------------------------------------|--------------------------|
| UART                                | 6h                                                   | <a href="#">FF_1800h</a> |

**Note 12.1** The Host LPC I/O addresses for each instance is selected via a Base Address Register (see [Section 6.6.2, "Base Address Registers,"](#) on page 144). LPC access to configuration registers is through the Host Access Configuration Port (see [Section 6.5.1, "Host Access Port,"](#) on page 142.)

[Table 12.4](#) is a register summary for one instance of the [Two Pin Serial Port \(UART\)](#). The LPC I/O address for each Run-Time Register is described below as an offset from its Base Address Register. Each EC address is indicated as an SPB Offset from its AHB base address. Each Configuration register access through the [Host Access Port](#) is via its LDN indicated in [Table 12.3](#) on page 227 and its [Host Access Port](#) index which is described as "Host Config Index" in the tables below.

The following table summarizes the registers allocated for the Controller. The offset field in the following table is the offset from the Embedded Controller's (EC) Base Address.

**Table 12.4 Two Pin Serial Port (UART) Register Summary**

| REGISTER NAME                                 | HOST I/O ACCESS    |             |           | DLAB<br>(Note 12.2) | EC INTERFACE |           |         | NOTES     |
|-----------------------------------------------|--------------------|-------------|-----------|---------------------|--------------|-----------|---------|-----------|
|                                               | HOST I/O INDEX     | SPB OFF-SET | HOST TYPE |                     | SPB OFF-SET  | BYTE LANE | EC TYPE |           |
| Receive Buffer Register (RB),                 | 00h                | 00h         | R         | 0                   | 200h         | 0         | R       | Note 12.3 |
| Transmit Buffer Register (TB)                 | 00h                | 00h         | W         | 0                   | 200h         | 0         | W       | Note 12.3 |
| Programmable Baud Rate Generator (and Divisor | 00h                | 00h         | R/W       | 1                   | 200h         | 0         | R/W     | Note 12.3 |
| Programmable Baud Rate Generator (and Divisor | 01h                | 01h         | R/W       | 1                   | 201h         | 1         | R/W     | Note 12.3 |
| Interrupt Enable Register (IER)               | 01h                | 01h         | R/W       | 0                   | 201h         | 1         | R/W     | Note 12.3 |
| FIFO Control Register (FCR),                  | 02h                | 02h         | W         | X                   | 202h         | 2         | W       | Note 12.3 |
| Interrupt Identification Register (IIR)       | 02h                | 02h         | R         | X                   | 202h         | 2         | R       | Note 12.3 |
| Line Control Register (LCR)                   | 03h                | 03h         | R/W       | X                   | 203h         | 3         | R/W     | Note 12.3 |
| Modem Control Register (MCR)                  | 04h                | 04h         | R/W       | X                   | 204h         | 0         | R/W     | Note 12.3 |
| Line Status Register (LSR)                    | 05h                | 05h         | R         | X                   | 205h         | 1         | R       | Note 12.3 |
| Modem Status Register (MSR)                   | 06h                | 06h         | R         | X                   | 206h         | 2         | R       | Note 12.3 |
| Scratchpad Register (SCR)                     | 07h                | 07h         | R/W       | X                   | 207h         | 3         | R/W     | Note 12.3 |
| REGISTER NAME                                 | HOST ACCESS        |             |           | N/A                 | EC INTERFACE |           |         |           |
|                                               | HOST CONFIG. INDEX | SPB OFF-SET | HOST TYPE |                     | EC OFF SET   | BYTE LANE | EC TYPE |           |
| Activate                                      | 30h                | 330h        | R/W       |                     | 330h         | 0         | R/W     | Note 12.3 |
| Configuration Select Register                 | F0h                | 3F0h        | R/W       |                     | 3F0h         | 0         | R/W     | Note 12.3 |

**Note 12.2** DLAB is Bit 7 of the Line Control Register

**Note 12.3** Access to this register should be limited to 8-bit loads and stores. 16-bit or 32-bit stores will be blocked and 16-bit or 32-bit loads have unexpected results. JTAG Debugger access should indirect using peek\_poke\_arc macros described in [SMSC AN #16.1, MEC5035 JTAG Design and Layout Guide](#).



## 12.5 Register Summary

Table 12.5 Register Summary

| ADDRESS<br>(Note 12.4) | R/W | REGISTER<br>NAME      | BIT 7                           | BIT 6                                | BIT 5                               | BIT 4                    | BIT 3                                | BIT 2                                        | BIT 1                                                        | BIT 0                                            |
|------------------------|-----|-----------------------|---------------------------------|--------------------------------------|-------------------------------------|--------------------------|--------------------------------------|----------------------------------------------|--------------------------------------------------------------|--------------------------------------------------|
| ADDR = 0<br>DLAB = 0   | R   | Receive Buffer r      | Data Bit 7                      | Data Bit 6                           | Data Bit 5                          | Data Bit 4               | Data Bit 3                           | Data Bit 2                                   | Data Bit 1                                                   | Data Bit 0<br><br>(Note 12.5)                    |
| ADDR = 0<br>DLAB = 0   | W   | Transmitter Holding r | Data Bit 7                      | Data Bit 6                           | Data Bit 5                          | Data Bit 4               | Data Bit 3                           | Data Bit 2                                   | Data Bit 1                                                   | Data Bit 0                                       |
| ADDR = 1<br>DLAB = 0   | R/W | Interrupt Enable r    | Reserved                        |                                      |                                     |                          | Enable Modem Status Interrupt (EMSI) | Enable Receiver Line Status Interrupt (ELSI) | Enable Transmitter Holding Register Empty Interrupt (ETHREI) | Enable Received Data Available Interrupt (ERDAI) |
| ADDR = 2               | R   | Interrupt Ident. r    | FIFOs Enabled (Note 12.9)       | FIFOs Enabled (Note 12.9)            | Reserved                            |                          | Interrupt ID Bit (Note 12.9)         | Interrupt ID Bit                             | Interrupt ID Bit                                             | "0" if Interrupt Pending                         |
| ADDR = 2               | W   | FIFO Control r        | RCVR Trigger MSB                | RCVR Trigger LSB                     | Reserved                            |                          | DMA Mode Select (Note 12.10)         | XMIT FIFO Reset                              | RCVR FIFO Reset                                              | FIFO Enable                                      |
| ADDR = 3               | R/W | Line Control r        | Divisor Latch Access Bit (DLAB) | Set Break                            | Stick Parity                        | Even Parity Select (EPS) | Parity Enable (PEN)                  | Number of Stop Bits (STB)                    | Word Length Select Bit 1 (WLS1)                              | Word Length Select Bit 0 (WLS0)                  |
| ADDR = 4               | R/W | MODEM Control r       | Reserved                        |                                      |                                     | Loop                     | OUT2 (Note 12.7)                     | OUT1 (Note 12.7)                             | Request to Send (RTS)                                        | Data Terminal Ready (DTR)                        |
| ADDR = 5               | R/W | Line Status r         | Error in RCVR FIFO (Note 12.9)  | Transmitter Empty (TEMT) (Note 12.6) | Transmitter Holding Register (THRE) | Break Interrupt (BI)     | Framing Error (FE)                   | Parity Error (PE)                            | Over-run Error (OE)                                          | Data Ready (DR)                                  |
| ADDR = 6               | R/W | MODEM Status r        | Data Carrier Detect (DCD)       | Ring Indicator (RI)                  | Data Set Ready (DSR)                | Clear to Send (CTS)      | Delta Data Carrier Detect (DDCD)     | Trailing Edge Ring Indicator (TERI)          | Delta Data Set Ready (DDSR)                                  | Delta Clear to Send (DCTS)                       |
| ADDR = 7               | R/W | Scratch r (Note 12.8) | Bit7                            | Bit6                                 | Bit5                                | Bit4                     | Bit3                                 | Bit2                                         | Bit1                                                         | Bit0                                             |
| ADDR = 0<br>DLAB = 1   | R/W | Divisor Latch (LS)    | Bit7                            | Bit6                                 | Bit5                                | Bit4                     | Bit3                                 | Bit2                                         | Bit1                                                         | Bit0                                             |
| ADDR = 1<br>DLAB = 1   | R/W | Divisor Latch (MS)    | Bit15                           | Bit14                                | Bit13                               | Bit12                    | Bit11                                | Bit10                                        | Bit9                                                         | Bit8                                             |

### UART Register Summary Notes:

**Note 12.4** DLAB is Bit 7 of the Line Control Register (ADDR = 3).

**Note 12.5** Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

**Note 12.6** When operating in the XT mode, this bit will be set any time that the transmitter shift register is empty.



**Note 12.7** This bit no longer has a pin associated with it.

**Note 12.8** When operating in the XT mode, this register is not available.

**Note 12.9** These bits are always zero in the non-FIFO mode.

**Note 12.10** Writing a one to this bit has no effect. DMA modes are not supported in this chip.

## 12.6 Detailed Description of Accessible Runtime Registers

### 12.6.1 Receive Buffer Register (RB)

**Table 12.6 Receive Buffer (RB)**

|             |                          |    |    |    |       |    |    |                                      |  |
|-------------|--------------------------|----|----|----|-------|----|----|--------------------------------------|--|
| HOST OFFSET | 0h (DLAB=0)              |    |    |    | 8-bit |    |    | HOST SIZE                            |  |
| EC OFFSET   | 0h (DLAB=0)              |    |    |    | 8-bit |    |    | EC SIZE                              |  |
| POWER       | VCC or VTR               |    |    |    | 00h   |    |    | nSYS_RST or<br>nSIO_RESET<br>DEFAULT |  |
| BUS         | LPC SPB                  |    |    |    |       |    |    |                                      |  |
| BYTE3 BIT   | D7                       | D6 | D5 | D4 | D3    | D2 | D1 | D0                                   |  |
| HOST TYPE   | R                        | R  | R  | R  | R     | R  | R  | R                                    |  |
| EC TYPE     | R                        | R  | R  | R  | R     | R  | R  | R                                    |  |
| BIT NAME    | Received Data byte [7:0] |    |    |    |       |    |    |                                      |  |

#### RECEIVED DATA BYTE

This register holds the received incoming data byte. Bit 0 is the least significant bit, which is transmitted and received first. Received data is double buffered; this uses an additional shift register to receive the serial data stream and convert it to a parallel 8 bit word which is transferred to the Receive Buffer register. The shift register is not accessible.

## 12.6.2 Transmit Buffer Register (TB)

**Table 12.7 Transmit Buffer (TB)**

|             |                          |    |    |       |    |    |                                          |    |
|-------------|--------------------------|----|----|-------|----|----|------------------------------------------|----|
| HOST OFFSET | 0h (DLAB=0)              |    |    | 8-bit |    |    | HOST SIZE                                |    |
| EC OFFSET   | 0h (DLAB=0)              |    |    | 8-bit |    |    | EC SIZE                                  |    |
| POWER       | VCC or VTR               |    |    | 00h   |    |    | nSYS_RST or VCC<br>Power Good<br>DEFAULT |    |
| BUS         | LPC SPB                  |    |    |       |    |    |                                          |    |
| BYTE3 BIT   | D7                       | D6 | D5 | D4    | D3 | D2 | D1                                       | D0 |
| HOST TYPE   | W                        | W  | W  | W     | W  | /W | W                                        | W  |
| EC TYPE     |                          | W  | W  | W     | W  | W  | W                                        | W  |
| BIT NAME    | Transmit data byte [7:0] |    |    |       |    |    |                                          |    |

### TRANSMIT DATA BYTE

This register contains the data byte to be transmitted. The transmit buffer is double buffered, utilizing an additional shift register (not accessible) to convert the 8 bit data word to a serial format. This shift register is loaded from the Transmit Buffer when the transmission of the previous byte is complete.

## 12.6.3 Interrupt Enable Register (IER)

**Table 12.8 Interrupt Enable (IER)**

|             |             |     |     |     |       |      |                                      |       |
|-------------|-------------|-----|-----|-----|-------|------|--------------------------------------|-------|
| HOST OFFSET | 1h (DLAB=0) |     |     |     | 8-bit |      | HOST SIZE                            |       |
| EC OFFSET   | 1h (DLAB=0) |     |     |     | 8-bit |      | EC SIZE                              |       |
| POWER       | VCC or VTR  |     |     |     | 00h   |      | nSYS_RST or<br>nSIO_RESET<br>DEFAULT |       |
| BUS         | LPC SPB     |     |     |     |       |      |                                      |       |
| BYTE3 BIT   | D7          | D6  | D5  | D4  | D3    | D2   | D1                                   | D0    |
| HOST TYPE   | R/W         | R/W | R/W | R/W | R/W   | R/W  | R/W                                  | R/W   |
| EC TYPE     | R/W         | R/W | R/W | R/W | R/W   | R/W  | R/W                                  | R/W   |
| BIT NAME    | Reserved    |     |     |     | EMSI  | ELSI | ETHREI                               | ERDAI |

The lower four bits of this register control the enables of the five interrupt sources of the Serial Port interrupt. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of this register. Similarly, setting the appropriate bits of this register to a high, selected interrupts can be enabled.

Disabling the interrupt system inhibits the Interrupt Identification Register and disables any Serial Port interrupt out of the MEC5035. All other system functions operate in their normal manner, including the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are described below.

**ERDAI**

This bit enables the Received Data Available Interrupt (and timeout interrupts in the FIFO mode) when set to logic "1".

**ETHREI**

This bit enables the Transmitter Holding Register Empty Interrupt when set to logic "1".

**ELSI**

This bit enables the Received Line Status Interrupt when set to logic "1". The error sources causing the interrupt are Overrun, Parity, Framing and Break. The Line Status Register must be read to determine the source.

**EMSI**

This bit enables the MODEM Status Interrupt when set to logic "1". This is caused when one of the Modem Status Register bits changes state.

## 12.6.4 FIFO Control Register (FCR)

**Table 12.9 FIFO Control (FCR)**

| HOST OFFSET | 02h                     |    |          | 8-bit |    |                 | HOST SIZE                                |      |
|-------------|-------------------------|----|----------|-------|----|-----------------|------------------------------------------|------|
| EC OFFSET   | 02h                     |    |          | 8-bit |    |                 | EC SIZE                                  |      |
| POWER       | VCC or VTR              |    |          | 00h   |    |                 | nSYS_RST or VCC<br>Power Good<br>DEFAULT |      |
| BUS         | LPC SPB                 |    |          |       |    |                 |                                          |      |
| BYTE3 BIT   | D7                      | D6 | D5       | D4    | D3 | D2              | D1                                       | D0   |
| HOST TYPE   | W                       | W  | W        | W     | W  | W               | W                                        | W    |
| EC TYPE     | W                       | W  | W        | W     | W  | W               | W                                        | W    |
| BIT NAME    | RECV FIFO Trigger Level |    | Reserved |       |    | Clear XMIT FIFO | Clear RECV FIFO                          | EXRF |

This is a write only register at the same location as the IIR.

**Note 12.11** DMA is not supported.

**EXRF**

Enable XMIT and RECV FIFO. Setting this bit to a logic "1" enables both the XMIT and RCVR FIFOs. Clearing this bit to a logic "0" disables both the XMIT and RCVR FIFOs and clears all bytes from both FIFOs. When changing from FIFO Mode to non-FIFO (16450) mode, data is automatically cleared from

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the FIFOs. This bit must be a 1 when other bits in this register are written to or they will not be properly programmed.

**CLEAR RECV FIFO**

Setting this bit to a logic "1" clears all bytes in the RCVR FIFO and resets its counter logic to "0". The shift register is not cleared. This bit is self-clearing.

**CLEAR XMIT FIFO**

Setting this bit to a logic "1" clears all bytes in the XMIT FIFO and resets its counter logic to "0". The shift register is not cleared. This bit is self-clearing.

**RECV FIFO TRIGGER LEVEL**

These bits are used to set the trigger level for the RCVR FIFO interrupt.

**Table 12.10 RECV FIFO Trigger Level**

| BIT 7 | BIT 6 | RECV FIFO<br>TRIGGER LEVEL (BYTES) |
|-------|-------|------------------------------------|
| 0     | 0     | 1                                  |
|       | 1     | 4                                  |
| 1     | 0     | 8                                  |
|       | 1     | 14                                 |

**12.6.5 Interrupt Identification Register (IIR)****Table 12.11 Interrupt Identification (IIR)**

|             |            |    |          |    |       |    |    |                                      |  |
|-------------|------------|----|----------|----|-------|----|----|--------------------------------------|--|
| HOST OFFSET | 02h        |    |          |    | 8-bit |    |    | HOST SIZE                            |  |
| EC OFFSET   | 02h        |    |          |    | 8-bit |    |    | EC SIZE                              |  |
| POWER       | VCC or VTR |    |          |    | 01h   |    |    | nSYS_RST or<br>nSIO_RESET<br>DEFAULT |  |
| BUS         | LPC SPB    |    |          |    |       |    |    |                                      |  |
| BYTE3 BIT   | D7         | D6 | D5       | D4 | D3    | D2 | D1 | D0                                   |  |
| HOST TYPE   | R          | R  | R        | R  | R     | R  | R  | R                                    |  |
| EC TYPE     | R          | R  | R        | R  | R     | R  | R  | R                                    |  |
| BIT NAME    | FIFO_En    |    | Reserved |    | IntID |    |    | IPEND                                |  |

By accessing this register, the host CPU can determine the highest priority interrupt and its source. Four levels of priority interrupt exist. They are in descending order of priority:

1. Receiver Line Status (highest priority)
2. Received Data Ready

3. Transmitter Holding Register Empty
4. MODEM Status (lowest priority)

Information indicating that a prioritized interrupt is pending and the source of that interrupt is stored in the Interrupt Identification Register (refer to [Table 12.12](#)). When the CPU accesses the IIR, the Serial Port freezes all interrupts and indicates the highest priority pending interrupt to the CPU. During this CPU access, even if the Serial Port records new interrupts, the current indication does not change until access is completed. The contents of the IIR are described below.

#### **IPEND**

This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic "0", an interrupt is pending and the contents of the IIR may be used as a pointer to the appropriate internal service routine. When bit 0 is a logic "1", no interrupt is pending.

#### **INTID**

These three bits of the IIR are used to identify the highest priority interrupt pending as indicated by [Table 12.12](#). In non-FIFO mode, Bit[3] is a logic "0". In FIFO mode Bit[3] is set along with Bit[2] when a timeout interrupt is pending.



Table 12.12 Interrupt Control Table

| FIFO MODE ONLY | INTERRUPT IDENTIFICATION REGISTER |                              |       | INTERRUPT SET AND RESET FUNCTIONS |                                                                                                                                                 |                                                               |                                                                 |                                                                                               |
|----------------|-----------------------------------|------------------------------|-------|-----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------|-----------------------------------------------------------------|-----------------------------------------------------------------------------------------------|
| BIT 3          | BIT 2                             | BIT 1                        | BIT 0 | PRIORITY LEVEL                    | INTERRUPT TYPE                                                                                                                                  | INTERRUPT SOURCE                                              | INTERRUPT RESET CONTROL                                         |                                                                                               |
| 0              | 0                                 | 0                            | 1     | -                                 | None                                                                                                                                            | None                                                          | -                                                               |                                                                                               |
|                | 1                                 | 1                            | 0     | Highest                           | Receiver Line Status                                                                                                                            | Overrun Error, Parity Error, Framing Error or Break Interrupt | Reading the Line Status Register                                |                                                                                               |
|                |                                   | 0                            |       | Second                            | Received Data Available                                                                                                                         | Receiver Data Available                                       | Read Receiver Buffer or the FIFO drops below the trigger level. |                                                                                               |
| 1              | 0                                 | Character Timeout Indication |       |                                   | No Characters Have Been Removed From or Input to the RCVR FIFO during the last 4 Char times and there is at least 1 char in it during this time | Reading the Receiver Buffer Register                          |                                                                 |                                                                                               |
| 0              |                                   | 0                            |       | 1                                 | Third                                                                                                                                           | Transmitter Holding Register Empty                            | Transmitter Holding Register Empty                              | Reading the IIR Register (if Source of Interrupt) or Writing the Transmitter Holding Register |
|                |                                   |                              |       | 0                                 |                                                                                                                                                 |                                                               |                                                                 |                                                                                               |

**FIFO\_EN**

These two bits are set when the FIFO CONTROL Register bit 0 equals 1.

## 12.6.6 Line Control Register (LCR)

**Table 12.13 Line Control (LCR)**

|             |            |               |              |               |               |           |                                      |     |
|-------------|------------|---------------|--------------|---------------|---------------|-----------|--------------------------------------|-----|
| HOST OFFSET | 03h        |               |              | 8-bit         |               |           | HOST SIZE                            |     |
| EC OFFSET   | 03h        |               |              | 8-bit         |               |           | EC SIZE                              |     |
| POWER       | VCC or VTR |               |              | 00h           |               |           | nSYS_RST or<br>nSIO_RESET<br>DEFAULT |     |
| BUS         | LPC SPB    |               |              |               |               |           |                                      |     |
| BYTE3 BIT   | D7         | D6            | D5           | D4            | D3            | D2        | D1                                   | D0  |
| HOST TYPE   | R/W        | R/W           | R/W          | R/W           | R/W           | R/W       | R/W                                  | R/W |
| EC TYPE     | R/W        | R/W           | R/W          | R/W           | R/W           | R/W       | R/W                                  | R/W |
| BIT NAME    | DLAB       | Break Control | Stick Parity | Parity Select | Enable Parity | Stop Bits | Word Length                          |     |

This register contains the format information of the serial line. The bit definitions are:

### WORD LENGTH

These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

### STOP BITS

This bit specifies the number of stop bits in each transmitted or received serial character. [Table 12.14](#) summarizes the information.

**Table 12.14 Stop Bits**

| <b>BIT 2</b> | <b>WORD LENGTH</b> | <b>NUMBER OF STOP BITS</b> |
|--------------|--------------------|----------------------------|
| 0            | --                 | 1                          |
| 1            | 5 bits             | 1.5                        |
|              | 6 bits             | 2                          |
|              | 7 bits             |                            |
|              | 8 bits             |                            |

**Note 12.12** The receiver will ignore all stop bits beyond the first, regardless of the number used in transmitting.

**Table 12.15 Serial Character**

| <b>BIT 1</b> | <b>BIT 0</b> | <b>WORD LENGTH</b> |
|--------------|--------------|--------------------|
| 0            | 0            | 5 Bits             |
| 0            | 1            | 6 Bits             |
| 1            | 0            | 7 Bits             |
| 1            | 1            | 8 Bits             |

The Start, Stop and Parity bits are not included in the word length.

**ENABLE PARITY**

Parity Enable bit. When bit 3 is a logic "1", a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and the first stop bit of the serial data. (The parity bit is used to generate an even or odd number of 1s when the data word bits and the parity bit are summed).

**PARITY SELECT**

Even Parity Select bit. When bit 3 is a logic "1" and bit 4 is a logic "0", an odd number of logic "1"s is transmitted or checked in the data word bits and the parity bit. When bit 3 is a logic "1" and bit 4 is a logic "1" an even number of bits is transmitted and checked.

**STICK PARITY**

Stick Parity bit. When parity is enabled it is used in conjunction with bit 4 to select Mark or Space Parity. When LCR bits 3, 4 and 5 are 1 the Parity bit is transmitted and checked as a 0 (Space Parity). If bits 3 and 5 are 1 and bit 4 is a 0, then the Parity bit is transmitted and checked as 1 (Mark Parity). If bit 5 is 0 Stick Parity is disabled.

Bit 3 is a logic "1" and bit 5 is a logic "1", the parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

**BREAK CONTROL**

Set Break Control bit. When bit 6 is a logic "1", the transmit data output (TXD) is forced to the Spacing or logic "0" state and remains there (until reset by a low level bit 6) regardless of other transmitter activity. This feature enables the Serial Port to alert a terminal in a communications system.

**DLAB**

Divisor Latch Access Bit (DLAB). It must be set high (logic "1") to access the Divisor Latches of the Baud Rate Generator during read or write operations. It must be set low (logic "0") to access the Receiver Buffer Register, the Transmitter Holding Register, or the Interrupt Enable Register.



## 12.6.7 Modem Control Register (MCR)

**Table 12.16 Modem Control (MCR)**

|             |            |     |     |               |      |      |                                      |     |
|-------------|------------|-----|-----|---------------|------|------|--------------------------------------|-----|
| HOST OFFSET | 04h        |     |     | 8-bit         |      |      | HOST SIZE                            |     |
| EC OFFSET   | 04h        |     |     | 8-bit         |      |      | EC SIZE                              |     |
| POWER       | VCC or VTR |     |     | 00h           |      |      | nSYS_RST or<br>nSIO_RESET<br>DEFAULT |     |
| BUS         | LPC SPB    |     |     |               |      |      |                                      |     |
| BYTE3 BIT   | D7         | D6  | D5  | D4            | D3   | D2   | D1                                   | D0  |
| HOST TYPE   | R/W        | R/W | R/W | R/W           | R/W  | R/W  | R/W                                  | R/W |
| EC TYPE     | R/W        | R/W | R/W | R/W           | R/W  | R/W  | R/W                                  | R/W |
| BIT NAME    | Reserved   |     |     | LOOP-<br>BACK | OUT2 | OUT1 | RTS                                  | DTR |

This 8-bit register controls the interface with the MODEM or data set (or device emulating a MODEM). The contents of the MODEM control register are described below.

### DTR

This bit controls the Data Terminal Ready (nDTR) output. When bit 0 is set to a logic "1", the nDTR output is forced to a logic "0". When bit 0 is a logic "0", the nDTR output is forced to a logic "1".

### RTS

This bit controls the Request To Send (nRTS) output. Bit 1 affects the nRTS output in a manner identical to that described above for bit 0.

### OUT1

This bit controls the Output 1 (OUT1) bit. This bit does not have an output pin and can only be read or written by the CPU.

### OUT2

Output 2 (OUT2). This bit is used to enable an UART interrupt. When OUT2 is a logic "0", the serial port interrupt output is forced to a high impedance state - disabled. When OUT2 is a logic "1", the serial port interrupt outputs are enabled.

### LOOPBACK

This bit provides the loopback feature for diagnostic testing of the Serial Port. When bit 4 is set to logic "1", the following occur:

1. The TXD is set to the Marking State (logic "1").
2. The receiver Serial Input (RXD) is disconnected.
3. The output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input.
4. All MODEM Control inputs (nCTS, nDSR, nRI and nDCD) are disconnected.
5. The four MODEM Control outputs (nDTR, nRTS, OUT1 and OUT2) are internally connected to the four MODEM Control inputs (nDSR, nCTS, RI, DCD).



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6. The Modem Control output pins are forced inactive high.
7. Data that is transmitted is immediately received.

This feature allows the processor to verify the transmit and receive data paths of the Serial Port. In the diagnostic mode, the receiver and the transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

## 12.6.8 Line Status Register (LSR)

Table 12.17 Line Status (LSR)

|             |            |                        |                        |                    |                |                 |                  |                                      |  |
|-------------|------------|------------------------|------------------------|--------------------|----------------|-----------------|------------------|--------------------------------------|--|
| HOST OFFSET | 05h        |                        |                        |                    | 8-bit          |                 |                  | HOST SIZE                            |  |
| EC OFFSET   | 05h        |                        |                        |                    | 8-bit          |                 |                  | EC SIZE                              |  |
| POWER       | VCC or VTR |                        |                        |                    | 60h            |                 |                  | nSYS_RST or<br>nSIO_RESET<br>DEFAULT |  |
| BUS         | LPC SPB    |                        |                        |                    |                |                 |                  |                                      |  |
| BYTE3 BIT   | D7         | D6                     | D5                     | D4                 | D3             | D2              | D1               | D0                                   |  |
| HOST TYPE   | R          | R                      | R                      | R                  | R              | R               | R                | R                                    |  |
| EC TYPE     | R          | R                      | R                      | R                  | R              | R               | R                | R                                    |  |
| BIT NAME    | FIFO Error | Trans-<br>mit<br>Error | Trans-<br>mit<br>Empty | Break<br>Interrupt | Frame<br>Error | Parity<br>Error | Overrun<br>Error | Data<br>Ready                        |  |

### DATA READY

Data Ready (DR). It is set to a logic "1" whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. Bit 0 is reset to a logic "0" by reading all of the data in the Receive Buffer Register or the FIFO.

### OVERRUN ERROR

Overrun Error (OE). Bit 1 indicates that data in the Receiver Buffer Register was not read before the next character was transferred into the register, thereby destroying the previous character. In FIFO mode, an overrun error will occur only when the FIFO is full and the next character has been completely received in the shift register, the character in the shift register is overwritten but not transferred to the FIFO. The OE indicator is set to a logic "1" immediately upon detection of an overrun condition, and reset whenever the Line Status Register is read.

### PARITY ERROR

Parity Error (PE). Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. The PE is set to a logic "1" upon detection of a parity error and is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO.

**FRAME ERROR**

Framing Error (FE). Bit 3 indicates that the received character did not have a valid stop bit. Bit 3 is set to a logic "1" whenever the stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. The Serial Port will try to resynchronize after a framing error. To do this, it assumes that the framing error was due to the next start bit, so it samples this 'start' bit twice and then takes in the 'data'.

**BREAK INTERRUPT**

Break Interrupt (BI). Bit 4 is set to a logic "1" whenever the received data input is held in the Spacing state (logic "0") for longer than a full word transmission time (that is, the total time of the start bit + data bits + parity bits + stop bits). The BI is reset after the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. Restarting after a break is received, requires the serial data (RXD) to be logic "1" for at least 1/2 bit time.

Bits 1 through 4 are the error conditions that produce a Receiver Line Status Interrupt **BIT 3**

**Note 12.13** whenever any of the corresponding conditions are detected and the interrupt is enabled

**TRANSMIT EMPTY**

Transmitter Holding Register Empty (THRE). Bit 5 indicates that the Serial Port is ready to accept a new character for transmission. In addition, this bit causes the Serial Port to issue an interrupt when the Transmitter Holding Register interrupt enable is set high. The THRE bit is set to a logic "1" when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic "0" whenever the CPU loads the Transmitter Holding Register. In the FIFO mode this bit is set when the XMIT FIFO is empty, it is cleared when at least 1 byte is written to the XMIT FIFO. Bit 5 is a read only bit.

**TRANSMIT ERROR**

Transmitter Empty (TEMT). Bit 6 is set to a logic "1" whenever the Transmitter Holding Register (THR) and Transmitter Shift Register (TSR) are both empty. It is reset to logic "0" whenever either the THR or TSR contains a data character. Bit 6 is a read only bit. In the FIFO mode this bit is set whenever the THR and TSR are both empty,

**FIFO ERROR**

This bit is permanently set to logic "0" in the 450 mode. In the FIFO mode, this bit is set to a logic "1" when there is at least one parity error, framing error or break indication in the FIFO. This bit is cleared when the LSR is read if there are no subsequent errors in the FIFO.

## 12.6.9 Modem Status Register (MSR)

Table 12.18 Modem Status (MSR)

|              |            |     |     |           |     |    |                                      |     |
|--------------|------------|-----|-----|-----------|-----|----|--------------------------------------|-----|
| HOST ADDRESS | 06h        |     |     | 8-bit     |     |    | HOST SIZE                            |     |
| EC OFFSET    | 06h        |     |     | 8-bit     |     |    | EC SIZE                              |     |
| POWER        | VCC or VTR |     |     | xxxx0000b |     |    | nSYS_RST or<br>nSIO_RESET<br>DEFAULT |     |
| BUS          | LPC SPB    |     |     |           |     |    |                                      |     |
| BYTE3 BIT    | D7         | D6  | D5  | D4        | D3  | D2 | D1                                   | D0  |
| HOST TYPE    | R          | R   | R   | R         | R   | R  | R                                    | R   |
| EC TYPE      | R          | R   | R   | R         | R   | R  | R                                    | R   |
| BIT NAME     | DCD#       | RI# | DSR | CTS       | DCD | RI | DSR                                  | CTS |

This 8 bit register provides the current state of the control lines from the MODEM (or peripheral device). In addition to this current state information, four bits of the MODEM Status Register (MSR) provide change information.

These bits are set to logic "1" whenever a control input from the MODEM changes state. They are reset to logic "0" whenever the MODEM Status Register is read.

### CTS

Delta Clear To Send (DCTS). Bit 0 indicates that the nCTS input to the chip has changed state since the last time the MSR was read.

### DSR

Delta Data Set Ready (DDSR). Bit 1 indicates that the nDSR input has changed state since the last time the MSR was read.

### RI

Trailing Edge of Ring Indicator (TERI). Bit 2 indicates that the nRI input has changed from logic "0" to logic "1".

### DCD

Delta Data Carrier Detect (DDCD). Bit 3 indicates that the nDCD input to the chip has changed state.

**Note 12.14** Whenever bit 0, 1, 2, or 3 is set to a logic "1", a MODEM Status Interrupt is generated.

### CTS

This bit is the complement of the Clear To Send (nCTS) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to nRTS in the MCR.

### DSR

This bit is the complement of the Data Set Ready (nDSR) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to DTR in the MCR.

**RI#**

This bit is the complement of the Ring Indicator (nRI) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT1 in the MCR.

**DCD**

This bit is the complement of the Data Carrier Detect (nDCD) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT2 in the MCR.

**APPLICATION NOTE:** The Modem Status Register (MSR) only provides the current state of the UART MODEM control lines in Loopback Mode. The MEC5035 does not support external connections for the MODEM Control inputs (nCTS, nDSR, nRI and nDCD) or for the four MODEM Control outputs (nDTR, nRTS, OUT1 and OUT2).

## 12.6.10 Scratchpad Register (SCR)

**Table 12.19 Scratch Pad (SCR)**

|             |            |     |     |       |     |     |                                      |     |
|-------------|------------|-----|-----|-------|-----|-----|--------------------------------------|-----|
| HOST OFFSET | 07h        |     |     | 8-bit |     |     | HOST SIZE                            |     |
| EC OFFSET   | 07h        |     |     | 8-bit |     |     | EC SIZE                              |     |
| POWER       | VCC or VTR |     |     | 00h   |     |     | nSYS_RST or<br>nSIO_RESET<br>DEFAULT |     |
| BUS         | LPC SPB    |     |     |       |     |     |                                      |     |
| BYTE3 BIT   | D7         | D6  | D5  | D4    | D3  | D2  | D1                                   | D0  |
| HOST TYPE   | R/W        | R/W | R/W | R/W   | R/W | R/W | R/W                                  | R/W |
| EC TYPE     | R/W        | R/W | R/W | R/W   | R/W | R/W | R/W                                  | R/W |
| BIT NAME    | Scratch    |     |     |       |     |     |                                      |     |

**SCRATCH**

This 8 bit read/write register has no effect on the operation of the Serial Port. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

## 12.6.11 Programmable Baud Rate Generator (and Divisor)

**Table 12.20 Programmable Baud Rate Generator (and Divisor)**

|             |                                                |     |     |       |     |     |                                      |     |
|-------------|------------------------------------------------|-----|-----|-------|-----|-----|--------------------------------------|-----|
| HOST OFFSET | BYTE1: 01h (DLAB = 1)<br>BYTE0: 00h (DLAB = 1) |     |     | 8-bit |     |     | HOST SIZE                            |     |
| EC OFFSET   | BYTE1: 01h (DLAB = 1)<br>BYTE0: 00h (DLAB = 1) |     |     | 8-bit |     |     | EC SIZE                              |     |
| POWER       | VCC or VTR                                     |     |     | 0000h |     |     | nSYS_RST or<br>nSIO_RESET<br>DEFAULT |     |
| BUS         | LPC SPB                                        |     |     |       |     |     |                                      |     |
| BYTE1 BIT   | D7                                             | D6  | D5  | D4    | D3  | D2  | D1                                   | D0  |
| HOST TYPE   | R/W                                            | R/W | R/W | R/W   | R/W | R/W | R/W                                  | R/W |
| EC TYPE     | R/W                                            | R/W | R/W | R/W   | R/W | R/W | R/W                                  | R/W |
| BIT NAME    | Baud_Rate_Divisor[15:8]                        |     |     |       |     |     |                                      |     |
| BYTE0 BIT   | D7                                             | D6  | D5  | D4    | D3  | D2  | D1                                   | D0  |
| HOST TYPE   | R/W                                            | R/W | R/W | R/W   | R/W | R/W | R/W                                  | R/W |
| EC TYPE     | R/W                                            | R/W | R/W | R/W   | R/W | R/W | R/W                                  | R/W |
| BIT NAME    | Baud_Rate_Divisor[7:0]                         |     |     |       |     |     |                                      |     |

### BAUD\_RATE\_DIVISOR

The Serial Port contains a programmable Baud Rate Generator that is capable of dividing the internal clock source by any divisor from 1 to 65535. The clock source is a 1.8432MHz clock derived from the 64.52MHz ring oscillator. The output frequency of the Baud Rate Generator is 16x the Baud rate. Two eight bit latches store the divisor in 16 bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16 bit Baud counter is immediately loaded. This prevents long counts on initial load. If a 0 is loaded into the BRG registers, the output divides the clock by the number 3. If a 1 is loaded, the output is the inverse of the input oscillator. If a two is loaded, the output is a divide by 2 signal with a 50% duty cycle. If a 3 or greater is loaded, the output is low for 2 bits and high for the remainder of the count.

Table 12.21 shows the baud rates possible.

**Table 12.21 UART Baud Rates**

| DESIRED<br>BAUD RATE | DIVISOR USED TO GENERATE<br>16X CLOCK |
|----------------------|---------------------------------------|
| 50                   | 2304                                  |
| 75                   | 1536                                  |
| 110                  | 1047                                  |

**Table 12.21 UART Baud Rates (continued)**

| DESIRED<br>BAUD RATE | DIVISOR USED TO GENERATE<br>16X CLOCK |
|----------------------|---------------------------------------|
| 134.5                | 857                                   |
| 150                  | 768                                   |
| 300                  | 384                                   |
| 600                  | 192                                   |
| 1200                 | 96                                    |
| 1800                 | 64                                    |
| 2000                 | 58                                    |
| 2400                 | 48                                    |
| 3600                 | 32                                    |
| 4800                 | 24                                    |
| 7200                 | 16                                    |
| 9600                 | 12                                    |
| 19200                | 6                                     |
| 38400                | 3                                     |
| 57600                | 2                                     |
| 115200               | 1                                     |

## 12.7 Detailed Description of Configuration Registers

### 12.7.1 Activate

**Table 12.22 Activate Register**

|             |          |    |    |    |        |    |    |                     |  |
|-------------|----------|----|----|----|--------|----|----|---------------------|--|
| HOST OFFSET | 30h      |    |    |    | 8-bit  |    |    | HOST SIZE           |  |
| EC OFFSET   | 330h     |    |    |    | 32-bit |    |    | EC SIZE             |  |
| POWER       | VTR      |    |    |    | 00b    |    |    | nSYS_RST<br>DEFAULT |  |
| BUS         | LPC SPB  |    |    |    |        |    |    |                     |  |
| BYTE0 BIT   | D7       | D6 | D5 | D4 | D3     | D2 | D1 | D0                  |  |
| HOST TYPE   | R        | R  | R  | R  | R      | R  | R  | R/W                 |  |
| EC TYPE     | R        | R  | R  | R  | R      | R  | R  | R/W                 |  |
| BIT NAME    | Reserved |    |    |    |        |    |    | Activate            |  |



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**ACTIVATE**

When this bit is 1, the UART logical device is powered and functional. When this bit is 0, the UART logical device is powered down and inactive.

**12.7.2 Configuration****Table 12.23 Configuration Select Register**

|             |          |    |    |    |       |          |       |                     |  |
|-------------|----------|----|----|----|-------|----------|-------|---------------------|--|
| HOST OFFSET | F0h      |    |    |    | 8-bit |          |       | HOST SIZE           |  |
| EC OFFSET   | 3F0h     |    |    |    | 8-bit |          |       | EC SIZE             |  |
| POWER       | VTR      |    |    |    | 00b   |          |       | nSYS_RST<br>DEFAULT |  |
| BUS         | LPC SPB  |    |    |    |       |          |       |                     |  |
| BYTE0 BIT   | D7       | D6 | D5 | D4 | D3    | D2       | D1    | D0                  |  |
| HOST TYPE   | R        | R  | R  | R  | R     | R        | R     | R/W                 |  |
| EC TYPE     | R        | R  | R  | R  | R     | R/W      | R/W   | R                   |  |
| BIT NAME    | Reserved |    |    |    |       | Polarity | Power | Reserved            |  |

**POWER**

When this bit is 1, the UART Runtime Registers (the registers at offsets 0h through 7h from the base of the UART Logical Device) are controlled by VCC. They are set to their POR defaults on a [nSIO\\_RESET](#). In addition, pins associated with the UART are powered down and place in a High-Z state on [nSIO\\_RESET](#).

When this bit is 0, the UART Runtime Registers are controlled by VTR. They are set to their POR defaults on an [nSYS\\_RST](#). In addition, the state of the UART pins is controlled by VTR.

**POLARITY**

When the Polarity bit is asserted ('1'), the UART\_TX and UART\_RX pins functions are inverted. When the Polarity bit is not asserted (default), the UART\_TX and UART\_RX pins functions are not inverted.



## 12.8 Sleep Enable/ Clock Request Power state controls

**Table 12.24 Generic Block Clocking Model Behavior**

| EXTERNAL SLEEP INPUT | BLOCK IDLE STATUS | CLOCK REQUIRED STATUS OUTPUT ( | STATE              | DESCRIPTION                                                                                                                                                                      |
|----------------------|-------------------|--------------------------------|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| X                    | X                 | 0                              | DISABLED           | Block is disabled by firmware and the core clock is not needed. Note: it is up to the host to guarantee that the block is not in use before the internal ENABLE bit is asserted. |
| 0                    | NOT IDLE          | 1                              | NORMAL OPERATION   | The block is neither disabled by firmware nor commanded to sleep.                                                                                                                |
|                      | IDLE              | 0                              |                    |                                                                                                                                                                                  |
| 1                    | NOT IDLE          | 1                              | PREPARING TO SLEEP | A sleep command has been asserted but the core clock is still required because the block is not idle.                                                                            |
|                      | IDLE              | 0                              | SLEEPING           | A sleep command has been asserted, the block is idle and the core clock can be stopped.                                                                                          |

## 12.9 Two Pin Serial Port (UART) Revision History

This revision history shows the changes made to this chapter.

**Table 12.25 Two Pin Serial Port (UART) Chapter Revision History**

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History,"</a> on page 539. |              |            |                                                                                                                             |                                                                                                                                                                  |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------------|-----------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE       | SECTION/FIGURE/ENTRY                                                                                                        | CORRECTION                                                                                                                                                       |
| 1.                                                                                                                                                                                                                                          | 0.6          | 07/05/2007 | <a href="#">Note 12.3 on page 228</a><br><br><a href="#">Break Interrupt on page 240 bit in Line Status (LSR) Register.</a> | Added note that EC or JTAG should be limited to 8-bit access to UART runtime registers. Duplicated Frame Error bit description removed from Break Interrupt bit. |
| 2.                                                                                                                                                                                                                                          |              |            |                                                                                                                             |                                                                                                                                                                  |
| 3.                                                                                                                                                                                                                                          |              |            |                                                                                                                             |                                                                                                                                                                  |
| 4.                                                                                                                                                                                                                                          |              |            |                                                                                                                             |                                                                                                                                                                  |



## Chapter 13 JTAG and XNOR

### 13.1 General Description

This chapter describes the MEC5035 Modified ARC JTAG port and the internal blocks and features that are accessed by it. These consist of:

- The JTAG port itself
- The JTAG port's interfaces to registers and the bus addressing space
- Other dedicated hardware features which may be incorporated for software debug (Actionpoints, HALT Input, Reset Input).

The ARC JTAG port is not intended for traditional Boundary Scan. Instead, its primary function is to provide a low pin-count interface for debugging the firmware running on the ARC Embedded Controller.

A secondary capability incorporated by SMSC are additional Test Mode Registers, see [Figure 13.1](#) and [JTAG Test Mode Data Registers](#) for Test Mode details.

#### 13.1.1 ARC JTAG Capabilities

- Fully compliant with IEEE1149.1 standard for a non-boundary-scan capable device
- Does not perform Boundary Scan
- 4-bit Instruction Register
- Standard 1-bit BYPASS register
- Standard 32-bit IDCODE register
- Four JTAG registers give access to on-chip memory and register resources
- Can read or write a 32-bit quantity from or to any ARC Core Register, Aux Register or 32-bit aligned memory location. No other interfaces are provided or needed
- Accesses to Aux Registers and Memory do not require the ARC processor to be halted
- Memory accesses are always performed in units of 32 bits

### 13.2 ARC JTAG System Block Diagram

- The ARC JTAG Port is defined in the ARC 600 External Interfaces Reference Manual, Chapter 2. The SMSC modifications are described in this chapter. The ARC JTAG Port has been modified by SMSC to provide additional Data Registers (see [Note 13.6](#).) The TEST MODE Register provide additional on-chip support specific to the MEC5035.

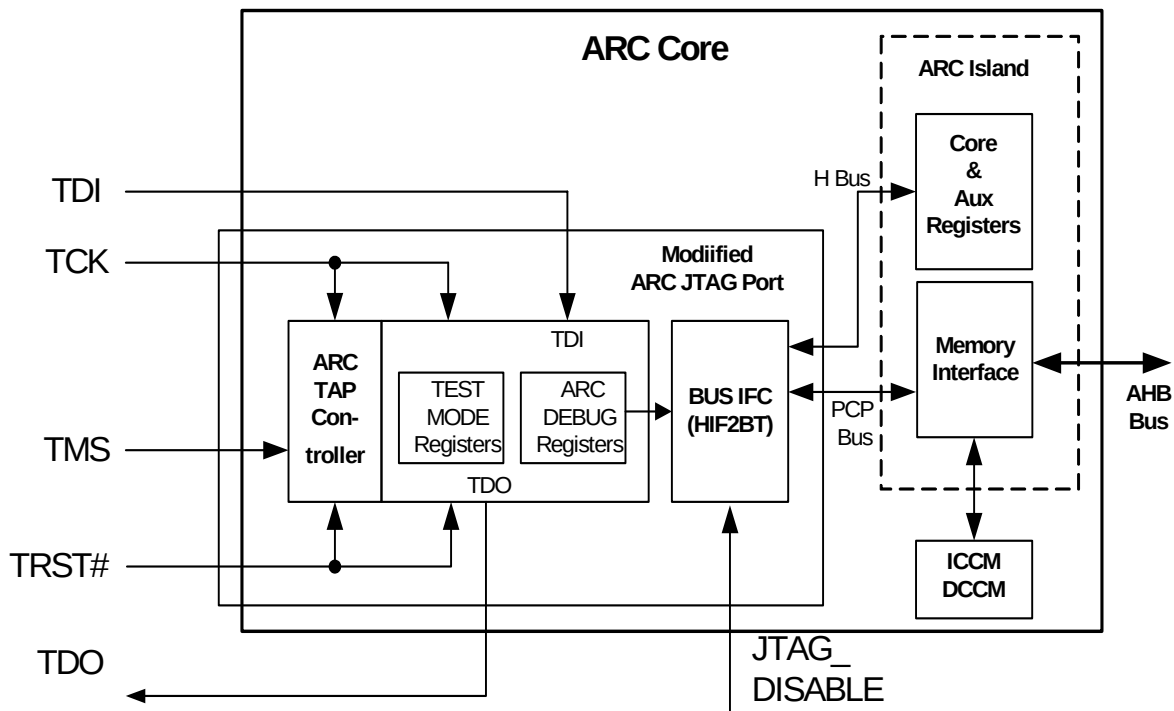


**Figure 13.1 Block Diagram of JTAG System**

As shown in [Figure 13.1](#), the ARC JTAG Port sits within the ARC Core, between the JTAG signals and the ARC Island block, which contains the Core and Aux register sets and the Memory Interface to the Closely-Coupled Memories (ICCM / DCCM) and the AHB Bus (FLASH memory and Memory-Mapped I/O registers). It is not associated with any form of Boundary Scan, but instead is used by an external JTAG host to access memory and register resources on behalf of a debugger program. There are no other connections between the ARC JTAG Port and the rest of the ARC Core: register access is enough to halt and restart the processor, as well as to detect that the processor has halted (a continuous poll on the STATUS32 Aux Register).

Internally, the ARC JTAG port consists of the following sub-blocks:

- The ARC Test Access Port (TAP) Controller. This block is driven by the JTAG\_CLK, TMS and JTAG\_RST# inputs, and provides the control signals for the JTAG data transfers. It is a single state machine consisting of 16 states, whose transitions are controlled strictly by the state of TMS on each rising edge of JTAG\_CLK. The low-active JTAG\_RST# input provides an asynchronous reset, though JTAG\_CLK and TMS together can also bring the TAP Controller to the reset state (5 consecutive JTAG\_CLK rising edges with TMS=1).
- The ARC DEBUG & TEST MODE Registers blocks. This blocks handles the data transfers as directed by the TAP, and contains the registers and shift registers internal to the JTAG Port. The holding registers in this block consist of a 4-bit Instruction register, a 1-bit Bypass register, and a set of Data registers (see [Note 13.6](#)) of various lengths. There are three sets of Data Registers: [JTAG Standard Data Registers](#), [JTAG Debug Data Registers](#), & [JTAG Test Mode Data Registers](#). The [JTAG Test Mode Data Registers](#) provide additional on-chip support specific to the MEC5035.
- The Bus Interface block. This block accepts values for the [JTAG Debug Data Registers](#): ADDRESS, DATA, STATUS and TRANSACTION COMMAND, and uses them to request data transfers from the ARC's inner core ("Island") sub-block. \
- As part of the Boot block portection the JTAG Port's [JTAG Debug Data Registers](#) can be disabled to prevent an external debugger from potentially halting the EC and then reading or reprogramming any word in the Boot Block.

## 13.3 JTAG Port Signal Interface Description

The signal pins are defined in [Table 3.8, "JTAG Interface," on page 43](#).

The JTAG\_CLK input is the clock that drives the JTAG interface. It is asynchronous to other clocks on-chip.

The TMS input is sampled on each rising edge of JTAG\_CLK, and governs the transitions among the 16 states of the state machine (TAP) that controls the transfer of data.

The TDI input is the serial data input, shifted in during the Shift-IR and Shift-DR states of the TAP. It is sampled on rising edges of JTAG\_CLK.

The TDO output is the serial data output. It is presented on falling edges of JTAG\_CLK, 1/2 clock before each input shift, to provide setup and hold time to the next JTAG controller in the chain. The final TDO output pin, after all on-chip chaining ([Figure 13.1](#)) is held in high-impedance mode (floating) except when valid data is being presented. The enabled/disabled state of the pin is also changed on falling edges of JTAG\_CLK.

The JTAG\_RST# input provides the [Async JTAG RESET](#). Note that the reset state of the JTAG port is only local to the JTAG port: its effect is to keep the JTAG port in an idle state and to disengage it from the rest of the system, so that it does not affect other on-chip logic in this state.

## 13.4 Power, Clocks and Reset

See [Section 34.10, "JTAG Interface Timing," on page 537](#) power on sequence and reset timing.

### 13.4.1 Power Domains

The ARC JTAG block is powered by VTR.

### 13.4.2 Clocks

The ARC JTAG port runs internally from the externally-provided JTAG\_CLK clock pulses only. There is no requirement for JTAG\_CLK to be constantly running.

The following JTAG Registers interface to the ARC Island block (as illustrated in [Figure 13.1](#)) for access to registers and memory: [STATUS Register \(8h\)](#), [TRANSACTION COMMAND Register \(9h\)](#), & [ADDRESS Register \(Ah\)](#), [DATA Register \(Bh\)](#). There is a clock relationship required between JTAG\_CLK and the ARC Core clock frequency. JTAG\_CLK may be asynchronous, but it must be slower than 1/2 the frequency of the ARC Core clock. In practical terms, then, JTAG\_CLK should be selected to be nominally 1/4 of the minimum Core clock frequency. See [APPLICATION NOTE: on page 107](#).

**APPLICATION NOTE:** The Ashling JTAG interface box is not documented to operate any slower than JTAG\_CLK = 1MHz, therefore the Core must be running at 4MHz in order to run the ARC debugger through the JTAG interface using the Ashling interface.

Stopping the Core clock disables the JTAG port for debugging purposes. It does not affect IDCODE or BYPASS operation.

See [Section 34.10, "JTAG Interface Timing," on page 537](#) for the maximum frequency  $f_{clk}$  on the JTAG\_CLK pin to access a JTAG Registers other than [STATUS Register \(8h\)](#), [TRANSACTION COMMAND Register \(9h\)](#), & [ADDRESS Register \(Ah\)](#), [DATA Register \(Bh\)](#).

### 13.4.3 Reset

The ARC JTAG block has two resets: [Async JTAG RESET](#) by its JTAG\_RST# input and [Sync JTAG RESET](#) by JTAG protocol.



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**13.4.3.1 Async JTAG RESET**

The JTAG\_RST# pin provides the [Async JTAG RESET](#) to the JTAG Registers. The JTAG\_RST# pin has an active low, asynchronous assertion and a synchronous deassertion. The JTAG Registers will be reset asynchronously (and immediately) upon the active low JTAG\_RST# assertion. Once the JTAG\_RST# pin has been asserted, the JTAG\_RST# pin is deasserted and three JTAG\_CLK's in order to access the JTAG Registers. The JTAG Registers will remain in reset until the three clocks complete the synchronous JTAG\_RST# pin deassertion. See [Section 34.10, "JTAG Interface Timing," on page 537](#).

**APPLICATION NOTE:** After asserting and deasserted the JTAG\_RST# pin, a [Sync JTAG RESET](#) can be applied before starting to access the JTAG Registers (to meet the JTAG\_RST# synchronous deassertion requirement).

**Note 13.2** JTAG registers, in particular the [JTAG Test Mode Data Registers](#), are set to their initial values by the assertion of the JTAG\_RST# pin, not the VTR Power On Reset. JTAG\_RST# must be held low while the MEC5035 is powering up so the registers can be set to their proper default values. If JTAG\_RST# is high during power up, the [JTAG Test Mode Data Registers](#) may be set to unpredictable values, which may trigger unwanted test modes.

**APPLICATION NOTE:** Care should be taken during VTR power up to insure that JTAG\_RST# is asserted for a longer time than the VTR rise time due to capacitive loading.

**13.4.3.2 Sync JTAG RESET**

It can also be reset synchronously by a JTAG\_CLK / TMS sequence, in accordance with the JTAG standard. A series of 5 successive JTAG\_CLK rising edges, with TMS held high throughout, will accomplish this from any state.

The ARC JTAG port, upon entering its Reset state, will be prepared to accept an Instruction or Data transfer. It will also be disengaged from external circuitry, allowing it to operate normally.

The initial contents of the Instruction Register are the IDCODE command (Ch). If a Data transfer is performed first after Reset, without an preceding Instruction transfer, then the IDCODE value will be loaded into its 32-bit shift register and presented serially, after which will appear the bits shifted in from TDI.

The initial contents of the Data registers are as listed in [Table 13.1 on page 256](#).

**13.5 Interrupts**

There are no interrupts assigned to the ARC JTAG block. Control of the processor is performed by monitoring, setting and clearing the H bit (Halt) in the Aux register STATUS32, and by register manipulations while the processor is halted.

However, any interrupt or other event that can be triggered by accessing registers (Core, Aux or Memory-Mapped) can be triggered through the JTAG port.

**13.6 JTAG Background**

The following is a simplified description, intended to provide background for the ARC JTAG port. For full details, see the JTAG specification (IEEE Standards 1149.1 and 1149.1b).

**13.6.1 Internal Structure**

A JTAG port operates by transferring information serially into and out of an Instruction register and one or more Data registers. These registers are connected in parallel with each other, and can be of arbitrary length. See [Figure 13.3](#).

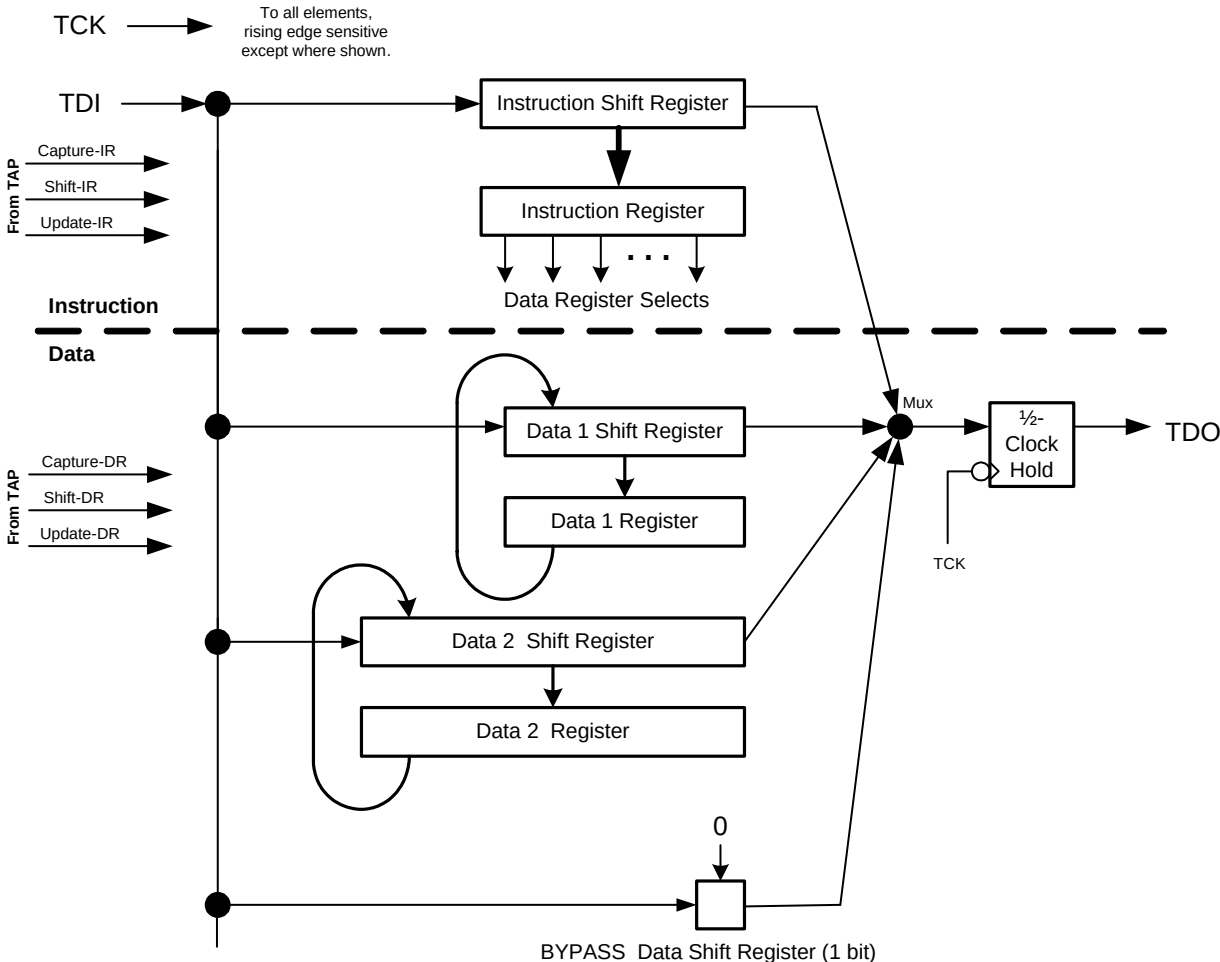


**Figure 13.3 Structure of a JTAG Port (Simplified)**

The protocol for shifting information makes a distinction between an Instruction transfer (to/from a single Instruction register) and a Data transfer (to/from one of several Data registers). The Instruction register is handled separately because it selects which specific Data register is accessed by subsequent Data transfers.

In daisy-chained JTAG controllers, the Instruction registers form one chain, and the currently-selected set of Data registers in each JTAG controller combine to form a second chain. To shorten the Data chain when not all JTAG controllers are of interest, a mandatory one-bit Data register called BYPASS is provided. There is no bypassing for the Instruction chain, so its full length must be shifted as each new instruction is transferred anywhere. Selecting the BYPASS Data register is the equivalent of a No-Operation instruction for a JTAG controller, and this instruction is always defined as a '1' in all Instruction register bits.

Each entity called a "Register" actually consists of two parts: the Register itself, and an associated Shift Register which connects to TDI and TDO. The Register may load from, and/or source information in parallel to, the Shift Register. These two parts are the same length, meaning that (for example) a 5-bit Register will be associated with a 5-bit Shift Register.

The Instruction register and the Data registers respond to decoded state signals from the TAP Controller sub-block ([Section 13.6.2](#)), which represent sub-steps of a transfer. The sub-steps they perform are **Capture**, which loads the shift register in parallel, **Shift**, which shifts information in from TDI and out on TDO, and **Update**, which writes information from the Shift Register in parallel. The **Capture-IR**, **Shift-IR** and **Update-IR** controls affect only the Instruction register. The **Capture-DR**,

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**Shift-DR** and **Update-DR** controls affect only the Data register that is currently selected by the contents of the Instruction register.

## 13.6.2 TAP Controller and Protocol

The JTAG protocol is driven by the level of the TMS (Test Mode Select) input pin at each rising edge of the JTAG\_CLK clock. This is the responsibility of the TAP Controller section of the JTAG controller, which performs state transitions as illustrated in the state diagram in [Figure 13.4](#). States whose names end with "IR" affect the Instruction register (the rightmost column of states in [Figure 13.4](#)), and those ending with "DR" affect a Data register (the middle column in [Figure 13.4](#)). Note that the TMS signal goes in parallel to all JTAG ports in a chain, so they are always in the same protocol state. The sequence of accessing any register is as follows:

- Capture (IR or DR), which loads a shift register from its source in preparation for shifting it out. In the case of the Instruction register, this is a fixed value, and not the previous contents of the Instruction register. In the case of the BYPASS Data register, this is a fixed '0' value. The Capture state is transitory, being present for only one JTAG\_CLK cycle, once per transfer.
- Shift (IR or DR), which shifts the Captured information in the Shift Register out on the TDO pin while also shifting information in from the TDI pin. The registers (by convention) shift from left to right, so the least-significant bit of a value is transferred first. This state may be held arbitrarily (holding TMS=0) to shift as many bits as desired.
- Update (IR or DR), which loads a Register from its Shift Register after the shifting has completed. The Update state is transitory, being present for only one JTAG\_CLK cycle, once per transfer.

There is also a Pause state (IR or DR) which may be used to exit and re-enter the Shift state without terminating the transfer in progress. This state may be held (TMS=0) in order to delay for any desired number of JTAG\_CLK cycles.

Outside of Instruction or Data transfers, there are two states which may be entered and held. These are shown in the leftmost column in [Figure 13.4](#).

- The Test-Logic-Reset state holds the JTAG logic in its reset state. This re-initializes the registers that are internal to the JTAG logic. This state is entered asynchronously by assertion of JTAG\_RST# low, and it can be seen in [Figure 13.4](#) that, from any other state, this state will be entered by 5 successive JTAG\_CLK cycles with TMS held to '1'.
- Run-Test/Idle holds JTAG logic idle, but not reset, between transfers.



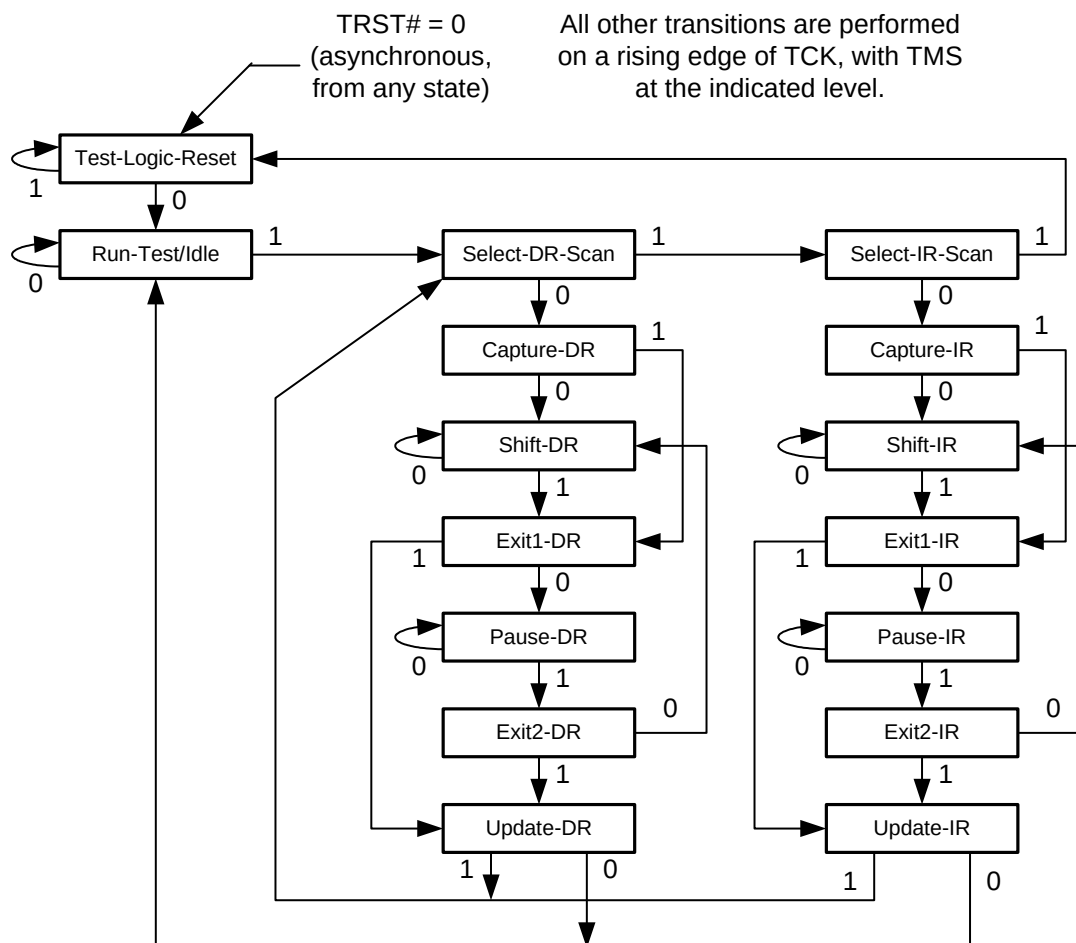


Figure 13.4 TAP Controller State Diagram

### 13.6.3 Interface Timing Example

Figure 13.5 illustrates the timing relationship between data shifting and the TAP Controller's Shift states, using a 1-bit Data register as an example. (This is in fact the exact situation when the BYPASS Data register is selected: refer to Figure 13.3 on page 252.)

The TAP Controller changes states on each rising edge of JTAG\_CLK, traversing the state table in Figure 13.4 as directed by the TMS input signal from the external interface.

Previous to the waveform in Figure 13.5, the TAP Controller has already passed through a Capture-DR state, so the 1-bit Shift Register has been pre-loaded with a "Capture Value", either from its associated parallel Register or from another source. (For the BYPASS register, this would be a fixed '0'.)

At the first rising edge of JTAG\_CLK in Figure 13.5, the Shift-DR state is being entered. As yet, no valid data needs to be present on TDI or TDO.

At the first falling edge of JTAG\_CLK, while the Shift-DR state is active, the TDO pin begins presenting the least-significant bit of the Shift Register (the only bit, in this example), which is holding the Captured Value. At about this time also, the external interface will drive TDI to the desired new state for this Data register.

At the next rising edge of JTAG\_CLK, the Shift-DR state is exited, and that same clock edge is used to actually perform the commanded shift. The TDI value "A" is shifted into the Shift Register. This same

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rising edge of JTAG\_CLK is used by the external interface to shift in the Captured Value from TDO. The TDO output does not change yet, because it is held by a 1/2 clock delay stage (see [Figure 13.3 on page 252](#)), providing hold time for the external interface.

On the next falling edge, the TDO output changes. Since the Shift state is no longer present, TDO is not required at this time to present valid data, and in fact for an off-chip connection it is required to float at this time.

After this timing diagram completes, the TAP machine will continue to an Update-DR state, at which time the value A, now present in the Shift Register, will be written to its destination. (In the specific case of the BYPASS register, there is no destination, and that step will do nothing.)

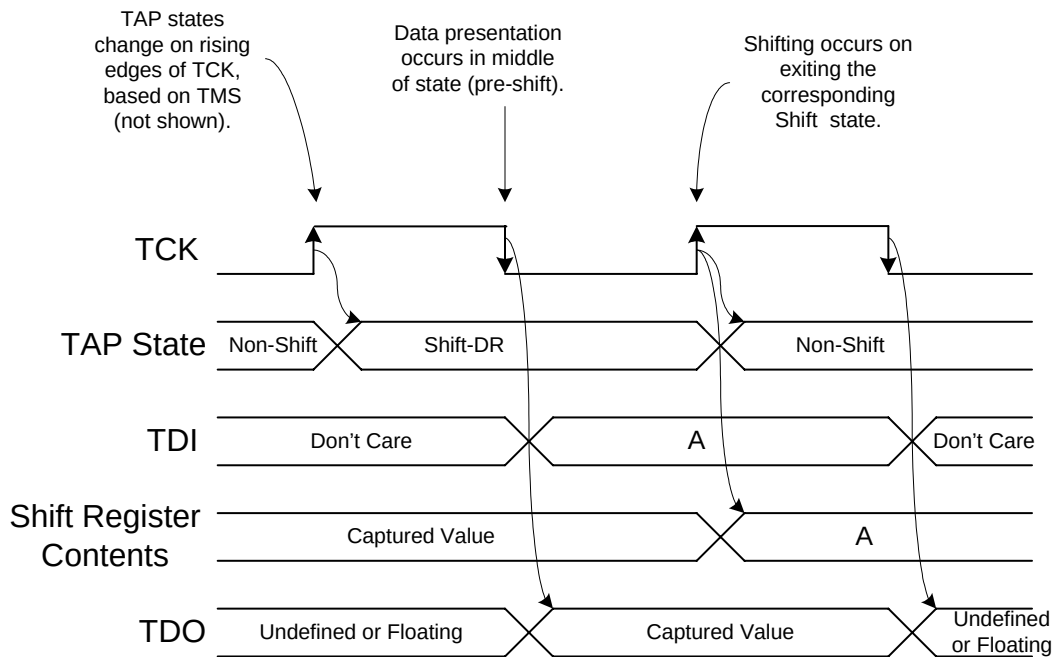


**Figure 13.5 Timing Illustration: 1-Bit Data Register**

## 13.7 Registers

The ARC JTAG Port is defined in the ARC 600 External Interfaces Reference Manual, Chapter 2.

There are no JTAG registers accessible in any EC or AHB memory space. JTAG registers are accessible only through the JTAG pins themselves ([Section 13.7.1, "Instruction Register," on page 255](#)).

### 13.7.1 Instruction Register

The Instruction Register is four bits wide. It selects among the implemented Data Registers as listed in [Table 13.1](#). When the Tap Controller is placed into the Test-Logic-Reset state, the Instruction register is initialized to Ch, selecting the IDCODE Data Register.

Table 13.1 ARC JTAG Instruction Register Encodings

| Instruction Register Contents | Data Register Selected     | Function of Data Register                                                                               | Width (bits) | State on JTAG Reset (Hex)          |
|-------------------------------|----------------------------|---------------------------------------------------------------------------------------------------------|--------------|------------------------------------|
| 0h                            | (Reserved: EXTEST)         | Not implemented, but reserved as required by JTAG standard.                                             | 32           | 0000_0000h                         |
| 1h                            | (Reserved: SAMPLE/PRELOAD) | Not implemented, but reserved as required by JTAG standard.                                             | 32           | 0000_0000h                         |
| 2h                            | RESET TEST                 | <a href="#">RESET TEST Register (2h)</a>                                                                | 32           | 0000_0000h                         |
| 3h                            | TEST                       |                                                                                                         | 32           | 0000_0000h                         |
| 4h                            | (Reserved)                 | Reserved for future use.)                                                                               | 32           | 0000_0000h                         |
| 5h                            | (Reserved)                 | (Reserved for future use.)                                                                              | 32           | 0000_0000h                         |
| 6h                            | (Reserved)                 | (Reserved for future use.)                                                                              | 32           | 0000_0000h                         |
| 7h                            | (Reserved)                 | (Reserved for future use.)                                                                              | 32           | 0000_0000h                         |
| 8h                            | STATUS                     | <a href="#">STATUS Register (8h)</a><br>Status of Current Debugger Transaction (Read-Only)              | 4            | undefined (based on bus status)    |
| 9h                            | TRANSACTION COMMAND        | <a href="#">TRANSACTION COMMAND Register (9h)</a><br>Initiates / Specifies a Debugger Transaction       | 4            | 3                                  |
| Ah                            | ADDRESS                    | <a href="#">ADDRESS Register (Ah)</a><br>Address of a Debugger Transaction                              | 32           | 0000_0000h                         |
| Bh                            | DATA                       | <a href="#">DATA Register (Bh)</a><br>Data In / Data Out for Debugger Transactions                      | 32           | Out = 0000_0000h<br>In = undefined |
| Ch                            | IDCODE                     | <a href="#">IDCODE Register (Ch)</a><br>JTAG Standard IDCODE Register (Capture = Read-Only fixed value) | 32           | 1000_24B1h                         |
| Dh                            | (Reserved)                 |                                                                                                         | 32           | 0000_0000h                         |
| Eh                            | (Reserved)                 | Reserved for future use.)                                                                               | 32           | 0000_0000h                         |
| Fh                            | BYPASS                     | <a href="#">BYPASS Register (Fh)</a><br>JTAG Standard BYPASS Register (Capture = Read-Only '0')         | 1            | 0                                  |

## 13.7.2 JTAG Debug Data Registers

**Note 13.6** Unfortunately, ARC names one of its JTAG Debug Data registers “DATA”. To avoid confusion, while maintaining the terminology in both ARC and JTAG documentation, the term “Data register” will refer to any of the JTAG Data registers, and the term “DATA register” (all upper-case) will refer to the specific JTAG Data register that is selected by Instruction Register = B. See [Section 13.7.2.2, “DATA Register \(Bh\),” on page 257](#).

The Debug Data Register set of the ARC JTAG Port provide the means for an external JTAG-connected debugger system to monitor and control the execution of a program. Using the JTAG Data registers ADDRESS, DATA, TRANSACTION COMMAND and STATUS, the debugger can perform “transactions” to read or write:

- Any Aux Register, giving it the ability to start, halt or step a program, and alter the PC and/or program status
- Any addressable memory or I/O location, as an aligned 32-bit value



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- Any Core Register, if the processor is in a halted state

To write to a specific register or a memory location, the debugger will place the desired register number or memory address into the ADDRESS register, place the value to be written into the DATA register, and then trigger the transfer by placing the direction and addressing space (Core register / Aux register / Memory) into the TRANSACTION COMMAND register. It will then read the STATUS register until it indicates that the transaction is finished.

To read from a specific register or memory location, the debugger will place the desired register number or memory address into the ADDRESS register, and trigger the transfer by placing the direction and addressing space (Core register / Aux register / Memory) into the TRANSACTION COMMAND register. It will then read the STATUS register until it indicates that the transaction is finished, and read the DATA register to access the value.

Optimizations are possible in repeated accesses, because of the actions of the ADDRESS and DATA registers, as described in [Section 13.7.2.1](#) and [Section 13.7.2.2](#).

### 13.7.2.1 ADDRESS Register (Ah)

The ADDRESS register is a 32-bit register which receives from the debugger either a Core Register number, an Aux Register number or an address in the Memory space (memory or I/O).

**Note:** As a memory address, the low-order 2 bits of the ADDRESS register are ignored (assumed by hardware to be 00), and a full 32-bit value is referenced at that location. There is no way for the debugger to specify a smaller width of data, and so a write to a single byte (for example) is performed using a read transaction followed by a write transaction, preserving the values of the unaffected bytes.

After use, the ADDRESS register automatically increments, by 1 if a register was accessed, and by 4 if a memory location was accessed. Therefore, as long as the JTAG TAP Controller is not brought to the Test-Logic-Reset state between accesses, it is not necessary to provide a new ADDRESS register value between transactions involving successive registers or memory locations. (The Test-Logic-Reset state must be avoided because it resets the value of the ADDRESS register.)

**Table 13.2 ADDRESS Register**

| INSTRUCTION REGISTER CONTENTS | Ah            |       |       | 32 bits    |   |      | REGISTER SIZE                                        |      |
|-------------------------------|---------------|-------|-------|------------|---|------|------------------------------------------------------|------|
| POWER                         | VTR           |       |       | 0000_0000h |   |      | Async JTAG RESET<br>OR<br>Sync JTAG RESET<br>DEFAULT |      |
| BIT                           | BIT31         | BIT30 | BIT29 | ...        |   | BIT2 | BIT1                                                 | BIT0 |
| JTAG TYPE                     | -             | -     | -     | -          | - | -    | -                                                    | -    |
| BIT NAME                      | Address[31:0] |       |       |            |   |      |                                                      |      |

### 13.7.2.2 DATA Register (Bh)

The DATA register is a 32-bit register which is the ARC JTAG Port's portal for data values that are being read or written by a transaction. When writing to a register or memory, the DATA register will be set up by the debugger before the transaction is triggered. When reading from a register or memory, the DATA register will be read by the debugger as the last step of the transaction. See [Note 13.2 on page 251](#).



The DATA register is not affected at the end of a write transaction, so (for example) to fill successive locations with the same value it is not necessary to provide it again, as long as the Test-Logic-Reset of the JTAG TAP Controller is not entered (which would clear it).

**Table 13.3 DATA Register**

|                                      |              |              |              |            |   |             |                                                      |             |
|--------------------------------------|--------------|--------------|--------------|------------|---|-------------|------------------------------------------------------|-------------|
| <b>INSTRUCTION REGISTER CONTENTS</b> | Bh           |              |              | 32 bits    |   |             | <b>REGISTER SIZE</b>                                 |             |
| <b>POWER</b>                         | VTR          |              |              | 0000_0000h |   |             | Async JTAG RESET<br>OR<br>Sync JTAG RESET<br>DEFAULT |             |
| <b>BIT</b>                           | <b>BIT31</b> | <b>BIT30</b> | <b>BIT29</b> | ...        |   | <b>BIT2</b> | <b>BIT1</b>                                          | <b>BIT0</b> |
| <b>JTAG TYPE</b>                     | -            | -            | -            | -          | - | -           | -                                                    | -           |
| <b>BIT NAME</b>                      | Data[31:0]   |              |              |            |   |             |                                                      |             |

### 13.7.2.3 TRANSACTION COMMAND Register (9h)

The TRANSACTION COMMAND register is written by the debugger to trigger a transaction. It is a 4-bit register, which is written with one of the values in [Table 13.5](#) to specify the direction and addressing space of the transaction.

**Table 13.4 DATA Register**

|                               |              |      |        |      |                                                      |
|-------------------------------|--------------|------|--------|------|------------------------------------------------------|
| INSTRUCTION REGISTER CONTENTS | 9h           |      | 4 bits |      | REGISTER SIZE                                        |
| POWER                         | VTR          |      | 0h     |      | Async JTAG RESET<br>OR<br>Sync JTAG RESET<br>DEFAULT |
| BIT                           | BIT3         | BIT2 |        | BIT1 | BIT0                                                 |
| JTAG TYPE                     | -            | -    |        | -    | -                                                    |
| BIT NAME                      | Command[3:0] |      |        |      |                                                      |



Table 13.5 TRANSACTION COMMAND Register Encodings

| Encoding (Binary) | Transaction Type          |
|-------------------|---------------------------|
| 0000              | Write to Memory space     |
| 0001              | Write to a Core register  |
| 0010              | Write to an Aux register  |
| 0011              | No Operation              |
| 0100              | Read from Memory space    |
| 0101              | Read from a Core register |
| 0110              | Read from an Aux register |
| 0111              | (obsolete Write form)     |
| 1000              | (obsolete Read form)      |
| (other)           | Reserved                  |

#### 13.7.2.4 STATUS Register (8h)

The STATUS register is a 4-bit read-only register. It is read by the debugger to determine when a transaction has completed internally, and when the next transaction may be started. It also provides additional status information useful to the debugger.

Table 13.6 STATUS Register

| INSTRUCTION REGISTER CONTENTS | 8h   | 4 bits |      |      | REGISTER SIZE                                        |
|-------------------------------|------|--------|------|------|------------------------------------------------------|
| POWER                         | VTR  | 0h     |      |      | Async JTAG RESET<br>OR<br>Sync JTAG RESET<br>DEFAULT |
| BIT                           | BIT3 | BIT2   | BIT1 | BIT0 |                                                      |
| JTAG TYPE                     | R    | R      | R    | R    |                                                      |
| BIT NAME                      | -PC  | -RD    | FL-  | ST-  |                                                      |

#### (ST): STALLED

- 1 = The current transaction is stalled (busy)
- 0 = The current transaction is not stalled (not busy)

#### (FL): FAILURE

- 1 = The transaction has failed
- 0 = The transaction has not failed

A transaction will fail if it attempts to access a Core register while the processor is running. Bus errors should also set this bit (specifics TBD).

**(RD): READY**

1 = The transaction is finished (ready)

0 = The transaction is not finished

**(PC): PC\_SEL**

This bit has no direct hardware effect. It displays the state of the PC\_SEL signal, which is bit 0 of the write-only Aux register PCPORT (Aux Register #24h). This bit is initialized to '1' on a processor reset, and is used internally by the debugger system as a means to communicate configuration information.

### 13.7.3 JTAG Standard Data Registers

#### 13.7.3.1 IDCODE Register (Ch)

This is a 32-bit read-only register containing the hex value 1000\_24B1. It serves to identify the ARC JTAG Port as belonging to an ARC600 core, in a component containing one processor.

IDCODE registers are required to conform to the JTAG standard, and they contain an 11-bit Manufacturer ID number, so

**Table 13.7 IDCODE Register**

| INSTRUCTION REGISTER CONTENTS | Ch           |       |       | 32 bits    |   |      | REGISTER SIZE                                        |      |
|-------------------------------|--------------|-------|-------|------------|---|------|------------------------------------------------------|------|
| POWER                         | VTR          |       |       | 1000_24B1h |   |      | Async JTAG RESET<br>OR<br>Sync JTAG RESET<br>DEFAULT |      |
| BIT                           | BIT31        | BIT30 | BIT29 | ...        |   | BIT2 | BIT1                                                 | BIT0 |
| JTAG TYPE                     | R            | R     | R     | R          | R | R    | R                                                    | R    |
| BIT NAME                      | IDCODE[31:0] |       |       |            |   |      |                                                      |      |

#### 13.7.3.2 BYPASS Register (Fh)

The BYPASS register consists only of a 1-bit shift register cell. The Capture-DR state clears it to '0' when selected. The Update-DR state does nothing.

The function of this register is to provide the minimum amount of delay (one bit of '0') when other JTAG ports on the chain are being exercised.

**Table 13.8 BYPASS Register**

|                                      |             |            |                                                      |
|--------------------------------------|-------------|------------|------------------------------------------------------|
| <b>INSTRUCTION REGISTER CONTENTS</b> | Fh          | 1 bit      | <b>REGISTER SIZE</b>                                 |
| <b>POWER</b>                         | VTR         | 1000_24B1h | Async JTAG RESET<br>OR<br>Sync JTAG RESET<br>DEFAULT |
| <b>BIT</b>                           | <b>BIT0</b> |            |                                                      |
| <b>JTAG TYPE</b>                     |             |            |                                                      |
| <b>BIT NAME</b>                      | BYPASS      |            |                                                      |

### 13.7.4 JTAG Test Mode Data Registers

JTAG Test Registers are 32-bit read/write registers that are used for test functions. These registers are always available to the JTAG port, even if access to the other JTAG registers is blocked

#### 13.7.4.1 RESET TEST Register (2h)

The RESET TEST Register is a 32-bit register used to explicitly control reset functions inside the MEC5035. The default for this register is 0000\_0000h.

**Table 13.9 RESET TEST Register**

|                                      |                   |              |               |               |               |               |                             |              |
|--------------------------------------|-------------------|--------------|---------------|---------------|---------------|---------------|-----------------------------|--------------|
| <b>INSTRUCTION REGISTER CONTENTS</b> | 2h                |              | 32 bits       |               |               |               | <b>REGISTER SIZE</b>        |              |
| <b>POWER</b>                         | VTR               |              | 0000_0000h    |               |               |               | Async JTAG RESET<br>DEFAULT |              |
| <b>BIT</b>                           | <b>Bits 31-14</b> |              | <b>Bit 13</b> | <b>Bit 12</b> | <b>Bit 11</b> | <b>Bit 10</b> | <b>Bit 9</b>                | <b>Bit 8</b> |
| <b>JTAG TYPE</b>                     | R                 | R            | R             | R             | R             | R             | R/W                         | R/W          |
| <b>BIT NAME</b>                      | Reserved          |              | Test          | Test          | Test          | Test          | Test                        | Test         |
| <b>BIT</b>                           | <b>Bit 7</b>      | <b>Bit 6</b> | <b>Bit 5</b>  | <b>Bit 4</b>  | <b>Bit 3</b>  | <b>Bit 2</b>  | <b>Bit 1</b>                | <b>Bit 0</b> |
| <b>JTAG TYPE</b>                     | R/W               | R/W          | R/W           | R/W           | R/W           | R/W           | R/W                         | R/W          |
| <b>BIT NAME</b>                      | Test              | Test         | Test          | Test          | POR<br>EN     | VTR<br>POR    | VCC<br>POR                  | Test         |

#### VCC POR

Asserts VCC Power On Reset: When the **VCC POR** active low bit is asserted '0' while the field **POR EN** in this register is '1', forces a VCC Power On Reset. When the **VCC POR** active low bit de-asserted '1', the VCC POR circuitry returns to its normal state.



**VTR POR**

Asserts VTR Power On Reset: When the **VTR POR** active low bit is asserted '0' while the field **POR EN** in this register is '1', forces a VTR Power On Reset. When the **VTR POR** active low bit de-asserted '1', the VCC POR circuitry returns to its normal state.

**POR EN**

Power On Reset Enable. When '1', the reset functions controlled by **VCC POR** and **VTR POR** are enabled. When '0', the **VCC POR** and **VTR POR** fields in this register have no effect on the POR circuitry.

**TEST**

All TEST bits should be set to '0' when writing this register.

**13.7.4.2 TEST REGISTER 4/Reset Register (Dh)**

The RESET TEST Register is a 32-bit register used to explicitly control reset functions inside the MEC5035. The default for this register is 0000\_0000h.

**ARC\_FAST\_RESET**

If this bit is '1b', the reset going to the ARC processor and select peripherals is reduced from its nominal 20ms duration. If this bit is '0b', the ARC reset is stretched by the nominal delay.

**TEST\_XNOR\_EN**

If this bit is '1b', the Device-Under-Test XNOR chain test mode is enabled. If this bit is '0b', the XNOR mode is disabled. See [Section 13.8, "XNOR Chain," on page 263](#).

**Note:** Once the XNOR chain is enabled, a power cycle is required to re-establish JTAG operation or.

**TEST**

All TEST bits should be set to '0' when writing this register.

**13.7.5 JTAG Standard Port Discovery**

This section provides information that is not unique to ARC, but is part of the JTAG standard, and is provided for information.

The Discovery process will identify each JTAG controller that has an IDCODE register. Part of what needs to be derived is the length of the Instruction register in each of the JTAG ports. If this cannot be derived from the IDCODE values, or if some JTAG ports do not have an IDCODE register, then the missing lengths must be provided by other means.

In the Test-Logic-Reset state, a JTAG port is required to initialize its Instruction register to select the IDCODE Data register if present, or if it is not present, then to select the BYPASS Data register.

The IDCODE Data register:

- Must be exactly 32 bits in length
- Must have '1' in its first (least-significant) bit
- Must not have the pattern 000011111111 (FFh) in its first (least-significant) 12 bits.
- Will contain a completely definitive port identification, because 11 bits of it are a Manufacturer ID number assigned by the JEDEC standards organization.

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A BYPASS Data register access will initialize its 1-bit shift register to '0' at the Capture-DR state, effectively making the BYPASS register appear to be 1-bit read-only '0'.

Discovery, therefore, consists of the external JTAG host doing the following:

- Place the chain of JTAG controllers into the Test-Logic-Reset state.
- Do a Data register access, without an Instruction register access first.  
This Data access will shift in 8 bits of ones, followed by all zeroes for the duration of the discovery phase.
- While shifting, examine the data appearing on TDO for IDCODE values.  
A '0' indicates a JTAG port that has no IDCODE register. Collect only this bit, and note that the JTAG port exists. Start looking for an IDCODE value at the next bit.  
A '1' indicates that an IDCODE register is coming. Collect this bit and the next 31 bits to identify the JTAG port. If, however, the value seen is 00h0000FF, then this is guaranteed to be the value provided originally on TDI, and indicates the end of the chain.

## 13.8 XNOR Chain

### 13.8.1 Overview

The [XNOR Chain](#) test mode allows users to confirm that all MEC5035 pins are in contact with the motherboard during assembly and test operations. The [XNOR Chain](#) test mode is enabled and disabled through the JTAG interface, using bit [Test\\_XNOR\\_En](#) in JTAG [TEST REGISTER 4/Reset Register \(Dh\)](#).

An example of an [XNOR Chain](#) test structure is illustrated below in [Figure 13.1](#). When the [XNOR Chain](#) test mode is enabled all pins except for the [Excluded Pins](#) shown in [Section 13.8.2](#) are disconnected from their internal functions and forced as inputs to the [XNOR Chain](#). This allows a single input pin to toggle the [XNOR Chain](#) output if all other input pins are held high or low. The [XNOR Chain](#) output is the nRESET\_OUT pin.

The tests that are performed when the [XNOR Chain](#) test mode is enabled require the board-level test hardware to control the device pins and observe the results at the [XNOR Chain](#) output pin; e.g., as described in [Section 13.8.3, "Test Procedure,"](#) on page 264.

### 13.8.2 Excluded Pins

The following pins are [XNOR Chain Excluded Pins](#): POWER PLANE pins, VR\_CAP, nRESET\_OUT, XTAL1, XTAL2 and JTAG\_RST# (see [Section 3.4, "Pin Description,"](#) on page 40).

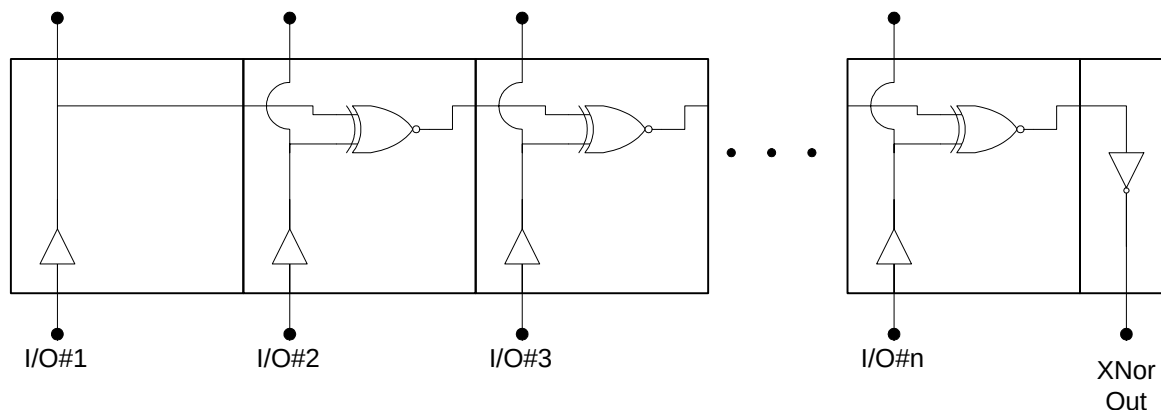


**Figure 13.1 XNOR Chain Test Structure**

### 13.8.3 Test Procedure

#### 13.8.3.1 Setup

1. Connect the VSS and AGND pins to ground.
2. Connect the VCC0, VCC1, and VCC2 pins to an unpowered 3.3V power source.
3. Connect an oscilloscope or voltmeter to the nRESET\_OUT pin.
4. All other pins should be tied to ground.

**Warning:** Ensure power supply is off during Setup.

#### 13.8.3.2 Testing

1. Turn on the 3.3V power source.
2. Enable the [XNOR Chain](#) through the JTAG interface ([Test\\_XNOR\\_En](#) in JTAG [TEST REGISTER 4/Reset Register \(Dh\)](#)). Note that at this point all inputs to the [XNOR Chain](#) are low and the output on the nRESET\_OUT pin is high (refer to the [Initial Configuration](#) row in [Table 13.10](#), "Toggling Inputs in Descending Pin Order").
3. Bring the highest numbered pin (N) high, where N is the number of pins to be tested as described in [Note 13.7](#). The output on the nRESET\_OUT pin should toggle (refer to [Step 1](#) in [Table 13.10](#)).
4. In descending pin order successively bring each input high. As shown in [Table 13.10](#) the nRESET\_OUT pin toggles after each step. Continue until all inputs are high. The output on the nRESET\_OUT pin is high (refer to the [Final Configuration](#) in [Table 13.10](#)).
5. The current state of the chip is now represented by the [Initial Configuration](#) row in [Table 13.11](#), "Toggling Inputs in Ascending Pin Order".
6. Each input should now be brought low, starting at pin one ([Step N+1](#)) and continuing in ascending pin order until all inputs are low. The output on the nRESET\_OUT pin is high (refer to the [Final Configuration](#) in [Table 13.11](#)).
7. Exit the [XNOR Chain](#) Test Mode by cycling VTR power.

**Table 13.10 Toggling Inputs in Descending Pin Order**

|                       | PIN NUMBER ( <a href="#">Note 13.7</a> ) |       |       |       |       |     |   | nRESET_OUT |
|-----------------------|------------------------------------------|-------|-------|-------|-------|-----|---|------------|
|                       | N                                        | N - 1 | N - 2 | N - 3 | N - 4 | ... | 1 |            |
| Initial Configuration | L                                        | L     | L     | L     | L     | L   | L | H          |
| Step 1                | H                                        | L     | L     | L     | L     | L   | L | L          |
| Step 2                | H                                        | H     | L     | L     | L     | L   | L | H          |
| Step 3                | H                                        | H     | H     | L     | L     | L   | L | L          |
| Step 4                | H                                        | H     | H     | H     | L     | L   | L | H          |
| Step 5                | H                                        | H     | H     | H     | H     | L   | L | L          |
| ...                   | H                                        | H     | H     | H     | H     | ... | L | ...        |
| Step N-1              | H                                        | H     | H     | H     | H     | H   | L | L          |
| Final Configuration   | H                                        | H     | H     | H     | H     | H   | H | H          |

**Table 13.11 Toggling Inputs in Ascending Pin Order**

|                       | PIN NUMBER (Note 13.7) |   |   |   |   |     |   | nRESET_OUT |
|-----------------------|------------------------|---|---|---|---|-----|---|------------|
|                       | 1                      | 2 | 3 | 4 | 5 | ... | N |            |
| Initial Configuration | H                      | H | H | H | H | H   | H | H          |
|                       |                        |   |   |   |   |     |   |            |
| Step N+1              | L                      | H | H | H | H | H   | H | L          |
| Step N+2              | L                      | L | H | H | H | H   | H | H          |
| Step N+3              | L                      | L | L | H | H | H   | H | L          |
| Step N+4              | L                      | L | L | L | H | H   | H | H          |
| Step N+5              | L                      | L | L | L | L | H   | H | L          |
| ...                   | L                      | L | L | L | L | ... | H | ...        |
| Step N+(N-1)          | L                      | L | L | L | L | L   | H | L          |
| Final Configuration   | L                      | L | L | L | L | L   | L | H          |

**Note 13.7** pin numbers in these tables represent the number of pins to be tested and do not include the pins listed in [Section 13.8.2, "Excluded Pins," on page 263](#)

## 13.9 JTAG and XNOR Revision History

| MEC5035 pin | Functional Signal Name                    | Test Signal Name   | Test Signal Description                                                                                                                                                                                                                         |
|-------------|-------------------------------------------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 72          | GPIO106/nRESET_OUT                        | XNOR_OUT           | XNOR chain out.                                                                                                                                                                                                                                 |
| 71          | GPIO105/UART_RX                           | INPUT_DRIVE        | Input drive. Most pins are auto configured as outputs in this test mode, and these outputs follow this pins input value. In pullup/pulldown mode, the pins are tristated and their respective pull-ups and pull-downs are enabled via this pin. |
| 2           | GPIO001                                   | TEST_CLKEN_OUT     | Test clock enable output. Internal clock enable signals viewable on this pin.                                                                                                                                                                   |
| 3           | GPIO002                                   | TEST_CLK_OUT       | Test clock output. Internal clocks viewable on this pin.                                                                                                                                                                                        |
| 5           | GPIO003/I2C1A_DATA                        | TEST_CLK_REQ_OUT   | Test clock required output. Internal logical-OR of the sleep signaling                                                                                                                                                                          |
| 73          | GPIO107                                   | TEST_RST_OUT       | Test reset output. Reflects the state of selected internal resets/PORs.                                                                                                                                                                         |
| 89          | GPIO124/GPTP-OUT5                         | SCAN_CLK1/ARC_CLK  | test_arc_clk/scan clock #1                                                                                                                                                                                                                      |
| 117         | GPIO160/32KHZ_OUT                         | SCAN_CLK2/KHZ32    | test_kh32_clk/scan clock #2 can be used to bypass the internal 32 KHz clock                                                                                                                                                                     |
| 58          | PCI_CLK                                   | SCAN_CLK3/PCI_CLK  | lpc_clk/scan clock #3 Normally PCI clock                                                                                                                                                                                                        |
| 91          | GPIO126                                   | SCAN_CLK4/MASTER   | test_master_clk/scan clock #4 can be used to bypass the internal master clock                                                                                                                                                                   |
| 90          | GPIO125/GPTP-IN5                          | SCAN_CLK5/SOURCE   | test_source_clk/scan clock #5 can be used to bypass the internal source clock, from the ring oscillator<br>NOTE: This clock is the source clock for the master clock and arc clock and thus can be used to drive these others                   |
| 105         | GPIO147 /I2C1J_DATA /I2C2C_DATA /JTAG_CLK | SCAN_CLK6/JTAG_TCK | test_tclk_out/scan clock #6 normally JTAG clock                                                                                                                                                                                                 |
| 16          | GPIO016/GPTP-IN8                          | TEST_SI1           | Scan Chain #1 SI                                                                                                                                                                                                                                |
| 17          | GPIO017/GPTP-OUT8                         | TEST_SO1           | Scan Chain #1 SO                                                                                                                                                                                                                                |
| 14          | GPIO014/GPTP-IN7                          | TEST_SI2           | Scan Chain #2 SI                                                                                                                                                                                                                                |
| 15          | GPIO015/GPTP-OUT7                         | TEST_SO2           | Scan Chain #2 SO                                                                                                                                                                                                                                |
| 28          | GPIO026/GPTP-IN1                          | TEST_SI3           | Scan Chain #3 SI                                                                                                                                                                                                                                |
| 29          | GPIO027/GPTP-OUT1                         | TEST_SO3           | Scan Chain #3 SO                                                                                                                                                                                                                                |
| 30          | GPIO030/GPTP-IN2                          | TEST_SI4           | Scan Chain #4 SI                                                                                                                                                                                                                                |
| 31          | GPIO031/GPTP-OUT2                         | TEST_SO4           | Scan Chain #4 SO                                                                                                                                                                                                                                |
| 32          | GPIO032/GPTP-IN3                          | TEST_SI5           | Scan Chain #5 SI                                                                                                                                                                                                                                |
| 33          | GPIO040/GPTP-OUT3                         | TEST_SO5           | Scan Chain #5 SO                                                                                                                                                                                                                                |
| 41          | GPIO050/FAN_TACH1                         | TEST_SI6           | Scan Chain #6 SI                                                                                                                                                                                                                                |
| 45          | GPIO053/PWM0                              | TEST_SO6           | Scan Chain #6 SO                                                                                                                                                                                                                                |
| 42          | GPIO051/FAN_TACH2                         | TEST_SI7           | Scan Chain #7 SI                                                                                                                                                                                                                                |
| 46          | GPIO054/PWM1                              | TEST_SO7           | Scan Chain #7 SO                                                                                                                                                                                                                                |
| 43          | GPIO052/FAN_TACH3                         | TEST_SI8           | Scan Chain #8 SI                                                                                                                                                                                                                                |
| 47          | GPIO055/PWM2                              | TEST_SO8           | Scan Chain #8 SO                                                                                                                                                                                                                                |
| 109         | GPIO152/GPTP-OUT4                         | TEST_SE            | Scan Shift Enable (TEST_SE)                                                                                                                                                                                                                     |
| 108         | GPIO151/GPTP-IN4                          | SCAN_RESET_N       | Scan Reset. Asynchronous active-low                                                                                                                                                                                                             |



## Product Customer Specification-ODM

This revision history shows the changes made to this chapter.

**Table 13.12 JTAG and XNOR Chapter Revision History**

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History," on page 539.</a> |              |            |                                                                                                                                                                                                                                                                                                                                             |                                                                                                                                                                                                                                                           |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE       | SECTION/FIGURE/ENTRY                                                                                                                                                                                                                                                                                                                        | CORRECTION                                                                                                                                                                                                                                                |
| 1.                                                                                                                                                                                                                                          | 0.4          | 04/30/2007 | <a href="#">Section 13.3, "JTAG Port Signal Interface Description," on page 250</a><br>Global                                                                                                                                                                                                                                               | Added reference to Pin Chapter<br>Changed names to pin names.                                                                                                                                                                                             |
| 2.                                                                                                                                                                                                                                          | 0.4          | 5/11/2007  | <a href="#">Section 13.2, "ARC JTAG System Block Diagram," on page 248</a><br><a href="#">Figure 13.1 Block Diagram of JTAG System on page 249</a>                                                                                                                                                                                          | Test Mode Register are relocated inside the                                                                                                                                                                                                               |
| 3.                                                                                                                                                                                                                                          | 0.4          | 5/11/2007  | <a href="#">TEST on page 262</a><br><a href="#">TEST on page 262</a>                                                                                                                                                                                                                                                                        | Added write '0' to test bits for customer                                                                                                                                                                                                                 |
| 4.                                                                                                                                                                                                                                          | 0.5          | 05/17/2007 | <a href="#">Section 13.2, "ARC JTAG System Block Diagram," on page 248 &amp; Figure 13.1 Block Diagram of JTAG System on page 249</a><br><br><a href="#">Section 13.4, "Power, Clocks and Reset," on page 250</a><br><br><a href="#">Section 13.4.3, "Reset," on page 250</a><br><br><a href="#">Section 13.7, "Registers," on page 255</a> | Change block diagram & description to match implementation.<br><br>Added xref's to <a href="#">Section 34.10, "JTAG Interface Timing," on page 537</a><br><br>Clarified Reset in block<br><br>Changed format of registers to be similar to reset of spec. |
| 5.                                                                                                                                                                                                                                          | 0.6          | 06/13/2007 | <a href="#">VTR POR &amp; VCC POR bits in the RESET TEST Register on page 261</a><br><br><a href="#">Figure 13.1 &amp; Section 13.2</a>                                                                                                                                                                                                     | <a href="#">VTR POR &amp; VCC POR</a> bits are active low.<br><br><a href="#">JTAG Debug Data Registers</a> can be disabled to protect the flash boot block. xref                                                                                         |

## Chapter 14 ARC 625D Embedded Controller

### 14.1 General Description

This chapter contains a description of the Embedded Controller used in the MEC5035.

The Embedded Controller on the MEC5035 is an ARC 625D Processor by ARC International. The ARC625D is a full-featured 32-bit embedded processor. Its features include:

- 5-stage instruction pipeline with single-cycle instruction execution
- Static branch prediction
- 32-bit data, instruction and address buses
- 16- and 32-bit instructions, with no overhead for switching between 16- and 32-bits
- 32 32-bit general purpose registers
- Scoreboarded data memory pipeline to reduce data stalls
- Debug features
  - Debug host can access all registers and CPU memory, with a JTAG interface to host tools
  - Multiple action points for real-time instruction and data breakpoints
- Industry standard AHB system interface
- Power saving features
  - Sleep mode via software instruction
  - Clock gating
- Two highly configurable action points for debugging

The ARC625D is highly configurable. The configuration used in the MEC5035 incorporates:

- 192KB plus 2KB single cycle Embedded Flash Closely Coupled instruction memory
- 4KB Single Cycle 32-bit wide dual-ported SRAM, accessible as both Closely Coupled Data Memory and Instruction Memory
- Interrupt controller with 32 interrupts
- Normalize instruction, which can find leading ones and zeros in a word
- Multiply instruction, which completes a 32x32 multiply in 10 cycles
- Two full-featured [Actionpoints \(Dedicated Breakpoint Blocks\)](#), which can trigger breakpoints on both instruction accesses and data access

For details on the architecture of the ARC625D processor, see ARC International's *ARCompact™ Instruction Set Architecture Programmer's Reference*, March 2005.

## 14.2 Block Diagram

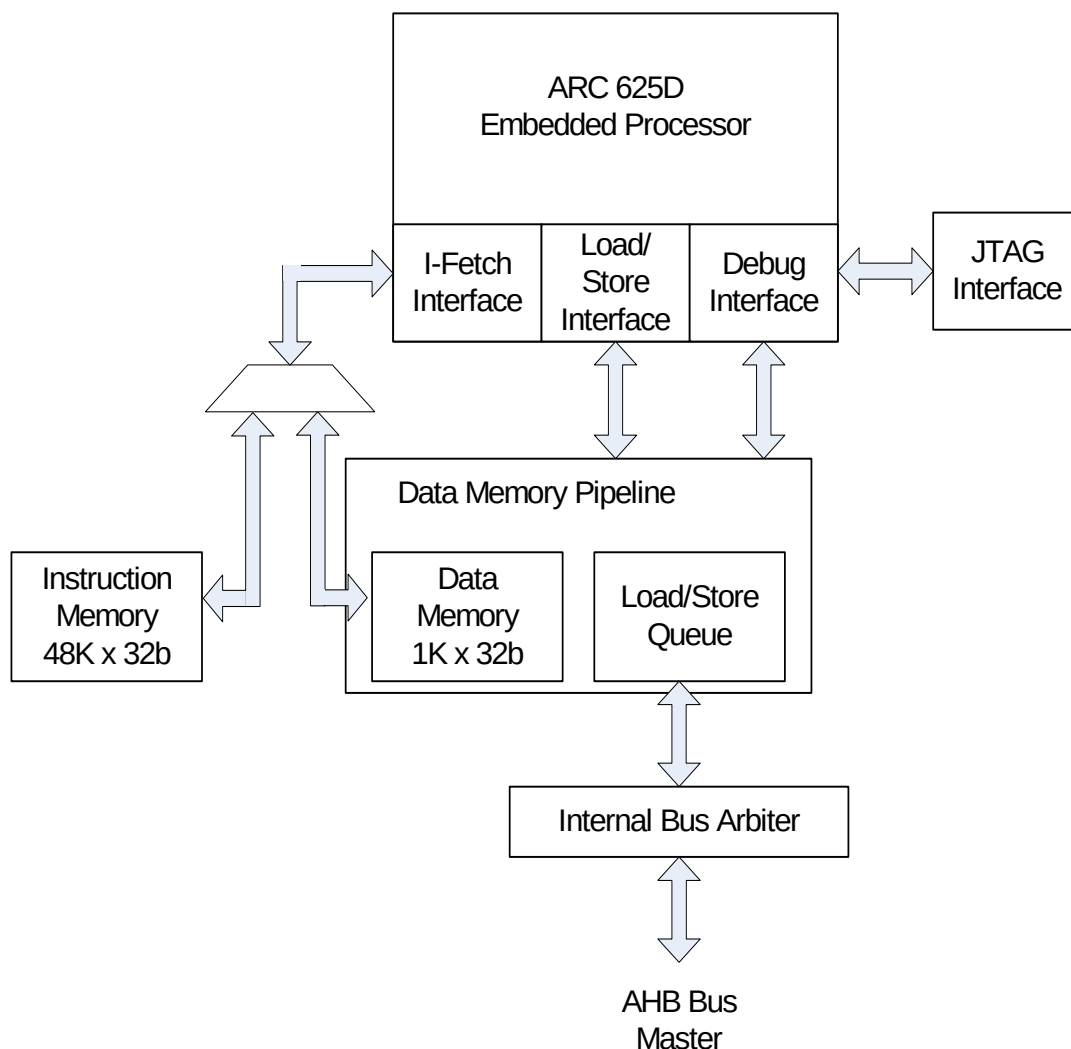


Figure 14.1 ARC Block Diagram

## 14.3 EC Clocking

The EC can be configured to clock at rates ranging from 32MHz to 250KHz. The highest speed (32MHz) cannot be used if the EC makes any reference, either instruction or data, to the Embedded Flash memory. The 32MHz rate can be used if instructions are solely in the SRAM memory and data references are to either the SRAM or registers in the AHB address space. The highest clock rate that can be used when accessing the Flash is 21.5MHz. EC clock rates are set via the [EC Clock Divider Register](#), described on [page 106](#). See [Chapter 4, "Power, Clocks and Resets,"](#) on [page 74](#).

Sleep mode via software instruction initiates power saving via Clock gating and ultimately by stopping [64.52 MHz Ring Oscillator](#). See [Section 4.4.7, "Power Management Interface,"](#) on [page 84](#) for detailed description of Block Clocking Model and power management.

## 14.4 EC Memory Map

The ARC processor executes code out of the [EC Instruction Memory](#). This instruction memory is an ARC ICCM (Instruction Closely-Coupled Memory) and each 32-bit word can be accessed in one



processor cycle. Data references can come from either the [EC Data Memory](#) or from addresses located in the [AHB Address Space](#). The [EC Data Memory](#) is an ARC DCCM (Data Closely-Coupled Memory), so each 32-bit word can read or written in one cycle.

See [Section 7.3.1, "ARC Address Space," on page 164](#) for further details on the ARC address space.

### 14.4.1 EC Data Memory

The EC has a 4KB Closely Coupled Data memory, implemented with static RAM and organized 1K x 32 bits. Loads and stores to this memory are completed in one cycle. The base address of the memory is 80\_0000h in the EC address space and extends to location 80\_0FFFh. The EC cannot execute instructions from this address range.

The 4KB Data memory also appears in the instruction space in the address range 6\_0000h through 6\_0FFF as described in [Section 14.4.2, "EC Instruction Memory"](#).

### 14.4.2 EC Instruction Memory

The primary instruction memory for the EC is a 48K x 32 bit Embedded Flash memory, located at locations 00\_0000h through 02\_FFFF in the EC address space. There is also an additional 512 x 32b block of Flash memory, called the Info block, located at addresses 04\_0000h through 04\_0FFFh. Instruction fetches to these two blocks complete in one cycle. The ARC can access locations in the Embedded Flash Memory through load and store instructions, with one additional processor cycle penalty.

The 4KB Data memory also appears in the instruction space in the address range 6\_0000h through 6\_0FFF. The memory is dual-ported, so instruction fetches from this space can occur in parallel with data loads and stores, without wait states for either instruction fetch or data reference. If the Embedded Flash memory is configured to be only accessible via the register interface (see [Section 14.7, "EC Registers," on page 272](#)), the EC can execute instructions out of the SRAM. For example, the EC could run code that programs the Flash while the Embedded Flash memory is set for the register interface.

[RAM\\_Select](#) in the [AHB SRAM Configuration Register](#) can be used to disable instruction access to the SRAM. If instruction access to the SRAM is not needed, disabling it saves power.

Instruction fetches in the range of 00\_0000h through 7F\_FFFFh do not incur bus errors. Any instruction fetch to non-existent memory will return FFFF\_FFFFh.

## 14.5 EC AHB Bus Interface

The ARC Embedded Controller has a single AHB Bus Master interface; see [Section 7.4, "AHB Buses," on page 169](#). The ARC can have at most one access pending on the AHB at one time. The ARC can perform 8-bit, 16-bit and 32-bit loads and stores on the AHB. Instruction fetches over the AHB can take the form of either a 32-bit word load or a 4-word (128-bit) cache line fill.

Possible AHB bus errors are described in [Section 7.4.3, "AHB Bus Errors," on page 170](#). The ARC processor responds to a bus error with Memory Error exception. The first address that caused a memory error is recorded in the [AHB Error Address Register](#). Because ARC exceptions are imprecise, and since several bus errors can occur between the time a bus error address is recorded and the time the ARC processes the exception, it is not always possible to determine which instruction caused the bus error.

## 14.6 Actionpoints (Dedicated Breakpoint Blocks)

Actionpoints are defined in the ARC 600 Ancillary Components Manual, Chapter 4. They are dedicated hardware blocks that provide an alternative source of breakpoints when the debugger cannot write to memory (e.g., the code being debugged is in ROM). They also provide the ability to break on memory or Aux register accesses.



## Product Customer Specification-ODM

The primary justification for including Actionpoints in the design is to provide breakpointing for code in ROM, while code is running at full speed (as opposed to being single-stepped). The debugger by default prefers to write Breakpoint instructions (BRK\_S: 7FFFh) into memory in order to perform breakpoints at specified PC values. It will instead use actionpoints if:

- The memory area is declared as ROM,  
or
- The flag "-off=prefer\_soft\_bp" is given to the debugger.

Actionpoints are controlled by a dedicated set of Aux Registers, in the range 220h - 237h, organized as 3 registers per actionpoint. These are:

- AMV: A 32-bit value (Address or sometimes Data). This register supplies the initial trigger value, as masked by the AMM register. Upon triggering, it is over-written by hardware with the exact value seen.
- AMM: A 32-bit mask applied to the AMV register, making any desired bits don't-cares.
- AC: Control register, selecting modes

The status of all actionpoints is visible in the Aux Register DEBUG, at 5h.

The MEC5035 incorporates two full-featured ARC Actionpoints, Actionpoint 0 and Actionpoint 1.

### 14.6.0.1 Actionpoint Configurations

Actionpoints may configured (at processor HW build) to be one of two configurations, Minimal or Full.

Minimal actionpoints may be configured to do the following:

- Trigger on an access by address and access type (Instruction, Bus access, or Aux Register)
- Instruction breakpoints trigger on execution at the address, not at the fetch itself
- Act by either Halt (debugger acts) or SW Interrupt (target SW acts)
- Qualify between Reads and Writes (or both)
- Qualify by masking bits of the address
- Invert Condition (Trigger if No Match)
- Gang actionpoints in pairs or quads: both/all must match

Full actionpoints add the following capabilities:

- Match on opcode for instruction fetches
- Match on data value for data read/write in Aux registers or memory
- Two 34-bit inputs from arbitrary sources (per actionpoint)

### 14.6.0.2 Significant Limitations

Address ranges may degrade performance. Because address matching is bit-masked, it may take multiple actionpoints to refine an address range. Even then, the final range is liable to be too big. The debugger allows a range to be too big, and continues from the breakpoint if the resulting trigger was not in the desired range. Note that this means that the program was being halted at undesired / unexpected times, and so is not running at full speed. A reliable way to avoid this is to specify a range only as a power of 2 in size, aligned on a boundary that is also a power of 2, the same or larger than the range.

There is no way to trigger on both the value and the address of a bus read (Memory, I/O), because the data and the address are not present simultaneously. An Aux register access, however, can trigger on data when either read or written. Do not try to enable Read and Write in the same actionpoint, because that will select only the Write data bus to monitor.

### 14.6.0.3 Debugger Support

As of version 7.4, the debugger supports:

1. Break on Instruction fetch by address  
Actionpoint is used if ROM detected or “-off=prefer\_soft\_bp” argument is specified
2. Break on Memory Space data accesses  
Read/Write or Both  
Address and Mask  
Range, if size is power of two and target aligned to a power of two (requires 2 Minimal actionpoints, paired)  
Value and Mask (requires 2 Minimal actionpoints, paired)  
Value and Range (requires 4 Full actionpoints, quadded)
3. Aux Register accesses  
Read/Write or Both

## 14.7 EC Registers

**Table 14.1 AHB SRAM Configuration Register**

|               |          |    |    |    |            |    |    |                     |  |
|---------------|----------|----|----|----|------------|----|----|---------------------|--|
| HOST OFFSET   | N/A      |    |    |    | N/A        |    |    | HOST SIZE           |  |
| EC ADDRESS    | F0_FC00h |    |    |    | 32-bit     |    |    | EC SIZE             |  |
| POWER         | VTR      |    |    |    | 0000_0000h |    |    | nSYS_RST<br>DEFAULT |  |
| BUS           | EC SPB   |    |    |    |            |    |    |                     |  |
| BYTE[3-1] BIT | D7       | D6 | D5 | D4 | D3         | D2 | D1 | D0                  |  |
| HOST TYPE     | -        | -  | -  | -  | -          | -  | -  | -                   |  |
| EC TYPE       | R        | R  | R  | R  | R          | R  | R  | R                   |  |
| BIT NAME      | Reserved |    |    |    |            |    |    |                     |  |
| BYTE0 BIT     | D7       | D6 | D5 | D4 | D3         | D2 | D1 | D0                  |  |
| HOST TYPE     | -        | -  | -  | -  | -          | -  | -  | -                   |  |
| EC TYPE       | R        | R  | R  | R  | R          | R  | R  | R/W                 |  |
| BIT NAME      | Reserved |    |    |    |            |    |    | RAM_Select          |  |

#### RAM\_SELECT

When this bit is clear (the default case), the 4KB on-chip SRAM that is part of the EC can only be accessed by loads and stores starting at address 80\_0000h. The EC can read and write data in the SRAM at addresses starting at 80\_0000h but cannot directly execute instructions.



## Product Customer Specification-ODM

When this bit is set, the 4KB SRAM is configured to be simultaneously accessible in the address range address 6\_0000h through 6\_0FFFh. The EC can execute directly out of the SRAM. The EC can still read and write data in the SRAM, with no time penalty per load or store.

Table 14.2 AHB Error Address Register

|             |                |      |      |            |      |      |                     |      |
|-------------|----------------|------|------|------------|------|------|---------------------|------|
| HOST OFFSET | N/A            |      |      | N/A        |      |      | HOST SIZE           |      |
| EC ADDRESS  | F0_FC04h       |      |      | 32-bit     |      |      | EC SIZE             |      |
| POWER       | VTR            |      |      | 0000_0000h |      |      | nSYS_RST<br>DEFAULT |      |
| BUS         | EC SPB         |      |      |            |      |      |                     |      |
| BYTE3 BIT   | D31            | D30  | D29  | D28        | D27  | D26  | D25                 | D24  |
| HOST TYPE   | -              | -    | -    | -          | -    | -    | -                   | -    |
| EC TYPE     | R              | R    | R    | R          | R    | R    | R                   | R    |
| BIT NAME    | Reserved       |      |      |            |      |      |                     |      |
| BYTE2 BIT   | D23            | D22  | D21  | D20        | D19  | D18  | D17                 | D16  |
| HOST TYPE   | -              | -    | -    | -          | -    | -    | -                   | -    |
| EC TYPE     | R/WC           | R/WC | R/WC | R/WC       | R/WC | R/WC | R/WC                | R/WC |
| BIT NAME    | EC_Addr[23:16] |      |      |            |      |      |                     |      |
| BYTE1 BIT   | D15            | D14  | D13  | D12        | D11  | D10  | D9                  | D8   |
| HOST TYPE   | -              | -    | -    | -          | -    | -    | -                   | -    |
| EC TYPE     | R/WC           | R/WC | R/WC | R/WC       | R/WC | R/WC | R/WC                | R/WC |
| BIT NAME    | EC_Addr[15:8]  |      |      |            |      |      |                     |      |
| BYTE0 BIT   | D7             | D6   | D5   | D4         | D3   | D2   | D1                  | D0   |
| HOST TYPE   | -              | -    | -    | -          | -    | -    | -                   | -    |
| EC TYPE     | R/WC           | R/WC | R/WC | R/WC       | R/WC | R/WC | R/WC                | R/WC |
| BIT NAME    | EC_Addr[7:0]   |      |      |            |      |      |                     |      |

**EC\_ADDR[23:0]**

If an AHB bus error occurs as the result of an EC AHB bus access, the address that caused the error is held. Once an address is held, additional bus errors are ignored, so this register records the first AHB address that caused an AHB bus error. Any write to this register re-enables capturing AHB bus addresses.

## 14.8 ARC 625D Embedded Controller Revision History

This revision history shows the changes made to this chapter.

**Table 14.3** ARC 625D Embedded Controller Chapter Revision History

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History," on page 539.</a> |              |            |                                           |                                                                               |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------------|-------------------------------------------|-------------------------------------------------------------------------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE       | SECTION/FIGURE/ENTRY                      | CORRECTION                                                                    |
| 1.                                                                                                                                                                                                                                          | 0.4          | 04/23/2007 | <a href="#">EC_Addr[23:0] on page 273</a> | Bus error register only latches error cycles                                  |
| 2.                                                                                                                                                                                                                                          | 0.4          | 05/11/2007 | Features <a href="#">page 268</a>         | 192KB plus 2KB single cycle Embedded Flash Closely Coupled instruction memory |
| 3.                                                                                                                                                                                                                                          |              |            |                                           |                                                                               |
| 4.                                                                                                                                                                                                                                          |              |            |                                           |                                                                               |



## Chapter 15 Embedded Flash Subsystem

### 15.1 General Description

The MEC5035 Embedded Flash Subsystem includes a 192KB embedded Flash memory. The memory appears in the system AHB address space and can store both instructions and data. The Flash memory can be programmed by the Embedded Controller, by the Host via LPC, and by ATE via JTAG.

### 15.2 Block Diagram

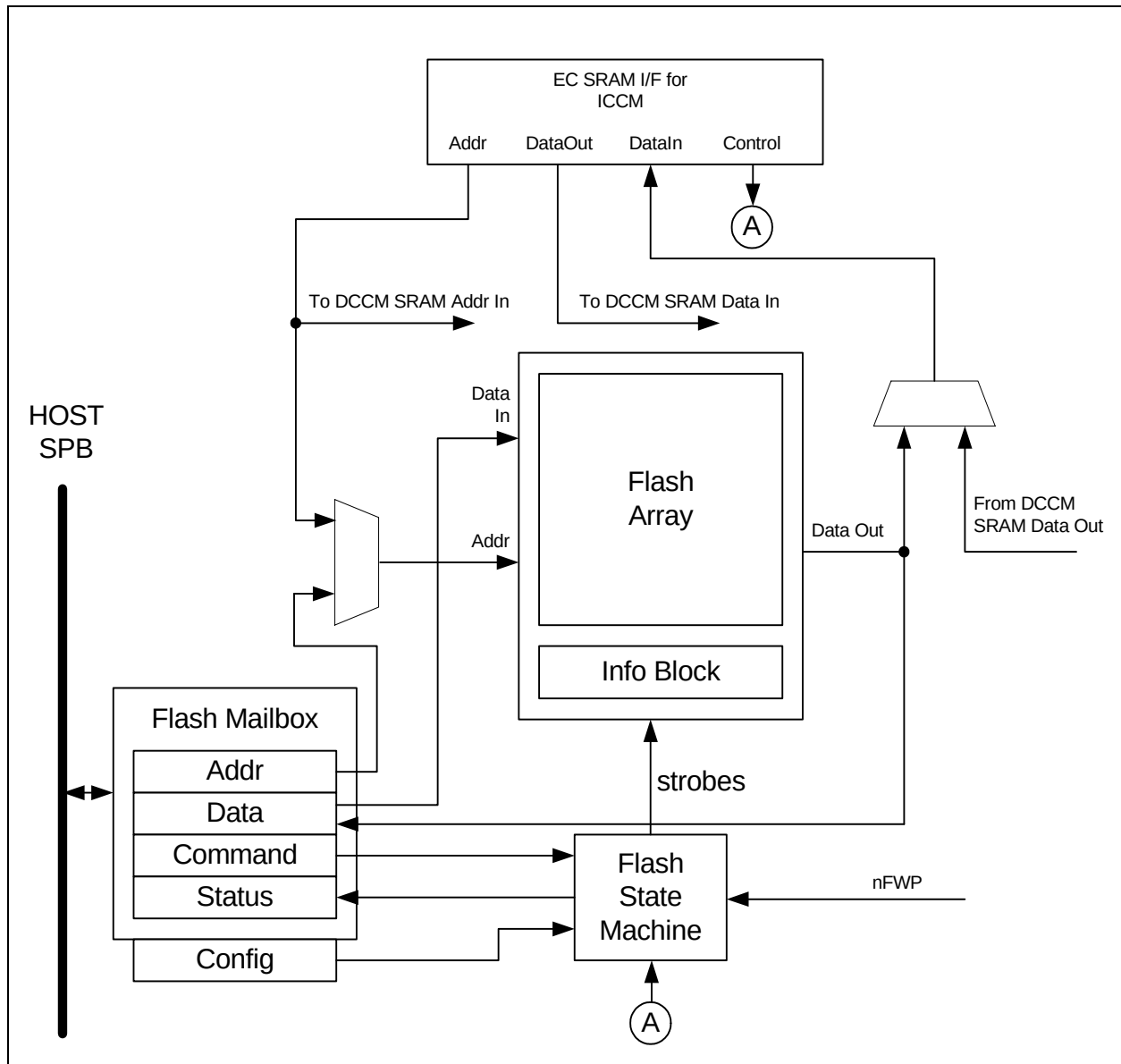


Figure 15.1 Embedded Flash Block Diagram



## 15.3 Power, Clocks and Reset

### 15.3.1 Power Domain

This block is powered by the VTR Power Supply.

See [Section 4.5, "Power Configuration," on page 96](#) for details on power domains.

### 15.3.2 Clocks

This block uses the [LPC Bus Clock](#), the 64.52MHz [MCLK](#) and the 100KHz [MCLK\\_DIV640\\_EN](#). [LPC Bus Clock](#) is used when reading and writing the [Embedded Flash Subsystem](#) control registers. All Flash signal timing is derived from the [MCLK](#). The 100KHz [MCLK\\_DIV640\\_EN](#) is used to determine the multiple-millisecond times required for [Erase Mode](#).

The Embedded Flash controller will keep the internal ring oscillator operating as long as the controller is not in the Standby state. This permits the controller to complete any program or erase operation even though the Embedded Controller may be in its sleep state.

See [Section 4.4, "Clock Generator," on page 77](#) for details on clocks.

#### 15.3.2.1 Clock Idle

The Embedded Flash controller will keep the internal ring oscillator operating as long as the controller is not in the Standby state. This permits the controller to complete any program or erase operation even though the Embedded Controller may be in its sleep state. See [APPLICATION NOTE: on page 289](#).

### 15.3.3 Reset

This block is reset by [nSYS\\_RST](#). Following a reset, all registers are set to their default values, and the internal state machines are reset to the standby state.

See [Section 4.6, "Reset Interface," on page 99](#) for details on reset.

The JTAG interface registers referenced in this chapter have an asynchronous reset. See [Note 13.2 on page 251](#).

### 15.3.4 Tracking Flash Program or Erase Activity

When the [Embedded Flash Command Register](#) is placed in [Program Mode](#) or [Erase Mode](#), the [FLASH](#) bit is asserted in the [Power-Fail and Reset Status Register](#). The [FLASH](#) bit in the [Power-Fail and Reset Status Register](#) is sticky, VBAT powered and reset by [VBAT\\_POR](#).

**APPLICATION NOTE:** The purpose of the [FLASH](#) bit in the [Power-Fail and Reset Status Register](#) is to provide the EC with status. Once this bit is asserted by hardware, EC firmware should clear the [FLASH](#) bit as soon as possible after every [Program Mode](#) or [Erase Mode](#) operation. EC software can detect unexpected events which may indicate flash corruption. For example, VTR POR, VCC POR, LRESET#, and VCC\_PWRGD transitions, as well as, completion of host flash erase or programming are example events when firmware should examine & clear the [FLASH](#) bit in the [Power-Fail and Reset Status Register](#) can be useful.

If a reset occurs, the software reset handler can examine the [FLASH](#) bit to determine if the Flash memory might be corrupted. Corruption can occur if Flash programming or erasure is interrupted by a reset.

If VCC power is removed, or if LRESET# is asserted, the LPC interface becomes inactive and the Embedded Flash controller must ensure that the flash subsystem is in a consistent state. When the



LPC bus is inoperative the EC should have full access to the Embedded Flash. [Table 15.1, "VCC PWRGD and LRESET# Behavior"](#) describes the different possible states and the response.

**Table 15.1 VCC PWRGD and LRESET# Behavior**

| Embedded Flash Configuration Register | Embedded Flash Command Register |              | ACTION ON LRESET# ASSERTED OR VCC PWRGD DE-ASSERTED                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|---------------------------------------|---------------------------------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Host_Ctl                              | Reg_Ctl                         | Flash_Mode   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| X                                     | 0                               | X            | No action (see <a href="#">Note 15.2</a> )                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 0                                     | 1                               | X            | No action (see <a href="#">Note 15.2</a> )                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 1                                     | 1                               | Standby Mode | <ul style="list-style-type: none"> <li>Reg_Ctl_En, Reg_Ctl and Host_Ctl are set to '0b'.</li> <li>EC_Int in <a href="#">Embedded Flash Command Register</a> is set to '1b'.</li> <li>The Embedded Flash is set to the <a href="#">Instruction Memory Interface</a> and a wakeup interrupt is sent to the EC.</li> </ul>                                                                                                                                                                                                                                                                 |
| 1                                     | 1                               | Read Mode    | <ul style="list-style-type: none"> <li>Any read of the Embedded Flash array in progress is completed.</li> <li>All strobes to the Embedded Flash array are set to '0b'.</li> <li>Reg_Ctl_En, Reg_Ctl and Host_Ctl are set to '0b'. The Program Mode is set to Standby.</li> <li>EC_Int in <a href="#">Embedded Flash Command Register</a> is set to '1b'.</li> <li>The Embedded Flash is set to the <a href="#">Instruction Memory Interface</a> and a wakeup interrupt is sent to the EC.</li> </ul>                                                                                   |
| 1                                     | 1                               | Program Mode | <ul style="list-style-type: none"> <li>Any word currently being programmed to the Embedded Flash array in progress is completed.</li> <li>The Program Mode epilogue sequence is issued.</li> <li>All strobes to the Embedded Flash array are set to '0b'.</li> <li>Reg_Ctl_En, Reg_Ctl and Host_Ctl are set to '0b'. The Program Mode is set to Standby.</li> <li>EC_Int in <a href="#">Embedded Flash Command Register</a> is set to '1b'.</li> <li>The Embedded Flash is set to the <a href="#">Instruction Memory Interface</a> and a wakeup interrupt is sent to the EC.</li> </ul> |

**Table 15.1 VCC PWRGD and LRESET# Behavior**

| Embedded Flash Configuration Register | Embedded Flash Command Register |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|---------------------------------------|---------------------------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1                                     | 1                               | Erase Mode | <ul style="list-style-type: none"> <li>■ The erase sequence is completed.</li> <li>■ All strobes to the Embedded Flash array are set to '0b'.</li> <li>■ Reg_Ctl_En, Reg_Ctl and Host_Ctl are set to '0b'.</li> <li>■ EC_Int in <a href="#">Embedded Flash Command Register</a> is set to '1b'. The Program Mode is set to Standby.</li> <li>■ The Embedded Flash is set to the <a href="#">Instruction Memory Interface</a> and a wakeup interrupt is sent to the EC.</li> </ul> |

**Note 15.2** The assertion of LRESET# or the de-assertion of VCC PWRGD has no effect in this state; the EC can set or clear Reg\_Ctl\_En, Reg\_Ctl and Host\_Ctl and EC\_Int is not set.

**APPLICATION NOTE:** The [FLASH](#) bit in the [Power-Fail and Reset Status Register on page 116](#) is asserted autonomously and is sticky. Firmware should examine this bit after either VCC POR or LRESET# assertion.

## 15.4 Interrupts

The [Embedded Flash Subsystem](#) can generate interrupts to the EC for four events, three of which are reported in the three error bits in the [Embedded Flash Status Register](#): [Protect\\_Err](#), [CMD\\_Err](#), & [Busy\\_](#). The error bits are routed onto the [FLASH\\_PROTECT\\_ERR](#), [FLASH\\_CMD\\_ERR](#), [FLASH\\_BUSY\\_ERR](#) bits of the [IRQ15 Source Register on page 332](#).

In addition, asserting [EC\\_Int](#) in the [Embedded Flash Command Register](#) can be used to generate an interrupt to the EC. This bit are routed onto the [FLASH\\_EC\\_INT](#), bit of the [IRQ15 Source Register on page 332](#)

EC interrupts generated by the LRESET# and VCC PWRGD pin signals are utilized as part of algorithms described in [Section 15.10, "Instruction Memory Interface or the Register Interface will return FFFF\\_FFFFh. Once set, only a VTR POR \(nSYS\\_RSTVTR POR \(nSYS\\_RSTVTR POR \(nSYS\\_RSTVTR POR \(nSYS\\_RSTVTR POR \(nEC\\_RST timingProgramming the Embedded Flash Array," on page 288. The LRESET# pin signal sets the \[LRESET#\]\(#\) bit in the \[IRQ15 Source Register on page 332\]\(#\). The VCC PWRGD pin signal sets the GPIO057 bit interrupt in the \[IRQ10 Source Register on page 320\]\(#\).](#)

## 15.5 Flash Memory Array

The [Flash Memory Array](#) is a CMOS page-erasable, mass-erasable, word-programmable Flash memory that is partitioned into two memory blocks. The main memory block is organized as 49.152 x 32-bit words. The information block is organized as 512 x 32-bit words.

An erase operation in the [Flash Memory Array](#) sets the affected memory array bits to one, while program operations write zeros. To reprogram any '0' bit in a page to '1,' the page must be erased.

A page (2048 bytes) in the main Flash array is composed of eight adjacent rows of 256 bytes. The Info block consists of one page composed of eight adjacent rows. The page erase operation erases all bytes within a page. A mass erase function that can erase the entire main Flash array and optionally the Info block as well is also provided.

The Flash Memory Array erases and programs with a 1.8V core power supply; i.e. MEC5035 does not require an external VPP supply. To modify the contents of the [Flash Memory Array](#), VTR must be >3V before program or erase operations may begin. A summary of the MEC5035 [Flash Memory Array](#) features is shown below in [Table 15.2](#).

**Table 15.2 MEC5035 192K Flash Feature Summary**

| FEATURE            |                          | DESCRIPTION                                                                                                                                 |
|--------------------|--------------------------|---------------------------------------------------------------------------------------------------------------------------------------------|
| PROG/ERASE VOLTAGE |                          | 1.8V ± 10% (T <sub>J</sub> = 0×C to 125×C)                                                                                                  |
| READ VOLTAGE       |                          |                                                                                                                                             |
| BUS WIDTH          |                          | 32-bit                                                                                                                                      |
| ACCESS TIME        |                          | 35 ns                                                                                                                                       |
| MEMORY ARRANGEMENT | MAIN BLOCK               | 48k x 32 in 96 pages of 2048 bytes                                                                                                          |
|                    | INFO. BLOCK              | 512 x 32 in one page of 2048 bytes                                                                                                          |
| BOOT BLOCK         | SIZE                     | 4096 bytes                                                                                                                                  |
|                    | LOCATION                 | Bottom                                                                                                                                      |
| ERASE              | TYPES                    | Page/Mass (2048 bytes/page)                                                                                                                 |
|                    | Program/<br>Erase Cycles | 1,000 Cycles                                                                                                                                |
| PROGRAMMING        |                          | Per 32-bit word                                                                                                                             |
| INTERFACE          |                          | All Program and Erase Operations are Enabled via a Command Sequence Interface using the Embedded Flash <a href="#">Register Interface</a> . |

### 15.5.1 Flash Address Mapping

The Main Block of the [Flash Memory Array](#) is located at 00\_0000h in the EC address space. The 2KB Info block is located at 4\_0000h. All locations can be used for both program and data by the EC. See [Figure 7.2, "MEC5035 EC Memory Map" on page 166](#).

The control registers used for programming the Flash are part of the Embedded Flash Logical Device. They are located in AHB address space starting at location [FF\\_3800h](#). The contents of both the Main Block and the Info block can also be read using the control registers.

## 15.6 Instruction Memory Interface

When [Reg\\_Ctl](#) of the [Embedded Flash Command Register](#) is '0b', access to the Embedded Flash memory is through the Instruction Closely Coupled Memory interface of the EC. The registers in the [Register Interface](#) may be read or written, but no operations will be initiated on the Embedded Array. The Flash memory can be read with no wait states at the peak EC clock rate of 21.5MHz.

## 15.7 Register Interface

Each instance of the [Embedded Flash Subsystem](#) has its own Logical Device Number, and Base Address as indicated in [Table 15.3](#).

**Table 15.3 Embedded Flash Subsystem Base Address Table**

| Embedded Flash Subsystem INSTANCE | LDN FROM (Host Logical Devices on MEC5035) | AHB BASE ADDRESS |
|-----------------------------------|--------------------------------------------|------------------|
| Embedded Flash                    | Eh                                         | FF_3800h         |

Table 15.4, "Embedded Flash Subsystem Register Summary," on page 282 summarizes the registers allocated for the Embedded Flash Subsystem.

The Table 15.4 is a register summary for one instance of the Embedded Flash Subsystem. The LPC I/O address for each Run-Time Register is described below as an offset from its Base Address Register. Each EC address is indicated as an SPB Offset from its AHB base address.

Both the Host and the Embedded Controller can communicate with the Embedded Flash Subsystem through a set of registers located on the LPC SPB bus. The Host uses the two byte Flash Mailbox interface, while the EC can access the register interface described in Section 15.7.2, "EC Register Interface".

### 15.7.1 Flash Mailbox interface

The Flash Mailbox interface provides the Host with a Message Interface similar to the MailBox Register Interface (see Chapter 8). The Flash Mailbox interface port occupies two addresses in the Host I/O space: FL\_MBX\_INDEX Register & FL\_MBX\_DATA Register.

To access a Flash Mailbox register once the Flash Mailbox BAR has been initialized, write the Host Offset of the desired 8-bit register into the Flash Mailbox INDX register. The register can then be accessed by reading or writing the Flash Mailbox DATA register.

It consists of 16 index-addressable 8-bit registers. These registers correspond to the four 32-bit registers that are shared between the Host and the EC.

To access a Flash Mailbox register once the Flash Mailbox BAR has been initialized, write the Host Offset of the desired 8-bit register into the Flash Mailbox INDX register. The register can then be accessed by reading or writing the Flash Mailbox DATA register.

**Note 15.3** In this specification, Host access to registers in the Flash Mailbox through the Flash Mailbox Access Port are identified by the prefix INDX in OFFSET fields in the register tables in Section 15.11, "Detailed Description of Accessible Registers".

### 15.7.2 EC Register Interface

The following table summarizes the registers allocated for the Embedded Flash Subsystem. The offset field in the following table is the offset from the EC Base Address.

Table 15.4 Embedded Flash Subsystem Register Summary

|                                          | HOST I/O ACCESS               |               |              | EC INTERFACE  |            |                       |
|------------------------------------------|-------------------------------|---------------|--------------|---------------|------------|-----------------------|
| Flash Mailbox interface<br>REGISTER NAME | HOST I/O<br>INDEX             | SPB<br>OFFSET | HOST<br>TYPE | SPB<br>OFFSET | EC<br>TYPE | VTR POR<br>(nSYS_RST) |
| FL_MBX_INDEX<br>Register                 | 00h                           | 00h           | R/W          | 00h           | R/W        | 00h                   |
| FL_MBX_DATA<br>Register                  | 04h                           | 04h           | R/W          | 04h           | R/W        | 00h                   |
| REGISTER NAME                            | FLASH<br>MAILBOX<br>INDEX     |               | HOST<br>TYPE | SPB<br>OFFSET | EC<br>TYPE | VTR POR               |
| Embedded Flash Data<br>Register          | INDX 00h,<br>01h, 02h,<br>03h | -             | R/W          | 100h          | R/W        | 0000_0000h            |
| Embedded Flash<br>Address Register       | INDX 04h,<br>05h, 06h,        | -             | R/W          | 104h          | R/W        | 0000_0000h            |
| Embedded Flash<br>Command Register       | INDX 08h,<br>09h              | -             | R/W          | 108h          | R/W        | 0000_0000h            |
| Embedded Flash<br>Status Register        | INDX 0Ch,<br>0Dh              | -             | R            | 10Ch          | R          | 0000_0000h            |
| Embedded Flash<br>Configuration Register | N/A                           | -             | -            | 110h          | R/W        | 0000_0000h            |

### 15.7.3 Flash Address and Data Registers

The [Embedded Flash Data Register](#) and the [Embedded Flash Address Register](#) are each implemented as a two entry FIFO, as illustrated in [Figure 15.4, "Embedded Flash Controller Address and Data registers"](#). The figure is suggestive and does not represent the precise implementation. Writes are always directed to the Tail register of the FIFO and reads are always sourced from the Head register. Each of the two registers has an associated Valid bit (V in the figure). The Tail Valid bit is set when the full Tail register is written and cleared when the Tail register is copied into the Head register. The Head Valid bit of the [Embedded Flash Data Register](#) is cleared whenever the full Head register is read by the Host or EC, or when the Embedded Flash Controller completes a Program transaction. The Head Valid bit of the [Embedded Flash Address Register](#) is cleared whenever the Embedded Flash controller completes a Read, Program or Erase function. Reading the [Embedded Flash Address Register](#) by a Host or EC register read does not affect the Head Valid bit. If the Head Valid bit is cleared and the Tail Valid bit is set, the Tail register is copied into the Head register, the Tail Valid bit is cleared and the Head Valid bit is set. All Valid bits are cleared when [Flash\\_Mode](#) of the [Embedded Flash Command Register](#) is set to [Standby Mode](#).

The Embedded Flash controller uses byte 0 of the [Embedded Flash Address Register](#) and byte 3 of the [Embedded Flash Data Register](#) to determine when the full register has been read or written. Writing byte 0 of the [Embedded Flash Address Register](#) sets the Valid bit on the Tail of the Address FIFO, while writing byte 3 of the [Embedded Flash Data Register](#) sets the Valid bit for the Tail of the Data FIFO. Reading byte 3 of the [Embedded Flash Data Register](#) clears the Valid bit for the Head of the Data FIFO. As stated above, reading any byte of the [Embedded Flash Address Register](#) does not cause a change in the Head Valid bit.

When the Valid bits of both the Head and Tail of the [Embedded Flash Data Register](#) are set, [Data\\_Full](#) in the [Embedded Flash Status Register](#) is set. If either bit is cleared, [Data\\_Full](#) is cleared. When the

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Valid bits of both the Head and Tail of the [Embedded Flash Address Register](#) are set, [Address\\_Full](#) in the [Embedded Flash Status Register](#) is set. If either bit is cleared, [Address\\_Full](#) is cleared.

The requesting Master will be stalled while attempting to read the [Embedded Flash Data Register](#) if the Embedded Flash controller is Busy and in the process of reading data into the [Embedded Flash Data Register](#). This will result in at most one EC wait state. Because the Host cannot read the Flash registers faster than the controller can read from the Flash array, a Host Read access over the LPC bus will not have any added Wait SYNC cycles because the Flash controller is busy. In other cases, a Host or EC read of either the [Embedded Flash Data Register](#) or the [Embedded Flash Address Register](#) always returns the value in the Head register, whether the Valid bit is set or not.

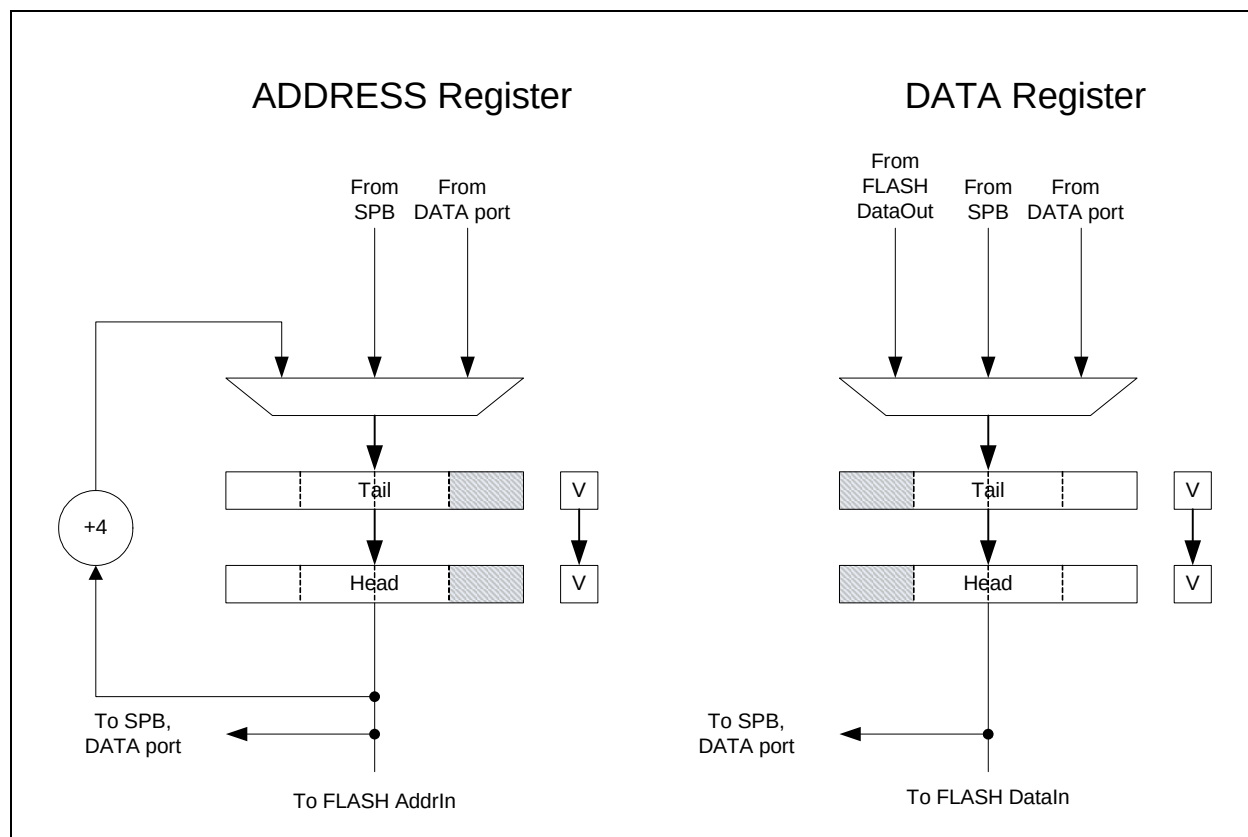


**Figure 15.4 Embedded Flash Controller Address and Data registers**

## 15.8 Embedded Flash Controller State Sequencing

The Embedded Flash controller proper timing on all strobe signals of the Embedded Flash array. [Figure 15.5, "Embedded Flash Controller State Diagram"](#) illustrates the primary state transitions for the controller.

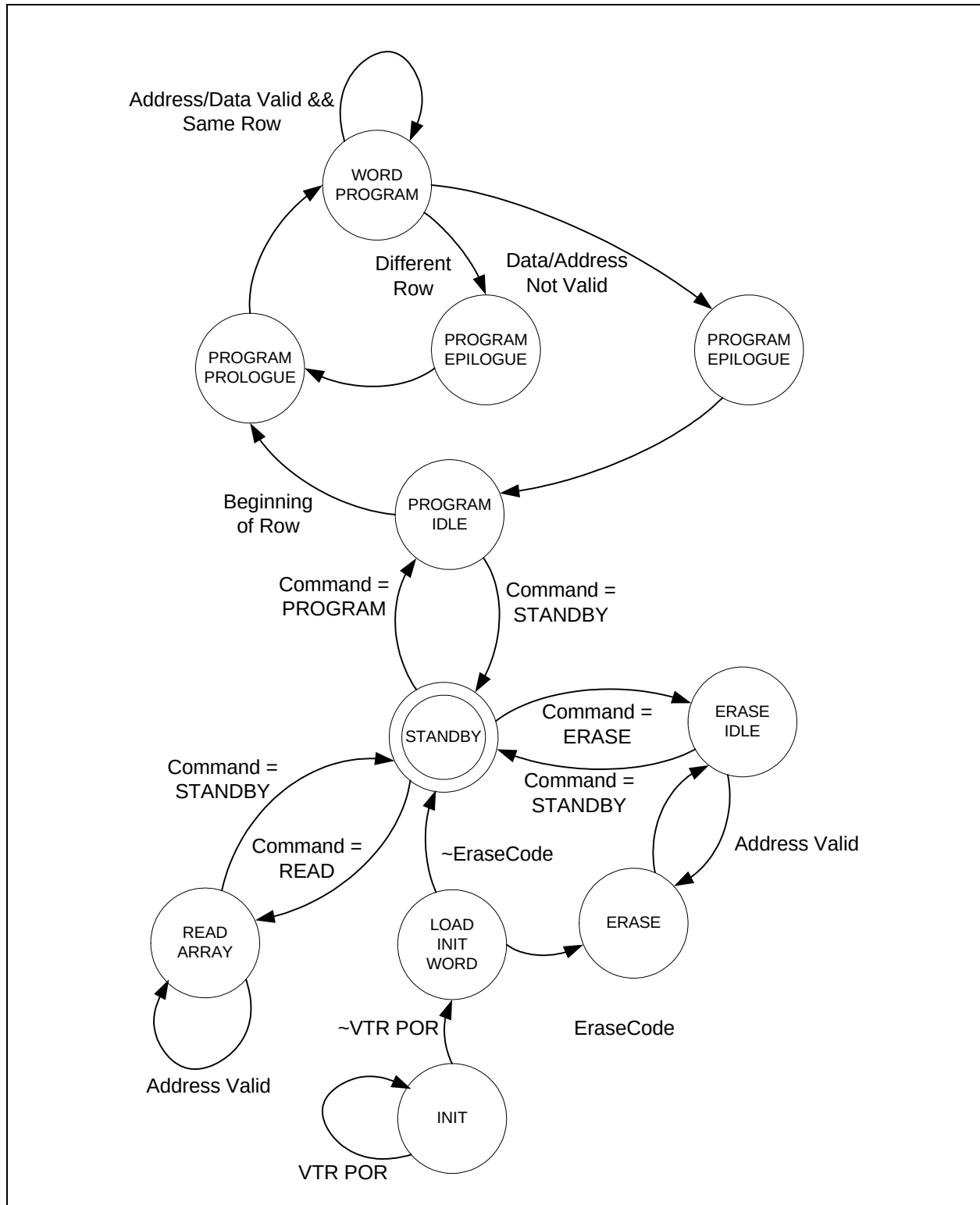


**Figure 15.5 Embedded Flash Controller State Diagram**

During VTR Reset, the Embedded Flash controller is kept in an initial state (INIT), after which it remains in **Standby Mode**. After initialization during normal operation, the Embedded Flash controller is placed into one of four modes (**Standby Mode**, **Read Mode**, **Program Mode** or **Erase Mode**) by



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setting [Flash\\_Mode](#) of the [Embedded Flash Command Register](#) to the appropriate values (0, 1, 2 or 3, respectively). Any write to the [Embedded Flash Command Register](#) while the controller is busy (when [Busy](#) of the [Embedded Flash Status Register](#) is '1b') will not modify the state and will set [Busy\\_Err](#) in the [Embedded Flash Status Register](#).

### 15.8.1 Standby Mode

When in this mode all strobes to the Flash Memory Array are de-asserted and the Flash Memory Array is placed in its lowest power state. Both the [Embedded Flash Data Register](#) FIFO and the [Embedded Flash Address Register](#) FIFO are flushed. The registers can be read and written by software without error. Data returned on a read of a flushed FIFO is undefined. On a transition from [Standby Mode](#) to [Program Mode](#), [Read Mode](#) or [Erase Mode](#) the FIFOs will be invalid and no action dependent on valid data in a FIFO will take place until new data is written into the registers.

The Embedded Flash controller must return to [Standby Mode](#) after any other state. An attempt to set the controller into a state other than [Standby Mode](#) when the controller is in [Program Mode](#), [Read Mode](#) or [Erase Mode](#) will put the controller in [Standby Mode](#) and set [CMD\\_Err](#) of the [Embedded Flash Status Register](#). [Flash\\_Mode](#) of the [Embedded Flash Command Register](#) will also be left in [Standby Mode](#). If the controller is busy, writes to the [Embedded Flash Command Register](#) are ignored and [Busy\\_Err](#) in the [Embedded Flash Status Register](#) is set.

### 15.8.2 Read Mode

When the Embedded Flash controller is in Read Mode the addressing strobes are kept de-asserted as long as no Read is in progress. When the strobes are de-asserted, the Embedded Flash array is maintained in its lowest power state (equivalent to [Standby Mode](#)). When the Valid bit associated with the Head register in the [Embedded Flash Address Register](#) is '1b' and the Data FIFO is not full, the data in the Embedded Flash array that corresponds to the [Embedded Flash Address Register](#) is loaded into the Tail register of the [Embedded Flash Data Register](#). The Data FIFO can hold two read results.

The Address FIFO is advanced when the Embedded Flash controller completes a read from the Embedded Flash array and stores the result in the Data FIFO. When byte 3 (the most significant byte) of the [Embedded Flash Data Register](#) is read, the Data FIFO is advanced. A read of the [Embedded Flash Address Register](#) will return the value of the Head register but will not advance the FIFO. A read of the [Embedded Flash Data Register](#) when the FIFO is empty but the controller is busy reading from the array will stall the read until the controller has completed the lookup and the data can be returned to the requestor.

#### 15.8.2.1 Burst Read Mode

When [Burst](#) in the [Embedded Flash Command Register](#) is set to '1b', the Read function automatically increments the [Embedded Flash Address Register](#) in order to minimize the time necessary to read a block of memory from the Embedded Flash. As in [Read Mode](#), a Flash read is initiated when the Head of the Address FIFO is Valid and the Data FIFO is empty. Whenever the Tail register in the Address FIFO is not Valid and the Head register in the FIFO is Valid, the Head register is incremented by 4 and written into the Tail. The Address FIFO will thus contain a sequence of consecutive word addresses as long as the Embedded Flash controller remains in [Burst Read Mode](#).

Reading the [Embedded Flash Data Register](#) from either the EC or the JTAG interface always reads 32 bits at a time, so the Data Register FIFO is always advanced when the EC or JTAG does a data read. In [Burst Read Mode](#) the entire Flash memory can be read by repeatedly reading the [Embedded Flash Data Register](#) without the need for reading or writing any other register in the Embedded Flash Subsystem.

The [Flash Mailbox interface](#) has an additional mechanism. When in [Burst Read Mode](#), the INDX portal has special behavior when it has the value 0h through 3h (that is, when INDX is set to point to the [Embedded Flash Data Register](#)). Every time the DATA portal is read by the Host, INDX will be automatically incremented by 1 when its value is 0h through 2h. If DATA is read by the Host when INDX is 3h, INDX is set to 0h and the Valid bit of the Head register of the Data FIFO is cleared. If there is a valid address in the Address FIFO, the sequence to read the next data value, described



above, will be initiated. When in **Burst Read Mode**, the entire contents of the Flash memory can be read by the Host with a sequence of reads to DATA, without any intervening writes to INDX.

**APPLICATION NOTE:** In **Burst Read Mode** the **Embedded Flash Data Register** will always contain the data from the next two locations after the last data location that is read.

### 15.8.3 Program Mode

When the Embedded Flash controller is in **Standby Mode**, setting the **Embedded Flash Command Register** to **Program Mode** will set up the Embedded Flash array for programming. The **Embedded Flash Data Register** and the **Embedded Flash Address Register** FIFOs are used for **Program Mode** in a manner similar to their use in **Read Mode**. When the Head registers in both the Address and Data FIFO are Valid, the Flash strobes are sequenced in order to write the contents of the Data register into the Flash Memory at the address specified in the Address register. At the end of the Word Program sequence the two FIFOs are advanced.

The following three sequences are used in programming the Embedded Flash:

5. Program Prologue: the controller issues the strobes required to set up programming a row (256 bytes) of the Flash, in either the main array or in the Info block. The Program Prologue takes approximately 16  $\mu$ s.
6. Word Program: the controller issues the strobes required to program the 32-bits present in the Head register of the Data FIFO into the Embedded Flash array at the address specified in the Head register of the Address FIFO. If Address bit 18 is '1b', the Data word is programmed into the Info block; if Address bit 18 is '0b', the Data word is programmed into the main Flash array. Word program takes approximately 22  $\mu$ s.
7. Program Epilogue: the controller issues the strobes required to finish programming a row. The Program Epilogue takes approximately 6.5  $\mu$ s.

During all three sequences, the controller asserts Busy while the sequence is in progress.

The Program Prologue is issued before the first time any word in a row can be programmed. The Program Epilogue is issued after the last time any word of a row is programmed. The Embedded Flash controller automatically issues the Program Prologue and Program Epilogue sequences as required. After the controller is placed in **Program Mode**, the Program Prologue is issued as soon as the Head registers in both the **Embedded Flash Data Register** and the **Embedded Flash Address Register** are Valid. Once the Program Prologue is completed, the controller will immediately issue the Word Program sequence.

While in **Program Mode**, if the Row address bits (bits 18 through 8) in the Head register of the **Embedded Flash Address Register** FIFO change, the controller issues the Program Epilogue followed by the Program Prologue before it issues the Word Program sequence. Programming one word could therefore take as long as 44.5  $\mu$ s to account for all three sequences to complete.

As long as the Head registers in both the **Embedded Flash Data Register** and the **Embedded Flash Address Register** are Valid the controller will continue to issue Word Program sequences. If either FIFO is invalid at the end of the Word Program sequence, the controller will issue the Program Epilogue sequence and the controller will be left in the initial **Program Mode** state. If new data arrives in the FIFOs, then the Program Prologue followed by the Word Program sequence will be issued.

The minimum time to program a row in the Embedded Flash is therefore

$$\text{time(Program Prologue)} + (64 \times \text{time(Word Program)}) + \text{time(Program Epilogue)}$$

or

$$16 \mu\text{s} + (64 \times 22 \mu\text{s}) + 6.5 \mu\text{s} = 1.43\text{ms}$$

If software cannot keep the Address and Data FIFOs filled at that rate, the time to program a row is therefore

$$64 \times (\text{time(Program Prologue)} + \text{time(Word Program)} + \text{time(Program Epilogue)})$$



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or

$$64 \times (16 \mu\text{s} + 22 \mu\text{s} + 6.5 \mu\text{s}) = 2.84\text{ms}$$

[Burst Program Mode](#), described in the next section, can help software keep the Address and Data FIFOs filled more efficiently.

Each address in the Embedded Flash can be programmed at most twice between erasures.

### 15.8.3.1 Burst Program Mode

[Burst Program Mode](#) is enabled whenever [Burst](#) in the [Embedded Flash Command Register](#) is set and the controller is in [Program Mode](#). The behavior is similar to [Burst Read Mode](#). When [Burst](#) is enabled, the [Embedded Flash Address Register](#) FIFO is always kept filled automatically with incrementing addresses. Whenever the Tail register in the Address FIFO is not Valid and the Head register is valid, the Head register is incremented by 4 and stored in the Tail. The controller otherwise behaves as in [Program Mode](#). When both the Head register of the Address FIFO and the Head register of the Data FIFO are Valid, a Word Program sequence is initiated (with the possible addition of Program Prologue and Program Epilogue, as described above). When the programming sequence is complete, the Head registers of both FIFOs are marked not Valid. With this mechanism the entire Flash array can be programmed with a sequence of writes to the [Embedded Flash Data Register](#) without any writes to the [Embedded Flash Address Register](#) or [Embedded Flash Command Register](#).

The [Flash Mailbox interface](#) has an additional mechanism, as in [Burst Read Mode](#). The INDX portal has special behavior when it has the value 0h through 3h (that is, when INDX is set to point to the [Embedded Flash Data Register](#)). Every time the DATA portal is written by the Host, INDX will be automatically incremented by 1 when its value is 0h through 2h. If DATA is written by the Host when INDX is 3h, INDX is set to 0h and the Tail register of the Data FIFO is advanced to the Head and the Tail is marked not Valid. If there is a valid address in the Head of the Address FIFO, the Word Program sequence will be initiated. In [Burst Program Mode](#), the entire contents of the Flash memory can be programmed by the Host with a sequence of writes to DATA, without any intervening writes to INDX.

### 15.8.4 Erase Mode

When [Embedded Flash Command Register](#) is set to [Erase Mode](#). The state machine will wait until a valid address is written into the [Embedded Flash Address Register](#). Once the register is valid, [Busy](#) in the [Embedded Flash Status Register](#) is set to '1b' and the Embedded Flash controller sequences the Embedded Flash array strobes to erase part or all of the Embedded Flash. All bits in the erased area are set to '1b'. [Busy](#) remains set during the operation. When the erase operation is complete [Busy](#) is set to '0b'. The controller remains in [Erase Mode](#) and can accept additional addresses in the [Embedded Flash Address Register](#).

The area to be erased is determined by Bits[23:18] of the [Embedded Flash Address Register](#), as shown in [Table 15.5, "Erase Mode Functions"](#). In all cases [Embedded Flash Address Register](#) bits[10:0] are ignored. The [Embedded Flash Address Register](#) should be configured with the proper page address before setting the [Embedded Flash Command Register](#) to [Erase Mode](#). Erase time is 22 ms, for all Erase Mode Functions.

**Table 15.5 Erase Mode Functions**

| ADDRESS REGISTER<br>BITS[23:18] | AREA ERASED                                                                                                |
|---------------------------------|------------------------------------------------------------------------------------------------------------|
| xxxx00b                         | 2KB Page in Embedded Flash Main Array specified by <a href="#">Embedded Flash Address Register</a> [17:11] |
| xxxx01b                         | Embedded Flash Info Block                                                                                  |
| 111110b                         | Mass erase of entire Embedded Flash Main Array                                                             |

Table 15.5 Erase Mode Functions

| ADDRESS REGISTER<br>BITS[23:18] | AREA ERASED                                                                  |
|---------------------------------|------------------------------------------------------------------------------|
| 111111b                         | Mass erase of entire Embedded Flash Main Array and Embedded Flash Info Block |

## 15.9 Flash Lock Controls

### 15.9.1 Flash Write Protect

When the [Boot\\_Lock](#) in the [Embedded Flash Configuration Register](#) is asserted or the input pin nFWP is asserted, the bottom 4K bytes (0000h – 0FFFh) of the Flash Main Memory Array (the Boot Block) are write protected and cannot be changed by any programming method including [Program Mode](#) or [Erase Mode](#). The Mass Erase function is therefore disabled, since it would erase the Boot Block. The rest of the Embedded Flash array, including the Info block, is not affected. If both [Boot\\_Lock](#) and the input pin nFWP are not asserted, all programming and erase functions, including [Erase Mode](#), are enabled and the bottom 4K bytes are not protected.

### 15.10 [Instruction Memory Interface](#) or the [Register Interface](#) will return FFFF\_FFFFh. Once set, only a VTR POR ([nSYS\\_RSTVTR](#) POR ([nSYS\\_RSTVTR](#) POR ([nSYS\\_RSTVTR](#) POR ([nSYS\\_RSTVTR](#) POR ([nSYS\\_RSTVTR](#) POR ([nEC\\_RST](#) timing

## Programming the Embedded Flash Array

In normal operation, the EC fetches all of its instructions from the Embedded Flash array. While it is executing out of Flash, the program interface using the registers described in the next section cannot be used. When the [Register Interface](#) is used, the EC cannot fetch either instructions or data out of the Embedded Flash. The EC can either sleep, or run entirely out of the [EC Data Memory](#). When running out of [EC Data Memory](#), EC firmware should insure that all interrupts are disabled, unless the interrupt vector table is relocated to the [EC Data Memory](#) along with any interrupt handler that is enabled.

There are three methods by which the Embedded Flash array can be programmed:

- The Flash may be programmed through the JTAG interface. Through the JTAG interface, the EC can be halted or directed to run entirely out of the [EC Data Memory](#). Once the EC no longer requires the Flash, the registers in the next section can be used to program the array, by first setting [Reg\\_Ctl\\_En](#) in the [Embedded Flash Configuration Register](#) (enabling register control of the Flash), then using the other registers to program the array. Once programming is completed, [Reg\\_Ctl\\_En](#) in the [Embedded Flash Configuration Register](#) is cleared (enabling EC instruction access) and then setting the EC into the RUN state. See [Chapter 13, "JTAG and XNOR," on page 248](#) for a description of JTAG operation.
- The Flash may be programmed by the Host. After co-ordination between the Host and the EC, the EC configures the [Embedded Flash Configuration Register](#) to enable the register programming mode and to give the Host write access to the registers (by setting both [Reg\\_Ctl\\_En](#) and [Host\\_Ctl](#) to '1b'). The EC would then disable all interrupts except the EC\_Int Flash Mailbox interrupt from the Host. The EC Interrupts for LRESET# and VCC PWRGD pin signals should also be enabled (see [Section 15.4, "Interrupts," on page 279](#)), in order to restore control to the EC in the event the Host loses power and does not return control to the EC properly. The EC then signals the Host that it can proceed. At this point the EC should verify that the Host can take control, by checking the state of LRESET# and VCC PWRGD. If LRESET# is asserted or VCC PWRGD is de-asserted, the Host will not respond to the EC signal to take control, and the EC should therefore cancel the hand off to the Host, clear [Reg\\_Ctl\\_En](#) and [Host\\_Ctl](#), re-enable interrupts and continue. If the Host is capable of responding to the EC signal, the EC finally either puts itself to sleep or runs entirely out of the. When the Host finishes programming the Embedded Flash array, it sets [EC\\_Int](#) in the [Embedded Flash Command Register](#) to '1b', which wakes the EC.



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The Host may also program the Flash through the use of the [MailBox Register Interface](#). The Host communicates the address to be modified and the data to program through a pre-arranged set of mailbox registers, then sends an interrupt to the EC. The EC would then program the Flash while running out of the on-chip SRAM, as described in the following bullet item.

- The EC can itself program the Flash array by loading a program to do so into the on-chip 4KB SRAM. Once the EC is running out of SRAM, it can disable all interrupts and configure the Flash array to be programmable through the registers (by setting [Reg\\_Ctl\\_En](#) in the [Embedded Flash Configuration Register](#)). After programming is completed, the EC can reset the [Reg\\_Ctl](#) bit to make the Flash accessible to instruction fetch.

In all cases, the [Embedded Flash Data Register](#) can be updated to set up the next write while the Flash is busy programming the current write.

**APPLICATION NOTE:** When the ARC is put to sleep during Flash programming, the [FLASH](#) bit in the [EC Blocks Sleep Enables Register on page 111](#) should be cleared to '0' insure that the ring oscillator never stops.

### 15.10.1 Transferring Control to the Host

In order to transfer control of the Embedded Flash to the Host, the EC has to enable the Host access to the Register interface, inform the Host that it has access, then either sleep or execute code entirely out of the [EC Data Memory](#). The EC must sleep or execute in RAM because it will no longer be able to use the ICCM instruction memory interface. The following sequence is an example of how this transfer can be accomplished:

```
// This code is located in the Flash
// Command_Address is 0xFF3908
// Config_Address is 0xFF3910
//
*Config_Address |= REG_CTL_EN | HOST_CTL; // Permit the Host to control the Flash
registers
Disable_all_interrupts();
Enable_Interrupt(EC_Int);                // Enable transition from Host back to EC
Enable_Interrupt(LRESET#);
Enable_Interrupt(VCC_PWRGD);
Host_Message(FLASH_READY);              // Tell Host it can take control of the Flash
if( asserted(LRESET) || deasserted(VCCPWRGD) ) {
    cancel_flash_transfer();              // Host is not powered: annul transfer
                                        // restore Flash configuration/command registers
    restore_interrupts();
    return();                            // return to regular EC code
} else {
    sleep();                             // Wait for EC_Int
}
```

The next code sequence would be executed by the Host once it receives the message from the EC that it may take control of the Flash:

```
// INDX is the address of INDX in the Host I/O space
// DATA is the address of DATA in the Host I/O space
//
INDX = 9; // index of Command register byte where Reg_Ctl bit is located
DATA = REG_CTL; Take control of the Flash Address and Data registers
```

As an alternative to the Flash-based EC code described above, the transfer function can run partially in Flash and partially in SRAM. In this mode it is not necessary to enable LRESET# or VCC PWRGD interrupts, since SRAM-based EC code can check the state of those signals through polling: Normal termination of Flash programming occurs as before when the Host sets the [EC\\_Int](#) bit in the Command register.

```
// This code is located in the Flash
// Command_Address is 0xFF3908
// Config_Address is 0xFF3910
//
```

```

*Config_Address |= REG_CTL_EN;    // Permit control of Flash via register interface
Disable_all_interrupts();
Enable_Interrupt(EC_Int);         // Enable transition back to EC
goto SRAM_Flash_Code;
...
SRAM_Flash_Code:                  // start of code in SRAM
*Command_Address |= REG_CTL;
*Config_Address |= HOST_CTL;
Host_Message(FLASH_READY);
while(true) {                     // commence polling on LRESET/VCC PWRGD
    if( asserted(LRESET) || deasserted(VCCPWRGD) ) {
        cancel_flash_transfer(); // Host is not powered: annul transfer
                                // restore Flash configuration/command registers
        restore_interrupts();
        return();               // return to EC code in Flash
    }
}

```

## 15.10.2 Reading the Embedded Flash

The Embedded Flash memory, in both the main array as well as the Info block, can most conveniently be read with Burst mode set. An initial Flash address should be configured, and then the rest of the Flash memory can be read with just a sequence of reads to the data register. The following pseudocode illustrates how reading the Flash from the Host might proceed:

```

// Byte_array[] is a data structure to receive the data. It is a sequence of bytes
// Flashbase is the first address in the flash memory to be read
// Limit is the total number of bytes to read
// INDX is the address of INDX in the Host I/O space
// DATA is the address of DATA in the Host I/O space
//
// this code works as long as the read does not wrap around the end of the Flash array
//
INDX = 8; // index of Command register
DATA = READ | BURST;
INDX = 6; // bits 24:16 of Flash Address register
DATA = Flashbase.byte2;
INDX = 5; // bits 15:8 of Flash Address register
DATA = Flashbase.byte1;
INDX = 4; // bits 7:0 of Flash Address register
DATA = Flashbase.byte0; // the Flash address advances in the Address FIFO
                        // Read from the Flash is started
INDX = 0; // bits 7:0 of Flash Data register
for( i = 0; i < Limit; i++)
{
    Byte_array[i] = DATA;
}
INDX = 8; // index of Command register
DATA = STANDBY; // Exit READ mode and flush Address/Data FIFOs

```

Reading from the EC is similar, except that data can be read four bytes at a time:

```

// Word_array[] is a data structure to receive the data.
// It is a sequence of 32-bit words
// Flashbase is the first address in the flash memory to be read
// Limit is the total number of 32-bit words to read
// Flash_Address is 0xFF3904
// Data_Address is 0xFF3900
// Command_Address is 0xFF3908
//
// this code works as long as the read does not wrap around the end of the Flash array
//
*Command_Address = READ | BURST;
*Flash_Address = Flashbase; // the Flash address advances in the Address FIFO
for( i = 0; i < Limit; i++)
{
    Word_array[i] = *Flash_Data;
}

```



```
}
*Command_Address = STANDBY; // Exit READ mode and flush Address/Data FIFOs
```

### 15.10.3 Writing the Embedded Flash

The Embedded Flash memory, in both the main array as well as the Info block, can most conveniently be programmed with Burst mode set. An initial Flash address should be configured, and then the rest of the Flash memory can be written with just a sequence of writes to the data register. Because programming takes between 20 and 40  $\mu$ s, the Host may choose to approximate the latency before polling the Status register. The following pseudocode illustrates how reading the Flash from the Host might proceed:

```
// Byte_array[] is a data structure that sources the data. It is a sequence of bytes
// Flashbase is the first address in the flash memory to be programmed
// Limit is the total number of bytes to write. It is assumed to be a multiple of
// the 256-byte row size for simplicity
// INDX is the address of INDX in the Host I/O space
// DATA is the address of DATA in the Host I/O space
//
// this code works as long as the write block does not wrap around
// the end of the Flash array.
//
INDX = 8; // index of Command register
DATA = PROGRAM | BURST;
INDX = 6; // bits 24:16 of Flash Address register
DATA = Flashbase.byte2;
INDX = 5; // bits 15:8 of Flash Address register
DATA = Flashbase.byte1;
INDX = 4; // bits 7:0 of Flash Address register
DATA = Flashbase.byte0; // the Flash address advances in the Address FIFO
for( i = 0; i < Limit; )
{
    INDX = 0xC; // index of Status register, to check space in Data FIFO
    while( DATA & DATA_FULL ); // stall while Data FIFO has no space
    INDX = 0; // bits 7:0 of Flash Data register
    // Write one word (four bytes) into the Flash array
    DATA = Byte_array[i++];
    DATA = Byte_array[i++];
    DATA = Byte_array[i++];
    DATA = Byte_array[i++];
}
INDX = 8; // index of Command register
DATA = STANDBY; // Exit PROGRAM mode and flush Address/Data FIFOs
```

Writing from the EC is similar, except that data can be written four bytes at a time

```
// Word_array[] is a data structure to receive the data.
// It is a sequence of 32-bit words
// Flashbase is the first address in the flash memory to be written
// Limit is the total number of 32-bit words to write
// Flash_Address is 0xFF3904
// Data_Address is 0xFF3900
// Command_Address is 0xFF3908
// Status_Address is 0xFF390C
//
// this code works as long as the program block does not wrap around
// the end of the Flash array
//
*Command_Address = PROGRAM | BURST;
*Flash_Address = Flashbase; // the Flash address advances in the Address FIFO
for( i = 0; i < Limit; i++)
{
    while( *Status_Address & DATA_FULL ); // stall while Data FIFO has no space
    *Flash_Data = Word_array[i];
}
*Command_Address = STANDBY; // Exit PROGRAM mode and flush Address/Data FIFOs
```



#### **15.10.4 ATE Programming**

There is no ATE-specific interface for programming the Embedded Flash. ATE will use either the LPC register interface, or the EC interface via JTAG.





## 15.11 Detailed Description of Accessible Registers

|    | MEC5035 pin | Foundry Flash Signal Name | Functional Signal Name          |
|----|-------------|---------------------------|---------------------------------|
| 1  | 5           | flash_se                  | GPIO003/I2C1A_DATA              |
| 2  | 6           | flash_nvstr               | GPIO004/I2C1A_CLK               |
| 3  | 7           | flash_erase               | GPIO005/I2C1B_DATA              |
| 4  | 8           | flash_prog                | GPIO006/I2C1B_CLK               |
| 5  | 9           | flash_yc                  | GPIO007 /I2C1D_DATA /PS2_CLK0B  |
| 6  | 10          | flash_yle                 | GPIO010 /I2C1D_CLK /PS2_DAT0B   |
| 7  | 11          | flash_xle                 | GPIO011/nSMI                    |
| 8  | 12          | flash_dle                 | GPIO012 /I2C1H_DATA /I2C2D_DATA |
| 9  | 13          | flash_fad31               | GPIO013 /I2C1H_CLK /I2C2D_CLK   |
| 10 | 14          | flash_fad30               | GPIO014/GPTP-IN7                |
| 11 | 15          | flash_fad29               | GPIO015/GPTP-OUT7               |
| 12 | 16          | flash_fad28               | GPIO016/GPTP-IN8                |
| 13 | 17          | flash_fad27               | GPIO017/GPTP-OUT8               |
| 14 | 18          | flash_fad26               | GPIO020                         |
| 15 | 19          | flash_fad25               | GPIO021/RC_ID                   |
| 16 | 27          | flash_fad24               | GPIO025/UART_CLK                |
| 17 | 28          | flash_fad23               | GPIO026/GPTP-IN1                |
| 18 | 29          | flash_fad22               | GPIO027/GPTP-OUT1               |
| 19 | 30          | flash_fad21               | GPIO030/GPTP-IN2                |
| 20 | 31          | flash_fad20               | GPIO031/GPTP-OUT2               |
| 21 | 32          | flash_fad19               | GPIO032/GPTP-IN3                |
| 22 | 33          | flash_fad18               | GPIO040/GPTP-OUT3               |
| 23 | 35          | flash_fad17               | GPIO042/BCM_C_INT#              |
| 24 | 38          | flash_fad16               | GPIO045/LSBCM_D_INT#            |
| 25 | 39          | flash_fad15               | GPIO046/LSBCM_D_DAT             |
| 26 | 40          | flash_fad14               | GPIO047/LSBCM_D_CLK             |
| 27 | 41          | flash_fad13               | GPIO050/FAN_TACH1               |
| 28 | 42          | flash_fad12               | GPIO051/FAN_TACH2               |
| 29 | 43          | flash_fad11               | GPIO052/FAN_TACH3               |
| 30 | 45          | flash_fad10               | GPIO053/PWM0                    |
| 31 | 46          | flash_fad9                | GPIO054/PWM1                    |
| 32 | 47          | flash_fad8                | GPIO055/PWM2                    |
| 33 | 48          | flash_fad7                | GPIO056/PWM3                    |
| 34 | 50          | flash_fad6                | GPIO060/KBRST                   |
| 35 | 54          | flash_fad5                | GPIO061/LPCPD#                  |
| 36 | 70          | flash_fad4                | GPIO104/UART_TX                 |
| 37 | 71          | flash_fad3                | GPIO105/UART_RX                 |
| 38 | 72          | flash_fad2                | GPIO106/nRESET_OUT              |
| 39 | 73          | flash_fad1                | GPIO107                         |
| 40 | 75          | flash_fad0                | GPIO110 /PS2_CLK2 /GPTP-IN6     |
| 41 | 76          | flash_trm                 | GPIO111 /PS2_DAT2 /GPTP-OUT6    |
| 42 | 77          | flash_xe                  | GPIO112/PS2_CLK1A               |
| 43 | 78          | flash_mas1                | GPIO113/PS2_DAT1A               |
| 44 | 79          | flash_ifren               | GPIO114/PS2_CLK0A               |
| 45 | 91          | test_mclk                 | GPIO126                         |
| 46 | No Bond     | FLASH_TM0                 |                                 |
| 47 | No Bond     | FLASH_TM1                 |                                 |
| 48 | No Bond     | FLASH_TM2                 |                                 |
| 49 | No Bond     | FLASH_DIRECT              |                                 |
| 50 | No Bond     | No Bond VPP               |                                 |



See [Section 15.7, "Register Interface,"](#) on page 280

### 15.11.1 Embedded Flash Data Register

The [Embedded Flash Data Register](#) can only be written when the Embedded Flash Controller is in [Program Mode](#). In [Standby Mode](#), [Read Mode](#) and [Program Mode](#) the register is read-only. Writes will complete but have no effect.

**Table 15.6 Embedded Flash Data Register**

|            |                                                                          |     |     |             |     |     |                     |     |
|------------|--------------------------------------------------------------------------|-----|-----|-------------|-----|-----|---------------------|-----|
| HOST INDEX | BYTE3: INDX 03h<br>BYTE2: INDX 02h<br>BYTE1: INDX 01h<br>BYTE0: INDX 00h |     |     | 8-bit       |     |     | HOST SIZE           |     |
| EC OFFSET  | 100h                                                                     |     |     | 32/16/8-bit |     |     | EC SIZE             |     |
| POWER      | VTR                                                                      |     |     | 0000_0000h  |     |     | nSYS_RST<br>DEFAULT |     |
| BUS        | LPC SPB                                                                  |     |     |             |     |     |                     |     |
| BYTE3 BIT  | D31                                                                      | D30 | D29 | D28         | D27 | D26 | D25                 | D24 |
| HOST TYPE  | R/W                                                                      | R/W | R/W | R/W         | R/W | R/W | R/W                 | R/W |
| EC TYPE    | R/W                                                                      | R/W | R/W | R/W         | R/W | R/W | R/W                 | R/W |
| BIT NAME   | Flash_Data[31:24]                                                        |     |     |             |     |     |                     |     |
| BYTE2 BIT  | D23                                                                      | D22 | D21 | D20         | D19 | D18 | D17                 | D16 |
| HOST TYPE  | R/W                                                                      | R/W | R/W | R/W         | R/W | R/W | R/W                 | R/W |
| EC TYPE    | R/W                                                                      | R/W | R/W | R/W         | R/W | R/W | R/W                 | R/W |
| BIT NAME   | Flash_Data[23:16]                                                        |     |     |             |     |     |                     |     |
| BYTE1 BIT  | D15                                                                      | D14 | D13 | D12         | D11 | D10 | D9                  | D8  |
| HOST TYPE  | R/W                                                                      | R/W | R/W | R/W         | R/W | R/W | R/W                 | R/W |
| EC TYPE    | R/W                                                                      | R/W | R/W | R/W         | R/W | R/W | R/W                 | R/W |
| BIT NAME   | Flash_Data[15:8]                                                         |     |     |             |     |     |                     |     |
| BYTE0 BIT  | D7                                                                       | D6  | D5  | D4          | D3  | D2  | D1                  | D0  |
| HOST TYPE  | R/W                                                                      | R/W | R/W | R/W         | R/W | R/W | R/W                 | R/W |
| EC TYPE    | R/W                                                                      | R/W | R/W | R/W         | R/W | R/W | R/W                 | R/W |
| BIT NAME   | Flash_Data[7:0]                                                          |     |     |             |     |     |                     |     |



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**FLASH\_DATA[31:0]**

This 32-bit register holds the data to be written into the Flash memory array during a program cycle, as well as the data returned from a Flash memory read during a Read From SPB cycle. It should be set up before the [Embedded Flash Address Register](#) is configured.

**15.11.2 Embedded Flash Address Register****Table 15.7 Embedded Flash Address Register**

|            |                                                                          |     |     |     |             |     |          |                     |
|------------|--------------------------------------------------------------------------|-----|-----|-----|-------------|-----|----------|---------------------|
| HOST INDEX | BYTE3: INDX 07h<br>BYTE2: INDX 06h<br>BYTE1: INDX 05h<br>BYTE0: INDX 04h |     |     |     | 8-bit       |     |          | HOST SIZE           |
| EC OFFSET  | 104h                                                                     |     |     |     | 32/16/8-bit |     |          | EC SIZE             |
| POWER      | VTR                                                                      |     |     |     | 0000_0000h  |     |          | nSYS_RST<br>DEFAULT |
| BUS        | LPC SPB                                                                  |     |     |     |             |     |          |                     |
| BYTE3 BIT  | D31                                                                      | D30 | D29 | D28 | D27         | D26 | D25      | D24                 |
| HOST TYPE  | R                                                                        | R   | R   | R   | R           | R   | R        | R                   |
| EC TYPE    | R                                                                        | R   | R   | R   | R           | R   | R        | R                   |
| BIT NAME   | Reserved                                                                 |     |     |     |             |     |          |                     |
| BYTE2 BIT  | D23                                                                      | D22 | D21 | D20 | D19         | D18 | D17      | D16                 |
| HOST TYPE  | R/W                                                                      | R/W | R/W | R/W | R/W         | R/W | R/W      | R/W                 |
| EC TYPE    | R/W                                                                      | R/W | R/W | R/W | R/W         | R/W | R/W      | R/W                 |
| BIT NAME   | Flash_Address[23:16]                                                     |     |     |     |             |     |          |                     |
| BYTE1 BIT  | D15                                                                      | D14 | D13 | D12 | D11         | D10 | D9       | D8                  |
| HOST TYPE  | R/W                                                                      | R/W | R/W | R/W | R/W         | R/W | R/W      | R/W                 |
| EC TYPE    | R/W                                                                      | R/W | R/W | R/W | R/W         | R/W | R/W      | R/W                 |
| BIT NAME   | Flash_Address[15:8]                                                      |     |     |     |             |     |          |                     |
| BYTE0 BIT  | D7                                                                       | D6  | D5  | D4  | D3          | D2  | D1       | D0                  |
| HOST TYPE  | R/W                                                                      | R/W | R/W | R/W | R/W         | R/W | R        | R                   |
| EC TYPE    | R/W                                                                      | R/W | R/W | R/W | R/W         | R/W | R        | R                   |
| BIT NAME   | Flash_Address[7:2]                                                       |     |     |     |             |     | Reserved |                     |

**FLASH\_ADDRESS[23:0]**

This register represents a byte address for the Embedded Flash array. Since all read and write operations are to 32-bit quantities, the low-order to bits (Flash\_Address[1:0] must always be 0, so

these bits are reserved. If the Flash state machine is in [Read Mode](#), writing Byte0 of the [Embedded Flash Address Register](#) initiates the Read sequence. If the Flash state machine is in [Program Mode](#), the Program sequence is initiated when there is both a valid Data value in the [Embedded Flash Data Register](#) and the [Embedded Flash Address Register](#) has been updated by writing Byte0. If Bit18 is '1b' then the Info block in the Embedded Flash subsystem is selected. Bit19 is only examined in [Erase Mode](#). When in [Erase Mode](#)., if Bits[23:19] contain any value other than '11111b', then Page Erase is enabled. If Bits[23:19] is '11111b', Mass Erase is enabled.

### 15.11.3 Embedded Flash Command Register

This register is Read-Only while [Busy](#) in the [Embedded Flash Status Register](#) is '1b'. An attempt to write this register while [Busy](#) is asserted will not modify the register and will set [Busy\\_Err](#) in the [Embedded Flash Status Register](#).

A write to this register causes the Embedded Flash controller to transition to the selected state.

**Table 15.8 Embedded Flash Command Register**

|               |                                  |     |     |             |        |       |                     |         |
|---------------|----------------------------------|-----|-----|-------------|--------|-------|---------------------|---------|
| HOST INDEX    | BYTE0: INDX 8h<br>BYTE1: INDX 9h |     |     | 8-bit       |        |       | HOST SIZE           |         |
| EC OFFSET     | 108h                             |     |     | 32/16/8-bit |        |       | EC SIZE             |         |
| POWER         | VTR                              |     |     | 00h         |        |       | nSYS_RST<br>DEFAULT |         |
| BUS           | LPC SPB                          |     |     |             |        |       |                     |         |
| BYTE[3:2] BIT | D31                              | D30 | D29 | ...         |        | D18   | D17                 | D16     |
| HOST TYPE     | R                                | R   | R   | R           | R      | R     | R                   | R       |
| EC TYPE       | R                                | R   | R   | R           | R      | R     | R                   | R       |
| BIT NAME      | Reserved                         |     |     |             |        |       |                     |         |
| BYTE1 BIT     | D15                              | D14 | D13 | D12         | D11    | D10   | D9                  | D8      |
| HOST TYPE     | R                                | R   | R   | R           | R      | R     | R                   | R/W     |
| EC TYPE       | R                                | R   | R   | R           | R      | R     | R                   | R/W     |
| BIT NAME      | Reserved                         |     |     |             |        |       |                     | Reg_Ctl |
| BYTE0 BIT     | D7                               | D6  | D5  | D4          | D3     | D2    | D1                  | D0      |
| HOST TYPE     | R                                | R   | R   | R/W         | R/W    | R/W   | R/W                 | R/W     |
| EC TYPE       | R                                | R   | R   | R/W         | R/W    | R/W   | R/W                 | R/W     |
| BIT NAME      | Reserved                         |     |     |             | EC_Int | Burst | Flash_Mode[1:0]     |         |

#### FLASH\_MODE

The field determines which Master may write the registers in the Embedded Flash controller:

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- 0 The Embedded Flash controller is placed in the Standby mode.
- 1 The Embedded Flash controller is placed in Read mode.
- 2 The Embedded Flash controller is placed in Program mode.
- 3 The Embedded Flash controller is placed in Erase mode.

**BURST**

If the Embedded Flash controller is in [Read Mode](#) or [Program Mode](#) and this bit is '1b', the contents of the Head register in the [Embedded Flash Address Register](#) FiFO will be incremented by 4 and written into the Tail register whenever the Head register is Valid. When this bit is '0b', the [Embedded Flash Address Register](#) and the INDEX register are not incremented automatically.

See [Section 15.8.2.1, "Burst Read Mode," on page 285](#) and [Section 15.8.3.1, "Burst Program Mode," on page 287](#) for information about the use of [Burst](#).

**EC\_INT**

Setting this bit to '1b' generates an EC interrupt and simultaneously sets [Reg\\_Ctl\\_En](#) and [Host\\_Ctl](#) in the [Embedded Flash Configuration Register](#) as well as [Reg\\_Ctl\\_En](#) in this register to '0b'. By setting these bits to '0b' the Embedded Flash array is configured for EC instruction access, so that when the EC awakes and responds to the interrupt request triggered by [EC\\_Int](#), it can fetch the interrupt vector from its usual location in the Embedded Flash array. See [Section 15.4, "Interrupts," on page 279](#).

The response to setting this bit is the same as the response to VCC PWRGD or PCIRESET signals, as detailed in [Table 15.1, "VCC PWRGD and LRESET# Behavior"](#). If the Embedded Flash Controller is in either [Erase Mode](#) or [Program Mode](#) the programming sequence is terminated, the Embedded Flash controller is set to [Standby Mode](#), [Reg\\_Ctl](#), [Reg\\_Ctl\\_En](#) and [Host\\_Ctl](#) are set to '0b' and the wakeup interrupt is sent to the EC.

**REG\_CTL**

When this bit is set, the address input and the control strobes of the Flash Memory Array are sourced from the registers in the [Embedded Flash Subsystem](#). Software on either the Host or the EC can read and write the Flash Memory Array by reading and writing the registers in the subsystem. The EC cannot execute instructions out of the Flash Memory Array.

When this bit is cleared (which is the default), the address input and the control strobes of the Flash Memory Array are sourced from the Instruction Closely Coupled Memory interface. The EC can execute instructions directly from the Flash Memory Array. The other registers in the [Embedded Flash Subsystem](#) can be read or written, but do not affect the Flash Memory Array.

**Note:** A 32-bit write from either the EC or JTAG with [Reg\\_Ctl\\_En](#) set to '1b' can simultaneously write the Byte 0 control bits in the [Embedded Flash Command Register](#).

This bit can only be set if [Reg\\_Ctl\\_En](#) in the [Embedded Flash Configuration Register](#) is '1b'.

## 15.11.4 Embedded Flash Status Register

**Table 15.9 Embedded Flash Status Register**

| HOST INDEX    | BYTE 1: INDX Dh<br>BYTE 0: INDX Ch |     |     |     | 8-bit       |              | HOST SIZE           |          |
|---------------|------------------------------------|-----|-----|-----|-------------|--------------|---------------------|----------|
| EC OFFSET     | 10Ch                               |     |     |     | 32/16/8-bit |              | EC SIZE             |          |
| POWER         | VTR                                |     |     |     | 0000_0000h  |              | nSYS_RST<br>DEFAULT |          |
| BUS           | LPC SPB                            |     |     |     |             |              |                     |          |
| BYTE[3:2] BIT | D31                                | D30 | D29 | ... |             | D18          | D17                 | D16      |
| HOST TYPE     | R                                  | R   | R   | R   | R           | R            | R                   | R        |
| EC TYPE       | R                                  | R   | R   | R   | R           | R            | R                   | R        |
| BIT NAME      | Reserved                           |     |     |     |             |              |                     |          |
| BYTE1 BIT     | D15                                | D14 | D13 | D12 | D11         | D10          | D9                  | D8       |
| HOST TYPE     | R                                  | R   | R   | R   | R           | R/WC         | R/WC                | R/WC     |
| EC TYPE       | R                                  | R   | R   | R   | R           | R/WC         | R/WC                | R/WC     |
| BIT NAME      | Reserved                           |     |     |     |             | Protect_Err  | CMD_Err             | Busy_Err |
| BYTE0 BIT     | D7                                 | D6  | D5  | D4  | D3          | D2           | D1                  | D0       |
| HOST TYPE     | R                                  | R   | R   | R   | R           | R            | R                   | R        |
| EC TYPE       | R                                  | R   | R   | R   | R           | R            | R                   | R        |
| BIT NAME      | Reserved                           |     |     | FWP | Boot_Lock   | Address_Full | Data_Full           | Busy     |

### BUSY

This bit reflects the state of the Embedded Flash controller. This bit is set while the controller is processing a flash control sequence. While this bit is set the [Embedded Flash Command Register](#) can not be written. If a write is attempted on this register, the write fails and [Busy\\_Err](#) in this register is set.

This bit is read-only.

### DATA\_FULL

This bit reflects the value of the Valid bit of the Tail register of the [Embedded Flash Data Register](#). When it is set the FIFO is full and any additional writes will set [Busy\\_Err](#).

This bit is read-only.

**Product Customer Specification-ODM****ADDRESS\_FULL**

This bit reflects the value of the Valid bit of the Tail register of the [Embedded Flash Address Register](#). When it is set the FIFO is full and any additional writes will set [Busy\\_Err](#).

This bit is read-only.

**BOOT\_LOCK**

This bit is set whenever the Boot Block is write-protected. The Boot Block will be write-protected when [Boot\\_Lock](#) in the [Embedded Flash Configuration Register](#) is set, or when the nFWP input pin is asserted.

. A copy is maintained in this register so that the Host can access it, since the Host has no access to the [Embedded Flash Configuration Register](#). See [Section 15.9.1, "Flash Write Protect," on page 288](#) for a description of write-protecting the boot block.

This bit is read-only.

**FWP**

The FWP bit reflects the state of the nFWP input pin. When the nFWP pin is asserted ('0b'), the FWP bit is '1b'. When the nFWP pin is not asserted ('1b'), the FWP bit is '0b'. See [Section 15.9.1, "Flash Write Protect," on page 288](#) for a description of write-protecting the boot block.

**BUSY\_ERR**

This bit is set if

- A write to the [Embedded Flash Command Register](#) occurs while [Busy](#) is set.
- A write to the [Embedded Flash Address Register](#) occurs while [Address\\_Full](#) is set.
- A write to the [Embedded Flash Data Register](#) occurs while [Data\\_Full](#) is set

This bit is sticky: once set, it remains set until cleared by a write with the value '1b' to this bit.

**CMD\_ERR**

If the Embedded Flash controller is in [Read Mode](#), [Program Mode](#) or [Erase Mode](#), this bit is set if the [Embedded Flash Command Register](#) is set to any value other than [Standby Mode](#).

This bit is sticky: once set, it remains set until cleared by a write with the value '1b' to this bit.

**PROTECT\_ERR**

If [Boot\\_Lock](#) in the [Embedded Flash Status Register](#) is set and a program operation to an address within the range 0000h - 0FFFh, or a page erase operation to page 0, or a mass erase operation to the main Embedded Flash array occurs, this bit is set. In addition,

This bit is sticky: once set, it remains set until cleared by a write with the value '1b' to this bit.

## 15.11.5 Embedded Flash Configuration Register

**Table 15.10 Embedded Flash Configuration Register**

|               |          |     |     |             |     |           |                     |            |
|---------------|----------|-----|-----|-------------|-----|-----------|---------------------|------------|
| HOST INDEX    | N/A      |     |     | N/A         |     |           | HOST SIZE           |            |
| EC OFFSET     | 110h     |     |     | 32/16/8-bit |     |           | EC SIZE             |            |
| POWER         | VTR      |     |     | 00h         |     |           | nSYS_RST<br>DEFAULT |            |
| BUS           | LPC SPB  |     |     |             |     |           |                     |            |
| BYTE[3:2] BIT | D31      | D30 | D29 | ...         |     | D18       | D17                 | D16        |
| HOST TYPE     | -        | -   | -   | -           | -   | -         | -                   | -          |
| EC TYPE       | R        | R   | R   | R           | R   | R         | R                   | R          |
| BIT NAME      | Reserved |     |     |             |     |           |                     |            |
| BYTE1 BIT     | D15      | D14 | D13 | D12         | D11 | D10       | D9                  | D8         |
| HOST TYPE     | -        | -   | -   | -           | -   | -         | -                   | -          |
| EC TYPE       | R        | R   | R   | R           | R   | R         | R                   | R          |
| BIT NAME      | Reserved |     |     |             |     |           | Prog_Time           |            |
| BYTE0 BIT     | D7       | D6  | D5  | D4          | D3  | D2        | D1                  | D0         |
| HOST TYPE     | -        | -   | -   | -           | -   | -         | -                   | -          |
| EC TYPE       | R        | R   | R/W | R/W         | R/W | R/W       | R/W                 | R/W        |
| BIT NAME      | Reserved |     |     |             |     | Boot_Lock | Host_Ctl            | Reg_Ctl_En |

**Note:** This register is accessible only by the EC.

### REG\_CTL\_EN

When this bit is set, [Reg\\_Ctl](#) of the [Embedded Flash Command Register](#) can be set to 1. When this bit is clear (the default), [Reg\\_Ctl](#) is forced to 0 and cannot be set.

Because this bit overrides any writes to [Reg\\_Ctl](#), EC firmware can clear this bit to prevent the Host from getting access to the Embedded Flash register interface.

### HOST\_CTL

When this bit is set, the [Embedded Flash Address Register](#), the [Embedded Flash Data Register](#) and the [Embedded Flash Command Register](#) can be read and written by the Host via the Flash Memory Mailbox registers in the [Flash Mailbox interface](#). The EC is inhibited from reading or writing these registers. Writes have no effect and all reads return all 0's.

When this bit is clear (the default), these registers can be read and written by the EC. The Host is inhibited from reading or writing these registers. Writes have no effect and all reads return all 0's.

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The [Embedded Flash Status Register](#) is always readable by both the Host and the EC, independent of the state of Host\_Ctl.

**BOOT\_LOCK**

The Boot\_Lock bit permits the EC to lock the Flash boot block when the nFWP input pin is not asserted (see [Table 3.9, "MISC Interface," on page 44](#)). When Boot\_Lock is '1b', the Flash boot block is locked regardless of the state of the nFWP input pin. Any attempt to write data in the address range 00000h through 00FFFh in the Embedded Flash address space will fail and set [Busy](#) in the [Embedded Flash Status Register](#). When Boot\_Lock is '0b' (the default), the Flash boot block is unlocked if the nFWP pin is not asserted.

**PROG\_TIME**

This field determines the length of time the Word Program function takes while in [Program Mode](#).

0: 22  $\mu$ s (default)

1: 26  $\mu$ s

2: 30  $\mu$ s

3: 34  $\mu$ s

**15.11.6 Flash Mailbox Index register****Table 15.11 FL\_MBX\_INDEX Register**

|             |         |        |        |        |        |        |                 |        |
|-------------|---------|--------|--------|--------|--------|--------|-----------------|--------|
| HOST OFFSET | 00h     |        |        | 8-Bit  |        |        | HOST SIZE       |        |
| EC OFFSET   | 00h     |        |        | 8-Bit  |        |        | EC SIZE         |        |
| POWER       | VTR     |        |        | 00h    |        |        | VCC POR DEFAULT |        |
| BUS         | LPC SPB |        |        |        |        |        |                 |        |
| BYTE0 BIT   | D7      | D6     | D5     | D4     | D3     | D2     | D1              | D0     |
| HOST TYPE   | R/W     | R/W    | R/W    | R/W    | R/W    | R/W    | R/W             | R/W    |
| EC TYPE     | -       | -      | -      | -      | -      | -      | -               | -      |
| BIT NAME    | INDEX7  | INDEX6 | INDEX5 | INDEX4 | INDEX3 | INDEX2 | INDEX1          | INDEX0 |



## 15.11.7 Flash Mailbox Data register

**Table 15.12 FL\_MBX\_DATA Register**

|             |         |       |       |       |       |       |       |                    |  |
|-------------|---------|-------|-------|-------|-------|-------|-------|--------------------|--|
| HOST OFFSET | 04h     |       |       |       | 8-Bit |       |       | HOST SIZE          |  |
| EC OFFSET   | 04h     |       |       |       | 8-bit |       |       | EC SIZE            |  |
| POWER       | VTR     |       |       |       | 00h   |       |       | VCC POR<br>DEFAULT |  |
| BUS         | LPC SPB |       |       |       |       |       |       |                    |  |
| BYTE0 BIT   | D7      | D6    | D5    | D4    | D3    | D2    | D1    | D0                 |  |
| HOST TYPE   | R/W     | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   | R/W                |  |
| EC TYPE     | -       | -     | -     | -     | -     | -     | -     | -                  |  |
| BIT NAME    | DATA7   | DATA6 | DATA5 | DATA4 | DATA3 | DATA2 | DATA1 | DATA0              |  |

## 15.12 Embedded Flash Subsystem Revision History

This revision history shows the changes made to this chapter.

**Table 15.13 Embedded Flash Subsystem Chapter Revision History**

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History," on page 539.</a> |              |            |                                                                                                                                                    |                                                                                  |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE       | SECTION/FIGURE/ENTRY                                                                                                                               | CORRECTION                                                                       |
| 1.                                                                                                                                                                                                                                          | 0.4          | 04/24/2007 | <a href="#">Table 15.6</a> ,<br><a href="#">Section 15.11.5</a>                                                                                    | Boot protection enabled on any instruction or data access to ICCM address space. |
| 2.                                                                                                                                                                                                                                          |              |            | <a href="#">Section 15.10</a> ,<br><a href="#">Section 15.10.1</a>                                                                                 | Transfer of control to Host examples changed to handle Host power loss.          |
|                                                                                                                                                                                                                                             |              |            | Global editorial                                                                                                                                   | Replace PCI RESET. PCIRST#, etc. with LRESET#.                                   |
| 3.                                                                                                                                                                                                                                          |              |            | <a href="#">Section 15.3.4, "Tracking Flash Program or Erase Activity," on page 277</a><br><a href="#">Section 15.4, "Interrupts," on page 279</a> | VCC PWRGD and LRESET# Behavior updated<br><br>Clarification of Flash interrupt   |
| 4.                                                                                                                                                                                                                                          |              |            | <a href="#">Section 15.3.2.1, "Clock Idle," on page 277</a>                                                                                        | Added Clock idle description                                                     |
| 5.                                                                                                                                                                                                                                          |              | 5/01/2007  | <a href="#">Section 15.3.4</a><br><a href="#">Section 15.7</a><br><a href="#">Section 15.7.2</a>                                                   | Editorial Changes<br>Global change reference nSYSRST for VTR POR                 |
| 6.                                                                                                                                                                                                                                          | 0.5          | 05/17/2007 |                                                                                                                                                    |                                                                                  |
| 7.                                                                                                                                                                                                                                          | 0.6          | 06/13/2007 | <a href="#">Reg_Ctl bit in Table 15.8, "Embedded Flash Command Register," on page 296</a>                                                          | Corrected bit access type to read/write.                                         |



## Chapter 16 EC Interrupt Aggregator

### 16.1 General Description

MEC5035 Interrupt source and Enable register definitions.

The [EC Interrupt Aggregator](#) block performs the following functions:

- Interrupt Source and Enable register are mapped on the EC SPB Bus
- Priority levels are selectable by firmware.
- Vector Table Base address is programmable.
- Interrupt sources may be level or trigger inputs.

## 16.2 Block Diagram

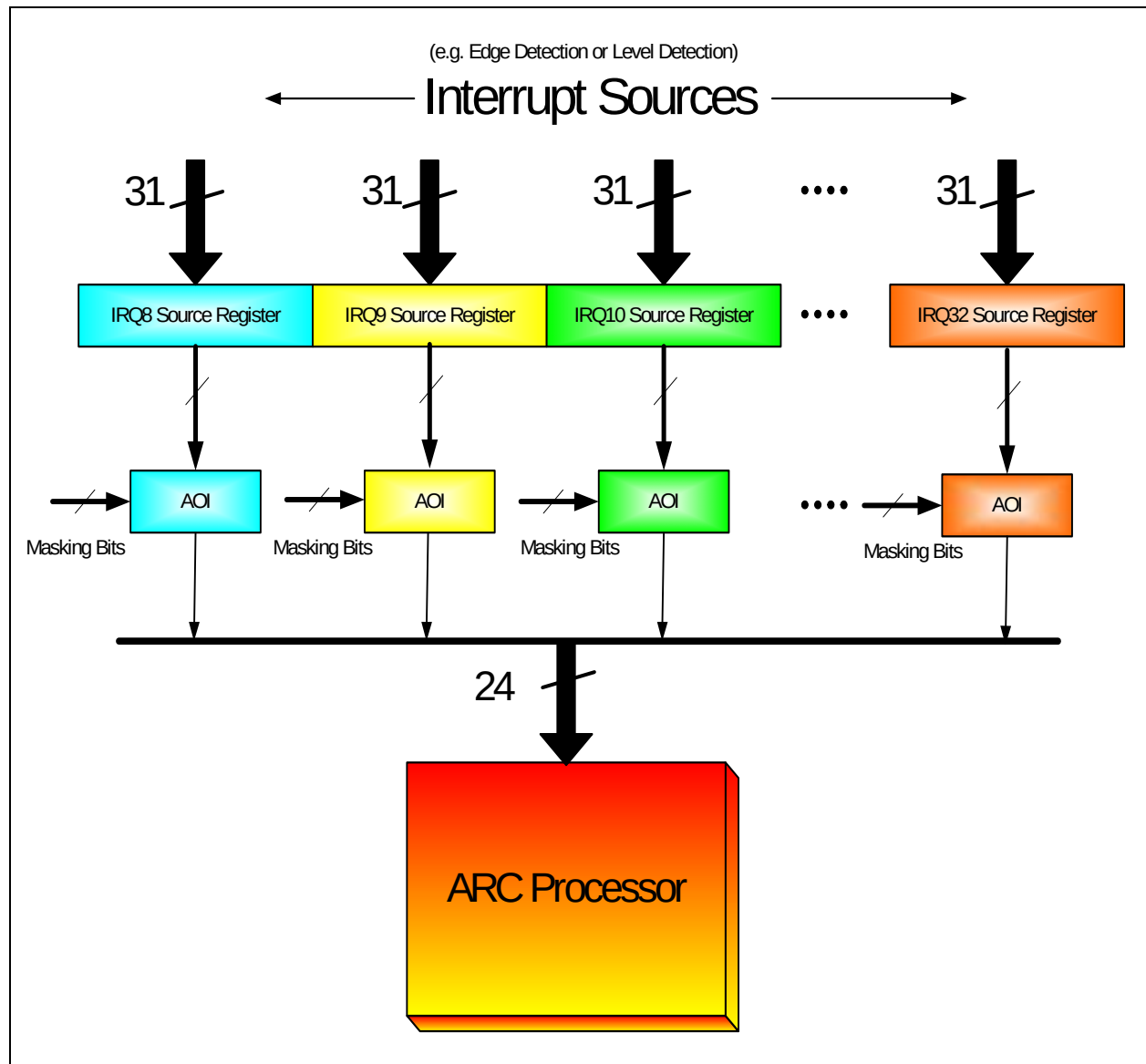


Figure 16.1 ARC Interrupt Generation

## 16.3 Power, Clocks and Reset

### 16.3.1 Power Domain

This block is powered by VTR for wake up capability.

See [Section 4.5, "Power Configuration," on page 96](#) for details on power domains.

### 16.3.2 Clocks

No clock is required for this block

### 16.3.3 Reset

This block is reset by [nSYS\\_RST](#). Following a reset, Interrupt Source, Enable and Result registers default to '0' and all interrupts are Enabled.

See [Section 4.6, "Reset Interface," on page 99](#) for details on reset.

### 16.3.4 Interrupt Routing

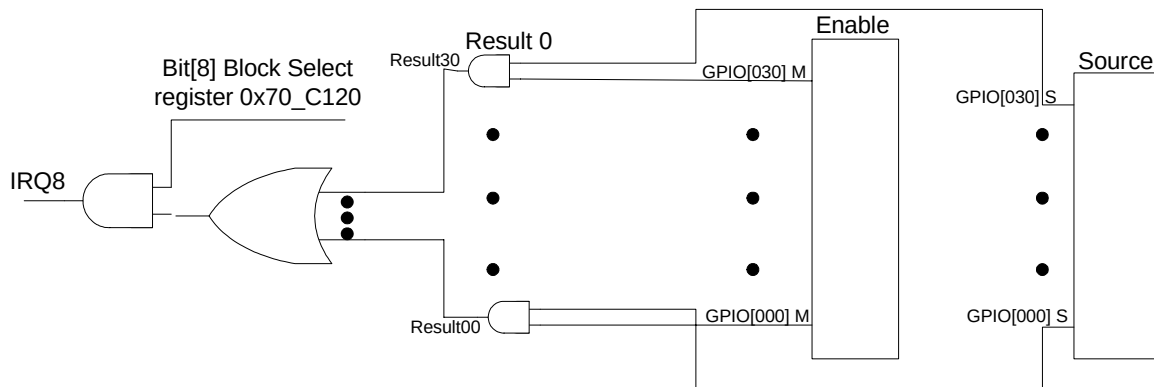


Figure 16.1 GPIO Interrupt Structure

### 16.3.5 WAKE Generation

The [EC Interrupt Aggregator](#) routes logic from WAKE Event Sources to the [WAKE](#) input of the [Power, Clocks and Resets-Power Management Interface](#) to wake the system. This logic requires no clocks.

The interrupt sources AND'd with the corresponding Enable bit will be OR'd to produce a wake event

The wake up sources are identified in a "WAKE" column of the Bit definitions table for each IRQ's Source Register.

## 16.4 Interrupt Summary

ARC International's *ARCompact™ Instruction Set Architecture Programmer's Reference*, March 2005 describes the ARC processor's response to interrupts. [Table 16.1, "EC Interrupt Structure"](#) summarizes the ARC interrupts, priorities and vector locations:

Table 16.1 EC Interrupt Structure

| VECTOR | NAME              | LINK REGISTER | PRIORITY (DEFAULT) | RELATIVE PRIORITY | BYTE OFFSET |
|--------|-------------------|---------------|--------------------|-------------------|-------------|
| 0      | Reset             | -             | High               | H1                | 0x00        |
| 1      | Memory Error      | ILINK2        | High               | H2                | 0x08        |
| 2      | Instruction Error | ILINK2        | High               | H3                | 0x10        |
| 3      | IRQ3-Reserved     | ILINK1        | level 1 (low)      | L27               | 0x18        |
| 4      | IRQ4-Reserved     | ILINK1        | level 1 (low)      | L26               | 0x20        |

Table 16.1 EC Interrupt Structure

| VECTOR | NAME          | LINK REGISTER | PRIORITY (DEFAULT) | RELATIVE PRIORITY | BYTE OFFSET |
|--------|---------------|---------------|--------------------|-------------------|-------------|
| 5      | IRQ5-Reserved | ILINK1        | level 1 (low)      | L25               | 0x28        |
| 6      | IRQ6-Reserved | ILINK2        | level 2 (mid)      | M2                | 0x30        |
| 7      | IRQ7-Reserved | ILINK2        | level 2 (mid)      | M1                | 0x38        |
| 8      | IRQ8          | ILINK1        | level 1 (low)      | L24               | 0x40        |
| 9      | IRQ9          | ILINK1        | level 1 (low)      | L23               | 0x48        |
| 10     | IRQ10         | ILINK1        | level 1 (low)      | L22               | 0x50        |
| 11     | IRQ11         | ILINK1        | level 1 (low)      | L21               | 0x58        |
| 12     | IRQ12         | ILINK1        | level 1 (low)      | L20               | 0x60        |
| 13     | IRQ13         | ILINK1        | level 1 (low)      | L19               | 0x68        |
| 14     | IRQ14         | ILINK1        | level 1 (low)      | L18               | 0x70        |
| 15     | IRQ15         | ILINK1        | level 1 (low)      | L17               | 0x78        |
| 16     | IRQ16         | ILINK1        | level 1 (low)      | L16               | 0x80        |
| 17     | IRQ17         | ILINK1        | level 1 (low)      | L15               | 0x88        |
| 18     | IRQ18         | ILINK1        | level 1 (low)      | L14               | 0x90        |
| 19     | IRQ19         | ILINK1        | level 1 (low)      | L13               | 0x98        |
| 20     | IRQ20         | ILINK1        | level 1 (low)      | L12               | 0xA0        |
| 21     | IRQ21         | ILINK1        | level 1 (low)      | L11               | 0xA8        |
| 22     | IRQ22         | ILINK1        | level 1 (low)      | L10               | 0xB0        |
| 23     | IRQ23         | ILINK1        | level 1 (low)      | L9                | 0xB8        |
| 24     | IRQ24         | ILINK1        | level 1 (low)      | L8                | 0xC0        |
| 25     | IRQ25         | ILINK1        | level 1 (low)      | L7                | 0xC8        |
| 26     | IRQ26         | ILINK1        | level 1 (low)      | L6                | 0xD0        |
| 27     | IRQ27         | ILINK1        | level 1 (low)      | L5                | 0xD8        |
| 28     | IRQ28         | ILINK1        | level 1 (low)      | L4                | 0xE0        |
| 29     | IRQ29         | ILINK1        | level 1 (low)      | L3                | 0xE8        |
| 30     | IRQ30         | ILINK1        | level 1 (low)      | L2                | 0xF0        |
| 31     | IRQ31         | ILINK1        | level 1 (low)      | L1                | 0xF8        |

**Note:** IRQ Vector 31 is the highest L1 Priority

## 16.5 Registers

The [EC Interrupt Aggregator](#) has its own Logical Device Number, and Base Address as indicated in [Table 16.2](#). The Host LPC I/O addresses for the [EC Interrupt Aggregator](#) is selected via Base Address Register (see [Section 6.6.2, "Base Address Registers," on page 144](#)). LPC access to configuration registers is through Host Access Configuration Port (see [Section 6.5.1, "Host Access Port," on page 142](#).)

[Table 16.3](#) is a register summary for the [EC Interrupt Aggregator](#) block.

**Table 16.2 EC Interrupt Aggregator Base Address Table**

| EC Interrupt Aggregator BLOCKS | LDN FROM<br>( <a href="#">Table 7.3 on page 168</a> ) | AHB BASE ADDRESS |
|--------------------------------|-------------------------------------------------------|------------------|
| EC Interrupt Aggregator        | 30h                                                   | F0_C000h         |

[Table 16.3](#) is a register summary for the [EC Interrupt Aggregator](#) block. The LPC I/O address for each Run-Time Register is described below as an offset from its Base Address Register. Each EC address is indicated as an SPB Offset from its AHB base address. Each Configuration register access through the [Host Access Port](#) address via its LND indicated in [Table 16.2 on page 308](#) and its [Host Access Port](#) index which is described as "Host Config Index" in the tables below.



Table 16.3 EC Interrupt Aggregator Register Summary

| REGISTER NAME         | HOST I/O ACCESS |            |           | EC INTERFACE |           |         | NOTES                   |
|-----------------------|-----------------|------------|-----------|--------------|-----------|---------|-------------------------|
|                       | HOST I/O INDEX  | SPB OFFSET | HOST TYPE | SPB OFFSET   | BYTE LANE | EC TYPE | BIT DEFINITIONS         |
| IRQ8 Source Register  | -               | -          | -         | 00h          | 3-0       | R/WC    | Table 16.5 on page 315  |
| IRQ8 Enable Register  | -               | -          | -         | 04h          | 3-0       | R/W     |                         |
| IRQ8 Result Register  | -               | -          | -         | 08h          | 3-0       | R       |                         |
| IRQ9 Source Register  | -               | -          | -         | 0Ch          | 3-0       | R/WC    | Table 16.9 on page 318  |
| IRQ9 Enable Register  | -               | -          | -         | 10h          | 3-0       | R/W     |                         |
| IRQ9 Result Register  | -               | -          | -         | 14h          | 3-0       | R       |                         |
| IRQ10 Source Register | -               | -          | -         | 18h          | 3-0       | R/WC    | Table 16.13 on page 320 |
| IRQ10 Enable Register | -               | -          | -         | 1Ch          | 3-0       | R/W     |                         |
| IRQ10 Result Register | -               | -          | -         | 20h          | 3-0       | R       |                         |
| IRQ11 Source Register | -               | -          | -         | 24h          | 3-0       | R/WC    | Table 16.17 on page 323 |
| IRQ11 Enable Register | -               | -          | -         | 28h          | 3-0       | R/W     |                         |
| IRQ11 Result Register | -               | -          | -         | 2Ch          | 3-0       | R       |                         |
| IRQ12 Source Register | -               | -          | -         | 30h          | 3-0       | R/WC    | Table 16.21 on page 325 |
| IRQ12 Enable Register | -               | -          | -         | 34h          | 3-0       | R/W     |                         |
| IRQ12 Result Register | -               | -          | -         | 38h          | 3-0       | R       |                         |
| IRQ13 Source Register | -               | -          | -         | 3Ch          | 3-0       | R/WC    | Table 16.25 on page 328 |
| IRQ13 Enable Register | -               | -          | -         | 40h          | 3-0       | R/W     |                         |



**Table 16.3 EC Interrupt Aggregator Register Summary**

| REGISTER NAME         | HOST I/O ACCESS |            |           | EC INTERFACE |           |         | NOTES                   |
|-----------------------|-----------------|------------|-----------|--------------|-----------|---------|-------------------------|
|                       | HOST I/O INDEX  | SPB OFFSET | HOST TYPE | SPB OFFSET   | BYTE LANE | EC TYPE | BIT DEFINITIONS         |
| IRQ13 Result Register | -               | -          | -         | 44h          | 3-0       | R       |                         |
| IRQ14 Source Register | -               | -          | -         | 48h          | 3-0       | R/WC    | Table 16.29 on page 330 |
| IRQ14 Enable Register | -               | -          | -         | 4Ch          | 3-0       | R/W     |                         |
| IRQ14 Result Register | -               | -          | -         | 50h          | 3-0       | R       |                         |
| IRQ15 Source Register | -               | -          | -         | 54h          | 3-0       | R/WC    | Table 16.33 on page 332 |
| IRQ15 Enable Register | -               | -          | -         | 58h          | 3-0       | R/W     |                         |
| IRQ15 Result Register | -               | -          | -         | 5Ch          | 3-0       | R       |                         |
| IRQ16 Source Register | -               | -          | -         | 60h          | 3-0       | R/WC    | Table 16.37 on page 334 |
| IRQ16 Enable Register | -               | -          | -         | 64h          | 3-0       | R/W     |                         |
| IRQ16 Result Register | -               | -          | -         | 68h          | 3-0       | R       |                         |
| IRQ17 Source Register | -               | -          | -         | 6Ch          | 3-0       | R/WC    | Table 16.41 on page 336 |
| IRQ17 Enable Register | -               | -          | -         | 70h          | 3-0       | R/W     |                         |
| IRQ17 Result Register | -               | -          | -         | 74h          | 3-0       | R       |                         |
| IRQ18 Source Register | -               | -          | -         | 78h          | 3-0       | R/WC    | Table 16.45 on page 338 |
| IRQ18 Enable Register | -               | -          | -         | 7Ch          | 3-0       | R/W     |                         |
| IRQ18 Result Register | -               | -          | -         | 80h          | 3-0       | R       |                         |
| IRQ19 Source Register | -               | -          | -         | 84h          | 3-0       | R/WC    | Table 16.49 on page 340 |
| IRQ19 Enable Register | -               | -          | -         | 88h          | 3-0       | R/W     |                         |

Table 16.3 [EC Interrupt Aggregator Register Summary](#)

| REGISTER NAME                         | HOST I/O ACCESS |            |           | EC INTERFACE |           |         | NOTES                                   |
|---------------------------------------|-----------------|------------|-----------|--------------|-----------|---------|-----------------------------------------|
|                                       | HOST I/O INDEX  | SPB OFFSET | HOST TYPE | SPB OFFSET   | BYTE LANE | EC TYPE | BIT DEFINITIONS                         |
| <a href="#">IRQ19 Result Register</a> | -               | -          | -         | 8Ch          | 3-0       | R       |                                         |
| <a href="#">IRQ20 Source Register</a> | -               | -          | -         | 90h          | 3-0       | R/WC    | <a href="#">Table 16.53 on page 342</a> |
| <a href="#">IRQ20 Enable Register</a> | -               | -          | -         | 94h          | 3-0       | R/W     |                                         |
| <a href="#">IRQ20 Result Register</a> | -               | -          | -         | 98h          | 3-0       | R       |                                         |
| <a href="#">IRQ21 Source Register</a> | -               | -          | -         | 9Ch          | 3-0       | R/WC    | <a href="#">Table 16.57 on page 344</a> |
| <a href="#">IRQ21 Enable Register</a> | -               | -          | -         | A0h          | 3-0       | R/W     |                                         |
| <a href="#">IRQ21 Result Register</a> | -               | -          | -         | A4h          | 3-0       | R       |                                         |
| <a href="#">IRQ22 Source Register</a> | -               | -          | -         | A8h          | 3-0       | R/WC    | <a href="#">Table 16.61 on page 346</a> |
| <a href="#">IRQ22 Enable Register</a> | -               | -          | -         | ACh          | 3-0       | R/W     |                                         |
| <a href="#">IRQ22 Result Register</a> | -               | -          | -         | B0h          | 3-0       | R       |                                         |
| <a href="#">IRQ23 Source Register</a> | -               | -          | -         | B4h          | 3-0       | R/WC    | <a href="#">Table 16.65 on page 348</a> |
| <a href="#">IRQ23 Enable Register</a> | -               | -          | -         | B8h          | 3-0       | R/W     |                                         |
| <a href="#">IRQ23 Result Register</a> | -               | -          | -         | BCh          | 3-0       | R       |                                         |
| <a href="#">IRQ24 Source Register</a> | -               | -          | -         | C0h          | 3-0       | R/WC    | <a href="#">Table 16.69 on page 350</a> |
| <a href="#">IRQ24 Enable Register</a> | -               | -          | -         | C4h          | 3-0       | R/W     |                                         |
| <a href="#">IRQ24 Result Register</a> | -               | -          | -         | C8h          | 3-0       | R       |                                         |
| <a href="#">IRQ25 Source Register</a> | -               | -          | -         | CCh          | 3-0       | R/WC    | <a href="#">Table 16.73 on page 352</a> |
| <a href="#">IRQ25 Enable Register</a> | -               | -          | -         | D0h          | 3-0       | R/W     |                                         |

**Table 16.3 EC Interrupt Aggregator Register Summary**

| REGISTER NAME         | HOST I/O ACCESS |            |           | EC INTERFACE |           |         | NOTES                                   |
|-----------------------|-----------------|------------|-----------|--------------|-----------|---------|-----------------------------------------|
|                       | HOST I/O INDEX  | SPB OFFSET | HOST TYPE | SPB OFFSET   | BYTE LANE | EC TYPE | BIT DEFINITIONS                         |
| IRQ25 Result Register | -               | -          | -         | D4h          | 3-0       | R       |                                         |
| IRQ26 Source Register | -               | -          | -         | D8h          | 3-0       | R/WC    | <a href="#">Table 16.77 on page 353</a> |
| IRQ26 Enable Register | -               | -          | -         | DCh          | 3-0       | R/W     |                                         |
| IRQ26 Result Register | -               | -          | -         | E0h          | 3-0       | R       |                                         |
| IRQ27 Source Register | -               | -          | -         | E4h          | 3-0       | R/WC    | <a href="#">Table 16.81 on page 355</a> |
| IRQ27 Enable Register | -               | -          | -         | E8h          | 3-0       | R/W     |                                         |
| IRQ27 Result Register | -               | -          | -         | EC           | 3-0       | R       |                                         |
| IRQ28 Source Register | -               | -          | -         | F0h          | 3-0       | R/WC    | <a href="#">Table 16.85 on page 357</a> |

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Table 16.3 EC Interrupt Aggregator Register Summary

| REGISTER NAME         | HOST I/O ACCESS |            |           | EC INTERFACE |           |         | NOTES                   |
|-----------------------|-----------------|------------|-----------|--------------|-----------|---------|-------------------------|
|                       | HOST I/O INDEX  | SPB OFFSET | HOST TYPE | SPB OFFSET   | BYTE LANE | EC TYPE | BIT DEFINITIONS         |
| IRQ28 Enable Register | -               | -          | -         | F4h          | 3-0       | R/W     |                         |
| IRQ28 Result Register | -               | -          | -         | F8h          | 3-0       | R       |                         |
| IRQ29 Source Register | -               | -          | -         | FCh          | 3-0       | R/WC    | Table 16.89 on page 358 |
| IRQ29 Enable Register | -               | -          | -         | 100h         | 3-0       | R/W     |                         |
| IRQ29 Result Register | -               | -          | -         | 104h         | 3-0       | R       |                         |
| IRQ30 Source Register | -               | -          | -         | 108h         | 3-0       | R/WC    | Table 16.93 on page 360 |
| IRQ30 Enable Register | -               | -          | -         | 10Ch         | 3-0       | R/W     |                         |
| IRQ30 Result Register | -               | -          | -         | 110h         | 3-0       | R       |                         |
| IRQ31 Source Register | -               | -          | -         | 114h         | 3-0       | R/WC    | Table 16.97 on page 361 |
| IRQ31 Enable Register | -               | -          | -         | 118h         | 3-0       | R/W     |                         |
| IRQ31 Result Register | -               | -          | -         | 11Ch         | 3-0       | R       |                         |
| Block Select register |                 |            |           | 120h         | 3-0       | R/W     |                         |

**Note 16.2** All Registers listed in Table 16.3 are powered by VTR and reset by nSYS\_RST.

## 16.6 Detailed Description of Accessible Registers

The interrupts consist of a status register, a Enable register and a results register.

The status and Enable are latched registers. The result is a bit by bit and function addressable for reading

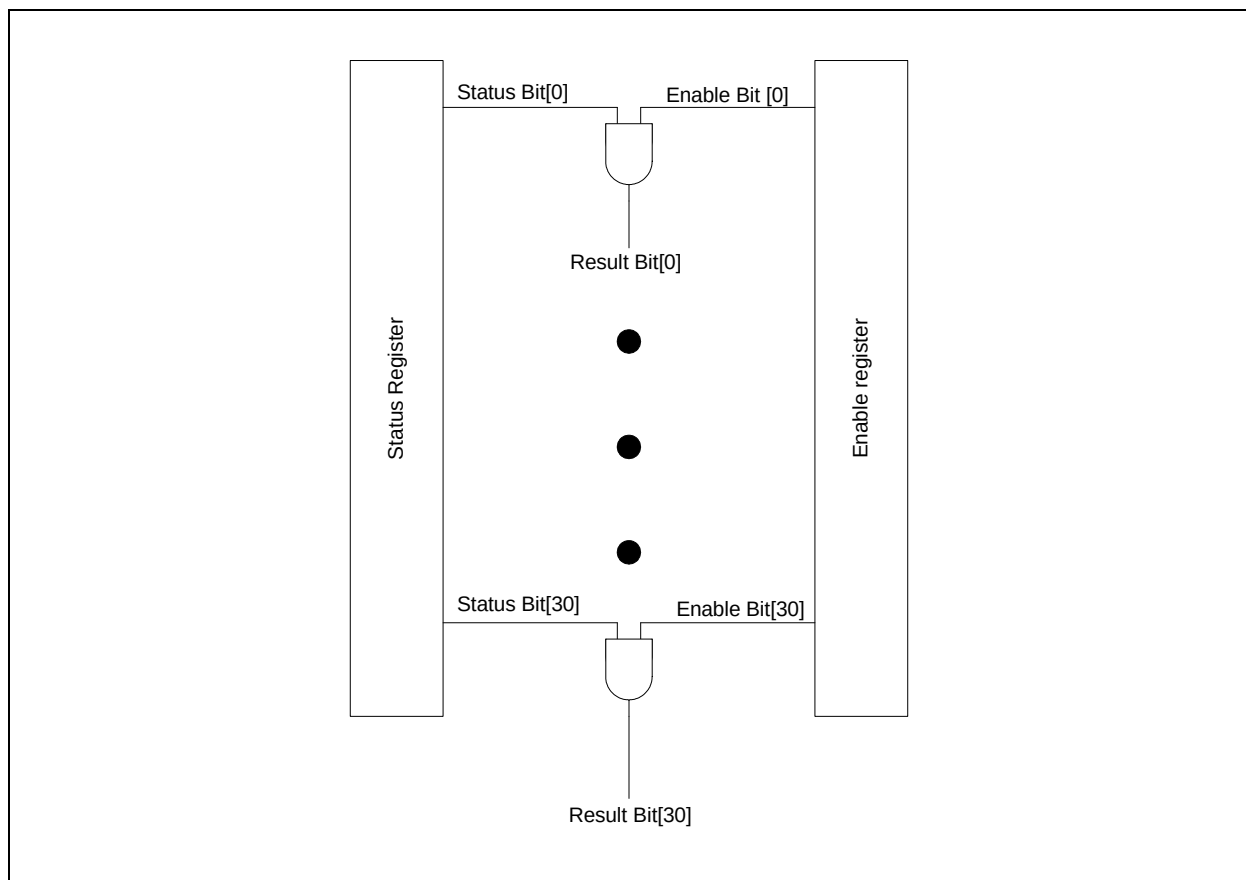


**Figure 16.2 Example of the Results register**

## 16.6.1 IRQ8 Source Register

**Table 16.4 IRQ8 Source Register**

| HOST ADDRESS | N/A      |                                                                                                     |     |   |            |    |    | HOST SIZE           |
|--------------|----------|-----------------------------------------------------------------------------------------------------|-----|---|------------|----|----|---------------------|
| EC OFFSET    | 00h      |                                                                                                     |     |   | 32-bit     |    |    | EC SIZE             |
| POWER        | VTR      |                                                                                                     |     |   | 0000_0000h |    |    | nSYS_RST<br>DEFAULT |
| BUS          | EC SPB   |                                                                                                     |     |   |            |    |    |                     |
| BIT          | D31      | D30                                                                                                 | D29 | ■ | ■          | D2 | D1 | D0                  |
| HOST TYPE    | -        | -                                                                                                   | -   | - | -          | -  | -  | -                   |
| EC TYPE      | R        | RWC except for reserved bits See <a href="#">Table 16.5</a> & <a href="#">Note 16.3 on page 315</a> |     |   |            |    |    |                     |
| BIT NAME     | Reserved | GPIO[140:176]                                                                                       |     |   |            |    |    |                     |

**Table 16.5 Bit definitions IRQ8 Source Register**

| BIT     | EC TYPE | SIGNAL NAME   | WAKE | DESCRIPTION                                                                                                                                                                                                                              |
|---------|---------|---------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:0]   | R/WC    | GPIO[147:140] | Y    | GPIO Interrupt Signal. This bit is set when a interrupt source is triggered. This bit is sticky; once set, it remains set until cleared by a write with the value '1' to this bit. Write to this bit with a value of '0' have no effect. |
| [15:8]  | R/WC    | GPIO[157:150] | Y    |                                                                                                                                                                                                                                          |
| [21:16] | R/WC    | GPIO[165:160] | Y    |                                                                                                                                                                                                                                          |
| [23:22] | R       | GPIO[167:166] | Y    | Reserved                                                                                                                                                                                                                                 |
| [30:24] | R       | GPIO[176:170] | N    | Reserved                                                                                                                                                                                                                                 |
| 31      | R       | Reserved      | N    | This bit is always reserved                                                                                                                                                                                                              |

**Note 16.3** Reserved Bits shown in the Source register are also reserved read only in the Corresponding Enable & Result register/

## 16.6.2 IRQ8 Enable Register

**Table 16.6 IRQ8 Enable Register**

| HOST ADDRESS | N/A      |                                                                                                    |     |                                                                                   |                                                                                     |    |    | HOST SIZE           |  |
|--------------|----------|----------------------------------------------------------------------------------------------------|-----|-----------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|----|----|---------------------|--|
| EC OFFSET    | 04h      |                                                                                                    |     |                                                                                   | 32-bit                                                                              |    |    | EC SIZE             |  |
| POWER        | VTR      |                                                                                                    |     |                                                                                   | 0000_0000h                                                                          |    |    | nSYS_RST<br>DEFAULT |  |
| BUS          | EC SPB   |                                                                                                    |     |                                                                                   |                                                                                     |    |    |                     |  |
| BIT          | D31      | D30                                                                                                | D29 |  |  | D2 | D1 | D0                  |  |
| HOST TYPE    | -        | -                                                                                                  | -   | -                                                                                 | -                                                                                   | -  | -  | -                   |  |
| EC TYPE      | R        | RW except for reserved bits See <a href="#">Table 16.5</a> & <a href="#">Note 16.3 on page 315</a> |     |                                                                                   |                                                                                     |    |    |                     |  |
| BIT NAME     | Reserved | GPIO[140:176]                                                                                      |     |                                                                                   |                                                                                     |    |    |                     |  |

### 16.6.3 IRQ8 Result Register

Table 16.7 IRQ8 Result Register

| HOST ADDRESS | N/A    |               |     |                                                                                   |                                                                                     |    | HOST SIZE           |    |
|--------------|--------|---------------|-----|-----------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|----|---------------------|----|
| EC OFFSET    | 08h    |               |     | 32-bit                                                                            |                                                                                     |    | EC SIZE             |    |
| POWER        | VTR    |               |     | 0000_0000h                                                                        |                                                                                     |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB |               |     |                                                                                   |                                                                                     |    |                     |    |
| BIT          | D31    | D30           | D29 |  |  | D2 | D1                  | D0 |
| HOST TYPE    | -      | -             | -   | -                                                                                 | -                                                                                   | -  | -                   | -  |
| EC TYPE      | R/W    | R             | R   | R                                                                                 | R                                                                                   | R  | R                   | R  |
| BIT NAME     | NORM   | GPIO[140:176] |     |                                                                                   |                                                                                     |    |                     |    |

#### NORM

This bit is a read write bit used by the NORM instruction

### 16.6.4 IRQ9 Source Register

Table 16.8 IRQ9 Source Register

| HOST ADDRESS | N/A      |                                                                                                     |     |                                                                                     |                                                                                       |    | HOST SIZE           |    |
|--------------|----------|-----------------------------------------------------------------------------------------------------|-----|-------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|----|---------------------|----|
| EC OFFSET    | 0Ch      |                                                                                                     |     | 32-bit                                                                              |                                                                                       |    | EC SIZE             |    |
| POWER        | VTR      |                                                                                                     |     | 0000_0000h                                                                          |                                                                                       |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB   |                                                                                                     |     |                                                                                     |                                                                                       |    |                     |    |
| BIT          | D31      | D30                                                                                                 | D29 |  |  | D2 | D1                  | D0 |
| HOST TYPE    | -        | -                                                                                                   | -   | -                                                                                   | -                                                                                     | -  | -                   | -  |
| EC TYPE      | R        | RWC except for reserved bits See <a href="#">Table 16.9</a> & <a href="#">Note 16.3 on page 315</a> |     |                                                                                     |                                                                                       |    |                     |    |
| BIT NAME     | Reserved | GPIO[100:136]                                                                                       |     |                                                                                     |                                                                                       |    |                     |    |



Table 16.9 Bit definitions IRQ9 Source Register

| BIT     | EC TYPE | SIGNAL NAME   | WAKE | DESCRIPTION                                                                                                                                                                                                                              |
|---------|---------|---------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:0]   | R/WC    | GPIO[107:100] | Y    | GPIO Interrupt Signal. This bit is set when a interrupt source is triggered. This bit is sticky; once set, it remains set until cleared by a write with the value '1' to this bit. Write to this bit with a value of '0' have no effect. |
| [15:8]  | R/WC    | GPIO[117:110] | Y    |                                                                                                                                                                                                                                          |
| [23:16] | R/WC    | GPIO[127:120] | Y    |                                                                                                                                                                                                                                          |
| [26:24] | R/WC    | GPIO[132:130] | Y    |                                                                                                                                                                                                                                          |
| [30:27] | R       | GPIO[136:133] | N    | Reserved                                                                                                                                                                                                                                 |
| 31      | R       | Reserved      | N    | This bit is always reserved                                                                                                                                                                                                              |

### 16.6.5 IRQ9 Enable Register

Table 16.10 IRQ9 Enable Register

|              |          |                                                                                                    |     |            |   |    |                     |    |
|--------------|----------|----------------------------------------------------------------------------------------------------|-----|------------|---|----|---------------------|----|
| HOST ADDRESS | N/A      |                                                                                                    |     |            |   |    | HOST SIZE           |    |
| EC OFFSET    | 10h      |                                                                                                    |     | 32-bit     |   |    | EC SIZE             |    |
| POWER        | VTR      |                                                                                                    |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB   |                                                                                                    |     |            |   |    |                     |    |
| BIT          | D31      | D30                                                                                                | D29 | ■          | ■ | D2 | D1                  | D0 |
| HOST TYPE    | -        | -                                                                                                  | -   | -          | - | -  | -                   | -  |
| EC TYPE      | R        | RW except for reserved bits See <a href="#">Table 16.9</a> & <a href="#">Note 16.3 on page 315</a> |     |            |   |    |                     |    |
| BIT NAME     | Reserved | GPIO[100:136]                                                                                      |     |            |   |    |                     |    |

## 16.6.6 IRQ9 Result Register

Table 16.11 IRQ9 Result Register

| HOST ADDRESS | N/A    |               |     |             |             |    | HOST SIZE           |    |
|--------------|--------|---------------|-----|-------------|-------------|----|---------------------|----|
| EC OFFSET    | 14h    |               |     | 32-bit      |             |    | EC SIZE             |    |
| POWER        | VTR    |               |     | 0000_0000h  |             |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB |               |     |             |             |    |                     |    |
| BIT          | D31    | D30           | D29 | <div></div> | <div></div> | D2 | D1                  | D0 |
| HOST TYPE    | -      | -             | -   | -           | -           | -  | -                   | -  |
| EC TYPE      | R/W    | R             | R   | R           | R           | R  | R                   | R  |
| BIT NAME     | NORM   | GPIO[100:136] |     |             |             |    |                     |    |

### NORM

This bit is a read write bit used by the NORM instruction

## 16.6.7 IRQ10 Source Register

**Table 16.12 IRQ10 Source Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |                                                                                   |                                                                                     |    | HOST SIZE           |    |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|-----------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|----|---------------------|----|
| EC OFFSET    | 18h      |                                                                                                      |     | 32-bit                                                                            |                                                                                     |    | EC SIZE             |    |
| POWER        | VTR      |                                                                                                      |     | 0000_0000h                                                                        |                                                                                     |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB   |                                                                                                      |     |                                                                                   |                                                                                     |    |                     |    |
| BIT          | D31      | D30                                                                                                  | D29 |  |  | D2 | D1                  | D0 |
| HOST TYPE    | -        | -                                                                                                    | -   | -                                                                                 | -                                                                                   | -  | -                   | -  |
| EC TYPE      | R        | RWC except for reserved bits See <a href="#">Table 16.13</a> & <a href="#">Note 16.3 on page 315</a> |     |                                                                                   |                                                                                     |    |                     |    |
| BIT NAME     | Reserved | GPIO[040:076]                                                                                        |     |                                                                                   |                                                                                     |    |                     |    |

**Table 16.13 Bit definitions IRQ10 Source Register**

| BIT     | EC TYPE | SIGNAL NAME   | WAKE | DESCRIPTION                                                                                                                                                                                                                              |
|---------|---------|---------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:0]   | R/WC    | GPIO[047:040] | Y    | GPIO Interrupt Signal. This bit is set when a interrupt source is triggered. This bit is sticky; once set, it remains set until cleared by a write with the value '1' to this bit. Write to this bit with a value of '0' have no effect. |
| [15:8]  | R/WC    | GPIO[057:050] | Y    |                                                                                                                                                                                                                                          |
| [23:16] | R/WC    | GPIO[067:060] | Y    |                                                                                                                                                                                                                                          |
| [30:24] | R       | GPIO[076:070] | N    | Reserved                                                                                                                                                                                                                                 |
| 31      | R       | Reserved      | N    | This bit is always reserved                                                                                                                                                                                                              |



## 16.6.8 IRQ10 Enable Register

**Table 16.14 IRQ10 Enable Register**

| HOST ADDRESS | N/A      |                                                                                                     |     |   |   |            |    | HOST SIZE           |
|--------------|----------|-----------------------------------------------------------------------------------------------------|-----|---|---|------------|----|---------------------|
| EC OFFSET    | 1Ch      |                                                                                                     |     |   |   | 32-bit     |    | EC SIZE             |
| POWER        | VTR      |                                                                                                     |     |   |   | 0000_0000h |    | nSYS_RST<br>DEFAULT |
| BUS          | EC SPB   |                                                                                                     |     |   |   |            |    |                     |
| BIT          | D31      | D30                                                                                                 | D29 |   |   | D2         | D1 | D0                  |
| HOST TYPE    | -        | -                                                                                                   | -   | - | - | -          | -  | -                   |
| EC TYPE      | R        | RW except for reserved bits See <a href="#">Table 16.13</a> & <a href="#">Note 16.3 on page 315</a> |     |   |   |            |    |                     |
| BIT NAME     | Reserved | GPIO[040:076]                                                                                       |     |   |   |            |    |                     |

## 16.6.9 IRQ10 Result Register

**Table 16.15 IRQ10 Result Register**

| HOST ADDRESS | N/A    |               |     |                                                                                   |                                                                                     |    | HOST SIZE           |    |
|--------------|--------|---------------|-----|-----------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|----|---------------------|----|
| EC OFFSET    | 20h    |               |     | 32-bit                                                                            |                                                                                     |    | EC SIZE             |    |
| POWER        | VTR    |               |     | 0000_0000h                                                                        |                                                                                     |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB |               |     |                                                                                   |                                                                                     |    |                     |    |
| BIT          | D31    | D30           | D29 |  |  | D2 | D1                  | D0 |
| HOST TYPE    | -      | -             | -   | -                                                                                 | -                                                                                   | -  | -                   | -  |
| EC TYPE      | R/W    | R             | R   | R                                                                                 | R                                                                                   | R  | R                   | R  |
| BIT NAME     | NORM   | GPIO[040:076] |     |                                                                                   |                                                                                     |    |                     |    |

### NORM

This bit is a read write bit used by the NORM instruction.

## 16.6.10 IRQ11 Source Register

**Table 16.16 IRQ11 Source Register**

|              |          |                                                                                                      |     |            |   |    |                     |    |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|------------|---|----|---------------------|----|
| HOST ADDRESS | N/A      |                                                                                                      |     |            |   |    | HOST SIZE           |    |
| EC OFFSET    | 24h      |                                                                                                      |     | 32-bit     |   |    | EC SIZE             |    |
| POWER        | VTR      |                                                                                                      |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB   |                                                                                                      |     |            |   |    |                     |    |
| BIT          | D31      | D30                                                                                                  | D29 | ■          | ■ | D2 | D1                  | D0 |
| HOST TYPE    | -        | -                                                                                                    | -   | -          | - | -  | -                   | -  |
| EC TYPE      | R        | RWC except for reserved bits See <a href="#">Table 16.17</a> & <a href="#">Note 16.3 on page 315</a> |     |            |   |    |                     |    |
| BIT NAME     | Reserved | GPIO[000:036]                                                                                        |     |            |   |    |                     |    |

Table 16.17 Bit definitions IRQ11 Source Register

| BIT     | EC TYPE | SIGNAL NAME   | WAKE | DESCRIPTION                                                                                                                                                                                                                              |
|---------|---------|---------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:0]   | R/WC    | GPIO[007:000] | Y    | GPIO Interrupt Signal. This bit is set when a interrupt source is triggered. This bit is sticky; once set, it remains set until cleared by a write with the value '1' to this bit. Write to this bit with a value of '0' have no effect. |
| [15:8]  | R/WC    | GPIO[017:010] | Y    |                                                                                                                                                                                                                                          |
| [23:16] | R/WC    | GPIO[027:020] | Y    |                                                                                                                                                                                                                                          |
| [26:24] | R/WC    | GPIO[032:030] | Y    |                                                                                                                                                                                                                                          |
| [30:27] | R       | GPIO[036:033] | N    | Reserved                                                                                                                                                                                                                                 |
| 31      | R       | Reserved      | N    | This bit is always reserved                                                                                                                                                                                                              |

### 16.6.11 IRQ11 Enable Register

Table 16.18 IRQ11 Enable Register

| HOST ADDRESS | N/A      |                                                                                                     |     |                                                                                     |                                                                                       |    | HOST SIZE           |    |
|--------------|----------|-----------------------------------------------------------------------------------------------------|-----|-------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|----|---------------------|----|
| EC OFFSET    | 28h      |                                                                                                     |     | 32-bit                                                                              |                                                                                       |    | EC SIZE             |    |
| POWER        | VTR      |                                                                                                     |     | 0000_0000h                                                                          |                                                                                       |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB   |                                                                                                     |     |                                                                                     |                                                                                       |    |                     |    |
| BIT          | D31      | D30                                                                                                 | D29 |  |  | D2 | D1                  | D0 |
| HOST TYPE    | -        | -                                                                                                   | -   | -                                                                                   | -                                                                                     | -  | -                   | -  |
| EC TYPE      | R        | RW except for reserved bits See <a href="#">Table 16.17</a> & <a href="#">Note 16.3 on page 315</a> |     |                                                                                     |                                                                                       |    |                     |    |
| BIT NAME     | Reserved | GPIO[000:036]                                                                                       |     |                                                                                     |                                                                                       |    |                     |    |



## 16.6.12 IRQ11 Result Register

**Table 16.19 IRQ11 Result Register**

| HOST ADDRESS | N/A    |               |     |            |   |    | HOST SIZE           |    |
|--------------|--------|---------------|-----|------------|---|----|---------------------|----|
| EC OFFSET    | 2Ch    |               |     | 32-bit     |   |    | EC SIZE             |    |
| POWER        | VTR    |               |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB |               |     |            |   |    |                     |    |
| BIT          | D31    | D30           | D29 | ■          | ■ | D2 | D1                  | D0 |
| HOST TYPE    | -      | -             | -   | -          | - | -  | -                   | -  |
| EC TYPE      | R/W    | R             | R   | R          | R | R  | R                   | R  |
| BIT NAME     | NORM   | GPIO[000:036] |     |            |   |    |                     |    |

**NORM**

This bit is a read write bit used by the NORM instruction.

## 16.6.13 IRQ12 Source Register

**Table 16.20 IRQ12 Source Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |   |            |    |    | HOST SIZE           |  |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|---|------------|----|----|---------------------|--|
| EC OFFSET    | 30h      |                                                                                                      |     |   | 32-bit     |    |    | EC SIZE             |  |
| POWER        | VTR      |                                                                                                      |     |   | 0000_0000h |    |    | nSYS_RST<br>DEFAULT |  |
| BUS          | EC SPB   |                                                                                                      |     |   |            |    |    |                     |  |
| BIT          | D31      | D30                                                                                                  | D29 | ■ | ■          | D2 | D1 | D0                  |  |
| HOST TYPE    | -        | -                                                                                                    | -   | - | -          | -  | -  | -                   |  |
| EC TYPE      | R        | RWC except for reserved bits See <a href="#">Table 16.21</a> & <a href="#">Note 16.3 on page 315</a> |     |   |            |    |    |                     |  |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.21</a> , “Bit definitions IRQ12 Source Register,” on page 325          |     |   |            |    |    |                     |  |

**Table 16.21 Bit definitions IRQ12 Source Register**

| BIT | SIGNAL NAME | WAKE | DESCRIPTION                                                                                                                               |
|-----|-------------|------|-------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | SMB1        | N    | I2C/SMBus controller 1 interrupt. This interrupt is signaled when the I2C/SMBus controller 1 asserts its interrupt request                |
| 1   | SMB2        | N    | I2C/SMBus controller 2 interrupt. This interrupt is signaled when the I2C/SMBus controller 2 asserts its interrupt request                |
| 2   | I2C1A WK    | Y    | I2C/SMBus controller 1A Wake interrupt. This interrupt is signaled when the I2C/SMBus controller 1 asserts its wake up interrupt request. |
| 3   | I2C1B WK    | Y    | I2C/SMBus controller 1B Wake interrupt. This interrupt is signaled when the I2C/SMBus controller 2 asserts its wake up interrupt request. |
| 4   | I2C1C WK    | Y    | I2C/SMBus controller 1C Wake interrupt. This interrupt is signaled when the I2C/SMBus controller 1 asserts its wake up interrupt request. |
| 5   | I2C1D WK    | Y    | I2C/SMBus controller 1D Wake interrupt. This interrupt is signaled when the I2C/SMBus controller 1 asserts its wake up interrupt request. |
| 6   | I2C1E WK    | Y    | I2C/SMBus controller 1E Wake interrupt. This interrupt is signaled when the I2C/SMBus controller 1 asserts its wake up interrupt request. |
| 7   | I2C1F WK    | Y    | I2C/SMBus controller 1F Wake interrupt. This interrupt is signaled when the I2C/SMBus controller 1 asserts its wake up interrupt request. |
| 8   | I2C1G WK    | Y    | I2C/SMBus controller 1G Wake interrupt. This interrupt is signaled when the I2C/SMBus controller 1 asserts its wake up interrupt request. |



**Table 16.21 Bit definitions IRQ12 Source Register**

| BIT   | SIGNAL NAME | WAKE | DESCRIPTION                                                                                                                               |
|-------|-------------|------|-------------------------------------------------------------------------------------------------------------------------------------------|
| 9     | I2C1H WK    | Y    | I2C/SMBus controller 1H Wake interrupt. This interrupt is signaled when the I2C/SMBus controller 1 asserts its wake up interrupt request. |
| 10    | I2C1J WK    | Y    | I2C/SMBus controller 1J Wake interrupt. This interrupt is signaled when the I2C/SMBus controller 1 asserts its wake up interrupt request. |
| 11    | I2C1K WK    | Y    | I2C/SMBus controller 1K Wake interrupt. This interrupt is signaled when the I2C/SMBus controller 1 asserts its wake up interrupt request. |
| 12    | I2C2A WK    | Y    | I2C/SMBus controller 2A Wake interrupt. This interrupt is signaled when the I2C/SMBus controller 1 asserts its wake up interrupt request. |
| 13    | I2C2B WK    | Y    | I2C/SMBus controller 2B Wake interrupt. This interrupt is signaled when the I2C/SMBus controller 1 asserts its wake up interrupt request. |
| 14    | I2C2C WK    | Y    | I2C/SMBus controller 2C Wake interrupt. This interrupt is signaled when the I2C/SMBus controller 1 asserts its wake up interrupt request. |
| 15    | I2C2D WK    | Y    | I2C/SMBus controller 2D Wake interrupt. This interrupt is signaled when the I2C/SMBus controller 1 asserts its wake up interrupt request. |
| 30-16 | Reserved    | N    | Reserved                                                                                                                                  |
| 31    | Reserved    | N    | This bit is always reserved                                                                                                               |

**Note 16.4** Source bits have corresponding Enable and Result bits.

## 16.6.14 IRQ12 Enable Register

**Table 16.22 IRQ12 Enable Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |            |   |    | HOST SIZE           |    |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|------------|---|----|---------------------|----|
| EC OFFSET    | 34h      |                                                                                                      |     | 32-bit     |   |    | EC SIZE             |    |
| POWER        | VTR      |                                                                                                      |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB   |                                                                                                      |     |            |   |    |                     |    |
| BIT          | D31      | D30                                                                                                  | D29 | ■          | ■ | D2 | D1                  | D0 |
| HOST TYPE    | -        | -                                                                                                    | -   | -          | - | -  | -                   | -  |
| EC TYPE      | R        | R/W except for reserved bits See <a href="#">Table 16.21</a> & <a href="#">Note 16.3 on page 315</a> |     |            |   |    |                     |    |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.21</a> , “Bit definitions IRQ12 Source Register,” on page 325          |     |            |   |    |                     |    |

## 16.6.15 IRQ12 Result Register

**Table 16.23 IRQ12 Result Register**

| HOST ADDRESS | N/A    |                                                                                             |     |                                                                                     |                                                                                       |    | HOST SIZE           |    |
|--------------|--------|---------------------------------------------------------------------------------------------|-----|-------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|----|---------------------|----|
| EC OFFSET    | 38h    |                                                                                             |     | 32-bit                                                                              |                                                                                       |    | EC SIZE             |    |
| POWER        | VTR    |                                                                                             |     | 0000_0000h                                                                          |                                                                                       |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB |                                                                                             |     |                                                                                     |                                                                                       |    |                     |    |
| BIT          | D31    | D30                                                                                         | D29 |  |  | D2 | D1                  | D0 |
| HOST TYPE    | -      | -                                                                                           | -   | -                                                                                   | -                                                                                     | -  | -                   | -  |
| EC TYPE      | R/W    | R                                                                                           | R   | R                                                                                   | R                                                                                     | R  | R                   | R  |
| BIT NAME     | NORM   | Refer to <a href="#">Table 16.21</a> , “Bit definitions IRQ12 Source Register,” on page 325 |     |                                                                                     |                                                                                       |    |                     |    |

### NORM

This bit is a read write bit used by the NORM instruction.

## 16.6.16 IRQ13 Source Register

**Table 16.24 IRQ13 Source Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |            |   |    | HOST SIZE           |    |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|------------|---|----|---------------------|----|
| EC OFFSET    | 3Ch      |                                                                                                      |     | 32-bit     |   |    | EC SIZE             |    |
| POWER        | VTR      |                                                                                                      |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB   |                                                                                                      |     |            |   |    |                     |    |
| BIT          | D31      | D30                                                                                                  | D29 | ■          | ■ | D2 | D1                  | D0 |
| HOST TYPE    | -        | -                                                                                                    | -   | -          | - | -  | -                   | -  |
| EC TYPE      | R        | RWC except for reserved bits See <a href="#">Table 16.25</a> & <a href="#">Note 16.3</a> on page 315 |     |            |   |    |                     |    |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.25</a> , “Bit definitions IRQ13 Source Register,” on page 328          |     |            |   |    |                     |    |

**Table 16.25 Bit definitions IRQ13 Source Register**

| BIT  | SIGNAL NAME | WAKE | DESCRIPTION                 |
|------|-------------|------|-----------------------------|
| 0    | PM1_CTL2    | N    | PM1_CTL2 written by Host    |
| 1    | PM1_EN2     | N    | PM1_EN2 written by Host     |
| 2    | PM1_STS2    | N    | PM1_STS2 written by Host    |
| 30-3 | Reserved    | N    | Reserved                    |
| 31   | Reserved    | N    | This bit is always reserved |

**Note 16.5** Source bits have corresponding Enable and Result bits.

**16.6.17 IRQ13 Enable Register****Table 16.26 IRQ13 Enable Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |            |   |    | HOST SIZE           |    |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|------------|---|----|---------------------|----|
| EC OFFSET    | 40h      |                                                                                                      |     | 32-bit     |   |    | EC SIZE             |    |
| POWER        | VTR      |                                                                                                      |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB   |                                                                                                      |     |            |   |    |                     |    |
| BIT          | D31      | D30                                                                                                  | D29 | ■          | ■ | D2 | D1                  | D0 |
| HOST TYPE    | -        | -                                                                                                    | -   | -          | - | -  | -                   | -  |
| EC TYPE      | R/W      | R/W except for reserved bits See <a href="#">Table 16.25</a> & <a href="#">Note 16.3</a> on page 315 |     |            |   |    |                     |    |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.25</a> , “Bit definitions IRQ13 Source Register,” on page 328          |     |            |   |    |                     |    |

**16.6.18 IRQ13 Result Register****Table 16.27 IRQ13 Result Register**

| HOST ADDRESS | N/A    |                                                                                             |     |                                                                                     |                                                                                       |    | HOST SIZE           |    |
|--------------|--------|---------------------------------------------------------------------------------------------|-----|-------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|----|---------------------|----|
| EC OFFSET    | 44h    |                                                                                             |     | 32-bit                                                                              |                                                                                       |    | EC SIZE             |    |
| POWER        | VTR    |                                                                                             |     | 0000_0000h                                                                          |                                                                                       |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB |                                                                                             |     |                                                                                     |                                                                                       |    |                     |    |
| BIT          | D31    | D30                                                                                         | D29 |  |  | D2 | D1                  | D0 |
| HOST TYPE    | -      | -                                                                                           | -   | -                                                                                   | -                                                                                     | -  | -                   | -  |
| EC TYPE      | R/W    | R                                                                                           | R   | R                                                                                   | R                                                                                     | R  | R                   | R  |
| BIT NAME     | NORM   | Refer to <a href="#">Table 16.25</a> , “Bit definitions IRQ13 Source Register,” on page 328 |     |                                                                                     |                                                                                       |    |                     |    |

**NORM**

This bit is a read write bit used by the NORM instruction.

## 16.6.19 IRQ14 Source Register

**Table 16.28 IRQ14 Source Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |            |   |    | HOST SIZE           |    |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|------------|---|----|---------------------|----|
| EC OFFSET    | 48h      |                                                                                                      |     | 32-bit     |   |    | EC SIZE             |    |
| POWER        | VTR      |                                                                                                      |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB   |                                                                                                      |     |            |   |    |                     |    |
| BIT          | D31      | D30                                                                                                  | D29 | ■          | ■ | D2 | D1                  | D0 |
| HOST TYPE    | -        | -                                                                                                    | -   | -          | - | -  | -                   | -  |
| EC TYPE      | R        | RWC except for reserved bits See <a href="#">Table 16.29</a> & <a href="#">Note 16.3 on page 315</a> |     |            |   |    |                     |    |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.29, “Bit definitions IRQ14 Source Register,” on page 330</a>           |     |            |   |    |                     |    |

**Table 16.29 Bit definitions IRQ14 Source Register**

| BIT  | SIGNAL NAME | WAKE | DESCRIPTION                 |
|------|-------------|------|-----------------------------|
| 30-0 | Reserved    | N    | Reserved                    |
| 31   | Reserved    | N    | This bit is always reserved |

**Note 16.6** Source bits have corresponding Enable and Result bits.

## 16.6.20 IRQ14 Enable Register

**Table 16.30 IRQ14 Enable Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |            |   |    | HOST SIZE           |    |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|------------|---|----|---------------------|----|
| EC OFFSET    | 4Ch      |                                                                                                      |     | 32-bit     |   |    | EC SIZE             |    |
| POWER        | VTR      |                                                                                                      |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB   |                                                                                                      |     |            |   |    |                     |    |
| BIT          | D31      | D30                                                                                                  | D29 | ■          | ■ | D2 | D1                  | D0 |
| HOST TYPE    | -        | -                                                                                                    | -   | -          | - | -  | -                   | -  |
| EC TYPE      | R        | R/W except for reserved bits See <a href="#">Table 16.29</a> & <a href="#">Note 16.3 on page 315</a> |     |            |   |    |                     |    |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.29</a> , “Bit definitions IRQ14 Source Register,” on page 330          |     |            |   |    |                     |    |

## 16.6.21 IRQ14 Result Register

**Table 16.31 IRQ14 Result Register**

| HOST ADDRESS | N/A    |                                                                                             |     |            |   |    | HOST SIZE           |    |
|--------------|--------|---------------------------------------------------------------------------------------------|-----|------------|---|----|---------------------|----|
| EC OFFSET    | 50h    |                                                                                             |     | 32-bit     |   |    | EC SIZE             |    |
| POWER        | VTR    |                                                                                             |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB |                                                                                             |     |            |   |    |                     |    |
| BIT          | D31    | D30                                                                                         | D29 | ■          | ■ | D2 | D1                  | D0 |
| HOST TYPE    | -      | -                                                                                           | -   | -          | - | -  | -                   | -  |
| EC TYPE      | R/W    | R                                                                                           | R   | R          | R | R  | R                   | R  |
| BIT NAME     | NORM   | Refer to <a href="#">Table 16.29</a> , “Bit definitions IRQ14 Source Register,” on page 330 |     |            |   |    |                     |    |

### NORM

This bit is a read write bit used by the NORM instruction.

## 16.6.22 IRQ15 Source Register

**Table 16.32 IRQ15 Source Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |            |   |    | HOST SIZE           |    |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|------------|---|----|---------------------|----|
| EC OFFSET    | 54h      |                                                                                                      |     | 32-bit     |   |    | EC SIZE             |    |
| POWER        | VTR      |                                                                                                      |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB   |                                                                                                      |     |            |   |    |                     |    |
| BIT          | D31      | D30                                                                                                  | D29 | ■          | ■ | D2 | D1                  | D0 |
| HOST TYPE    | -        | -                                                                                                    | -   | -          | - | -  | -                   | -  |
| EC TYPE      | R        | RWC except for reserved bits See <a href="#">Table 16.33</a> & <a href="#">Note 16.3</a> on page 315 |     |            |   |    |                     |    |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.33</a> , “Bit definition IRQ15 source Register,” on page 332           |     |            |   |    |                     |    |

**Table 16.33 Bit definition IRQ15 source Register**

| BIT  | SIGNAL NAME       | WAKE | DESCRIPTION                                                                          |
|------|-------------------|------|--------------------------------------------------------------------------------------|
| 0    | LPCPD#            | Y    | LPC Power Down pin state                                                             |
| 1    | LRESET#           | Y    | LRESET Interrupt. This interrupt is signaled when LRESET is asserted.                |
| 2    | LPC_AHB_ERR       | N    | either a LPC BAR conflict or an AHB bus error occurred as a result of an LPC access. |
| 3    | SPI_TXBE_GP       | N    | General Purpose SPI controller Transmit Buffer Empty Interrupt                       |
| 4    | SPI_RXBF_GP       | N    | General Purpose SPI controller Receive Buffer Full Interrupt                         |
| 5    | FLASH_BUSY_ERR    | N    | Embedded Flash Error                                                                 |
| 6    | FLASH_CMD_ERR     | N    | Embedded Flash Error                                                                 |
| 7    | FLASH_PROTECT_ERR | N    | Embedded Flash Error                                                                 |
| 8    | FLASH_EC_INT      | N    | Host-to-EC Interrupt that transfers control of the Flash to the EC                   |
| 30-9 | Reserved          | N    | Reserved                                                                             |
| 31   | Reserved          | N    | This bit is always reserved                                                          |

**Note 16.7** Source bits have corresponding Enable and Result bits.

## 16.6.23 IRQ15 Enable Register

**Table 16.34 IRQ15 Enable Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |                                                                                   |                                                                                     |    | HOST SIZE           |    |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|-----------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|----|---------------------|----|
| EC OFFSET    | 58h      |                                                                                                      |     | 32-bit                                                                            |                                                                                     |    | EC SIZE             |    |
| POWER        | VTR      |                                                                                                      |     | 0000_0000h                                                                        |                                                                                     |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB   |                                                                                                      |     |                                                                                   |                                                                                     |    |                     |    |
| BIT          | D31      | D30                                                                                                  | D29 |  |  | D2 | D1                  | D0 |
| HOST TYPE    | -        | -                                                                                                    | -   | -                                                                                 | -                                                                                   | -  | -                   | -  |
| EC TYPE      | R        | R/W except for reserved bits See <a href="#">Table 16.33</a> & <a href="#">Note 16.3</a> on page 315 |     |                                                                                   |                                                                                     |    |                     |    |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.33</a> , “Bit definition IRQ15 source Register,” on page 332           |     |                                                                                   |                                                                                     |    |                     |    |

## 16.6.24 IRQ15 Result Register

**Table 16.35 IRQ15 Result Register**

| HOST ADDRESS | N/A    |                                                                                           |     |            |   |    | HOST SIZE           |    |
|--------------|--------|-------------------------------------------------------------------------------------------|-----|------------|---|----|---------------------|----|
| EC OFFSET    | 5Ch    |                                                                                           |     | 32-bit     |   |    | EC SIZE             |    |
| POWER        | VTR    |                                                                                           |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB |                                                                                           |     |            |   |    |                     |    |
| BIT          | D31    | D30                                                                                       | D29 | ■          | ■ | D2 | D1                  | D0 |
| HOST TYPE    | -      | -                                                                                         | -   | -          | - | -  | -                   | -  |
| EC TYPE      | R/W    | R                                                                                         | R   | R          | R | R  | R                   | R  |
| BIT NAME     | NORM   | Refer to <a href="#">Table 16.33, “Bit definition IRQ15 source Register,” on page 332</a> |     |            |   |    |                     |    |

### NORM

This bit is a read write bit used by the NORM instruction.



## 16.6.25 IRQ16 Source Register

**Table 16.36 IRQ16 Source Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |            |   |    | HOST SIZE           |    |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|------------|---|----|---------------------|----|
| EC OFFSET    | 60h      |                                                                                                      |     | 32-bit     |   |    | EC SIZE             |    |
| POWER        | VTR      |                                                                                                      |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB   |                                                                                                      |     |            |   |    |                     |    |
| BIT          | D31      | D30                                                                                                  | D29 | ■          | ■ | D2 | D1                  | D0 |
| HOST TYPE    | -        | -                                                                                                    | -   | -          | - | -  | -                   | -  |
| EC TYPE      | R        | RWC except for reserved bits See <a href="#">Table 16.37</a> & <a href="#">Note 16.3 on page 315</a> |     |            |   |    |                     |    |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.37</a> , “Bit definition IRQ16 source Register,” on page 334           |     |            |   |    |                     |    |

**Table 16.37 Bit definition IRQ16 source Register**

| BIT  | SIGNAL NAME | WAKE | DESCRIPTION                 |
|------|-------------|------|-----------------------------|
| 30-0 | Reserved    | N    | Reserved                    |
| 31   | Reserved    | N    | This bit is always reserved |

**Note 16.8** Source bits have corresponding Enable and Result bits.

## 16.6.26 IRQ16 Enable Register

**Table 16.38 IRQ16 Enable Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |            |   |    | HOST SIZE           |    |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|------------|---|----|---------------------|----|
| EC OFFSET    | 64h      |                                                                                                      |     | 32-bit     |   |    | EC SIZE             |    |
| POWER        | VTR      |                                                                                                      |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB   |                                                                                                      |     |            |   |    |                     |    |
| BIT          | D31      | D30                                                                                                  | D29 | ■          | ■ | D2 | D1                  | D0 |
| HOST TYPE    | -        | -                                                                                                    | -   | -          | - | -  | -                   | -  |
| EC TYPE      | R        | R/W except for reserved bits See <a href="#">Table 16.37</a> & <a href="#">Note 16.3</a> on page 315 |     |            |   |    |                     |    |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.37</a> , “Bit definition IRQ16 source Register,” on page 334           |     |            |   |    |                     |    |

## 16.6.27 IRQ16 Result Register

**Table 16.39 IRQ16 Result Register**

| HOST ADDRESS | N/A    |                                                                                            |     |                                                                                     |                                                                                       |    | HOST SIZE           |    |
|--------------|--------|--------------------------------------------------------------------------------------------|-----|-------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|----|---------------------|----|
| EC OFFSET    | 68h    |                                                                                            |     | 32-bit                                                                              |                                                                                       |    | EC SIZE             |    |
| POWER        | VTR    |                                                                                            |     | 0000_0000h                                                                          |                                                                                       |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB |                                                                                            |     |                                                                                     |                                                                                       |    |                     |    |
| BIT          | D31    | D30                                                                                        | D29 |  |  | D2 | D1                  | D0 |
| HOST TYPE    | -      | -                                                                                          | -   | -                                                                                   | -                                                                                     | -  | -                   | -  |
| EC TYPE      | R/W    | R                                                                                          | R   | R                                                                                   | R                                                                                     | R  | R                   | R  |
| BIT NAME     | NORM   | Refer to <a href="#">Table 16.37</a> , “Bit definition IRQ16 source Register,” on page 334 |     |                                                                                     |                                                                                       |    |                     |    |

### NORM

This bit is a read write bit used by the NORM instruction.

## 16.6.28 IRQ17 Source Register

**Table 16.40 IRQ17 Source Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |                                                                                   |                                                                                    |    | HOST SIZE           |    |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|-----------------------------------------------------------------------------------|------------------------------------------------------------------------------------|----|---------------------|----|
| EC OFFSET    | 6Ch      |                                                                                                      |     | 32-bit                                                                            |                                                                                    |    | EC SIZE             |    |
| POWER        | VTR      |                                                                                                      |     | 0000_0000h                                                                        |                                                                                    |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB   |                                                                                                      |     |                                                                                   |                                                                                    |    |                     |    |
| BIT          | D31      | D30                                                                                                  | D29 |  |  | D2 | D1                  | D0 |
| HOST TYPE    | -        | -                                                                                                    | -   | -                                                                                 | -                                                                                  | -  | -                   | -  |
| EC TYPE      | R        | RWC except for reserved bits See <a href="#">Table 16.41</a> & <a href="#">Note 16.3</a> on page 315 |     |                                                                                   |                                                                                    |    |                     |    |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.41</a> , “Bit definition IRQ17 source Register,” on page 336           |     |                                                                                   |                                                                                    |    |                     |    |

**Table 16.41 Bit definition IRQ17 source Register**

| BIT  | SIGNAL NAME | WAKE | DESCRIPTION                             |
|------|-------------|------|-----------------------------------------|
| 0    | UART_RX     | N    | UART Interrupt                          |
| 1    | MBX         | N    | Mailbox Register Interface EC Interrupt |
| 30-2 | Reserved    | N    | Reserved                                |
| 31   | Reserved    | N    | This bit is always reserved             |

**Note 16.9** Source bits have corresponding Enable and Result bits.

## 16.6.29 IRQ17 Enable Register

**Table 16.42 IRQ17 Enable Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |            |   |    | HOST SIZE           |    |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|------------|---|----|---------------------|----|
| EC OFFSET    | 70h      |                                                                                                      |     | 32-bit     |   |    | EC SIZE             |    |
| POWER        | VTR      |                                                                                                      |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB   |                                                                                                      |     |            |   |    |                     |    |
| BIT          | D31      | D30                                                                                                  | D29 | ■          | ■ | D2 | D1                  | D0 |
| HOST TYPE    | -        | -                                                                                                    | -   | -          | - | -  | -                   | -  |
| EC TYPE      | R        | R/W except for reserved bits See <a href="#">Table 16.41</a> & <a href="#">Note 16.3 on page 315</a> |     |            |   |    |                     |    |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.41</a> , “Bit definition IRQ17 source Register,” on page 336           |     |            |   |    |                     |    |

## 16.6.30 IRQ17 Result Register

**Table 16.43 IRQ17 Result Register**

| HOST ADDRESS | N/A    |                                                                                           |     |                                                                                     |                                                                                       |    | HOST SIZE           |    |
|--------------|--------|-------------------------------------------------------------------------------------------|-----|-------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|----|---------------------|----|
| EC OFFSET    | 74h    |                                                                                           |     | 32-bit                                                                              |                                                                                       |    | EC SIZE             |    |
| POWER        | VTR    |                                                                                           |     | 0000_0000h                                                                          |                                                                                       |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB |                                                                                           |     |                                                                                     |                                                                                       |    |                     |    |
| BIT          | D31    | D30                                                                                       | D29 |  |  | D2 | D1                  | D0 |
| HOST TYPE    | -      | -                                                                                         | -   | -                                                                                   | -                                                                                     | -  | -                   | -  |
| EC TYPE      | R/W    | R                                                                                         | R   | R                                                                                   | R                                                                                     | R  | R                   | R  |
| BIT NAME     | NORM   | Refer to <a href="#">Table 16.41, “Bit definition IRQ17 source Register,” on page 336</a> |     |                                                                                     |                                                                                       |    |                     |    |

### NORM

This bit is a read write bit used by the NORM instruction.

## 16.6.31 IRQ18 Source Register

**Table 16.44 IRQ18 Source Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |                                                                                   |                                                                                     |    |    | HOST SIZE           |  |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|-----------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|----|----|---------------------|--|
| EC OFFSET    | 78h      |                                                                                                      |     |                                                                                   | 32-bit                                                                              |    |    | EC SIZE             |  |
| POWER        | VTR      |                                                                                                      |     |                                                                                   | 0000_0000h                                                                          |    |    | nSYS_RST<br>DEFAULT |  |
| BUS          | EC SPB   |                                                                                                      |     |                                                                                   |                                                                                     |    |    |                     |  |
| BIT          | D31      | D30                                                                                                  | D29 |  |  | D2 | D1 | D0                  |  |
| HOST TYPE    | -        | -                                                                                                    | -   | -                                                                                 | -                                                                                   | -  | -  | -                   |  |
| EC TYPE      | R        | RWC except for reserved bits See <a href="#">Table 16.45</a> & <a href="#">Note 16.3 on page 315</a> |     |                                                                                   |                                                                                     |    |    |                     |  |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.45</a> , “Bit definition IRQ18 source Register,” on page 338           |     |                                                                                   |                                                                                     |    |    |                     |  |

**Table 16.45 Bit definition IRQ18 source Register**

| BIT  | SIGNAL NAME | WAKE | DESCRIPTION                 |
|------|-------------|------|-----------------------------|
| 31   | Reserved    | N    | This bit is always reserved |
| 30-0 | Reserved    | N    | Reserved                    |

**Note 16.10** Source bits have corresponding Enable and Result bits.

## 16.6.32 IRQ18 Enable Register

**Table 16.46 IRQ18 Enable Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |            |   |    | HOST SIZE           |    |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|------------|---|----|---------------------|----|
| EC OFFSET    | 7Ch      |                                                                                                      |     | 32-bit     |   |    | EC SIZE             |    |
| POWER        | VTR      |                                                                                                      |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB   |                                                                                                      |     |            |   |    |                     |    |
| BIT          | D31      | D30                                                                                                  | D29 | ■          | ■ | D2 | D1                  | D0 |
| HOST TYPE    | -        | -                                                                                                    | -   | -          | - | -  | -                   | -  |
| EC TYPE      | R        | R/W except for reserved bits See <a href="#">Table 16.45</a> & <a href="#">Note 16.3 on page 315</a> |     |            |   |    |                     |    |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.45</a> , “Bit definition IRQ18 source Register,” on page 338           |     |            |   |    |                     |    |

## 16.6.33 IRQ18 Result Register

**Table 16.47 IRQ18 Result Register**

| HOST ADDRESS | N/A    |                                                                                            |     |                                                                                     |                                                                                       |    | HOST SIZE           |    |
|--------------|--------|--------------------------------------------------------------------------------------------|-----|-------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|----|---------------------|----|
| EC OFFSET    | 80h    |                                                                                            |     | 32-bit                                                                              |                                                                                       |    | EC SIZE             |    |
| POWER        | VTR    |                                                                                            |     | 0000_0000h                                                                          |                                                                                       |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB |                                                                                            |     |                                                                                     |                                                                                       |    |                     |    |
| BIT          | D31    | D30                                                                                        | D29 |  |  | D2 | D1                  | D0 |
| HOST TYPE    | -      | -                                                                                          | -   | -                                                                                   | -                                                                                     | -  | -                   | -  |
| EC TYPE      | R/W    | R                                                                                          | R   | R                                                                                   | R                                                                                     | R  | R                   | R  |
| BIT NAME     | NORM   | Refer to <a href="#">Table 16.45</a> , “Bit definition IRQ18 source Register,” on page 338 |     |                                                                                     |                                                                                       |    |                     |    |

### NORM

This bit is a read write bit used by the NORM instruction.

## 16.6.34 IRQ19 Source Register

**Table 16.48 IRQ19 Source Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |            |   |    | HOST SIZE           |    |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|------------|---|----|---------------------|----|
| EC OFFSET    | 84h      |                                                                                                      |     | 32-bit     |   |    | EC SIZE             |    |
| POWER        | VTR      |                                                                                                      |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB   |                                                                                                      |     |            |   |    |                     |    |
| BIT          | D31      | D30                                                                                                  | D29 | ■          | ■ | D2 | D1                  | D0 |
| HOST TYPE    | -        | -                                                                                                    | -   | -          | - | -  | -                   | -  |
| EC TYPE      | R        | RWC except for reserved bits See <a href="#">Table 16.49</a> & <a href="#">Note 16.3</a> on page 315 |     |            |   |    |                     |    |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.49</a> , “Bit definition IRQ19 source Register,” on page 340           |     |            |   |    |                     |    |

**Table 16.49 Bit definition IRQ19 source Register**

| BIT  | SIGNAL NAME | WAKE | DESCRIPTION                          |
|------|-------------|------|--------------------------------------|
| 0    | RCID        | N    | 0-to-1 transition of RC_ID done flag |
| 30-1 | Reserved    | N    | Reserved                             |
| 31   | Reserved    | N    | This bit is always reserved          |

**Note 16.11** Source bits have corresponding Enable and Result bits.

### 16.6.35 IRQ19 Enable Register

**Table 16.50 IRQ19 Enable Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |             |   |    | HOST SIZE           |    |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|-------------|---|----|---------------------|----|
| EC OFFSET    | 88h      |                                                                                                      |     | 32-bit      |   |    | EC SIZE             |    |
| POWER        | VTR      |                                                                                                      |     | 0000_00000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB   |                                                                                                      |     |             |   |    |                     |    |
| BIT          | D31      | D30                                                                                                  | D29 | ■           | ■ | D2 | D1                  | D0 |
| HOST TYPE    | -        | -                                                                                                    | -   | -           | - | -  | -                   | -  |
| EC TYPE      | R        | R/W except for reserved bits See <a href="#">Table 16.49</a> & <a href="#">Note 16.3</a> on page 315 |     |             |   |    |                     |    |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.49</a> , “Bit definition IRQ19 source Register,” on page 340           |     |             |   |    |                     |    |

### 16.6.36 IRQ19 Result Register

**Table 16.51 IRQ19 Result Register**

| HOST ADDRESS | N/A    |                                                                                            |     |                                                                                     |                                                                                       |    | HOST SIZE           |    |
|--------------|--------|--------------------------------------------------------------------------------------------|-----|-------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|----|---------------------|----|
| EC OFFSET    | 8Ch    |                                                                                            |     | 32-bit                                                                              |                                                                                       |    | EC SIZE             |    |
| POWER        | VTR    |                                                                                            |     | 0000_0000h                                                                          |                                                                                       |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB |                                                                                            |     |                                                                                     |                                                                                       |    |                     |    |
| BIT          | D31    | D30                                                                                        | D29 |  |  | D2 | D1                  | D0 |
| HOST TYPE    | -      | -                                                                                          | -   | -                                                                                   | -                                                                                     | -  | -                   | -  |
| EC TYPE      | R/W    | R                                                                                          | R   | R                                                                                   | R                                                                                     | R  | R                   | R  |
| BIT NAME     | NORM   | Refer to <a href="#">Table 16.49</a> , “Bit definition IRQ19 source Register,” on page 340 |     |                                                                                     |                                                                                       |    |                     |    |

#### NORM

This bit is a read write bit used by the NORM instruction.



## 16.6.37 IRQ20 Source Register

**Table 16.52 IRQ20 Source Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |            |   |    | HOST SIZE           |    |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|------------|---|----|---------------------|----|
| EC OFFSET    | 90h      |                                                                                                      |     | 32-bit     |   |    | EC SIZE             |    |
| POWER        | VTR      |                                                                                                      |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB   |                                                                                                      |     |            |   |    |                     |    |
| BIT          | D31      | D30                                                                                                  | D29 | ■          | ■ | D2 | D1                  | D0 |
| HOST TYPE    | -        | -                                                                                                    | -   | -          | - | -  | -                   | -  |
| EC TYPE      | R        | RWC except for reserved bits See <a href="#">Table 16.53</a> & <a href="#">Note 16.3 on page 315</a> |     |            |   |    |                     |    |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.53</a> , “Bit definition IRQ20 source Register,” on page 342           |     |            |   |    |                     |    |

**Table 16.53 Bit definition IRQ20 source Register**

| BIT  | SIGNAL NAME | WAKE | DESCRIPTION                                                                              |
|------|-------------|------|------------------------------------------------------------------------------------------|
| 0    | TACH1       | N    | Fan TACH1 Interrupt. This interrupt is signaled when the Fan TACH1 signals an interrupt. |
| 1    | TACH2       | N    | Fan TACH2 Interrupt. This interrupt is signaled when the Fan TACH2 signals an interrupt. |
| 2    | TACH3       | N    | Fan TACH3 Interrupt. This interrupt is signaled when the Fan TACH3 signals an interrupt. |
| 30-3 | Reserved    | N    | Reserved                                                                                 |
| 31   | Reserved    | N    | This bit is always reserved                                                              |

**Note 16.12** Source bits have corresponding Enable and Result bits.

### 16.6.38 IRQ20 Enable Register

**Table 16.54 IRQ20 Enable Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |                                                                                   |                                                                                     |    |    | HOST SIZE           |  |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|-----------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|----|----|---------------------|--|
| EC OFFSET    | 94h      |                                                                                                      |     |                                                                                   | 32-bit                                                                              |    |    | EC SIZE             |  |
| POWER        | VTR      |                                                                                                      |     |                                                                                   | 0000_0000h                                                                          |    |    | nSYS_RST<br>DEFAULT |  |
| BUS          | EC SPB   |                                                                                                      |     |                                                                                   |                                                                                     |    |    |                     |  |
| BIT          | D31      | D30                                                                                                  | D29 |  |  | D2 | D1 | D0                  |  |
| HOST TYPE    | -        | -                                                                                                    | -   | -                                                                                 | -                                                                                   | -  | -  | -                   |  |
| EC TYPE      | R        | R/W except for reserved bits See <a href="#">Table 16.53</a> & <a href="#">Note 16.3</a> on page 315 |     |                                                                                   |                                                                                     |    |    |                     |  |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.53</a> , “Bit definition IRQ20 source Register,” on page 342           |     |                                                                                   |                                                                                     |    |    |                     |  |

### 16.6.39 IRQ20 Result Register

**Table 16.55 IRQ20 Result Register**

| HOST ADDRESS | N/A    |                                                                                            |     |            |   |    | HOST SIZE           |    |
|--------------|--------|--------------------------------------------------------------------------------------------|-----|------------|---|----|---------------------|----|
| EC OFFSET    | 98h    |                                                                                            |     | 32-bit     |   |    | EC SIZE             |    |
| POWER        | VTR    |                                                                                            |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB |                                                                                            |     |            |   |    |                     |    |
| BIT          | D31    | D30                                                                                        | D29 | ■          | ■ | D2 | D1                  | D0 |
| HOST TYPE    | -      | -                                                                                          | -   | -          | - | -  | -                   | -  |
| EC TYPE      | R/W    | R                                                                                          | R   | R          | R | R  | R                   | R  |
| BIT NAME     | NORM   | Refer to <a href="#">Table 16.53</a> , “Bit definition IRQ20 source Register,” on page 342 |     |            |   |    |                     |    |

#### NORM

This bit is a read write bit used by the NORM instruction.

## 16.6.40 IRQ21 Source Register

**Table 16.56 IRQ21 Source Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |   |            |    |    | HOST SIZE           |  |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|---|------------|----|----|---------------------|--|
| EC OFFSET    | 9Ch      |                                                                                                      |     |   | 32-bit     |    |    | EC SIZE             |  |
| POWER        | VTR      |                                                                                                      |     |   | 0000_0000h |    |    | nSYS_RST<br>DEFAULT |  |
| BUS          | EC SPB   |                                                                                                      |     |   |            |    |    |                     |  |
| BIT          | D31      | D30                                                                                                  | D29 | ■ | ■          | D2 | D1 | D0                  |  |
| HOST TYPE    | -        | -                                                                                                    | -   | - | -          | -  | -  | -                   |  |
| EC TYPE      | R        | RWC except for reserved bits See <a href="#">Table 16.57</a> & <a href="#">Note 16.3 on page 315</a> |     |   |            |    |    |                     |  |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.57, “Bit definition IRQ21 source Register,” on page 344</a>            |     |   |            |    |    |                     |  |

**Table 16.57 Bit definition IRQ21 source Register**

| BIT   | SIGNAL NAME     | WAKE | DESCRIPTION                          |
|-------|-----------------|------|--------------------------------------|
| 0     | BCM_BUSY_CLR[A] | N    | BC-LINK Busy Clear Flag Interrupt    |
| 1     | BCM_ERR[A]      | N    | BC_LINK Error Flag Interrupt         |
| 2     | BCM_INT#[A]     | Y    | Interrupt from the BC_LINK Companion |
| 3     | BCM_BUSY_CLR[B] | N    | BC-LINK Busy Clear Flag Interrupt    |
| 4     | BCM_ERR[B]      | N    | BC_LINK Error Flag Interrupt         |
| 5     | BCM_INT#[B]     | Y    | Interrupt from the BC_LINK Companion |
| 6     | BCM_BUSY_CLR[C] | N    | BC-LINK Busy Clear Flag Interrupt    |
| 7     | BCM_ERR[C]      | N    | BC_LINK Error Flag Interrupt         |
| 8     | BCM_INT#[C]     | Y    | Interrupt from the BC_LINK Companion |
| 9     | BCM_BUSY_CLR[D] | N    | BC-LINK Busy Clear Flag Interrupt    |
| 10    | BCM_ERR[D]      | N    | BC_LINK Error Flag Interrupt         |
| 11    | BCM_INT#[D]     | Y    | Interrupt from the BC_LINK Companion |
| 30-12 | Reserved        | N    | Reserved                             |
| 31    | Reserved        | N    | This bit is always reserved          |

**Note 16.13** Source bits have corresponding Enable and Result bits.

## 16.6.41 IRQ21 Enable Register

**Table 16.58 IRQ21 Enable Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |            |   |    | HOST SIZE           |    |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|------------|---|----|---------------------|----|
| EC OFFSET    | A0h      |                                                                                                      |     | 32-bit     |   |    | EC SIZE             |    |
| POWER        | VTR      |                                                                                                      |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB   |                                                                                                      |     |            |   |    |                     |    |
| BIT          | D31      | D30                                                                                                  | D29 | ■          | ■ | D2 | D1                  | D0 |
| HOST TYPE    | -        | -                                                                                                    | -   | -          | - | -  | -                   | -  |
| EC TYPE      | R        | R/W except for reserved bits See <a href="#">Table 16.57</a> & <a href="#">Note 16.3 on page 315</a> |     |            |   |    |                     |    |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.57</a> , “Bit definition IRQ21 source Register,” on page 344           |     |            |   |    |                     |    |

## 16.6.42 IRQ21 Result Register

**Table 16.59 IRQ21 Result Register**

| HOST ADDRESS | N/A    |                                                                                           |     |                                                                                     |                                                                                       |    | HOST SIZE           |    |
|--------------|--------|-------------------------------------------------------------------------------------------|-----|-------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|----|---------------------|----|
| EC OFFSET    | A4h    |                                                                                           |     | 32-bit                                                                              |                                                                                       |    | EC SIZE             |    |
| POWER        | VTR    |                                                                                           |     | 0000_0000h                                                                          |                                                                                       |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB |                                                                                           |     |                                                                                     |                                                                                       |    |                     |    |
| BIT          | D31    | D30                                                                                       | D29 |  |  | D2 | D1                  | D0 |
| HOST TYPE    | -      | -                                                                                         | -   | -                                                                                   | -                                                                                     | -  | -                   | -  |
| EC TYPE      | R/W    | R                                                                                         | R   | R                                                                                   | R                                                                                     | R  | R                   | R  |
| BIT NAME     | NORM   | Refer to <a href="#">Table 16.57, “Bit definition IRQ21 source Register,” on page 344</a> |     |                                                                                     |                                                                                       |    |                     |    |

### NORM

This bit is a read write bit used by the NORM instruction.

## 16.6.43 IRQ22 Source Register

**Table 16.60 IRQ22 Source Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |            |   |    | HOST SIZE           |    |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|------------|---|----|---------------------|----|
| EC OFFSET    | A8h      |                                                                                                      |     | 32-bit     |   |    | EC SIZE             |    |
| POWER        | VTR      |                                                                                                      |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB   |                                                                                                      |     |            |   |    |                     |    |
| BIT          | D31      | D30                                                                                                  | D29 | ■          | ■ | D2 | D1                  | D0 |
| HOST TYPE    | -        | -                                                                                                    | -   | -          | - | -  | -                   | -  |
| EC TYPE      | R        | RWC except for reserved bits See <a href="#">Table 16.61</a> & <a href="#">Note 16.3 on page 315</a> |     |            |   |    |                     |    |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.61</a> , “Bit definition IRQ22 source Register,” on page 346           |     |            |   |    |                     |    |

**Table 16.61 Bit definition IRQ22 source Register**

| BIT  | SIGNAL NAME | WAKE | DESCRIPTION                 |
|------|-------------|------|-----------------------------|
| 30-0 | Reserved    | N    | Reserved                    |
| 31   | Reserved    | N    | This bit is always reserved |

**Note 16.14** Source bits have corresponding Enable and Result bits.

## 16.6.44 IRQ22 Enable Register

**Table 16.62 IRQ22 Enable Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |            |   |    | HOST SIZE           |    |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|------------|---|----|---------------------|----|
| EC OFFSET    | ACh      |                                                                                                      |     | 32-bit     |   |    | EC SIZE             |    |
| POWER        | VTR      |                                                                                                      |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB   |                                                                                                      |     |            |   |    |                     |    |
| BIT          | D31      | D30                                                                                                  | D29 | ■          | ■ | D2 | D1                  | D0 |
| HOST TYPE    | -        | -                                                                                                    | -   | -          | - | -  | -                   | -  |
| EC TYPE      | R        | R/W except for reserved bits See <a href="#">Table 16.61</a> & <a href="#">Note 16.3</a> on page 315 |     |            |   |    |                     |    |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.61</a> , “Bit definition IRQ22 source Register,” on page 346           |     |            |   |    |                     |    |

## 16.6.45 IRQ22 Result Register

**Table 16.63 IRQ22 Result Register**

| HOST ADDRESS | N/A    |                                                                                            |     |                                                                                     |                                                                                       |    | HOST SIZE           |    |
|--------------|--------|--------------------------------------------------------------------------------------------|-----|-------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|----|---------------------|----|
| EC OFFSET    | B0h    |                                                                                            |     | 32-bit                                                                              |                                                                                       |    | EC SIZE             |    |
| POWER        | VTR    |                                                                                            |     | 0000_0000h                                                                          |                                                                                       |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB |                                                                                            |     |                                                                                     |                                                                                       |    |                     |    |
| BIT          | D31    | D30                                                                                        | D29 |  |  | D2 | D1                  | D0 |
| HOST TYPE    | -      | -                                                                                          | -   | -                                                                                   | -                                                                                     | -  | -                   | -  |
| EC TYPE      | R/W    | R                                                                                          | R   | R                                                                                   | R                                                                                     | R  | R                   | R  |
| BIT NAME     | NORM   | Refer to <a href="#">Table 16.61</a> , “Bit definition IRQ22 source Register,” on page 346 |     |                                                                                     |                                                                                       |    |                     |    |

### NORM

This bit is a read write bit used by the NORM instruction.

## 16.6.46 IRQ23 Source Register

**Table 16.64 IRQ23 Source Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |                                                                                   |                                                                                     |    | HOST SIZE           |    |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|-----------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|----|---------------------|----|
| EC OFFSET    | B4h      |                                                                                                      |     | 32-bit                                                                            |                                                                                     |    | EC SIZE             |    |
| POWER        | VTR      |                                                                                                      |     | 0000_0000h                                                                        |                                                                                     |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB   |                                                                                                      |     |                                                                                   |                                                                                     |    |                     |    |
| BIT          | D31      | D30                                                                                                  | D29 |  |  | D2 | D1                  | D0 |
| HOST TYPE    | -        | -                                                                                                    | -   | -                                                                                 | -                                                                                   | -  | -                   | -  |
| EC TYPE      | R        | RWC except for reserved bits See <a href="#">Table 16.65</a> & <a href="#">Note 16.3</a> on page 315 |     |                                                                                   |                                                                                     |    |                     |    |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.65</a> , “Bit definition IRQ23 source Register,” on page 348           |     |                                                                                   |                                                                                     |    |                     |    |

**Table 16.65 Bit definition IRQ23 source Register**

| BIT   | SIGNAL NAME | WAKE | DESCRIPTION                                                                                                               |
|-------|-------------|------|---------------------------------------------------------------------------------------------------------------------------|
| 0     | KBD_OBF     | N    | Keyboard Controller OBF Interrupt. This interrupt is signaled when the OBF bit in the KBD status register has been clear. |
| 1     | KBD_IBF     | N    | Keyboard Controller IBF Interrupt. This interrupt is signaled when the host writes to the KBD Command or Data port.       |
| 12-2  | Reserved    | N    | Reserved                                                                                                                  |
| 13    | PS2_ACT_0   | N    | PS2_0 Activity Interrupt form PS/2 Block                                                                                  |
| 14    | PS2_ACT_1   | N    | PS2_1 Activity Interrupt form PS/2 Block                                                                                  |
| 15    | PS2_ACT_2   | N    | PS2_2 Activity Interrupt form PS/2 Block                                                                                  |
| 16    | Reserved    | N    | Reserved                                                                                                                  |
| 17    | PS2_WK_0A   | Y    | PS2_0A Start Detectform pin signal                                                                                        |
| 18    | PS2_WK_0B   | Y    | PS2_0B Start Detectform pin signal                                                                                        |
| 19    | PS2_WK_1A   | Y    | PS2_1A Start Detectform pin signal                                                                                        |
| 20    | PS2_WK_1B   | Y    | PS2_1B Start Detectform pin signal                                                                                        |
| 21    | PS2_WK_2    | Y    | PS2_2 Start Detectform pin signal                                                                                         |
| 30-22 | Reserved    | N    | Reserved                                                                                                                  |
| 31    | Reserved    | N    | This bit is always reserved                                                                                               |

**Note 16.15** Source bits have corresponding Enable and Result bits.

## 16.6.47 IRQ23 Enable Register

**Table 16.66 IRQ23 Enable Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |                                                                                   |                                                                                     |    | HOST SIZE           |    |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|-----------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|----|---------------------|----|
| EC OFFSET    | B8h      |                                                                                                      |     | 32-bit                                                                            |                                                                                     |    | EC SIZE             |    |
| POWER        | VTR      |                                                                                                      |     | 0000_0000h                                                                        |                                                                                     |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB   |                                                                                                      |     |                                                                                   |                                                                                     |    |                     |    |
| BIT          | D31      | D30                                                                                                  | D29 |  |  | D2 | D1                  | D0 |
| HOST TYPE    | -        | -                                                                                                    | -   | -                                                                                 | -                                                                                   | -  | -                   | -  |
| EC TYPE      | R        | R/W except for reserved bits See <a href="#">Table 16.65</a> & <a href="#">Note 16.3</a> on page 315 |     |                                                                                   |                                                                                     |    |                     |    |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.65</a> , “Bit definition IRQ23 source Register,” on page 348           |     |                                                                                   |                                                                                     |    |                     |    |

## 16.6.48 IRQ23 Result Register

**Table 16.67 IRQ23 Result Register**

| HOST ADDRESS | N/A    |                                                                                            |     |                                                                                     |                                                                                       |    | HOST SIZE           |    |
|--------------|--------|--------------------------------------------------------------------------------------------|-----|-------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|----|---------------------|----|
| EC OFFSET    | BCh    |                                                                                            |     | 32-bit                                                                              |                                                                                       |    | EC SIZE             |    |
| POWER        | VTR    |                                                                                            |     | 0000_0000h                                                                          |                                                                                       |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB |                                                                                            |     |                                                                                     |                                                                                       |    |                     |    |
| BIT          | D31    | D30                                                                                        | D29 |  |  | D2 | D1                  | D0 |
| HOST TYPE    | -      | -                                                                                          | -   | -                                                                                   | -                                                                                     | -  | -                   | -  |
| EC TYPE      | R/W    | R                                                                                          | R   | R                                                                                   | R                                                                                     | R  | R                   | R  |
| BIT NAME     | NORM   | Refer to <a href="#">Table 16.65</a> , “Bit definition IRQ23 source Register,” on page 348 |     |                                                                                     |                                                                                       |    |                     |    |

### NORM

This bit is a read write bit used by the NORM instruction.



## 16.6.49 IRQ24 Source Register

**Table 16.68 IRQ24 Source Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |            |   |    | HOST SIZE           |    |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|------------|---|----|---------------------|----|
| EC OFFSET    | C0h      |                                                                                                      |     | 32-bit     |   |    | EC SIZE             |    |
| POWER        | VTR      |                                                                                                      |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB   |                                                                                                      |     |            |   |    |                     |    |
| BIT          | D31      | D30                                                                                                  | D29 | ■          | ■ | D2 | D1                  | D0 |
| HOST TYPE    | -        | -                                                                                                    | -   | -          | - | -  | -                   | -  |
| EC TYPE      | R        | RWC except for reserved bits See <a href="#">Table 16.69</a> & <a href="#">Note 16.3 on page 315</a> |     |            |   |    |                     |    |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.69, “Bit definition IRQ24 source Register,” on page 350</a>            |     |            |   |    |                     |    |

**Table 16.69 Bit definition IRQ24 source Register**

| BIT  | SIGNAL NAME | WAKE | DESCRIPTION                                                                                                                 |
|------|-------------|------|-----------------------------------------------------------------------------------------------------------------------------|
| 0    | EC2_OBF     | N    | Embedded Controller 2 OBF Interrupt. This interrupt is signaled when the OBF bit in the EC2 status register has been clear. |
| 1    | EC2_IBF     | N    | Embedded Controller 2 IBF Interrupt. This interrupt is signaled when the host writes to the EC2 Command or Data port.       |
| 2    | EC1_OBF     | N    | Embedded Controller 1 OBF Interrupt. This interrupt is signaled when the OBF bit in the EC1 status register has been clear. |
| 3    | EC1_IBF     | N    | Embedded Controller 1 IBF Interrupt. This interrupt is signaled when the host writes to the EC1 Command or Data port.       |
| 4    | EC0_OBF     | N    | Embedded Controller 0 OBF Interrupt. This interrupt is signaled when the OBF bit in the EC0 status register has been clear. |
| 5    | EC0_IBF     | N    | Embedded Controller 0 IBF Interrupt. This interrupt is signaled when the host writes to the EC0 Command or Data port.       |
| 30-6 | Reserved    | N    | Reserved                                                                                                                    |
| 31   | Reserved    | N    | This bit is always reserved                                                                                                 |

**Note 16.16** Source bits have corresponding Enable and Result bits.

## 16.6.50 IRQ24 Enable Register

**Table 16.70 IRQ24 Enable Register**

| HOST ADDRESS | N/A      |                                                                                            |     |            |     |     | HOST SIZE           |     |
|--------------|----------|--------------------------------------------------------------------------------------------|-----|------------|-----|-----|---------------------|-----|
| EC OFFSET    | C4h      |                                                                                            |     | 32-bit     |     |     | EC SIZE             |     |
| POWER        | VTR      |                                                                                            |     | 0000_0000h |     |     | nSYS_RST<br>DEFAULT |     |
| BUS          | EC SPB   |                                                                                            |     |            |     |     |                     |     |
| BIT          | D31      | D30                                                                                        | D29 | ■          | ■   | D2  | D1                  | D0  |
| HOST TYPE    | -        | -                                                                                          | -   | -          | -   | -   | -                   | -   |
| EC TYPE      | R        | R/W                                                                                        | R/W | R/W        | R/W | R/W | R/W                 | R/W |
| BIT NAME     | Reserved | Refer to <a href="#">Table 16.69</a> , “Bit definition IRQ24 source Register,” on page 350 |     |            |     |     |                     |     |

## 16.6.51 IRQ24 Result Register

**Table 16.71 IRQ24 Result Register**

| HOST ADDRESS | N/A    |                                                                                            |     |                                                                                     |                                                                                       |    | HOST SIZE           |    |
|--------------|--------|--------------------------------------------------------------------------------------------|-----|-------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|----|---------------------|----|
| EC OFFSET    | C8h    |                                                                                            |     | 32-bit                                                                              |                                                                                       |    | EC SIZE             |    |
| POWER        | VTR    |                                                                                            |     | 0000_0000h                                                                          |                                                                                       |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB |                                                                                            |     |                                                                                     |                                                                                       |    |                     |    |
| BIT          | D31    | D30                                                                                        | D29 |  |  | D2 | D1                  | D0 |
| HOST TYPE    | -      | -                                                                                          | -   | -                                                                                   | -                                                                                     | -  | -                   | -  |
| EC TYPE      | R/W    | R                                                                                          | R   | R                                                                                   | R                                                                                     | R  | R                   | R  |
| BIT NAME     | NORM   | Refer to <a href="#">Table 16.69</a> , “Bit definition IRQ24 source Register,” on page 350 |     |                                                                                     |                                                                                       |    |                     |    |

### NORM

This bit is a read write bit used by the NORM instruction.

## 16.6.52 IRQ25 Source Register

**Table 16.72 IRQ25 Source Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |                                                                                   |                                                                                    |    | HOST SIZE           |    |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|-----------------------------------------------------------------------------------|------------------------------------------------------------------------------------|----|---------------------|----|
| EC OFFSET    | CCh      |                                                                                                      |     | 32-bit                                                                            |                                                                                    |    | EC SIZE             |    |
| POWER        | VTR      |                                                                                                      |     | 0000_0000h                                                                        |                                                                                    |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB   |                                                                                                      |     |                                                                                   |                                                                                    |    |                     |    |
| BIT          | D31      | D30                                                                                                  | D29 |  |  | D2 | D1                  | D0 |
| HOST TYPE    | -        | -                                                                                                    | -   | -                                                                                 | -                                                                                  | -  | -                   | -  |
| EC TYPE      | R        | RWC except for reserved bits See <a href="#">Table 16.73</a> & <a href="#">Note 16.3</a> on page 315 |     |                                                                                   |                                                                                    |    |                     |    |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.73</a> , “Bit definition IRQ25 source Register,” on page 352           |     |                                                                                   |                                                                                    |    |                     |    |

**Table 16.73 Bit definition IRQ25 source Register**

| BIT  | SIGNAL NAME | WAKE | DESCRIPTION                 |
|------|-------------|------|-----------------------------|
| 30:0 | Reserved    | N    | Reserved                    |
| 31   | Reserved    | N    | This bit is always reserved |

**Note 16.17** Source bits have corresponding Enable and Result bits.

## 16.6.53 IRQ25 Enable Register

**Table 16.74 IRQ25 Enable Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |            |   |    | HOST SIZE           |    |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|------------|---|----|---------------------|----|
| EC OFFSET    | D0h      |                                                                                                      |     | 32-bit     |   |    | EC SIZE             |    |
| POWER        | VTR      |                                                                                                      |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB   |                                                                                                      |     |            |   |    |                     |    |
| BIT          | D31      | D30                                                                                                  | D29 | ■          | ■ | D2 | D1                  | D0 |
| HOST TYPE    | -        | -                                                                                                    | -   | -          | - | -  | -                   | -  |
| EC TYPE      | R        | R/W except for reserved bits See <a href="#">Table 16.73</a> & <a href="#">Note 16.3</a> on page 315 |     |            |   |    |                     |    |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.73</a> , “Bit definition IRQ25 source Register,” on page 352           |     |            |   |    |                     |    |

## 16.6.54 IRQ25 Result Register

**Table 16.75 IRQ25 Result Register**

| HOST ADDRESS | N/A    |                                                                                           |     |                                                                                   |                                                                                     |    | HOST SIZE           |    |
|--------------|--------|-------------------------------------------------------------------------------------------|-----|-----------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|----|---------------------|----|
| EC OFFSET    | D4h    |                                                                                           |     | 32-bit                                                                            |                                                                                     |    | EC SIZE             |    |
| POWER        | VTR    |                                                                                           |     | 0000_0000h                                                                        |                                                                                     |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB |                                                                                           |     |                                                                                   |                                                                                     |    |                     |    |
| BIT          | D31    | D30                                                                                       | D29 |  |  | D2 | D1                  | D0 |
| HOST TYPE    | -      | -                                                                                         | -   | -                                                                                 | -                                                                                   | -  | -                   | -  |
| EC TYPE      | R/W    | R                                                                                         | R   | R                                                                                 | R                                                                                   | R  | R                   | R  |
| BIT NAME     | NORM   | Refer To <a href="#">Table 16.73, “Bit definition IRQ25 source Register,” on page 352</a> |     |                                                                                   |                                                                                     |    |                     |    |

### NORM

This bit is a read write bit used by the NORM instruction.

## 16.6.55 IRQ26 Source Register

**Table 16.76 IRQ26 Source Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |   |            |    |    | HOST SIZE           |  |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|---|------------|----|----|---------------------|--|
| EC OFFSET    | D8h      |                                                                                                      |     |   | 32-bit     |    |    | EC SIZE             |  |
| POWER        | VTR      |                                                                                                      |     |   | 0000_0000h |    |    | nSYS_RST<br>DEFAULT |  |
| BUS          | EC SPB   |                                                                                                      |     |   |            |    |    |                     |  |
| BIT          | D31      | D30                                                                                                  | D29 | ■ | ■          | D2 | D1 | D0                  |  |
| HOST TYPE    | -        | -                                                                                                    | -   | - | -          | -  | -  | -                   |  |
| EC TYPE      | R        | RWC except for reserved bits See <a href="#">Table 16.77</a> & <a href="#">Note 16.3 on page 315</a> |     |   |            |    |    |                     |  |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.77</a> , “Bit definitions IRQ26 Source Register,” on page 353          |     |   |            |    |    |                     |  |

**Table 16.77 Bit definitions IRQ26 Source Register**

| BIT    | SIGNAL NAME | WAKE | DESCRIPTION |
|--------|-------------|------|-------------|
| [30:0] | Reserved    | N    | Reserved    |

Table 16.77 Bit definitions IRQ26 Source Register

| BIT | SIGNAL NAME | WAKE | DESCRIPTION                 |
|-----|-------------|------|-----------------------------|
| 31  | Reserved    | N    | This bit is always reserved |

### 16.6.56 IRQ26 Enable Register

Table 16.78 IRQ26 Enable Register

| HOST ADDRESS | N/A      |                                                                                            |     |            |     |     | HOST SIZE           |     |
|--------------|----------|--------------------------------------------------------------------------------------------|-----|------------|-----|-----|---------------------|-----|
| EC OFFSET    | DCh      |                                                                                            |     | 32-bit     |     |     | EC SIZE             |     |
| POWER        | VTR      |                                                                                            |     | 0000_0000h |     |     | nSYS_RST<br>DEFAULT |     |
| BUS          | EC SPB   |                                                                                            |     |            |     |     |                     |     |
| BIT          | D31      | D30                                                                                        | D29 | ■          | ■   | D2  | D1                  | D0  |
| HOST TYPE    | -        | -                                                                                          | -   | -          | -   | -   | -                   | -   |
| EC TYPE      | R        | R/W                                                                                        | R/W | R/W        | R/W | R/W | R/W                 | R/W |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.77, “Bit definitions IRQ26 Source Register,” on page 353</a> |     |            |     |     |                     |     |

### 16.6.57 IRQ26 Result Register

Table 16.79 IRQ26 Result Register

| HOST ADDRESS | N/A    |                                                                                            |     |                                                                                     |                                                                                       |    | HOST SIZE           |    |
|--------------|--------|--------------------------------------------------------------------------------------------|-----|-------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|----|---------------------|----|
| EC OFFSET    | E0h    |                                                                                            |     | 32-bit                                                                              |                                                                                       |    | EC SIZE             |    |
| POWER        | VTR    |                                                                                            |     | 0000_0000h                                                                          |                                                                                       |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB |                                                                                            |     |                                                                                     |                                                                                       |    |                     |    |
| BIT          | D31    | D30                                                                                        | D29 |  |  | D2 | D1                  | D0 |
| HOST TYPE    | -      | -                                                                                          | -   | -                                                                                   | -                                                                                     | -  | -                   | -  |
| EC TYPE      | R/W    | R                                                                                          | R   | R                                                                                   | R                                                                                     | R  | R                   | R  |
| BIT NAME     | NORM   | Refer To <a href="#">Table 16.77, “Bit definitions IRQ26 Source Register,” on page 353</a> |     |                                                                                     |                                                                                       |    |                     |    |

#### NORM

This bit is a read write bit used by the NORM instruction.

## 16.6.58 IRQ27 Source Register

**Table 16.80 IRQ27 Source Register**

| HOST ADDRESS | N/A      |                                                                                                      |     |   |   |            |    | HOST SIZE           |
|--------------|----------|------------------------------------------------------------------------------------------------------|-----|---|---|------------|----|---------------------|
| EC OFFSET    | E4h      |                                                                                                      |     |   |   | 32-bit     |    | EC SIZE             |
| POWER        | VTR      |                                                                                                      |     |   |   | 0000_0000h |    | nSYS_RST<br>DEFAULT |
| BUS          | EC SPB   |                                                                                                      |     |   |   |            |    |                     |
| BIT          | D31      | D30                                                                                                  | D29 |   |   | D2         | D1 | D0                  |
| HOST TYPE    | -        | -                                                                                                    | -   | - | - | -          | -  | -                   |
| EC TYPE      | R        | RWC except for reserved bits See <a href="#">Table 16.81</a> & <a href="#">Note 16.3</a> on page 315 |     |   |   |            |    |                     |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.81</a> , "Bit definitions IRQ27 Source Register," on page 355          |     |   |   |            |    |                     |

**Table 16.81 Bit definitions IRQ27 Source Register**

| BIT    | SIGNAL NAME | WAKE | DESCRIPTION                 |
|--------|-------------|------|-----------------------------|
| [30:0] | Reserved    | N    | Reserved                    |
| 31     | Reserved    | N    | This bit is always reserved |

## 16.6.59 IRQ27 Enable Register

**Table 16.82 IRQ27 Enable Register**

| HOST ADDRESS | N/A      |                                                                             |     |     |     |            |     | HOST SIZE           |
|--------------|----------|-----------------------------------------------------------------------------|-----|-----|-----|------------|-----|---------------------|
| EC OFFSET    | E8h      |                                                                             |     |     |     | 32-bit     |     | EC SIZE             |
| POWER        | VTR      |                                                                             |     |     |     | 0000_0000h |     | nSYS_RST<br>DEFAULT |
| BUS          | EC SPB   |                                                                             |     |     |     |            |     |                     |
| BIT          | D31      | D30                                                                         | D29 |     |     | D2         | D1  | D0                  |
| HOST TYPE    | -        | -                                                                           | -   | -   | -   | -          | -   | -                   |
| EC TYPE      | R        | R/W                                                                         | R/W | R/W | R/W | R/W        | R/W | R/W                 |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.80</a> , "IRQ27 Source Register," on page 355 |     |     |     |            |     |                     |

## 16.6.60 IRQ27 Result Register

**Table 16.83 IRQ27 Result Register**

| HOST ADDRESS | N/A    |                                                                            |     |                                                                                   |                                                                                     |    | HOST SIZE           |    |
|--------------|--------|----------------------------------------------------------------------------|-----|-----------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|----|---------------------|----|
| EC OFFSET    | ECh    |                                                                            |     | 32-bit                                                                            |                                                                                     |    | EC SIZE             |    |
| POWER        | VTR    |                                                                            |     | 0000_0000h                                                                        |                                                                                     |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB |                                                                            |     |                                                                                   |                                                                                     |    |                     |    |
| BIT          | D31    | D30                                                                        | D29 |  |  | D2 | D1                  | D0 |
| HOST TYPE    | -      | -                                                                          | -   | -                                                                                 | -                                                                                   | -  | -                   | -  |
| EC TYPE      | R/W    | R                                                                          | R   | R                                                                                 | R                                                                                   | R  | R                   | R  |
| BIT NAME     | NORM   | Refer To <a href="#">Table 16.80, “IRQ27 Source Register,”</a> on page 355 |     |                                                                                   |                                                                                     |    |                     |    |

### NORM

This bit is a read write bit used by the NORM instruction.

## 16.6.61

## 16.6.62 IRQ28 Source Register

**Table 16.84 IRQ28 Source Register**

| HOST ADDRESS | N/A      |                                                                            |      |                                                                                     |                                                                                       |      | HOST SIZE           |      |
|--------------|----------|----------------------------------------------------------------------------|------|-------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|------|---------------------|------|
| EC OFFSET    | F0h      |                                                                            |      | 32-bit                                                                              |                                                                                       |      | EC SIZE             |      |
| POWER        | VTR      |                                                                            |      | 0000_0000h                                                                          |                                                                                       |      | nSYS_RST<br>DEFAULT |      |
| BUS          | EC SPB   |                                                                            |      |                                                                                     |                                                                                       |      |                     |      |
| BIT          | D31      | D30                                                                        | D29  |  |  | D2   | D1                  | D0   |
| HOST TYPE    | -        | -                                                                          | -    | -                                                                                   | -                                                                                     | -    | -                   | -    |
| EC TYPE      | R        | R/WC                                                                       | R/WC | R/WC                                                                                | R/WC                                                                                  | R/WC | R/WC                | R/WC |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.84, “IRQ28 Source Register,”</a> on page 356 |      |                                                                                     |                                                                                       |      |                     |      |



Table 16.85 Bit definitions IRQ28 Source Register

| BITS   | SIGNAL NAME | WAKE | DESCRIPTION                 |
|--------|-------------|------|-----------------------------|
| [30:0] | Reserved    | N    | Reserved                    |
| 31     | Reserved    | N    | This bit is always reserved |

### 16.6.63 IRQ28 Enable Register

Table 16.86 IRQ28 Enable Register

| HOST ADDRESS | N/A      |                                                                            |     |            |     |     | HOST SIZE           |     |
|--------------|----------|----------------------------------------------------------------------------|-----|------------|-----|-----|---------------------|-----|
| EC OFFSET    | F4h      |                                                                            |     | 32-bit     |     |     | EC SIZE             |     |
| POWER        | VTR      |                                                                            |     | 0000_0000h |     |     | nSYS_RST<br>DEFAULT |     |
| BUS          | EC SPB   |                                                                            |     |            |     |     |                     |     |
| BIT          | D31      | D30                                                                        | D29 | ■          | ■   | D2  | D1                  | D0  |
| HOST TYPE    | -        | -                                                                          | -   | -          | -   | -   | -                   | -   |
| EC TYPE      | R        | R/W                                                                        | R/W | R/W        | R/W | R/W | R/W                 | R/W |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.84, “IRQ28 Source Register,” on page 356</a> |     |            |     |     |                     |     |

### 16.6.64 IRQ28 Result Register

Table 16.87 IRQ28 Result Register

| HOST ADDRESS | N/A    |                                                                            |     |            |   |    | HOST SIZE           |    |
|--------------|--------|----------------------------------------------------------------------------|-----|------------|---|----|---------------------|----|
| EC OFFSET    | F8h    |                                                                            |     | 32-bit     |   |    | EC SIZE             |    |
| POWER        | VTR    |                                                                            |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB |                                                                            |     |            |   |    |                     |    |
| BIT          | D31    | D30                                                                        | D29 | ■          | ■ | D2 | D1                  | D0 |
| HOST TYPE    | -      | -                                                                          | -   | -          | - | -  | -                   | -  |
| EC TYPE      | R/W    | R                                                                          | R   | R          | R | R  | R                   | R  |
| BIT NAME     | NORM   | Refer To <a href="#">Table 16.84, “IRQ28 Source Register,” on page 356</a> |     |            |   |    |                     |    |



**NORM**

This bit is a read write bit used by the NORM instruction.

**16.6.65 IRQ29 Source Register****Table 16.88 IRQ29 Source Register**

| HOST ADDRESS | N/A      |                                                                            |      |                                                                                   |                                                                                     |      | HOST SIZE           |      |
|--------------|----------|----------------------------------------------------------------------------|------|-----------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|------|---------------------|------|
| EC OFFSET    | FCh      |                                                                            |      | 32-bit                                                                            |                                                                                     |      | EC SIZE             |      |
| POWER        | VTR      |                                                                            |      | 0000_0000h                                                                        |                                                                                     |      | nSYS_RST<br>DEFAULT |      |
| BUS          | EC SPB   |                                                                            |      |                                                                                   |                                                                                     |      |                     |      |
| BIT          | D31      | D30                                                                        | D29  |  |  | D2   | D1                  | D0   |
| HOST TYPE    | -        | -                                                                          | -    | -                                                                                 | -                                                                                   | -    | -                   | -    |
| EC TYPE      | R        | R/WC                                                                       | R/WC | R/WC                                                                              | R/WC                                                                                | R/WC | R/WC                | R/WC |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.88, “IRQ29 Source Register,”</a> on page 358 |      |                                                                                   |                                                                                     |      |                     |      |

**Table 16.89 Bit definitions IRQ29 Source Register**

| BIT    | SIGNAL NAME | WAKE | DESCRIPTION                 |
|--------|-------------|------|-----------------------------|
| [30:0] | Reserved    | N    | Reserved                    |
| 31     | Reserved    | N    | This bit is always reserved |

## 16.6.66 IRQ29 Enable Register

**Table 16.90 IRQ29 Enable Register**

| HOST ADDRESS | N/A      |                                                                            |     |            |     |     | HOST SIZE           |     |
|--------------|----------|----------------------------------------------------------------------------|-----|------------|-----|-----|---------------------|-----|
| EC OFFSET    | 100h     |                                                                            |     | 32-bit     |     |     | EC SIZE             |     |
| POWER        | VTR      |                                                                            |     | 0000_0000h |     |     | nSYS_RST<br>DEFAULT |     |
| BUS          | EC SPB   |                                                                            |     |            |     |     |                     |     |
| BIT          | D31      | D30                                                                        | D29 | ■          | ■   | D2  | D1                  | D0  |
| HOST TYPE    | -        | -                                                                          | -   | -          | -   | -   | -                   | -   |
| EC TYPE      | R        | R/W                                                                        | R/W | R/W        | R/W | R/W | R/W                 | R/W |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.88, “IRQ29 Source Register,”</a> on page 358 |     |            |     |     |                     |     |

## 16.6.67 IRQ29 Result Register

**Table 16.91 IRQ29 Result Register**

| HOST ADDRESS | N/A    |                                                                            |     |                                                                                     |                                                                                       |    | HOST SIZE           |    |
|--------------|--------|----------------------------------------------------------------------------|-----|-------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|----|---------------------|----|
| EC OFFSET    | 104h   |                                                                            |     | 32-bit                                                                              |                                                                                       |    | EC SIZE             |    |
| POWER        | VTR    |                                                                            |     | 0000_0000h                                                                          |                                                                                       |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB |                                                                            |     |                                                                                     |                                                                                       |    |                     |    |
| BIT          | D31    | D30                                                                        | D29 |  |  | D2 | D1                  | D0 |
| HOST TYPE    | -      | -                                                                          | -   | -                                                                                   | -                                                                                     | -  | -                   | -  |
| EC TYPE      | R/W    | R                                                                          | R   | R                                                                                   | R                                                                                     | R  | R                   | R  |
| BIT NAME     | NORM   | Refer To <a href="#">Table 16.88, “IRQ29 Source Register,”</a> on page 358 |     |                                                                                     |                                                                                       |    |                     |    |

### NORM

This bit is a read write bit used by the NORM instruction.

## 16.6.68 IRQ30 Source Register

**Table 16.92 IRQ30 Source Register**

| HOST ADDRESS | N/A      |                                                                                            |      |                                                                                   |                                                                                     |      | HOST SIZE           |      |
|--------------|----------|--------------------------------------------------------------------------------------------|------|-----------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|------|---------------------|------|
| EC OFFSET    | 108h     |                                                                                            |      | 32-bit                                                                            |                                                                                     |      | EC SIZE             |      |
| POWER        | VTR      |                                                                                            |      | 0000_0000h                                                                        |                                                                                     |      | nSYS_RST<br>DEFAULT |      |
| BUS          | EC SPB   |                                                                                            |      |                                                                                   |                                                                                     |      |                     |      |
| BIT          | D31      | D30                                                                                        | D29  |  |  | D2   | D1                  | D0   |
| HOST TYPE    | -        | -                                                                                          | -    | -                                                                                 | -                                                                                   | -    | -                   | -    |
| EC TYPE      | R/       | R/WC                                                                                       | R/WC | R/WC                                                                              | R/WC                                                                                | R/WC | R/WC                | R/WC |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.93, “Bit definitions IRQ30 Source Register,” on page 360</a> |      |                                                                                   |                                                                                     |      |                     |      |

**Table 16.93 Bit definitions IRQ30 Source Register**

| BIT    | SIGNAL NAME | WAKE | DESCRIPTION                 |
|--------|-------------|------|-----------------------------|
| [30:0] | Reserved    | N    | Reserved                    |
| 31     | Reserved    | N    | This bit is always reserved |

## 16.6.69 IRQ30 Enable Register

**Table 16.94 IRQ30 Enable Register**

| HOST ADDRESS | N/A      |                                                                                            |     |            |     |     | HOST SIZE           |     |
|--------------|----------|--------------------------------------------------------------------------------------------|-----|------------|-----|-----|---------------------|-----|
| EC OFFSET    | 10Ch     |                                                                                            |     | 32-bit     |     |     | EC SIZE             |     |
| POWER        | VTR      |                                                                                            |     | 0000_0000h |     |     | nSYS_RST<br>DEFAULT |     |
| BUS          | EC SPB   |                                                                                            |     |            |     |     |                     |     |
| BIT          | D31      | D30                                                                                        | D29 | ■          | ■   | D2  | D1                  | D0  |
| HOST TYPE    | -        | -                                                                                          | -   | -          | -   | -   | -                   | -   |
| EC TYPE      | R        | R/W                                                                                        | R/W | R/W        | R/W | R/W | R/W                 | R/W |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.93, “Bit definitions IRQ30 Source Register,” on page 360</a> |     |            |     |     |                     |     |

## 16.6.70 IRQ30 Result Register

Table 16.95 IRQ30 Result Register

| HOST ADDRESS | N/A    |                                                                                            |     |            |   |    | HOST SIZE           |    |
|--------------|--------|--------------------------------------------------------------------------------------------|-----|------------|---|----|---------------------|----|
| EC OFFSET    | 110h   |                                                                                            |     | 32-bit     |   |    | EC SIZE             |    |
| POWER        | VTR    |                                                                                            |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB |                                                                                            |     |            |   |    |                     |    |
| BIT          | D31    | D30                                                                                        | D29 | ■          | ■ | D2 | D1                  | D0 |
| HOST TYPE    | -      | -                                                                                          | -   | -          | - | -  | -                   | -  |
| EC TYPE      | R/W    | R                                                                                          | R   | R          | R | R  | R                   | R  |
| BIT NAME     | NORM   | Refer To <a href="#">Table 16.93, “Bit definitions IRQ30 Source Register,”</a> on page 360 |     |            |   |    |                     |    |

### NORM

This bit is a read write bit used by the NORM instruction.

## 16.6.71 IRQ31 Source Register

Table 16.96 IRQ31 Source Register

| HOST ADDRESS | N/A      |                                                                                            |      |                                                                                     |                                                                                       |      | HOST SIZE           |      |
|--------------|----------|--------------------------------------------------------------------------------------------|------|-------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|------|---------------------|------|
| EC OFFSET    | 114h     |                                                                                            |      | 32-bit                                                                              |                                                                                       |      | EC SIZE             |      |
| POWER        | VTR      |                                                                                            |      | 0000_0000h                                                                          |                                                                                       |      | nSYS_RST<br>DEFAULT |      |
| BUS          | EC SPB   |                                                                                            |      |                                                                                     |                                                                                       |      |                     |      |
| BIT          | D31      | D30                                                                                        | D29  |  |  | D2   | D1                  | D0   |
| HOST TYPE    | -        | -                                                                                          | -    | -                                                                                   | -                                                                                     | -    | -                   | -    |
| EC TYPE      | R        | R/WC                                                                                       | R/WC | R/WC                                                                                | R/WC                                                                                  | R/WC | R/WC                | R/WC |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.97, “Bit definitions IRQ31 Source Register,” on page 361</a> |      |                                                                                     |                                                                                       |      |                     |      |

Table 16.97 Bit definitions IRQ31 Source Register

| BIT | SIGNAL NAME | WAKE | DESCRIPTION            |
|-----|-------------|------|------------------------|
| 0   | TIMER0      | N    | 16-bit Timer Interrupt |

**Table 16.97 Bit definitions IRQ31 Source Register**

| BIT     | SIGNAL NAME | WAKE | DESCRIPTION                                                                                                  |
|---------|-------------|------|--------------------------------------------------------------------------------------------------------------|
| 1       | TIMER1      | N    | 16-bit Timer Interrupt                                                                                       |
| 2       | TIMER2      | N    | 16-bit Timer Interrupt                                                                                       |
| 3       | TIMER3      | N    | 16-bit Timer Interrupt                                                                                       |
| 4       | Reserved    | N    | Reserved                                                                                                     |
| 5       | PFR         | N    | Power Fail Register Interrupt                                                                                |
| 6       | Reserved    | N    | Reserved                                                                                                     |
| 7       | WEEK_ALR    | Y    | Week Alarm Interrupt. Week Timer has reached it's terminal count.                                            |
| 8       | VCI_OVRD_IN | Y    | Pin input of VCI_OVRD_IN                                                                                     |
| 9       | VCI_IN0     | Y    | input of VCI_IN0# pins                                                                                       |
| 10      | VCI_IN1     | Y    | input of VCI_IN1# pins                                                                                       |
| 11      | VCI_IN2     | Y    | input of VCI_IN2# pins                                                                                       |
| 12      | VCI_IN3     | Y    | input of VCI_IN3# pins                                                                                       |
| 13      | HTIMER0     | Y    | Hibernation Timer Interrupt. This interrupt is signaled when the hibernation timer has counter down to zero. |
| 14      | HTIMER1     | Y    | Hibernation Timer Interrupt. This interrupt is signaled when the hibernation timer has counter down to zero. |
| [30:15] | Reserved    | N    | Reserved                                                                                                     |
| 31      | Reserved    | N    | This bit is always reserved                                                                                  |

### 16.6.72 IRQ31 Enable Register

**Table 16.98 IRQ31 Enable Register**

| HOST ADDRESS | N/A      |                                                                                            |     |            |     |     | HOST SIZE           |     |
|--------------|----------|--------------------------------------------------------------------------------------------|-----|------------|-----|-----|---------------------|-----|
| EC OFFSET    | 118h     |                                                                                            |     | 32-bit     |     |     | EC SIZE             |     |
| POWER        | VTR      |                                                                                            |     | 0000_0000h |     |     | nSYS_RST<br>DEFAULT |     |
| BUS          | EC SPB   |                                                                                            |     |            |     |     |                     |     |
| BIT          | D31      | D30                                                                                        | D29 | ■          | ■   | D2  | D1                  | D0  |
| HOST TYPE    | -        | -                                                                                          | -   | -          | -   | -   | -                   | -   |
| EC TYPE      | R        | R/W                                                                                        | R/W | R/W        | R/W | R/W | R/W                 | R/W |
| BIT NAME     | Reserved | Refer To <a href="#">Table 16.97, “Bit definitions IRQ31 Source Register,” on page 361</a> |     |            |     |     |                     |     |

## 16.6.73 IRQ31 Result Register

I

Table 16.99 IRQ31 Result Register

| HOST ADDRESS |        |                                                                                            |     |                                                                                   |                                                                                     |    |    | HOST SIZE           |
|--------------|--------|--------------------------------------------------------------------------------------------|-----|-----------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|----|----|---------------------|
| EC OFFSET    | 11Ch   |                                                                                            |     |                                                                                   | 32-bit                                                                              |    |    | EC SIZE             |
| POWER        | VTR    |                                                                                            |     |                                                                                   | 0000_0000h                                                                          |    |    | nSYS_RST<br>DEFAULT |
| BUS          | EC SPB |                                                                                            |     |                                                                                   |                                                                                     |    |    |                     |
| BIT          | D31    | D30                                                                                        | D29 |  |  | D2 | D1 | D0                  |
| HOST TYPE    | -      | -                                                                                          | -   | -                                                                                 | -                                                                                   | -  | -  | -                   |
| EC TYPE      | R/W-   | R                                                                                          | R   | R                                                                                 | R                                                                                   | R  | R  | R                   |
| BIT NAME     | NORM   | Refer To <a href="#">Table 16.97, “Bit definitions IRQ31 Source Register,”</a> on page 361 |     |                                                                                   |                                                                                     |    |    |                     |

### Bit 31 NORM

This bit is a read write bit used by the NORM instruction.

## 16.6.74 Bank Select Register

**Table 16.100 Block Select register**

| HOST ADDRESS |          |        |        |            |        |        | HOST SIZE           |        |
|--------------|----------|--------|--------|------------|--------|--------|---------------------|--------|
| EC OFFSET    | 120h     |        |        | 32-bit     |        |        | EC SIZE             |        |
| POWER        | VTR      |        |        | FFFF_FF00h |        |        | nSYS_RST<br>DEFAULT |        |
| BUS          | EC SPB   |        |        |            |        |        |                     |        |
| BYTE3 BIT    | D31      | D30    | D29    | D28        | D27    | D26    | D25                 | D24    |
| HOST TYPE    | -        | -      | -      | -          | -      | -      | -                   | -      |
| EC TYPE      | R/W      | R/W    | R/W    | R/W        | R/W    | R/W    | R/W                 | R/W    |
| BIT NAME     | IRQ 31   | IRQ 30 | IRQ 29 | IRQ 28     | REQ 27 | IRQ 26 | IRQ 25              | IRQ 24 |
| BYTE2 BIT    | D23      | D22    | D21    | D20        | D19    | D18    | D17                 | D16    |
| HOST TYPE    | -        | -      | -      | -          | -      | -      | -                   | -      |
| EC TYPE      | R/W      | R/W    | R/W    | R/W        | R/W    | R/W    | R/W                 | R/W    |
| BIT NAME     | IRQ 23   | IRQ 22 | IRQ 21 | IRQ 20     | IRQ 19 | IRQ 18 | IRQ 17              | IRQ 16 |
| BYTE1 BIT    | D15      | D14    | D13    | D12        | D11    | D10    | D9                  | D8     |
| HOST TYPE    | -        | -      | -      | -          | -      | -      | -                   | -      |
| EC TYPE      | R/W      | R/W    | R/W    | R/W        | R/W    | R/W    | R/W                 | R/W    |
| BIT NAME     | IRQ 15   | IRQ 14 | IRQ 13 | IRQ 12     | IRQ 11 | IRQ 10 | IRQ 9               | IRQ 8  |
| BYTE0 BIT    | D7       | D6     | D5     | D4         | D3     | D2     | D1                  | D0     |
| HOST TYPE    | -        | -      | -      | -          | -      | -      | -                   | -      |
| EC TYPE      | R        | R      | R      | R          | R      | R      | R                   | R      |
| BIT NAME     | Reserved |        |        |            |        |        |                     |        |

0 All Interrupts in the associated IRQ will be disabled

1 All Interrupts in the associated IRQ will be enabled

## 16.7 EC Interrupt Aggregator Revision History

This revision history shows the changes made to this chapter.

**Table 16.101 EC Interrupt Aggregator Chapter Revision History**

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History," on page 539.</a> |              |            |                                                                                                                                                                                                                                                     |                                                                                                                                                     |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE       | SECTION/FIGURE/ENTRY                                                                                                                                                                                                                                | CORRECTION                                                                                                                                          |
| 1.                                                                                                                                                                                                                                          | 0.04         | 04/25/2007 | <a href="#">PFR on page 362</a>                                                                                                                                                                                                                     | This interrupts are not wake capable.                                                                                                               |
| 2.                                                                                                                                                                                                                                          | 0.4          | 04/25/2007 | <a href="#">Table 16.1, "EC Interrupt Structure," on page 306</a><br><a href="#">Table 16.100, "Block Select register," on page 364</a>                                                                                                             | Editorial change: Arc interrupt IRQ[4:7] are reserved.<br>Change default value <a href="#">Block Select register</a> from FFFF_FFF0h to FFFF_FF00h. |
| 3.                                                                                                                                                                                                                                          |              | 5/9/2007   | <a href="#">Section 16.3.2, "Clocks," on page 305</a><br><a href="#">Section 16.3.3, "Reset," on page 306</a><br><a href="#">Section 16.3.4, "Interrupt Routing," on page 306</a><br><a href="#">Section 16.3.5, "WAKE Generation," on page 306</a> | Reorganized and added content and xrefs                                                                                                             |
| 4.                                                                                                                                                                                                                                          |              |            |                                                                                                                                                                                                                                                     |                                                                                                                                                     |



## Chapter 17 GPIO Interface

### 17.1 General Description

17.2 This block provides GPIO input monitoring and output controls, as well as, pin signal function multiplexing control, asynchronous wakeup, and synchronous interrupt controls for the MEC5035. In addition this block provides

- 101 General Purpose I/O Pin signals.
- General Purpose Inputs
  - Asynchronous edge rising and falling edge wakeup detection
  - High or Low Level Interrupts
- General Purpose Outputs
  - Push Pull output, or
  - Open Drain output
- Pull up or pull down control
- Interrupts available for all GPIOs
- Multiplex control for all GPIOs
- [GPIO Pass-Through Ports](#) for 8 GPIOs

The [GPIO Interface](#) routes pin inputs to WAKE Events outputs which can be programmed using the associated [Pin Control Register](#) and the [EC Interrupt Aggregator](#). This logic requires no clocks. See [Chapter 16, "EC Interrupt Aggregator,"](#) on page 304.

## 17.3 Block Diagram

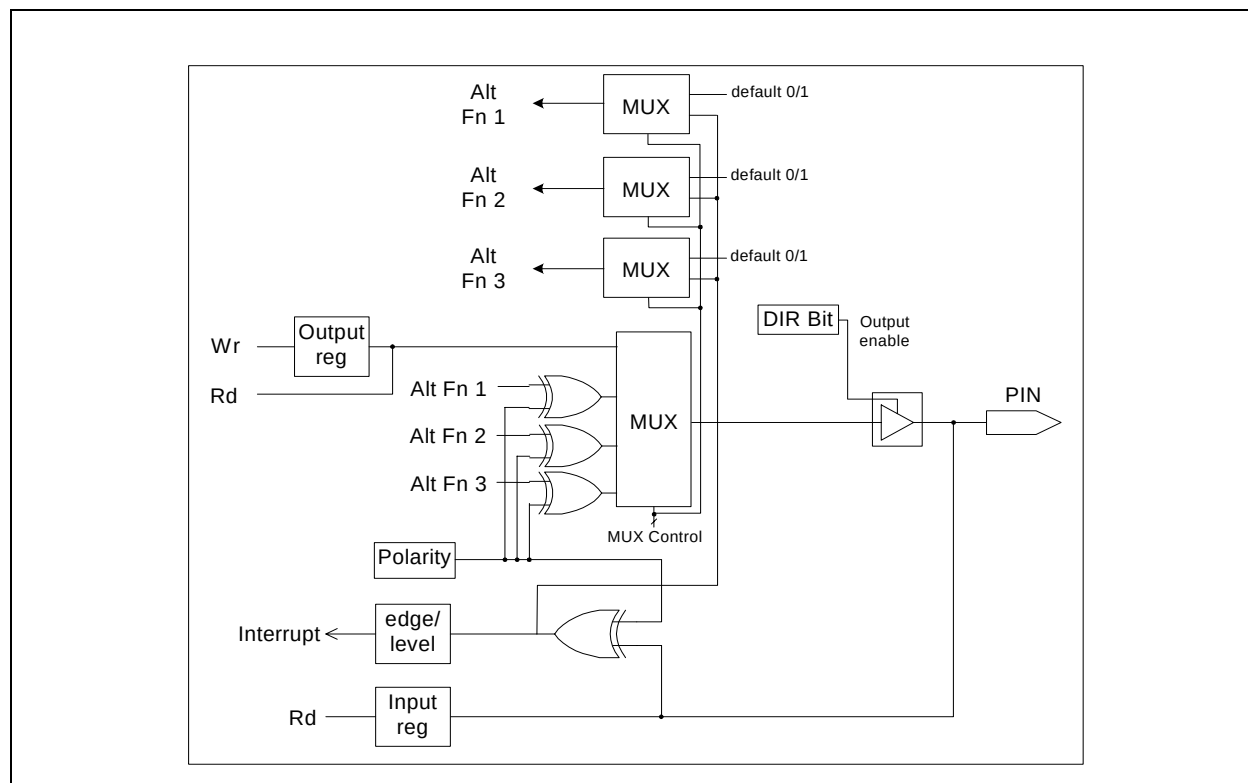


Figure 17.1 GPIO Interface Block Diagram

## 17.4 Detailed Pin Muxing assignments.

All Pin Signal Function muxing, GPIO outputs and inputs are controlled by the GPIO octal numbering assignment. In the MEC5035 all GPIO number assignments are related to pin assignments as follows:

The pinout is divided into four quadrants pins 1:32, 33:64, 65:96, 97:128. The first pin in each quadrant (pins 1, 33, 65, & 97) follows the following formula: GPIO OCTAL NUMBER = OCTAL (decimal pin number - 1). The remainder of the pins in each quadrant increment the GPIO Octal Numbering. Power pins and other pins are skipped. The unused GPIO Octal numbers are reserved.

**Note 17.1** The following pin is the exception to the Programmable OD/PP Muxing Design Rule defined in [Note 17.5 on page 377](#).

The notes in [Table 17.1](#) - [Table 17.4](#) are listed below:

|               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Note9</b>  | When the JTAG_RST# pin is deasserted (logic'1'), the JTAG_TDI, JTAG_TDO, JTAG_CLK, JTAG_TMS signal functions in the JTAG interface are unconditionally routed to the JTAG signal functions; the Pin Control register for these pins has no effect. When the JTAG_RST# pin is asserted (logic'0'), the JTAG_TDI, JTAG_TDO, JTAG_CLK, JTAG_TMS signal functions in the JTAG interface are not routed to the interface and the Pin Control Register for these pins controls the muxing. The pin control registers can not route the JTAG interface to the pins. System Board Designer should terminate this pin in all functional state using jumpers and pull-up or pull down resistors, etc . |
| <b>Note10</b> | All VBAT powered pins with GPIO's on then have only one direction selected by the default signal function. The associated GPIO input register, output register bits are not connected to the pin. Only the Interrupt Detection field in the associated pin control register function is functional; the remainder of the bits in the pin control register has no effect.                                                                                                                                                                                                                                                                                                                     |
| <b>Note11</b> | PS/2 ports ending with signal functions ending with "A" or "B" are muxed to a single controller. Only one set of clock and data are intended to used at a time (either "A" or "B") not both. The unused port segment should have its associated pin control register's, Mux Control Field programmed away from the PS2 controller.                                                                                                                                                                                                                                                                                                                                                           |
| <b>Note12</b> | Most GPIO's are (I/O/OD). See Multiplexing tables below and associated notes for specific exceptions.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| <b>Note13</b> | GPIO assignments on this pin is present only to provide interrupt and wakeup capability. This is provided by the Interrupt Detection field in the Pin Control register. The Mux control field in the Pin Control Register should <b>not</b> be set to '00' = GPIO or undesirable results may occur.                                                                                                                                                                                                                                                                                                                                                                                          |
| <b>Note14</b> | This pin has no internal pullup or pulldown capability. The PU/PD Enable Bits in the associated Pin Control Register has no effect. This pin has no input hysteresis; therefore, signals with slow rise and fall times (usecs) will retrigger interrupts.                                                                                                                                                                                                                                                                                                                                                                                                                                    |



## Product Customer Specification-ODM

Table 17.1 Pin Control Muxing Package Pin[1:32]

| 128 pins<br>MEC<br>5035 | gpio<br>octal<br>number | Pin<br>Control<br>Reg<br>offset | Pin<br>Control<br>Reg POR<br>Value | POR signal<br>function | Mux<br>control<br>= 00 | Mux control<br>= 01 | Mux<br>control =<br>10 | Mux<br>control =<br>11 | Notes  |
|-------------------------|-------------------------|---------------------------------|------------------------------------|------------------------|------------------------|---------------------|------------------------|------------------------|--------|
| 1                       | GPIO000                 | 0000                            | 00001000                           | VCI_IN3#               | GPIO000                | VCI_IN3#            | reserved               | reserved               | Note10 |
| 2                       | GPIO001                 | 0004                            | 00000000                           | GPIO001                | GPIO001                | reserved            | reserved               | reserved               |        |
| 3                       | GPIO002                 | 0008                            | 00000000                           | GPIO002                | GPIO002                | reserved            | reserved               | reserved               |        |
| 4                       |                         |                                 | reserved                           |                        |                        |                     |                        |                        |        |
| 5                       | GPIO003                 | 000C                            | 00000000                           | GPIO003                | GPIO003                | I2C1A_DATA          | reserved               | reserved               |        |
| 6                       | GPIO004                 | 0010                            | 00000000                           | GPIO004                | GPIO004                | I2C1A_CLK           | reserved               | reserved               |        |
| 7                       | GPIO005                 | 0014                            | 00000000                           | GPIO005                | GPIO005                | I2C1B_DATA          | reserved               | reserved               |        |
| 8                       | GPIO006                 | 0018                            | 00000000                           | GPIO006                | GPIO006                | I2C1B_CLK           | reserved               | reserved               |        |
| 9                       | GPIO007                 | 001C                            | 00000000                           | GPIO007                | GPIO007                | I2C1D_DATA          | PS2_CLK0B              | reserved               |        |
| 10                      | GPIO010                 | 0020                            | 00000000                           | GPIO010                | GPIO010                | I2C1D_CLK           | PS2_DAT0B              | reserved               |        |
| 11                      | GPIO011                 | 0024                            | 00000000                           | GPIO011                | GPIO011                | nSMI                | reserved               | reserved               |        |
| 12                      | GPIO012                 | 0028                            | 00000000                           | GPIO012                | GPIO012                | I2C1H_DATA          | I2C2D_DATA             | reserved               |        |
| 13                      | GPIO013                 | 002C                            | 00000000                           | GPIO013                | GPIO013                | I2C1H_CLK           | I2C2D_CLK              | reserved               |        |
| 14                      | GPIO014                 | 0030                            | 00000000                           | GPIO014                | GPIO014                | GPTP-IN7            | reserved               | reserved               |        |
| 15                      | GPIO015                 | 0034                            | 00000000                           | GPIO015                | GPIO015                | GPTP-OUT7           | reserved               | reserved               |        |
| 16                      | GPIO016                 | 0038                            | 00000000                           | GPIO016                | GPIO016                | GPTP-IN8            | reserved               | reserved               |        |
| 17                      | GPIO017                 | 003C                            | 00000000                           | GPIO017                | GPIO017                | GPTP-OUT8           | reserved               | reserved               |        |
| 18                      | GPIO020                 | 0040                            | 00000000                           | GPIO020                | GPIO020                | reserved            | reserved               | reserved               |        |
| 19                      | GPIO021                 | 0044                            | 00000000                           | GPIO021                | GPIO021                | RC_ID               | reserved               | reserved               |        |
| 20                      |                         |                                 | reserved                           |                        |                        |                     |                        |                        |        |
| 21                      |                         |                                 | reserved                           |                        |                        |                     |                        |                        |        |
| 22                      |                         |                                 | reserved                           |                        |                        |                     |                        |                        |        |
| 23                      | GPIO022                 | 0048                            | 00000000                           | GPIO022                | GPIO022                | BCM_B_CLK           |                        | reserved               |        |
| 24                      | GPIO023                 | 004C                            | 00000000                           | GPIO023                | GPIO023                | BCM_B_DAT           |                        | reserved               |        |
| 25                      | GPIO024                 | 0050                            | 00000000                           | GPIO024                | GPIO024                | BCM_B_INT#          |                        | reserved               |        |
| 26                      |                         |                                 | reserved                           | VSS[1]                 | VSS[1]                 | reserved            | reserved               | reserved               |        |
| 27                      | GPIO025                 | 0054                            | 00000000                           | GPIO025                | GPIO025                | UART_CLK            | reserved               | reserved               |        |
| 28                      | GPIO026                 | 0058                            | 00000000                           | GPIO026                | GPIO026                | GPTP-IN1            | reserved               | reserved               |        |
| 29                      | GPIO027                 | 005C                            | 00000000                           | GPIO027                | GPIO027                | GPTP-OUT1           | reserved               | reserved               |        |
| 30                      | GPIO030                 | 0060                            | 00000000                           | GPIO030                | GPIO030                | GPTP-IN2            | reserved               | reserved               |        |
| 31                      | GPIO031                 | 0064                            | 00000000                           | GPIO031                | GPIO031                | GPTP-OUT2           | reserved               | reserved               |        |
| 32                      | GPIO032                 | 0068                            | 00000000                           | GPIO032                | GPIO032                | GPTP-IN3            | reserved               | reserved               |        |



Table 17.2 Pin Control Muxing Package Pin[33:64]

| 128 pins<br>MEC<br>5035 | gpio<br>octal<br>number | Pin<br>Control<br>Reg<br>offset | Pin<br>Control<br>Reg POR<br>Value | POR signal<br>function | Mux<br>control<br>= 00 | Mux control<br>= 01 | Mux<br>control =<br>10 | Mux<br>control =<br>11 | Notes            |
|-------------------------|-------------------------|---------------------------------|------------------------------------|------------------------|------------------------|---------------------|------------------------|------------------------|------------------|
| 33                      | GPIO040                 | 0080                            | 00000000                           | GPIO040                | GPIO040                | GPTP-OUT3           | reserved               | reserved               |                  |
| 34                      | GPIO041                 | 0084                            | 00000000                           | GPIO041                | GPIO041                | reserved            | reserved               | reserved               |                  |
| 35                      | GPIO042                 | 0088                            | 00000000                           | GPIO042                | GPIO042                | BCM_C_INT#          | reserved               | reserved               |                  |
| 36                      | GPIO043                 | 008C                            | 00000000                           | GPIO043                | GPIO043                | BCM_C_DAT           | reserved               | reserved               |                  |
| 37                      | GPIO044                 | 0090                            | 00000000                           | GPIO044                | GPIO044                | BCM_C_CLK           | reserved               | reserved               |                  |
| 38                      | GPIO045                 | 0094                            | 00000000                           | GPIO045                | GPIO045                | LSBCM_D_IN<br>T#    | reserved               | reserved               |                  |
| 39                      | GPIO046                 | 0098                            | 00000000                           | GPIO046                | GPIO046                | LSBCM_D_DA<br>T     | reserved               | reserved               |                  |
| 40                      | GPIO047                 | 009C                            | 00000000                           | GPIO047                | GPIO047                | LSBCM_D_CL<br>K     | reserved               | reserved               |                  |
| 41                      | GPIO050                 | 00A0                            | 00000000                           | GPIO050                | GPIO050                | FAN_TACH1           | reserved               | reserved               |                  |
| 42                      | GPIO051                 | 00A4                            | 00000000                           | GPIO051                | GPIO051                | FAN_TACH2           | reserved               | reserved               |                  |
| 43                      | GPIO052                 | 00A8                            | 00000000                           | GPIO052                | GPIO052                | FAN_TACH3           | reserved               | reserved               |                  |
| 44                      |                         |                                 | reserved                           | VTR[2]                 | VTR[2]                 | reserved            | reserved               | reserved               |                  |
| 45                      | GPIO053                 | 00AC                            | 00000000                           | GPIO053                | GPIO053                | PWM0                | reserved               | reserved               |                  |
| 46                      | GPIO054                 | 00B0                            | 00000000                           | GPIO054                | GPIO054                | PWM1                | reserved               | reserved               |                  |
| 47                      | GPIO055                 | 00B4                            | 00000000                           | GPIO055                | GPIO055                | PWM2                | reserved               | reserved               |                  |
| 48                      | GPIO056                 | 00B8                            | 00000000                           | GPIO056                | GPIO056                | PWM3                | reserved               | reserved               |                  |
| 49                      | GPIO057                 | 00BC                            | 00001000                           | VCC_PWRGD              | GPIO057                | VCC_PWRGD           | reserved               | reserved               | Note13           |
| 50                      | GPIO060                 | 00C0                            | 00000000                           | GPIO060                | GPIO060                | KBRST               | reserved               | reserved               |                  |
| 51                      |                         |                                 | reserved                           | VSS[2]                 |                        |                     |                        |                        |                  |
| 52                      |                         |                                 | reserved                           | VTR[8]                 |                        |                     |                        |                        |                  |
| 53                      |                         |                                 | reserved                           | VSS[8]                 |                        |                     |                        |                        |                  |
| 54                      | GPIO061                 | 00C4                            | 00000000                           | GPIO061                | GPIO061                | LPCPD#              | reserved               | reserved               |                  |
| 55                      | GPIO062                 | 00C8                            | 00001000                           | LDRQ#                  | GPIO062                | LDRQ#               | reserved               | reserved               | Note13<br>Note14 |
| 56                      | GPIO063                 | 00CC                            | 00001000                           | SER_IRQ                | GPIO063                | SER_IRQ             | reserved               | reserved               | Note13<br>Note14 |
| 57                      | GPIO064                 | 00D0                            | 00001000                           | LRESET#                | GPIO064                | LRESET#             | reserved               | reserved               | Note13<br>Note14 |
| 58                      | GPIO065                 | 00D4                            | 00001000                           | PCI_CLK                | GPIO065                | PCI_CLK             | reserved               | reserved               | Note13<br>Note14 |
| 59                      | GPIO066                 | 00D8                            | 00001000                           | LFRAME#                | GPIO066                | LFRAME#             | reserved               | reserved               | Note13<br>Note14 |
| 60                      |                         |                                 | reserved                           | LAD0                   |                        |                     |                        |                        |                  |
| 61                      |                         |                                 | reserved                           | LAD1                   |                        |                     |                        |                        |                  |
| 62                      |                         |                                 | reserved                           | LAD2                   |                        |                     |                        |                        |                  |
| 63                      |                         |                                 | reserved                           | LAD3                   |                        |                     |                        |                        |                  |
| 64                      | GPIO067                 | 00DC                            | 00001000                           | CLKRUN#                | GPIO067                | CLKRUN#             | reserved               | reserved               | Note13<br>Note14 |



Table 17.3 Pin Control Muxing Package Pin[65:96]

| 128 pins<br>MEC<br>5035 | gpio<br>octal<br>number | Pin<br>Control<br>Reg<br>offset | Pin<br>Control<br>Reg POR<br>Value | POR signal<br>function | Mux<br>control<br>= 00 | Mux control<br>= 01 | Mux<br>control =<br>10 | Mux<br>control =<br>11 | Notes |
|-------------------------|-------------------------|---------------------------------|------------------------------------|------------------------|------------------------|---------------------|------------------------|------------------------|-------|
| 65                      |                         |                                 | reserved                           | VTR[3]                 |                        |                     |                        |                        |       |
| 66                      | GPIO100                 | 0100                            | 00000000                           | GPIO100                | GPIO100                | nEC_SCI             | reserved               | reserved               |       |
| 67                      | GPIO101                 | 0104                            | 00000000                           | GPIO101                | GPIO101                | ECGP_SCLK           | reserved               | reserved               |       |
| 68                      | GPIO102                 | 0108                            | 00000000                           | GPIO102                | GPIO102                | ECGP_SOUT           | reserved               | reserved               |       |
| 69                      | GPIO103                 | 010C                            | 00000000                           | GPIO103                | GPIO103                | ECGP_SIN            | reserved               | reserved               |       |
| 70                      | GPIO104                 | 0110                            | 00000000                           | GPIO104                | GPIO104                | UART_TX             | reserved               | reserved               |       |
| 71                      | GPIO105                 | 0114                            | 00000000                           | GPIO105                | GPIO105                | UART_RX             | reserved               | reserved               |       |
| 72                      | GPIO106                 | 0118                            | 00000000                           | GPIO106                | GPIO106                | nRESET_OUT          | reserved               | reserved               |       |
| 73                      | GPIO107                 | 011C                            | 00000000                           | GPIO107                | GPIO107                | reserved            | reserved               | reserved               |       |
| 74                      |                         |                                 | reserved                           | VSS[3]                 |                        |                     |                        |                        |       |
| 75                      | GPIO110                 | 0120                            | 00000000                           | GPIO110                | GPIO110                | PS2_CLK2            | GPTP-IN6               | reserved               |       |
| 76                      | GPIO111                 | 0124                            | 00000000                           | GPIO111                | GPIO111                | PS2_DAT2            | GPTP-OUT6              | reserved               |       |
| 77                      | GPIO112                 | 0128                            | 00000000                           | GPIO112                | GPIO112                | PS2_CLK1A           | reserved               | reserved               |       |
| 78                      | GPIO113                 | 012C                            | 00000000                           | GPIO113                | GPIO113                | PS2_DAT1A           | reserved               | reserved               |       |
| 79                      | GPIO114                 | 0130                            | 00000000                           | GPIO114                | GPIO114                | PS2_CLK0A           | reserved               | reserved               |       |
| 80                      | GPIO115                 | 0134                            | 00000000                           | GPIO115                | GPIO115                | PS2_DAT0A           | reserved               | reserved               |       |
| 81                      | GPIO116                 | 0138                            | 00000000                           | GPIO116                | GPIO116                | MSDATA              | reserved               | reserved               |       |
| 82                      | GPIO117                 | 013C                            | 00000000                           | GPIO117                | GPIO117                | MSCLK               | reserved               | reserved               |       |
| 83                      |                         |                                 | 00000000                           | VTR[4]                 |                        |                     |                        |                        |       |
| 84                      | GPIO120                 | 0140                            | 00000000                           | GPIO120                | GPIO120                | reserved            | reserved               | reserved               |       |
| 85                      | GPIO121                 | 0144                            | 00000000                           | GPIO121                | GPIO121                | BCM_A_INT#          | reserved               | reserved               |       |
| 86                      | GPIO122                 | 0148                            | 00000000                           | GPIO122                | GPIO122                | BCM_A_DAT           | reserved               | reserved               |       |
| 87                      | GPIO123                 | 014C                            | 00000000                           | GPIO123                | GPIO123                | BCM_A_CLK           | reserved               | reserved               |       |
| 88                      |                         |                                 | 00000000                           | VSS[4]                 |                        |                     |                        |                        |       |
| 89                      | GPIO124                 | 0150                            | 00000000                           | GPIO124                | GPIO124                | GPTP-OUT5           | reserved               | reserved               |       |
| 90                      | GPIO125                 | 0154                            | 00000000                           | GPIO125                | GPIO125                | GPTP-IN5            | reserved               | reserved               |       |
| 91                      | GPIO126                 | 0158                            | 00000000                           | GPIO126                | GPIO126                | reserved            | reserved               | reserved               |       |
| 92                      | GPIO127                 | 015C                            | 00000000                           | GPIO127                | GPIO127                | A20M                | reserved               | reserved               |       |
| 93                      | GPIO130                 | 0160                            | 00000000                           | GPIO130                | GPIO130                | I2C2A_DAT           | reserved               | reserved               |       |
| 94                      | GPIO131                 | 0164                            | 00000000                           | GPIO131                | GPIO131                | I2C2A_CLK           | reserved               | reserved               |       |
| 95                      | GPIO132                 | 0168                            | 00000000                           | GPIO132                | GPIO132                | I2C1G_DATA          | reserved               | reserved               |       |
| 96                      | GPIO140                 | 0180                            | 00000000                           | GPIO140                | GPIO140                | I2C1G_CLK           | reserved               | reserved               |       |



Table 17.4 Pin Control Muxing Package Pin[97:128]

| 128 pins<br>MEC<br>5035 | gpio<br>octal<br>number | Pin<br>Control<br>Reg<br>offset | Pin<br>Control<br>Reg POR<br>Value | POR signal<br>function | Mux<br>control<br>= 00 | Mux control<br>= 01 | Mux<br>control =<br>10 | Mux<br>control =<br>11 | Notes  |
|-------------------------|-------------------------|---------------------------------|------------------------------------|------------------------|------------------------|---------------------|------------------------|------------------------|--------|
| 97                      | GPIO141                 | 0184                            | 00000000                           | GPIO141                | GPIO141                | I2C1F_DATA          | I2C2B_DATA             | reserved               |        |
| 98                      | GPIO142                 | 0188                            | 00000000                           | GPIO142                | GPIO142                | I2C1F_CLK           | I2C2B_CLK              | reserved               |        |
| 99                      | GPIO143                 | 018C                            | 00000000                           | GPIO143                | GPIO143                | I2C1E_DATA          | reserved               | reserved               |        |
| 100                     | GPIO144                 | 0190                            | 00000000                           | GPIO144                | GPIO144                | I2C1E_CLK           | reserved               | reserved               |        |
| 101                     |                         |                                 | reserved                           | VSS_RO                 |                        |                     |                        |                        |        |
| 102                     | GPIO145                 | 0194                            | 00000000                           | GPIO145                | GPIO145                | I2C1K_DATA          | JTAG_TDI               | reserved               | Note9  |
| 103                     | GPIO146                 | 0198                            | 00000000                           | GPIO146                | GPIO146                | I2C1K_CLK           | JTAG_TDO               | reserved               | Note9  |
| 104                     |                         |                                 | reserved                           | VTR[6]                 |                        |                     |                        |                        |        |
| 105                     | GPIO147                 | 019C                            | 00000000                           | GPIO147                | GPIO147                | I2C1J_DATA          | I2C2C_DATA             | JTAG_CLK               | Note9  |
| 106                     | GPIO150                 | 01A0                            | 00000000                           | GPIO150                | GPIO150                | I2C1J_CLK           | I2C2C_CLK              | JTAG_TMS               | Note9  |
| 107                     |                         |                                 | reserved                           | JTAG_RST#              |                        |                     |                        |                        | Note9  |
| 108                     | GPIO151                 | 01A4                            | 00000000                           | GPIO151                | GPIO151                | GPTP-IN4            | reserved               | reserved               |        |
| 109                     | GPIO152                 | 01A8                            | 00000000                           | GPIO152                | GPIO152                | GPTP-OUT4           | reserved               | reserved               |        |
| 110                     | GPIO153                 | 01AC                            | 00000000                           | GPIO153                | GPIO153                | LED3                | reserved               | reserved               |        |
| 111                     | GPIO154                 | 01B0                            | 00000000                           | GPIO154                | GPIO154                | I2C1C_DATA          | PS2_CLK1B              | reserved               |        |
| 112                     | GPIO155                 | 01B4                            | 00000000                           | GPIO155                | GPIO155                | I2C1C_CLK           | PS2_DAT1B              | reserved               |        |
| 113                     |                         |                                 | reserved                           | VSS[5]                 |                        |                     |                        |                        |        |
| 114                     | GPIO156                 | 01B8                            | 00000000                           | GPIO156                | GPIO156                | LED1                | reserved               | reserved               |        |
| 115                     | GPIO157                 | 01BC                            | 00000000                           | GPIO157                | GPIO157                | LED2                | reserved               | reserved               |        |
| 116                     |                         |                                 | reserved                           | VTR[5]                 |                        |                     |                        |                        |        |
| 117                     | GPIO160                 | 01C0                            | 00000000                           | GPIO160                | GPIO160                | 32KHZ_OUT           | reserved               | reserved               |        |
| 118                     |                         |                                 | reserved                           | BGPO0                  |                        | BGPO0               | reserved               | reserved               |        |
| 119                     | GPIO161                 | 01C4                            | 00001000                           | VCI_IN2#               | GPIO161                | VCI_IN2#            | reserved               | reserved               | Note10 |
| 120                     |                         |                                 | reserved                           | VCI_OUT                |                        |                     |                        |                        |        |
| 121                     |                         |                                 | reserved                           | VBAT                   |                        |                     |                        |                        |        |
| 122                     |                         |                                 | reserved                           | XTAL1                  |                        |                     |                        |                        |        |
| 123                     |                         |                                 | reserved                           | nFWP                   |                        |                     |                        |                        |        |
| 124                     |                         |                                 | reserved                           | XTAL2                  |                        |                     |                        |                        |        |
| 125                     |                         |                                 | reserved                           | AGND                   |                        |                     |                        |                        |        |
| 126                     | GPIO162                 | 01C8                            | 00001000                           | VCI_IN1#               | GPIO162                | VCI_IN1#            | reserved               | reserved               | Note10 |
| 127                     | GPIO163                 | 01CC                            | 00001000                           | VCI_IN0#               | GPIO163                | VCI_IN0#            | reserved               | reserved               | Note10 |
| 128                     | GPIO164                 | 01D0                            | 00001000                           | VCI_OVRD_IN            | GPIO164                | VCI_OVRD_IN         | reserved               | reserved               | Note10 |

## 17.5 Power, Clocks and Reset

### 17.5.1 Power Domain

This block is powered by the VTR Power Supply.

See [Section 4.5, "Power Configuration," on page 96](#) for details on power domains.

### 17.5.2 Clocks

This block uses the [EC Bus Clock](#) and the 64.52MHz [MCLK](#). [EC Bus Clock](#) is used for access to registers. The [MCLK](#) is used for synchronizing the GPIO inputs.

See [Section 4.4, "Clock Generator," on page 77](#) for details on clocks.

### 17.5.3 Reset

This block is reset on a [nSYS\\_RST](#). On reset, all Registers are reset to their default values.

See [Section 4.6, "Reset Interface," on page 99](#) for details on reset.

## 17.6 Interrupts

Each [GPIO Interface](#) has both an interrupt and/or a Wake-up event. The interrupt source is routed onto the GPIO Status Bits corresponding to the GPIO in the [IRQ8 Source Register - IRQ11 Source Register on page 322](#). The GPIO's can generate an interrupt on a high level, low level, rising edge and falling edge, as configured by the [Interrupt Detection](#) bits in the [Pin Control Register \[000:176\]](#) associated with the GPIO signal function.

**Note 17.2** The minimum GPIO signal pulse width guaranteed to be detected is 5ns. No filtering is done to prevent detection of narrower signals.

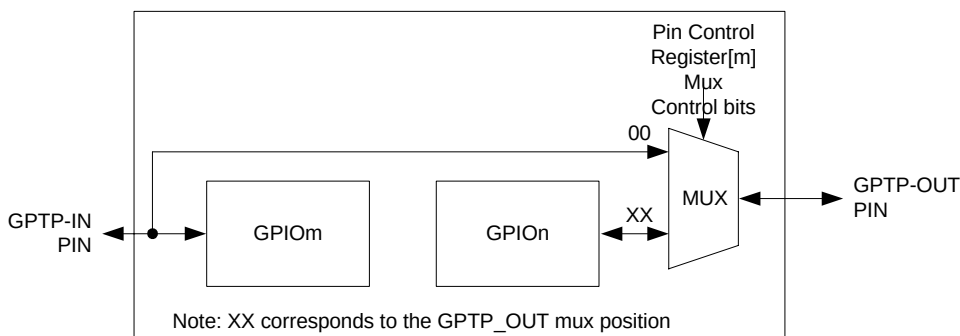
## 17.7 GPIO Pass-Through Ports

[GPIO Pass-Through Ports](#) (GPTP) can multiplex two general purpose I/O pins as shown in [Figure 17.2. GPIO Pass-Through Ports](#) connect the GPTP-IN pin to the GPTP-OUT pin. The eight pin pairs are listed in [Table 3.7, "GPIO Interface," on page 43](#). The GPTP are sequentially assigned values 1:8. The GPTP port assignment have no relation to the GPIO octal assignments. The GPTP ports are controlled by the [Mux Control](#) bits in the [Pin Control Register \[000:176\]](#) associated with the GPTP-OUT signal function.

In order to enable the GPTP Pass-Through Mode the following steps are required:

1. The GPIO's Pin Control Register[m] (associated with the GPTP-IN signal function) must assign [Mux Control](#) field = 00 (gpio) and [GPIO](#) bit = 0 (input)
2. the GPIO's Pin Control Register[n] (associated with the GPTP-OUT signal function) must assign [Mux Control](#) field = "GPTP-OUT". The [Mux Control](#) field = "GPTP-OUT" can differ from pin to pin. For each pin, the [Mux Control](#) value is identified by the column heading in which the "GPTP-OUT" signal function is located in the tables in [Section 17.4, "Detailed Pin Muxing assignments., on page 367](#).




**Figure 17.2 GPIO Pass-Through Port Example**

**Note:** This figure is for illustration purposes only and is not intended to suggest specific implementation details.

**Note 17.3** When Pass-Through Mode is enabled, the GPIOn output is disconnected from the GPIOn pin and the GPIOm pin signal appears on GPIOn pin. Note that in this case the GPIOm input register still reflects the state of the GPIOm pin.

## 17.8 Registers

The [GPIO Interface](#) has its own Logical Device Number, and Base Address as indicated in [Table 17.5](#). [Table 17.6](#) is a register summary for the [GPIO Interface](#) block.

**Table 17.5 GPIO Interface Base Address Table**

| <a href="#">GPIO Interface BLOCKS</a> | LDN FROM<br>( <a href="#">Table 7.2</a> on<br>page 167) | AHB BASE ADDRESS         |
|---------------------------------------|---------------------------------------------------------|--------------------------|
| <b>GPIO Interface 1</b>               | 31h                                                     | <a href="#">F0_C400h</a> |

[Table 17.6](#) is a register summary for the [GPIO Interface](#) block. Each EC address is indicated as an SPB Offset from its AHB base address.



Table 17.6 GPIO Interface Register Summary

|                                | 1             | EC<br>INTE<br>RFAC<br>E |            | NOTES |
|--------------------------------|---------------|-------------------------|------------|-------|
| REGISTER NAME                  | SPB<br>OFFSET | BYTE<br>LANE            | EC<br>TYPE |       |
| Pin Control Register [000:176] | 0000h - 01FCh | 0-3                     | R/W        |       |
| GPIO[000:036] Output Register  | 200h          | 0-3                     | R/W        |       |
| GPIO[040:076] Output Register  | 204h          | 0-3                     | R/W        |       |
| GPIO[100:136] Output Register  | 208h          | 0-3                     | R/W        |       |
| GPIO[140:176] Output Register  | 20Ch          | 0-3                     | R/W        |       |
| GPIO[000:036] Input Register   | 210h          | 0-3                     | R/W        |       |
| GPIO[040:076] Input Register   | 214h          | 0-3                     | R/W        |       |
| GPIO[100:136] Input Register   | 218h          | 0-3                     | R/W        |       |
| GPIO[140:176] Input Register   | 21Ch          | 0-3                     | R/W        |       |

**APPLICATION NOTE:** Bit31 in the four GPIO input registers (GPIO[140:176] Input Register, GPIO[100:136] Input Register, GPIO[040:076] Input Register, GPIO[000:036] Input Register) is a single bit register that can be set or cleared by software. It is provided to enable the use of the NORM instruction in the ARC instruction set in order to quickly find the first set or cleared bit in the register. Setting Bit31 to '0b' makes the NORM instruction find the first set bit; setting Bit31 to '1b' makes the NORM instruction find the first cleared bit. For example, if Bit31 of GPIO[000:036] Input Register is '0b' and Bit17 is the highest numbered bit position for which a GPIO signal is set high, then the instruction sequence:

```
LD      R0, [GPIO[000:036] Input Register]
NORM    R0, R0
```

will return the value 17 in ARC register R0.

## 17.8.1 Pin Control Register

**Table 17.7 Pin Control Register [000:176]**

| HOST ADDRESS | N/A                                                                                 |     |             |     |                                                                                     |          |                | HOST SIZE           |
|--------------|-------------------------------------------------------------------------------------|-----|-------------|-----|-------------------------------------------------------------------------------------|----------|----------------|---------------------|
| EC OFFSET    | See <a href="#">Table 17.1 on page 369</a> - <a href="#">Table 17.4 on page 372</a> |     |             |     | 32-bit                                                                              |          |                | EC SIZE             |
| POWER        | VTR                                                                                 |     |             |     | See <a href="#">Table 17.1 on page 369</a> - <a href="#">Table 17.4 on page 372</a> |          |                | nSYS_RST<br>DEFAULT |
| BUS          | <a href="#">EC SPB</a>                                                              |     |             |     |                                                                                     |          |                |                     |
| BYTE[3:2 BIT | D31                                                                                 | D30 | D29         | ... |                                                                                     | D18      | D17            | D16                 |
| HOST TYPE    | R                                                                                   | R   | R           | R   | R                                                                                   | R        | R              | R                   |
| EC TYPE      | R                                                                                   | R   | R           | R   | R                                                                                   | R        | R              | R                   |
| BIT NAME     | Reserved                                                                            |     |             |     |                                                                                     |          |                |                     |
| BYTE1 BIT    | D15                                                                                 | D14 | D13         | D12 | D11                                                                                 | D10      | D9             | D8                  |
| HOST TYPE    | -                                                                                   |     | -           |     | -                                                                                   | -        | -              | -                   |
| EC TYPE      | R                                                                                   |     | R/W         |     | R                                                                                   | R/W      | R/W            | R/W                 |
| BIT NAME     | Reserved                                                                            |     | Mux Control |     | Polarity                                                                            | Reserved | GPIO Direction | Output Buffer Type  |
| BYTE0 BIT    | D7                                                                                  | D6  | D5          | D4  | D3                                                                                  | D2       | D1             | D0                  |
| HOST TYPE    | -                                                                                   |     |             |     | -                                                                                   | -        | -              |                     |
| EC TYPE      | R/W                                                                                 |     |             |     | R                                                                                   |          | R/W            |                     |
| BIT NAME     | Interrupt Detection                                                                 |     |             |     | Reserved                                                                            |          | PU/PD          |                     |

PU/PD

**Table 17.8 PU/PD Enable Bit Definition**

| BIT 1 | BIT 0 | SELECTED FUNCTION |
|-------|-------|-------------------|
| 0     | 0     | None              |
| 0     | 1     | Pull Up Enabled   |
| 1     | 0     | Pull Down Enabled |
| 1     | 1     | None              |



## Product Customer Specification-ODM

## INTERRUPT DETECTION

The [Interrupt Detection](#) field in a [Pin Control Register \[000:176\]](#) controls the asynchronous wakeup and synchronous interrupt detection. The [Interrupt Detection](#) field selection is inverted by the [Polarity](#) bit. When the most significant bit of the [Interrupt Detection](#) field is cleared to '0', the interrupt detection logic is in a low power state. When the most significant bit of the [Interrupt Detection](#) field is set to '1', the interrupt detection logic is active and the remaining bits in [Interrupt Detection](#) field select the interrupt sense.

Table 17.9 [Interrupt Detection Bit Definition](#)

| D7                             | D6 | D5 | D4 | SELECTED FUNCTION                          |
|--------------------------------|----|----|----|--------------------------------------------|
| 0                              | 1  | X  | X  | Edge Detection power save mode (no clocks) |
| X<br><a href="#">Note 17.4</a> | 0  | 0  | 0  | Low Level Sensitive                        |
|                                | 0  | 0  | 1  | High Level Sensitive                       |
| X                              | 0  | 1  | 0  | Reserved                                   |
|                                | 0  | 1  | 1  | Reserved                                   |
|                                | 1  | 0  | 0  | Reserved                                   |
| 1                              | 1  | 0  | 1  | Rising Edge Triggered                      |
|                                | 1  | 1  | 0  | Falling Edge Triggered                     |
|                                | 1  | 1  | 1  | Either edge triggered                      |

**Note 17.4** The most significant bit of the [Interrupt Detection](#) field controls edge detection power save mode. When this bit is set to '0', edge triggered interrupts are blocked; however, level sensitive interrupts are forwarded to the interrupt block.

## OUTPUT BUFFER TYPE

Table 17.10 [Output Buffer Type Bit Definition](#)

| BIT 8 | SELECTED FUNCTION |
|-------|-------------------|
| 0     | Push-Pull         |
| 1     | Open Drain        |

**Note 17.5** Unless explicitly stated otherwise, pins with (IO/IOD) or (O/OD) in their buffer type column in the tables in [Section 3.5, "Pin Signal Function Multiplexing," on page 47](#) are compliant with the following Programmable OD/PP Muxing Design Rule: Each compliant pin has a programmable open drain/push-pull buffer controlled by the [Output Buffer Type](#) bit in the associated [Pin Control Register \[000:176\]](#). The state of this bit controls the mode of the interface buffer for all alternate functions as well as GPIO functions.

## GPIO DIRECTION

The [GPIO](#) bit in a [Pin Control Register \[000:176\]](#) effects the buffer direction only when the [Mux Control](#) field is '00' selecting the pin signal function to be GPIO. When the [Mux Control](#) field is selecting an alternate function (not '00'), then the [GPIO](#) bit in a [Pin Control Register \[000:176\]](#) has no effect and the selected alternate function logic directly controls the pin direction.

**Table 17.11 GPIO Type Bit Definition**

| BIT 9 | SELECTED FUNCTION |
|-------|-------------------|
| 0     | Input             |
| 1     | Output            |

#### POLARITY

When the [Polarity](#) bit in a [Pin Control Register \[000:176\]](#) is set to '1', the alternate function outputs are inverted and [Interrupt Detection](#) (sense defined in [Table 17.9 on page 377](#)) are inverted. When the [Mux Control](#) field is selecting the GPIO signal function (value = '00'), then the [Polarity](#) bit in a [Pin Control Register \[000:176\]](#) does not effect the output. Regardless of the state of the [Mux Control](#) field and the [Polarity](#) bit, the state of the pin is always reported without inversion in the GPIO input register. See [Figure 17.1 GPIO Interface Block Diagram on page 367](#).

**Table 17.12 Polarity Bit Definition**

| BIT 11 | SELECTED FUNCTION |
|--------|-------------------|
| 0      | Non-inverted      |
| 1      | Inverted          |

#### MUX CONTROL

The [Mux Control](#) select the signal function which is routed to the pin. See [Section 17.4, "Detailed Pin Muxing assignments.," on page 367](#) individual pin assignments.

**Table 17.13 Mux Control Bit Definition**

| D13 | D12 | SELECTED FUNCTION    |
|-----|-----|----------------------|
| 0   | 0   | GPIO                 |
| 0   | 1   | Alternate Function 1 |
| 1   | 0   | Alternate Function 2 |
| 1   | 1   | Alternate Function 3 |

## 17.8.2 Output GPIO[000:036]

**Table 17.14 GPIO[000:036] Output Register**

| HOST ADDRESS | N/A                                         |     |     |            |   | HOST SIZE           |    |    |
|--------------|---------------------------------------------|-----|-----|------------|---|---------------------|----|----|
| EC OFFSET    | 200h                                        |     |     | 32         |   | EC SIZE             |    |    |
| POWER        | VTR                                         |     |     | 0000_0000h |   | nSYS_RST<br>DEFAULT |    |    |
| BUS          | EC SPB                                      |     |     |            |   |                     |    |    |
| BIT          | D31                                         | D30 | D29 | ...        |   | D2                  | D1 | D0 |
| HOST TYPE    | -                                           | -   | -   | -          | - | -                   | -  | -  |
| EC TYPE      | See <a href="#">Table 17.17 on page 380</a> |     |     |            |   |                     |    |    |
| BIT NAME     | GPIO[000:036] Output                        |     |     |            |   |                     |    |    |

**Table 17.15 Bit definitions GPIO[000:036] Output Register**

| BIT     | EC TYPE | SIGNAL NAME   | WAKE | DESCRIPTION                                      |
|---------|---------|---------------|------|--------------------------------------------------|
| [7:0]   | R/WC    | GPIO[007:000] | Y    | Each bit monitors the corresponding pins status. |
| [15:8]  | R/WC    | GPIO[017:010] | Y    |                                                  |
| [23:16] | R/WC    | GPIO[027:020] | Y    |                                                  |
| [26:24] | R/WC    | GPIO[032:030] | Y    |                                                  |
| [30:27] | R       | GPIO[036:033] | N    | Reserved                                         |
| 31      | R       | Reserved      | N    | This bit is always reserved                      |

### 17.8.3 Output GPIO[040:076]

**Table 17.16 GPIO[040:076] Output Register**

| HOST ADDRESS | N/A                                         |     |     |           |   |    | HOST SIZE           |    |
|--------------|---------------------------------------------|-----|-----|-----------|---|----|---------------------|----|
| EC OFFSET    | 204h                                        |     |     | 32        |   |    | EC SIZE             |    |
| POWER        | VTR                                         |     |     | 0000_000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB                                      |     |     |           |   |    |                     |    |
| BIT          | D31                                         | D30 | D29 | ...       |   | D2 | D1                  | D0 |
| HOST TYPE    | -                                           | -   | -   | -         | - | -  | -                   | -  |
| EC TYPE      | See <a href="#">Table 17.17 on page 380</a> |     |     |           |   |    |                     |    |
| BIT NAME     | GPIO[040:076] Output                        |     |     |           |   |    |                     |    |

**Table 17.17 Bit definitions GPIO[040:076] Output Register**

| BIT     | EC TYPE | SIGNAL NAME   | WAKE | DESCRIPTION                                      |
|---------|---------|---------------|------|--------------------------------------------------|
| [7:0]   | R/WC    | GPIO[047:040] | Y    | Each bit monitors the corresponding pins status. |
| [15:8]  | R/WC    | GPIO[057:050] | Y    |                                                  |
| [23:16] | R/WC    | GPIO[067:060] | Y    |                                                  |
| [30:24] | R       | GPIO[076:070] | N    | Reserved                                         |
| 31      | R       | Reserved      | N    | This bit is always reserved                      |

## 17.8.4 Output GPIO[100:136]

**Table 17.18 GPIO[100:136] Output Register**

| HOST ADDRESS | N/A                                         |     |     |            |   |    | HOST SIZE           |    |
|--------------|---------------------------------------------|-----|-----|------------|---|----|---------------------|----|
| EC OFFSET    | 208h                                        |     |     | 32         |   |    | EC SIZE             |    |
| POWER        | VTR                                         |     |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB                                      |     |     |            |   |    |                     |    |
| BIT          | D31                                         | D30 | D29 | ...        |   | D2 | D1                  | D0 |
| HOST TYPE    | -                                           | -   | -   | -          | - | -  | -                   | -  |
| EC TYPE      | See <a href="#">Table 17.19 on page 381</a> |     |     |            |   |    |                     |    |
| BIT NAME     | GPIO[100:136] Output                        |     |     |            |   |    |                     |    |

**Table 17.19 Bit definitions GPIO[100:136] Output Register**

| BIT     | EC TYPE | SIGNAL NAME   | DESCRIPTION                                      |
|---------|---------|---------------|--------------------------------------------------|
| [7:0]   | R/W     | GPIO[107:100] | Each bit monitors the corresponding pins status. |
| [15:8]  | R/W     | GPIO[117:110] |                                                  |
| [23:16] | R/W     | GPIO[127:120] |                                                  |
| [26:24] | R/W     | GPIO[132:130] |                                                  |
| [30:27] | R       | GPIO[136:133] | Reserved                                         |
| 31      | R       | Reserved      | This bit is always reserved                      |



## 17.8.5 Output GPIO[140:176]

**Table 17.20 GPIO[140:176] Output Register**

| HOST ADDRESS | N/A                                         |     |     |            |   |    | HOST SIZE           |    |
|--------------|---------------------------------------------|-----|-----|------------|---|----|---------------------|----|
| EC OFFSET    | 20Ch                                        |     |     | 32         |   |    | EC SIZE             |    |
| POWER        | VTR                                         |     |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB                                      |     |     |            |   |    |                     |    |
| BIT          | D31                                         | D30 | D29 | ...        |   | D2 | D1                  | D0 |
| HOST TYPE    | -                                           | -   | -   | -          | - | -  | -                   | -  |
| EC TYPE      | See <a href="#">Table 17.21 on page 382</a> |     |     |            |   |    |                     |    |
| BIT NAME     | GPIO[140:176] Output                        |     |     |            |   |    |                     |    |

**Table 17.21 Bit definitions GPIO[140:176] Output Register**

| BIT     | EC TYPE | SIGNAL NAME   | DESCRIPTION                                      |
|---------|---------|---------------|--------------------------------------------------|
| [7:0]   | R/W     | GPIO[147:140] | Each bit monitors the corresponding pins status. |
| [15:8]  | R/W     | GPIO[157:150] |                                                  |
| [21:16] | R/W     | GPIO[165:160] |                                                  |
| [23:22] | R       | GPIO[167:166] | Reserved                                         |
| [30:24] | R       | GPIO[176:170] | Reserved                                         |
| 31      | R       | Reserved      | This bit is always reserved                      |

## 17.8.6 Input GPIO[000:036]

The GPIO Input data registers are always active, that is they can always be used to read the state of a pin, even when the pin is in output mode and/or when an alternate function is selected.



Table 17.22 GPIO[000:036] Input Register

| HOST ADDRESS | N/A    |                     |     |            |   |    | HOST SIZE           |    |
|--------------|--------|---------------------|-----|------------|---|----|---------------------|----|
| EC OFFSET    | 210h   |                     |     | 32         |   |    | EC SIZE             |    |
| POWER        | VTR    |                     |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB |                     |     |            |   |    |                     |    |
| BIT          | D31    | D30                 | D29 | ...        |   | D2 | D1                  | D0 |
| HOST TYPE    | -      | -                   | -   | -          | - | -  | -                   | -  |
| EC TYPE      | R/W    | R                   | R   | R          | R | R  | R                   | R  |
| BIT NAME     | NORM   | GPIO[000:036] INPUT |     |            |   |    |                     |    |

### 17.8.7 Input GPIO[040:076]

The GPIO Input data registers are always active, that is they can always be used to read the state of a pin, even when the pin is in output mode and/or when an alternate function is selected.

Table 17.23 GPIO[040:076] Input Register

| HOST ADDRESS | N/A    |                     |     |            |   |    | HOST SIZE           |    |
|--------------|--------|---------------------|-----|------------|---|----|---------------------|----|
| EC OFFSET    | 214h   |                     |     | 32         |   |    | EC SIZE             |    |
| POWER        | VTR    |                     |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB |                     |     |            |   |    |                     |    |
| BIT          | D31    | D30                 | D29 | ...        |   | D2 | D1                  | D0 |
| HOST TYPE    | -      | -                   | -   | -          | - | -  | -                   | -  |
| EC TYPE      | R/W    | R                   | R   | R          | R | R  | R                   | R  |
| BIT NAME     | NORM   | GPIO[040:076] INPUT |     |            |   |    |                     |    |

### 17.8.8 Input GPIO[100:136]

The GPIO Input data registers are always active, that is they can always be used to read the state of a pin, even when the pin is in output mode and/or when an alternate function is selected.

**Table 17.24 GPIO[100:136] Input Register**

| HOST ADDRESS | N/A    |                     |     |            |   |    | HOST SIZE           |    |
|--------------|--------|---------------------|-----|------------|---|----|---------------------|----|
| EC OFFSET    | 218h   |                     |     | 32         |   |    | EC SIZE             |    |
| POWER        | VTR    |                     |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB |                     |     |            |   |    |                     |    |
| BIT          | D31    | D30                 | D29 | ...        |   | D2 | D1                  | D0 |
| HOST TYPE    | -      | -                   | -   | -          | - | -  | -                   | -  |
| EC TYPE      | R/W    | R                   | R   | R          | R | R  | R                   | R  |
| BIT NAME     | NORM   | GPIO[100:136] INPUT |     |            |   |    |                     |    |

### 17.8.9 Input GPIO[140:176]

The GPIO Input data registers are always active, that is they can always be used to read the state of a pin, even when the pin is in output mode and/or when an alternate function is selected.

**Table 17.25 GPIO[140:176] Input Register**

| HOST ADDRESS | N/A    |                     |     |            |   |    | HOST SIZE           |    |
|--------------|--------|---------------------|-----|------------|---|----|---------------------|----|
| EC OFFSET    | 21Ch   |                     |     | 32         |   |    | EC SIZE             |    |
| POWER        | VTR    |                     |     | 0000_0000h |   |    | nSYS_RST<br>DEFAULT |    |
| BUS'         | EC SPB |                     |     |            |   |    |                     |    |
| BIT          | D31    | D30                 | D29 | ...        |   | D2 | D1                  | D0 |
| HOST TYPE    | -      | -                   | -   | -          | - | -  | -                   | -  |
| EC TYPE      | R/W    | R                   | R   | R          | R | R  | R                   | R  |
| BIT NAME     | NORM   | GPIO[140:176] INPUT |     |            |   |    |                     |    |



## 17.9 GPIO Interface Revision History

This revision history shows the changes made to this chapter.

**Table 17.26 GPIO Interface Chapter Revision History**

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History," on page 539.</a> |              |            |                                                                                                                                                                                                                                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE       | SECTION/FIGURE/ENTRY                                                                                                                                                                                                                 | CORRECTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 1.                                                                                                                                                                                                                                          | 0.4          | 04/30/2007 | <a href="#">Section 17.4, "Detailed Pin Muxing assignments," on page 367.</a><br><br><a href="#">Table 17.8 on page 376 - Table 17.8 on page 376</a>                                                                                 | Corrected excel formula glitch; replace "0" with "reserved" pins 34, 58, 59.<br>Change default Pin control registers GPIO041, GPIO067 offsets 0084, 00DC from value 00000100h to 00001000h. Change default Pin control registers GPIO0145, GPIO0146, GPIO0147, GPIO0150, offsets 0194, 0198, 019C, 01A0 from value 00001000h to 00000000h.<br><br>Corrected conflict bit locations. <a href="#">Table 17.7 on page 376</a> register table accurate; Field tables updated. |
| 2.                                                                                                                                                                                                                                          | 0.4          | 04/30/2007 | <a href="#">Note 17.2 on page 373</a>                                                                                                                                                                                                | Min pulse width for GPIO wakeup is 5ns. Bug 337.                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 3.                                                                                                                                                                                                                                          | 0.4          | 04/30/2007 | <a href="#">Table 17.2 on page 370</a><br><br><a href="#">Section 17.7, "GPIO Pass-Through Ports," on page 373</a><br><a href="#">Figure 17.2 on page 374</a>                                                                        | GPIO057 Pin control reg. default change from 00010000h to 00001000h.<br><br>Corrected mux control values in figure.<br>Editorial change: breakdown step to setup GPTP's.                                                                                                                                                                                                                                                                                                  |
| 4.                                                                                                                                                                                                                                          | 0.4          | 5/08/2007  | <a href="#">Section 17.8, "Registers," on page 374</a><br>APPLICATION NOTE: <a href="#">on page 375</a><br><a href="#">Section 17.1, "General Description," on page 366</a><br><a href="#">Section 17.5.2, "Clocks," on page 373</a> | Editorial-Reordered Registers to lowest to highest address.<br>Editorial-Changed to app note.<br><br>Added no clocks wake description<br><br>Added content and xrefs.                                                                                                                                                                                                                                                                                                     |
| 5.                                                                                                                                                                                                                                          | 0.6          | 07/09/2007 | <a href="#">Table 17.2, "Pin Control Muxing Package Pin[33:64]," on page 370</a>                                                                                                                                                     | Added note 12 to indicate the PCI buffers do not have internal pullup/pulldown resistors. Effects pins 55-59 & 64.                                                                                                                                                                                                                                                                                                                                                        |
| 6.                                                                                                                                                                                                                                          | 0.61         | 08/29/2007 | <a href="#">Table 17.2, "Pin Control Muxing Package Pin[33:64]," on page 370</a>                                                                                                                                                     | Updated pin note 14 to indicate the PCI buffers have no internal Hysteresis and can retrigger interrupts. Effects pins 55-59 & 64.                                                                                                                                                                                                                                                                                                                                        |
| 7.                                                                                                                                                                                                                                          | 0.61         | 8/31/2007  | <a href="#">Section 17.4, "Detailed Pin Muxing assignments," on page 367</a>                                                                                                                                                         | Added visability of SMBus ports 2B, 2C & 2D Functional Signals<br>I2C2B_CLK, I2C2B_DATA, I2C2C_CLK, I2C2C_DATA, I2C2D_CLK, I2C2D_DATA on pins 98, 97, 106, 105, 13, 12.                                                                                                                                                                                                                                                                                                   |

## Chapter 18 Serial Debug Port

### 18.1 General Description

The Serial Debug Port serially transmits MCU-originated diagnostic vectors to an external debug trace system.

The Serial Debug Port consists of the [Debug Data Register](#), [Debug Control Register](#), a Parallel-to-Serial Converter, a Clock/Control Interface and a two-pin external interface (Debug\_CLK, Debug\_DAT). See [Figure 18.1](#).

### 18.2 Power, Clocks and Reset

#### 18.2.1 Power Domain

This block is powered by the VTR Power Supply.

See [Section 4.5, "Power Configuration," on page 96](#) for details on power domains.

#### 18.2.2 Clocks

This block has one clock input, the [EC Bus Clock](#).

See [Section 4.4, "Clock Generator," on page 77](#) for details on clocks.

#### 18.2.3 Reset

This block is reset on a [nSYS\\_RST](#).

See [Section 4.6, "Reset Interface," on page 99](#) for details on reset.

### 18.3 Block Diagram

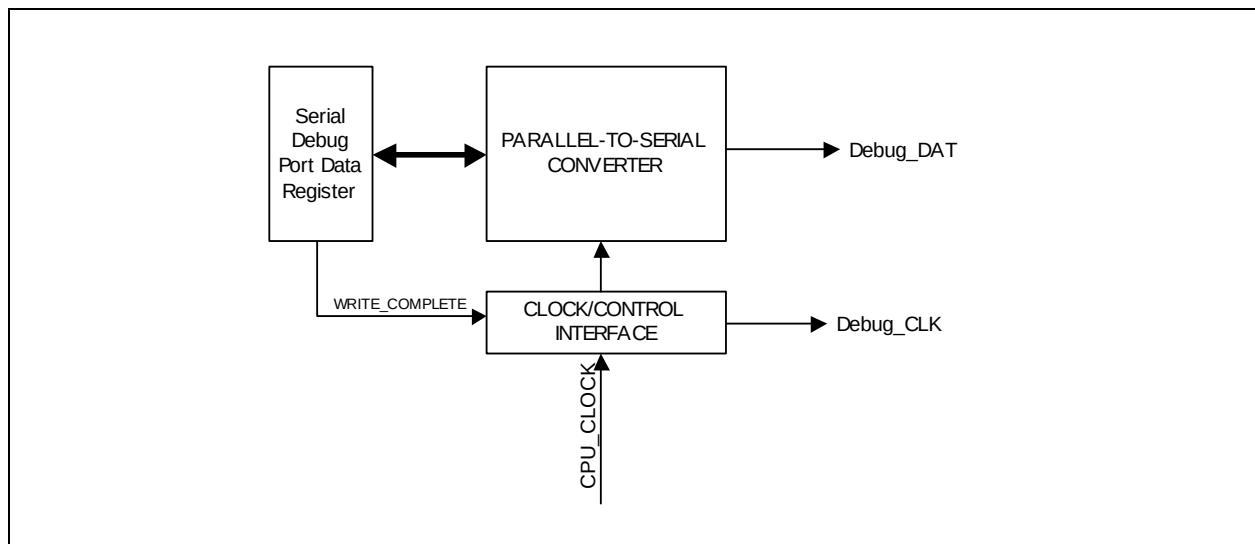


Figure 18.1 Serial Debug Port Block Diagram

## 18.4 Block Diagram Port List

**Table 18.1** Serial Debug Port Port List

| SIGNAL NAME                  | DIRECTION | DESCRIPTION                                    |
|------------------------------|-----------|------------------------------------------------|
| Debug Clock                  | OUTPUT    | Derived from the <a href="#">EC Bus Clock</a>  |
| Debug Data                   | OUTPUT    | Serialized Data shifter out by the Debug Clock |
| <a href="#">EC Bus Clock</a> | INPUT     | EC AHB Bus Clock                               |

## 18.5 Interrupts

There are no interrupts from this block

## 18.6 Functional Description

Writes to the [Debug Data Register](#) initiate an transfer cycle ([Figure 18.2](#)). Data from the [Debug Data Register](#) is shifted LSB first and is transmitted one byte per transfer cycle.

Data is transferred in one direction only from the [Debug Data Register](#) to the external interface. The data is shifted out on the clock edge selected by the [EDGE\\_SEL](#) bit in the [Debug Control Register on page 389](#). Valid data is guaranteed on opposite edge of Debug\_CLK after being shifted out. For example when the [EDGE\\_SEL](#) bit is '0' (default), Valid data is guaranteed on the falling edge of Debug\_CLK. The Setup Time to the falling edge of Debug\_CLK is 10ns minimum; the Hold Time is 1ns minimum.

The Debug\_CLK and Debug\_DAT outputs are '1' when the serial Debug Port is inactive. The transfer clock is [EC Bus Clock](#).

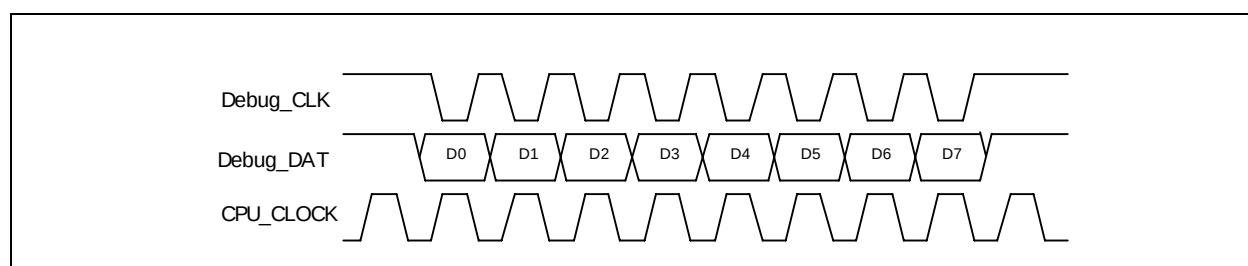


**Figure 18.2** Data Transfer

## 18.7 Instance Description

There is one block instance defined in this chapter: [Serial Debug Port](#).

## 18.8 Registers

Each instance of the [Serial Debug Port](#) has its own Logical Device Number, and Base Address as indicated in [Table 18.2](#).

**Table 18.2 Serial Debug Port Base Address Table**

| Serial Debug Port INSTANCE | LDN FROM (Table 7.2 on page 167) | AHB BASE ADDRESS |
|----------------------------|----------------------------------|------------------|
| MCU Debug Port             | 23h                              | F0_8C00h         |

The following table summarizes the registers allocated for the [Serial Debug Port](#). The offset field in the following table is the offset from the [Serial Debug Port](#)'s EC Base Address.

**Table 18.3 Serial Debug Port Register Summary**

| REGISTER NAME                          | EC INTERFACE |           |         | NOTES |
|----------------------------------------|--------------|-----------|---------|-------|
|                                        | SPB OFFSET   | BYTE LANE | EC TYPE |       |
| <a href="#">Debug Data Register</a>    | 00h          | 0         | R/W     |       |
| <a href="#">Debug Control Register</a> | 04h          | 0         | R/W     |       |

### 18.8.1 Detailed Register Descriptions

The [Debug Data Register](#) is R/W. It always returns the last data written by the MCU or the power-on default '00h'.

**Table 18.4 Debug Data Register**

| HOST ADDRESS | NA                     |     |     |     |       |     |     | HOST SIZE                           |  |
|--------------|------------------------|-----|-----|-----|-------|-----|-----|-------------------------------------|--|
| EC OFFSET    | 00h                    |     |     |     | 8-bit |     |     | EC SIZE                             |  |
| POWER        | VTR                    |     |     |     | 00h   |     |     | <a href="#">nSYS_RST</a><br>DEFAULT |  |
| BUS          | <a href="#">EC SPB</a> |     |     |     |       |     |     |                                     |  |
| BYTE0 BIT    | D7                     | D6  | D5  | D4  | D3    | D2  | D1  | D0                                  |  |
| HOST TYPE    | -                      | -   | -   | --  | -     | -   | -   | -                                   |  |
| EC TYPE      | R/W                    | R/W | R/W | R/W | R/W   | R/W | R/W | R/W                                 |  |
| BIT NAME     | Data[7:0]              |     |     |     |       |     |     |                                     |  |

#### DATA[7:0]

Debug data to be shifted out on the MCU Debug Port. While data is being shifted out, the SPB interface will 'hold-off' additional writes to the data register until the transfer is complete.



Table 18.5 Debug Control Register

| HOST ADDRESS | NA       |    |    |       |    |    | HOST SIZE           |          |
|--------------|----------|----|----|-------|----|----|---------------------|----------|
| EC OFFSET    | 04h      |    |    | 8-bit |    |    | EC SIZE             |          |
| POWER        | VTR      |    |    | 00h   |    |    | nSYS_RST<br>DEFAULT |          |
| BUS          | EC SPB   |    |    |       |    |    |                     |          |
| BYTE0 BIT    | D7       | D6 | D5 | D4    | D3 | D2 | D1                  | D0       |
| HOST TYPE    | -        | -  | -  | --    | -  | -  | -                   | -        |
| EC TYPE      | R        |    |    |       |    |    | R/W                 | R/W      |
| BIT NAME     | Reserved |    |    |       |    |    | EN                  | EDGE_SEL |

**EDGE\_SEL**

0= Data is shifted out on the rising edge of the debug clock (Default)

1= Data is shifted out on the falling edge of the debug clock

**EN**

0= Clock is disabled (Default)

1= Clock enabled

## 18.9 Serial Debug Port Revision History

This revision history shows the changes made to this chapter.

Table 18.6 Serial Debug Port Chapter Revision History

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History," on page 539.</a> |              |            |                                                                  |                                                 |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------------|------------------------------------------------------------------|-------------------------------------------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE       | SECTION/FIGURE/ENTRY                                             | CORRECTION                                      |
| 1.                                                                                                                                                                                                                                          | 0.4          | 04/25/2007 | <a href="#">Section 18.1, "General Description," on page 386</a> | Valid data valid on programmable edge of clock. |
| 2.                                                                                                                                                                                                                                          |              |            |                                                                  |                                                 |
| 3.                                                                                                                                                                                                                                          |              |            |                                                                  |                                                 |
| 4.                                                                                                                                                                                                                                          |              |            |                                                                  |                                                 |



## Chapter 19 Watchdog Timer Interface

### 19.1 General Description

The function of the Watchdog Timer is to provide a mechanism to detect if the embedded controller has failed.

When enabled, the WATCHDOG Timer (WDT) circuit will generate a [WDT Event](#) if the user program fails to reload the WDT within a specified length of time known as the [WDT Interval](#).

This timer can be held inactive via the WDT Stall feature if the Hibernation timer, Week Timer, or the JTAG interface are enabled and active. This featured if enabled can be used to avoid unintended system resets.

### 19.2 Block Diagram

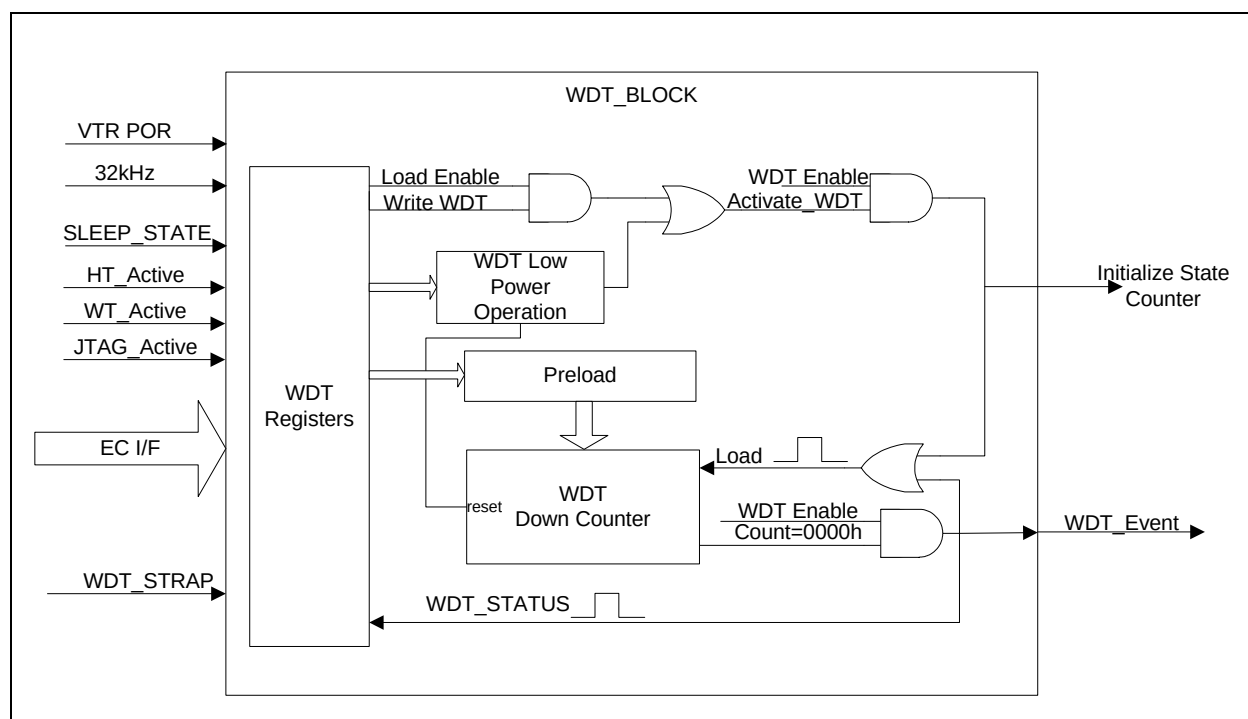


Figure 19.1 Watchdog Timer Interface Block Diagram

### 19.3 Watchdog Timer Interface Signal List

Table 19.1 Watchdog Timer Interface Signal List

| SIGNAL NAME              | DIRECTION | DESCRIPTION                                           |
|--------------------------|-----------|-------------------------------------------------------|
| <a href="#">nSYS_RST</a> | INPUT     | Power on Reset to the block                           |
| 32kHz                    | INPUT     | <a href="#">X32K_CLK</a> , Clock source for WDT logic |

**Table 19.1 Watchdog Timer Interface Signal List (continued)**

| SIGNAL NAME   | DIRECTION | DESCRIPTION                                                                                                                        |
|---------------|-----------|------------------------------------------------------------------------------------------------------------------------------------|
| HT_Active     | INPUT     | Signal indicating the Hibernation Timer is active and counting. See <a href="#">Chapter 20, "Hibernation Timer," on page 399</a> . |
| WT_Active     | INPUT     | Signal indicating the Week Timer is active and counting. See <a href="#">Chapter 21, "Week Alarm Interface," on page 404</a> .     |
| JTAG_Active   | INPUT     | Signal indicating the JTAG interface is active. See <a href="#">Chapter 13, "JTAG and XNOR," on page 248</a> .                     |
| SPB Interface | I/O Bus   | Bus used by microprocessor to access the registers in this block.                                                                  |
| WDT Event     | OUTPUT    | Pulse generated when WDT expires                                                                                                   |

**Note 19.1** In the MEC5035, the assertion of the [WDT Event](#) output from this block causes a [Watch-Dog Timer Forced Reset](#). See [Section 4.6.10, "Watch-Dog Timer Forced Reset," on page 103](#).

## 19.4 Power, Clocks and Reset

### 19.4.1 Power Domain

This block is powered by the VTR Power Supply.

See [Section 4.5, "Power Configuration," on page 96](#) for details on power domains.

### 19.4.2 Clocks

This block has two clock inputs, the [EC Bus Clock](#) and [X32K\\_CLK](#). The [EC Bus Clock](#) is used in the interface to the embedded controller accessible registers. The 32.768KHz [X32K\\_CLK](#) is the clock source for the Watchdog Timer functional logic, including the counter.

See [Section 4.4, "Clock Generator," on page 77](#) for details on clocks.

### 19.4.3 Reset

This block is reset on a [nSYS\\_RST](#).

See [Section 4.6, "Reset Interface," on page 99](#) for details on reset.

## 19.5 WDT Event output routing

The WDT Event (output) causes the [Watch-Dog Timer Forced Reset on page 103](#).

The WDT Event state is also retained through a [Watch-Dog Timer Forced Reset](#) in the [WDT](#) bit of the [Power-Fail and Reset Status Register on page 116](#). The [Power-Fail and Reset Status Register](#) can generate a interrupt via the [PFR interrupt IRQ31 Source Register on page 361](#).

The WDT Event output is not directly connected to an EC interrupt.

## 19.6 WDT Operation

### 19.6.1 WDT Activation Mechanism

The WDT is activated by the following sequence of operations during normal operation:

1. Load the [WDT Load Register](#) with the count value.
2. Set the [WDT Enable](#) bit in the [WDT Control Register](#).

The [WDT Activation Mechanism](#) starts the WDT decrementing counter.

### 19.6.2 WDT Deactivation Mechanism

The WDT is deactivated by the clearing the [WDT Enable](#) bit in the [WDT Control Register](#). The [WDT Deactivation Mechanism](#) places the WDT in a low power state in which clock are gated and the counter stops decrementing.

### 19.6.3 WDT Reload Mechanism

The WDT must be reloaded within periods that are shorter than the programmed watchdog interval; otherwise the WDT will underflow and a [WDT Event](#) will be generated and the WDT\_STAT bit will be set in the [WDT Control Register](#). It is the responsibility of the user program to continually execute sections of code which reload the watchdog timer (WDT) causing the counter to be reloaded

There are two methods of reloading the WDT: a write to the [WDT Kick Register](#) or the [WDT Activation Mechanism](#).

### 19.6.4 WDT Interval

The [WDT Interval](#) is the time it takes for the WDT to decrements from the [WDT Load Register](#) value to 0000h. The [WDT Count Register](#) value takes 1.007ms to decrement by 1 count.

### 19.6.5 WDT STALL Operation

The WDT has several events that can cause the WDT STALL. When a WDT STALL event is asserted, the WDT stops decrementing, and the WDT enters a low power state. When a WDT STALL event is de-asserted, the counter is reloaded with the programmed preload value and starts decrementing.

The WDT STALL feature has been implemented for convenience. If the system designer chooses not to utilize the WDT STALL feature, the WDT defaults with the WDT STALL feature disabled.

There are three Stall inputs to the WDT are [HT\\_Active](#), [WT\\_Active](#), [JTAG\\_Active](#) (corresponding to the Hibernation Timer, the Week Alarm Timer, & the J-TAG interface being active. The Stall inputs have individual enable bits: [HT\\_STALL\\_EN](#), [WT\\_STALL\\_EN](#), [JTAG\\_STALL\\_EN](#) bits in the [WDT Control Register](#) on page 395.

**Note 19.2** Only a single instance of the Hibernation Timer ([Hibernation Timer.0](#) on page 400) is routed to the [HT\\_Active](#) stall input of the [Watchdog Timer Interface](#).

**Table 19.2 WDT STALL event Behavior**

| WDT STALL Input<br>(activity indicator) | WDT Control Register<br>on page 395 |                | WDT BEHAVIOR                                                                        | WDT Event OUTPUT |
|-----------------------------------------|-------------------------------------|----------------|-------------------------------------------------------------------------------------|------------------|
|                                         | STALL_EN BIT                        | WDT Enable BIT |                                                                                     |                  |
| X                                       | X                                   | 0              | Counter is reset and not active.<br>Clock source to counter is gated to save power. | 0                |
| X                                       | 0                                   | 1              | Count is active. (see <a href="#">Note 19.1</a> )<br>If counter > 0000h             | 1                |
| 0                                       | 1                                   | 1              |                                                                                     |                  |
| X                                       | X                                   | 1              | Count is decremented to 0000h                                                       | 1                |
| 1                                       | 1                                   | 1              | Counter is not active.<br>Clock source to counter is gated to save power.           | 0                |

**Note 19.1** When the WDT recovers from a STALL event, the counter is reloaded with the programmed preload value.

**Note 19.2** When the counter reaches 0000h it wraps to the preload value and starts counting down again. This creates a pulse on the [WDT Event](#) output.

## 19.7 Instance Description

There is one instance of the [Watchdog Timer Interface](#) block implemented in the MEC5035.

Each instance of the [Watchdog Timer Interface](#) has its own Logical Device Number, and Base Address as indicated in [Table 19.3](#).

**Table 19.3 Watchdog Timer Interface Base Address Table**

| Watchdog Timer INSTANCE | LDN FROM<br>( <a href="#">Table 7.3</a> on page 168) | AHB BASE ADDRESS |
|-------------------------|------------------------------------------------------|------------------|
| Watchdog Timer          | 1h                                                   | F0_0400h         |

The [Table 19.4](#) is a register summary for one instance of the [Watchdog Timer Interface](#). Each EC address is indicated as an SPB Offset from its AHB address.

**Table 19.4 Watchdog Timer Interface Register Summary**

| REGISTER NAME        | EC INTERFACE |           |         | NOTES |
|----------------------|--------------|-----------|---------|-------|
|                      | SPB OFFSET   | BYTE LANE | EC TYPE |       |
| WDT Load Register    | 00h          | 0         | R/W     |       |
|                      |              | 1         |         |       |
| WDT Control Register | 04h          | 0         |         |       |
| WDT Kick Register    | 08h          | 0         | R/W     |       |
| WDT Count Register   | 0Ch          | 0         | R       |       |
|                      |              | 1         |         |       |

**Note:** All Registers listed in Table 19.4 are powered by VTR and reset by nSYS\_RST.

**Note 19.3** All register are clocked by the

## 19.8 Detailed Register Descriptions

### 19.8.1 WDT Load Register

**Table 19.5 WDT Load Register**

| HOST ADDRESS | n/a            |     |     | n/a    |     |     | HOST SIZE           |     |
|--------------|----------------|-----|-----|--------|-----|-----|---------------------|-----|
| EC OFFSET    | 00h            |     |     | 16-bit |     |     | EC SIZE             |     |
| POWER        | VTR            |     |     | FFFFh  |     |     | nSYS_RST<br>DEFAULT |     |
| BUS          | EC SPB         |     |     |        |     |     |                     |     |
| BIT          | D15            | D14 | D13 | ■      | ■   | D2  | D1                  | D0  |
| HOST TYPE    | N/A            | N/A | N/A | N/A    | N/A | N/A | N/A                 | N/A |
| EC TYPE      | R/W            | R/W | R/W | R/W    | R/W | R/W | R/W                 | R/W |
| BIT NAME     | WDT load[15:0] |     |     |        |     |     |                     |     |

#### WDT LOAD[15:0]

Writing this field reloads the Watch Dog Timer counter.

## 19.8.2 WDT Control Register

Table 19.6 WDT Control Register

| HOST ADDRESS | n/a      |     |     |                      | n/a                |                    |               | HOST SIZE           |  |
|--------------|----------|-----|-----|----------------------|--------------------|--------------------|---------------|---------------------|--|
| EC OFFSET    | 04h      |     |     |                      | 8-bit              |                    |               | EC SIZE             |  |
| POWER        | VTR      |     |     |                      | 00h                |                    |               | nSYS_RST<br>DEFAULT |  |
| BUS          | EC SPB   |     |     |                      |                    |                    |               |                     |  |
| BYTE0 BIT    | D7       | D6  | D5  | D4                   | D3                 | D2                 | D1            | D0                  |  |
| HOST TYPE    | N/A      | N/A | N/A | N/A                  | N/A                | N/A                | N/A           | N/A                 |  |
| EC TYPE      | R/W      | R/W | R/W | R/W                  | R/W                | R/W                | R/W           | R/W                 |  |
| BIT NAME     | Reserved |     |     | JTAG<br>STALL_<br>EN | WT<br>STALL_<br>EN | HT<br>STALL_<br>EN | WDT<br>Status | WDT<br>Enable       |  |

### WDT ENABLE

**Note:** The default of the WDT is inactive.

In [WDT Operation](#), the WDT is activated by the sequence of operations defined in [Section 19.6.1, "WDT Activation Mechanism"](#) and deactivated by the sequence of operations defined in [Section 19.6.2, "WDT Deactivation Mechanism"](#). In [WDT STALL Operation](#), hardware may be enabled to automatically activate and deactivate the WDT.

### WDT STATUS

WDT\_RST is set by hardware if the last reset of MEC5035 was caused by an underflow of the WDT. See [Section 19.6.3, "WDT Reload Mechanism," on page 392](#) for more information.

This bit must be cleared by the EC firmware writing a '1' to this bit. Writing a '0' to this bit has no effect.

### JTAG STALL\_EN

This bit is used to enable the [JTAG\\_Active](#) (JTAG\_RST# pin not asserted) [WDT STALL Operation on page 392](#).

0= [JTAG\\_Active WDT STALL Operation](#) not enabled

1= [JTAG\\_Active WDT STALL Operation](#) enabled

### WT STALL\_EN

This bit is used to enable the [WT\\_Active](#) (Week Timer) [WDT STALL Operation on page 392](#).

0= [WT\\_Active WDT STALL Operation](#) events not enabled

1= [WT\\_Active WDT STALL Operation](#) events enabled.

### HT STALL\_EN

This bit is used to enable the [HT\\_Active](#) (Hibernation Timer) [WDT STALL Operation on page 392](#).

0= [HT\\_Active WDT STALL Operation](#) events not enabled

1= [HT\\_Active WDT STALL Operation](#) events enabled.

### 19.8.3 WDT Kick Register

**Table 19.7 WDT Kick Register**

| HOST ADDRESS | n/a    |     |     |     | n/a   |     |     | HOST SIZE           |  |
|--------------|--------|-----|-----|-----|-------|-----|-----|---------------------|--|
| EC OFFSET    | 08h    |     |     |     | 8-bit |     |     | EC SIZE             |  |
| POWER        | VTR    |     |     |     | n/a   |     |     | nSYS_RST<br>DEFAULT |  |
| BUS          | EC SPB |     |     |     |       |     |     |                     |  |
| BYTE0 BIT    | D7     | D6  | D5  | D4  | D3    | D2  | D1  | D0                  |  |
| HOST TYPE    | N/A    | N/A | N/A | N/A | N/A   | N/A | N/A | N/A                 |  |
| EC TYPE      | W      | W   | W   | W   | W     | W   | W   | W                   |  |
| BIT NAME     | Kick   |     |     |     |       |     |     |                     |  |

#### KICK

The [WDT Kick Register](#) is a strobe. Reads of the [WDT Kick Register](#) return 0.

Writes to the [WDT Kick Register](#) cause the WDT to reload the [WDT Load Register](#) value and start decrementing when the [WDT Enable](#) bit in the [WDT Control Register](#) is set to '1'. When the [WDT Enable](#) bit in the [WDT Control Register](#) is cleared to '0', writes to the [WDT Kick Register](#) have no effect.

### 19.8.4 WDT Count Register

**Table 19.8 WDT Count Register**

| HOST ADDRESS | n/a             |     |     | n/a    |     |     | HOST SIZE           |     |
|--------------|-----------------|-----|-----|--------|-----|-----|---------------------|-----|
| EC OFFSET    | 00h             |     |     | 16-bit |     |     | EC SIZE             |     |
| POWER        | VTR             |     |     | FFFFh  |     |     | nSYS_RST<br>DEFAULT |     |
| BUS          | EC SPB          |     |     |        |     |     |                     |     |
| BIT          | D15             | D14 | D13 | ■      | ■   | D2  | D1                  | D0  |
| HOST TYPE    | N/A             | N/A | N/A | N/A    | N/A | N/A | N/A                 | N/A |
| EC TYPE      | R/W             | R/W | R/W | R/W    | R/W | R/W | R/W                 | R/W |
| BIT NAME     | WDT COUNT[15:0] |     |     |        |     |     |                     |     |

#### WDT COUNT[15:0]

This read-only register provide the current WDT count.



## 19.9 Watchdog Timer Interface Revision History

This revision history shows the changes made to this chapter.

**Table 19.9 Watchdog Timer Interface Chapter Revision History**

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History," on page 539.</a> |              |            |                      |                                                        |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------------|----------------------|--------------------------------------------------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE       | SECTION/FIGURE/ENTRY | CORRECTION                                             |
| 1.                                                                                                                                                                                                                                          | 0.3          | <3/01/2007 | All                  | Initial Release of Delta Chapter                       |
| 2.                                                                                                                                                                                                                                          | 0.4          | 04/25/2007 | All                  | Replacement of entire chapter to match implementation. |





## Chapter 20 Hibernation Timer

### 20.1 General Description

The Hibernation Timer can generate a wake event to the Embedded Controller (EC) when it is in a hibernation mode. This block supports wake events up to 2 hours in duration. The timer is a 16-bit binary count-down timer that can be programmed in 30.5 $\mu$ s and 0.125 second increments for period ranges of 30.5 $\mu$ s to 2s or 0.125s to 136.5 minutes, respectively. The Hibernation Timer asserts a wake-up interrupt when the count reaches zero. See [IRQ31 Source Register on page 361](#) for details on enabling the Hibernation Timer wake-up event. Writing a non-zero value to this register starts the counter from that value.

### 20.2 Block Diagram

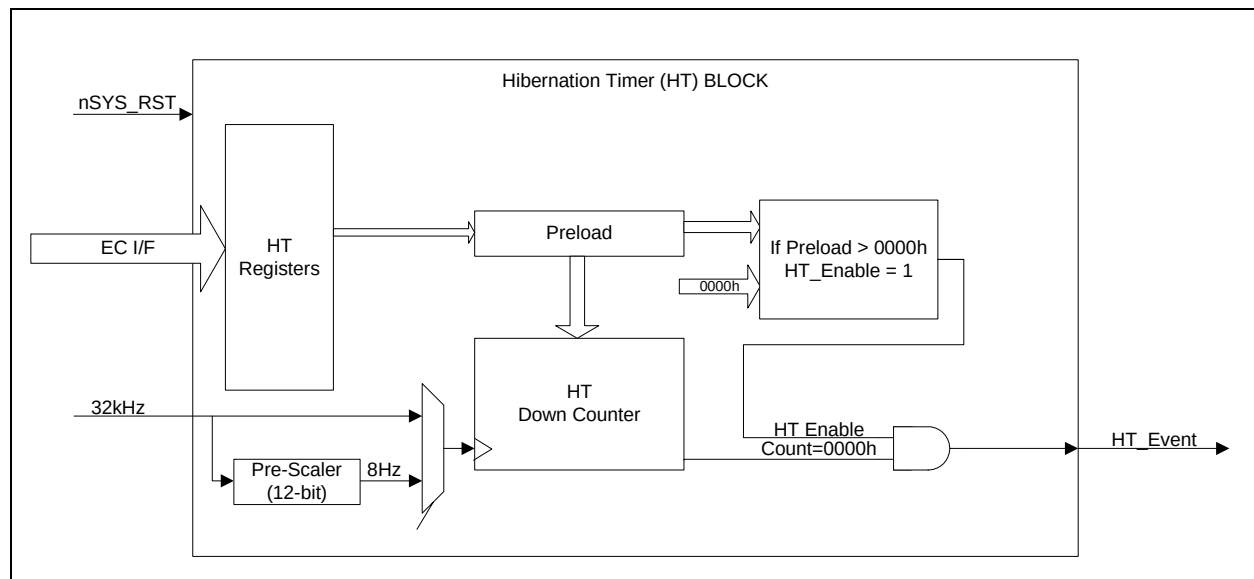


Figure 20.1 Hibernation Timer Block Diagram

### 20.3 Block Diagram Signal List

Table 20.1 Block Diagram Signal List Description

| SIGNAL NAME              | DIRECTION | DESCRIPTION                                                                                                                        |
|--------------------------|-----------|------------------------------------------------------------------------------------------------------------------------------------|
| <a href="#">nSYS_RST</a> | INPUT     | VTR Power on Reset.                                                                                                                |
| <a href="#">X32K_CLK</a> | INPUT     | 32Khz, Clock Source for Hibernation Timer                                                                                          |
| HT_Active                | OUTPUT    | Signal indicating that the timer is enabled and actively counting                                                                  |
| HT_Event                 | OUTPUT    | Signal indicating that the timer is enabled and has expired. This signal is used to generate an Hibernation Timer interrupt event. |
| E/C IF                   | I/O Bus   | Bus used by microprocessor to access the registers in this block.                                                                  |

## 20.4 Power, Clocks and Reset

### 20.4.1 Power Domain

This block is powered by the VTR Power Supply.

See [Section 4.5, "Power Configuration," on page 96](#) for details on power domains.

### 20.4.2 Clocks

This block has two clock inputs, the [EC Bus Clock](#), and [X32K\\_CLK](#). The [EC Bus Clock](#) is used in the interface to the embedded controller accessible registers. The 32.768KHz [X32K\\_CLK](#) is the clock source for the Hibernation Timer functional logic, including the counters.

See [Section 4.4, "Clock Generator," on page 77](#) for details on clocks.

### 20.4.3 Reset

This block is reset on a [nSYS\\_RST](#).

See [Section 4.6, "Reset Interface," on page 99](#) for details on reset.

## 20.5 Interrupts

Each instance of the Hibernation Timer in the MEC5035 can be used to generate interrupts and wake-up events when the timer underflows. The Hibernation Timer interrupts are routed to the [HTIMER1](#) & [HTIMER0](#) bits in [IRQ31 Source Register on page 361](#).

## 20.6 Registers

There are two instances of [Hibernation Timer](#) block implemented in the MEC5035 enumerated as [Hibernation Timer.0](#) & [Hibernation Timer.1](#). Each instance of the [Hibernation Timer](#) has its own Logical Device Number, and Base Address as indicated in [Table 20.2](#).

**Table 20.2 Hibernation Timer Base Address Table**

| Hibernation<br>Timer<br>INSTANCE        | LDN<br>FROM<br>( <a href="#">Table 7.2</a><br>on<br><a href="#">page 167</a> ) | AHB BASE ADDRESS               |
|-----------------------------------------|--------------------------------------------------------------------------------|--------------------------------|
| <a href="#">Hibernation<br/>Timer.0</a> | 0h                                                                             | <a href="#">F0_0000h</a>       |
| <a href="#">Hibernation<br/>Timer.1</a> |                                                                                | <a href="#">F0_0000h</a> + 80h |

The [Table 20.3](#) is a register summary for one instance of the [Hibernation Timer](#). Each EC address is indicated as an SPB Offset from its AHB base address.

Table 20.3 Hibernation Timer Register Summary

| REGISTER NAME                                      | EC INTERFACE |           |         | NOTES |
|----------------------------------------------------|--------------|-----------|---------|-------|
|                                                    | SPB OFFSET   | BYTE LANE | EC TYPE |       |
| <a href="#">HTimer Preload Register</a>            | 00h          | 1-0       | R/W     |       |
| <a href="#">Hibernation Timer Control Register</a> | 04h          | 0         | R/W     |       |
| <a href="#">Hibernation Timer Count Register</a>   | 08h          | 1-0       | R       |       |

## 20.6.1 HTimer x Preload Register

Table 20.4 HTimer Preload Register

| HOST ADDRESS | n/a              |     |     | n/a    |     |     | HOST SIZE           |     |
|--------------|------------------|-----|-----|--------|-----|-----|---------------------|-----|
| EC OFFSET    | 00h              |     |     | 16-bit |     |     | EC SIZE             |     |
| POWER        | VTR              |     |     | 0000h  |     |     | nSYS_RST<br>DEFAULT |     |
| BUS          | EC SPB           |     |     |        |     |     |                     |     |
| BIT          | D15              | D14 | D13 | ...    |     | D2  | D1                  | D0  |
| HOST TYPE    | -                | -   | -   | -      | -   | -   | -                   | -   |
| EC TYPE      | R/W              | R/W | R/W | R/W    | R/W | R/W | R/W                 | R/W |
| BIT NAME     | HT Preload[15:0] |     |     |        |     |     |                     |     |

### HT PRELOAD[15:0]

This register is used to set the Hibernation Timer Preload value. Writing this register to a non-zero value resets the down counter to start counting down from this programmed value. Writing this register to 0000h disables the hibernation counter. The resolution of this timer is determined by the CTRL bit in the [HTimer x Control Register](#).

## 20.6.2 HTimer x Control Register

Table 20.5 Hibernation Timer Control Register

| HOST ADDRESS | n/a      |     |     | n/a    |   |    | HOST SIZE           |      |
|--------------|----------|-----|-----|--------|---|----|---------------------|------|
| EC OFFSET    | 04h      |     |     | 16-bit |   |    | EC SIZE             |      |
| POWER        | VTR      |     |     | 0000h  |   |    | nSYS_RST<br>DEFAULT |      |
| BUS          | EC SPB   |     |     |        |   |    |                     |      |
| BIT          | D15      | D14 | D13 | ...    |   | D2 | D1                  | D0   |
| HOST TYPE    | -        | -   | -   | -      | - | -  | -                   | -    |
| EC TYPE      | R        |     |     |        |   |    |                     | R/W  |
| BIT NAME     | Reserved |     |     |        |   |    |                     | CTRL |

### CTRL

0= The Hibernation Timer has a resolution of 30.5us per LSB, which yields a maximum time of ~2seconds.

1= The Hibernation Timer has a resolution of 0.125s per LSB, which yields a maximum time in excess of 2 hours.

## 20.6.3 HTimer x Count Register

Table 20.6 Hibernation Timer Count Register

| HOST ADDRESS | n/a         |     |     | n/a    |   |    | HOST SIZE           |    |
|--------------|-------------|-----|-----|--------|---|----|---------------------|----|
| EC OFFSET    | 08h         |     |     | 16-bit |   |    | EC SIZE             |    |
| POWER        | VTR         |     |     | 0000h  |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB      |     |     |        |   |    |                     |    |
| BIT          | D15         | D14 | D13 | ...    |   | D2 | D1                  | D0 |
| HOST TYPE    | -           | -   | -   | -      | - | -  | -                   | -  |
| EC TYPE      | R           |     |     |        |   |    |                     |    |
| BIT NAME     | Count[15:0] |     |     |        |   |    |                     |    |

### COUNT[15:0]

The current state of the Hibernation Timer.



## Product Customer Specification-ODM

## 20.7 Hibernation Timer Revision History

This revision history shows the changes made to this chapter.

**Table 20.7 Hibernation Timer Chapter Revision History**

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History," on page 539.</a> |              |      |                      |            |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------|----------------------|------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE | SECTION/FIGURE/ENTRY | CORRECTION |
| 1.                                                                                                                                                                                                                                          |              |      |                      |            |
| 2.                                                                                                                                                                                                                                          |              |      |                      |            |
| 3.                                                                                                                                                                                                                                          |              |      |                      |            |

## Chapter 21 Week Alarm Interface

### 21.1 General Description

This block provides a 16-bit, battery-powered, Week Timer that supports 1ms, 1 second and 1 minute resolution and auto reloads following a counter underflow.

In addition, this block has the VBAT Power Control Logic.

### 21.2 Block Diagram

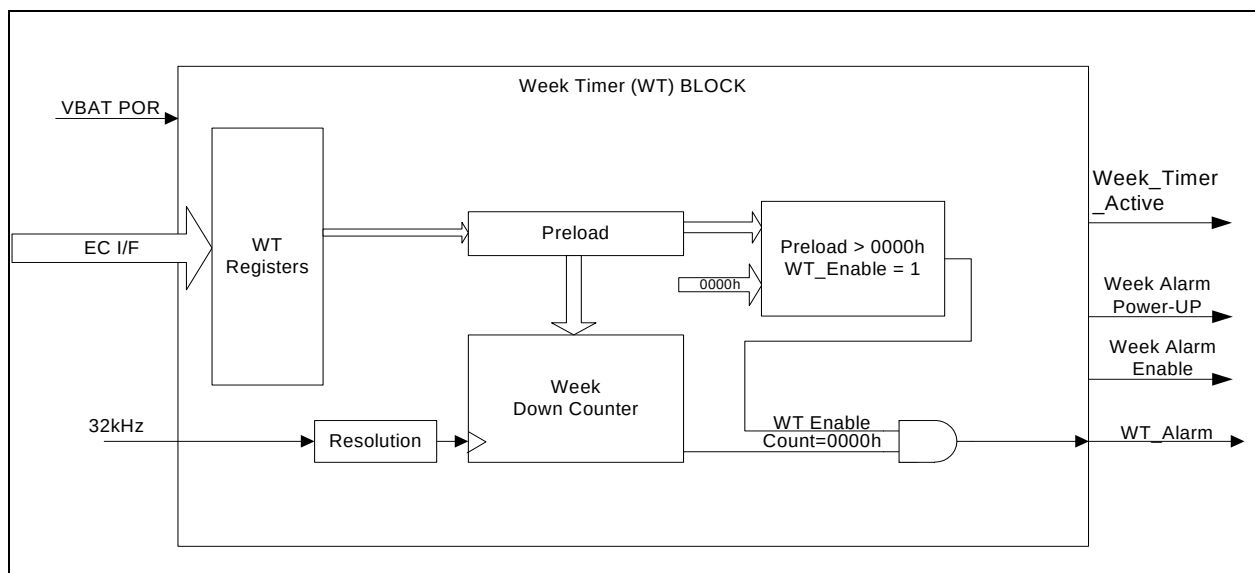


Figure 21.1 Week Timer Block Diagram

### 21.3 Signal List for Block Diagram

Table 21.1 Week Alarm Interface Signal List

| SIGNAL NAME                | DIRECTION | DESCRIPTION                                                 |
|----------------------------|-----------|-------------------------------------------------------------|
| VBAT_POR                   | Input     | VTR Power on Reset.                                         |
| EC Bus Clock               | Input     | Bus Clock                                                   |
| X32K_CLK                   | Input     | Core logic clock                                            |
| Week Alarm Power-Up Output | Output    | Week Timer wake up event signal                             |
| WEEK_ALRM_EN               | Output    | Output to control the function of the Week Timer Output     |
| WEEK_ALR                   | Output    | Week Timer Interrupt indicating that the timer has expired. |

**Table 21.1 Week Alarm Interface Signal List**

| SIGNAL NAME       | DIRECTION | DESCRIPTION                                                                                                                                       |
|-------------------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| Week_Timer_Active | Output    | The Week_Timer_Active output is asserted when the counter is enabled and counting. It is cleared when the Week_Timer is disabled or not counting. |
| BGPO0             | Output    | VBAT powered GPIO control                                                                                                                         |
| SPB Interface     | I/O Bus   | Bus used by microprocessor to access the registers in this block.                                                                                 |

## 21.4 Power, Clocks and Reset

### 21.4.1 Power Domain

This block is powered by the VBAT power supply.

See [Section 4.5, "Power Configuration," on page 96](#) for details on power domains.

### 21.4.2 Clocks

This block has two clock inputs: [EC Bus Clock](#) and the [X32K\\_CLK](#). [EC Bus Clock](#) is used by the EC Data Memory Bus to interface to the embedded controller accessible registers. The 32.768KHz [X32K\\_CLK](#) clock source is the clock source for the week alarm logic.

See [Section 4.4, "Clock Generator," on page 77](#) for details on clocks.

### 21.4.3 Power On Reset

This block is reset on [VBAT\\_POR](#).

See [Section 4.6, "Reset Interface," on page 99](#) for details on reset.

## 21.5 Interrupts

The [Week Alarm Interface](#) generates an interrupt and wakeup event following a Week Timer underflow. The Interrupt is routed [WEEK\\_ALR](#) in [IRQ31 Source Register](#). The [WEEK\\_ALR](#) wake and interrupt event can be asserted when VBAT is powered and VTR is unpowered. The [WEEK\\_ALR](#) wake event and Interrupt event is retained during VBAT and is detected after the next VTR POR power sequence.

## 21.6 Week Timer

The Week\_Timer\_Active output is asserted when the counter is enabled and counting. It is cleared when the Week\_Timer is disabled or not counting.

## 21.7 Week Alarm Power-Up Output

The internal Week Alarm Power-Up Output signal drives an input to the [VBAT-Powered Control Interface](#) as described in [Chapter 22, "VBAT-Powered Control Interface," on page 410](#). The [Week Alarm Power-Up Output](#) signal is driven even when the VTR supply is unpowered.

The [WEEK\\_ALRM\\_EN](#) bit in the [Week Timer Control Register](#) enables the [Week Alarm Power-Up Output](#) function in the [VBAT-Powered Control Interface](#) (see [Figure 22.1 on page 410](#)). Once the internal [Week Alarm Power-Up Output](#) signal drives the input to the [VBAT-Powered Control Interface](#)



as a result of an [Interrupts](#), the [WEEK\\_ALRM\\_EN](#) bit must be cleared to reset the [Week Alarm Interface](#).

**APPLICATION NOTE:** The [WEEK\\_ALRM\\_EN](#) bit defaults to '0,' disabling the ability to power the system up by the [Week Alarm Interface](#). This is necessary to avoid an uninitialized [Week Alarm Interface](#) from causing unintended power-up events.

## 21.8 Registers

The [Week Alarm Interface](#) has its own Logical Device Number, and Base Address as indicated in [Table 21.2](#). [Table 21.3](#) is a register summary for the [Week Alarm Interface](#) block. See [Note 7.3](#) on [page 168](#).

**Table 21.2** [Week Alarm Interface](#) Base Address Table

| Week Alarm Interface BLOCKS      | LDN FROM<br>( <a href="#">Table 7.3</a> on <a href="#">page 168</a> ) | AHB BASE ADDRESS         |
|----------------------------------|-----------------------------------------------------------------------|--------------------------|
| <a href="#">Week Alarm Timer</a> | 33h                                                                   | <a href="#">F0_CC80h</a> |

[Table 21.3](#) is a register summary for the [Week Alarm Interface](#) block. Each EC address is indicated as an SPB Offset from its AHB base address.

**Table 21.3** [Week Alarm Interface](#) Register Summary

| REGISTER NAME                               | EC INTERFACE |           |         | NOTES |
|---------------------------------------------|--------------|-----------|---------|-------|
|                                             | SPB OFFSET   | BYTE LANE | EC TYPE |       |
| <a href="#">Week Timer Control Register</a> | 00h          | 0         | R/W     |       |
| <a href="#">Week Timer Reload Register</a>  | 04h          | 0:1       | R/W     |       |
| <a href="#">Week Timer Data Register</a>    | 08h          | 0:1       | R       |       |

### 21.8.1 Week Timer Control Register

The [Week Timer Control Register](#) is used to configure the [Week Timer](#).



Table 21.4 Week Timer Control Register

| HOST ADDRESS | n/a      |               |       | n/a      |    |                 | HOST SIZE           |           |
|--------------|----------|---------------|-------|----------|----|-----------------|---------------------|-----------|
| EC OFFSET    | 00h      |               |       | 8-bit    |    |                 | EC SIZE             |           |
| POWER        | VBAT     |               |       | 01h      |    |                 | VBAT_POR<br>DEFAULT |           |
| BUS          | EC SPB   |               |       |          |    |                 |                     |           |
| BYTE0 BIT    | D7       | D6            | D5    | D4       | D3 | D2              | D1                  | D0        |
| HOST TYPE    | -        | -             | -     | -        | -  | -               | -                   | -         |
| EC TYPE      | R        | R/W           | R     | R        | R  | R/W (Note 21.1) |                     | R/W       |
| BIT NAME     | Reserved | WEEK_ALARM_EN | BGPO0 | Reserved |    | Resolution      |                     | WT_ENABLE |

**WT\_ENABLE**

Week Timer Enable - This bit is used to start and stop the Week Timer. The Week timer is held when the timer is disabled and starts counting from the value in the Week Timer Reload register when enabled.

0 - Week Timer is disabled.  
1 - Week Timer is enabled.

(See [Note 21.1 on page 408](#))

**RESOLUTION**

Week Timer Resolution - These bits are used to control the resolution of the Week Timer counter.

00 - 1 minute resolution.  
01 - 1 Second resolution  
10 - 1 Millisecond resolution.

**BGPO0**

VBAT-powered General Purpose Output Control that is used as part of the [VBAT-Powered Control Interface](#).

0= output low (default)  
1= output high

**WEEK\_ALARM\_EN**

VCI Week Alarm Enable- This bit controls the routing of the [Week Alarm Power-Up Output](#) output to [VBAT-Powered Control Interface](#) to assert the VCI signal. Once the internal [WEEK\\_ALARM\\_EN](#) signal drives the input to the [VBAT-Powered Control Interface](#) as a result of an [Interrupts](#), this bit must be cleared to reset the [Week Alarm Interface](#).

0 - Disable routing (Default)  
1 - Enable routing

**Note:** the Week Timer Enable bit [D0] must be cleared ('0') when changing the Week Timer Resolution bits. For example to change the resolution of the Week Timer two writes to the [Week Timer Control Register](#) are required: the first write de-asserts the [WT\\_ENABLE](#) bit, the second write modifies the [RESOLUTION](#) bits and asserts the [WT\\_ENABLE](#) bit.

## 21.8.2 Week Timer Reload Register

**Table 21.5 Week Timer Reload Register**

|              |                               |     |     |     |        |    |                     |    |
|--------------|-------------------------------|-----|-----|-----|--------|----|---------------------|----|
| HOST ADDRESS | n/a                           |     |     |     | n/a    |    | HOST SIZE           |    |
| EC OFFSET    | 04h                           |     |     |     | 16-bit |    | EC SIZE             |    |
| POWER        | VBAT                          |     |     |     | 2760h  |    | VBAT_POR<br>DEFAULT |    |
| BUS          | EC SPB                        |     |     |     |        |    |                     |    |
| BIT          | D15                           | D14 | D13 | ... |        | D2 | D1                  | D0 |
| HOST TYPE    | -                             | -   | -   | -   | -      | -  | -                   | -  |
| EC TYPE      | R/W <a href="#">Note 21.1</a> |     |     |     |        |    |                     |    |
| BIT NAME     | WEEK TIMER RELOAD[15:0]       |     |     |     |        |    |                     |    |

### WEEK TIMER RELOAD[15:0]

This register contains the value that is used to reload the [Week Timer Data Register](#) when the latter underflows. A Reload value of 0000h is equivalent to a reload value of FFFFh. In both cases the Week Timer will count  $2^{16}$  times before triggering an interrupt.

**Note 21.1** The EC must clear the Enable bit in the [Week Timer Control Register](#) to perform a write access to the [Week Timer Reload Register](#).

**Note 21.2** A write to the [Week Timer Reload Register](#) of 0000h will be treated as a full count (FFFFh +1) and start downcounting when the [WT\\_ENABLE](#) bit in the [Week Timer Reload Register](#) is set to '1'.

## 21.8.3 Week Timer Data Register

Table 21.6 Week Timer Data Register

| HOST ADDRESS | n/a                      |     |     |     | n/a    |    | HOST SIZE           |    |
|--------------|--------------------------|-----|-----|-----|--------|----|---------------------|----|
| EC OFFSET    | 08h                      |     |     |     | 16-bit |    | EC SIZE             |    |
| POWER        | VBAT                     |     |     |     | 2760h  |    | VBAT_POR<br>DEFAULT |    |
| BUS          | EC SPB                   |     |     |     |        |    |                     |    |
| BIT          | D15                      | D14 | D13 | ... |        | D2 | D1                  | D0 |
| HOST TYPE    | -                        | -   | -   | -   | -      | -  | -                   | -  |
| EC TYPE      | R                        |     |     |     |        |    |                     |    |
| BIT NAME     | WEEK TIMER Counter[15:0] |     |     |     |        |    |                     |    |

### WEEK TIMER COUNTER[15:0]

The current state of the Week Timer.

## 21.9 Week Alarm Interface Revision History

This revision history shows the changes made to this chapter.

Table 21.7 Week Alarm Interface Chapter Revision History

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History," on page 539.</a> |              |            |                                                                                                                         |                                                                                      |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------------|-------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE       | SECTION/FIGURE/ENTRY                                                                                                    | CORRECTION                                                                           |
| 1.                                                                                                                                                                                                                                          | 0.4          | 05/09/2007 | <a href="#">Section 21.4.3, "Power On Reset," on page 405</a><br><a href="#">Section 21.8, "Registers," on page 406</a> | No nSYSRST in this block.<br><br>Editorial changed <a href="#">VBAT_POR</a> to xref. |
| 2.                                                                                                                                                                                                                                          | 0.5          | 05/29/2007 | <a href="#">Table 21.1 on page 404</a><br><a href="#">Note 21.2 on page 408</a>                                         | nSYSRST s/b <a href="#">VBAT_POR</a><br>load 0000 = FFFF+1                           |
| 3.                                                                                                                                                                                                                                          |              |            |                                                                                                                         |                                                                                      |
| 4.                                                                                                                                                                                                                                          |              |            |                                                                                                                         |                                                                                      |

## Chapter 22 VBAT-Powered Control Interface

### 22.1 General Description

The [VBAT-Powered Control Interface](#) has VBAT powered combinational logic and Input and output Signal Pins. The [VBAT-Powered Control Interface](#) has one VTR powered register. The [VBAT-Powered Control Interface](#) block interfaces with the VBAT powered [Week Alarm Interface](#) on page 404 and the VTR powered Pin Control Registers [Pin Control Register \[000:176\]](#) on page 376.

### 22.2 Features

### 22.3 Block Diagram

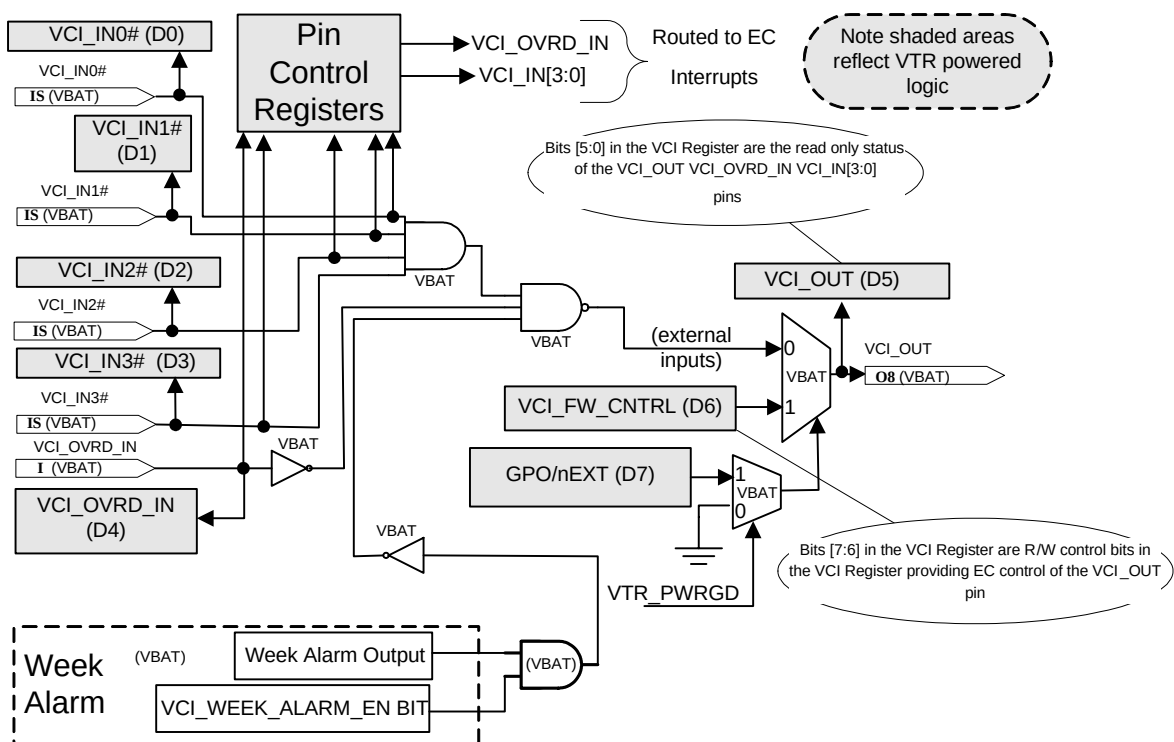


Figure 22.1 VBAT-Powered Control Interface Block Diagram

**Note:** Shaded bit are located in this block in the [VCI register](#), all other logic is in the [Week Alarm Interface](#)

### 22.4 Block Diagram Signal List

Table 3.11, "Power Switch Interface," on page 45 includes the Pin Signal Function descriptions for the [VBAT-Powered Control Interface](#).

**Table 22.1 VBAT-Powered Control Interface Signal List**

| SIGNAL NAME       | DIRECTION | DESCRIPTION                                                                           |
|-------------------|-----------|---------------------------------------------------------------------------------------|
| VCI_OUT           | Output    | <a href="#">VBAT-Powered Control Interface</a> Pin Status Bit                         |
| VCI_IN[3:0]#      | Input     |                                                                                       |
| VCI_OVRD_IN       | Output    | Mux control in the VBAT control logic See <a href="#">Week Alarm Interface</a>        |
| Week Alarm Output | Input     | Asserted signal enables Week Alarm terminal count to assert <a href="#">VCI_OUT</a>   |
| VCI_WEEK_ALARM_EN | Input     | Asserted signal enables Week Alarm terminal count to assert <a href="#">VCI_OUT</a> . |
| Interrupts        | Output    | See <a href="#">Section 22.6, "Interrupts," on page 411</a>                           |
| uP Interface      | I/O Bus   | Bus used by microprocessor to access the registers in this block.                     |

This block is powered by the VBAT power supply.

## 22.5 Power, Clocks and Reset

### 22.5.1 Power Domain

This block is in the VTR power domain for EC interaction and uses the VBAT power domain for memory retention.

See [Section 4.5, "Power Configuration," on page 96](#) for details on power domains.

### 22.5.2 Clocks

The [VBAT-Powered Control Interface](#) has one clock input, the [EC Bus Clock](#), which is used to interface to the embedded controller accessible register.

See [Section 4.4, "Clock Generator," on page 77](#) for details on clocks.

### 22.5.3 Power On Reset

The [VBAT-Powered Control Interface](#) is reset on a [VBAT\\_POR](#). [VCI Register on page 414](#) are VTR powered and on a [nSYS\\_RST](#). See [Section 4.6.4, "nSYS\\_RST," on page 101](#).

See [Section 4.6, "Reset Interface," on page 99](#) for details on reset.

## 22.6 Interrupts

The [VBAT-Powered Control Interface](#) generates interrupts and wakeup events for the following pin inputs: [VCI\\_IN\[3:0\]#](#) & [VCI\\_OVRD\\_IN](#). The Interrupts is routed [VCI\\_OVRD\\_IN](#), [VCI\\_IN0](#), [VCI\\_IN1](#), [VCI\\_IN2](#), [VCI\\_IN3](#), bits in [IRQ31 Source Register](#). The [VBAT-Powered Control Interface](#) Interrupt and wake events can only be asserted when VBAT and VTR is both applied; edge detection is disabled when VTR is unpowered. The edge detection for the interrupt and wake events are controlled each pin by the pin's associated Pin Control Register. See [Pin Control Register \[000:176\] on page 376](#).

## 22.7 General Description

The MEC5035 [VBAT-Powered Control Interface](#) (VCI) is illustrated in [Figure 22.1](#). This block contains the [VCI Register](#). This register monitors the status of the [VCI\\_IN\[3:0\]#](#), [VCI\\_OVRD\\_IN](#), & [VCI\\_OUT](#) pins and also provides firmware control of [VCI\\_OUT](#) when VTR is present.

The state of the [VCI\\_OUT](#) pin can be determined using the [Table 22.2, "VCI Output Truth Table,"](#) on [page 412](#). Signals in [Table 22.2](#) are described in [Section Table 22.1, "VBAT-Powered Control Interface Signal List,"](#) on [page 411](#) and in [Section 22.10, "VCI Register,"](#) on [page 414](#).

**Table 22.2 VCI Output Truth Table**

| INPUTS                          |                              |                              |                              |                              |                                   |                                   |                                  |                              |                       | OUTPUT                      | DESCRIPTION                                                                                                 |
|---------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|-----------------------------------|-----------------------------------|----------------------------------|------------------------------|-----------------------|-----------------------------|-------------------------------------------------------------------------------------------------------------|
| <a href="#">VCI_OVRD_IN</a> PIN | <a href="#">VCI_IN0#</a> PIN | <a href="#">VCI_IN1#</a> PIN | <a href="#">VCI_IN2#</a> PIN | <a href="#">VCI_IN3#</a> PIN | <a href="#">Week Alarm Output</a> | <a href="#">VCI_WEEK_ALARM_EN</a> | <a href="#">VCI_FW_CNTRL BIT</a> | <a href="#">GPO/nEXT BIT</a> | <a href="#">VTRGD</a> | <a href="#">VCI_OUT</a> PIN |                                                                                                             |
| X                               | 0                            | X                            | X                            | X                            | X                                 | X                                 | X                                | X                            | 0                     | 1                           | VTR = OFF<br>External inputs<br>can drive<br><a href="#">VCI_OUT</a>                                        |
| X                               | X                            | 0                            | X                            | X                            | X                                 | X                                 | X                                | X                            | 0                     | 1                           |                                                                                                             |
| X                               | X                            | X                            | 0                            | X                            | X                                 | X                                 | X                                | X                            | 0                     | 1                           |                                                                                                             |
| X                               | X                            | X                            | X                            | 0                            | X                                 | X                                 | X                                | X                            | 0                     | 1                           |                                                                                                             |
| 1                               | X                            | X                            | X                            | X                            | X                                 | X                                 | X                                | X                            | 0                     | 1                           |                                                                                                             |
| X                               | X                            | X                            | X                            | X                            | 1                                 | 1                                 | X                                | X                            | 0                     | 1                           |                                                                                                             |
| 0                               | 1                            | 1                            | 1                            | 1                            | 0                                 | 0                                 | X                                | X                            | 0                     | 0                           |                                                                                                             |
| X                               | 0                            | X                            | X                            | X                            | X                                 | X                                 | X                                | 0                            | 1                     | 1                           | VTR = ON<br>External inputs<br>can drive<br><a href="#">VCI_OUT</a><br>( <a href="#">GPO/nEXT</a> =<br>'0') |
| X                               | X                            | 0                            | X                            | X                            | X                                 | X                                 | X                                | 0                            | 1                     | 1                           |                                                                                                             |
| X                               | X                            | X                            | 0                            | X                            | X                                 | X                                 | X                                | 0                            | 1                     | 1                           |                                                                                                             |
| X                               | X                            | X                            | X                            | 0                            | X                                 | X                                 | X                                | 0                            | 1                     | 1                           |                                                                                                             |
| X                               | X                            | X                            | X                            | X                            | 1                                 | 1                                 | X                                | 0                            | 1                     | 1                           |                                                                                                             |
| 1                               | X                            | X                            | X                            | X                            | X                                 | X                                 | X                                | 0                            | 1                     | 1                           |                                                                                                             |
| 0                               | 1                            | 1                            | 1                            | 1                            | 0                                 | 0                                 | X                                | 0                            | 1                     | 0                           |                                                                                                             |
| X                               | X                            | X                            | X                            | X                            | X                                 | X                                 | 0                                | 1                            | 1                     | 0                           | VTR = ON<br>EC drives<br><a href="#">VCI_OUT</a><br>( <a href="#">GPO/nEXT</a> =<br>'1')                    |
| X                               | X                            | X                            | X                            | X                            | X                                 | X                                 | 1                                | 1                            | 1                     | 1                           |                                                                                                             |

**Note:** When [VTRGD](#) is not asserted '0,' VTR is unpowered and both the EC and the [VCI register](#) are unavailable. When [VTRGD](#) is asserted '1,' the VTR well is powered, the [VCI register](#) is powered, accessible to the EC, and contributes to the resultant logic driving the [VCI\\_OUT](#) pin.

**APPLICATION NOTE:** The [VBAT-Powered Control Interface](#) can be used in a system as follows:



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1. The initial condition is the VBAT battery is installed causing a **VBAT\_POR**, no AC power applied and no power button event. Therefore no power is applied to VTR power well. The **VCI\_OUT** pin is de-asserted, the EC is not running, the Week Alarm has not been initialized or enabled.
2. Either applying AC charger power and asserting the **VCI\_OVRD\_IN** input or depressing a power button asserting a one or more of the **VCI\_IN[3:0]#** input pins causes the **VCI\_OUT** pin to be asserted (maybe a pulse for seconds). This powers up the VTR power well. This starts the EC and allows access to the **VCI register**.
3. If the **VCI register** is not written then the **VBAT-Powered Control Interface** glue logic behaves the same way as when VTR is empowered; the **VCI\_OUT** pin is asserted when any one of the an external input (**Figure 22.1 on page 410**) are asserted: the **VCI\_OVRD\_IN**, or **VCI\_IN[3:0]#**, or the Week Alarm Power-up signal are asserted.
4. The EC can read the status of the **VCI\_OVRD\_IN** and **VCI\_IN[3:0]#** in the **VCI register** (similar to a GP input.) The EC can enable interrupts from these pins.
5. The EC can take programmable control of the **VCI\_OUT** pin output by setting both the **VCI\_FW\_CNTRL** and the **GPO/nEXT** bits in the **VCI register**.

**Note:** BIOS should set **VCI\_FW\_CNTRL** bit to 1 prior to setting the **GPO/nEXT** bit to 1 to guarantee a glitch free **VCI\_OUT** pin output.

6. Clearing the **VCI\_FW\_CNTRL** bit and setting the **GPO/nEXT** bit in the **VCI register** causes the **VCI\_OUT** pin to be de-asserted. The **VCI\_OUT** pin remains de-asserted until VTR is empowered. When VTR=0, the **VCI\_OVRD\_IN** and **VCI\_IN[3:0]#** inputs pins control the **VCI\_OUT** pin.

**Note:** The **VCI\_IN[3:0]#** pins have no direct effect on the **VCI\_OUT** pin when **VCI\_OVRD\_IN** is asserted. However, when VTR is on and EC is running, the **VCI\_IN[3:0]#** pins can cause an interrupts and the EC can de-assert the **VCI\_OUT** pin by programming the **VCI\_FW\_CNTRL** and the **GPO/nEXT** bits in the **VCI register**. The **VCI\_OVRD\_IN** and the **VCI\_IN[3:0]#** pins can also cause EC wake events.

The state of the **VCI\_OUT** pin can be determined using the **Table 22.2, "VCI Output Truth Table," on page 412**. Signals in **Table 22.2** are described in **Section Table 22.1, "VBAT-Powered Control Interface Signal List," on page 411** and in **Section 22.10, "VCI Register," on page 414**.

**Note:** When **VTRGD on page 99** is not asserted '0,' VTR is unpowered and both the EC and the **VCI register** are unavailable. When **VTRGD** is asserted '1,' the VTR well is powered, the **VCI register** is powered, accessible to the EC, and contributes to the resultant logic driving the **VCI\_OUT** pin.

## 22.8 Registers

The **VBAT-Powered Control Interface** has its own Logical Device Number, and Base Address as indicated in **Table 22.3**.

**Table 22.4** is a register summary for the **VBAT-Powered Control Interface** block.

Each instance of the **VBAT-Powered Control Interface** Base Address as indicated in **Table 22.3**.

**Table 22.3 VBAT-Powered Control Interface Base Address Table**

| VBAT-Powered Control Interface INSTANCE | LDN FROM (Table 7.3 on page 168) | AHB BASE ADDRESS         |
|-----------------------------------------|----------------------------------|--------------------------|
| VBAT-Powered Control Interface          | 3Fh                              | FF_FD00h = FF_FC00h+100h |



**Note:** The VBAT-Powered Control Interface is in the Global Configuration Logical Device, Host Logical Device Number 3Fh, in EC-only space (see Section 7.4.2, "Address Framing," on page 169).

Table 22.4 is a register summary for the [VBAT-Powered Control Interface](#) block. Each EC address is indicated as an SPB Offset from its AHB base address.

**Table 22.4 VBAT-Powered Control Interface Register Summary**

| REGISTER NAME                | EC INTERFACE |           |         | NOTES |
|------------------------------|--------------|-----------|---------|-------|
|                              | SPB OFFSET   | BYTE LANE | EC TYPE |       |
| <a href="#">VCI register</a> | 00h          | 0         | R       |       |

## 22.9 Detailed Description of Accessible Registers

### 22.10 VCI Register

The [VCI Register](#) contains various pin status indicators and control bits. This register is

**Table 22.5 VCI register**

| HOST ADDRESS | NA           |                      |             |                     |             |    |    | HOST SIZE           |  |
|--------------|--------------|----------------------|-------------|---------------------|-------------|----|----|---------------------|--|
| EC OFFSET    | 00           |                      |             |                     | 8-bit       |    |    | EC SIZE             |  |
| POWER        | VTR          |                      |             |                     | 00h         |    |    | nSYS_RST<br>DEFAULT |  |
| BUS          | EC SPB       |                      |             |                     |             |    |    |                     |  |
| BYTE0 BIT    | D7           | D6                   | D5          | D4                  | D3          | D2 | D1 | D0                  |  |
| HOST TYPE    | -            | -                    | -           | -                   | -           | -  | -  | -                   |  |
| EC TYPE      | R/W          | R/W                  | R           | R                   | R           | R  | R  | R                   |  |
| BIT NAME     | GPO/<br>NEXT | VCI_<br>FW_<br>CNTRL | VCI_<br>OUT | VCI_<br>OVRD_<br>IN | VCI_IN[3:0] |    |    |                     |  |

**Note:** The [VCI\\_IN\[3:0\]#](#), [VCI\\_OVRD\\_IN](#), & [VCI\\_OUT](#) pins bits default at VCC1\_POR to the current state of their respective input pins.

#### [VCI\\_IN\[3:0\]](#)

These read-only bits provide the current status of the associated [VCI\\_IN\[3:0\]#](#) pins.

#### [VCI\\_OVRD\\_IN](#)

This read-only bit provides the current status of the [VCI\\_OVRD\\_IN](#) pin.

#### [VCI\\_OUT](#)

This read-only bit provides the current status of the [VCI\\_OUT](#) pin.

**Product Customer Specification-ODM****VCI\_FW\_CNTRL**

The **VCI\_FW\_CNTRL** allows EC firmware to control the **VCI\_OUT** pin. Clearing this bit can de-assert the active high **VCI\_OUT**.

**APPLICATION NOTE:** BIOS should set **VCI\_FW\_CNTRL** bit to 1 prior to setting the **GPO/nEXT** bit to 1 on power up.

**GPO/nEXT**

The **GPO/nEXT** bit controls the Mux selecting between the external **VBAT-Powered Control Interface Signal List** inputs and the **VCI\_FW\_CNTRL** bit output. When **GPO/nEXT** is set ('1'), **VCI\_OUT** follows the **VCI\_FW\_CNTRL** bit setting. When **GPO/nEXT** is clear ('0'), **VCI\_OUT** follows the external inputs.

## 22.11 VBAT-Powered Control Interface Revision History

This revision history shows the changes made to this chapter.

**Table 22.6 VBAT-Powered Control Interface Chapter Revision History**

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History," on page 539.</a> |              |      |                      |            |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------|----------------------|------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE | SECTION/FIGURE/ENTRY | CORRECTION |
| 1.                                                                                                                                                                                                                                          |              |      |                      |            |
| 2.                                                                                                                                                                                                                                          |              |      |                      |            |
| 3.                                                                                                                                                                                                                                          |              |      |                      |            |
| 4.                                                                                                                                                                                                                                          |              |      |                      |            |

## Chapter 23 VBAT POWERED RAM

### 23.1 Abstract

#### 23.1.0.1 Chip level Interface Clock domain/power domain crossings

Powered by VBAT but only clocked or accessed when VTR power is available.

### 23.2 General Description

The VBAT Powered RAM provides a 64 Byte Random Accessed Memory that is operational while VTR is powered, and will retain its values while powered by VBAT powered and VTR is unpowered. The RAM is organized as a 16 "words" x 32-bit wide for a total of 64 bytes.

### 23.3 Block Diagram

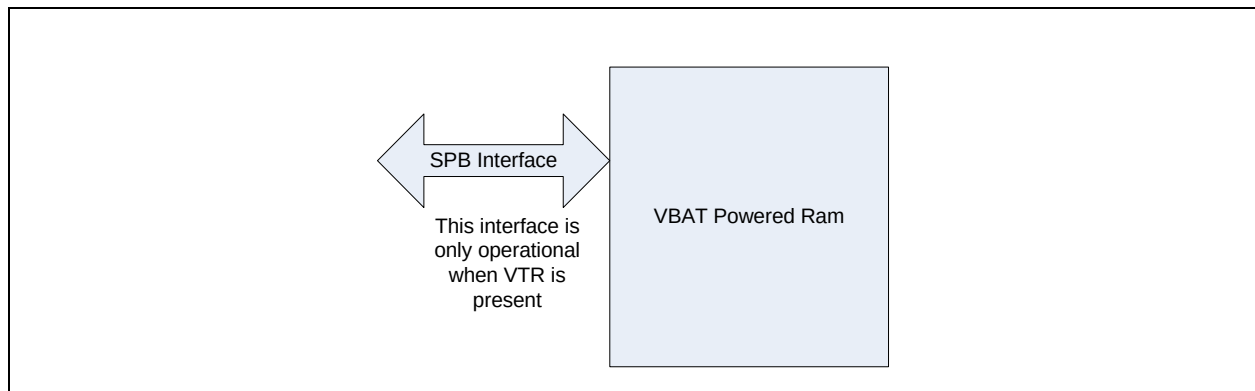


Figure 23.1 Block Diagram of VBAT POWERED RAM

### 23.4 Power, Clocks and Reset

#### 23.4.1 Power Domain

This block is in the VTR power domain for EC interaction and uses the VBAT power domain for memory retention

See [Section 4.5, "Power Configuration," on page 96](#) for details on power domains.

#### 23.4.2 Clocks

The [VBAT POWERED RAM](#) has one clock input., the [EC Bus Clock](#).

See [Section 4.4, "Clock Generator," on page 77](#) for details on clocks.

#### 23.4.3 Power On Reset

The [VBAT POWERED RAM](#) is reset on a [VBAT\\_POR](#).

See [Section 4.6, "Reset Interface," on page 99](#) for details on reset.

## 23.5 Interrupts

The **VBAT POWERED RAM** has not interrupts

## 23.6 Registers

The **VBAT POWERED RAM** has it's own Logical Device Number, and Base Address as indicated in [Table 23.1](#). See [Note 7.3 on page 168](#).

**Table 23.1** **VBAT POWERED RAM** Base Address Table

| <b>VBAT<br/>POWERED<br/>RAM<br/>BLOCKS</b> | <b>LDN<br/>FROM<br/>(Table 7.3<br/>on<br/>page 168)</b> | <b>AHB BASE ADDRESS</b> |
|--------------------------------------------|---------------------------------------------------------|-------------------------|
| VBAT Backed<br>Memory                      | 33h                                                     | F0_CD00h                |

Each 32-bit RAM location is an SPB Offset from the AHB base address.

## 23.7 VBAT POWERED RAM Revision History

This revision history shows the changes made to this chapter.

**Table 23.2** **VBAT POWERED RAM** Chapter Revision History

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History," on page 539</a> . |              |      |                      |            |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------|----------------------|------------|
| #                                                                                                                                                                                                                                            | REV# IN SPEC | DATE | SECTION/FIGURE/ENTRY | CORRECTION |
| 1.                                                                                                                                                                                                                                           |              |      |                      |            |
| 2.                                                                                                                                                                                                                                           |              |      |                      |            |
| 3.                                                                                                                                                                                                                                           |              |      |                      |            |
| 4.                                                                                                                                                                                                                                           |              |      |                      |            |





## Chapter 24 General Purpose Serial Peripheral Interface (GP-SPI)

### 24.1 General Description

The SPI interface may be used to communicate with various peripheral devices (EEPROMS, DACs, ADCs) that use a standard Serial Peripheral Interface (SPI).

Characteristics include:

- 8-bit serial data transmitted and received simultaneously over two data pins in Full Duplex mode with options to transmit and receive data serially on one data pin in Half Duplex (Bidirectional) mode.
- An internal programmable clock generator and clock polarity and phase controls allowing communication with various SPI peripherals with specific clocking requirements.
- SPI cycle completion that can be determined by status polling or interrupts.
- The ability to read data in on both SPDIN and SPDOUT in parallel. This allows this SPI Interface to support dual data rate read accesses for emerging double rate SPI flashes
- Support of back-to-back reads and writes without clock stretching, provided the host can read and write the data registers within one byte transaction time.

The MEC5035 SPI is a master only device and does not support multiple-master SPI configurations.

## 24.2 SPI Block Diagram

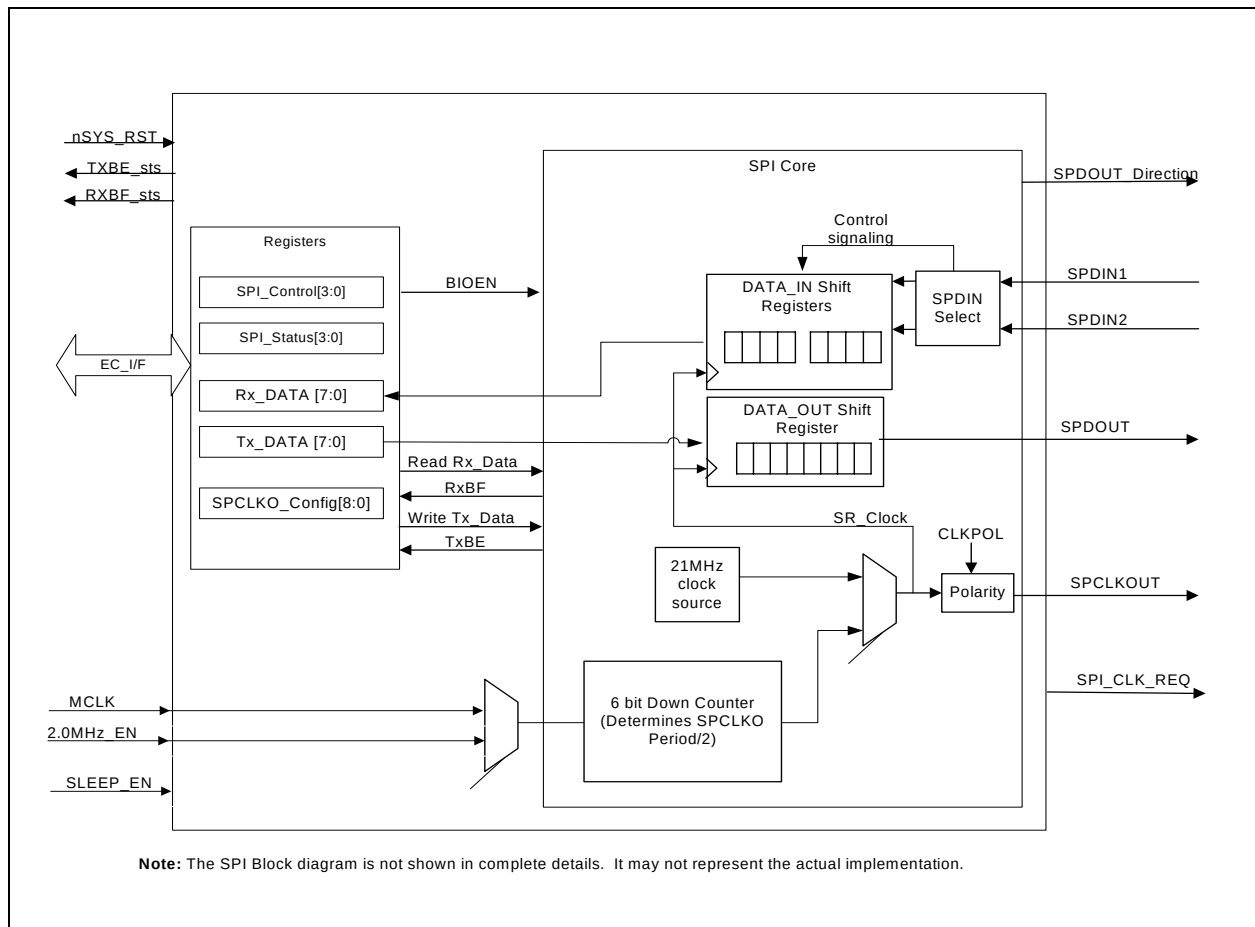


Figure 24.1 SPI Block Diagram

## 24.3 SPI Block Diagram Signal Description

The signal names in this chapter are

Table 24.1 SPI Block Signals

| SIGNAL                 | DIRECTION | DESCRIPTION                                                                       |
|------------------------|-----------|-----------------------------------------------------------------------------------|
| <code>nSYS_RST</code>  | INPUT     | VTR Power on Reset.                                                               |
| <code>TXBE_STS</code>  | OUTPUT    | Interrupt output to EC driven by TXBE status bit                                  |
| <code>RXBF_STS</code>  | OUTPUT    | Interrupt output to EC driven by RXBF status bit                                  |
| 64.52MHz               | INPUT     | Clock input to SPI Interface logic                                                |
| <code>2.0MHz_EN</code> | INPUT     | Clock Enable input to SPI Interface logic                                         |
| <code>SPDOUT</code>    | OUTPUT    | Serial Data Out to the SPDOUT pin                                                 |
| <code>SPDIN1</code>    | INPUT     | Serial Data In 1 from SPPDIN pin.<br>Input in full-duplex mode and Dual Read mode |

**Table 24.1 SPI Block Signals (continued)**

| SIGNAL           | DIRECTION | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|------------------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SPDIN2           | INPUT     | Serial Data In 2 from SPDOUT pin.<br>Input in bi-directional mode and Dual Read mode.                                                                                                                                                                                                                                                                                                                                                                                          |
| SPCLKOUT         | OUTPUT    | SPI Clock output used to drive the SPCLK pin.                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| SPDOUT_Direction | OUTPUT    | The SPDOUT pin may be used as an output or an input. This signal is used to determine the direction of the SPDOUT buffer.<br>0=output (SPDOUT pin is controlled by the <a href="#">SPDOUT</a> signal)<br>1=input (SPDOUT pin is an input driving the <a href="#">SPDIN2</a> signal)<br><br>The SPDOUT pin has I/O capability. The I/O capability is implemented to support the Half-Duplex mode of operation (also referred to as bi-directional mode) and the Dual Read mode. |
| SLEEP_EN         | INPUT     | External enable/disable signal used to put the block in the lowest power consumption state.<br>0=No Sleep Requested.<br>The block should operate as configured.<br>1=Sleep Requested.<br>The block enters sleep mode. See <a href="#">Low Power Mode on page 423</a> .                                                                                                                                                                                                         |
| SPI_CLK_REQ      | OUTPUT    | This output indicates when this block requires this clock input.<br>0= 64MHz can be turned 'off' when appropriate<br>1= 64MHz is required to be 'on.'                                                                                                                                                                                                                                                                                                                          |
| E/C IF           | I/O Bus   | Bus used by microprocessor to access the registers in this block.                                                                                                                                                                                                                                                                                                                                                                                                              |

## 24.4 SPI Interface Signals

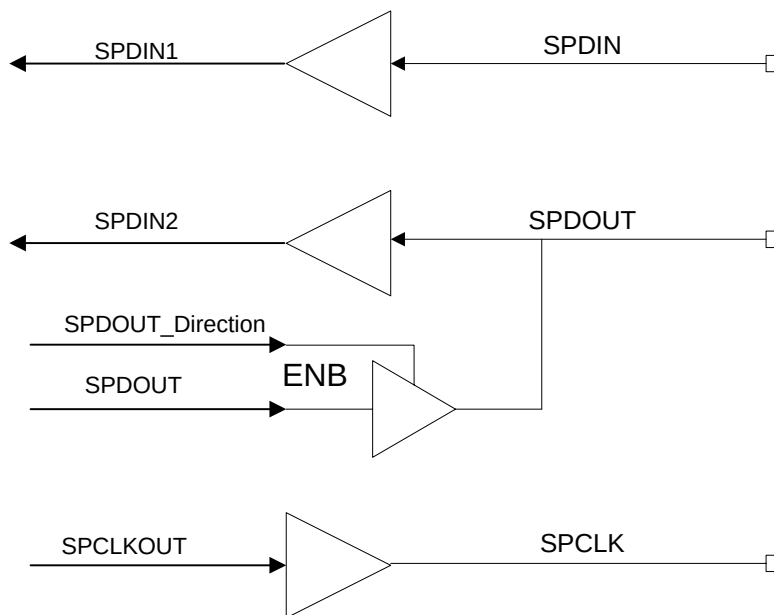
The following subsections describe the SPI Block Signals that are routed to the SPI pins. This chapter utilizes generic signal nomenclature for the Pin Signal Functions. [Table 24.2](#) is a specific lookup table for pin signal function names used in this chapter and used elsewhere. [Figure 24.2](#) show typical routing of the block interface (illustrated in [Figure 24.1](#) to the pins. [Table 3.9, "MISC Interface," on page 44](#) in [Chapter 3, Pinout and Pin Description](#) includes the pin description for the SPI interface.

Since there is only one instance of SPI port in the MEC5035, there is a one to one correspondence.

**Table 24.2 Pin Signal Function Nomenclature Lockup Table**

| MEC5035 pin | Routing Figure Generic Pin Signal Name | Pin Signal Function Name Used in other Chapter | Pin Function Signal Description |
|-------------|----------------------------------------|------------------------------------------------|---------------------------------|
| 67          | SPCLK                                  | ECGP_SCLK                                      | General Purpose SPI Clock       |
| 68          | SPDOUT                                 | ECGP_SOUT                                      | General Purpose SPI Output      |
| 69          | SPDIN                                  | ECGP_SIN                                       | General Purpose SPI Input       |





Note: This figure is for illustration purposes only, and not meant to imply specific implementation details

**Figure 24.2 Typical Block/Pin Interface**

#### 24.4.1 SPDOUT PIN - Serial Peripheral Data Out

In Full Duplex Mode, this is the serial data output to the SPI interface. In half-duplex mode (also referred to as bi-directional mode) this is the serial data I/O port for the SPI interface.

For special SPI Flash devices that support Dual Read Modes the SPDOUT operates as an input in parallel with the SPDIN during the data portion of the Fast Dual Read command.

**Note:** In the Bi-directional mode, some slave devices may tristate the last few bits to signal a turn-around; therefore, an external weak pull-up may be required on the pin.

#### 24.4.2 SPDIN PIN - Serial Peripheral Data In

In Full Duplex Mode, this is the serial data input from the SPI interface. In half-duplex mode (also referred to as bi-directional mode) this pin is unused.

**Note:** Some slave device may tristate the SPDIN pin during command phase; therefore, an external weak pull-up or pull-down may be required on the pin.

#### 24.4.3 SPCLK PIN - Serial Peripheral Clock

This is the serial clock driven by the MEC5035 SPI (master) and connected to all SPI slaves. All data (input and output) is sampled/shifted on SPCLK according to the clock controls CLKPH and CLKPOL (See [TCLKPH](#) and [CLKPOL](#) in [Section 24.11.6, "SPICC - SPI Clock Control Register," on page 436](#)).

**Note 24.1** In the MEC5035, the SPI interface has 8mA buffers. The maximum SPCLK pin clock frequency is 16.128MHz for all modes. Limited functionality is available at Although the block can be programmed for higher frequencies, performance is not guaranteed. See [Table 24.15 on page 438](#) and [Section 24.9.4.5, "Limits of SPI configurations," on page 430](#).



## 24.5 Power, Clocks and Reset

### 24.5.1 Power Domain

This block is powered by the VTR Power Supply.

See [Section 4.5, "Power Configuration," on page 96](#) for details on power domains.

### 24.5.2 Clocks

This block uses the [EC Bus Clock](#), the 64.52MHz ([MCLK](#)) and the 2MHz ([MCLK\\_DIV32\\_EN](#)). [EC Bus Clock](#) is used when reading and writing the [General Purpose Serial Peripheral Interface \(GP-SPI\)](#) registers. The 6-bit down counter may use either [MCLK](#) or [MCLK\\_DIV32\\_EN](#) to directly decrement the counter, which is the [SPCLKOUT](#) source.

See [Section 4.4, "Clock Generator," on page 77](#) for definition and details on clocks of: [MCLK on page 93](#), [MCLK\\_DIV32\\_EN on page 94](#), and [EC Bus Clock on page 94](#)

## 24.6 Reset

This block is reset on a [nSYS\\_RST](#). On reset, the General Purpose SPI interface defaults to disabled. The block can also be reset by software, by setting the Soft Reset bit located in the [SPICR - SPI Control Register](#). Setting this bit reinitializes the SPI Control block back to its [nSYS\\_RST](#) state.

See [Section 4.6, "Reset Interface," on page 99](#) for definition and details on reset: [nSYS\\_RST on page 101](#).

## 24.7 SPI Interrupts

The [General Purpose Serial Peripheral Interface \(GP-SPI\)](#) can generate an interrupt events to the Embedded Controller (EC) to indicate that the block requires servicing. The SPI TXBE status and RXBF status bits in the [SPISR - SPI Status Register on page 434](#) are routed onto the [SPI\\_TXBE\\_GP](#) & [SPI\\_RXBF\\_GP](#) bits of the [IRQ15 Source Register on page 332](#).

## 24.8 Low Power Mode

This block is designed to conserve power when it is either sleeping or disabled. There are two ways to put the SPI interface into a low power mode: Disabled the SPI Interface via the Enable Bit or Assert the [SLEEP\\_EN](#) signal to the SPI Interface. The following table summarizes the SPI behavior for each of these low power modes.

**Table 24.3 Block Clock Gating in Low Power Modes**

| ENABLE BIT | <a href="#">SLEEP_EN</a> | BLOCK IDLE STATUS | <a href="#">SPI_CLK_REQ</a> | STATE              | DESCRIPTION                                                                                  |
|------------|--------------------------|-------------------|-----------------------------|--------------------|----------------------------------------------------------------------------------------------|
| 0          | X                        | NOT IDLE          | 1                           | PREPARING to SLEEP | The core clock is required until the current transaction is completed and the Block is IDLE. |
|            |                          | IDLE              | 0                           | SLEEPING           | The block is idle and the core clock can be stopped.                                         |

Table 24.3 Block Clock Gating in Low Power Modes

| ENABLE BIT | SLEEP_EN | BLOCK IDLE STATUS | SPI_CLK_REQ | STATE              | DESCRIPTION                                                                                  |
|------------|----------|-------------------|-------------|--------------------|----------------------------------------------------------------------------------------------|
| 1          | 0        | X                 | 1           | NORMAL OPERATION   | The block is neither disabled by firmware nor commanded to SLEEP                             |
|            | 1        | NOT IDLE          | 1           | PREPARING to SLEEP | The core clock is required until the current transaction is completed and the Block is IDLE. |
|            |          | IDLE              | 0           | SLEEPING           | The block is idle and the core clock can be stopped.                                         |

### 24.8.1 Disabling the SPI Interface Block via the Enable Bit

The enable bit is located in [Section 24.11.1, "SPIAR - SPI Enable Register," on page 432](#). When this bit is cleared the SPI interface is in its lowest power state. The 64.52MHz clock input is gated and the [SPDOUT](#) and [SPCLKOUT](#) pins are set to their inactive state as determined by the configuration bits.

**Note:** The SPI Interface is required to finish the current transaction and enter the Idle state before deasserting the [SPI\\_CLK\\_REQ](#) signal and gating its internal clock source.

### 24.8.2 Asserting the SLEEP\_EN Signal to the SPI Interface Block

When the [SLEEP\\_EN](#) signal is asserted the SPI interface completes the current transaction and then enters the low power state. In the low power state the 64.52MHz clock input is gated, the [SPDOUT](#) and [SPCLKOUT](#) pins are set to their inactive state as determined by the configuration bits, and the [SPI\\_CLK\\_REQ](#) signal is de-asserted.

## 24.9 Operation

The Serial Peripheral Interface (SPI) block is a master SPI block used to communicate with external SPI devices. The SPI master is responsible for generating the SPI clock and is designed to operate in Full Duplex, Half Duplex, and Dual modes of operation. The clock source may be programmed to operate at various clock speeds. The data is transmitted serially via 8-bit transmit and receive shift registers. Communication with SPI peripherals that require transactions of varying lengths can be achieved with multiple 8-bit cycles.

This block has many configuration options: The data may be transmitted and received either MSbit or LSbit first; The SPI Clock Polarity may be either active high or active low; Data may be sampled or presented on either the rising or falling edge of the clock (referred to as the transmit clock phase); and the [SPCLKOUT](#) [SPDOUT](#) frequency may be programmed to select values from 9.52kHz to 64.52MHz. In addition to these many programmable options, this feature has several status bits that may be enabled to notify the host that data is being transmitted or received.

### 24.9.1 Initiating an SPI Transaction

All SPI transactions are initiated by a write to the TX\_DATA register. No read or write operations can be initiated until the Transmit Buffer is Empty, which is indicated by a one in the TXBE status bit.

If the transaction is a write operation, the host writes the TX\_DATA register with the value to be transmitted. Writing the TX\_DATA register causes the TXBE status bit to be cleared, indicating that the value has been registered. If empty, the SPI Core loads this TX\_DATA value into an 8-bit transmit shift register and begins shifting the data out. Loading the value into the shift register causes the TXBE status bit to be asserted, indicating to software that the next byte can be written to the TX\_DATA register.



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If the transaction is a read operation, the host initiates a write to the TX\_DATA register in the same manner as the write operation. Unlike the transmit command, the host must clear the RXBF status bit by reading the RX\_DATA register before writing the TX\_DATA register. This time, the host will be required to poll the RXBF status bit to determine when the value in the RX\_DATA register is valid.

**Note:** If the SPI interface is configured for Half Duplex mode, the host must still write a dummy byte to receive data.

**Note:** Since RX and TX transactions are executed by the same sequence of transactions, data is always shifted into the RX\_DATA register. Therefore, every write operation causes data to be latched into the RX\_DATA register and the RXBF bit is set. This status bit should be cleared before initiating subsequent transactions. The host utilizing this SPI core to transmit SPI Data must discard the unwanted receive bytes.

**Note:** The length and order of data sent to and received from a SPI peripheral varies between peripheral devices. The SPI must be properly configured and software-controlled to communicate with each device and determine whether SPIRD data is valid slave data.

The following diagrams show sample single byte and multi-byte SPI Transactions.

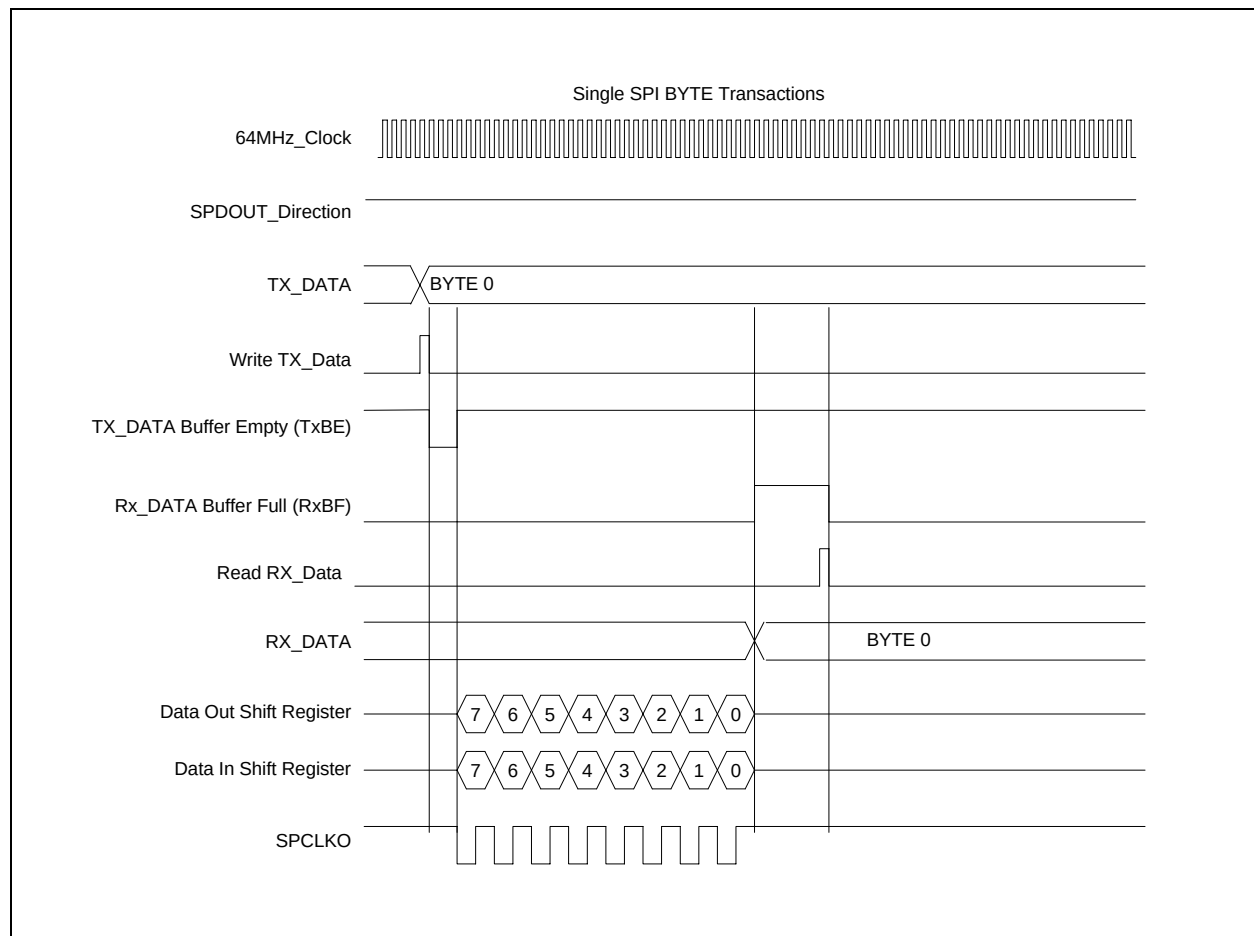


**Figure 24.3 Single Byte SPI Tx/Rx Transactions (Full Duplex Mode)**

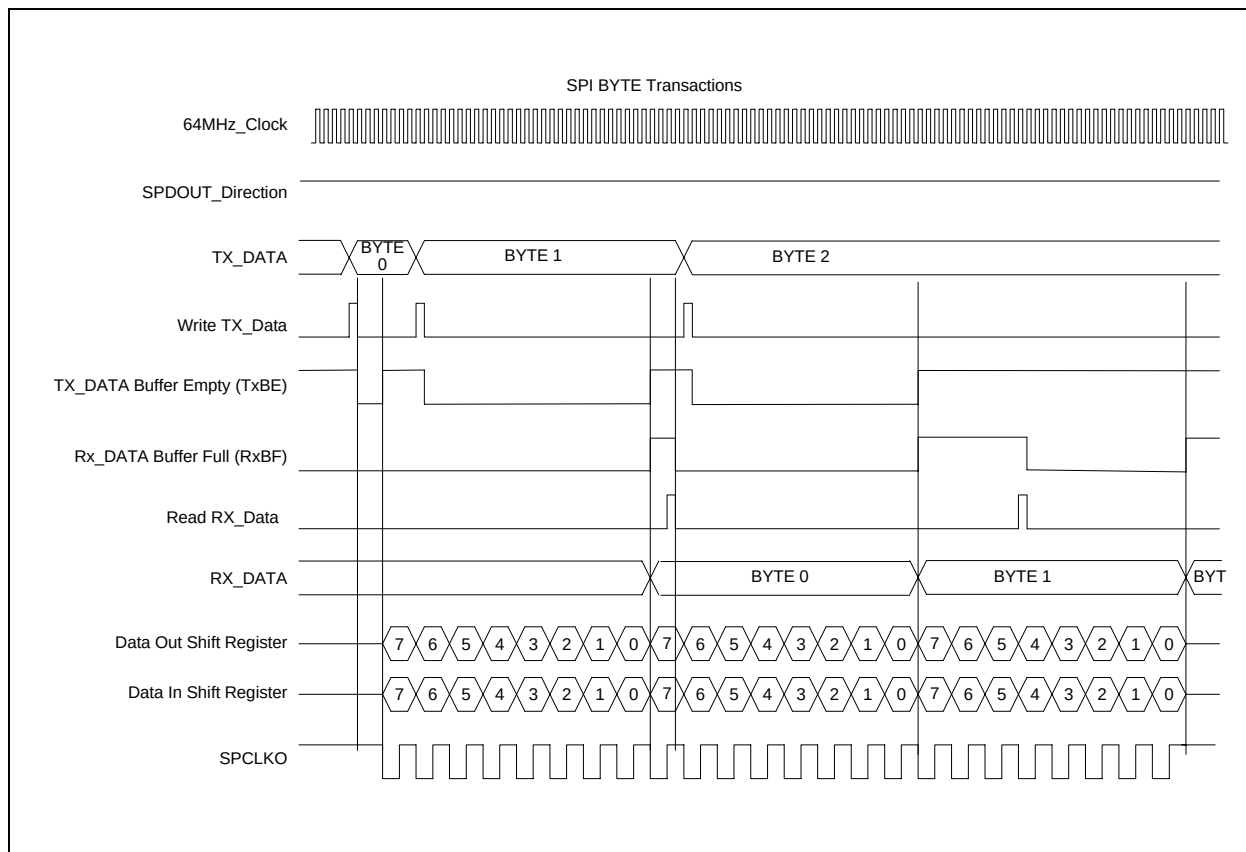


**Figure 24.4 Multi-Byte SPI Tx/Rx Transactions (Full Duplex Mode)**

The data may be configured to be transmitted MSB or LSB first. This is configured by the LSBF bit in the [Section 24.11.2, "SPICR - SPI Control Register," on page 433](#). The transmit data is shifted out on the edge as selected by the TCLKPH bit in the SPICC register. See [Section 24.11.6, "SPICC - SPI Clock Control Register," on page 436](#). All received data can be sampled on a rising or falling SPCLKOUT edge using RCLKPH (see RCLKPH in [Section 24.11.6, "SPICC - SPI Clock Control Register," on page 436](#) for clock controls). This clock setting must be identical to the clocking requirements of the current SPI slave

**Note:** Common peripheral devices require a chip select signal to be asserted during a transaction. Chip selects for SPI devices may be controlled by MEC5035 GPIO pins.

There are three types of transactions that can be implemented for transmitting and receiving the SPI data. They are Full Duplex, Half Duplex, and Dual Mode. These modes are define in [Section 24.9.2, "Types of SPI Transactions," on page 426](#).

## 24.9.2 Types of SPI Transactions

The MEC5035 SPI can be configured to operate in three modes: Full Duplex, Half Duplex, and Dual Mode.

### 24.9.2.1 Full Duplex

In Full Duplex Mode, serial data is transmitted and received simultaneously by the SPI master over the SPDOUT and SPDIN pins. To enable Full Duplex Mode clear [SPDIN Select](#).

When a transaction is completed in the full-duplex mode, the RX\_DATA shift register always contains received data (valid or not) from the last transaction.

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In Half Duplex Mode, serial data is transmitted and received sequentially over a single data line (referred to as the **SPDOUT** pin). To enable Half Duplex Mode set **SPDIN Select** to 01b. The direction of the **SPDOUT** signal is determined by the **BIOEN** bit (See [Section , "BIOEN," on page 433](#)).

- To transmit data in half duplex mode set the **BIOEN** bit before writing the **TX\_DATA** register.
- To receive data in half duplex mode clear the **BIOEN** bit before writing the **TX\_DATA** register with a dummy byte.

**Note:** The Software driver must properly drive the **BIOEN** bit and store received data depending on the transaction format of the specific slave device.

**24.9.2.3 Dual Mode of Operation**

**Note:** The Dual Mode of Operation has been implemented to support selected SPI Flash devices that support the Fast Dual Mode command.

In Dual Mode, serial data is transmitted sequentially from the **SPDOUT** pin and received in by the SPI master from the **SPDOUT** and **SPDIN** pins. This essentially doubles the received data rate. To enable Dual Mode of operation the SPI core must be configured to receive data in path on the **SPDIN1** and **SPDIN2** inputs via **SPDIN Select**. The **BIOEN** bit determines if the SPI core is transmitting or receiving. The setting of this bit determines the direction of the **SPDOUT** signal. The **SPDIN Select** bits are configuration bits that remain static for the duration of a dual read command. The **BIOEN** bit must be toggled to indicate when the SPI core is transmitting and receiving. For a description of the **BIOEN** bit see [BIOEN on page 433](#).

- To transmit data in dual mode set the **BIOEN** bit before writing the **TX\_DATA** register.
- To receive data in dual mode clear the **BIOEN** bit before writing the **TX\_DATA** register with a dummy byte. The even bits (0,2,4,and 6) are received on the **SPDOUT** pin and the odd bits (1,3,5,and 7) are received on the **SPDIN** pin. The hardware assembles these received bits into a single byte and loads them into the **RX\_DATA** register accordingly.

The following diagram illustrates a Dual Fast Read Command that is supported by some SPI Flash devices.

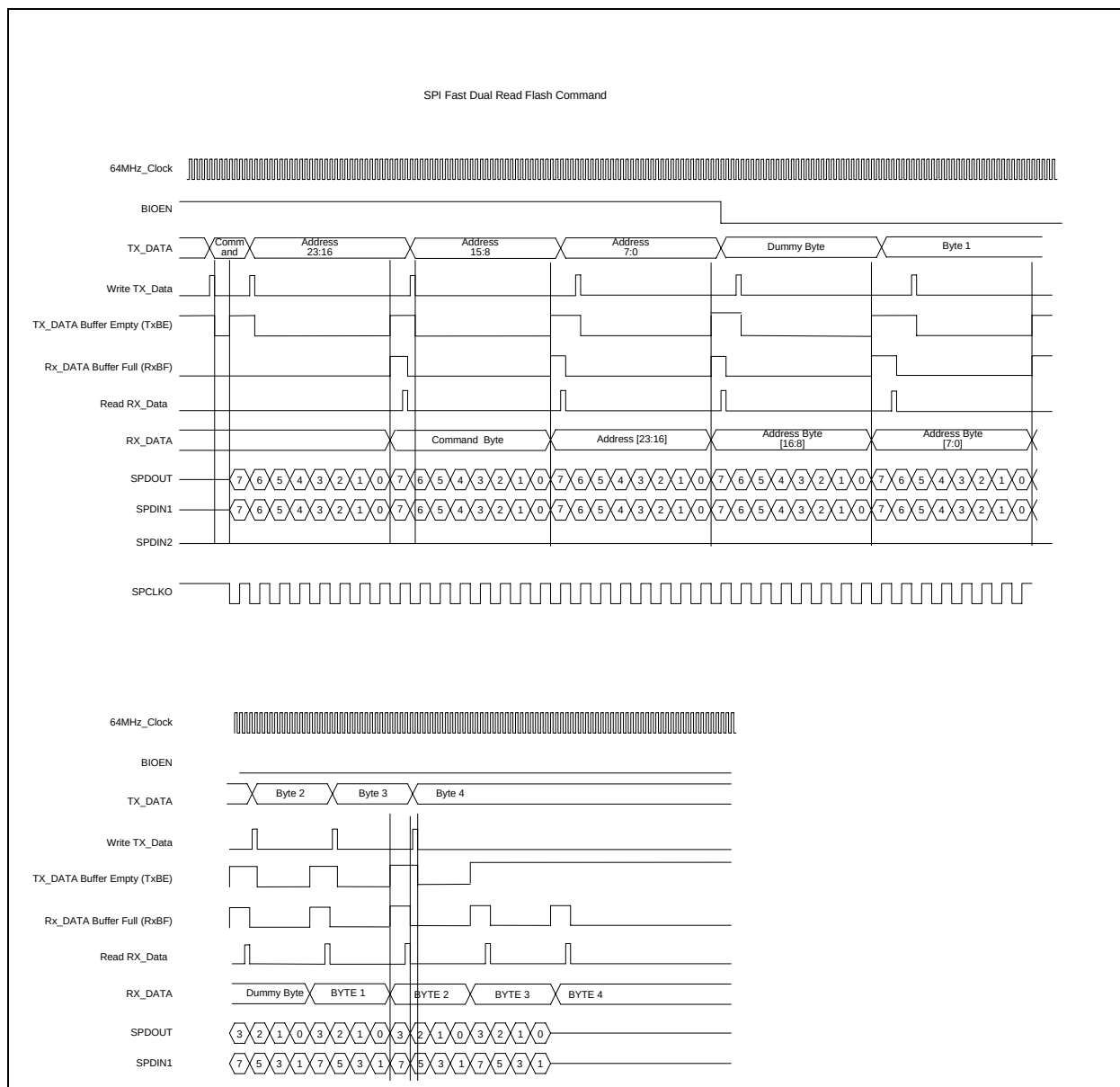


**Figure 24.5 Dual Fast Read Flash Command**

**Note:** When the SPI core is used for flash commands, like the Dual Read command, the host discards the bytes received during the command, address, and dummy byte portions of the transaction.

### 24.9.3 How BIOEN bit controls Direction of SPDOUT Buffer

When the SPI is configured for [Half Duplex](#) mode or Dual Mode the [SPDOUT](#) pin operates as a bi-directional signal. The BIOEN bit is used to determine the direction of the [SPDOUT](#) buffer when a byte is transmitted. Internally, the BIOEN bit is sampled to control the direction of the [SPDOUT](#) buffer when the TX\_DATA value is loaded into the transmit shift register. The direction of the buffer is never changed while a byte is being transmitted.

Since the TX\_DATA register may be written while a byte is being shifted out on the [SPDOUT](#) pin, the BIOEN bit does not directly control the direction of the [SPDOUT](#) buffer. An internal DIRECTION bit,



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which is a latched version of the BIOEN bit determines the direction of the **SPDOUT** buffer. The following list summarizes when the BIOEN bit is sampled.

- The DIRECTION bit is equal to the BIOEN bit when data is not being shifted out (i.e., SPI interface is idle).
- The hardware samples the BIOEN bit when it is shifting out the last bit of a byte to determine if the buffer needs to be turned around for the next byte.
- The BIOEN bit is also sampled any time the value in the TX\_DATA register is loaded into the shift register to be transmitted.

**APPLICATION NOTE:** If a TAR (Turn-around time) is required between transmitting and receiving bytes on the SPDOUT signal, software should allow all the bytes to be transmitted before changing the buffer to an input and then load the TX\_DATA register to begin receiving bytes. This allows the SPI block to operate the same as legacy SMSC SPI devices.

## 24.9.4 Configuring the Clock Generator for an SPI Transaction

The SPI Core generates the **SPCLKOUT** signal to the external SPI device. This clock may be configured for frequencies from 9.52kHz to 64.52MHz. The clock phase and polarity are configurable as well. The following sections define how to program these features.

**USER'S NOTE:** The clock source configuration should not be changed during an SPI transaction.

### 24.9.4.1 Configuring the Frequency of the SPI Clock

The frequency of the **SPCLKOUT** signal is determined by the clock source enabled to the clock generator and the preload value of the clock generator down counter. The clock generator toggles the **SPCLKOUT** output every time the counter underflows, while data is being transmitted. If the preload value is set to 0 the 64.52 MHz clock source bypasses the down counter to directly create the clock generator output.

**Note:** When the SPI interface is in the idle state and data is not being transmitted, the **SPCLKOUT** signal stops in the inactive state as determined by the configuration bits.

The clock source to the down counter is determined by Bit **CLKSRC**. Either the 64.52MHz clock or the 2.0MHz clock enable can be used to decrement the down counter in the clock generator logic.

### 24.9.4.2 Configuring the SPI Mode

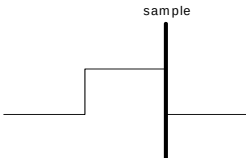
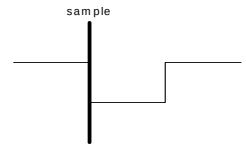
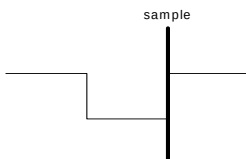
In practice, there are four modes of operation that define when data should be latched. These four modes are the combinations of the **SPCLKOUT** polarity (**CLKPOL**) and phase (**RCLKPH** and **TCLKPH**). Phase is programmable independently for the receive and transmit phases. **CLKPOL**, **RCLKPH** and **TCLKPH** bits are programmable as defined in [Section 24.9.4.3](#) and [Section 24.9.4.4](#) below.

**Table 24.4 SPI Modes**

| SPI MODE | CLKPOL | CLKPH | DEFINITION                           | DIAGRAM |
|----------|--------|-------|--------------------------------------|---------|
| 0        | 0      | 0     | data sampled on rising edge of clock |         |



Table 24.4 SPI Modes

| SPI MODE | CLKPOL | CLKPH | DEFINITION                            | DIAGRAM                                                                             |
|----------|--------|-------|---------------------------------------|-------------------------------------------------------------------------------------|
| 1        | 0      | 1     | data sampled on falling edge of clock |  |
| 2        | 1      | 0     | data sampled on falling edge of clock |  |
| 3        | 1      | 1     | data sampled on rising edge of clock  |  |

#### 24.9.4.3 Configuring the Polarity of the SPI Clock

The output of the clock generator may be inverted to create an active high or active low clock pulse. This is used to determine the inactive state of the [SPCLKOUT](#) signal and is used for determining the first edge for shifting the data. The polarity is selected by Bit [CLKPOL](#) in the [SPI Clock Control Register \(SPICC\)](#).

#### 24.9.4.4 Configuring the Phase of the SPI Clock

The SPI devices need to know when to sample the data, which may be either on the first edge of the clock or on the second edge of the clock. The phase of the clock is selected independently for receiving data and transmitting data. The receive phase is determine by Bit [RCLKPH](#) and the transmit phase is determine by [TCLKPH](#) in the [SPI Clock Control Register \(SPICC\)](#).

#### 24.9.4.5 Limits of SPI configurations

The following limits Modes, clock frequency, & board layout.

**Note 24.2** In the MEC5035, the SPI interface are on has 8ma buffers. The maximum SPCLK pin clock frequency is 16.128MHz for all modes. Limited functionality is available at Although the block can be programmed for higher frequencies, performance is not guaranteed. See Table 24.15 on page 438 and Section 24.9.4.5, "Limits of SPI configurations," on page 430.



Table 24.5

| MASTER (MEC5035)     |                        |                            |                    | SLAVE (NOT MEC5035)     |                    |
|----------------------|------------------------|----------------------------|--------------------|-------------------------|--------------------|
| MAX SPICLK FREQUENCY | Dual Mode of Operation | OUTPUT DATA TRANSITIONS    | INPUT DATA SAMPLED | OUTPUT DATA TRANSITIONS | INPUT DATA SAMPLED |
| 64.52MHz             | Not supported          |                            |                    |                         |                    |
| 32.26MHz             | Not supported          | Pos edge of clk            | Pos edge of clk    | Pos edge of clk         | Either edge of clk |
| 16.13MHz or less     | Supported              | All combinations are valid |                    |                         |                    |

## 24.10 Instance Description

There are one instances of [General Purpose Serial Peripheral Interface \(GP-SPI\)](#) block implemented in the MEC5035.

Each instance of the [General Purpose Serial Peripheral Interface \(GP-SPI\)](#) has its own Logical Device Number, and Base Address as indicated in [Table 24.6](#).

Table 24.6 [General Purpose Serial Peripheral Interface \(GP-SPI\)](#) Base Address Table

| General Purpose Serial Peripheral Interface (GP-SPI) INSTANCE | LDN FROM (Table 7.2 on page 167) | AHB BASE ADDRESS |
|---------------------------------------------------------------|----------------------------------|------------------|
| General Purpose SPI Peripheral                                | 7h                               | F0_1C00h         |

The [Table 24.7](#) is a register summary for one instance of the [General Purpose Serial Peripheral Interface \(GP-SPI\)](#). Each EC address is indicated as an SPB Offset from its AHB base address.

**Table 24.7 General Purpose Serial Peripheral Interface (GP-SPI) Register Summary**

| REGISTER NAME                        | EC INTERFACE |           |         | NOTES |
|--------------------------------------|--------------|-----------|---------|-------|
|                                      | SPB OFFSET   | BYTE LANE | EC TYPE |       |
| SPIAR - SPI Enable Register          | 00h          | 3-0       | R/W     |       |
| SPICR - SPI Control Register         | 04h          | 3-0       | R/W     |       |
| SPISR - SPI Status Register          | 08h          | 3-0       | R       |       |
| SPITD - SPI TX_Data Register         | 0Ch          | 3-0       | R/W     |       |
| SPIRD - SPI RX_Data Register         | 10h          | 3-0       | R       |       |
| SPICC - SPI Clock Control Register   | 14h          | 3-0       | R/W     |       |
| SPICG - SPI Clock Generator Register | 18h          | 3-0       | R/W     |       |
| SPIAR - SPI Enable Register          | 00h          | 3-0       | R/W     |       |

## 24.11 Detailed Register Descriptions

**APPLICATION NOTE:** In the SPI registers some configuration bits are assumed to be static, while others may be updated dynamically by software. The BIOEN and ENABLE bits are considered dynamic bits that can be modified by software at anytime, regardless if a transaction is active or not. These values are latched in hardware, so as to not effect the current operation being performed. All other bits are considered static and cannot be changed by Software while an SPI Transaction is in process.

### 24.11.1 SPIAR - SPI Enable Register

**Table 24.8 SPI Enable Register**

| HOST ADDRESS | n/a      |    |    |    | n/a   |    |    | HOST SIZE           |  |
|--------------|----------|----|----|----|-------|----|----|---------------------|--|
| EC OFFSET    | 00h      |    |    |    | 8-bit |    |    | EC SIZE             |  |
| POWER        | VTR      |    |    |    | 00h   |    |    | nSYS_RST<br>DEFAULT |  |
| BUS          | EC SPB   |    |    |    |       |    |    |                     |  |
| BYTE0 BIT    | D7       | D6 | D5 | D4 | D3    | D2 | D1 | D0                  |  |
| HOST TYPE    | -        | -  | -  | -  | -     | -  | -  | -                   |  |
| EC TYPE      | R        | R  | R  | R  | R     | R  | R  | R/W                 |  |
| BIT NAME     | Reserved |    |    |    |       |    |    | Enable              |  |

**ENABLE**

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0=Disabled. Clocks are gated to conserve power and the **SPDOUT** and **SPCLKOUT** signals are set to their inactive state

1=Enabled. The device is fully operational.

**24.11.2 SPICR - SPI Control Register****Table 24.9 SPI Control Register**

| HOST ADDRESS | n/a      |    |    | 8-bit      |              |     | HOST SIZE           |      |
|--------------|----------|----|----|------------|--------------|-----|---------------------|------|
| EC OFFSET    | 04h      |    |    | 8-bit      |              |     | EC SIZE             |      |
| POWER        | VTR      |    |    | 02h        |              |     | nSYS_RST<br>DEFAULT |      |
| BUS          | EC SPB   |    |    |            |              |     |                     |      |
| BYTE0 BIT    | D7       | D6 | D5 | D4         | D3           | D2  | D1                  | D0   |
| HOST TYPE    | -        | -  | -  | -          | -            | -   | -                   | -    |
| EC TYPE      | R        | R  | R  | R/W        | R/W          | R/W | R/W                 | R/W  |
| BIT NAME     | Reserved |    |    | Soft Reset | SPDIN Select |     | BIOEN               | LSBF |

**LSBF**

Least Significant Bit First control.

0= The data is transferred in MSB-first order. (default)

1= The data is transferred in LSB-first order.

**BIOEN**

Bidirectional Output Enable control. When the SPI is configured for **Half Duplex** mode or Dual Mode the **SPDOUT** pin operates as a bi-directional signal. The BIOEN bit is used by the internal DIRECTION bit to control the direction of the **SPDOUT** buffers. The direction of the buffer is never changed while a byte is being transmitted.

0=The **SPDOUT\_Direction** signal configures the **SPDOUT** signal as an input.

1=The **SPDOUT\_Direction** signal configures the **SPDOUT** signal as an output. (default)

**Note:** If the SPI MODE bit is configured for Full Duplex mode the BIOEN bit must be set to '1' to configure the **SPDOUT** signal as an output.

**APPLICATION NOTE:** Although the design supports back-to-back transmissions even when the direction of the buffer is changed, it is the software's responsibility to avoid collisions on the **SPDOUT** signal. The design has been implemented to support a 0 second (max) turn-around (TAR) time. If TAR greater than zero is required, the software must wait for the transmission in one direction to complete before writing the TX\_DATA register to start sending/receiving in the opposite direction.

**SPDIN SELECT**

The SPDIN Select which SPI input signals are enabled when the BIOEN bit is configured as an input.

00= SPDIN1 only

//Select this option for Full Duplex (default)

01=SPDIN2 only //Select this option for Half Duplex  
1x=SPDIN1 and SPDIN2 //Select this option for Dual Mode

#### SOFT RESET

Soft Reset is a self-clearing bit. Writing zero to this bit has no effect. Writing a one to this bit resets the entire SPI Interface, including all counters and registers back to their initial state (i.e., the same as a [nSYS\\_RST](#)).

### 24.11.3 SPIR - SPI Status Register

Table 24.10 SPI Status Register

| HOST ADDRESS | n/a      |    |    |    | 8-bit |    | HOST SIZE           |      |
|--------------|----------|----|----|----|-------|----|---------------------|------|
| EC OFFSET    | 08h      |    |    |    | 8-bit |    | EC SIZE             |      |
| POWER        | VTR      |    |    |    | 01h   |    | nSYS_RST<br>DEFAULT |      |
| BUS          | EC SPB   |    |    |    |       |    |                     |      |
| BYTE0 BIT    | D7       | D6 | D5 | D4 | D3    | D2 | D1                  | D0   |
| HOST TYPE    | -        | -  | -  | -  | -     | -  | -                   | -    |
| EC TYPE      | R        | R  | R  | R  | R     | R  | R                   | R    |
| BIT NAME     | Reserved |    |    |    |       |    | RxBF                | TxBE |

#### TXBE

Transmit Data Buffer Empty status. This bit is a read-only bit used to indicate that the Tx\_Data buffer is empty. Writing the Tx\_DATA Buffer clears this bit. This signal may be used to generate an interrupt to the EC, if not masked.

#### RXBF

Receive Data Buffer Full status. This bit is a read-only bit used to indicate when the Rx\_Data buffer is full. Reading the Rx\_DATA Buffer clears this bit. This signal may be used to generate an interrupt to the EC, if not masked.



## 24.11.4 SPITD - SPI TX\_Data Register

**Table 24.11 SPI TX Data Register (SPITD)**

|              |              |     |     |       |     |     |                     |     |
|--------------|--------------|-----|-----|-------|-----|-----|---------------------|-----|
| HOST ADDRESS | n/a          |     |     | 8-bit |     |     | HOST SIZE           |     |
| EC OFFSET    | 0Ch          |     |     | 8-bit |     |     | EC SIZE             |     |
| POWER        | VTR          |     |     | 00h   |     |     | nSYS_RST<br>DEFAULT |     |
| BUS          | EC SPB       |     |     |       |     |     |                     |     |
| BYTE0 BIT    | D7           | D6  | D5  | D4    | D3  | D2  | D1                  | D0  |
| HOST TYPE    | -            | -   | -   | -     | -   | -   | -                   | -   |
| EC TYPE      | R/W          | R/W | R/W | R/W   | R/W | R/W | R/W                 | R/W |
| BIT NAME     | TX_Data[7:0] |     |     |       |     |     |                     |     |

### TX\_DATA[7:0]

A write to this register with the TXFE bit asserted '1' initiates an SPI transaction. If the Transmit Shift Register is empty the byte written to this register will be loaded into the shift register and the TXFE flag will be asserted. This indicates that the next byte can be written into the TX\_DATA register. This byte will remain in the TX\_DATA register until the SPI core has finished shifting out the previous byte. Once the shift register is empty, the hardware will load the pending byte into the shift register and once again assert the TXFE bit.

**Note:** The TX\_DATA register must not be written when the TXBE bit is zero. Writing this register may overwrite the transmit data before it is loaded into the shift register.

Reading the TX\_DATA register will return the last value written to this register.

## 24.11.5 SPIRD - SPI RX\_Data Register

**Table 24.12 SPI RX Data Register (SPIRD)**

| HOST ADDRESS | n/a          |    |    |    | 8-bit |    |    | HOST SIZE           |  |
|--------------|--------------|----|----|----|-------|----|----|---------------------|--|
| EC OFFSET    | 10h          |    |    |    | 8-bit |    |    | EC SIZE             |  |
| POWER        | VTR          |    |    |    | 00h   |    |    | nSYS_RST<br>DEFAULT |  |
| BUS          | EC SPB       |    |    |    |       |    |    |                     |  |
| BYTE0 BIT    | D7           | D6 | D5 | D4 | D3    | D2 | D1 | D0                  |  |
| HOST TYPE    | -            | -  | -  | -  | -     | -  | -  | -                   |  |
| EC TYPE      | R            | R  | R  | R  | R     | R  | R  | R                   |  |
| BIT NAME     | RX_Data[7:0] |    |    |    |       |    |    |                     |  |

### RX\_DATA[7:0]

This register is used to read the value returned by the external SPI device. At the end of a byte transfer the RX\_DATA register contains serial input data (valid or not) from the last transaction and the RXBF bit is set to one. This status bit indicates that the RX\_DATA register has been loaded with a the serial input data. The RX\_DATA register should not be read before the RXBF bit is set.

**Note:** The RX\_DATA register must be read, clearing the RXBF status bit before writing the TX\_DATA register. The data in the receive shift register is only loaded into the RX\_DATA register when this bit is cleared. If a data byte is pending in the receive shift register the value will be loaded immediately into the RX\_DATA register and the RXBF status flag will be asserted. Software should read the RX\_DATA register twice before starting a new transaction to make sure the RX\_DATA buffer and shift register are both empty.

## 24.11.6 SPICC - SPI Clock Control Register

**Table 24.13 SPI Clock Control Register (SPICC)**

| HOST ADDRESS | n/a      |    |    | 8-bit  |          |        | HOST SIZE        |        |
|--------------|----------|----|----|--------|----------|--------|------------------|--------|
| EC OFFSET    | 14h      |    |    | 8-bit  |          |        | EC SIZE          |        |
| POWER        | VTR      |    |    | 02h    |          |        | nSYS_RST DEFAULT |        |
| BUS          | EC SPB   |    |    |        |          |        |                  |        |
| BYTE0 BIT    | D7       | D6 | D5 | D4     | D3       | D2     | D1               | D0     |
| HOST TYPE    | -        | -  | -  | -      | -        | -      | -                | -      |
| EC TYPE      | R        | R  | R  | R/W    | R        | R/W    | R/W              | R/W    |
| BIT NAME     | Reserved |    |    | CLKSRC | Reserved | CLKPOL | RCLKPH           | TCLKPH |

**Product Customer Specification-ODM****TCLKPH**

The TCLKPH bit determines the Transmit Clock Phase, the SPCLK edge on which the master will clock data out.

0= Valid data is clocked out on the SPDOOUT signal prior to the first SPCLKOUT edge. The slave device should sample this data on the first and following odd SPCLKOUT edges (i.e., sample data on rising edge). (default)

1= Valid data is clocked out on the first SPCLKOUT edge on SPDOOUT signal. The slave device should sample this data on the second and following even SPCLKOUT edges (i.e., sample data on falling edge).

**Note:** This functionality is independent of the polarity of SPCLK. See [Section 34.9, "Serial Peripheral Interface \(SPI\) Timings," on page 534](#) for timing diagrams.

**RCLKPH**

The RCLKPH bit determines the Receive Clock Phase, the SPCLKOUT edge on which the master will sample data.

0= Valid data is expected on the SPDIN signal on the first SPCLKOUT edge. This data is sampled on the first and following odd SPCLKOUT edges (i.e., sample data on rising edge).

1= Valid data on SPDIN signal is expected after the first SPCLKOUT edge. This data is sampled on the second and following even SPCLKOUT edges (i.e., sample data on falling edge). (default)

**Note:** This functionality is independent of the polarity of SPCLKOUT. See [Section 34.9, "Serial Peripheral Interface \(SPI\) Timings," on page 534](#) for timing diagrams.

**CLKPOL**

This bit controls the polarity of the SPI clock.

0= The SPCLKOUT is low when the interface is idle and the first clock edge is a rising edge. (default)

1= The SPCLKOUT signal is high when the interface is idle and the first clock edge is a falling edge

**CLKSRC**

This bit controls the clock source to SPI Clock Generator

0=The clock source to the SPI Clock Generator 6-bit down counter is 64.52MHz clock enable (default)

1=The clock source to the SPI Clock Generator 6-bit down counter is 2MHz clock enable

**Note:** The CLKSRC bit should not be changed during a SPI transaction.



## 24.11.7 SPICG - SPI Clock Generator Register

**Table 24.14 SPI Clock Generator Register (SPICG)**

|              |          |    |              |       |     |     |                     |     |
|--------------|----------|----|--------------|-------|-----|-----|---------------------|-----|
| HOST ADDRESS | n/a      |    |              | 8-bit |     |     | HOST SIZE           |     |
| EC OFFSET    | 18h      |    |              | 8-bit |     |     | EC SIZE             |     |
| POWER        | VTR      |    |              | 02h   |     |     | nSYS_RST<br>DEFAULT |     |
| BUS          | EC SPB   |    |              |       |     |     |                     |     |
| BYTE0 BIT    | D7       | D6 | D5           | D4    | D3  | D2  | D1                  | D0  |
| HOST TYPE    | -        | -  | -            | -     | -   | -   | -                   | -   |
| EC TYPE      | R        | R  | R/W          | R/W   | R/W | R/W | R/W                 | R/W |
| BIT NAME     | Reserved |    | Preload[5:0] |       |     |     |                     |     |

### PRELOAD[5:0]

The SPI Clock Generator Preload value. The **SPCLKOUT** signal is a clock output with a 50% duty cycle. The signal is generated from a 6-bit down counter that toggles the **SPCLKOUT** pin every time it reaches zero and reloads the counter. This counter is decremented at the rate of the input clock enable, which is either the 64.52MHz clock enable or the 2MHz clock enable.

$$SPCLKO\_FREQ = \left( \left( \frac{1}{2} \times \text{CLOCK\_ENABLE\_FREQ} \right) / \text{PRELOAD} \right)$$

The PRELOAD field contains the preload value for the counter that determines the resulting frequency. The following table outlines the ranges of frequencies possible. Notice that a preload value of zero effectively bypasses the counter and maps the 64.52MHz clock onto the **SPCLKOUT** signal.

**Table 24.15 SPCLKOUT Frequencies**

| CLOCK ENABLE<br>FREQUENCY | PRELOAD | SPCLKOUT Frequency | NOTES                        |
|---------------------------|---------|--------------------|------------------------------|
| Don't Care                | 0       | 64.52MHz           | Max Frequency<br>(Note 24.3) |
| 64.52MHz                  | 1       | 32.26MHz           |                              |
| 64.52MHz                  | 2       | 16.13MHz           | Default Frequency            |
| 64.52MHz                  | 3       | 10.75MHz           |                              |
| 64.52MHz                  | 63      | 0.51MHz            |                              |
| 2.016MHz                  | 0       | 2.016MHz           |                              |
| 2.016MHz                  | 1       | 1.008MHz           |                              |



Table 24.15 SPCLKOUT Frequencies

| CLOCK ENABLE FREQUENCY | PRELOAD | SPCLKOUT Frequency | NOTES         |
|------------------------|---------|--------------------|---------------|
| 2.016MHz               | 2       | 504kHz             |               |
| 2.016MHz               | 3       | 336kHz             |               |
| 2.016MHz               | 63      | 16kHz              | Min Frequency |

**Note 24.3** When the Preload value is programmed to zero the 64.52MHz Clock Source is directly mapped to the SPCLKOUT signal. Since the 64.52MHz signal is a 50% duty cycle it may be directly used as an SPCLKOUT frequency.

**Note 24.4** In the MEC5035, the SPI interface are on has 8ma buffers. The maximum SPCLK pin clock frequency is 16.128MHz for all modes. Limited functionality is available at Although the block can be programmed for higher frequencies, performance is not guaranteed. See Table 24.15 on page 438 and Section 24.9.4.5, "Limits of SPI configurations," on page 430.

## 24.12 SPI Examples

### 24.12.1 Full Duplex Mode Transfer Examples

#### 24.12.1.1 Read Only

The slave device used in this example is a MAXIM MAX1080 10 bit, 8 channel ADC:

- The SPI block is activated by setting the enable bit in [SPIAR - SPI Enable Register](#)
- The SPIMODE bit is de-asserted '0' to enable the SPI interface in Full Duplex mode.
- The CLKPOL and TCLKPH bits are de-asserted '0', and RCLKPH is asserted '1' to match the clocking requirements of the slave device.
- The LSBF bit is de-asserted '0' to indicate that the slave expects data in MSB-first order.
- Assert #CS using a GPIO pin.
- Write a valid command word (as specified by the slave device) to the [SPITD - SPI TX\\_Data Register](#) with TXFE asserted '1'. The SPI master automatically clears the TXFE bit indicating the byte has been put in the TX buffer. If the shift register is empty the TX\_DATA byte is loaded into the shift register and the SPI master reasserts the TXFE bit. Once the data is in the shift register the SPI master begins shifting the data value onto the SPDOUT pin and drives the SPCLK pin. Data on the SPDIN pin is also sampled on each clock.
- Once the TXFE bit is asserted the SPI Master is ready to receive its next byte. Before writing the next TX\_DATA value, software must clear the RXBF status bit by reading the [SPIRD - SPI RX\\_Data Register](#).
- A dummy 8 bit data value (any value) is written to the TX\_DATA register. The SPI master automatically clears the TXFE bit, but does not begin shifting the dummy data value onto the SPDOUT pin. This byte will remain in the TX\_DATA register until the TX shift register is empty.
- **After 8 SPCLKOUT pulses from the first transmit bytes:**  
The first SPI cycle is complete, RXBF bit is asserted '1', and the SPINT interrupt is asserted, if enabled. (See [Section 24.7, "SPI Interrupts"](#)). The data now contained in [SPIRD - SPI RX\\_Data Register](#) is invalid since the last cycle was initiated solely to transmit command data to the slave. This particular slave device drives '0' on the SPDIN pin to the master while it is accepting command data. This SPIRD data is ignored.  
Once the first SPI cycle is completed, the SPI master takes the pending data in the TX\_DATA register and loads it into the TX shift register. Loading the shift register automatically asserts the TXFE bit, begins shifting the dummy data value onto the SPDOUT pin, and drives the SPCLK pin. Data on the SPDIN pin is also sampled on each clock.

- Once the TXFE bit is asserted the SPI Master is ready to receive its next byte. Before writing the next TX\_DATA value, software must clear the RXBF status bit by reading the [SPIRD - SPI RX\\_Data Register](#).
- The final SPI cycle is initiated when another dummy 8 bit data value (any value) is written to the TX\_DATA register. Note that this value may be another dummy value or it can be a new 8 bit command to be sent to the ADC. The new command will be transmitted while the final data from the last command is received simultaneously. This overlap allows ADC data to be read every 16 SPCLK cycles after the initial 24 clock cycle. The SPI master automatically clears the TXFE bit, but does not begin shifting the dummy data value onto the SPDOUT pin. This byte will remain in the TX\_DATA register until the TX shift register is empty.
- **After 8 SPCLKOUT pulses, the second SPI cycle is complete:**  
The first SPI cycle is complete, RXBF bit is asserted '1', and the SPINT interrupt is asserted, if enabled. (See [Section 24.7, "SPI Interrupts"](#)). The data now contained in [SPIRD - SPI RX\\_Data Register](#) is the first half of a valid 16 bit ADC value. SPIRD is read and stored.  
Once the second SPI cycle is completed, the SPI master takes the pending data in the TX\_DATA register and loads it into the TX shift register. Loading the shift register automatically asserts the TXFE bit, begins shifting the data value onto the SPDOUT pin, and drives the SPCLK pin. Data on the SPDIN pin is also sampled on each clock.
- After 8 [SPCLKOUT](#) pulses, the final SPI cycle is complete, TXBF is asserted '1', and the SPINT interrupt is asserted (if enabled). The data now contained in [SPIRD - SPI RX\\_Data Register](#) is the second half of a valid 16 bit ADC value. SPIRD is read and stored.
- If a command was overlapped with the received data in the final cycle, #CS should remain asserted and the SPI master will initiate another SPI cycle. If no new command was sent, #CS is released and the SPI is idle.

#### 24.12.1.2 Read/Write

The slave device used in this example is a Fairchild NS25C640 FM25C640 64K Bit Serial EEPROM. The following sub-sections describe the read and write sequences.

##### Read

- The SPI block is activated by setting the enable bit in [SPIAR - SPI Enable Register](#)
- The SPIMODE bit is de-asserted '0' to enable the SPI interface in Full Duplex mode.
- The CLKPOL, TCLKPH and RCLKPH bits are de-asserted '0' to match the clocking requirements of the slave device.
- The LSBF bit is de-asserted '0' to indicate that the slave expects data in MSB-first order.
- Assert CS# low using a GPIO pin.
- Write a valid command word (as specified by the slave device) to the [SPITD - SPI TX\\_Data Register](#) with TXFE asserted '1'. The SPI master automatically clears the TXFE bit indicating the byte has been put in the TX buffer. If the shift register is empty the TX\_DATA byte is loaded into the shift register and the SPI master reasserts the TXFE bit. Once the data is in the shift register the SPI master begins shifting the data value onto the SPDOUT pin and drives the [SPCLKOUT](#) pin. Data on the SPDIN pin is also sampled on each clock.
- Once the TXFE bit is asserted the SPI Master is ready to receive its next byte. Before writing the next TX\_DATA value, software must clear the RXBF status bit by reading the [SPIRD - SPI RX\\_Data Register](#).
- Next, EEPROM address A15-A8 is written to the TX\_DATA register. The SPI master automatically clears the TXFE bit, but does not begin shifting the dummy data value onto the SPDOUT pin. This byte will remain in the TX\_DATA register until the TX shift register is empty.
- **After 8 SPCLKOUT pulses from the first transmit byte (Command Byte transmitted):**  
The first SPI cycle is complete, RXBF bit is asserted '1', and the SPINT interrupt is asserted, if enabled. (See [Section 24.7, "SPI Interrupts"](#)). The data now contained in [SPIRD - SPI RX\\_Data Register](#) is invalid since the last cycle was initiated solely to transmit command data to the slave.

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This particular slave device tri-states the SPDIN pin to the master while it is accepting command data. This SPIRD data is ignored.

**USER'S NOTE:** External pull-up or pull-down is required on the SPDIN pin if it is tri-stated by the slave device.

Once the first SPI cycle is completed, the SPI master takes the pending data in the TX\_DATA register (EEPROM address A15-A8) and loads it into the TX shift register. Loading the shift register automatically asserts the TXFE bit, begins shifting the dummy data value onto the SPDOUT pin, and drives the **SPCLKOUT** pin. Data on the SPDIN pin is also sampled on each clock. Note: The particular slave device ignores address A15-A13.

- Once the TXFE bit is asserted the SPI Master is ready to receive its next byte. Before writing the next TX\_DATA value, software must clear the RXBF status bit by reading the [SPIRD - SPI RX\\_Data Register](#).
- Next, EEPROM address A7-A0 is written to the TX\_DATA register. The SPI master automatically clears the TXFE bit, but does not begin shifting this data value onto the SPDOUT pin. This byte will remain in the TX\_DATA register until the TX shift register is empty.
- **After 8 SPCLKOUT pulses from the second transmit byte (Address Byte (MSB) transmitted):**  
EEPROM address A15-A8 has been transmitted to the slave completing the second SPI cycle. Once again, the RXBF bit is asserted '1' and the SPINT interrupt is asserted, if enabled. (See [Section 24.7, "SPI Interrupts"](#)). The data now contained in [SPIRD - SPI RX\\_Data Register](#) is invalid since the last cycle was initiated solely to transmit address data to the slave.  
Once the second SPI cycle is completed, the SPI master takes the pending data in the TX\_DATA register (EEPROM address A7-A0) and loads it into the TX shift register. Loading the shift register automatically asserts the TXFE bit, begins shifting the dummy data value onto the SPDOUT pin, and drives the SPCLK pin. Data on the SPDIN pin is also sampled on each clock.
- Once the TXFE bit is asserted the SPI Master is ready to receive its next byte. Before writing the next TX\_DATA value, software must clear the RXBF status bit by reading the [SPIRD - SPI RX\\_Data Register](#).
- Next, a dummy byte is written to the TX\_DATA register. The SPI master automatically clears the TXFE bit, but does not begin shifting this data value onto the SPDOUT pin. This byte will remain in the TX\_DATA register until the TX shift register is empty.
- **After 8 SPCLKOUT pulses, the third SPI cycle is complete (Address Byte (LSB) transmitted):**  
EEPROM address A7-A0 has been transmitted to the slave completing the third SPI cycle. Once again, the RXBF bit is asserted '1' and the SPINT interrupt is asserted, if enabled. (See [Section 24.7, "SPI Interrupts"](#)). The data now contained in [SPIRD - SPI RX\\_Data Register](#) is invalid since the last cycle was initiated solely to transmit address data to the slave.  
Once the third SPI cycle is completed, the SPI master takes the pending data in the TX\_DATA register (dummy byte) and loads it into the TX shift register. Loading the shift register automatically asserts the TXFE bit, begins shifting the dummy data value onto the SPDOUT pin, and drives the SPCLK pin. Data on the SPDIN pin is also sampled on each clock.
- Once the TXFE bit is asserted the SPI Master is ready to receive its next byte. Before writing the next TX\_DATA value, software must clear the RXBF status bit by reading the [SPIRD - SPI RX\\_Data Register](#).
- If only one receive byte is required, the host would not write any more value to the TX\_DATA register until this transaction completes. If more than one byte of data is to be received, another dummy byte would be written to the TX\_DATA register (one dummy byte per receive byte is required). The SPI master automatically clears the TXFE bit when the TX\_DATA register is written, but does not begin shifting this data value onto the SPDOUT pin. This byte will remain in the TX\_DATA register until the TX shift register is empty.
- **After 8 SPCLKOUT pulses, the fourth SPI cycle is complete (First Data Byte received):**  
The dummy byte has been transmitted to the slave completing the fourth SPI cycle. Once again, the RXBF bit is asserted '1' and the SPINT interrupt is asserted, if enabled. (See [Section 24.7, "SPI Interrupts"](#)). Unlike the command and address phases, the data now contained in [SPIRD - SPI RX\\_Data Register](#) is the 8-bit EEPROM data since the last cycle was initiated to receive data from the slave.

Once the fourth SPI cycle is completed, the SPI master takes the pending data in the TX\_DATA register (if any) and loads it into the TX shift register. This process will be repeated until all the desired data is received.

- The host software will read and store the EEPROM data value in [SPIRD - SPI RX\\_Data Register](#).
- If no more data needs to be received by the master, CS# is released and the SPI is idle. Otherwise, master continues reading the data by writing a dummy value to the TX\_DATA register after every 8 [SPCLKOUT](#) cycles.

#### Write

- The SPI block is activated by setting the enable bit in [SPIAR - SPI Enable Register](#)
- The SPIMODE bit is de-asserted '0' to enable the SPI interface in Full Duplex mode.
- The CLKPOL, TCLKPH and RCLKPH bits are de-asserted '0' to match the clocking requirements of the slave device.
- The LSBF bit is de-asserted '0' to indicate that the slave expects data in MSB-first order.
- Assert WR# high using a GPIO pin.
- Assert CS# low using a GPIO pin.
- Write a valid command word (as specified by the slave device) to the [SPITD - SPI TX\\_Data Register](#) with TXFE asserted '1'. The SPI master automatically clears the TXFE bit indicating the byte has been put in the TX buffer. If the shift register is empty the TX\_DATA byte is loaded into the shift register and the SPI master reasserts the TXFE bit. Once the data is in the shift register the SPI master begins shifting the data value onto the SPDOUT pin and drives the [SPCLKOUT](#) pin. Data on the SPDIN pin is also sampled on each clock.
- Once the TXFE bit is asserted the SPI Master is ready to receive its next byte. Before writing the next TX\_DATA value, software must clear the RXBF status bit by reading the [SPIRD - SPI RX\\_Data Register](#).
- Next, EEPROM address A15-A8 is written to the TX\_DATA register. The SPI master automatically clears the TXFE bit, but does not begin shifting the dummy data value onto the SPDOUT pin. This byte will remain in the TX\_DATA register until the TX shift register is empty.
- **After 8 [SPCLKOUT](#) pulses from the first transmit byte (Command Byte transmitted):**  
The first SPI cycle is complete, RXBF bit is asserted '1', and the SPINT interrupt is asserted, if enabled. (See [Section 24.7, "SPI Interrupts"](#)). The data now contained in [SPIRD - SPI RX\\_Data Register](#) is invalid since the last cycle was initiated solely to transmit command data to the slave. This particular slave device tri-states the SPDIN pin to the master while it is accepting command data. This SPIRD data is ignored.

**USER'S NOTE:** External pull-up or pull-down is required on the SPDIN pin if it is tri-stated by the slave device.

Once the first SPI cycle is completed, the SPI master takes the pending data in the TX\_DATA register (EEPROM address A15-A8) and loads it into the TX shift register. Loading the shift register automatically asserts the TXFE bit, begins shifting the dummy data value onto the SPDOUT pin, and drives the [SPCLKOUT](#) pin. Data on the SPDIN pin is also sampled on each clock. Note: The particular slave device ignores address A15-A13.

- Once the TXFE bit is asserted the SPI Master is ready to receive its next byte. Before writing the next TX\_DATA value, software must clear the RXBF status bit by reading the [SPIRD - SPI RX\\_Data Register](#).
- Next, EEPROM address A7-A0 is written to the TX\_DATA register. The SPI master automatically clears the TXFE bit, but does not begin shifting this data value onto the SPDOUT pin. This byte will remain in the TX\_DATA register until the TX shift register is empty.
- **After 8 [SPCLKOUT](#) pulses from the second transmit byte (Address Byte (MSB) transmitted):**  
EEPROM address A15-A8 has been transmitted to the slave completing the second SPI cycle. Once again, the RXBF bit is asserted '1' and the SPINT interrupt is asserted, if enabled. (See [Section 24.7, "SPI Interrupts"](#)). The data now contained in [SPIRD - SPI RX\\_Data Register](#) is invalid since the last cycle was initiated solely to transmit address data to the slave.



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Once the second SPI cycle is completed, the SPI master takes the pending data in the TX\_DATA register (EEPROM address A7-A0) and loads it into the TX shift register. Loading the shift register automatically asserts the TXFE bit, begins shifting the dummy data value onto the SPDOUT pin, and drives the SPCLK pin. Data on the SPDIN pin is also sampled on each clock.

- Once the TXFE bit is asserted the SPI Master is ready to receive its next byte. Before writing the next TX\_DATA value, software must clear the RXBF status bit by reading the [SPIRD - SPI RX\\_Data Register](#).
- Next, a data byte (D7:D0) is written to the TX\_DATA register. The SPI master automatically clears the TXFE bit, but does not begin shifting this data value onto the SPDOUT pin. This byte will remain in the TX\_DATA register until the TX shift register is empty.
- **After 8 SPCLKOUT pulses, the third SPI cycle is complete (Address Byte (LSB) transmitted):**  
EEPROM address A7-A0 has been transmitted to the slave completing the third SPI cycle. Once again, the RXBF bit is asserted '1' and the SPINT interrupt is asserted, if enabled. (See [Section 24.7, "SPI Interrupts"](#)). The data now contained in [SPIRD - SPI RX\\_Data Register](#) is invalid since the last cycle was initiated solely to transmit address data to the slave.  
Once the third SPI cycle is completed, the SPI master takes the pending data in the TX\_DATA register (data byte D7:D0) and loads it into the TX shift register. Loading the shift register automatically asserts the TXFE bit, begins shifting the dummy data value onto the SPDOUT pin, and drives the SPCLK pin. Data on the SPDIN pin is also sampled on each clock.
- Once the TXFE bit is asserted the SPI Master is ready to receive its next byte. Before writing the next TX\_DATA value, software must clear the RXBF status bit by reading the [SPIRD - SPI RX\\_Data Register](#).
- If only one data byte is to be written, the host would not write any more values to the TX\_DATA register until this transaction completes. If more than one byte of data is to be written, another data byte would be written to the TX\_DATA register. The SPI master automatically clears the TXFE bit when the TX\_DATA register is written, but does not begin shifting this data value onto the SPDOUT pin. This byte will remain in the TX\_DATA register until the TX shift register is empty.
- **After 8 SPCLKOUT pulses, the fourth SPI cycle is complete (First Data Byte transmitted):**  
The data byte has been transmitted to the slave completing the fourth SPI cycle. Once again, the RXBF bit is asserted '1' and the SPINT interrupt is asserted, if enabled. (See [Section 24.7, "SPI Interrupts"](#)). Like the command and address phases, the data now contained in [SPIRD - SPI RX\\_Data Register](#) is invalid since the last cycle was initiated to transmit data to the slave.  
Once the fourth SPI cycle is completed, the SPI master takes the pending data in the TX\_DATA register (if any) and loads it into the TX shift register. This process will be repeated until all the desired data is transmitted.
- If no more data needs to be transmitted by the master, CS# and WR# are released and the SPI is idle.

### 24.12.2 Half Duplex (Bidirectional Mode) Transfer Example

The slave device used in this example is a National LM74 12 bit (plus sign) temperature sensor.

- The SPI block is activated by setting the enable bit in [SPIAR - SPI Enable Register](#)
- The SPIMODE bit is asserted '1' to enable the SPI interface in Half Duplex mode.
- The CLKPOL, TCLKPH and RCLKPH bits are de-asserted '0' to match the clocking requirements of the slave device.
- The LSBF bit is de-asserted '0' to indicate that the slave expects data in MSB-first order.
- BIOEN is asserted '0' to indicate that the first data in the transaction is to be received from the slave.
- Assert #CS using a GPIO pin.

//Receive 16-bit Temperature Reading

- Write a dummy command byte (as specified by the slave device) to the [SPITD - SPI TX\\_Data Register](#) with TXFE asserted '1'. The SPI master automatically clears the TXFE bit indicating the



byte has been put in the TX buffer. If the shift register is empty the TX\_DATA byte is loaded into the shift register and the SPI master reasserts the TXFE bit. Once the data is in the shift register the SPI master begins shifting the data value onto the SPDOUT pin and drives the **SPCLKOUT** pin. This data is lost because the output buffer is disabled. Data on the SPDIN pin is sampled on each clock.

- Once the TXFE bit is asserted the SPI Master is ready to receive its next byte. Before writing the next TX\_DATA value, software must clear the RXBF status bit by reading the **SPIRD - SPI RX\_Data Register**.
- Next, another dummy byte is written to the TX\_DATA register. The SPI master automatically clears the TXFE bit, but does not begin shifting the dummy data value onto the SPDOUT pin. This byte will remain in the TX\_DATA register until the TX shift register is empty.
- **After 8 SPCLKOUT pulses from the first receive byte**  
The first SPI cycle is complete, RXBF bit is asserted '1', and the SPINT interrupt is asserted, if enabled. (See [Section 24.7, "SPI Interrupts"](#)). The data now contained in **SPIRD - SPI RX\_Data Register** is the first half of the 16 bit word containing the temperature data.  
Once the first SPI cycle is completed, the SPI master takes the pending data in the TX\_DATA register (dummy byte 2) and loads it into the TX shift register. Loading the shift register automatically asserts the TXFE bit, begins shifting the dummy data value onto the SPDOUT pin, and drives the **SPCLKOUT** pin. Data on the SPDIN pin is also sampled on each clock.
- Once the TXFE bit is asserted the SPI Master is ready to receive its next byte. Before writing the next TX\_DATA value, software must clear the RXBF status bit by reading the **SPIRD - SPI RX\_Data Register**.

//Transmit next reading command

- BIOEN is asserted '1' to indicate that data will now be driven by the master.
- Next, a command byte is written to the TX\_DATA register. This value is the first half of a 16 bit command to be sent to temperature sensor peripheral. The SPI master automatically clears the TXFE bit, but does not begin shifting the command data value onto the SPDOUT pin. This byte will remain in the TX\_DATA register until the TX shift register is empty. This data will be transmitted because the output buffer is enabled. Data on the SPDIN pin is sampled on each clock.
- **After 8 SPCLKOUT pulses from the second receive byte:**  
The second SPI cycle is complete, RXBF bit is asserted '1', and the SPINT interrupt is asserted, if enabled. (See [Section 24.7, "SPI Interrupts"](#)). The data now contained in **SPIRD - SPI RX\_Data Register** is the second half of the 16 bit word containing the temperature data.  
Once the first SPI cycle is completed, the SPI master takes the pending data in the TX\_DATA register (command byte 1) and loads it into the TX shift register. Loading the shift register automatically asserts the TXFE bit, begins shifting the dummy data value onto the SPDOUT pin, and drives the **SPCLKOUT** pin. Data on the SPDIN pin is also sampled on each clock.
- Once the TXFE bit is asserted the SPI Master is ready to receive its next byte. Before writing the next TX\_DATA value, software must clear the RXBF status bit by reading the **SPIRD - SPI RX\_Data Register**.
- Next, the second command byte is written to the TX\_DATA register. The SPI master automatically clears the TXFE bit, but does not begin shifting the command data value onto the SPDOUT pin. This byte will remain in the TX\_DATA register until the TX shift register is empty.
- **After 8 SPCLKOUT pulses from the first transmit byte:**  
The third SPI cycle is complete, RXBF bit is asserted '1', and the SPINT interrupt is asserted, if enabled. (See [Section 24.7, "SPI Interrupts"](#)). The data now contained in **SPIRD - SPI RX\_Data Register** is invalid, since this command was used to transmit the first command byte to the SPI slave.  
Once the first SPI cycle is completed, the SPI master takes the pending data in the TX\_DATA register (command byte 2) and loads it into the TX shift register. Loading the shift register automatically asserts the TXFE bit, begins shifting the dummy data value onto the SPDOUT pin, and drives the **SPCLKOUT** pin. Data on the SPDIN pin is also sampled on each clock.

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- Once the TXFE bit is asserted the SPI Master is ready to transmit or receive its next byte. Before writing the next TX\_DATA value, software must clear the RXBF status bit by reading the [SPIRD - SPI RX\\_Data Register](#).
- Since no more data needs to be transmitted, the host software will wait for the RXBF status bit to be asserted indicating the second command byte was transmitted successfully.
- #CS is de-asserted.

## 24.13 General Purpose Serial Peripheral Interface (GP-SPI) Revision History

This revision history shows the changes made to this chapter.

**Table 24.16 General Purpose Serial Peripheral Interface (GP-SPI) Chapter Revision History**

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History," on page 539</a> . |              |            |                                                                                                                                                                                                                              |                                                                                                                                                                                                                                                    |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| #                                                                                                                                                                                                                                            | REV# IN SPEC | DATE       | SECTION/FIGURE/ENTRY                                                                                                                                                                                                         | CORRECTION                                                                                                                                                                                                                                         |
| 1.                                                                                                                                                                                                                                           | 0.4          | 04/25/2007 | <a href="#">Table 24.15, "SPCLKOUT Frequencies," on page 438</a>                                                                                                                                                             | Updated frequency to match Ring oscillator & devisors.                                                                                                                                                                                             |
| 2.                                                                                                                                                                                                                                           | 0.4          | 04/25/2007 | <a href="#">Section 24.5.2,</a><br><a href="#">Section 24.9.4,</a><br><a href="#">Section 24.11.6</a><br><br><a href="#">Section 24.4, "SPI Interface Signals," on page 421</a><br><br><a href="#">Note 24.1 on page 422</a> | <ul style="list-style-type: none"> <li>■ Removed references to a separate 21.5MHz clock source.</li> <li>■ Added reference to <a href="#">Table 3.9, "MISC Interface," on page 44</a>.</li> <li>■ With 8ma Buffer clock speed 16.13MHz.</li> </ul> |
| 3.                                                                                                                                                                                                                                           |              | 05/06/2007 | <a href="#">Section 24.9.4.5, "Limits of SPI configurations," on page 430</a><br><a href="#">Note 24.1 on page 422</a>                                                                                                       | <ul style="list-style-type: none"> <li>■ Limits in function updated</li> </ul>                                                                                                                                                                     |
| 4.                                                                                                                                                                                                                                           |              | 5/10/2007  | <a href="#">Section 24.4, "SPI Interface Signals," on page 421,</a><br><a href="#">Table 24.2, &amp; Figure 24.2.</a>                                                                                                        | <ul style="list-style-type: none"> <li>■ Added Explicit block to pin routing information.</li> </ul>                                                                                                                                               |



## Chapter 25 RC Identification Detection (RC\_ID)

## 25.1 General Description

The Resistor/Capacitor Identification Detection (RC\_ID) interface provides a single pin interface which can discriminate a number of quantized RC constants. The judicious selection of RC values can provide a low cost means for system element configuration identification. The RC\_ID I/O pin measures the charge/discharge time for an RC circuit connected to the pin as shown in [Figure 25.1](#).

## 25.2 Block Diagram

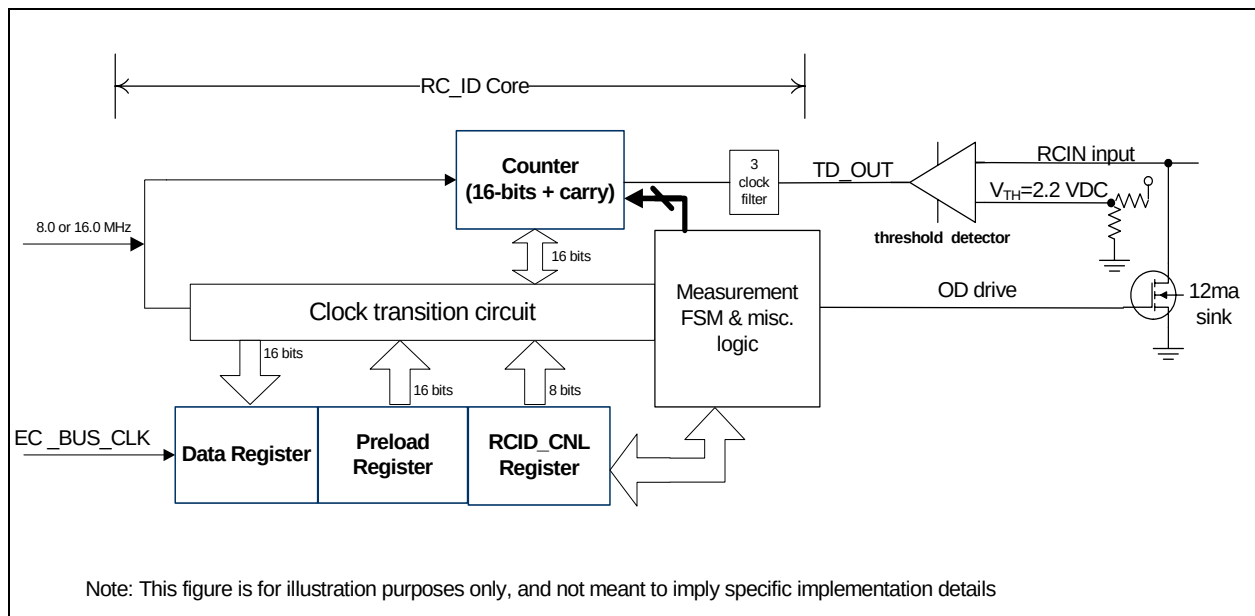


**Figure 25.1 Block Diagram of RC Identification Detection (RC\_ID)**

## 25.3 Power, Clocks and Reset

### 25.3.1 Power Domain

This block is powered by the VTR Power Supply.

See [Section 4.5, "Power Configuration," on page 96](#) for details on power domains.

### 25.3.2 Clocks

This block uses the [EC Bus Clock](#) and the 64.52MHz [MCLK](#). The [EC Bus Clock](#) is used to access the [Registers](#) described in this block. [MCLK](#) is divided down to provide a sampling clock.

See [Section 4.4, "Clock Generator," on page 77](#) for details on clocks.

### 25.3.3 Power On Reset

This block is reset on a [nSYS\\_RST](#). Following a system reset, all Register are reset to 00h and the state machines are set to [Reset](#).

See [Section 4.6, "Reset Interface," on page 99](#) for details on reset.

## 25.4 Interrupts

The [RC Identification Detection \(RC\\_ID\)](#) can generate an RCID\_DONE interrupt when the [DONE](#) bit in the [RCID\\_CTL Register](#) is set. The interrupt source is routed onto the [RCID](#) bit in [IRQ19 Source Register on page 340](#) and is a level, active high signal.

## 25.5 Time Constants

This section lists a set of proposed R and C values which can be connected to the RC\_ID pin. However, the number of R/C combinations that can be discriminated is tentative at this writing, pending full characterization.

### 25.5.1 PROPOSED Specific Time constant - 16 MHz Clock

Table 25.1 Sample RC values (C=2200 pF. R varied)

| C (pF)<br>10% | R (K)<br>5% | Rise Time<br>(usec) | Minimum<br>Cycle Count | Maximum<br>Cycle Count |
|---------------|-------------|---------------------|------------------------|------------------------|
| 2200          | 1           | 2.20                | 30                     | 40                     |
| 2200          | 2           | 4.40                | 60                     | 81                     |
| 2200          | 4.3         | 9.46                | 129                    | 174                    |
| 2200          | 8.2         | 18.04               | 246                    | 333                    |
| 2200          | 33          | 72.60               | 993                    | 1341                   |
| 2200          | 62          | 136.40              | 1865                   | 2520                   |
| 2200          | 130         | 286.00              | 3912                   | 5285                   |
| 2200          | 240         | 528.00              | 7223                   | 9757                   |

Table 25.2 Sample RC values (C=3000 pF. R varied)

| C (pF)<br>10% | R (K)<br>5% | Rise Time<br>(usec) | Minimum<br>Cycle Count | Maximum<br>Cycle Count |
|---------------|-------------|---------------------|------------------------|------------------------|
| 3000          | 1           | 3.00                | 41                     | 55                     |
| 3000          | 2           | 6.00                | 82                     | 110                    |
| 3000          | 4.3         | 12.90               | 176                    | 238                    |
| 3000          | 8.2         | 24.60               | 336                    | 454                    |
| 3000          | 33          | 99.00               | 1354                   | 1829                   |
| 3000          | 62          | 186.00              | 2544                   | 3437                   |
| 3000          | 130         | 390.00              | 5335                   | 7207                   |
| 3000          | 240         | 720.00              | 9849                   | 13305                  |

**Table 25.3 Sample RC values (C=4700 pF. R varied)**

| C (pF)<br>10% | R (K)<br>5% | Rise Time<br>(usec) | Minimum<br>Cycle Count | Maximum<br>Cycle Count |
|---------------|-------------|---------------------|------------------------|------------------------|
| 4700          | 1           | 4.70                | 64                     | 86                     |
| 4700          | 2           | 9.40                | 128                    | 173                    |
| 4700          | 4.3         | 20.21               | 276                    | 373                    |
| 4700          | 8.2         | 38.54               | 527                    | 712                    |
| 4700          | 33          | 155.10              | 2121                   | 2866                   |
| 4700          | 62          | 291.40              | 3986                   | 5385                   |
| 4700          | 130         | 611.00              | 8358                   | 11291                  |
| 4700          | 240         | 1128.00             | 15431                  | 20845                  |

**Table 25.4 Sample RC values (C=4700 pF. R varied)**

| C (pF)<br>10% | R (K)<br>5% | Rise Time<br>(usec) | Minimum<br>Cycle Count | Maximum<br>Cycle Count |
|---------------|-------------|---------------------|------------------------|------------------------|
| 4700          | 1           | 4.70                | 64                     | 86                     |
| 4700          | 2           | 9.40                | 128                    | 173                    |
| 4700          | 4.3         | 20.21               | 276                    | 373                    |
| 4700          | 8.2         | 38.54               | 527                    | 712                    |
| 4700          | 33          | 155.10              | 2121                   | 2866                   |
| 4700          | 62          | 291.40              | 3986                   | 5385                   |
| 4700          | 130         | 611.00              | 8358                   | 11291                  |
| 4700          | 240         | 1128.00             | 15431                  | 20845                  |

## 25.5.2 PROPOSED Specific Time constant - 8 MHz Clock

**Table 25.5 Sample RC values (C=2200 pF. R varied)**

| C (pF)<br>10% | R (K)<br>5% | Rise Time<br>(usec) | Minimum<br>Cycle Count | Maximum<br>Cycle Count |
|---------------|-------------|---------------------|------------------------|------------------------|
| 2200          | 1           | 2.20                | 15                     | 20                     |
| 2200          | 2           | 4.40                | 30                     | 40                     |
| 2200          | 4.3         | 9.46                | 64                     | 87                     |
| 2200          | 8.2         | 18.04               | 123                    | 166                    |
| 2200          | 33          | 72.60               | 496                    | 670                    |
| 2200          | 62          | 136.40              | 932                    | 1260                   |
| 2200          | 130         | 286.00              | 1956                   | 2642                   |
| 2200          | 240         | 528.00              | 3611                   | 4878                   |



Table 25.6 Sample RC values (C=3000 pF. R varied)

| C (pF)<br>10% | R (K)<br>5% | Rise Time<br>(usec) | Minimum<br>Cycle Count | Maximum<br>Cycle Count |
|---------------|-------------|---------------------|------------------------|------------------------|
| 3000          | 1           | 3.00                | 20                     | 27                     |
| 3000          | 2           | 6.00                | 41                     | 55                     |
| 3000          | 4.3         | 12.90               | 88                     | 119                    |
| 3000          | 8.2         | 24.60               | 168                    | 227                    |
| 3000          | 33          | 99.00               | 677                    | 914                    |
| 3000          | 62          | 186.00              | 1272                   | 1718                   |
| 3000          | 130         | 390.00              | 2667                   | 3603                   |
| 3000          | 240         | 720.00              | 4924                   | 6652                   |

Table 25.7 Sample RC values (C=4700 pF. R varied)

| C (pF)<br>10% | R (K)<br>5% | Rise Time<br>(usec) | Minimum<br>Cycle Count | Maximum<br>Cycle Count |
|---------------|-------------|---------------------|------------------------|------------------------|
| 4700          | 1           | 4.70                | 32                     | 43                     |
| 4700          | 2           | 9.40                | 64                     | 86                     |
| 4700          | 4.3         | 20.21               | 138                    | 186                    |
| 4700          | 8.2         | 38.54               | 263                    | 356                    |
| 4700          | 33          | 155.10              | 1060                   | 1433                   |
| 4700          | 62          | 291.40              | 1993                   | 2692                   |
| 4700          | 130         | 611.00              | 4179                   | 5645                   |
| 4700          | 240         | 1128.00             | 7715                   | 10422                  |

## 25.6 Block Diagram

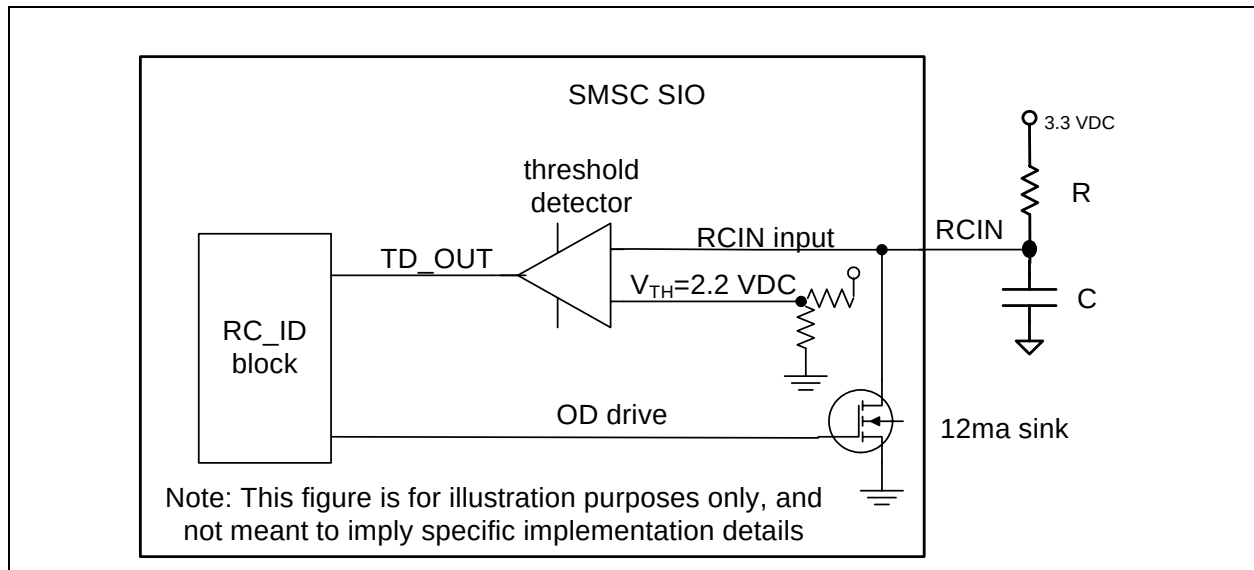


**Figure 25.2**

The RC\_ID uses the 8.0 / 16.0MHz clock input; therefore, a measurement can only be made when VTR and this clock are present.

The RC\_ID block initiates the discharging followed by the charging of the external RC circuit (see [Figure 25.1](#)). At the same time, the RCID input goes through a threshold detector set at 68% of 3.3 VDC. The accuracy of the threshold detector is TBD, based on characterization. Original goal  $\pm 5\%$ . The TD\_OUT gates the 16 bit Counter with a 125 ns Resolution per bit with a 8.0 MHz clock or 62.5 ns with a 16.0 MHz clock. The input has an input glitch rejection filter. Any change in input less than 210 ns is ignored.



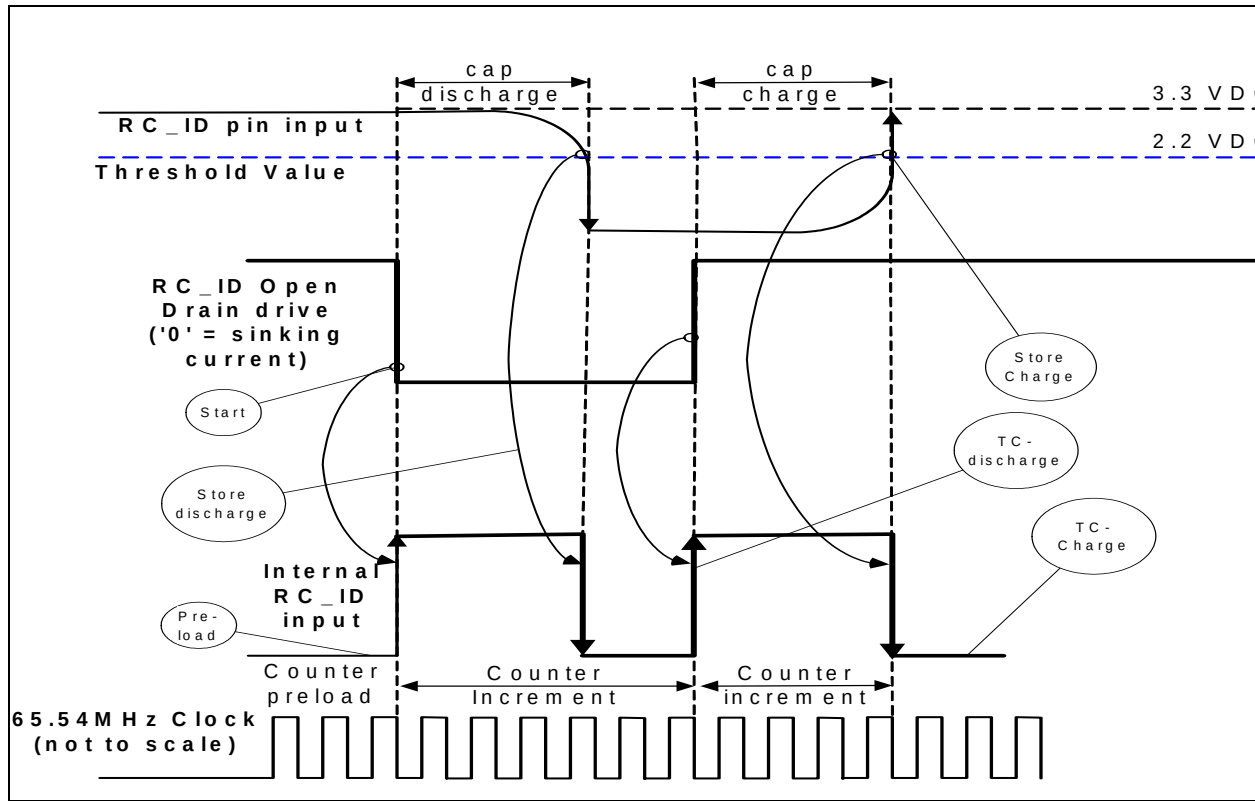
## Product Customer Specification-ODM

**APPLICATION NOTE:** After completion of a measurement cycle with the **DONE** bit set to '1' in the **RCID\_CTL**

Table 25.8 RC\_ID Measurement States

| STATE             | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Reset             | <p>The <b>RCID_CTL Register ENABLE</b> bit is cleared to '0' by <b>nSYS_RST</b> or a write. The pin OD output driver is tristated, the RCID blocked is placed in low power mode. The <b>DONE</b>, <b>CY_ER</b>, <b>TC</b> bits in the <b>RCID_CTL Register</b> are autonomously cleared to '0'.</p> <p><b>Note:</b> Clearing the <b>ENABLE</b> bit with a value other than 00h to the <b>RCID_CTL Register</b> is not defined and may create unpredictable results.</p>                                                             |
| Enabled           | Setting the <b>ENABLE</b> bit to '1' in the <b>RCID_CTL Register</b> places the RC_ID interface active high power state. .                                                                                                                                                                                                                                                                                                                                                                                                          |
| Start             | <p>The <b>Start</b> state is initiated by a write to the <b>RCID_CTL Register</b> setting the <b>START</b> bit to '1'. The counter is initiated to the preload value of 0000h and starts incrementing. The pin OD driver begins to sink current and external capacitor starts discharging. The <b>DONE</b>, <b>CY_ER</b>, <b>TC</b> bits in the <b>RCID_CTL Register</b> are autonomously cleared to '0'.</p>                                                                                                                       |
| Detect Dis-charge | The pin voltage decays as the external capacitor discharges and the counter continues to increment until the terminal count is reached. The pin voltage is monitored to detect the discharge voltage reaches below the threshold voltage before the counter reaches terminal count.                                                                                                                                                                                                                                                 |
| TC-Dis-charged    | <p>The incrementing counter reaches the terminal count value of FFFFh. The <b>TC</b> bit in the <b>RCID_CTL Register</b> is autonomously set to '1'. If the pin voltage fails to discharge below the threshold voltage before the counter reaches terminal count during <b>Detect Discharge</b>, then <b>CY_ER</b> bit in the <b>RCID_CTL Register</b> is autonomously set to '1'; otherwise, then <b>CY_ER</b> bit remains clear.</p> <p>The pin OD output driver is tristated and the counter starts incrementing from 0000h.</p> |
| Detect Charge     | <p>The pin voltage rises to the threshold voltage, counter stops counting, and the present value of the counter is stored in the <b>RC_ID Data Register</b>. The <b>DONE</b> bit in the <b>RCID_CTL Register</b> is autonomously set to '1'.</p>                                                                                                                                                                                                                                                                                    |
| TC-Charged        | <p>The incrementing counter reaches the terminal count value of FFFFh and the pin voltage is below the threshold value. The <b>CY_ER</b> bit and <b>DONE</b> bits in the <b>RCID_CTL Register</b> are autonomously set to '1'.</p> <p><b>Note:</b> The <b>Detect Charge</b> and the <b>TC-Discharged</b> STATES are mutually exclusive.</p>                                                                                                                                                                                         |

**Register**, the programmer must place the RC\_ID back into the reset state to before starting a new measurement.


**Figure 25.3**

All registers are VTR powered and are placed in reset when `nSYS_RST` (internal signal) is '0'.

## 25.7 Registers

Each instance of the [RC Identification Detection \(RC\\_ID\)](#) has its own Logical Device Number, and Base Address as indicated in [Table 25.9](#).

**Table 25.9 RC Identification Detection (RC\_ID) Base Address Table**

| RC Identification Detection (RC_ID) INSTANCE | LDN FROM (Table 7.3 on page 168) | AHB BASE ADDRESS |
|----------------------------------------------|----------------------------------|------------------|
| RC ID                                        | 4h                               | F0_1000h         |

[Table 25.10](#) is a register summary for this instance of the [RC Identification Detection \(RC\\_ID\)](#).

**Table 25.10 RC Identification Detection (RC\_ID) Register Summary**

|                                     | EC INTERFACE |           |         | NOTES |
|-------------------------------------|--------------|-----------|---------|-------|
| REGISTER NAME                       | SPB OFFSET   | BYTE LANE | EC TYPE |       |
| <a href="#">RCID_CTL Register</a>   | 00h          | 0         | R/W     |       |
| <a href="#">RC_ID Data Register</a> | 04h          | 0         | R       |       |
|                                     |              | 1         |         |       |

## 25.8 Runtime Registers

**Table 25.11 RCID\_CTL Register**

|             |          |       |          |        |     |       |                     |      |
|-------------|----------|-------|----------|--------|-----|-------|---------------------|------|
| HOST OFFSET | N/A      |       |          |        |     |       | HOST SIZE           |      |
| EC OFFSET   | 00h      |       |          | 16-Bit |     |       | EC SIZE             |      |
| POWER       | VTR      |       |          | 00h    |     |       | nSYS_RST<br>DEFAULT |      |
| BUS         | EC SPB   |       |          |        |     |       |                     |      |
| BYTE1 BIT   | D15      | D14   | D13      | D12    | D11 | D10   | D9                  | D8   |
| HOST TYPE   | -        | -     | -        | -      | -   | -     | -                   | -    |
| EC TYPE     | R        | R     | R        | R      | R   | R     | R/W                 | R/W  |
| BIT NAME    | Reserved |       |          |        |     |       | Clock_Sel           |      |
| BYTE0 BIT   | D7       | D6    | D5       | D4     | D3  | D2    | D1                  | D0   |
| HOST TYPE   | -        | -     | -        | -      | -   | -     | -                   | -    |
| EC TYPE     | R/W      | R/W   | R        | R      | R   | R     | R                   | R    |
| BIT NAME    | ENABLE   | START | Reserved |        |     | CY_ER | TC                  | DONE |

is12.904'0'This field selects the frequency of the Counter circuit clock. [Table 25.12, "Clock Select Field"](#) shows the clock frequencies that can be selected:

**Table 25.12 Clock Select Field**

|   | COUNTER CLOCK |            | FULL COUNT DURATION |
|---|---------------|------------|---------------------|
| 0 | DIVIDE BY 1   | 64.512 MHz | 1.02 $\mu$ sec      |
| 1 | DIVIDE BY 2   | 32.256 MHz | 2.03 $\mu$ sec      |



**Table 25.12 Clock Select Field**

|   | COUNTER CLOCK |            | FULL COUNT DURATION |
|---|---------------|------------|---------------------|
| 2 | DIVIDE BY 4   | 16.128 MHz | 4.06 $\mu$ sec      |
| 3 | DIVIDE BY 8   | 8.064 MHz  | 8.13 $\mu$ sec      |

The values in the [Clock Select Field](#) should only be changed when the [ENABLE](#) bit in the [RCID\\_CTL Register](#) is cleared to '0'.

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**Table 25.13 RC\_ID Data Register**

| HOST ADDRESS |                        |     |     |     |     |     | HOST SIZE |                                     |
|--------------|------------------------|-----|-----|-----|-----|-----|-----------|-------------------------------------|
| EC OFFSET    | 04h                    |     |     |     |     |     | 16-bit    | EC SIZE                             |
| POWER        | VTR                    |     |     |     |     |     | 0000h     | <a href="#">nSYS_RST</a><br>DEFAULT |
| BUS          | <a href="#">EC SPB</a> |     |     |     |     |     |           |                                     |
| BYTE1 BIT    | D15                    | D14 | D13 | D12 | D11 | D10 | D9        | D8                                  |
| HOST TYPE    | -                      | -   | -   | -   | -   | -   | -         | -                                   |
| EC TYPE      | R                      | R   | R   | R   | R   | R   | R         | R                                   |
| BIT NAME     | Data[15:8]             |     |     |     |     |     |           |                                     |
| BYTE0 BIT    | D7                     | D6  | D5  | D4  | D3  | D2  | D1        | D0                                  |
| HOST TYPE    | -                      | -   | -   | -   | -   | -   | -         | -                                   |
| EC TYPE      | R                      | R   | R   | R   | R   | R   | R         | R                                   |
| BIT NAME     | Data[7:0]              |     |     |     |     |     |           |                                     |



## 25.9 RC Identification Detection (RC\_ID) Revision History

This revision history shows the changes made to this chapter.

**Table 25.14 RC Identification Detection (RC\_ID) Chapter Revision History**

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History," on page 539.</a> |              |            |                                                               |                                                                                                         |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------------|---------------------------------------------------------------|---------------------------------------------------------------------------------------------------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE       | SECTION/FIGURE/ENTRY                                          | CORRECTION                                                                                              |
| 1.                                                                                                                                                                                                                                          | 0.4          | 04/25/2007 | <a href="#">Table 25.11, "RCID_CTL Register," on page 453</a> | <ul style="list-style-type: none"> <li>■ Bit D5 is Read-Only</li> <li>■ Bit D9 is Read/write</li> </ul> |
| 2.                                                                                                                                                                                                                                          |              |            |                                                               |                                                                                                         |
| 3.                                                                                                                                                                                                                                          |              |            |                                                               |                                                                                                         |
| 4.                                                                                                                                                                                                                                          |              |            |                                                               |                                                                                                         |



## Chapter 26 16-Bit Timer Interface

### 26.1 General Description

The MEC5035 [16-Bit Timer Interface](#) implements four 16-bit auto-reloading timers.

### 26.2 Terms

The following section defines terms used in this chapter.

| TERM            | DEFINITION                                                         |
|-----------------|--------------------------------------------------------------------|
| Overflow        | When the timer counter transitions from FFFFh to 0000h             |
| Underflow       | When the timer counter transitions from 0000h to FFFFh.            |
| timer tick rate | This is the rate at which the timer is incremented or decremented. |

### 26.3 Block Diagram

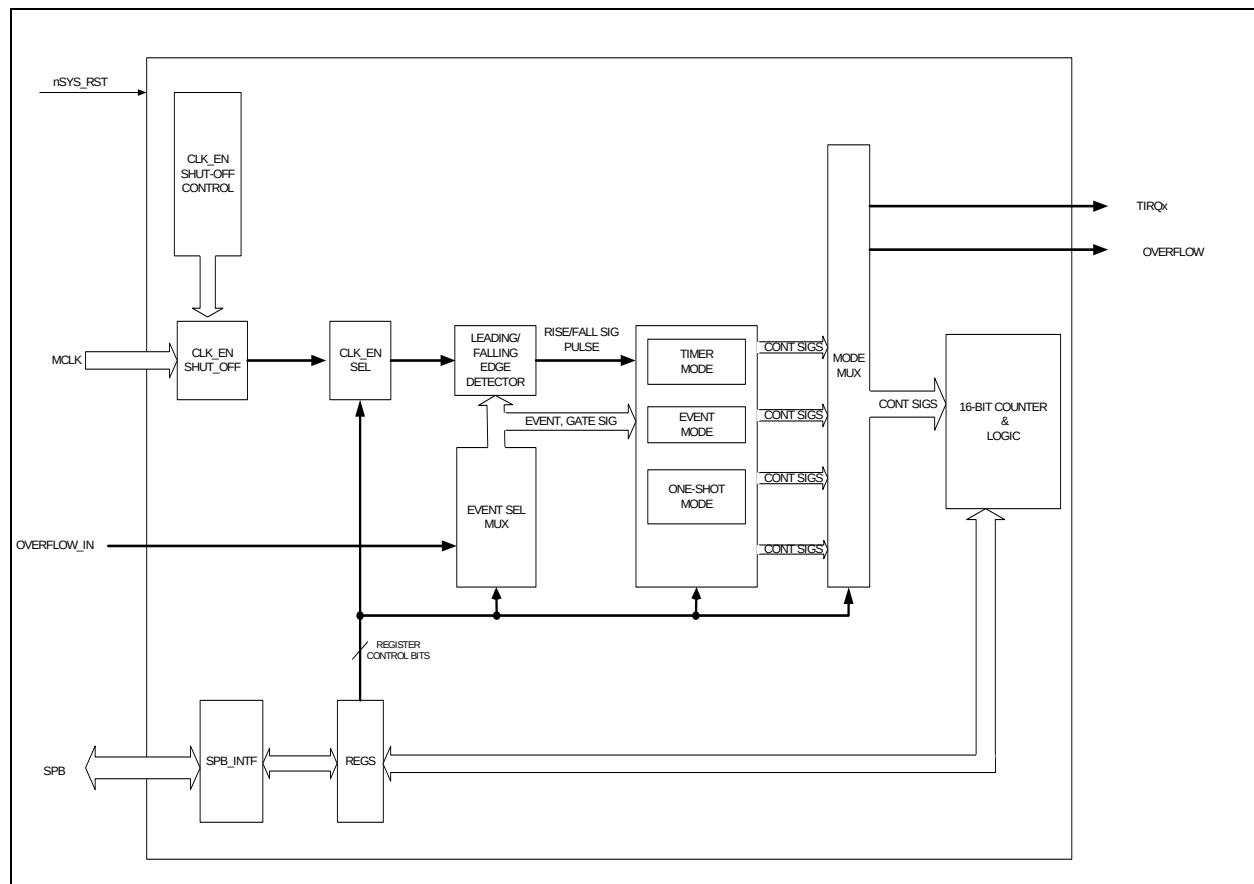


Figure 26.1 Block Diagram for Timer x

## 26.4 Signal List for Block Diagram

**Table 26.1 Block Diagram Signal List Description**

| SIGNAL NAME          | DIRECTION | DESCRIPTION                                                                                                                        |
|----------------------|-----------|------------------------------------------------------------------------------------------------------------------------------------|
| VTR POR              | INPUT     | <a href="#">nSYS_RST</a>                                                                                                           |
| <a href="#">MCLK</a> | INPUT     | Clock source to block.                                                                                                             |
| OVERFLOW_IN          | INPUT     | External Timer input. Used for cascading timers.                                                                                   |
| TIRQx                | OUTPUT    | Timer x Interrupt Request                                                                                                          |
| OVERFLOW             | OUTPUT    | One clock wide pulse that is generated every time the timer underflows or overflows. This signal is used for cascading the timers. |
| SPB                  | I/O Bus   | Bus used by microprocessor to access the registers in this block.                                                                  |

## 26.5 Timers

**Table 26.2 Timer Type and I/O Description**

| TIMER NAME | TIMER TYPE      | OVER-FLOW/<br>UNDER-FLOW<br>INPUT |
|------------|-----------------|-----------------------------------|
| Timer 0    | General Purpose | Timer 3                           |
| Timer 1    | General Purpose | Timer 0                           |
| Timer 2    | General Purpose | Timer 1                           |
| Timer 3    | General Purpose | Timer 2                           |

**Note:** All timers cascaded together must be on the same clock source.

## 26.6 Power, Clocks and Reset

### 26.6.1 Power Domain

This block is powered by the VTR power supply.

See [Section 4.5, "Power Configuration," on page 96](#) for details on power domains.

### 26.6.2 Clocks

This block has two main clock inputs: [EC Bus Clock](#) and [MCLK](#). The [EC Bus Clock](#) is used by the EC Data Memory Bus to interface to the embedded controller accessible registers. The [MCLK](#) clock source is the clock source for the week alarm logic.

In addition to the main clock inputs, there is a clock enable input for each of the supported frequencies listed in [Table 26.11, "Timer Clock Frequencies," on page 466](#). Any of these enables may be selected for the Timer Clock Frequency. Independently, any of these clock frequencies may be selected for the

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filter clock via the FCLK[3:0] bits located in [Section 26.11.2, "Timer x Clock and Event Control Register," on page 466](#).

See [Section 4.4, "Clock Generator," on page 77](#) for details on clocks.

### 26.6.3 Reset

This block is reset on a [nSYS\\_RST](#). On [nSYS\\_RST](#) all timers are reset to their default values. The timers are also reset by the [RESET](#) bit in each [Timer x Control Register](#).

See [Section 4.6, "Reset Interface," on page 99](#) for details on reset.

## 26.7 Interrupts

The timers in the MEC5035 can be used to generate interrupts when the timer overflows or underflows. The timer interrupts are routed to the [TIMER3](#), [TIMER2](#), [TIMER1](#), and [TIMER0](#) bits in [IRQ31 Source Register](#).

**Note:** No interrupts are generated while the [ENABLE](#) bit is cleared.

## 26.8 Low Power Modes

This block is designed to conserve power when it is either sleeping or a clock source is not required.

During normal operation, if the timer is disabled via the PD bit the [TIMERx\\_CLK\\_REQ](#) signal is de-asserted. This indicates to the clock generator logic that this timer does not require the 64.52MHz clock source.

During Sleep modes the clock input is gated, the [TIMERx\\_CLK\\_REQ](#) signal is asserted, and the interrupt output goes to the inactive state. When the block returns from sleep, if enabled, it will be restarted from the preload value.

**Note:** The timer is terminated one TCLK after the [SLEEP ENABLE](#) is asserted.

The following table illustrates the low power mode options.

**Table 26.3 Block Clock Gating in Low Power Modes**

| POWER DOWN (PD) BIT | <a href="#">SLEEP ENABLE</a> | BLOCK IDLE STATUS | <a href="#">TIMERx_CLK_REQ</a> | STATE              | DESCRIPTION                                                        |
|---------------------|------------------------------|-------------------|--------------------------------|--------------------|--------------------------------------------------------------------|
| 1                   | X                            | NOT IDLE          | 1                              | PREPARING to SLEEP | The core clock is still required for up to one Timer Clock period. |
|                     |                              | IDLE              | 0                              | SLEEPING           | The block is idle and the core clock can be stopped.               |
| 0                   | 0                            | X                 | 1                              | NORMAL OPERATION   | The block is neither disabled by firmware nor commanded to SLEEP   |
|                     | 1                            | NOT IDLE          | 1                              | PREPARING to SLEEP | The core clock is still required for up to one Timer Clock period. |
|                     |                              | IDLE              | 0                              | SLEEPING           | The block is idle and the core clock can be stopped.               |

## 26.9 Operating Modes

### 26.9.1 Starting and Stopping

The MEC5035 timers can be started and stopped by setting and clearing the Timer Enable bit in the Timer Control Register in all modes, except one-shot.

### 26.9.2 Timer Mode

The Timer mode of the MEC5035 is used to generate periodic interrupts to the 8051. When operating in this mode the timer always counts down based on one of the internally generated clock sources. The Timer mode is selected by setting the Timer Mode Select bits in the Timer Control Register. See [Section 26.11.1, "Timer x Control Register," on page 464](#)

The period between timer interrupts and the width of the output pulse is determined by the speed of the clock source, the clock divide ratio and the value programmed into the Timer Reload Register. The timer clock source and clock rate are selected using the Clock Source Select bits (TCLK) in the [Timer x Clock and Event Control Register](#). See [Section 26.11.2, "Timer x Clock and Event Control Register," on page 466](#)

**Table 26.4 Timer Mode Operational Summary**

| ITEM                                | DESCRIPTION                                                                                                                                                                                                                                                                                                                       |
|-------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Timer Clock Frequencies             | This mode supports all the programmable frequencies listed in <a href="#">Table 26.11, "Timer Clock Frequencies," on page 466</a>                                                                                                                                                                                                 |
| Count Operation                     | Down Counter                                                                                                                                                                                                                                                                                                                      |
| Reload Operation                    | When the timer underflows:<br>RLOAD = 1, timer reloads from Timer Reload Reg<br>RLOAD = 0, timer rolls over to FFFFh.                                                                                                                                                                                                             |
| Count Start Condition               | ENABLE = 1                                                                                                                                                                                                                                                                                                                        |
| Count Stop Condition                | ENABLE = 0                                                                                                                                                                                                                                                                                                                        |
| Interrupt Request Generation Timing | When timer underflows from 0000h to reload value (as determined by RLOAD) an interrupt is generated.                                                                                                                                                                                                                              |
| Read From Timer                     | Current count value can be read by reading the Timer Count Register                                                                                                                                                                                                                                                               |
| Write to Preload Register           | When the timer is stopped, values written to the Timer Reload Register are copied into the timer counter. When the timer is running, values written to the Timer Reload Register are written to the timer counter when the timer underflows. The assertion of Reset also copies the Timer Reload Register into the timer counter. |
| Selectable Functions                | <ul style="list-style-type: none"> <li>■ Reload timer on underflow with programmed Preload value (Basic Timer)</li> <li>■ Reload timer with FFFFh in Free Running Mode (Free-running Timer)</li> </ul>                                                                                                                            |

#### 26.9.2.1 Timer Mode Underflow

The MEC5035 timers operating in Timer mode can underflow in two different ways. One method, the Reload mode shown in [Figure 26.2](#), is to reload the value programmed into the Reload register and continue counting from this value. The second method, Free Running mode [Figure 26.3](#), is to set the timer to FFFFh and continue counting from this value. The underflow behavior is controlled by the RLOAD bit in the Timer Control Register.

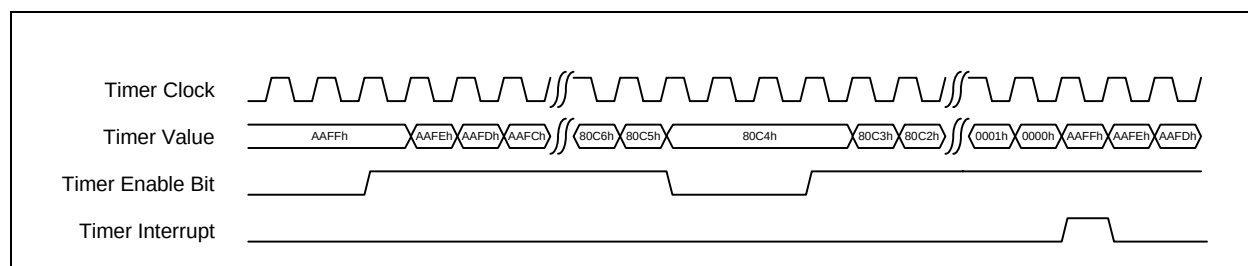


Figure 26.2 Reload Mode Behavior

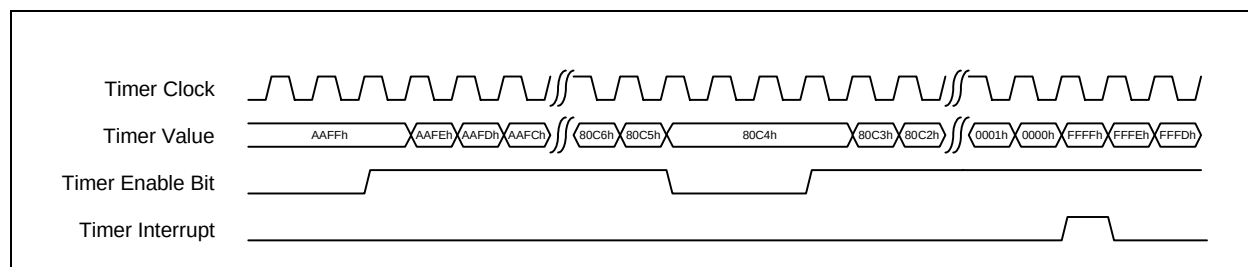


Figure 26.3 Free Running Mode Behavior

### 26.9.3 Event Mode

Event mode is used to overflow events from the previous timer. The direction the timer counts in Event mode is controlled by the [UPDN](#) bit in the Timer Control Register.

The timer can be programmed using the Clock and Event Control register to respond to the rising edge of overflow input, falling edge of the overflow input, and the rising and falling edges of the overflow input.

Table 26.5 Event Mode Operational Summary

| ITEM                                | DESCRIPTION                                                                                                                                                                                                                                                                                               |
|-------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Timer Clock Frequencies             | This mode supports all the programmable frequencies listed in <a href="#">Table 26.11, "Timer Clock Frequencies,"</a> on page 466                                                                                                                                                                         |
| Count Operation                     | Up/Down Counter                                                                                                                                                                                                                                                                                           |
| Reload Operation                    | <ul style="list-style-type: none"> <li>When the timer underflows:<br/>RLOAD = 1, timer reloads from Timer Reload Reg<br/>RLOAD = 0, timer rolls over to FFFFh.</li> <li>When the timer overflows:<br/>RLOAD = 1, timer reloads from Timer Reload Reg<br/>RLOAD = 0, timer rolls over to 0000h.</li> </ul> |
| Count Start Condition               | Timer Enable is set ( <a href="#">ENABLE</a> = 1)                                                                                                                                                                                                                                                         |
| Count Stop Condition                | Timer Enable is cleared ( <a href="#">ENABLE</a> = 0)                                                                                                                                                                                                                                                     |
| Interrupt Request Generation Timing | When timer overflows or underflows                                                                                                                                                                                                                                                                        |
| Read From Timer                     | Current count value can be read by reading the Timer Count Register                                                                                                                                                                                                                                       |

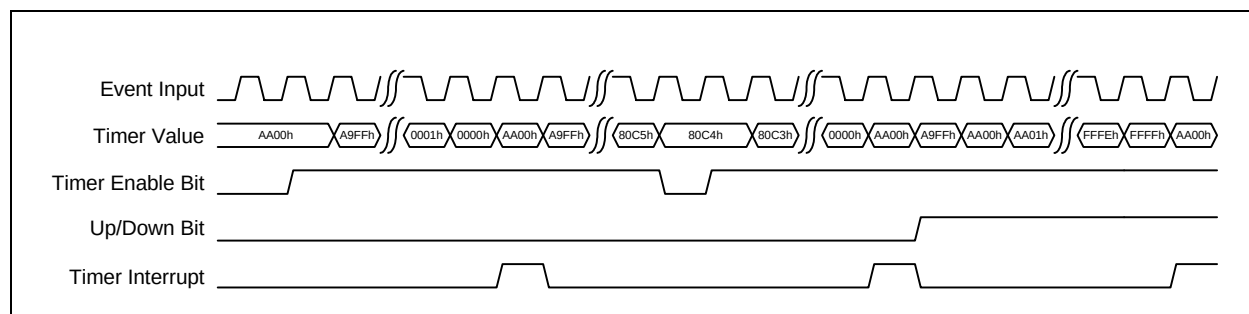


**Table 26.5 Event Mode Operational Summary (continued)**

| ITEM                      | DESCRIPTION                                                                                                                                                                                                                                                                                                                       |
|---------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Write to Preload Register | When the timer is stopped, values written to the Timer Reload Register are copied into the timer counter. When the timer is running, values written to the Timer Reload Register are written to the timer counter when the timer underflows. The assertion of Reset also copies the Timer Reload Register into the timer counter. |
| Selectable Functions      | <ul style="list-style-type: none"> <li>■ The direction of the counter is selectable via the UPDN bit.</li> <li>■ Reload timer on underflow/overflow with programmed Preload value (Basic Timer)</li> <li>■ Reload timer with FFFFh in Free Running Mode (Free-running Timer)</li> </ul>                                           |

### 26.9.3.1 Event Mode Operation

The timer starts counting events when the **ENABLE** bit in the Timer Control Register is set and continues to count until the **ENABLE** bit is cleared. When the **ENABLE** bit is set, the timer continues counting from the current value in the timer except after a reset event. After a reset event, the timer always starts counting from the value programmed in the Reload Register if counting down or from 0000h if counting up. [Figure 26.4](#) shows an example of timer operation in Event mode. The RLOAD bit controls the behavior of the timer when it underflows or overflows.


**Figure 26.4 Event Mode Operation**

### 26.9.4 One-Shot Mode

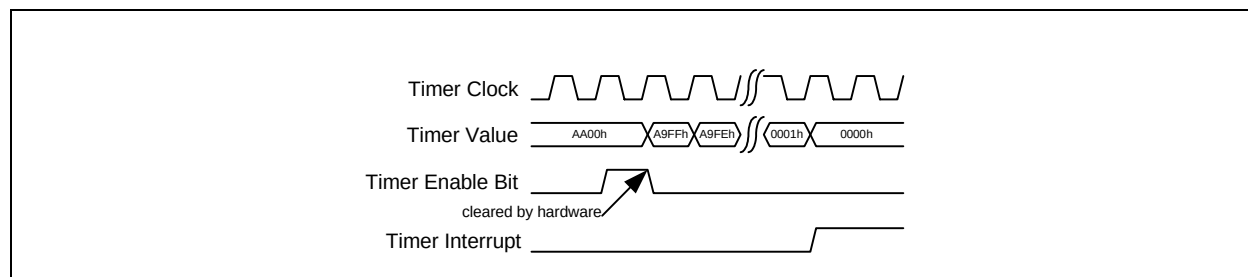
The One-Shot mode of the timer is used to generate a single interrupt to the EC after a specified amount of time. The timer can be configured to start using the EN bit ([Figure 26.5](#)) or on a timer overflow event from the previous timer. See [Section 26.11.2, "Timer x Clock and Event Control Register," on page 466](#) for configuration details. The **ENABLE** bit must be set for an event to start the timer. The **ENABLE** bit is cleared one clock after the timer starts. The timer always starts from the value in the Reload Register and counts down in One-Shot mode.

**Table 26.6 One Shot Mode Operational Summary**

| ITEM                    | DESCRIPTION                                                                                                                                                                                     |
|-------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Timer Clock Frequencies | This mode supports all the programmable frequencies listed in <a href="#">Table 26.11, "Timer Clock Frequencies," on page 466</a>                                                               |
| Count Operation         | Down Counter                                                                                                                                                                                    |
| Reload Operation        | <p>When the timer underflows the timer will stop.</p> <p>When the timer is enabled timer starts counting from value programmed in Timer Reload Register. (RLOAD has no effect in this mode)</p> |

**Table 26.6 One Shot Mode Operational Summary (continued)**

| ITEM                                | DESCRIPTION                                                                                                                                                                                                                                                                                                                       |
|-------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Count Start Condition               | Setting the <a href="#">ENABLE</a> bit to 1 starts One-Shot mode. The timer clock automatically clears the enable bit one timer tick later.<br><b>Note:</b> One-Shot mode may be enabled in Event Mode. In Event mode an overflow from the previous timer is used for timer tick rate.                                            |
| Count Stop Condition                | <ul style="list-style-type: none"> <li>■ Timer is reset (RESET = 1)</li> <li>■ Timer underflows</li> </ul>                                                                                                                                                                                                                        |
| Interrupt Request Generation Timing | When an underflow occurs.                                                                                                                                                                                                                                                                                                         |
| Read From Timer                     | Current count value can be read by reading the Timer Count Register                                                                                                                                                                                                                                                               |
| Write to Preload Register           | When the timer is stopped, values written to the Timer Reload Register are copied into the timer counter. When the timer is running, values written to the Timer Reload Register are written to the timer counter when the timer underflows. The assertion of Reset also copies the Timer Reload Register into the timer counter. |
| Selectable Functions                | Pulse Output Function                                                                                                                                                                                                                                                                                                             |

**Figure 26.5 Timer Start Based on EN Bit**

## 26.10 16-Bit Counter/Timer Interface Register Summary

There are four instances of the [16-Bit Timer Interface](#) block implemented in the MEC5035 enumerated as [0:3] with an overflow/underflow interface. Each instance of the [16-Bit Timer Interface](#) has its Base Address as indicated in [Table 26.7](#).

**Table 26.7 16-Bit Counter/Timer Interface Base Address Table**

| 16-Bit Timer Interface INSTANCE | LDN FROM (Table 7.3 on page 168) | AHB BASE ADDRESS           |
|---------------------------------|----------------------------------|----------------------------|
| 16-bit Timer.0                  | 3h                               | F0_0C00h                   |
| 16-bit Timer.1                  |                                  | F0_0C80h = F0_0C00h + 80h  |
| 16-bit Timer.2                  |                                  | F0_0D00h = F0_0C00h + 100h |
| 16-bit Timer.3                  |                                  | F0_0D80h = F0_0C00h + 180h |

[Table 26.8](#) is a register summary for one instance of the [16-Bit Timer Interface](#).

Table 26.8 16-Bit Counter/Timer Interface Register Summary

| REGISTER NAME                            | EC INTERFACE |         | NOTES |
|------------------------------------------|--------------|---------|-------|
|                                          | SPB OFFSET   | EC TYPE |       |
| Timer x Control Register                 | 00h          | R/W     |       |
| Timer x Clock and Event Control Register | 04h          | R/W     |       |
| Timer x Reload Register                  | 08h          | R/W     |       |
| Timer x Count Register                   | 0Ch          | R       |       |

## 26.11 Detailed Register Descriptions

### 26.11.1 Timer x Control Register

Table 26.9 Timer x Control Register

| HOST ADDRESS | n/a      |          |      | n/a                    |                 |          | HOST SIZE           |          |
|--------------|----------|----------|------|------------------------|-----------------|----------|---------------------|----------|
| EC OFFSET    | 00h      |          |      | 16-bit                 |                 |          | EC SIZE             |          |
| POWER        | VTR      |          |      | 0200h                  |                 |          | nSYS_RST<br>DEFAULT |          |
| BUS          | EC SPB   |          |      |                        |                 |          |                     |          |
| BYTE1 BIT    | D15      | D14      | D13  | D12                    | D11             | D10      | D9                  | D8       |
| HOST TYPE    | -        | -        | -    | -                      | -               | -        | -                   | -        |
| EC TYPE      | R        | R        | R    | R/W                    | R/W             | R/W      | R/W                 | R/W      |
| BIT NAME     | Reserved |          |      | TIMERx<br>_CLK_<br>REQ | SLEEP<br>ENABLE | Reserved | PD                  | Reserved |
| BYTE0 BIT    | D7       | D6       | D5   | D4                     | D3              | D2       | D1                  | D0       |
| HOST TYPE    | -        | -        | -    | -                      | -               | -        | -                   | -        |
| EC TYPE      | R/W      | R/W      | R/W  | R/W                    | R/W             | R/W      | R/W                 | R/W      |
| BIT NAME     | RLOAD    | Reserved | UPDN | Reserved               | MODE            |          | RESET               | ENABLE   |

#### ENABLE

Timer Enable - This bit is used to start and stop the timer. This bit does not reset the timer count but does reset the timer pulse output. This bit will be cleared when the timer starts counting in One-Shot mode.

0=Timer is disabled.

**Product Customer Specification-ODM**

1=Timer is enabled.

**Note:** The **ENABLE** bit is cleared after the RESET cycle is done. Firmware must poll the RESET bit.

**RESET**

Timer Reset - This bit stops the timer and resets the internal counter to the value in the Timer Reload Register. This bit also clears the Timer Enable bit if it is set. This bit is self clearing after the timer is reset. Firmware must poll this RESET bit.

0=Normal timer operation

1=Timer reset

**Note:** When the RESET takes effect interrupts are blocked.

**APPLICATION NOTE:** Interrupts are not blocked until RESET takes effect and the **ENABLE** bit is cleared. If interrupts are not desired, firmware must mask interrupt in the interrupt block.

**MODE**

Timer Mode Select - These bits control the timer mode.

00=Timer Mode

01=Event Mode

10=One Shot Mode

11=Reserved

**UPDN**

Up/Down. In Event mode this bit selects the timer count direction. This bit is only valid in Event mode.

Event Mode:

0=The timer counts down.

1=The timer counts up.

**RLOAD**

Reload Control. This bit controls how the timer is reloaded on overflow or underflow in Event and Timer modes, it has no effect in One Shot mode.

0=Roll timer over to FFFFh and continue counting when counting down and rolls over to 0000h and continues counting when counting up.

1=Reload timer from Timer Reload Register and continue counting.

**PD**

Power Down.

0=The timer is in a running state (default).

1=The timer is powered down and all clocks are gated.

**SLEEP ENABLE**

This bit is a read-only bit that reflects the state of the **SLEEP ENABLE** signal. This signal stops the timer and resets the internal counter to the value in the Timer Reload Register. Once the timer is disabled, the **TIMERx\_CLK** bits will be de-asserted. This signal does not clear the Timer Enable bit if it is set. If the timer is enabled, the counter will resume operation when the **SLEEP ENABLE** signal is de-asserted. The timer is held in reset as long as the input signal is asserted.

0=Normal timer operation. In Normal Mode, the timer operates as configured. When returning from a sleep mode, if enabled, the counter will be restarted from the preload value.

1=Sleep Mode Requested. In Sleep Mode, the timer is reset, the counter is disabled, and the **TIMERx\_CLK\_REQ** outputs are de-asserted.

## TIMERX\_CLK\_REQ

The **TIMERx\_CLK\_** bit is a read-only bit that reflects the state of the **TIMERX\_CLK\_REQ** output signal.

0=Indicates the 64.52MHz clock domain can be turned 'off' when appropriate

1=Indicates the 64.52MHz clock domain is required to be 'on.'

## 26.11.2 Timer x Clock and Event Control Register

**Table 26.10 Timer x Clock and Event Control Register**

|              |          |      |     |          |      |     |                     |     |
|--------------|----------|------|-----|----------|------|-----|---------------------|-----|
| HOST ADDRESS | n/a      |      |     | n/a      |      |     | HOST SIZE           |     |
| EC OFFSET    | 04h      |      |     | 16-bit   |      |     | EC SIZE             |     |
| POWER        | VTR      |      |     | 0000h    |      |     | nSYS_RST<br>DEFAULT |     |
| BUS          | EC SPB   |      |     |          |      |     |                     |     |
| BYTE1 BIT    | D15      | D14  | D13 | D12      | D11  | D10 | D9                  | D8  |
| HOST TYPE    | -        | -    | -   | -        | -    | -   | -                   | -   |
| EC TYPE      | R        | R    | R   | R        | R/W  | R/W | R/W                 | R/W |
| BIT NAME     | Reserved |      |     |          |      |     |                     |     |
| BYTE0 BIT    | D7       | D6   | D5  | D4       | D3   | D2  | D1                  | D0  |
| HOST TYPE    | -        | -    | -   | -        | -    | -   | -                   | -   |
| EC TYPE      | R/W      | R/W  | R/W | R        | R/W  | R/W | R/W                 | R/W |
| BIT NAME     | EVENT    | EDGE |     | Reserved | TCLK |     |                     |     |

### TCLK

This field is the Timer Clock Select, used to determine the clock source to the 16-bit timer.

**Table 26.11 Timer Clock Frequencies**

| Timer Clock Select | 64.520192 MHz Frequency divide Selected | Frequency Selected      |
|--------------------|-----------------------------------------|-------------------------|
| 0000               | Divide by 1                             | 64.52 MHz               |
| 0001               | Divide by 2                             | 32.26 MHz               |
| 0010               | Divide by 4                             | 16.13 MHz               |
| 0011               | Divide by 8                             | 8.06 MHz                |
| 0100               | Divide by 16                            | 4.03 MHz                |
| 0101               | Divide by 32                            | 2.01 MHz                |
| 0110               | Divide by 64                            | 1 MHz                   |
| 0111               | Divide by 128                           | 0.5 MHz                 |
| 1xxx               | Reserved for Future Use                 | Reserved for Future Use |

**Product Customer Specification-ODM****EDGE**

Edge Type Select. These bits are used to select the edge type that the timer counts. In One-Shot mode these bits select which edge starts the timer.

Event Mode:

00=Counts falling edges.

01=Counts rising edges

10=Counts rising and falling edges.

11=No event selected.

One-Shot Mode:

00=Starts counting on a falling edge.

01=Starts counting on a rising edge.

10=Starts counting on a rising or falling edge.

11=Start counting when the EN bit is set.

**EVENT**

Event Select - This bit is used to select the count source when the timer is operating in event mode. This bit should never be set to 1 for timers 0, 1 and 2.

0=Timer x-1 overflow is count source.

1=Timer disabled.

**26.11.3 Timer x Reload Register****Table 26.12 Timer x Reload Register**

| HOST ADDRESS | n/a                 |     |     | n/a    |     |     | HOST SIZE           |     |
|--------------|---------------------|-----|-----|--------|-----|-----|---------------------|-----|
| EC OFFSET    | 08h                 |     |     | 16-bit |     |     | EC SIZE             |     |
| POWER        | VTR                 |     |     | FFFFh  |     |     | nSYS_RST<br>DEFAULT |     |
| BUS          | EC SPB              |     |     |        |     |     |                     |     |
| BIT          | D15                 | D14 | D13 | ...    |     | D2  | D1                  | D0  |
| HOST TYPE    | -                   | -   | -   | -      | -   | -   | -                   | -   |
| EC TYPE      | R/W                 | R/W | R/W | R/W    | R/W | R/W | R/W                 | R/W |
| BIT NAME     | Timer Reload [15:0] |     |     |        |     |     |                     |     |

**TIMER RELOAD**

The Timer Reload register is used in Timer and One-Shot modes to set the lower limit of the timer. In Event mode the Timer Reload register sets either the upper or lower limit of the timer depending on if the timer is counting up or down. The Timer Reload register must be accessed low byte first. If the timer is running, the reload value will not be updated until the timer overflows or underflows.

**Note:** Programming a 0000h as a preload value is a valid count value and the timer will wrap on the next TCLK.

## 26.11.4 Timer x Count Register

**Table 26.13** Timer x Count Register

| HOST ADDRESS | n/a                |     |     | n/a    |   |    | HOST SIZE           |    |
|--------------|--------------------|-----|-----|--------|---|----|---------------------|----|
| EC OFFSET    | 0Ch                |     |     | 16-bit |   |    | EC SIZE             |    |
| POWER        | VTR                |     |     | FFFFh  |   |    | nSYS_RST<br>DEFAULT |    |
| BUS          | EC SPB             |     |     |        |   |    |                     |    |
| BIT          | D15                | D14 | D13 | ...    |   | D2 | D1                  | D0 |
| HOST TYPE    | -                  | -   | -   | -      | - | -  | -                   | -  |
| EC TYPE      | R                  | R   | R   | R      | R | R  | R                   | R  |
| BIT NAME     | Timer Count [15:0] |     |     |        |   |    |                     |    |

### TIMER COUNT

The Timer Count register returns the current value of the timer in all modes.

## 26.12 16-Bit Timer Interface Revision History

This revision history shows the changes made to this chapter.

**Table 26.14** 16-Bit Timer Interface Chapter Revision History

| “REV# IN SPEC” column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, “MEC5035 Product Customer Specification-ODM Revision History,” on page 539.</a> |              |           |                                   |                                                                                                           |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|-----------|-----------------------------------|-----------------------------------------------------------------------------------------------------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE      | SECTION/FIGURE/ENTRY              | CORRECTION                                                                                                |
| 1.                                                                                                                                                                                                                                          |              |           |                                   |                                                                                                           |
| 2.                                                                                                                                                                                                                                          | 0.5          | 6/06/2007 | <a href="#">RLOAD on page 465</a> | Swap bit definition as to the following: 1=Reload timer from Timer Reload Register and continue counting. |
| 3.                                                                                                                                                                                                                                          |              |           |                                   |                                                                                                           |
| 4.                                                                                                                                                                                                                                          |              |           |                                   |                                                                                                           |





## Chapter 27 LED

### 27.1 General Description

The LED can control three external LEDs. Each LED can be individually set to be full on, full off, or oscillate. Oscillation can in turn be configured to “blink”, where the LED output switches between full on and full off at a fixed frequency, or to “breathe”, where the brightness of the LED increases and decreases at a fixed rate. The periodic behavior of the LEDs is driven by the 32.768KHz crystal oscillator clock, so the LEDs will continue to function even when the EC is in sleep mode or the master 64.52MHz ring oscillator is shut down.

### 27.2 LED Block Diagram

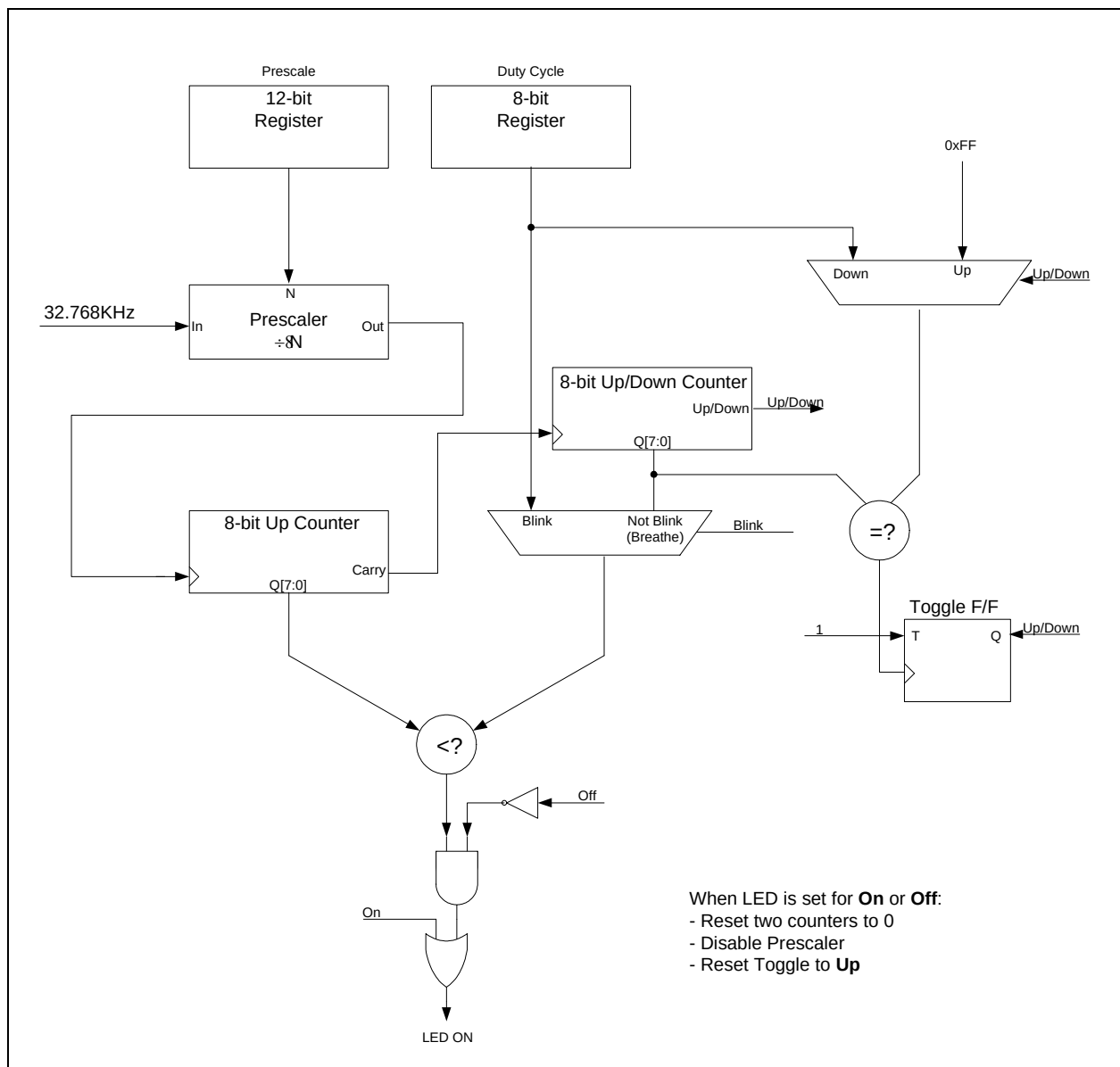


Figure 27.1 LED Block Diagram

## 27.3 Block Diagram Signal List

Table 27.1 LED Port List

| SIGNAL NAME | DIRECTION | DESCRIPTION                                                |
|-------------|-----------|------------------------------------------------------------|
| 32.768KHz   | INPUT     | <a href="#">X32K_CLK</a> , 32.768 crystal controlled clock |
| Blink       | Internal  | Control signal from <a href="#">LED Control Register</a>   |
| Up/Down     | Internal  | Control signal generated by 8-bit Up/Down counter          |
| LED ON      | OUTPUT    | LED outputs                                                |

## 27.4 Power, Clocks and Reset

### 27.4.1 Power Domain

This block is powered by the VTR Power Supply.

See [Section 4.5, "Power Configuration," on page 96](#) for details on power domains.

### 27.4.2 Clocks

This block has two clock inputs, the [EC Bus Clock](#) and [X32K\\_CLK](#). The [EC Bus Clock](#) is used in the interface to the embedded controller accessible registers. The 32.768KHz [X32K\\_CLK](#) is the clock source for the LED functional logic, including the counters.

See [Section 4.4, "Clock Generator," on page 77](#) for details on clocks.

### 27.4.3 Reset

This block is reset on a [nSYS\\_RST](#).

See [Section 4.6, "Reset Interface," on page 99](#) for details on reset.

## 27.5 Interrupts

The LED block does not generate interrupts.

## 27.6 LED Blinking and Breathing

Blinking and breathing is controlled by two registers for each LED. The first register controls the clock prescaler that sets the oscillation period. An 8-bit counter clocked on the pre-scaled 32.768KHz clock defines a blink period with 256 phases. In "blink" mode, the second register determines the duty cycle of the LED blink. In "breathe" mode, the second register determines the minimum duty cycle of the LED.

When the prescale is 0, the blink period will use the 32.768KHz clock (with 30.5 $\mu$ s phases). For  $N > 0$ , the 32.768KHz clock will be divided by  $N+1$ . For examples of settings of the prescale and duty cycle registers, see [Table 27.2, "LED Control Configuration Examples"](#). The maximum blink period is 32 seconds.

When an LED is configured to be fully off or fully on, the prescaler and other counters in the LED circuitry are shut down, in order to save power.

## 27.6.1 Blinking

When configured for blinking, the LED will be on for all phases of the prescaled period that are less than the duty cycle and off for all phases that are greater than the duty cycle. An LED with a duty cycle value of 0h will be fully off, while an LED with a duty cycle value of FFh will be fully on.

## 27.6.2 Breathing

When configured for breathing, the duty cycle of the LED blink will continuously increase and decrease between full on (a duty cycle of FFh) and a minimum duty cycle set by the duty cycle register. After each blink period the duty cycle will increase by 1, until the duty cycle saturates at FFh. Once the duty cycle saturates, it is reduced by 1 after each blink period, until it reaches a minimum duty cycle set by the duty cycle register. Once the minimum duty cycle is reached, the duty cycle will start increasing again. If the frequency of the LED blink period is sufficiently fast (for example, greater than 30Hz), the LED will not appear to blink but will instead appear dimmer or brighter, depending on the duty cycle.

The overall duration of the breathing oscillation is a factor of the blink period and the minimum duty cycle. The total time will be  $2 \times (BLINK\_PERIOD \times (FFh - MIN\_DUTY\_CYCLE))$ .

**Table 27.2 LED Control Configuration Examples**

| PRESCALE | DUTY CYCLE | BLINK PERIOD | BLINK                 | BREATHE                                            |
|----------|------------|--------------|-----------------------|----------------------------------------------------|
| 000h     | 00h        | 128Hz        | full off              | full off to full on<br>4s oscillation cycle        |
| 001h     | 40h        | 64Hz         | 3.9ms on, 11.6ms off  | quarter on to full on<br>6s oscillation cycle      |
| 003h     | 80h        | 32Hz         | 15.5ms on, 15.5ms off | half on to full on<br>8s oscillation cycle         |
| 07Fh     | 20h        | 1Hz          | 125ms on, 0.875s off  | blink to 1s on<br>7m 26s oscillation cycle         |
| 0BFh     | 16h        | 0.66Hz       | 125ms on, 1.375s off  | blink to 1.5s on<br>11m 39s oscillation period     |
| 0FFh     | 10         | 0.5Hz        | 125ms on, 1.875s off  | blink to 2s on<br>15m 56s oscillation period       |
| 180h     | 0Bh        | 0.33Hz       | 125ms on, 2.875s off  | blink to 3s on<br>24m 24s oscillation period       |
| 1FFh     | 40h        | 0.25Hz       | 1s on, 3s off         | 1s/3s on/off to 4s on<br>12m 48s oscillation cycle |

## 27.7 LED Registers

There are four instances of the [LED](#) block implemented in the MEC5035 enumerated as [0:2]. Each instance of the [LED](#) has its Base Address as indicated in [Table 27.3, "LED Base Address Table"](#).



Table 27.3 LED Base Address Table

| LED INSTANCE | LDN FROM<br>(Table 7.2 on page 167) | AHB BASE ADDRESS |
|--------------|-------------------------------------|------------------|
| LED.0        | 21h                                 | F0_8400h         |
| LED.1        |                                     | F0_8400h + 80h   |
| LED.2        |                                     | F0_8400h + 100h  |

Table 27.4 is a register summary for one instance of the LED block.

Table 27.4 LED Register Summary

| REGISTER NAME        | EC INTERFACE |           |         | NOTES |
|----------------------|--------------|-----------|---------|-------|
|                      | SPB OFFSET   | BYTE LANE | EC TYPE |       |
| LED Control Register | 00h          | 0         | R/W     |       |
| LED Rate Register    | 04h          | 3-0       | R/W     |       |

**Note:** It may take up to 30μs for a change to an LED register to take effect.

### 27.7.1 LED Control Register

The LED Control Register is used to control the behavior of each of the three output LEDs.

**Table 27.5 LED Control Register**

| HOST OFFSET   | N/A      |     |     |     | N/A        |       | HOST SIZE           |     |
|---------------|----------|-----|-----|-----|------------|-------|---------------------|-----|
| EC OFFSET     | 0h       |     |     |     | 32-bit     |       | EC SIZE             |     |
| POWER         | VTR      |     |     |     | 0000_0000h |       | nSYS_RST<br>DEFAULT |     |
| BUS           | EC SPB   |     |     |     |            |       |                     |     |
| BYTE[3:1] BIT | D31      | D30 | D29 | ... |            | D10   | D9                  | D8  |
| HOST TYPE     | R        | R   | R   | R   | R          | R     | R                   | R   |
| EC TYPE       | R        | R   | R   | R   | R          | R     | R                   | R   |
| BIT NAME      | Reserved |     |     |     |            |       |                     |     |
| BYTE0 BIT     | D7       | D6  | D5  | D4  | D3         | D2    | D1                  | D0  |
| HOST TYPE     | -        | -   | -   | -   | -          | -     | -                   | -   |
| EC TYPE       | R        | R   | R   | R   | R/W        | R/W   | R/W                 | R/W |
| BIT NAME      | Reserved |     |     |     |            | Synch | Control             |     |

### CONTROL

This bit controls the behavior of LED:

0= LED is always off

1= LED blinks, at a rate controlled by the [LED Rate Register](#)

2= LED breathes, at a rate controlled by the [LED Rate Register](#)

3= LED is always on

### SYNCH

When this bit is 1, all counters for all LEDs are reset to their initial values. When this bit is 0 in the [LED Control Register](#) for all LEDs, then all counters for LEDs that are configured to blink or breathe will increment or decrement, as required.

**APPLICATION NOTE:** To synchronize blinking or breathing, the [Synch](#) bit should be set for at least one LED, the [LED Control Register](#) and the [LED Rate Register](#) for each LED should be set to their required values, then the [Synch](#) bits should all be cleared. If the [LED Rate Registers](#) are set for the same blink period, they will all be synchronized.

## 27.7.2 LED Rate Register

The [LED Rate Register](#) is used to configure the blinking and breathing rate of each of the LEDs.



Table 27.6 LED Rate Register

|             |                   |     |     |     |                    |     |     |                     |  |
|-------------|-------------------|-----|-----|-----|--------------------|-----|-----|---------------------|--|
| HOST OFFSET | N/A               |     |     |     | N/A                |     |     | HOST SIZE           |  |
| EC OFFSET   | 04h               |     |     |     | 32-bit             |     |     | EC SIZE             |  |
| POWER       | VTR               |     |     |     | 0000_0000h         |     |     | nSYS_RST<br>DEFAULT |  |
| BUS         | EC SPB            |     |     |     |                    |     |     |                     |  |
| BYTE3 BIT   | D31               | D30 | D29 | D28 | D27                | D26 | D25 | D24                 |  |
| HOST TYPE   | -                 | -   | -   | -   | -                  | -   | -   | -                   |  |
| EC TYPE     | R                 | R   | R   | R   | R/W                | R/W | R/W | R/W                 |  |
| BIT NAME    | Reserved          |     |     |     | LED_Prescale[11:8] |     |     |                     |  |
| BYTE2 BIT   | D23               | D22 | D21 | D20 | D19                | D18 | D17 | D16                 |  |
| HOST TYPE   | -                 | -   | -   | -   | -                  | -   | -   | -                   |  |
| EC TYPE     | R/W               | R/W | R/W | R/W | R/W                | R/W | R/W | R/W                 |  |
| BIT NAME    | LED_Prescale[7:0] |     |     |     |                    |     |     |                     |  |
| BYTE1 BIT   | D15               | D14 | D13 | D12 | D11                | D10 | D9  | D8                  |  |
| HOST TYPE   | -                 | -   | -   | -   | -                  | -   | -   | -                   |  |
| EC TYPE     | R                 | R   | R   | R   | R                  | R   | R   | R                   |  |
| BIT NAME    | Reserved          |     |     |     |                    |     |     |                     |  |
| BYTE0 BIT   | D7                | D6  | D5  | D4  | D3                 | D2  | D1  | D0                  |  |
| HOST TYPE   | -                 | -   | -   | -   | -                  | -   | -   | -                   |  |
| EC TYPE     | R/W               | R/W | R/W | R/W | R/W                | R/W | R/W | R/W                 |  |
| BIT NAME    | LED_DutyCycle     |     |     |     |                    |     |     |                     |  |

**LED\_DUTYCYCLE[7:0]**

The field determines the duty cycle of the LED blink pattern. A value of 0 means full off, a value of FFh means full on.

**LED\_PRESCALE[11:0]**

If this field is 0, the 32.768KHz clock will be used to determine the blink period of LED: If this field is greater than 0, then the 32.768KHz clock will be divided by [LED\\_Prescale\[11:0\]+1](#)



## 27.8 LED Revision History

This revision history shows the changes made to this chapter.

**Table 27.7 LED Chapter Revision History**

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History," on page 539.</a> |              |      |                      |            |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------|----------------------|------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE | SECTION/FIGURE/ENTRY | CORRECTION |
| 1.                                                                                                                                                                                                                                          |              |      |                      |            |
| 2.                                                                                                                                                                                                                                          |              |      |                      |            |
| 3.                                                                                                                                                                                                                                          |              |      |                      |            |
| 4.                                                                                                                                                                                                                                          |              |      |                      |            |





## Chapter 28 PWM Controller

### 28.1 General Description

The function of this block is to generate a PWM output that may be used to control 4-wire fans, blink LEDs, etc. Each PWM can generate an arbitrary duty cycle output at frequencies from 0.125Hz to 32MHz.

The PWMx Counter ON Time registers and PWMx Counter OFF Time registers determine the operation of the PWM\_OUTPUT signal. See [Section 28.3.1, "PWMx Counter ON/OFF Time Registers," on page 482](#) for a description of the PWM\_OUTPUT signal.

#### 28.1.1 PWM\_OUTPUT

The PWM\_OUTPUT signal is used to generate a duty cycle at a frequency. This block has been designed such that the PWM signal may be programmed to hold PWM\_OUTPUT high, to hold PWM\_OUTPUT low, or to toggle PWM\_OUTPUT. If the PWM is configured to toggle, then PWM\_OUTPUT will alternate high and low for the programmed duration in the [PWMx Counter ON/OFF Time Registers](#) registers as defined in the register description. The PWM equations are described in [Figure 28.1](#).

The PWM pin signal functions are routed pins described in [Table 3.6, "Fan & Tachometer," on page 42](#).

#### 28.1.2 PWM Features

**APPLICATION NOTE:** Each PWM pin signal functions is muxed with a GPIO pin signal function. The pin's default signal function is GPIO input as controlled by the associated [Pin Control Register](#). (See [Chapter 17, "GPIO Interface," on page 366](#)). At VTR POR or when a WDT event occurs (see [Chapter 19, "Watchdog Timer Interface," on page 390](#)), the pin will tristate. For fan applications, an external resistor termination can provide the pin state to force the external fans to the full on state, thereby protecting the system from overheating.

#### 28.1.3 PWM Controller Block Diagram

|                                                                                                                                                                                                                                                                                                                                                                                       |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $\text{PWM Frequency} = \frac{1}{(\text{PreDeviver} + 1)} \times \frac{(\overline{\text{Clock Select}} * 64.52\text{MHz} \& \text{Clock Select} * 100\text{KHz})}{\text{PWM Counter OFF Time}[15:0] + \text{PWM Counter ON Time}[15:0]}$                                                                                                                                              |
| $\text{PWM Duty Cycle} = \frac{\text{PWM Counter ON Time}[15:0]}{\text{PWM Counter OFF Time}[15:0] + \text{PWM Counter ON Time}[15:0]}$                                                                                                                                                                                                                                               |
| <div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> <p><u>Legend:</u></p> <p>* = a Boolean AND operator</p> <p>&amp; = a Boolean OR operator</p> </div> <div style="width: 45%;"> <p><u>Notes:</u></p> <p>Clock Select, PreDeviver, PWM Counter OFF Time[15:0], and PWM Counter ON Time[15:0] are register values defined below.</p> </div> </div> |

**Figure 28.1 PWM Equations**

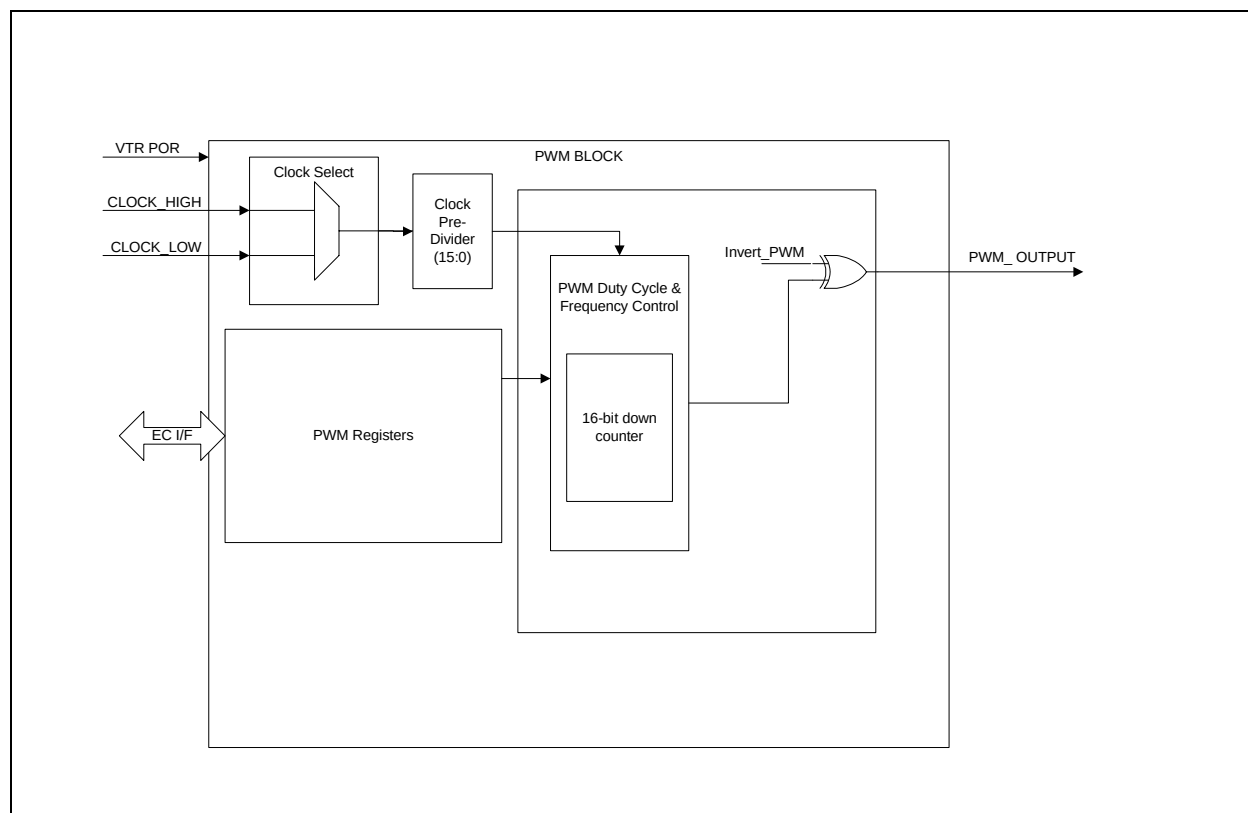


Figure 28.1 Block Diagram of PWM Controller

### 28.1.3.1 Block Diagram Signal List

Table 28.1 Block Diagram Signal List Description

| SIGNAL NAME | DIRECTION | DESCRIPTION                               |
|-------------|-----------|-------------------------------------------|
| VTR POR     | INPUT     | VTR Power on Reset.                       |
| CLOCK_HIGH  | INPUT     | 64.52MHz <a href="#">MCLK</a>             |
| CLOCK_LOW   | INPUT     | 100KHz <a href="#">MCLK_DIV640_EN</a>     |
| PWM_OUTPUT  | OUTPUT    | Pulse Width Modulated signal to PWMx pin. |
| E/C IF      | I/O Bus   | EC-side SPB bus                           |

## 28.2 Power, Clocks and Reset

### 28.2.1 Power Domain

This block is powered by the VTR Power Supply.

See [Section 4.5, "Power Configuration,"](#) on [page 96](#) for details on power domains.

## 28.2.2 Clocks

This block uses the [EC Bus Clock](#), the 64.52MHz [MCLK](#) and the 100KHz [MCLK\\_DIV640\\_EN](#). The [EC Bus Clock](#) is used when reading and writing the [PWM Controller](#) control registers. The individual PWM counters can be driven either by [MCLK](#) or [MCLK\\_DIV640\\_EN](#).

See [Section 4.4, "Clock Generator," on page 77](#) for details on clocks.

### 28.2.2.1 Pre-Divider

The clock source to the PWM Down Counter used to generate a duty cycle and frequency on the PWM\_OUTPUT may be pre-divided via bits D6:D3 in the [PWMx Configuration Register](#). This results in a wide range of frequencies for the pwm output. [Table 28.2](#) shows examples of frequencies supported

**Table 28.2 Example of PWM Frequencies Derived Using Pre-Divider**

| EXAMPLE | CLOCK SELECT | CLOCK PRE-DIVIDER | HIGH COUNT | LOW COUNT | PWM_OUTPUT FREQ | PWM_OUTPUT DUTY CYCLE |
|---------|--------------|-------------------|------------|-----------|-----------------|-----------------------|
| 1.      | 64.52MHz     | 0                 | 32768      | 32768     | 984Hz           | 50%                   |
| 2.      | 64.52MHz     | 0                 | 192        | 192       | 168kHz          | 50%                   |
| 3.      | 64.52MHz     | 0                 | 382        | 2         | 168kHz          | 99.5%                 |
| 4.      | 64.52MHz     | 0                 | 960        | 960       | 33.6kHz         | 50%                   |
| 5.      | 100KHz       | 0                 | 32767      | 32767     | 1.5Hz           | 50%                   |
| 6.      | 100KHz       | 1                 | 32767      | 32767     | 0.76Hz          | 50%                   |
| 7.      | 100KHz       | 11                | 32767      | 32767     | 0.12Hz          | 50%                   |

### 28.2.2.2 Sleep Enable

The Embedded Controller can put each PWM into a sleep state. When a PWM is in the sleep state the internal counters are reset to 0 and the internal state of the PWM and thus the PWM\_OUTPUT signal is set to the OFF state. The PWM participation in the sleep state is controlled by the [PWM1](#), [PWM2](#), [PWM3](#), [PWM4](#) bits in the ["EC Blocks Sleep Enables Register" on page 111](#).

## 28.2.3 Reset

This block is reset by [nSYS\\_RST](#). After the assertion of [nSYS\\_RST](#), PWM\_OUTPUT is held in the OFF state and the hardware resets the pwm counter registers to their default value.

See [Section 4.6, "Reset Interface," on page 99](#) for details on reset.

## 28.3 Registers

There are four instances of the [PWM Controller](#) block implemented in the MEC5035 enumerated [1:4]. Each instance of the [PWM Controller](#) has its Base Address as indicated in [Table 28.3, "PWMx Controller Base Address Table"](#):



Table 28.3 PWMx Controller Base Address Table

| PWM Controller INSTANCE | LDN FROM<br>(Table 7.3 on page 168) | AHB BASE ADDRESS           |
|-------------------------|-------------------------------------|----------------------------|
| PWM.1                   | 16h                                 | F0_5800h                   |
| PWM.2                   |                                     | F0_5880h = F0_5800h + 80h  |
| PWM.3                   |                                     | F0_5900h = F0_5800h + 100h |
| PWM.4                   |                                     | F0_5980h = F0_5800h + 180h |

Table 28.4 summarizes the registers allocated for each Instance. The offset field in the following table is the offset from the Embedded Controller (EC) Base Address.

Table 28.4 PWMx Register Summary

| REGISTER NAME                  | EC INTERFACE |           |         | NOTES |
|--------------------------------|--------------|-----------|---------|-------|
|                                | SPB OFFSET   | BYTE LANE | EC TYPE |       |
| PWMx Counter ON Time Register  | 00h          | 1-0       | R/W     |       |
| PWMx Counter OFF Time Register | 04h          | 1-0       | R/W     |       |
| PWMx Configuration Register    | 08h          | 1-0       | R/W     |       |

Table 28.5 PWMx EC Accessible Registers

| OFFSET | REGISTER NAME                  | VTR POR (SUSPEND) | FULL FAN RESET |
|--------|--------------------------------|-------------------|----------------|
| 0h     | PWMx Counter ON Time Register  | 0000h             | 0000h          |
| 4h     | PWMx Counter OFF Time Register | FFFFh             | 0000h          |
| 8h     | PWMx Configuration Register    | 0000h             | n/a            |

## 28.3.1 PWMx Counter ON/OFF Time Registers

**Table 28.6 PWMx Counter ON Time Register**

| HOST ADDRESS | n/a                        |     |     |     | n/a            |     | HOST SIZE                          |     |
|--------------|----------------------------|-----|-----|-----|----------------|-----|------------------------------------|-----|
| EC OFFSET    | 00h                        |     |     |     | 16-bit         |     | EC SIZE                            |     |
| POWER        | VTR                        |     |     |     | 0000h<br>0000h |     | nSYS_RST DEFAULT<br>FULL FAN RESET |     |
| BUS          | EC SPB                     |     |     |     |                |     |                                    |     |
| BIT          | D15                        | D30 | D29 | ... |                | D2  | D1                                 | D0  |
| HOST TYPE    | -                          | -   | -   | -   | -              | -   | -                                  | -   |
| EC TYPE      | R/W                        | R/W | R/W | R/W | R/W            | R/W | R/W                                | R/W |
| BIT NAME     | PWMx Counter ON Time[15:0] |     |     |     |                |     |                                    |     |

**Table 28.7 PWMx Counter OFF Time Register**

| HOST ADDRESS | n/a                         |     |     | n/a            |     |     | HOST SIZE                             |     |
|--------------|-----------------------------|-----|-----|----------------|-----|-----|---------------------------------------|-----|
| EC OFFSET    | 04h                         |     |     | 16-bit         |     |     | EC SIZE                               |     |
| POWER        | VTR                         |     |     | FFFFh<br>0000h |     |     | nSYS_RST<br>DEFAULT<br>FULL FAN RESET |     |
| BUS          | EC SPB                      |     |     |                |     |     |                                       |     |
| BIT          | D15                         | D30 | D29 | ...            |     | D2  | D1                                    | D0  |
| HOST TYPE    | -                           | -   | -   | -              | -   | -   | -                                     | -   |
| EC TYPE      | R/W                         | R/W | R/W | R/W            | R/W | R/W | R/W                                   | R/W |
| BIT NAME     | PWMx Counter OFF Time[15:0] |     |     |                |     |     |                                       |     |

The PWMx Counter ON/OFF Time registers determine both the duty cycle and frequency of the signal generated on PWM\_OUTPUT. See [Figure 28.2](#) and [Figure 28.3](#).

$$\text{PWM\_Frequency} = \frac{1}{(\text{PWM Counter OFF Time} + \text{PWM Counter ON Time})}$$

**Figure 28.2 Determining PWM Frequency**



$$\text{PWM\_DutyCycle} = \frac{\text{PWMCounter ON Time}}{(\text{PWM Counter OFF Time} + \text{PWM Counter ON Time})}$$

**Figure 28.3 Determining PWM Duty Cycle**

If the PWMx Counter OFF Time[15:0] is set to zero, PWM\_OUTPUT is held high (Full On). If the PWMx Counter ON Time is set to zero and the PWMx Counter OFF Time[15:0] is not set to zero, PWM\_OUTPUT is held low (Full Off). Note that the default case is full off. Otherwise, both the high and low count registers will contain a value that will be used to determine the length of time PWM\_OUTPUT will be held high and low. See [Table 28.8, "PWM\\_OUTPUT State"](#).

**Table 28.8 PWM\_OUTPUT State**

| PWM COUNT ON TIME | PWM COUNT OFF TIME | STATE OF PWM_OUTPUT |
|-------------------|--------------------|---------------------|
| Don't Care        | 0000h              | Full On             |
| 0000h             | Non-Zero Value     | Full Off            |
| Non-Zero Value    | Non-Zero Value     | Toggling On and Off |

The counter values preload a 16-bit down-counter that is clocked by either the high frequency clock source or the low frequency clock source (see bit[1] CLK\_Select of [PWMx Configuration Register](#)). The firmware will program the on and off count values that correspond to the PWM Current Duty Cycle and PWM Frequency. When PWM\_OUTPUT is OFF and the internal counter is zero, the PWMx Counter ON Time is loaded into the counter. The PWM\_OUTPUT signal will transition to the ON state and the internal counter will count down to zero at the programmed frequency for the duration of the programmed on time. Similarly, when the PWM\_OUTPUT is in the ON state and the internal counter is zero, the PWMx Counter OFF Time is loaded into the counter. The PWM\_OUTPUT signal will transition OFF and the internal counter will count down to zero at the programmed frequency for the duration of the programmed off time.

The [PWMx Counter ON/OFF Time Registers](#) may be updated at any time. Values written into the two registers are kept in holding registers. The holding registers are transferred into the [PWMx Counter ON/OFF Time Registers](#) when all four bytes have been written with new values and the internal counter completes the OFF time count. If the PWM is in the Full On state then the [PWMx Counter ON/OFF Time Registers](#) are updated from the holding registers as soon as all four bytes have been written. Once the two registers have been updated the holding registers are marked empty, and all four bytes must again be written before the holding registers will be reloaded into the [PWMx Counter ON/OFF Time Registers](#). Reads of the [PWMx Counter ON/OFF Time Registers](#) return the current contents of the registers that are used to load the counter and not the holding registers.

## 28.3.2 PWMx Configuration Register

**Table 28.9 PWMx Configuration Register**

| HOST ADDRESS | n/a      |                   |     |     | n/a    |        |              | HOST SIZE           |  |
|--------------|----------|-------------------|-----|-----|--------|--------|--------------|---------------------|--|
| EC OFFSET    | 08h      |                   |     |     | 16-bit |        |              | EC SIZE             |  |
| POWER        | VTR      |                   |     |     | 0000h  |        |              | nSYS_RST<br>DEFAULT |  |
| BUS          | EC SPB   |                   |     |     |        |        |              |                     |  |
| BYTE1 BIT    | D15      | D14               | D13 | D12 | D11    | D10    | D9           | D8                  |  |
| HOST TYPE    | -        | -                 | -   | -   | -      | -      | -            | -                   |  |
| EC TYPE      | R        |                   |     |     |        |        |              |                     |  |
| BIT NAME     | Reserved |                   |     |     |        |        |              |                     |  |
| BYTE0 BIT    | D7       | D6                | D5  | D4  | D3     | D2     | D1           | D0                  |  |
| HOST TYPE    | -        | -                 | -   | -   | -      | -      | -            | -                   |  |
| EC TYPE      | R        | R/W               | R/W | R/W | R/W    | R/W    | R/W          | R/W                 |  |
| BIT NAME     | Reserved | Clock Pre-Divider |     |     |        | Invert | Clock Select | PWM Enable          |  |

### PWM ENABLE

0= disabled (gates clocks to save power)

1= enabled (default)

**Note:** When the PWM enable bit is set to 0 the internal counters are reset and the internal state machine is set to the OFF state. In addition, the PWM\_OUTPUT signal is set to the inactive state as determined by the Invert bit. The [PWMx Counter ON/OFF Time Registers](#) are not affected by the PWM enable bit and may be read and written while the PWM enable bit is 0.

### CLOCK SELECT

The Clk\_Select bit determines the clock source used by the PWM duty cycle and frequency control logic.

0= 64.52MHz [MCLK](#) (default)

1= 100KHz [MCLK\\_DIV640\\_EN](#)

### INVERT

0= PWM\_OUTPUT ON State is active high

1= PWM\_OUTPUT ON State is active low



## Product Customer Specification-ODM

**CLOCK PRE-DIVIDER**

The Clock source for the 16-bit down counter (see [PWMx Counter ON/OFF Time Registers](#)) is determined by bit D1 of this register. The Clock source is then divided by the value of Pre-Divider+1 and the resulting signal determines the rate at which the down counter will be decremented. For example, a Pre-Divider value of 1 divides the input clock by 2 and a value of 2 divides the input clock by 3. A Pre-Divider of 0 will disable the Pre-Divider option.

## 28.4 PWM Controller Revision History

This revision history shows the changes made to this chapter.

**Table 28.10 PWM Controller Chapter Revision History**

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History," on page 539.</a> |              |            |                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                                     |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE       | SECTION/FIGURE/ENTRY                                                                                                                                                                                                                                                                                                                                                           | CORRECTION                                                                                                                                                                                                                                          |
| 1.                                                                                                                                                                                                                                          | 0.4          | 04/27/2007 | <a href="#">APPLICATION NOTE: on page 478</a>                                                                                                                                                                                                                                                                                                                                  | Added Application note.                                                                                                                                                                                                                             |
| 2.                                                                                                                                                                                                                                          |              |            | <a href="#">Section 28.1.2, "PWM Features," on page 478</a><br><a href="#">Table 28.1, "Block Diagram Signal List Description," on page 479</a><br><br><a href="#">Table 28.2, "Example of PWM Frequencies Derived Using Pre-Divider," on page 480</a><br><br><a href="#">Table 28.3, "PWMx Controller Base Address Table," on page 481</a><br><br><a href="#">Figure 28.1</a> | Full Fan port is tied off disabled. Make Full Fan Feature, Port engineering note. Remove from figure.<br><br><br>Updated frequencies from 64Mhz based to 64.52MHz.<br><br><br>Updated base addresses<br><br><br>Replace PWM equations with similar. |
| 3.                                                                                                                                                                                                                                          |              |            |                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                                     |
| 4.                                                                                                                                                                                                                                          |              |            |                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                                     |



## Chapter 29 TACH Monitor

### 29.1 General Description

This block is designed to monitor tach output signals or locked rotor signals from various types of fans to determine their speed. One mode returns the value in number of **CLOCK\_LOW** pulses. Another mode returns the value in pulses per programmed amount of time. This second mode can use the raw tach input. Each Tach is associated with a pair of limit registers that define maximum and minimum acceptable Tach counter values. If the readings on a Tach is outside these limits an interrupt to the EC can be generated.

In typical systems the fans are powered by the main power supply. Firmware may disable this block when it detects the main power rail has been turned off.

The TACH Monitor performs the following functions:

- Count the number of pulses detected on the raw tach input.
- Count the number of clocks for a programmed number of pulses.
- Generate an interrupt when the count value is latched into the reading register.
- Generate a programmable either-edge triggered interrupt for detecting when the tach input changes state. This may be used for Locked Rotor detection.
- Generate an interrupt when the count value latched into the reading register is greater than the high limit or less than the low limit

### 29.2 TACH Monitor Block Diagram

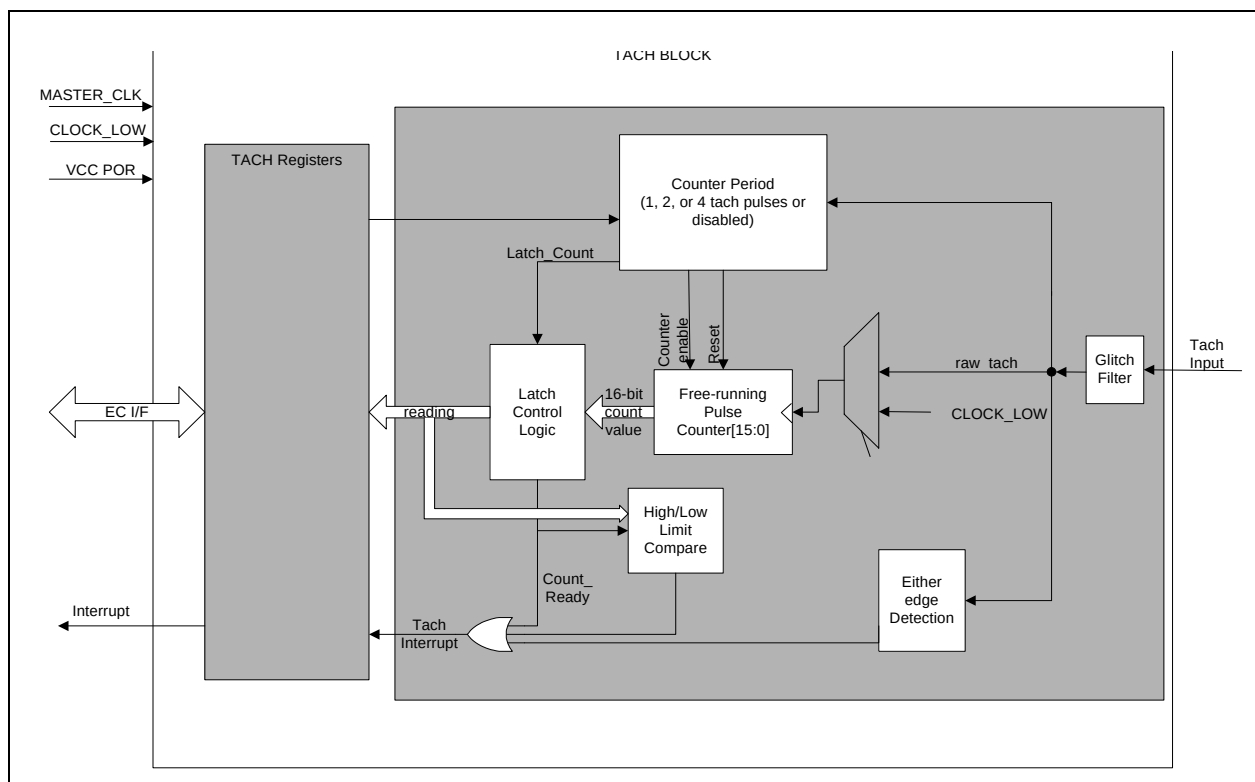


Figure 29.1 Block Diagram of TACH Monitor



## Product Customer Specification-ODM

**Note:** Once the counter is enabled it is a 16-bit free-running counter. Latch count value on a read or when number of tach pulses is detected (if enabled) for 1, 2, or 4 pulses. Counter is reset to 0000h if the count value is latched by a programmed number of tach pulses and on a VCC POR. Counter enable is software controlled signal.

## 29.3 Block Diagram Signal List

Table 29.1 TACH Port List

| SIGNAL NAME  | DIRECTION | DESCRIPTION                                                                                                            |
|--------------|-----------|------------------------------------------------------------------------------------------------------------------------|
| VTR POR      | INPUT     | nSYS_RST                                                                                                               |
| Master_Clock | INPUT     | 64.52MHz MCLK                                                                                                          |
| CLOCK_LOW    | INPUT     | 100KHz MCLK_DIV640_EN                                                                                                  |
| EC I/F       | I/O Bus   | EC-side SPB bus                                                                                                        |
| Tach Input   | INPUT     | Tachometer signal from TACHx Pin                                                                                       |
| Interrupts   | OUTPUT    | Interrupt used to indicate that either Tach Input has changed state or the TACH reading has been updated. One per TACH |

## 29.4 Power, Clocks and Reset

### 29.4.1 Power Domain

This block is powered by the VTR Power Supply.

See [Section 4.5, "Power Configuration," on page 96](#) for details on power domains.

### 29.4.2 Clocks

This block uses the [EC Bus Clock](#) and the 100KHz [MCLK\\_DIV640\\_EN](#). [EC Bus Clock](#) is used when reading and writing the [TACH Monitor](#) control registers. The individual TACH counters are driven by Clock\_Low, the [MCLK\\_DIV640\\_EN](#).

See [Section 4.4, "Clock Generator," on page 77](#) for details on clocks.

#### 29.4.2.1 Clock Idle

When the internal ring oscillator is disabled or when the TACH block is disabled, the internal TACH counters are reset. The reading register is not affected. This insures that inaccurate readings are not generated if the master clock halts in the middle of a TACH reading or when the TACH starts up.

**Note:** Each Tach pin should be pulled up via an external resistor to the main power supply.

### 29.4.3 Reset

This block is reset on a [nSYS\\_RST](#).

See [Section 4.6, "Reset Interface," on page 99](#) for details on reset.

## 29.5 TACH Interrupts

Each [TACH Monitor](#) in the MEC5035 can be used to generate one interrupt event. Each [TACH Monitor](#) interrupt source is a level, active high signal. The three [TACH Monitor](#) interrupts are routed to the [TACH3](#), [TACH2](#), & [TACH1](#) bits in [IRQ20 Source Register](#) on page 342. The [TACH Monitor](#) interrupts generate interrupt events.

## 29.6 TACH Circuitry

The TACH Circuitry is implemented as a pulse counter. There are two types of toggling signals that can be used to increment the counter: the raw tach input or [CLOCK\\_LOW](#). See [Figure 29.1, "Block Diagram of TACH Monitor" on page 486](#). The two modes for incrementing the counter are controlled by [Tach Reading Mode Select](#) in the [TACHx Control Register](#).

If the raw tach is used to increment the counter, the circuitry can be configured as a free-running counter that increments when a pulse from the tach is detected (i.e., input signal transitions from low-to-high). The counter is latched into the reading register ([Tachx Counter](#) in the [TACHx Control Register](#)) every time it is incremented. If this mode is selected, firmware will monitor the number of pulses detected over a period of time to determine the speed of the attached fan.

If [CLOCK\\_LOW](#) is used to increment the counter, the raw tach input will be used to determine when to latch the current count value into the reading register and reset the counter to 0000h. The counter is latched after a programmed number of tach pulses is detected. The programmed period can be configured to be 1, 2, or 4 tach pulses in duration.

Each Tach counter has comparison logic to compare the counter value with the high limit and low limit registers.

### 29.6.1 Tach Interrupt Sources

There are three interrupt source events: notify EC when reading is updated, notify EC when TACH input toggles, or notify EC when the TACH reading exceeds a programmed limit. The corresponding interrupt status bits are Count Ready Status Toggle Status Out-of-Limit Status Bits[3,1,0] in [TACHx Status Register](#) on page 492.

#### 29.6.1.1 Count Reading Ready Status

This status bit is asserted when the counter value is latched. The bit is implemented in Bit D3 of the [TACHx Control Register](#).

#### 29.6.1.2 Tach Input Toggle Status

This status bit is asserted when the Tach input changes state. The bit is implemented in Bit D2 of the [TACHx Control Register](#).

#### 29.6.1.3 TACH Out-of\_Limit STATUS

To generate a TACH out-of-limit status event, the high and low limits may be programmed in the [TACHx High Limit Register](#) and [TACHx Low Limit Register](#). An out-of-limit event is triggered when the reading register ([Tachx Counter](#) in the [TACHx Control Register](#)) is set to a value less than the [TACHx Low Limit Register](#) or to a value greater than the [TACHx High Limit Register](#). If the value in the [Tachx Counter](#) violates the programmed limits the TACH limit registers a status event will be generated, indicating the out-of-limit event. This status bit is implemented in Bit D0 of the [TACHx Status Register](#). This signal may be used to interrupt the Embedded Controller, if enabled via Bit D0 of the [TACHx Control Register](#).

**Note:** If the [TACHx Low Limit Register](#) is set to 0000h, no out-of-limit event will be triggered by a Tachx Counter value that is below the limit. If the [TACHx High Limit Register](#) is set to FFFFh, no out-of-limit event will be triggered by a Tachx Counter value that is above the limit.

## Product Customer Specification-ODM

**APPLICATION NOTE:** Out-of-Limit checks are typically only used when the tach counter is incremented in Mode 1 (in which the counter counts the number of [CLOCK\\_LOW](#) until a programmed number of pulses occur on the raw tach input).

## 29.7 Registers

There are three block instances defined in this chapter: TACH[1,2,3].

Each instance of the [TACH Monitor](#) has its own Logical Device Number, and Base Address as indicated in [Table 29.2](#).

**Table 29.2 TACH Monitor Base Address Table**

| TACH Monitor INSTANCES | LDN FROM<br>( <a href="#">Table 7.3 on page 168</a> ) | AHB BASE ADDRESS          |
|------------------------|-------------------------------------------------------|---------------------------|
| TACH0                  | 17h                                                   | F0_5C00h                  |
| TACH1                  |                                                       | F0_5C80h = F0_5C00h +80h  |
| TACH2                  |                                                       | F0_5D00h = F0_5C00h +100h |

[Table 29.3](#) is a register summary for one instance of the [TACH Monitor](#).

**Table 29.3 TACHx Register Summary**

| REGISTER NAME                             | EC INTERFACE |           |         | NOTES |
|-------------------------------------------|--------------|-----------|---------|-------|
|                                           | SPB OFFSET   | BYTE LANE | EC TYPE |       |
| <a href="#">TACHx Control Register</a>    | 00h          | 3-0       | R/W     |       |
| <a href="#">TACHx Status Register</a>     | 04h          | 0         | R/W     |       |
| <a href="#">TACHx High Limit Register</a> | 08h          | 1-0       | R/W     |       |
| <a href="#">TACHx Low Limit Register</a>  | 0Ch          | 1-0       | R/W     |       |

### 29.7.1 Detailed Description of Tachometer Register Values

This section describes the parameters that must be stored in hardware registers that will be used by the TACH logic.

### 29.7.1.1 TACHx Control Register

**Table 29.4 TACHx Control Register**

| HOST ADDRESS | n/a                           |                          |          |            | n/a        |                                   |                | HOST SIZE                          |  |
|--------------|-------------------------------|--------------------------|----------|------------|------------|-----------------------------------|----------------|------------------------------------|--|
| EC OFFSET    | 00h                           |                          |          |            | 32-bit     |                                   |                | EC SIZE                            |  |
| POWER        | VTR                           |                          |          |            | 0000_0000h |                                   |                | nSYS_RST<br>DEFAULT                |  |
| BUS          | EC SPB                        |                          |          |            |            |                                   |                |                                    |  |
| BYTE3 BIT    | D31                           | D30                      | D29      | D28        | D27        | D26                               | D25            | D24                                |  |
| HOST TYPE    | -                             | -                        | -        | -          | -          | -                                 | -              | -                                  |  |
| EC TYPE      | R                             | R                        | R        | R          | R          | R                                 | R              | R                                  |  |
| BIT NAME     | TACHx Counter [15:8] Register |                          |          |            |            |                                   |                |                                    |  |
| BYTE2 BIT    | D23                           | D22                      | D21      | D20        | D19        | D18                               | D17            | D16                                |  |
| HOST TYPE    | -                             | -                        | -        | -          | -          | -                                 | -              | -                                  |  |
| EC TYPE      | R                             | R                        | R        | R          | R          | R                                 | R              | R                                  |  |
| BIT NAME     | TACHx Counter [7:0] Register  |                          |          |            |            |                                   |                |                                    |  |
| BYTE1 BIT    | D15                           | D14                      | D13      | D12        | D11        | D10                               | D9             | D8                                 |  |
| HOST TYPE    | -                             | -                        | -        | -          | -          | -                                 | -              | -                                  |  |
| EC TYPE      | R/W                           | R/W                      | R/W      | R/W        | R/W        | R/W                               | R/W            | R/W                                |  |
| BIT NAME     | Tach Input<br>INT_EN          | Count<br>Ready<br>INT_EN | Reserved | Tach Edges |            | Tach<br>Reading<br>Mode<br>Select | Reserved       | Filter<br>Enable                   |  |
| BYTE0 BIT    | D7                            | D6                       | D5       | D4         | D3         | D2                                | D1             | D0                                 |  |
| HOST TYPE    | -                             | -                        | -        | -          | -          | -                                 | -              | -                                  |  |
| EC TYPE      | R                             | R                        | R        | R          | R          | R                                 | R/W            | R/W                                |  |
| BIT NAME     | Reserved                      |                          |          |            |            |                                   | TACH<br>Enable | Tach<br>Out-of-<br>Limit<br>Enable |  |

#### TACH OUT-OF-LIMIT ENABLE

The TACH Out-of\_Limit Enable is used to enable Bit[0] TACH Out-of\_Limit Status bit to generate an interrupt event.

0=disable interrupt output from tach block (default)

1=enable interrupt output from tach block

**Product Customer Specification-ODM****TACH ENABLE**

This bit enables the TACH logic.

0=TACH Idle (default)

This mode gates the clocks to the TACH block. The TACHx pin is tristate in the idle mode.

1=TACH Monitoring enabled.

**APPLICATION NOTE:** This bit gates the clocks into the block. When re-enabled, the internal counters will continue from the last known state and stale status events may still be pending. Firmware should discard any status or reading values until the reading value has been updated at least one time after the enable bit is set.

**FILTER ENABLE**

This filter is used to remove high frequency glitches from Tach Input. This filter must be disabled when the Tach synchronizing pulses are enabled for 3-wire fan support because tach pulses 1-2 **CLOCK\_LOW** wide would get filtered.

0=Filter disabled (default)

1=Filter enabled

**TACH READING MODE SELECT**

0 = Counter is incremented when Tach Input transitions from low-to-high state (default)

1 = Counter is incremented on the rising edge of the **CLOCK\_LOW** input. The counter is latched into **Tachx Counter** and reset when the programmed number of edges is detected.

**TACH EDGES**

A tach signal is a square wave with a 50% duty cycle. Typically, two tach periods represents one revolution of the fan. A tach period consists of three tach edges.

This programmed value represents the number of tach edges that will be used to determine the interval for which the number of **CLOCK\_LOW** pulses will be counted

00 = 2 Tach edges (1/2 tach period)

01 = 3 Tach edges (1 tach period)

10 = 5 Tach edges (2 tach periods)

01 = 9 Tach edges (4 tach periods)

**COUNT READY INT\_EN**

0=disable interrupt output from tach block (default)

1=enable interrupt output from tach block

**TACH INPUT INT\_EN**

0=disable interrupt output from tach block (default)

1=enable interrupt output from tach block

**TACHX COUNTER**

This 16-bit field contains the latched value of the tach counter, which may be configured to operate as a free-running counter or to be gated by the tach input signal.

If the counter is free-running (Mode 0), it increments (if enabled) at the rate determined by the raw tach signal and latched into this field every time it is incremented. The act of reading this field will not reset the counter, which rolls over to 0000h after FFFFh. The firmware will compute the delta between the current count reading and the previous count reading, to determine the number of pulses detected over a programmed period.



If the counter is being gated by the tach input and clocked by the [CLOCK\\_LOW](#) (Mode 1), the counter will be latched into the reading register when the programmed number of edges is detected or when the counter reaches FFFFh and the counter will be reset to zero.

**APPLICATION NOTE:** In Mode 1, a counter rate of FFFFh means that the tach did not detect the programmed number of edges in 655ms. A stuck fan can be detected by setting the [TACHx High Limit Register](#) to a number less than FFFFh. If the counter then reaches FFFFh, the reading register will be set to FFFFh and an out-of-limit interrupt can be sent to the EC.

### 29.7.1.2 TACHx Status Register

Table 29.5 TACHx Status Register

| HOST ADDRESS | n/a      |     |     | n/a    |                    |               | HOST SIZE           |                          |
|--------------|----------|-----|-----|--------|--------------------|---------------|---------------------|--------------------------|
| EC OFFSET    | 04h      |     |     | 32-bit |                    |               | EC SIZE             |                          |
| POWER        | VTR      |     |     | 0000h  |                    |               | nSYS_RST<br>DEFAULT |                          |
| BUS          | EC SPB   |     |     |        |                    |               |                     |                          |
| BYTE3-1 BIT  | D31      | D32 | D31 | ...    |                    | D10           | D9                  | D8                       |
| HOST TYPE    | -        | -   | -   | -      | -                  | -             | -                   | -                        |
| EC TYPE      | R        | R   | R   | R      | R                  | R             | R                   | R                        |
| BIT NAME     | Reserved |     |     |        |                    |               |                     |                          |
| BYTE0 BIT    | D7       | D6  | D5  | D4     | D3                 | D2            | D1                  | D0                       |
| HOST TYPE    | -        | -   | -   | -      | -                  | -             | -                   | -                        |
| EC TYPE      | R        | R   | R   | R      | R/WC               | R/WC          | R                   | R/WC                     |
| BIT NAME     | Reserved |     |     |        | Count Ready Status | Toggle Status | TACH Pin Status     | Tach Out-of-Limit Status |

#### TACH OUT-OF-LIMIT STATUS

This bit is set when the Tach Count value is greater than the high limit or less than the low limit. It is cleared when written with a 1. To disable this status event set the limits to their extreme values. If enabled via [TACH Out-of-Limit Enable](#) in the [TACHx Control Register](#), this status bit will assert the Interrupt signal, which may be enabled to cause an interrupt event to the embedded controller.

0=Tach Input is low  
1=Tach Input is high

#### TACH PIN STATUS

This bit reflects the state of Tach Input. This bit is a read only bit that may be polled by the embedded controller.

0=Tach Input is low  
1=Tach Input is high



## Product Customer Specification-ODM

**TOGGLE STATUS**

This bit is set when Tach Input changes state. It is cleared when written with a 1. If enabled via [Tach Input INT\\_EN](#) in the [TACHx Control Register](#), this status bit will assert the Interrupt signal, which may be enabled to cause an interrupt event to the embedded controller.

0=Tach stable (default)

1=Tach Input changed state (this bit is set on a low-to-high or high-to-low transition)

**APPLICATION NOTE:** Some fans offer a Locked Rotor output pin that generates a level event if a locked rotor is detected. This bit may be used in combination with the tach pin status bit to detect a locked rotor signal event from a fan.

**APPLICATION NOTE:** Tach Input may come up as active for Locked Rotor events. This would not cause an interrupt event because the pin would not toggle. Firmware must read the status events as part of the initialization process, if polling is not implemented.

**COUNT READY STATUS**

The [Count Ready Status](#) bit remains cleared to '0' when the [Tach Reading Mode Select](#) bit in the [TACHx Control Register](#) is clear to '0'.

When the [Tach Reading Mode Select](#) bit in the [TACHx Control Register](#) is set to '1', The [Count Ready Status](#) bit is set when the counter value is latched by the hardware. It is cleared when written with a 1. If enabled via the [Count Ready INT\\_EN](#) bit in the [TACHx Control Register](#), this status bit will assert the Interrupt signal, which may be enabled to cause an interrupt event to the embedded controller.

0=Reading not ready

1=Reading ready

**29.7.1.3 TACHx High Limit Register**

Table 29.6 TACHx High Limit Register

|               |                                  |     |     |        |     |     |                     |     |
|---------------|----------------------------------|-----|-----|--------|-----|-----|---------------------|-----|
| HOST ADDRESS  | n/a                              |     |     | n/a    |     |     | HOST SIZE           |     |
| EC OFFSETS    | 08h                              |     |     | 32-bit |     |     | EC SIZE             |     |
| POWER         | VTR                              |     |     | FFFFh  |     |     | nSYS_RST<br>DEFAULT |     |
| BUS           | EC SPB                           |     |     |        |     |     |                     |     |
| BYTE[3:2] BIT | D31                              | D30 | D29 | ...    |     | D18 | D17                 | D16 |
| HOST TYPE     | R                                | R   | R   | R      | R   | R   | R                   | R   |
| EC TYPE       | R                                | R   | R   | R      | R   | R   | R                   | R   |
| BIT NAME      | Reserved                         |     |     |        |     |     |                     |     |
| BYTE1-0 BIT   | D15                              | D30 | D29 | ...    |     | D2  | D1                  | D0  |
| HOST TYPE     | -                                | -   | -   | -      | -   | -   | -                   | -   |
| EC TYPE       | R/W                              | R/W | R/W | R/W    | R/W | R/W | R/W                 | R/W |
| BIT NAME      | TACHx High Limit [15:0] Register |     |     |        |     |     |                     |     |



The TACHx High Limit [15:0] value is compared with the value in the [TACHx Control Register](#). If the value in the [TACHx Control Register](#) is greater than the value programmed in the [TACHx High Limit Register](#) the TACH Out-of\_Limit STATUS bit will be set. The TACH Out-of-Limit status event may be enabled to generate an interrupt to the embedded controller via Bit[0] of the [TACHx Control Register](#).

**Note:** To disable this event program FFFFh into this register.

#### 29.7.1.4 TACHx Low Limit Register

**Table 29.7 TACHx Low Limit Register**

|              |                                 |     |     |        |     |     |                     |     |
|--------------|---------------------------------|-----|-----|--------|-----|-----|---------------------|-----|
| HOST ADDRESS | n/a                             |     |     | n/a    |     |     | HOST SIZE           |     |
| EC OFFSETS   | 0Ch                             |     |     | 32-bit |     |     | EC SIZE             |     |
| POWER        | VTR                             |     |     | 0000h  |     |     | nSYS_RST<br>DEFAULT |     |
| BUS          | EC SPB                          |     |     |        |     |     |                     |     |
| BYTE3-2 BIT  | D31                             | D32 | D31 | ...    |     | D18 | D17                 | D16 |
| HOST TYPE    | -                               | -   | -   | -      | -   | -   | -                   | -   |
| EC TYPE      | R                               | R   | R   | R      | R   | R   | R                   | R   |
| BIT NAME     | Reserved                        |     |     |        |     |     |                     |     |
| BIT          | D15                             | D30 | D29 | ...    |     | D2  | D1                  | D0  |
| HOST TYPE    | -                               | -   | -   | -      | -   | -   | -                   | -   |
| EC TYPE      | R/W                             | R/W | R/W | R/W    | R/W | R/W | R/W                 | R/W |
| BIT NAME     | TACHx Low Limit [15:0] Register |     |     |        |     |     |                     |     |

The TACHx Low Limit [15:0] value is compared with the value in the [Tachx Counter](#) Field of the [TACHx Control Register](#). If the value in the [Tachx Counter](#) Field is less than the value programmed in the [TACHx Low Limit Register](#) the TACH Out-of\_Limit STATUS bit will be set. The TACH Out-of-Limit status event may be enabled to generate an interrupt to the embedded controller via Bit[0] of the [TACHx Control Register](#).

To disable this event program 0000h into this register.



## 29.8 TACH Monitor Revision History

This revision history shows the changes made to this chapter.

**Table 29.8 TACH Monitor Chapter Revision History**

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History,"</a> on page 539. |              |             |                                                              |                                                                                                                                                                                 |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|-------------|--------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE        | SECTION/FIGURE/ENTRY                                         | CORRECTION                                                                                                                                                                      |
| 1.                                                                                                                                                                                                                                          |              |             |                                                              |                                                                                                                                                                                 |
| 1.                                                                                                                                                                                                                                          | 0.61         | 08//03/2007 | <a href="#">Count Ready Status on page 493</a>               | Added relationship of the <a href="#">Count Ready Status</a> bit to setting of the <a href="#">Tach Reading Mode Select</a> bit in the <a href="#">TACHx Control Register</a> . |
| 2.                                                                                                                                                                                                                                          | 0.61         | 08//03/2007 | <a href="#">Section 29.5, "TACH Interrupts," on page 488</a> | Tach interrupts do not cause wake events.                                                                                                                                       |
| 3.                                                                                                                                                                                                                                          |              |             |                                                              |                                                                                                                                                                                 |

## Chapter 30 PS/2 Device Interface

### 30.1 General Description

There are three PS/2 Ports in the MEC5035 independent EC PS/2 serial ports implemented in hardware which are directly controlled by the EC (see [Figure 30.1 on page 496](#)). The hardware implementation eliminates the need to bit bang I/O ports to generate PS/2 traffic, however bit banging is available via the associated GPIO's.

Each EC PS/2 serial channels use a synchronous serial protocol to communicate with the auxiliary device. Each PS/2 channel has Clock and Data signal lines. The signal lines are bi-directional and employ open drain outputs capable of sinking 16mA. A pull-up resistor, typically 10K, is connected to both lines. This allows either the MEC5035 EC PS/2 logic or the auxiliary device to drive the lines. Regardless of the drive source, the auxiliary device always provides the clock for transmit and receive operations. The serial packet is made up of eleven bits, listed in the order they appear on the data line: start bit, eight data bits (least significant bit first), odd parity, and stop bit. Each bit cell is from 60μS to 100μS long.

All PS/2 Serial Channel signals (CLK and DAT) are driven by open drain drivers which can be pulled to VTR or VCC (+3.3V nominal) through 10K-ohm resistors.

The MEC5035 supports a PS/2 Wake Interface that can wake the EC from the IDLE or SLEEP states. The PS/2 Wake Interface is powered by VCC1 and can generate wake interrupts without a clock.

**APPLICATION NOTE:** the PS/2 Wake Interface is only active when the KBC/Mouse and external pull-up resistors are powered by the VCC1supply. The external pull-up resistor must always be powered by the same source as the KBC/Mouse.

### 30.2 Block Diagram

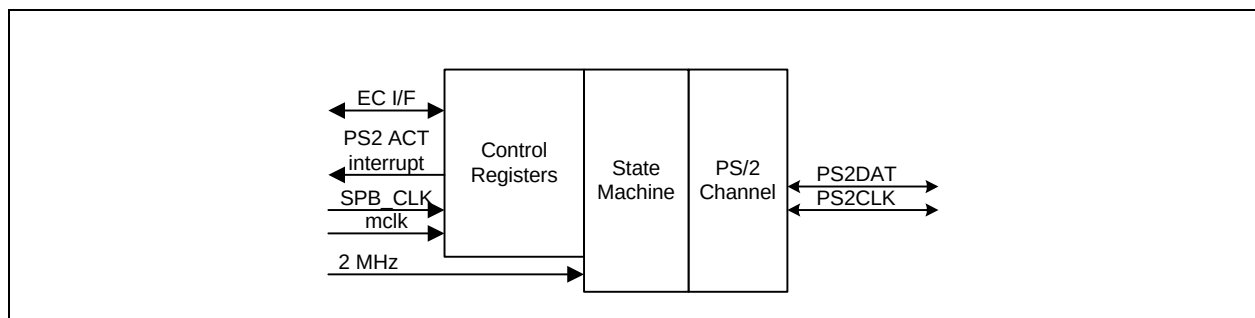


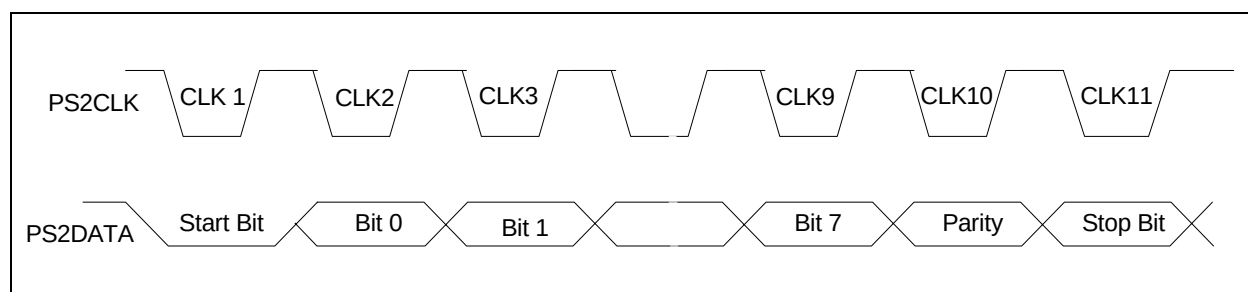
Figure 30.1 Port PS/2 Block Diagram

### 30.3 PS/2 Port Physical Layer Byte Transmission Protocol

The PS/2 physical layer transfers a byte of data via an eleven bit serial stream as shown in [Table 30.1](#). A logic 1 is sent at an active high level. Data sent from a Keyboard or mouse device to the host is read on the falling edge of the clock signal. The Keyboard or mouse device always generates the signal. The Host may inhibit communication by pulling the Clock line low. The Clock line must be continuously high for at least 50 microseconds before the Keyboard or mouse device can begin to transmit its data. See [Table 30.2, "PS/2 Port Physical Layer Bus States"](#).

**Table 30.1 PS/2 Port Physical Layer Byte Transmission Protocol**

| BIT | FUNCTION                           |
|-----|------------------------------------|
| 1   | Start bit (always 0)               |
| 2   | Data bit 0 (least significant bit) |
| 3   | Data bit 1                         |
| 4   | Data bit 2                         |
| 5   | Data bit 3                         |
| 6   | Data bit 4                         |
| 7   | Data bit 5                         |
| 8   | Data bit 6                         |
| 9   | Data bit 7 (most significant bit)  |
| 10  | Parity bit (odd parity)            |
| 11  | Stop Bit (always 1)                |

**Figure 30.2 PS/2 Port Physical Layer Byte Transmission Protocol****Table 30.2 PS/2 Port Physical Layer Bus States**

| DATA | CLOCK | STATE                   |
|------|-------|-------------------------|
| high | high  | Idle                    |
| high | low   | Communication Inhibited |
| low  | low   | Request to Send         |

## 30.4 Block Diagram Signal List

**Table 30.3 PS/2 Port List**

| SIGNAL NAME | DIRECTION    | DESCRIPTION                |
|-------------|--------------|----------------------------|
| PS2DAT      | Input/Output | Data from the PS/2 device  |
| PS2CLK      | Output       | Clock from the PS/2 device |

**Table 30.3 PS/2 Port List**

| SIGNAL NAME              | DIRECTION | DESCRIPTION                                                                                                                                                                                                           |
|--------------------------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <a href="#">nSYS_RST</a> | INPUT     | Chip Power on Reset (i.e., Suspend Well)                                                                                                                                                                              |
| SPB_CLK                  | INPUT     | Clock Source to EC micro controller. Used for reading/writing registers on the EC memory i/f.                                                                                                                         |
| mclk                     | INPUT     | <a href="#">MCLK</a>                                                                                                                                                                                                  |
| 2 MHz                    | INPUT     | <a href="#">MCLK_DIV32_EN</a> , State machine clock                                                                                                                                                                   |
| SLEEP_EN                 | Input     | External enable/disable signal used to put the block in the lowest power consumption state.<br>0=No Sleep Requested.<br>The block should operate as configured.<br>1=Sleep Requested.<br>The block enters sleep mode. |
| Clock Required           | Output    | This output indicates when this block requires this clock input.<br>0= CLOCK1 can be turned 'off' when appropriate<br>1= CLOCK1 is required to be 'on.'                                                               |
| EC Interface             | I/O Bus   | EC-side SPB bus                                                                                                                                                                                                       |
| PS2 ACT                  | Output    | Asynchronous Interrupt                                                                                                                                                                                                |

## 30.5 Power, Clocks and Reset

### 30.5.1 Power Domain

This block is powered by the VTR Power Supply.

See [Section 4.5, "Power Configuration," on page 96](#) for details on power domains.

### 30.5.2 Clocks

This block uses the [EC Bus Clock](#), the 64.52MHz [MCLK](#) and the 2MHz [MCLK\\_DIV32\\_EN](#). [EC Bus Clock](#) is used when reading and writing the [PS/2 Device Interface](#) registers. The state machine is clocked with [MCLK\\_DIV32\\_EN](#).

See [Section 4.4, "Clock Generator," on page 77](#) for details on clocks.

## 30.6 Reset

This block is reset on a [nSYS\\_RST](#).

See [Section 4.6, "Reset Interface," on page 99](#) for details on reset.

## 30.7 Instance Description

There are three block instances defined in this chapter: PS/2[0,1,2]. The pin signals are defined in [Table 3.10, "PS/2 Interface," on page 44](#). PS/2 ports ending with signal functions ending with "A" or "B" are muxed to a single controller. Only one Port set of clock and data are intended to be used at a time (either "A" or "B" not both.) The unused port segment should have its associated [Pin Control Register](#)'s, Mux Control Field programmed away from the PS2 controller. See [Chapter 17, "GPIO Interface," on page 366](#).

## 30.8 Interrupts

Each EC PS/2 Channel has two interrupts: a PS/2 activity interrupt event and a START Bit detection Wake-up event. Each PS/2 Channel activity interrupt event is generated by changes in status bits in this block. The PS/2 Channel activity interrupt event are routed to the [PS2\\_ACT\\_0](#), [PS2\\_ACT\\_1](#), [PS2\\_ACT\\_2](#) bits in the [IRQ23 Source Register on page 348](#). The START Bit detection Wake-up event is a PS/2 Channel/segment (see [Section 30.9](#)) Data pin signal edge detection interrupt and wake event. Each PS/2 Channel/segment START Bit detection Wake-up event is controlled by their associated Data pin's [Pin Control Register](#). (See [Chapter 17, "GPIO Interface," on page 366](#). The START Bit detection Wake-up events routed to the [PS2\\_WK\\_0A](#), [PS2\\_WK\\_0B](#), [PS2\\_WK\\_1A](#), [PS2\\_WK\\_1B](#), [PS2\\_WK\\_2](#) bits in the [IRQ23 Source Register on page 348](#)

**APPLICATION NOTE:** The pin control registers for a PS2 wakeup event should be programmed to Input, Falling Edge Triggered, non-inverted polarity detection.

## 30.9 Registers

There are three block instances defined in this chapter: PS/2[0,1,2]. The pin signals are defined in [Table 3.10, "PS/2 Interface," on page 44](#). PS/2 ports ending with signal functions ending with "A" or "B" are muxed to a single controller. Only one Port set of clock and data are intended to be used at a time (either "A" or "B" not both.) The unused port segment should have its associated [Pin Control Register's](#) Mux Control Field programmed away from the PS2 controller. (See [Chapter 17, "GPIO Interface," on page 366](#)).

Each instance of the [PS/2 Device Interface](#) has its Base Address as indicated in [Table 30.4](#).

**Table 30.4 PS/2 Device Interface Base Address Table**

| PS/2 Device Interface INSTANCE | LDN FROM<br>( <a href="#">Table 7.2 on page 167</a> ) | AHB BASE ADDRESS                                           |
|--------------------------------|-------------------------------------------------------|------------------------------------------------------------|
| <a href="#">PS/2.0</a>         | 22h                                                   | <a href="#">F0_8800h</a>                                   |
| <a href="#">PS/2.1</a>         |                                                       | <a href="#">F0_8880h</a> = <a href="#">F0_8800h</a> + 80h  |
| <a href="#">PS/2.2</a>         |                                                       | <a href="#">F0_8900h</a> = <a href="#">F0_8800h</a> + 100h |

[Table 30.5](#) is a register summary for each instance of the [PS/2 Device Interface](#).

**Table 30.5 PS/2 Device Interface Register Summary**

| REGISTER NAME                                 | EC INTERFACE |           |         | NOTES |
|-----------------------------------------------|--------------|-----------|---------|-------|
|                                               | SPB OFFSET   | BYTE LANE | EC TYPE |       |
| <a href="#">PS/2 Transmit Buffer Register</a> | 00h          | 0         | W       |       |
| <a href="#">PS/2 Receive Buffer Register</a>  | 00h          | 0         | R       |       |
| <a href="#">PS/2 Control Register</a>         | 04h          | 0         | R/W     |       |
| <a href="#">PS/2 Status Register</a>          | 08h          | 0         | R/WC    |       |

## 30.10 Detailed Description of Accessible Registers

### 30.10.1 PS/2 Transmit Buffer

**Table 30.6 PS/2 Transmit Buffer Register**

| HOST ADDRESS | NA                 |    |    |    |    |    | HOST SIZE |                     |
|--------------|--------------------|----|----|----|----|----|-----------|---------------------|
| EC OFFSET    | 00h                |    |    |    |    |    | 8-bit     | EC SIZE             |
| POWER        | VTR                |    |    |    |    |    | 00h       | nSYS_RST<br>DEFAULT |
| BUS          | EC SPB             |    |    |    |    |    |           |                     |
| BYTE0 BIT    | D7                 | D6 | D5 | D4 | D3 | D2 | D1        | D0                  |
| HOST TYPE    | -                  | -  | -  | -- | -  | -  | -         | -                   |
| EC TYPE      | W                  | W  | W  | W  | W  | W  | W         | W                   |
| BIT NAME     | Transmit Data[7:0] |    |    |    |    |    |           |                     |

#### TRANSMIT DATA

The byte written to this register, when PS2\_T/R and PS2\_EN in the [PS/2 Control Register](#) and XMIT\_IDLE in the [PS/2 Status Register](#) are set, is transmitted automatically by the PS/2 channel control logic. If any of these three bits (PS2\_T/R, PS2\_EN, and XMIT\_IDLE) are not set, then writes to this register are ignored. On successful completion of this transmission or upon a Transmit Time-out condition, the PS2\_T/R bit is automatically cleared and the XMIT\_IDLE bit is automatically set. The PS2\_T/R bit must be written to a '1' before initiating another transmission to the remote device.

#### Notes:

- Even if PS2\_T/R, PS2\_EN, and XMIT\_IDLE are all set, writing the Transmit Register will not start a transmission if RDATA\_RDY in the [PS/2 Status Register](#) is set. The automatic PS/2 logic forces data to be read from the Receive Register before allowing a transmission.
- An interrupt is generated on the low to high transition of XMIT\_IDLE.
- All bits of this register are write only.

### 30.10.2 PS/2 Receive Buffer

**Table 30.7 PS/2 Receive Buffer Register**

| HOST ADDRESS | NA                |    |    |    |       |    |    | HOST SIZE           |  |
|--------------|-------------------|----|----|----|-------|----|----|---------------------|--|
| EC OFFSET    | 00h               |    |    |    | 8-bit |    |    | EC SIZE             |  |
| POWER        | VTR               |    |    |    | FFh   |    |    | nSYS_RST<br>DEFAULT |  |
| BUS          | EC SPB            |    |    |    |       |    |    |                     |  |
| BYTE0 BIT    | D7                | D6 | D5 | D4 | D3    | D2 | D1 | D0                  |  |
| HOST TYPE    | -                 | -  | -  | -- | -     | -  | -  | -                   |  |
| EC TYPE      | R                 |    |    |    |       |    |    |                     |  |
| BIT NAME     | Receive Data[7:0] |    |    |    |       |    |    |                     |  |

#### RECEIVE DATA

When PS2\_EN=1 and PS2\_T/R=0 in the [PS/2 Control Register](#), the PS2 Channel is configured to automatically receive data on that channel (both the CLK and DATA lines will float waiting for the peripheral to initiate a reception by sending a start bit followed by the data bits). After a successful reception, data is placed in this register and the RDATA\_RDY bit in the [PS/2 Status Register](#) is set and the CLK line is forced low by the PS2 channel logic. RDATA\_RDY is cleared and the CLK line is released to high-z following a read of this register. This automatically holds off further receive transfers until the EC has had a chance to get the data.

#### Notes:

- The Receive Register is initialized to FFh after a read or after a Time-out has occurred.
- The channel can be enabled to automatically transmit data (PS2\_EN=1) by setting PS2\_T/R while RDATA\_RDY is set, however a transmission can not be kicked off until the data has been read from the Receive Register.
- An interrupt is generated on the low to high transition of RDATA\_RDY.
- If a receive time-out (REC\_TIMEOUT=1 in the [PS/2 Control Register](#)) or a transmit time-out (XMIT\_TIMEOUT=1 in the [PS/2 Control Register](#)) occurs the channel is busied (CLK held low) for 300us (Hold Time) to guarantee that the peripheral aborts. Writing to the Transmit Register will be allowed, however the data written will not be transmitted until the Hold Time expires.
- All bits in this register are read only

**Note 30.1** In receive mode the RX\_BUSY bit for a particular channel is set in the [PS/2 Status Register](#).



### 30.10.3 PS/2 Control

There are three PS/2 Control Registers, one for each channel.

**Table 30.8 PS/2 Control Register**

| HOST ADDRESS | NA       |    |      |     |        |     |        | HOST SIZE           |     |  |
|--------------|----------|----|------|-----|--------|-----|--------|---------------------|-----|--|
| EC OFFSET    | 04h      |    |      |     | 8-bit  |     |        | EC SIZE             |     |  |
| POWER        | VTR      |    |      |     | 00h    |     |        | nSYS_RST<br>DEFAULT |     |  |
| BUS          | EC SPB   |    |      |     |        |     |        |                     |     |  |
| BYTE0 BIT    | D7       | D6 | D5   | D4  | D3     | D2  | D1     | D0                  |     |  |
| HOST TYPE    | -        | -  | -    | -   | -      | -   | -      | -                   | -   |  |
| EC TYPE      | R        | R  | R/W  | R/W | R/W    | R/W | R/W    | R/W                 | R/W |  |
| BIT NAME     | Reserved |    | STOP |     | PARITY |     | PS2_EN | PS2_T/R             |     |  |

#### PS2\_T/R

PS/2 Channel Transmit/Receive (default = 0). Configures the PS2 logic for automatic transmission when set or reception when cleared. This bit is only valid when PS2\_EN is set.

When set the PS/2 channel is enabled to transmit data. To properly initiate a transmit operation, this bit must be set prior to writing to the Transmit Register. Writes to the Transmit Register are blocked when this bit is cleared. Upon setting the PS2\_T/R bit, the channel will drive its CLK line low and then float the DATA line and hold this state until a write occurs to the Transmit Register or until the PS2\_T/R bit is cleared. Writing to the Transmit Register initiates the transmit operation. MEC5035 drives the data line low and, within 80ns, floats the clock line (externally pulled high by the pull-up resistor) to signal to the external PS/2 device that data is now available. The PS2\_T/R bit is cleared on the 11th clock edge of the transmission or if a Transmit Time-out error condition occurs.

**Note:** If the PS2\_T/R bit is set while the channel is actively receiving data prior to the leading edge of the 10th (parity bit) clock edge, the receive data is discarded. If this bit is not set prior to the 10th clock signal, then the receive data is saved in the Receive Register.

When the PS2\_T/R bit is cleared, the PS/2 channel is enabled to receive data. Upon clearing this bit, if RDATA\_RDY is also cleared, the channel's CLK and DATA will float waiting for the external PS/2 device to signal the start of a transmission. If the PS2\_T/R bit is set while RDATA\_RDY is set, then the channel's DATA line will float but its CLK line will be held low, holding off the peripheral, until the Receive Register is read.

#### PS2\_EN

PS2 Channel ENable (default = 0). When PS2\_EN is set, the PS/2 State machine is enabled allowing the channel to perform automatic reception or transmission depending on the bit value of PS2\_T/R. When PS2\_EN is cleared, the channel's automatic PS/2 state machine is disabled and the PW/2 channel's CLK pin driven low and DATA pin not driven.

**Note:** If the PS2\_EN bit is cleared prior to the leading edge (falling edge) of the 10th (parity bit) clock edge the receive data is discarded (RDATA\_RDY remains low). If the PS2\_EN bit is cleared following the leading edge of the 10th clock signal, then the receive data is saved in the Receive Register (RDATA\_RDY goes high) assuming no parity error.



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**PARITY**

These bits are used to set the parity expected by the PS/2 channel state machine. These bits are therefore only valid when PS2\_EN is set.

00=Receiver expects Odd Parity (default).

01=Receiver expects Even Parity.

10=Receiver ignores level of the parity bit (10th bit is not interpreted as a parity bit).

11=Reserved

**STOP**

These bits are used to set the level of the stop bit expected by the PS/2 channel state machine. These bits are therefore only valid when PS2\_EN is set.

00=Receiver expects an active high stop bit.

01=Receiver expects an active low stop bit.

10=Receiver ignores the level of the Stop bit (11th bit is not interpreted as a stop bit).

11=Reserved.

**APPLICATION NOTE:** Changing values in the control register at a rate faster than 2 MHz, may result in unpredictable behavior.

This register should be read to determine the status of PS2\_T/R and PS2\_EN prior to clearing by writing a 1 to that bit.

**30.10.4 PS/2 Status****Table 30.9 PS/2 Status Register**

| HOST ADDRESS | NA                         |             |                       |               |      |      | HOST SIZE            |               |
|--------------|----------------------------|-------------|-----------------------|---------------|------|------|----------------------|---------------|
| EC OFFSET    | 08h                        |             |                       | 8-bit         |      |      | EC SIZE              |               |
| POWER        | VTR                        |             |                       | 10h           |      |      | nSYS_RST<br>DEFAULT  |               |
| BUS          | EC SPB                     |             |                       |               |      |      |                      |               |
| BYTE0 BIT    | D7                         | D6          | D5                    | D4            | D3   | D2   | D1                   | D0            |
| HOST TYPE    | -                          | -           | -                     | -             | -    | -    | -                    | -             |
| EC TYPE      | R/WC                       | R           | R/WC                  | R             | R/WC | R/WC | R/WC                 | R             |
| BIT NAME     | XMIT_<br>START_<br>TIMEOUT | RX_<br>BUSY | XMIT_<br>TIME-<br>OUT | XMIT_<br>IDLE | FE   | PE   | REC_<br>TIME-<br>OUT | RDATA_<br>RDY |

**APPLICATION NOTE:** This register should be read to determine the status of R/WC bits prior to clearing by writing a 1 to that bit.

**RDATA\_RDY**

Receive Data Ready: Under normal operating conditions, this bit is set following the falling edge of the 11th clock given successful reception of a data byte from the PS/2 peripheral (i.e., no parity, framing, or receive time-out errors) and indicates that the received data byte is available to be read from the Receive Register. This bit may also be set in the event that the PS2\_EN bit is cleared following the 10th CLK edge. Reading the Receive Register clears this bit.

**Note:** An Interrupt is generated on the low-to-high transition of the RDATA\_RDY bit.

#### **REC\_TIMEOUT**

Following assertion of the REC\_TIMEOUT bit, the channel's CLK line is automatically pulled low for a minimum of 300us until the PS/2 status register is read. Under PS2 automatic operation, PS2\_EN is set, this bit is set on one of three receive error conditions:

- When the receiver bit time (time between falling edges) exceeds 300us.
  - If the time from the first bit (start) to the 10th bit (parity) exceeds 2ms.
  - On a receive parity error along with the Parity Error (PE) bit.
  - On a receive framing error due to an incorrect STOP bit along with the framing error (FE) bit.
- The REC\_TIMEOUT bit is cleared when the Status Register is read.

**Note:** An Interrupt is generated on the low-to-high transition of the REC\_TIMEOUT bit.

#### **PE**

Parity Error: When receiving data, the parity bit is clocked in on the falling edge of the 10th CLK edge. If the channel is configured to expect either even or odd parity and the 10th bit is contrary to the expected parity, then the PE and REC\_TIMEOUT bits are set following the falling edge of the 10th CLK edge and an interrupt is generated.

#### **FE**

Framing Error: When receiving data, the stop bit is clocked in on the falling edge of the 11th CLK edge. If the channel is configured to expect either a high or low stop bit and the 11th bit is contrary to the expected stop polarity, then the FE and REC\_TIMEOUT bits are set following the falling edge of the 11th CLK edge and an interrupt is generated.

#### **XMIT\_IDLE**

Transmitter Idle: When low, the XMIT\_IDLE bit is a status bit indicating that the PS/2 channel is actively transmitting data to the PS2 peripheral device. Writing to the Transmit Register when the channel is ready to transmit will cause the XMIT\_IDLE bit to clear and remain clear until one of the following conditions occur: the falling edge of the 11th CLK, XMIT\_TIMEOUT is set; the PS2\_T/R bit is cleared or the PS2\_EN bit is cleared.

**Note 30.2** An interrupt is generated on the low-to-high transition of XMIT\_IDLE.

#### **XMIT\_TIMEOUT**

When the XMIT\_TIMEOUT bit is set, the PS2\_T/R bit is held clear, the PS/2 channel's CLK line is pulled low for a minimum of 300us until the PS/2 Status register is read. The XMIT\_TIMEOUT bit is set on one of three transmit conditions: when the transmitter bit time (time between falling edges) exceeds 300us, when the transmitter start bit is not received within 25ms from signaling a transmit start event or if the time from the first bit (start) to the 10th bit (parity) exceeds 2ms.

#### **RX\_BUSY**

When a RX\_BUSY bit is set, the associated channel is actively receiving PS/2 data; when a RX\_BUSY bit is clear, the channel is idle. See [Note 30.1 on page 501](#).

#### **XMIT\_START\_TIMEOUT**

When the XMIT\_START\_TIMEOUT bit is set, a start bit was not received within 25 ms following the transmit start event. Writing a '1' to the bit clears the XMIT\_START\_TIMEOUT bit. The XMIT\_START\_TIMEOUT bit is a 'sticky' bit and is intended to uniquely indicate the status of the transmit start bit time-out condition. These bit affect no other logic. Note that the transmit start bit time-out condition is also indicated by the XMIT\_TIMEOUT bit.

**PROGRAMMER'S NOTE:** Always check that an EC PS/2 channel is idle, i.e. the RX\_BUSY bit is clear, before attempting to transmit on that channel. Receive data may be lost by setting an EC PS/2

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channel to transmit while the RX\_BUSY bit is set depending where in the message frame the transmit mode change occurs.

## 30.11 PS/2 Device Interface Revision History

This revision history shows the changes made to this chapter.

**Table 30.10 PS/2 Device Interface Chapter Revision History**

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History,"</a> on page 539. |              |            |                                                      |                                                       |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------------|------------------------------------------------------|-------------------------------------------------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE       | SECTION/FIGURE/ENTRY                                 | CORRECTION                                            |
| 1.                                                                                                                                                                                                                                          | 0.4          | 04/27/2007 | <a href="#">Section 30.7, "Instance Description"</a> | ■ Added section to clarify instance naming convention |
| 2.                                                                                                                                                                                                                                          | 0.5          | 05/22/2007 | <a href="#">Table 30.3 on page 497</a>               | Swapped polarity of Clock Required signal.            |
| 3.                                                                                                                                                                                                                                          |              |            |                                                      |                                                       |
| 4.                                                                                                                                                                                                                                          |              |            |                                                      |                                                       |

## Chapter 31 SMB Device Interface

### 31.1 General Description

The MEC5035 [SMB Device Interface](#) includes two instances of an SMBus controller core: [SMBus 1](#) and [SMBus 2](#). This chapter describes aspects of the [SMB Device Interface](#) that are unique to the MEC5035 instantiations of this core; including, [Power Domain](#), [Resets](#), [Clocks](#), [Interrupts](#), [Registers](#) and the [Physical Interface](#). For a *General Description*, *Features*, *Block Diagram*, *Functional Description*, *Registers Interface* and other core-specific details, see Ref [1] (note: in this chapter, *italicized text* typically refers to SMBus controller core interface elements as described in Ref [1]).

#### 31.1.1 References

1. SMBus Controller Core Interface, Rev. 0.5, Core-Level Architecture Specification, SMSC, 3/27/07

#### 31.1.2 SMB Pin Signal Interface Description

The pin signals are defined in [Table 3.12, "SMBus Interface,"](#) on page 45.

### 31.2 Power, Clocks and Reset

#### 31.2.1 Power Domain

This block is powered by the VTR Power Supply.

See [Section 4.5, "Power Configuration,"](#) on page 96 for details on power domains. For more detail about the SMBus controller core Power Domain, see [Section 3.1, "Power Configuration"](#) in Ref [1].

#### 31.2.2 Clocks

This block uses the [EC Bus Clock](#), the 64.52MHz [MCLK](#) and the 8.06MHz [MCLK\\_DIV8\\_EN](#). The [EC Bus Clock](#) is used when reading and writing the [SMB Device Interface](#) control registers. [MCLK\\_DIV8\\_EN](#) is used when programming the *Bus Clock Register*, *Data Timing Register* and the *Time-Out Scaling Register* described in Ref [1]. [MCLK](#) is used as the [SMB Device Interface](#) Core Clock.

See [Section 4.4, "Clock Generator,"](#) on page 77 for details on the MEC5035 clocks. See [Section 3.3, "Clocking"](#), and [Chapter 2, "Hardware Interface"](#) in Ref [1] for a description of SMBus controller core Clocking.

#### 31.2.3 Resets

Both of the SMBus controller core instances in the MEC5035 [SMB Device Interface](#) are reset by [nSYS\\_RST](#).

See [Section 4.6, "Reset Interface,"](#) on page 99 for details on reset on the MEC5035. For more detail about SMBus controller core Resets, see [Section 3.2, "Reset Interface"](#) in Ref [1].

### 31.3 Interrupts

Each EC SMB Controller has both an activity interrupt event and a START Bit detection Wake-up event. The SMB activity interrupt events are routed to the [SMB1](#) & [SMB2](#), bits in the [IRQ12 Source Register](#) on page 325. The START Bit detection Wake-up events are routed to the [I2C1A WK](#), [I2C1B WK](#), [I2C1C WK](#), [I2C1D WK](#), [I2C1E WK](#), [I2C1F WK](#), [I2C1G WK](#), [I2C1H WK](#), [I2C1J WK](#), [I2C1K WK](#), [I2C2A WK](#), [I2C2B WK](#), [I2C2D WK](#), bits in the [IRQ23 Source Register](#) on page

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348. The edge detection of the interrupt and wake events are controlled by their associated pin control registers in the [Chapter 17, "GPIO Interface," on page 366](#)

**APPLICATION NOTE:** The pin control registers for a SMB wakeup event should be programmed to Input, Falling Edge Triggered, non-inverted polarity detection.

## 31.4 Registers

Each SMBus controller core instance in the MEC5035 [SMB Device Interface](#) has unique Register Interface Addressing, defined by a base address as indicated in [Table 31.1](#). For more detail about SMBus controller core registers, see [Chapter 5, "Registers Interface"](#) in Ref [1].

**Table 31.1 SMB Device Interface Base Address Table**

| SMB Device Interface INSTANCE | LDN FROM<br>(Table 7.3 on page 168) | AHB BASE ADDRESS          |
|-------------------------------|-------------------------------------|---------------------------|
| SMBus.0                       | 6h                                  | F0_1800h                  |
| SMBus.1                       |                                     | F0_1880h = F0_1800h + 80h |

## 31.5 Physical Interface

### 31.5.1 Overview

The [Physical Interface](#) for the [SMBus 1](#) controller core includes ten ports as defined below in [Section 31.5.2](#); [SMBus 2](#) includes four ports as defined below in [Section 31.5.3](#). The port signal-function names and pin numbers are defined in [Table 3.12, "SMBus Interface," on page 45.](#) The [SMB Device Interface](#) port selection is made using the *PORT SEL [3:0]* bits in the *Configuration Register* as described in Ref [1] and in the subsections that follow.

For [SMB Device Interface](#) port signal functions that are alternate functions of GPIO pins, the buffer type for these pins must be configured as open-drain outputs when the port is selected as defined in [Section 31.5.2](#) and [Section 31.5.3](#), below. For more information regarding the SMBus controller core [Physical Interface](#), see [Section 2.2, "Physical Interface"](#) in Ref [1].

### 31.5.2 SMBus 1

[SMBus 1 Port Selection](#) is defined below in [Table 31.2](#).

**Table 31.2 SMBus 1 Port Selection**

| PORT SEL [3:0] |   |   |   | PORT (Note 31.1) |
|----------------|---|---|---|------------------|
| 3              | 2 | 1 | 0 |                  |
| 0              | 0 | 0 | 0 | I2C1A            |
| 0              | 0 | 0 | 1 | I2C1B            |
| 0              | 0 | 1 | 0 | I2C1C            |
| 0              | 0 | 1 | 1 | I2C1D            |

**Table 31.2 SMBus 1 Port Selection**

| PORT SEL [3:0] |   |   |   | PORT (Note 31.1) |
|----------------|---|---|---|------------------|
| 3              | 2 | 1 | 0 |                  |
| 0              | 1 | 0 | 0 | I2C1E            |
| 0              | 1 | 0 | 1 | I2C1F            |
| 0              | 1 | 1 | 0 | I2C1G            |
| 0              | 1 | 1 | 1 | I2C1H            |
| 1              | 0 | 0 | 0 | I2C1J            |
| 1              | 0 | 0 | 1 | I2C1K            |
| 1010b - 1111b  |   |   |   | Reserved         |

**Note 31.1** see [Table 3.12, "SMBus Interface,"](#) on page 45 for pin interface."

### 31.5.3 SMBus 2

[SMBus 2 Port Selection](#) is defined below in [Table 31.3](#).

**Table 31.3 SMBus 2 Port Selection**

| PORT SEL [3:0] |   |   |   | PORT (Note 31.1) |
|----------------|---|---|---|------------------|
| 3              | 2 | 1 | 0 |                  |
| 0              | 0 | 0 | 0 | I2C2A            |
| 0              | 0 | 0 | 1 | I2C2B            |
| 0              | 0 | 1 | 0 | I2C2C            |
| 0              | 0 | 1 | 1 | I2C2D            |
| 0100b - 1111b  |   |   |   | Reserved         |

## 31.6 SMB Device Interface Revision History

This revision history shows the changes made to this chapter.

**Table 31.4 SMB Device Interface Chapter Revision History**

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History,"</a> on page 539. |              |      |                      |            |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------|----------------------|------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE | SECTION/FIGURE/ENTRY | CORRECTION |
| 1.                                                                                                                                                                                                                                          |              |      |                      |            |
| 2.                                                                                                                                                                                                                                          |              |      |                      |            |

**Table 31.4** SMB Device Interface Chapter Revision History

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History," on page 539.</a> |              |      |                      |            |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------|----------------------|------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE | SECTION/FIGURE/ENTRY | CORRECTION |
| 3.                                                                                                                                                                                                                                          |              |      |                      |            |
| 4.                                                                                                                                                                                                                                          |              |      |                      |            |



## Chapter 32 SMSC BC-Link Master

### 32.1 General Description

The function of this block is to provide SMSC BC\_Link™ to a slave device. The SMSC BC\_Link™ protocol includes a start bit to signal the beginning of a message, and a turnaround (TAR) period for bus transfer between the Master and Companion devices. The SMSC BC\_Link™ protocol is defined in SMSC BC-Link (TM) Specification, Revision1.02, dated September 05, 2007.

**Note:** A weak pull-up resistor is recommended on the data line (100KΩ).

There are three instances of the BC\_Link Master interface in the MEC5035. Instance A, B, and C are high speed BC-links with high speed buffers attached. Instance D is a low speed BC\_link which uses 8 ma buffer. Instance D consists of signals LSBCM\_D\_INT#, LSBCM\_D\_DAT, LSBCM\_D\_CLK.

The maximum usable clock frequency for Instances A, B and C is 12MHz. The maximum clock frequency of Instance D is 3MHz. Instance D can be used for ribbon cable applications; in this configuration, the clock frequency on LSBCM\_D\_CLK should be programmed to 1.5Mhz. The clock speed for each instance is set with each instance's [BBC Clock Select Register](#).

**Note:** A weak pull-up resistor is recommended on the data line (100KΩ).

## 32.2 Block Diagram

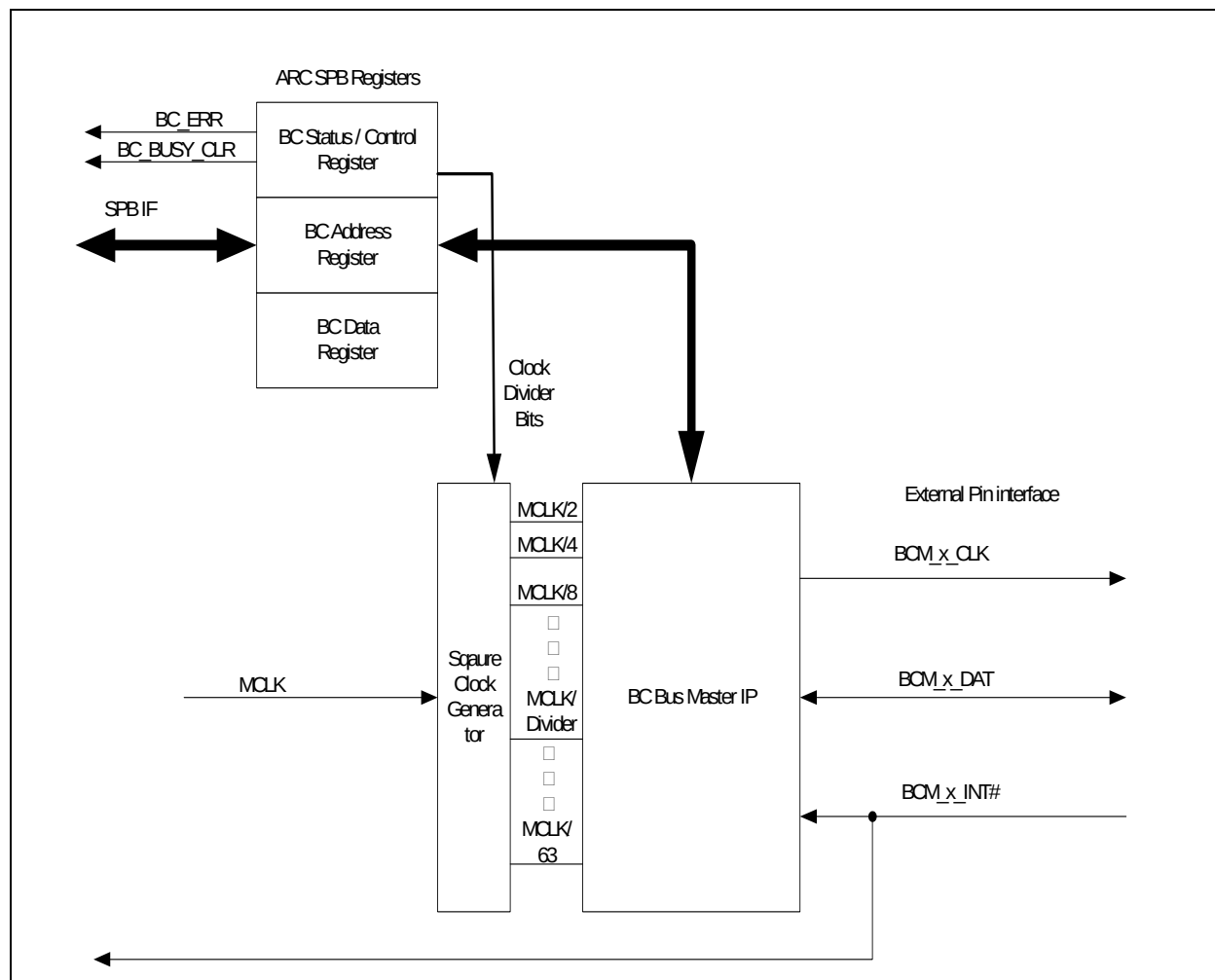


Figure 32.1 BC-LINK Master Block Diagram

## 32.3 Signal List

Table 32.1 BC-Link Signal List

| SIGNAL NAME | DIRECTION    | DESCRIPTION                                               |
|-------------|--------------|-----------------------------------------------------------|
| BCM_x_CLK   | OUTPUT       | 64MHz - 252KHz output clock, where x is A, B,C or D.      |
| BCM_x_DAT   | INPUT/OUTPUT | Bidirectional data line, where x is A, B,C or D.          |
| BMM_x_INT#  | INPUT        | Input from the companion device, where x is A, B,C or D.. |
| BC_ERR      | OUTPUT       | BC-Link master error interrupt                            |
| BC_BUSY_CLR | OUTPUT       | BC-Link master Busy Clear interrupt                       |
| MCLK        | INPUT        | 64 MHz Master clock                                       |
| SPBIF       | I/O Bus      | Bus used for register access                              |

**Note:** The Low Speed BC-Link Master Block has an identical organization, but the external signals are LSBCM\_D\_CLK, LSBCM\_D\_DAT and LSBCM\_D\_INT#.

See [Table 3.4, "BC-Link Interface," on page 41](#) for the pin interface

## 32.4 Power, Clocks and Reset

### 32.4.1 Power Domain

This block is powered by the VTR Power Supply.

See [Section 4.5, "Power Configuration," on page 96](#) for details on power domains.

### 32.4.2 Clocks

This block uses the [EC Bus Clock](#) and the 64.52MHz ([MCLK](#)). The [EC Bus Clock](#) is used to access the [Registers](#) described in this block. [MCLK](#) is divided down to generate the external bus clock.

See [Section 4.4, "Clock Generator," on page 77](#) for details on clocks.

### 32.4.3 Power On Reset

This block is reset on a [nSYS\\_RST](#). On reset, the BC-Link state machine transitions to the Idle state and waits for the address and data registers to be written.

See [Section 4.6, "Reset Interface," on page 99](#) for details on reset.

## 32.5 Interrupts

Each [SMSC BC-Link Master](#) instance has three interrupts events [BC\\_BUSY\\_CLR](#), [BC\\_ERR](#), & [BC\\_INT#](#). The [SMSC BC-Link Master](#) [BC\\_BUSY\\_CLR](#) and [BC\\_ERR](#) interrupt are generated by changes to the [BC-Link Status Register](#). The [BC\\_INT#](#) is an active low level interrupt generated by input pin signal function. The edge detection of the interrupt and wake events are controlled by their associated pin control registers in the [Chapter 17, "GPIO Interface," on page 366](#)

The [SMSC BC-Link Master](#) block Instance A are routed to the [BCM\\_BUSY\\_CLR\[A\]](#), [BCM\\_ERR\[A\]](#), & [BCM\\_INT#\[A\]](#) bits in the [IRQ21 Source Register on page 344](#). The [SMSC BC-Link Master](#) block Instance B are routed to the [BCM\\_BUSY\\_CLR\[B\]](#), [BCM\\_ERR\[B\]](#), & [BCM\\_INT#\[B\]](#) bits in the [IRQ21 Source Register on page 344](#). The [SMSC BC-Link Master](#) block Instance C are routed to the [BCM\\_BUSY\\_CLR\[C\]](#), [BCM\\_ERR\[C\]](#), & [BCM\\_INT#\[C\]](#) bits in the [IRQ21 Source Register on page 344](#). The [SMSC BC-Link Master](#) block Instance D are routed to the [BCM\\_BUSY\\_CLR\[D\]](#), [BCM\\_ERR\[D\]](#), & [BCM\\_INT#\[D\]](#) bits in the [IRQ21 Source Register on page 344](#).

### 32.5.1 Instance Buffers vs Clock

There are four instances of the [SMSC BC-Link Master](#) block implemented in the MEC5035 enumerated as A, B, C, D. [Table 3.4, "BC-Link Interface," on page 41](#) list the pin functions for all instances. The base address for all instances are listed in [Table 32.3, "SMSC BC-Link Master Base Address Table"](#).

Instance A, B, & C are high speed BC-links with higher current buffers driving the external signals. Instance D is a low speed BC-link, which is implemented lower current buffers. Signal names for the high speed interfaces are [BCM\[A,B,C\]\\_CLK](#), [BCM\[A,B,C\]\\_DAT](#) and [BCM\[A,B,C\]\\_INT#](#). Signal names for the low speed instance are [LSBCM\\_D\\_CLK](#), [LSBCM\\_D\\_DAT](#) and [LSBCM\\_D\\_INT#](#).

**Note:** For ribbon cable applications, the Low Speed BC-Link Master should be used with a maximum clock frequency of 3Mhz. Clock frequency is set with the [BBC Clock Select Register](#).



Table 32.2 SMSC BC-Link Master Pin Interface

| PIN             | DESCRIPTION                                     | BUFFER                            | MAX FREQ | MIN VALUE IN BBC Clock Select Register |
|-----------------|-------------------------------------------------|-----------------------------------|----------|----------------------------------------|
| BCM[A,B,C]_CLK  | High Speed Clock supplied by the MEC5035 Device | O16                               | 12Mhz    | 4                                      |
| BCM[A,B,C]_DAT  | High Speed Data Line                            | IO16<br><a href="#">Note 32.1</a> |          |                                        |
| BCM[A,B,C]_INT# | Interrupt signal                                | I                                 |          |                                        |
| LSBCM_D_CLK     | Low Speed Clock supplied by the MEC5035 Device  | O16                               | 3MHz     | 21                                     |
| LSBCM_D_DAT     | Data Line                                       | IO16<br><a href="#">Note 32.1</a> |          |                                        |
| LSBCM_D_INT     | Interrupt signal                                | I                                 |          |                                        |

**Note 32.1** This requires a weak pull up (100K)

## 32.6 Registers

Table 32.3 SMSC BC-Link Master Base Address Table

| BC-LINK INSTANCES | LDN FROM<br>( <a href="#">Table 7.3</a><br>on<br><a href="#">page 168</a> ) | AHB BASE ADDRESS                      |
|-------------------|-----------------------------------------------------------------------------|---------------------------------------|
| BC-LINK.A         | 5h                                                                          | <a href="#">F0_1400h</a>              |
| BC-LINK.B         |                                                                             | $F0\_1480h = \text{F0\_1400h} + 80h$  |
| BC-Link.C         |                                                                             | $F0\_1500h = \text{F0\_1400h} + 100h$ |
| BC-Link.D         |                                                                             | $F0\_1580h = \text{F0\_1400h} + 180h$ |

Table 32.4 SMSC BC-Link Master Register Summary

| REGISTER NAME                             | EC INTERFACE |           |         | NOTES |
|-------------------------------------------|--------------|-----------|---------|-------|
|                                           | SPB OFFSET   | BYTE LANE | EC TYPE |       |
| <a href="#">BC-Link Status Register</a>   | 00h          | 3-0       | R/W     |       |
| <a href="#">BC-Link Address Register</a>  | 04h          | 0         | R/W     |       |
| <a href="#">BC-Link Data Register</a>     | 08h          | 1-0       | R/W     |       |
| <a href="#">BBC Clock Select Register</a> | 0Ch          | 1-0       | R/W     |       |

## 32.6.1 BC-Link Status

**Table 32.5 BC-Link Status Register**

| HOST ADDRESS | N/A    |        |               |                    |          |    |    | HOST SIZE           |
|--------------|--------|--------|---------------|--------------------|----------|----|----|---------------------|
| EC OFFSET    | 00h    |        |               |                    | 8-bit    |    |    | EC SIZE             |
| POWER        | VCC    |        |               |                    | 81h      |    |    | nSYS_RST<br>DEFAULT |
| BUS          | EC SPB |        |               |                    |          |    |    |                     |
| BYTE3 BIT    | D7     | D6     | D5            | D4                 | D3       | D2 | D1 | D0                  |
| HOST TYPE    | -      | -      | -             | -                  | -        | -  | -  | -                   |
| EC TYPE      | R/W    | R/WC   | R/W           | R/W                | R        | R  | R  | R/W                 |
| BIT NAME     | RESET  | BC_ERR | BC_ERR_INT_EN | BC_Busy_CLR_INT_EN | Reserved |    |    | BUSY                |

### BUSY

This bit is asserted when the BC interfaces are transferring data and on reset. Otherwise it is asserted 0. When **BUSY** is cleared by hardware, a positive edge interrupt is generated.

### BC\_BUSY\_CLR\_INT\_EN

Enable signal for **BC\_**. When asserted 1, the interrupt signal is enabled. When 0 the interrupt is disabled. When enabled this interrupt occurs after a BC Bus read or write. [Figure 32.2](#) show when the interrupt is generated when enabled.

### BC\_ERR\_INT\_EN

Enable signal for **BC\_**. When asserted 1, the interrupt signal is enabled. When 0 the interrupt is disabled. The **BC\_** bit will be set, the interrupt will not be generated. [Figure 32.2](#) show when the interrupt is generated when enabled.

### BC\_ERR

This bit indicates that a Bus Error has occurred. This is a high level interrupt Software clears this bit when the interrupt is processed. This bit is cleared by writing a 1 to bit 6 in this register.

Errors that cause this interrupt are: Bad Data received by the BASE (CRC Error) or a time-out caused by the COMPANION not responding. All COMPANION errors cause the COMPANION to abort the operation and cause the BASE to time-out. [Figure 32.2](#) shows the timing of this interrupt.

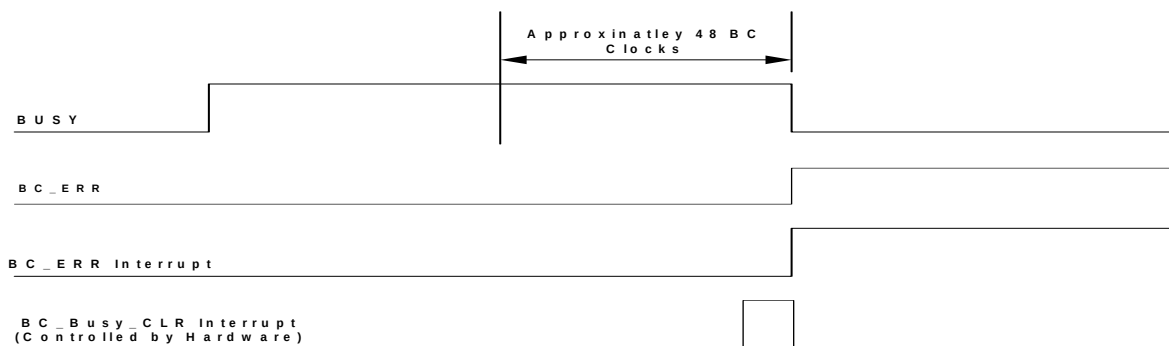


Figure 32.2 BC Bus BC\_ERR Interrupt Timing

**Note 32.3** When the **BC\_** bit is set. The BASE will continue to clock the interface with the data line high to assure the COMPANION interface returns to idle.

#### RESET

Asserted 1 the BASE BC Interface will be reset and be held in reset until this bit is de-asserted. Reset causes the **BUSY** bit to be set and will not be cleared until the reset operation of the BC Interface is completed (proximately 48 BC clocks).

**PROGRAMMER'S NOTE:** The de-assertion of the **BUSY** bit on reset will not generate an interrupt, even if the **BC\_** is asserted 1. The **BUSY** bit must be polled.

## 32.6.2 BC-Link Address

Table 32.6 BC-Link Address Register

| HOST ADDRESS | N/A          |     |     |       |     |     | HOST SIZE           |     |
|--------------|--------------|-----|-----|-------|-----|-----|---------------------|-----|
| EC OFFSET    | 04h          |     |     | 8-bit |     |     | EC SIZE             |     |
| POWER        | VCC          |     |     | 00h   |     |     | nSYS_RST<br>DEFAULT |     |
| BUS          | EC SPB       |     |     |       |     |     |                     |     |
| BYTE3 BIT    | D7           | D6  | D5  | D4    | D3  | D2  | D1                  | D0  |
| HOST TYPE    | -            | -   | -   | -     | -   | -   | -                   | -   |
| EC TYPE      | R/W          | R/W | R/W | R/W   | R/W | R/W | R/W                 | R/W |
| BIT NAME     | Address[7:0] |     |     |       |     |     |                     |     |

### 32.6.3 BC-Link Data

Table 32.7 BC-Link Data Register

| HOST ADDRESS | N/A       |     |     |       |     |     | HOST SIZE           |     |
|--------------|-----------|-----|-----|-------|-----|-----|---------------------|-----|
| EC OFFSET    | 08h       |     |     | 8-bit |     |     | EC SIZE             |     |
| POWER        | VCC       |     |     | 00h   |     |     | nSYS_RST<br>DEFAULT |     |
| BUS          | EC SPB    |     |     |       |     |     |                     |     |
| BYTE3 BIT    | D7        | D6  | D5  | D4    | D3  | D2  | D1                  | D0  |
| HOST TYPE    | -         | -   | -   | -     | -   | -   | -                   | -   |
| EC TYPE      | R/W       | R/W | R/W | R/W   | R/W | R/W | R/W                 | R/W |
| BIT NAME     | Data[7:0] |     |     |       |     |     |                     |     |

### 32.6.4 BC Clock Select

Table 32.8 BBC Clock Select Register

| HOST ADDRESS | N/A          |     |     |       |     |     | HOST SIZE           |     |
|--------------|--------------|-----|-----|-------|-----|-----|---------------------|-----|
| EC OFFSET    | 0Ch          |     |     | 8-bit |     |     | EC SIZE             |     |
| POWER        | VCC          |     |     | N = 4 |     |     | nSYS_RST<br>DEFAULT |     |
| BUS          | EC SPB       |     |     |       |     |     |                     |     |
| BYTE3 BIT    | D7           | D6  | D5  | D4    | D3  | D2  | D1                  | D0  |
| HOST TYPE    | -            | -   | -   | -     | -   | -   | -                   | -   |
| EC TYPE      | R/W          | R/W | R/W | R/W   | R/W | R/W | R/W                 | R/W |
| BIT NAME     | Divider[7:0] |     |     |       |     |     |                     |     |

#### DIVIDER

The BC Clock is set to the Master Clock divided by this field, or  $MCLK / N$ , Where N is 0 to 255. The clock divider bits can only be changed when the BC Bus is in soft RESET (when either the [Reset](#) bit is set by software or when the [BUSY](#) Bit is set by the interface).

Example settings are shown in [Table 32.9, "Example Frequency Settings"](#):

**Table 32.9 Example Frequency Settings**

| DIVIDER | FREQUENCY |
|---------|-----------|
| 0       | 64.52MHz  |
| 1       | 32.25MHz  |
| 2       | 21.41MHz  |
| 3       | 16.13MHz  |
| 4       | 12.9MHz   |
| 15      | 4.033MHz  |
| 21      | 2.99MHz   |
| 2A      | 1.50 MHz  |
| 63      | 1MHz      |

## 32.7 SMSC BC-Link Master Revision History

This revision history shows the changes made to this chapter.

**Table 32.10 SMSC BC-Link Master Chapter Revision History**

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History," on page 539.</a> |              |            |                                                                          |                                                                                                |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------------|--------------------------------------------------------------------------|------------------------------------------------------------------------------------------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE       | SECTION/FIGURE/ENTRY                                                     | CORRECTION                                                                                     |
| 1.                                                                                                                                                                                                                                          |              |            |                                                                          | ■                                                                                              |
| 2.                                                                                                                                                                                                                                          |              |            |                                                                          | ■                                                                                              |
| 3.                                                                                                                                                                                                                                          | 0.5          | 05/29/2007 | <a href="#">Figure 32.1 on page 511</a>                                  | Replaced 32,16,8,& 4 Mhz Clk outputs of the Square Clock Generator with <a href="#">MCLK/n</a> |
| 4.                                                                                                                                                                                                                                          |              | 06/05/2007 | <a href="#">Section 32.5.1, "Instance Buffers vs Clock," on page 512</a> | Added clock instance section and included BC_CLK limits                                        |
| 5.                                                                                                                                                                                                                                          |              |            |                                                                          |                                                                                                |



## Chapter 33 Electrical Specifications

### 33.1 Maximum Guaranteed Ratings\*

|                                                     |                                |
|-----------------------------------------------------|--------------------------------|
| Operating Temperature Range                         | 0°C to +70°C                   |
| Storage Temperature Range                           | -55° to +150°C                 |
| Lead Temperature Range                              | Refer to JEDEC Spec J-STD-020B |
| Positive Voltage on any pin, with respect to Ground | +5.5V                          |
| Negative Voltage on any pin, with respect to Ground | -0.3V                          |
| Supply Voltage Range $V_{VTR}$                      | 3.6 VDC                        |

\*Stresses above those listed above could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

**Note:** When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

**Table 33.1 Operating Conditions**

| SYMBOL      | PARAMETER               | MIN  | TYP    | MAX  | UNITS |
|-------------|-------------------------|------|--------|------|-------|
| VBAT        | Battery Backup Supply   | 2.0  | 3.0    | 3.6  | V     |
| VTR         | Main Supply             | 2.97 | 3.3    | 3.63 | V     |
| PCI_CLK     | PCI Clock               |      | 33     |      | MHz   |
| XTAL1/XTAL2 | Clock Generator Crystal |      | 32.768 |      | KHz   |
| $T_A$       | Operating Temperature   | 0    |        | 70   | °C    |

### 33.2 DC Specifications

#### 33.2.1 Electrical Characteristics

**Table 33.2 DC Electrical Characteristics**

( $T_A = 0^\circ\text{C} - 70^\circ\text{C}$ ,  $V_{CC1} = 3.3 \text{ VDC} \pm 10\%$ )

All buffer types are 5V tolerant, except as indicated in [Note 33.1](#).

| PARAMETER           | SYMBOL    | MIN | TYP | MAX | UNITS | COMMENTS   |
|---------------------|-----------|-----|-----|-----|-------|------------|
| I Type Input Buffer |           |     |     |     |       |            |
| Low Input Level     | $V_{ILI}$ |     |     | 0.8 | V     | TTL Levels |
| High Input Level    | $V_{IHI}$ | 2.0 |     |     | V     |            |

## Product Customer Specification-ODM

**Table 33.2 DC Electrical Characteristics (continued)**(T<sub>A</sub> = 0°C - 70°C, V<sub>CC1</sub> = 3.3 VDC ±10%)All buffer types are 5V tolerant, except as indicated in [Note 33.1](#).

| PARAMETER                                             | SYMBOL                                                                                                                                                                                                                                                                                | MIN | TYP | MAX | UNITS | COMMENTS                               |
|-------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|-------|----------------------------------------|
| IPD Type Buffer                                       |                                                                                                                                                                                                                                                                                       |     |     |     |       |                                        |
| Low Input Level                                       | V <sub>ILI</sub>                                                                                                                                                                                                                                                                      |     |     | 0.8 | V     |                                        |
| High Input Level                                      | V <sub>IHI</sub>                                                                                                                                                                                                                                                                      | 2.0 |     |     | V     |                                        |
| Pull Down                                             | PD                                                                                                                                                                                                                                                                                    |     | 30  |     | uA    |                                        |
| IS Type Input Buffer                                  |                                                                                                                                                                                                                                                                                       |     |     |     |       |                                        |
| Low Input Level                                       | V <sub>ILIS</sub>                                                                                                                                                                                                                                                                     |     |     | 0.8 | V     | Schmitt Trigger                        |
| High Input Level                                      | V <sub>IHIS</sub>                                                                                                                                                                                                                                                                     | 2.2 |     |     | V     | Schmitt Trigger                        |
| Schmitt Trigger Hysteresis                            | V <sub>HYS</sub>                                                                                                                                                                                                                                                                      |     | 250 |     | mV    |                                        |
| ISP Type Input Buffer with 90 mA weak pull-up         |                                                                                                                                                                                                                                                                                       |     |     |     |       |                                        |
| Low Input Level                                       | V <sub>ILIS</sub>                                                                                                                                                                                                                                                                     | 2.2 |     | 0.8 | V     | Schmitt Trigger                        |
| High Input Level                                      | V <sub>IHIS</sub>                                                                                                                                                                                                                                                                     |     | 250 |     | V     | Schmitt Trigger                        |
| Schmitt Trigger Hysteresis                            | V <sub>HYS</sub>                                                                                                                                                                                                                                                                      |     |     |     | mV    |                                        |
| I <sub>CLK</sub> /O <sub>CLK</sub> Crystal Oscillator | Use a 32 KHz parallel resonant crystal oscillator. The load capacitors are seen by the crystal as two capacitors in series and should be approximately <b>CL = X/Y, X = CL1* CL2, Y = CL1 + CL2</b> . For example, a 7.5pF crystal should use two 15pF capacitors for proper loading. |     |     |     |       |                                        |
| O8 Type Buffer                                        |                                                                                                                                                                                                                                                                                       |     |     |     |       |                                        |
| Low Output Level                                      | V <sub>OL</sub>                                                                                                                                                                                                                                                                       |     |     | 0.4 | V     | I <sub>OL</sub> = 8 mA                 |
| High Output Level                                     | V <sub>OH</sub>                                                                                                                                                                                                                                                                       | 2.4 |     |     | V     | I <sub>OH</sub> = -4 mA                |
| Output Leakage                                        | I <sub>OL</sub>                                                                                                                                                                                                                                                                       | -10 |     | +10 | μA    | V <sub>IN</sub> = 0 to V <sub>CC</sub> |
| OD8 Type Buffer                                       |                                                                                                                                                                                                                                                                                       |     |     |     |       |                                        |
| Low Output Level                                      | V <sub>OL</sub>                                                                                                                                                                                                                                                                       |     |     | 0.4 | V     | V <sub>OL</sub> = 8 mA                 |
| Output Leakage                                        | I <sub>OH</sub>                                                                                                                                                                                                                                                                       | -10 |     | +10 | μA    | I <sub>OH</sub> = 0 to V <sub>CC</sub> |
| O12 Type Buffer                                       |                                                                                                                                                                                                                                                                                       |     |     |     |       |                                        |
| Low Output Level                                      | V <sub>OL</sub>                                                                                                                                                                                                                                                                       |     |     | 0.4 | V     | I <sub>OL</sub> = 12mA                 |
| High Output Level                                     | V <sub>OH</sub>                                                                                                                                                                                                                                                                       | 2.4 |     |     | V     | I <sub>OH</sub> = -6mA                 |
| Output Leakage                                        | I <sub>OL</sub>                                                                                                                                                                                                                                                                       | -10 |     | +10 | μA    | V <sub>IN</sub> = 0 to V <sub>CC</sub> |
| OD12 Type Buffer                                      |                                                                                                                                                                                                                                                                                       |     |     |     |       |                                        |
| Low Output Level                                      | V <sub>OL</sub>                                                                                                                                                                                                                                                                       |     |     | 0.4 | V     | I <sub>OL</sub> = 12mA                 |
| Output Leakage                                        | I <sub>OL</sub>                                                                                                                                                                                                                                                                       | -10 |     | +10 | μA    | V <sub>IN</sub> = 0 to V <sub>CC</sub> |

**Table 33.2 DC Electrical Characteristics (continued)**
 $(T_A = 0^{\circ}\text{C} - 70^{\circ}\text{C}, V_{CC1} = 3.3 \text{ VDC} \pm 10\%)$ 

All buffer types are 5V tolerant, except as indicated in [Note 33.1](#).

| PARAMETER             | SYMBOL   | MIN | TYP | MAX | UNITS         | COMMENTS                        |
|-----------------------|----------|-----|-----|-----|---------------|---------------------------------|
| OD16 Type Buffer      |          |     |     |     |               |                                 |
| Low Output Level      | $V_{OL}$ |     |     | 0.4 | V             | $I_{OL} = 16\text{mA}$          |
| Output Leakage        | $I_{OL}$ | -10 |     | +10 | $\mu\text{A}$ | $V_{IN} = 0 \text{ to } V_{CC}$ |
| IO8 Type Buffer       |          |     |     |     |               |                                 |
| Low Output Level      | $V_{OL}$ |     |     | 0.4 | V             | $I_{OL} = 8\text{mA}$           |
| High Output Level     | $V_{OH}$ | 2.4 |     |     | V             | $I_{OH} = -4\text{mA}$          |
| Output Leakage        | $I_{OL}$ | -10 |     | +10 | $\mu\text{A}$ | $V_{IN} = 0 \text{ to } V_{CC}$ |
| Pull Down Type Buffer |          |     |     |     |               |                                 |
| IOD8 Type Buffer      |          |     |     |     |               |                                 |
| Low Output Level      | $V_{OL}$ |     |     | 0.5 | V             | $I_{OL} = 8 \text{ mA}$         |
| High Input Level      | $V_{IH}$ | 2.0 |     |     | V             |                                 |
| Low Input Level       | $V_{IL}$ |     |     | 0.8 | V             |                                 |
| Output Leakage        | $I_{OL}$ | -10 |     | +10 | $\mu\text{A}$ | $V_{IN} = 0 \text{ to } V_{CC}$ |
| IO12 Type Buffer      |          |     |     |     |               |                                 |
| Low Output Level      | $V_{OL}$ |     |     | 0.4 | V             | $I_{OL} = 12\text{mA}$          |
| High Output Level     | $V_{OH}$ | 2.4 |     |     | V             | $I_{OH} = -6\text{mA}$          |
| Output Leakage        | $I_{OL}$ | -10 |     | +10 | $\mu\text{A}$ | $V_{IN} = 0 \text{ to } V_{CC}$ |
| IOD12 Type Buffer     |          |     |     |     |               |                                 |
| Low Output Level      | $V_{OL}$ |     |     | 0.4 | V             | $I_{OL} = 12\text{mA}$          |
| High Input Level      | $V_{IH}$ | 2.0 |     |     | V             |                                 |
| Low Input Level       | $V_{IL}$ |     |     | 0.8 | V             |                                 |
| Output Leakage        | $I_{OL}$ | -10 |     | +10 | $\mu\text{A}$ | $V_{IN} = 0 \text{ to } V_{CC}$ |
| IO16 Type Buffer      |          |     |     |     |               |                                 |
| Low Output Level      | $V_{OL}$ |     |     | 0.5 | V             | $I_{OL} = 16\text{mA}$          |
| High Output Level     | $V_{OH}$ | 2.4 |     |     | V             | $I_{OH} = -8\text{mA}$          |
| Output Leakage        | $I_{OL}$ | -10 |     | +10 | $\mu\text{A}$ | $V_{IN} = 0 \text{ to } V_{CC}$ |



## Product Customer Specification-ODM

**Table 33.2 DC Electrical Characteristics (continued)**(T<sub>A</sub> = 0°C - 70°C, V<sub>CC1</sub> = 3.3 VDC ±10%)All buffer types are 5V tolerant, except as indicated in [Note 33.1](#).

| PARAMETER           | SYMBOL                   | MIN | TYP | MAX | UNITS | COMMENTS                                        |
|---------------------|--------------------------|-----|-----|-----|-------|-------------------------------------------------|
| IOD16 Type Buffer   |                          |     |     |     |       |                                                 |
| Low Output Level    | V <sub>OL</sub>          |     |     | 0.5 | V     | I <sub>OL</sub> =16 mA                          |
| High Input Level    | V <sub>IH</sub>          | 2.0 |     |     | V     |                                                 |
| Low Input Level     | V <sub>IL</sub>          |     |     | 0.8 | V     |                                                 |
| Output Leakage      | I <sub>OL</sub>          | -10 |     | +10 | μA    | V <sub>IN</sub> = 0 to V <sub>CC</sub>          |
| IO24 Type Buffer    |                          |     |     |     |       |                                                 |
| Low Output Level    | V <sub>OL</sub>          |     |     | .5  | V     | I <sub>OL</sub> = 24mA                          |
| High Output Level   | V <sub>OH</sub>          | 2.4 |     |     | V     | I <sub>OH</sub> = -24mA                         |
| Output Leakage      | I <sub>OL</sub>          | -10 |     | +10 | μA    | V <sub>IN</sub> = 0 to V <sub>CC</sub>          |
| PCI_CLK Type Buffer | PCI_ICLK                 |     |     |     |       | See <i>PCI Local Bus Specification Rev. 2.2</i> |
| PCI_IO Type Buffers | PCI_IO<br>PCI_O<br>PCI_I |     |     |     |       | See <a href="#">Note 33.2</a>                   |
| PCI_OD Type Buffer  | PCI_OD                   |     |     |     |       |                                                 |

**Note 33.1** All signal pins are 5V Tolerant except as listed in [Table 3.32](#), "Non 5 Volt Tolerant Signal Buffers," on page 68. The pin listed in [Table 3.32](#) are 3.3 Volt tolerant

**Note 33.2** All Signal functions in [Section 3.5](#), "Pin Signal Function Multiplexing," on page 47 listed as having an "VCC" emulated power tri-stated when the input VCC\_PWRGD is inactive.

**Note 33.3** All 5V Tolerant I-type & I/O-type input buffers can be pulled to 5 volts.

**Note 33.4** All 5V Tolerant OD-type output buffers can be pulled to 5 volts.

**Note 33.5** All 5V Tolerant O-type and I/O-type output buffers will only drive to 3.3 volts, even if pulled-up externally to 5 volts.

## 33.3 Power Consumption

**Table 33.3 MEC5035 Power Consumption**

|         | VBAT | VTR  | 64.52 MHZ RING OSCILLATOR | ARC (EC_CLK_DIV/MHz) | VCC_PWRGD | PM STATE (Note 33.6) | I <sub>VBAT</sub> | I <sub>VTR</sub>         |
|---------|------|------|---------------------------|----------------------|-----------|----------------------|-------------------|--------------------------|
| MAXIMUM | –    | 3.3V | ON                        |                      | 1         | RUN                  | –                 | 40mA                     |
| RUN     | –    | 3.3V | ON                        | 20h/2MHz             | 0         | FULL POWER           | –                 | 28mA                     |
|         |      |      |                           | 10h/4MHz             |           |                      |                   | 29mA                     |
|         |      |      |                           | 8h/8MHz              |           |                      |                   | 32mA                     |
|         |      |      |                           | 4h/16MHz             |           |                      |                   | 36mA                     |
|         |      |      |                           | 3h/21.3MHz           |           |                      |                   | 37mA                     |
| IDLE    | –    | 3.3V | ON                        | TBD                  | 0         | SYSTEM LIGHT SLEEP   | –                 | TBD                      |
|         |      | 3.3V | ON                        | TBD                  |           | SYSTEM HEAVY SLEEP   |                   | 1.3mA                    |
| SLEEP   | –    | 3.3V | OFF                       | –                    | 0         | SYSTEM DEEPEST SLEEP | –                 | 900μA Typical<br>2mA Max |
| MINIMUM | >2V  | 0V   | –                         | –                    | 0         | (XOSEL=1)            | –                 | TBD                      |
|         |      |      |                           |                      |           | (XOSEL=0)            | –                 | TBD                      |

**Note 33.6** the MEC5035 Power Management (PM) States are described in [Section 4.4.7.2, "EC Controlled Dynamic Power States,"](#) on page 85.

**Note 33.7** [EC\\_CLK\\_DIV](#) bits are located in the [EC Clock Divider Register](#) on page 107.

## 33.4 AC Specifications

AC Test Conditions

CAPACITANCE T<sub>A</sub> = 25°C; f<sub>c</sub> = 1MHz; V<sub>cc</sub> = 3.3 VDC



| PARAMETER               | SYMBOL           | LIMITS |     |     | UNIT | TEST CONDITION                                   |
|-------------------------|------------------|--------|-----|-----|------|--------------------------------------------------|
|                         |                  | MIN    | TYP | MAX |      |                                                  |
| Clock Input Capacitance | C <sub>IN</sub>  |        |     | 20  | pF   | All pins except pin under test tied to AC ground |
| Input Capacitance       | C <sub>IN</sub>  |        |     | 10  | pF   |                                                  |
| Output Capacitance      | C <sub>OUT</sub> |        |     | 20  | pF   |                                                  |

### 33.5 Electrical Specifications Revision History

This revision history shows the changes made to this chapter.

**Table 33.4 Electrical Specifications Chapter Revision History**

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History," on page 539.</a> |              |           |                                                                |               |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|-----------|----------------------------------------------------------------|---------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE      | SECTION/FIGURE/ENTRY                                           | CORRECTION    |
| 1.                                                                                                                                                                                                                                          | 0.6          | 7/30/2007 | <a href="#">Section 33.3, "Power Consumption," on page 522</a> | Added Section |
| 2.                                                                                                                                                                                                                                          |              |           |                                                                |               |
| 3.                                                                                                                                                                                                                                          |              |           |                                                                |               |
| 4.                                                                                                                                                                                                                                          |              |           |                                                                |               |

## Chapter 34 Timing Diagrams

### 34.1 Clock and Reset Timing

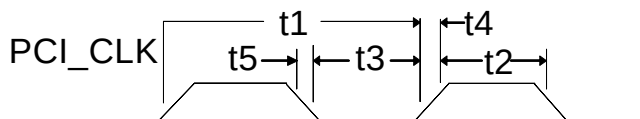


Figure 34.1 PCI Clock Timing

Table 34.1 PCI Clock Timing Parameters

| NAME | DESCRIPTION | MIN | TYP | MAX  | UNITS |
|------|-------------|-----|-----|------|-------|
| t1   | Period      | 30  |     | 33.3 | nsec  |
| t2   | High Time   | 12  |     |      |       |
| t3   | Low Time    |     |     |      |       |
| t4   | Rise Time   |     |     | 3    |       |
| t5   | Fall Time   |     |     |      |       |

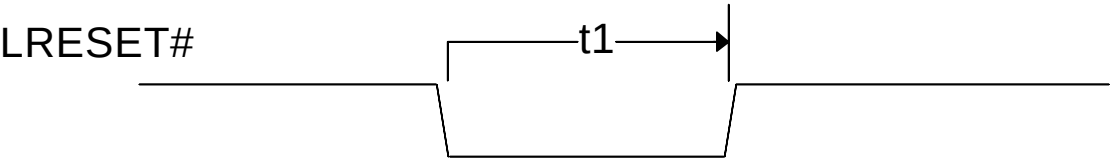


Figure 34.2 Reset Timing

Table 34.2 Reset Timing Parameters

| NAME | DESCRIPTION   | MIN | TYP | MAX | UNITS |
|------|---------------|-----|-----|-----|-------|
| t1   | LRESET# width | 1   |     |     | ms    |



## 34.2 LPC Timing

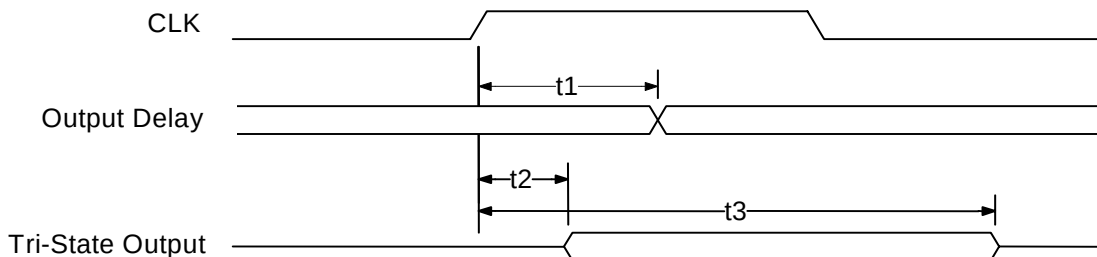


**Figure 34.3 Output Timing Measurement Conditions, LPC Signals**

**Table 34.3 Output Timing Measurement Conditions, LPC Signals Parameters**

| NAME | DESCRIPTION                               | MIN | TYP | MAX | UNITS |
|------|-------------------------------------------|-----|-----|-----|-------|
| t1   | CLK to Signal Valid Delay – Bused Signals | 2   |     | 11  | ns    |
| t2   | Float to Active Delay                     |     |     |     |       |
| t3   | Active to Float Delay                     |     |     | 28  |       |

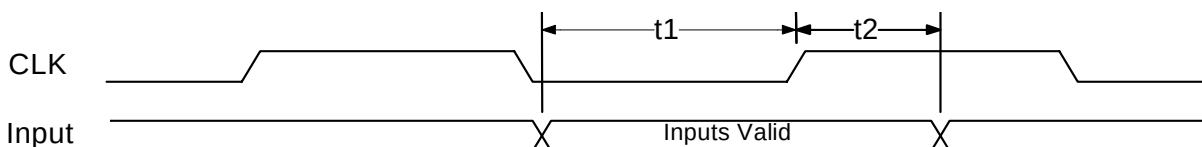


**Figure 34.4 Input Timing Measurement Conditions, LPC Signals**

**Table 34.4 Input Timing Measurement Conditions, LPC Signals Parameters**

| NAME | DESCRIPTION                              | MIN | TYP | MAX | UNITS |
|------|------------------------------------------|-----|-----|-----|-------|
| t1   | Input Set Up Time to CLK – Bused Signals | 7   |     |     | ns    |
| t2   | Input Hold Time from CLK                 | 0   |     |     |       |

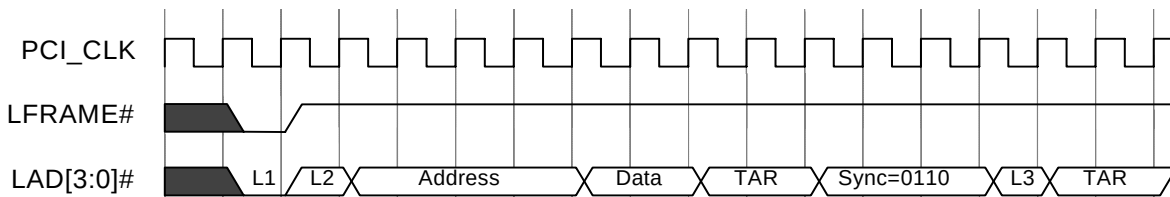


**Figure 34.5 I/O Write**

## Product Customer Specification-ODM

**Note:** L1=Start; L2=CYCTYP+DIR; L3=Sync of 0000

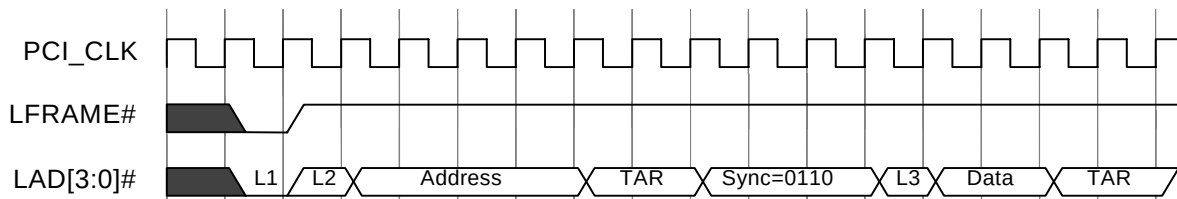


Figure 34.6 I/O Read

**Note:** L1=Start; L2=CYCTYP+DIR; L3=Sync of 0000

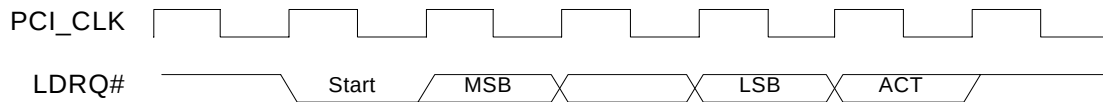


Figure 34.7 DMA Request Assertion Through LDRQ#

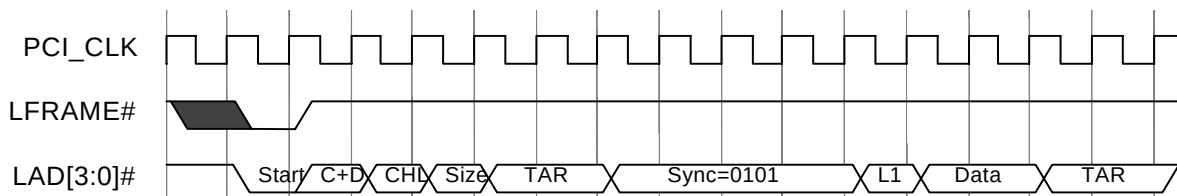


Figure 34.8 DMA Write (First Byte)

**Note:** L1=Sync of 0000

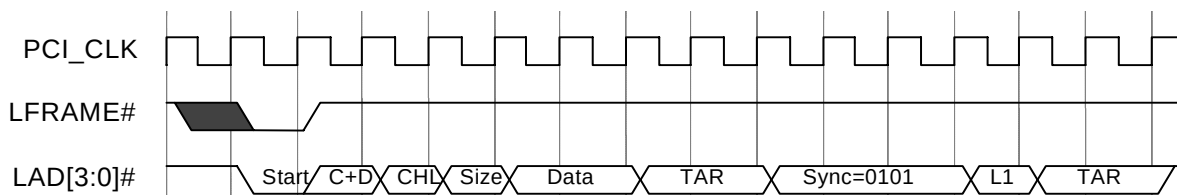


Figure 34.9 DMA Read (First Byte)

**Note:** L1=Sync of 0000

### 34.3 Serial IRQ Timing

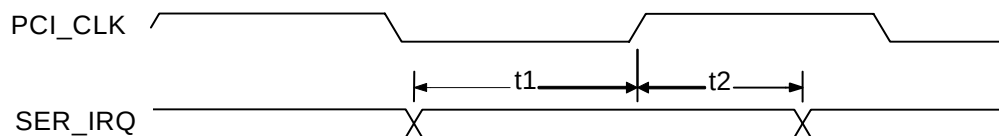


Figure 34.10 Setup and Hold Time

Table 34.5 Setup and Hold Time

| NAME | DESCRIPTION                          | MIN | TYP | MAX | UNITS |
|------|--------------------------------------|-----|-----|-----|-------|
| t1   | SER_IRQ Setup Time to PCI_CLK Rising | 7   |     |     | nsec  |
| t2   | SER_IRQ Hold Time to PCI_CLK Rising  | 0   |     |     |       |

### 34.4 Serial Port Data Timing

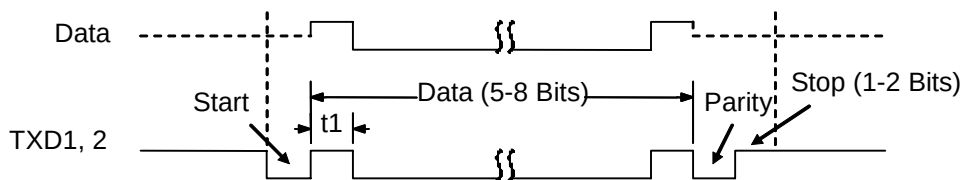


Figure 34.11 Serial Port Data

Table 34.6 Serial Port Data Parameters

| NAME | DESCRIPTION               | MIN | TYP                                       | MAX | UNITS |
|------|---------------------------|-----|-------------------------------------------|-----|-------|
| t1   | Serial Port Data Bit Time |     | $t_{BR}$<br>( <a href="#">Note 34.1</a> ) |     | nsec  |

**Note 34.1**  $t_{BR}$  is 1/Baud Rate. The Baud Rate is programmed through the divisor latch registers. Baud Rates have percentage errors indicated in [Table 12.21, "UART Baud Rates," on page 243](#).

### 34.5 I2C/SMBus Timing

See SMBus Controller Core Interface, Rev. 0.4, Core-Level Architecture Specification, SMSC, 1/31/07

### 34.6 Fan Tachometer Timing

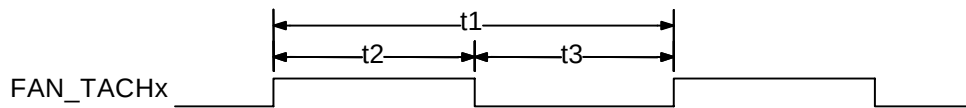


Figure 34.12 Fan Tachometer Input Timing

Table 34.7 Fan Tachometer Input Timing Parameters

| NAME | DESCRIPTION     | MIN | TYP | MAX | UNITS |
|------|-----------------|-----|-----|-----|-------|
| t1   | Pulse Time      | 100 |     |     | μsec  |
| t2   | Pulse High Time |     |     |     |       |
| t3   | Pulse Low Time  | 10  |     |     |       |

**Note 34.2**  $t_{TACH}$  is the clock used for the tachometer counter. It is  $30.52 * \text{prescaler}$ , where the prescaler is programmed in the Fan Tachometer Timebase Prescaler register.

## 34.7 PS/2 Timing

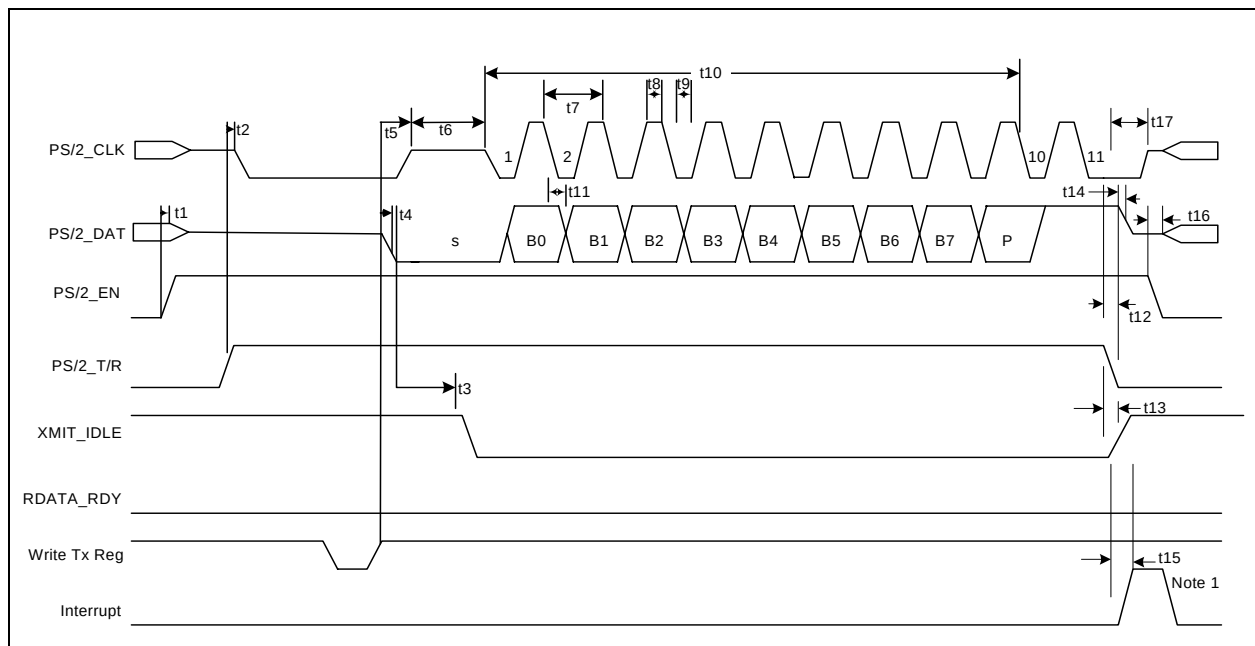


Figure 34.13 PS/2 Transmit Timing

**Table 34.8 PS/2 Channel Transmission Timing Parameters**

| NAME | DESCRIPTION                                                                                                                                                                             | MIN   | TYP | MAX    | UNITS |
|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-----|--------|-------|
| t1   | The PS2 Channel's CLK and DATA lines are floated following PS2_EN=1 and PS2_T/R=0.                                                                                                      |       |     | 1000   | ns    |
| t2   | PS2_T/R bit set to CLK driven low preparing the PS2 Channel for data transmission.                                                                                                      |       |     |        |       |
| t3   | CLK line floated to XMIT_IDLE bit de-asserted.                                                                                                                                          |       |     |        |       |
| t4   | Trailing edge of 8051 WR of Transmit Register to DATA line driven low.                                                                                                                  | 45    |     |        |       |
| t5   | Trailing edge of EC WR of Transmit Register to CLK line floated.                                                                                                                        | 90    |     | 130    | ns    |
| t6   | Initiation of Start of Transmit cycle by the PS2 channel controller to the auxiliary peripheral's responding by latching the Start bit and driving the CLK line low.                    | 0.002 |     | 25.003 | ms    |
| t7   | Period of CLK                                                                                                                                                                           | 60    |     | 302    | μs    |
| t8   | Duration of CLK high (active)                                                                                                                                                           | 30    |     | 151    |       |
| t9   | Duration of CLK low (inactive)                                                                                                                                                          |       |     |        |       |
| t10  | Duration of Data Frame. Falling edge of Start bit CLK (1st clk) to falling edge of Parity bit CLK (10th clk).                                                                           |       |     | 2.002  | ms    |
| t11  | DATA output by MEC5035 following the falling edge of CLK. The auxiliary peripheral device samples DATA following the rising edge of CLK.                                                | 3.5   |     | 7.1    | μs    |
| t12  | Rising edge following the 11th falling clock edge to PS_T/R bit driven low.                                                                                                             | 0     |     | 800    | ns    |
| t13  | Trailing edge of PS_T/R to XMIT_IDLE bit asserted.                                                                                                                                      |       |     | 500    |       |
| t14  | DATA released to high-Z following the PS2_T/R bit going low.                                                                                                                            |       |     |        |       |
| t15  | XMIT_IDLE bit driven high to interrupt generated.<br>Note1- Interrupt is cleared by writing a 1 to the status bit in <a href="#">Table 16.64, "IRQ23 Source Register," on page 348.</a> |       |     |        |       |
| t16  | The PS2 Channel's CLK and DATA lines are driven to the values stored in the WR_CLK and WR_DATA bits of the Control Register when PS2_EN is written to 0.                                |       |     |        |       |
| t17  | Trailing edge of CLK is held low prior to going high-Z                                                                                                                                  |       |     |        |       |

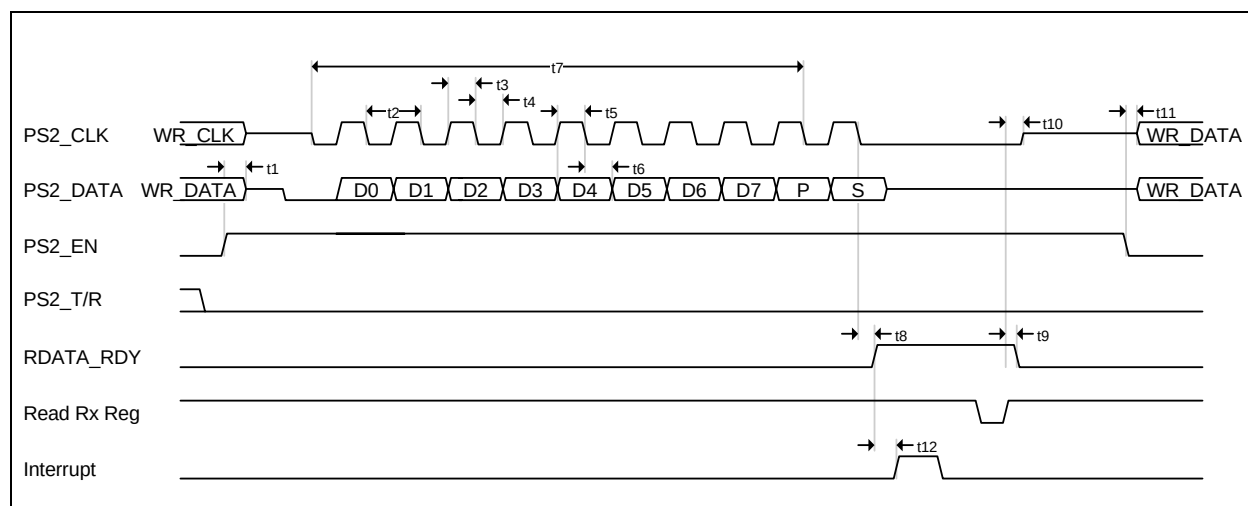


Figure 34.14 PS/2 Receive Timing

Table 34.9 PS/2 Channel Receive Timing Diagram Parameters

| NAME | DESCRIPTION                                                                                                   | MIN | TYP | MAX   | UNITS |
|------|---------------------------------------------------------------------------------------------------------------|-----|-----|-------|-------|
| t1   | The PS2 Channel's CLK and DATA lines are floated following PS2_EN=1 and PS2_T/R=0.                            |     |     | 1000  | ns    |
| t2   | Period of CLK                                                                                                 | 60  |     | 302   | μs    |
| t3   | Duration of CLK high (active)                                                                                 | 30  |     | 151   |       |
| t4   | Duration of CLK low (inactive)                                                                                |     |     |       |       |
| t5   | DATA setup time to falling edge of CLK. MEC5035 samples the data line on the falling CLK edge.                | 1   |     |       |       |
| t6   | DATA hold time from falling edge of CLK. MEC5035 samples the data line on the falling CLK edge.               | 2   |     |       |       |
| t7   | Duration of Data Frame. Falling edge of Start bit CLK (1st clk) to falling edge of Parity bit CLK (10th clk). |     |     | 2.002 | ms    |
| t8   | Falling edge of 11th CLK to RDATA_RDY asserted.                                                               |     |     | 1.6   | μs    |

**Table 34.9 PS/2 Channel Receive Timing Diagram Parameters (continued)**

| NAME | DESCRIPTION                                                                                                                                              | MIN | TYP | MAX | UNITS |
|------|----------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|-------|
| t9   | Trailing edge of the EC's RD signal of the Receive Register to RDATA_RDY bit deasserted.                                                                 |     |     | 500 | ns    |
| t10  | Trailing edge of the EC's RD signal of the Receive Register to the CLK line released to high-Z.                                                          |     |     |     |       |
| t11  | The PS2 Channel's CLK and DATA lines are driven to the values stored in the WR_CLK and WR_DATA bits of the Control Register when PS2_EN is written to 0. |     |     |     |       |
| t12  | RDATA_RDY asserted an interrupt is generated.                                                                                                            |     |     |     |       |



34.8 BC-Link Timing

The SMSC BC\_Link™ protocol is defined in SMSC BC-Link (TM) Specification, Revision1.02, dated September 05, 2007.

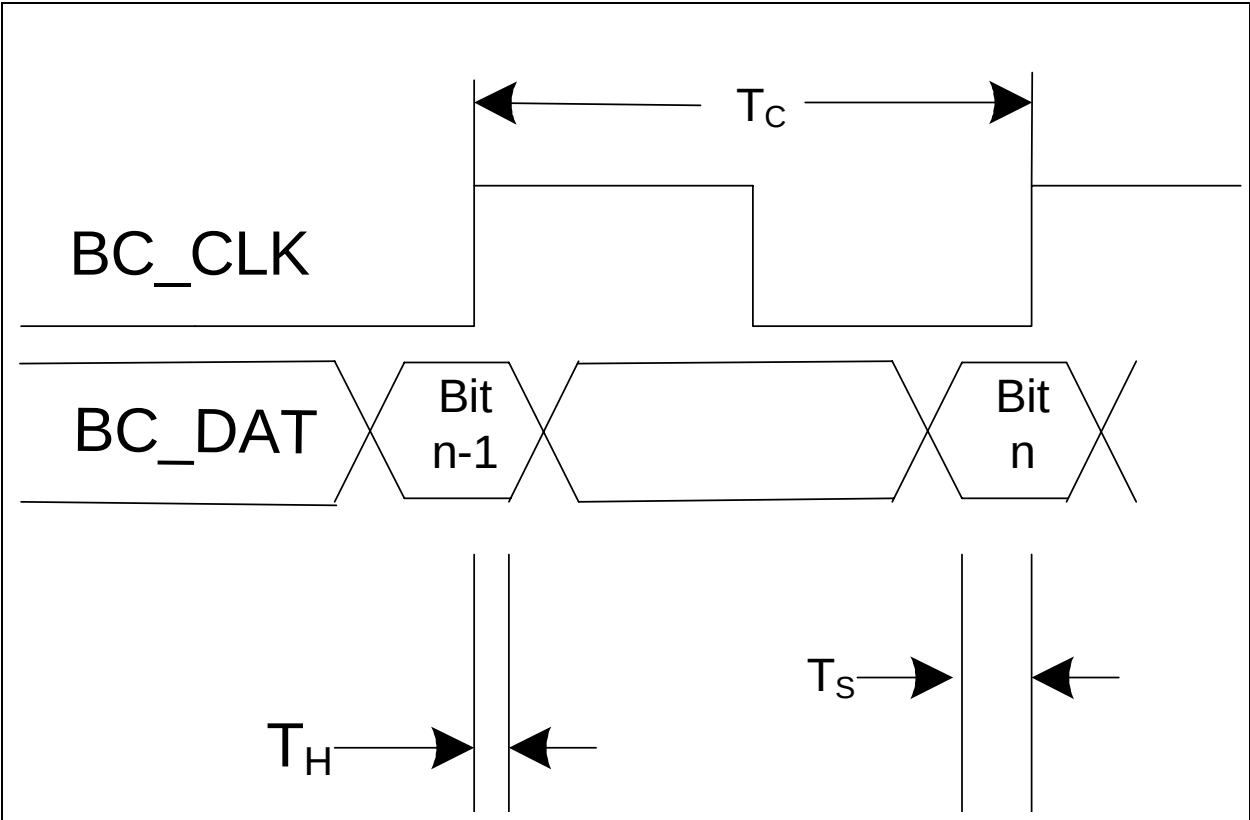


Figure 34.15 BC-Link Timing

Table 34.10 BC-Link Timing Diagram Parameters

| NAME               | DESCRIPTION                                  | MIN | TYP | MAX | UNITS |
|--------------------|----------------------------------------------|-----|-----|-----|-------|
| $t_c$ (High Speed) | High Spec BC Clock Period<br>Clock Frequency |     |     |     |       |
| $t_H$              | DATA hold time from rising edge of CLK.      | 0   |     |     | ns    |
| $t_s$              | DATA setup time before rising edge of CLK.   | 5   |     |     | ns    |



## 34.9 Serial Peripheral Interface (SPI) Timings

### 34.9.1 SPI Clock Timing

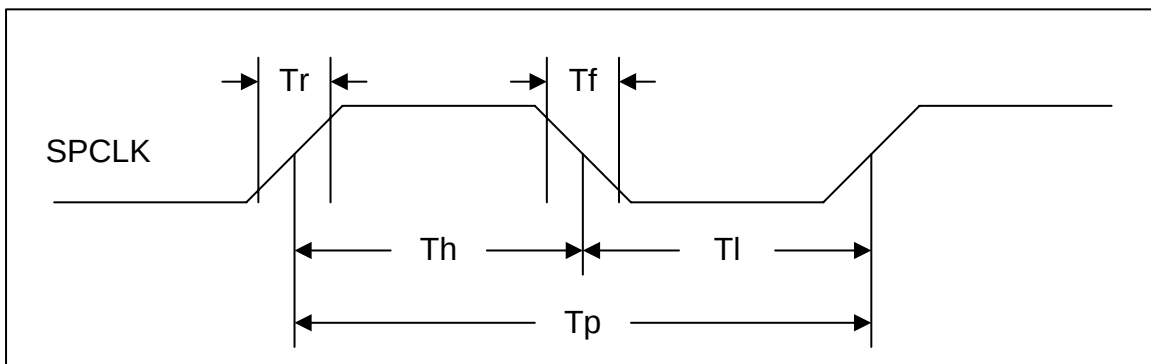


Figure 34.16 SPI Clock Timing

Table 34.11 SPI Clock Timing Parameters

| NAME  | DESCRIPTION                                       | MIN                 | TYP                                | MAX                 | UNITS |
|-------|---------------------------------------------------|---------------------|------------------------------------|---------------------|-------|
| Tr    | SPI Clock Rise Time. Measured from 10% to 90%.    |                     |                                    | 10% of SPCLK Period | ns    |
| Tf    | SPI Clock Fall Time. Measured from 90% to 10%.    |                     |                                    | 10% of SPCLK Period | ns    |
| Th/Tl | SPI Clock High Time/SPI Clock Low Time            | 40% of SPCLK Period | 50% of SPCLK Period<br>(Note 34.3) | 60% of SPCLK Period | ns    |
| Tp    | SPI Clock Period – As selected by SPIBR register. | 15.50               |                                    | 62492.25            | ns    |

**Note 34.3** If divide by 1 is used on the ring oscillator, the duty cycle may not be 50%. The actual duty cycle of divide by 1 will be provided after characterization.

## 34.9.2 SPI Setup and Hold Times

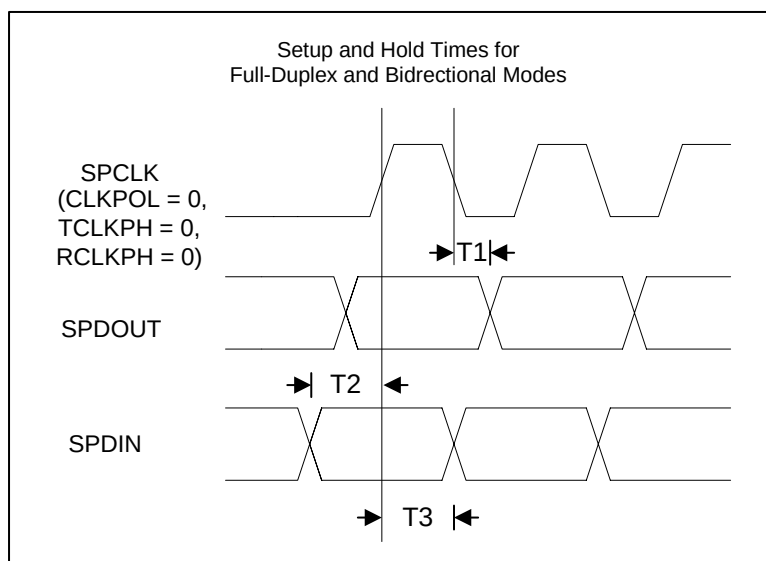


Figure 34.17 SPI Setup and Hold Times

Table 34.12 SPI Setup and Hold Times Parameters

| NAME | DESCRIPTION        | MIN | TYP | MAX | UNITS |
|------|--------------------|-----|-----|-----|-------|
| T1   | Data Output Delay  |     |     | 1   | ns    |
| T2   | Data IN Setup Time | 1   |     |     | ns    |
| T3   | Data IN Hold Time  | 4   |     |     | ns    |

## 34.9.3 SPI Interface Timings

The following timing diagrams represent a single-byte transfer over the SPI interface using different SPCLK phase settings. Data bits are transmitted in bit order starting with the MSB (LSBF='0') or the LSB (LSBF='1'). See the [SPICR - SPI Control Register on page 433](#) for information on the LSBF bit. The CS signal in each diagram is a generic bit-controlled chip select signal required by most peripheral devices. This signal and additional chip selects can be GPIO controlled. Note that these timings for Full Duplex Mode are also applicable to Half Duplex (or Bi-directional) mode.

### 34.9.3.1 SPI Interface Timing – Full Duplex Mode (TCLKPH = 0, RCLKPH = 0)

In this mode, data is available immediately when a device is selected and is sampled on the first and following odd SPCLK edges by the master and slave.

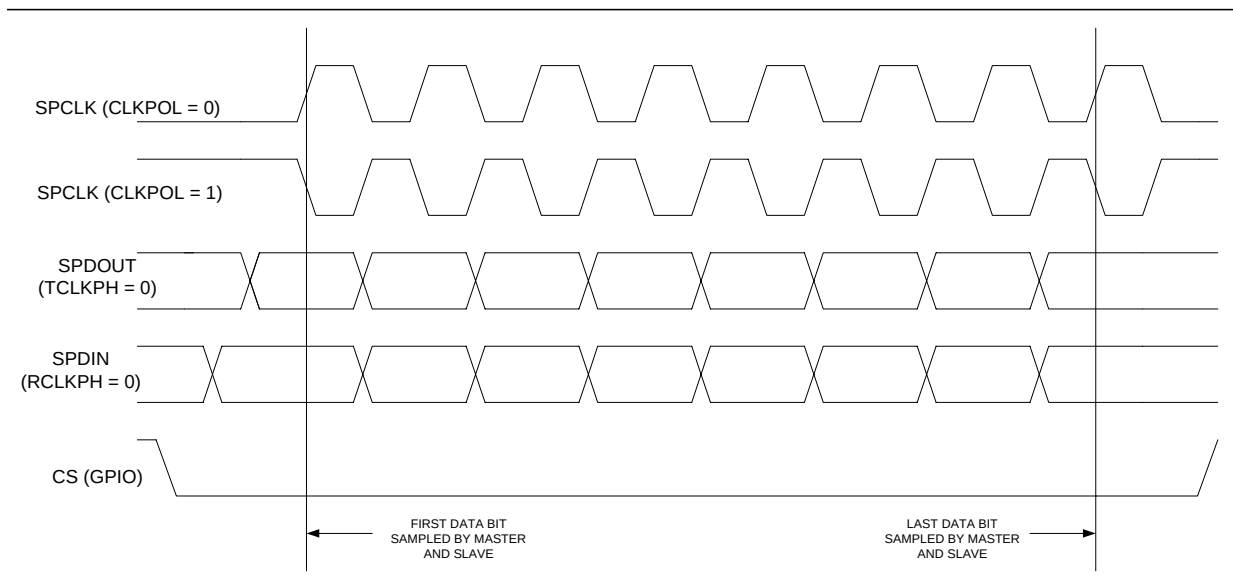


**Figure 34.18 Interface Timing, Full Duplex Mode (TCLKPH = 0, RCLKPH = 0)**

### 34.9.3.2 SPI Interface Timing - Full Duplex Mode (TCLKPH = 1, RCLKPH = 0)

In this mode, the master requires an initial SPCLK edge before data is available. The data from slave is available immediately when the slave device is selected. The data is sampled on the first and following odd edges by the master. The data is sampled on the second and following even SPCLK edges by the slave.

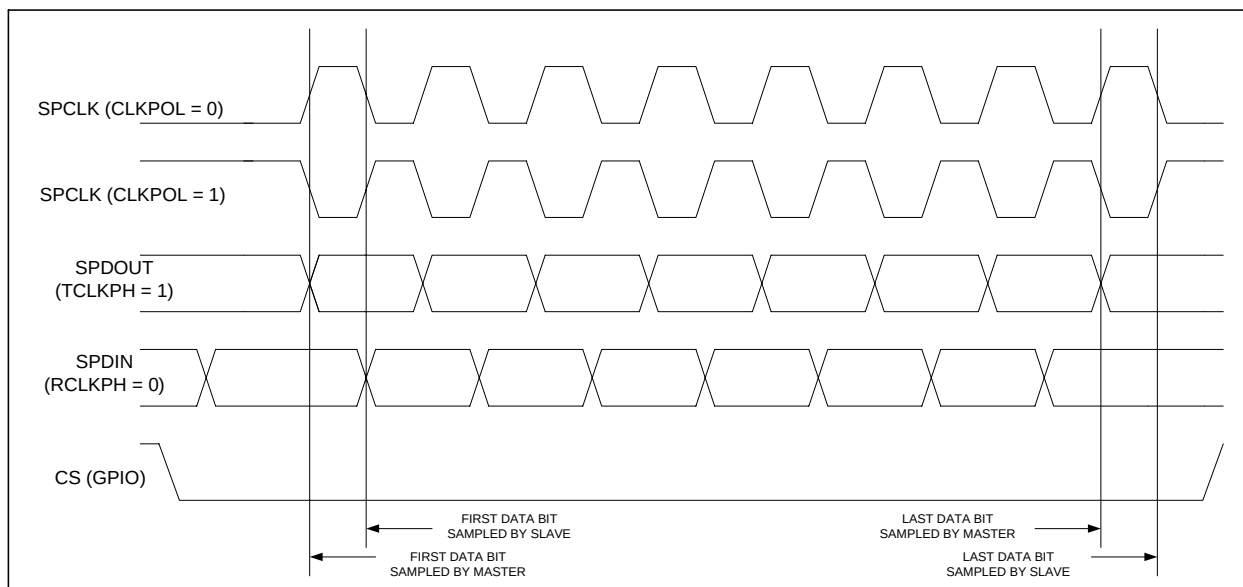


**Figure 34.19 SPI Interface Timing, Full Duplex Mode (TCLKPH = 1, RCLKPH = 0)**

### 34.9.3.3 SPI Interface Timing - Full Duplex Mode (TCLKPH = 0, RCLKPH = 1)

In this mode, the data from slave is available immediately when the slave device is selected. The slave device requires an initial SPCLK edge before data is available. The data is sampled on the second

## 34.10 JTAG Interface Timing

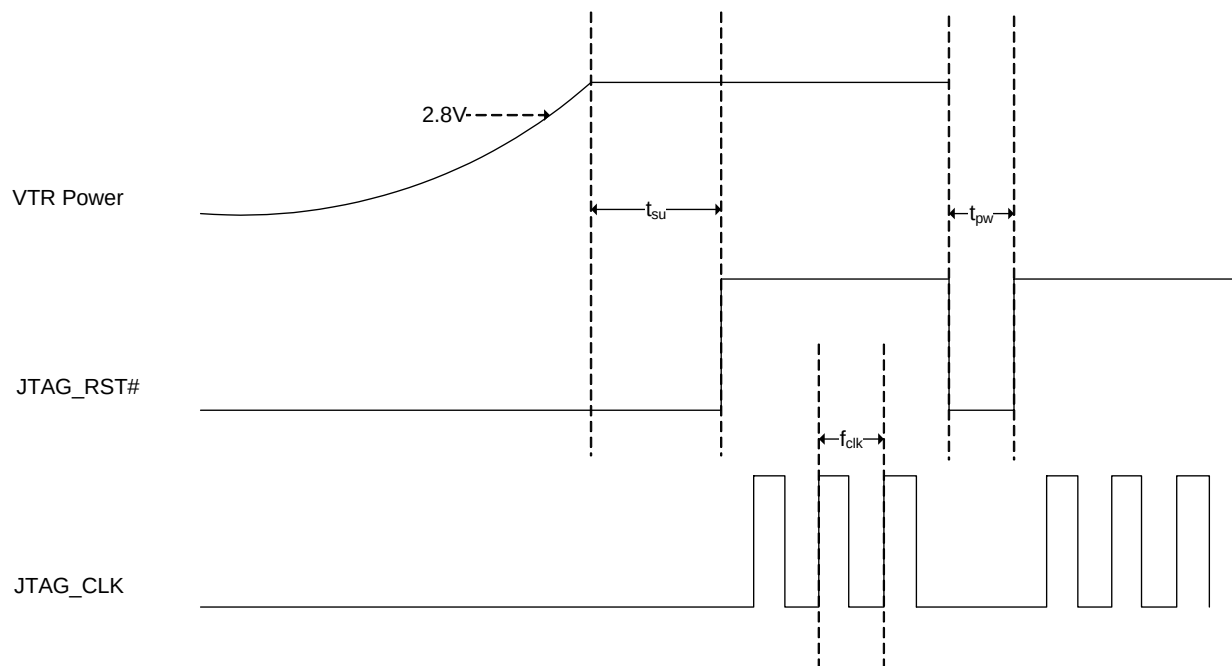


Figure 34.4 JTAG Timing

Table 34.13 Setup and Hold Time

| NAME      | DESCRIPTION                                    | MIN | TYP | MAX | UNITS |
|-----------|------------------------------------------------|-----|-----|-----|-------|
| $t_{su}$  | JTAG_RST# assertion after VTR power is applied | 200 |     |     | nsec  |
| $t_{pw}$  | JTAG_RST# assertion pulsewidth                 | 5   |     |     |       |
| $f_{clk}$ | JTAG_CLK frequency (see note)                  |     |     | 32  | MHz   |

**Note 34.5**  $f_{clk}$  is the maximum frequency to access a JTAG Register. Additional JTAG\_CLK frequency constraints are described in [Chapter 13, JTAG and XNOR, Section 13.4.2, "Clocks,"](#) on [page 250](#).

## 34.11 LED Interface

TBD

## 34.12 Timing Diagrams Revision History

This revision history shows the changes made to this chapter.

**Table 34.14 Timing Diagrams Chapter Revision History**

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History," on page 539.</a> |              |            |                                                                                           |                        |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------------|-------------------------------------------------------------------------------------------|------------------------|
| #                                                                                                                                                                                                                                           | REV# IN SPEC | DATE       | SECTION/FIGURE/ENTRY                                                                      | CORRECTION             |
| 1.                                                                                                                                                                                                                                          | 0.4          | 04/27/2007 | <a href="#">Table 34.9, "PS/2 Channel Receive Timing Diagram Parameters," on page 531</a> | Added table.           |
| 2.                                                                                                                                                                                                                                          | 0.5          | 06/01/2007 | <a href="#">Section 34.10, "JTAG Interface Timing," on page 537</a>                       | Added section content. |
| 3.                                                                                                                                                                                                                                          |              |            |                                                                                           |                        |
| 4.                                                                                                                                                                                                                                          |              |            |                                                                                           |                        |

## Chapter 35 Spec Revision History

### 35.1 Aurora Marketing Documentation

Table 35.1 Aurora Architecture Documentation Publication

| DOCUMENT NAME                      | REVISION | DATE       |
|------------------------------------|----------|------------|
| Product Customer Specification     | 0.1      | 02/27/2007 |
| Product Customer Specification     | 0.2      | 03/08/2007 |
| Product Customer Specification     | 0.3      | 03/12/2007 |
| Product Architecture Specification | 0.3      | 03/12/2007 |
| Product Customer Specification-ODM | 0.4      | 04/30/2007 |
| Product Customer Specification-OEM | 0.4      | 04/30/2007 |
| Product Architecture Specification | 0.4      | 05/11/2007 |
| Product Architecture Specification | 0.5      | 06/08/2007 |
| Product Architecture Specification | 0.6      | 07/23/2007 |
| Product Customer Specification-ODM | 0.6      | 07/23/2007 |
| Product Customer Specification-OEM | 0.6      | 07/23/2007 |
| Product Architecture Specification | 0.61     | 08/31/2007 |
| Product Customer Specification-ODM | 0.61     | 08/31/2007 |
| Product Customer Specification-OEM | 0.61     | 08/31/2007 |

### 35.2 Spec Revision History

Table 35.2 MEC5035 Product Customer Specification-ODM Revision History

| NAME | REVISION<br>LEVEL AND<br>DATE | CROSS-REFERENCE TO INDIVIDUAL CHAPTER REVISION HISTORIES |
|------|-------------------------------|----------------------------------------------------------|
| Raf  | 0.03                          | Initial release with revisions tracked.                  |

Table 35.2 MEC5035 Product Customer Specification-ODM Revision History

| NAME | REVISION<br>LEVEL AND<br>DATE | CROSS-REFERENCE TO INDIVIDUAL CHAPTER REVISION HISTORIES                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|------|-------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Raf  | 0.4                           | <p>Chapter 2, General Description item 1. on page 36.</p> <p>Chapter 3, Pinout and Pin Description items 1.- 2. on page 71</p> <p>Chapter 4, Power, Clocks and Resets item 1. on page 118</p> <p>Chapter 5, Host Interface item on page 138</p> <p>Chapter 6, Logical Device Configuration items 1. - 3. on page 159.</p> <p>Chapter 7, Bus Hierarchy item 1. - 2. on page 171.</p> <p>Chapter 8, MailBox Register Interface item 1. on page 180.</p> <p>Chapter 9, ACPI Embedded Controller Interface item 1. on page 190.</p> <p>Chapter 10, 8042 Emulated Keyboard Controller item 1. on page 211.</p> <p>Chapter 13, JTAG and XNOR items 1.. - 3. on page 267</p> <p>Chapter 14, ARC 625D Embedded Controller items 1.. - 2. on page 274</p> <p>Chapter 15, Embedded Flash Subsystem items 1. - 5. on page 303</p> <p>Chapter 16, EC Interrupt Aggregator items 1. - 3. on page 365.</p> <p>Chapter 17, GPIO Interface items 1. - 4. on page 385</p> <p>Chapter 18, Serial Debug Port item 1. on page 389.</p> <p>Chapter 19, Watchdog Timer Interface items 2. on page 397.</p> <p>Chapter 21, Week Alarm Interface item 1. on page 409.</p> <p>Chapter 24, General Purpose Serial Peripheral Interface (GP-SPI) items 1. - 4. on page 445.</p> <p>Chapter 25, RC Identification Detection (RC_ID) item 1. on page 455.</p> <p>Chapter 26, 16-Bit Timer Interface item 1. on page 468.</p> <p>Chapter 28, PWM Controller item 1. - 2. on page 485.</p> <p>Chapter 30, "PS/2 Device Interface," on page 496 item 1. on page 505</p> <p>Chapter 34, "Timing Diagrams," on page 524 item 1. on page 538.</p> |
|      | 0.5                           | <p>Chapter 3, Pinout and Pin Description items 3. -4. on page 71</p> <p>Chapter 4, Power, Clocks and Resets item 2. on page 118</p> <p>Chapter 13, JTAG and XNOR item 4. on page 267</p> <p>Chapter 15, Embedded Flash Subsystem item 6. on page 303</p> <p>Chapter 26, "16-Bit Timer Interface," on page 457 item 2. on page 468</p> <p>Chapter 30, "PS/2 Device Interface," on page 496 item 2. on page 505</p> <p>Chapter 32, SMSC BC-Link Master item 4. on page 517.</p> <p>Chapter 34, "Timing Diagrams," on page 524 item 2. on page 538.</p> <p>Chapter 36, Reference Documents item 2. on page 541</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|      | 0.6                           | <p>Chapter 3, Pinout and Pin Description item 5. on page 71</p> <p>Chapter 4, Power, Clocks and Resets item 3. on page 118</p> <p>Chapter 12, Two Pin Serial Port (UART) item 1. on page 246</p> <p>Chapter 7, Bus Hierarchy item 4. on page 171</p> <p>Chapter 15, Embedded Flash Subsystem item 6. on page 303</p> <p>Chapter 13, JTAG and XNOR items 5. on page 267</p> <p>Chapter 17, GPIO Interface item 5. on page 385</p> <p>Chapter 29, TACH Monitor item 1. - 2. on page 495</p> <p>Chapter 33, Electrical Specifications item 1. on page 523</p> <p>Chapter 36, Reference Documents item 3. on page 541</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|      | 0.61                          | <p>Chapter 1, MEC5035 Features items 5. - 6. on page 32</p> <p>Chapter 3, Pinout and Pin Description items 6. - 7. on page 72</p> <p>Chapter 17, GPIO Interface items 6.- 7. on page 385.</p> <p>Chapter 36, Reference Documents item 4. on page 541</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |



## Chapter 36 Reference Documents

This document was created using the following parent documents:

1. Intel Low Pin Count Specification, Revision 1.0, September 29, 1997
2. PCI Local Bus Specification, Revision 2.2, December 18, 1998
3. Advanced Configuration and Power Interface Specification, Revision 1.0b, February 2, 1999
4. System Management Bus Specification, Revision 1.1, December 11, 1998.
5. Plug and Play ISA Specification, Version 1.0a, Intel Corp. and Microsoft Corp., May 5, 1994
6. I2C-BUS Specification, Version 2.1, January 2000.
7. ECE1077 MEC-04 Keyboard Scan Extension, Product Architecture Specification, Rev 0.23, January 12, 2006, SMSC Confidential
8. Intel® 82801DBM I/O Controller Hub 4 Mobile (ICH4-M), Datasheet, Order Number: 252337-001, Intel Corp., January 2003
9. SMSC BC-Link (TM) Specification, Revision1.02, dated September 05, 2007
10. SMSC AN #16.1, MEC5035 JTAG Design and Layout Guide

**Table 36.1 Reference Documents Revision History**

| "REV# IN SPEC" column in this table refers of the revision level of the spec into which the table entry below was incorporated. If a chapter is published separately, a blank in the "REV# IN SPEC" column indicates the change has not be incorporated in the spec. See <a href="#">Table 35.2, "MEC5035 Product Customer Specification-ODM Revision History," on page 539.</a> |              |             |                      |                                 |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|-------------|----------------------|---------------------------------|
| #                                                                                                                                                                                                                                                                                                                                                                                | REV# IN SPEC | DATE        | SECTION/FIGURE/ENTRY | CORRECTION                      |
| 1.                                                                                                                                                                                                                                                                                                                                                                               | 0.3          | 06/26/2006  |                      | Initial Release of Chapter      |
| 2.                                                                                                                                                                                                                                                                                                                                                                               | 0.5          | 06/05/2007' |                      | Updated BC-Link Spec revision   |
| 3.                                                                                                                                                                                                                                                                                                                                                                               | 0.6          | 07/05/2007  |                      | Added JTAG App note.            |
| 4.                                                                                                                                                                                                                                                                                                                                                                               | 0.61         | 08/15/2007  |                      | Replace TBD for JTAG App note # |