MCS9865

PCI to Peripheral Controller

Datasheet

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1. General Description

MCS9865 is a PCI based Peripheral Controller. It supports dual-channel high performance Serial Ports, dual enhanced IEEE 1284 compliant parallel ports and an ISA style interface. MCS9865 is ideally suited for Desktop PC and Notebook applications, such as PCI / Mini-PCI add-in Cards for high-speed Serial / Parallel Port expansion.

The PCI interface of MCS9865 is fully Compliant with PCI Local Bus Specification, Revision 2.3. It supports five functions through single device.

On-Chip Serial Ports of MCS9865 support extended 16C550 UART mode and support serial speeds up to 16Mbps. MCS9865 has 256 byte deep Transmit and Receive FIFO for each UART. Deep FIFOs enable high serial speeds / throughputs and reduce CPU Utilization. Each Serial Port is compatible with industry standard 16C550 devices including Standard COM Port of Industrial PC, MosChip family of UARTs like MCS9901/ MCS9835 / MCS9845 / MCS9820 / MCS7840 / MCS7820 / MCS7720 / MCS7703.

The Parallel Port interface is an IEEE 1284 compliant SPP / PS2 / EPP / ECP Parallel Port that fully supports Centronics interface.

ISA Style interface is designed to add additional Serial / Parallel Ports by using external ISA peripherals. ISA interface can be used to achieve additional Serial / Parallel port expansions. Following IO expansions can be supported through MCS9865 ISA interface :

- 1 to 4 Serial
- 1 Serial + 1 Parallel
- 2 Serial + 1 Parallel
- 2 Parallel

MCS9865 has 4 mode select pins. These pins can be bonded at system level for following product configurations:

- PCI to 1 Serial
- PCI to 2 Serial + 1 Parallel
- PCI to 2 Serial + ISA
- PCI to 1 Parallel
- PCI to 2 Parallel

When ISA mode is selected, MCS9865 assumes the presence of an external “ISA to 4 Serial” peripheral on the ISA interface as default configuration and this combination can be supported without an external EEPROM. External EEPROM is needed for other ISA based Serial/Parallel combinations.

Many Serial, Parallel Port product configurations can be supported by using external EEPROM. Refer to **Section 16** for details.

2. Features

PCI

- Fully compliant with PCI Local Bus Specification, Revision 2.3
- Compatible for MiniPCI application requirements
- Fully customizable PCI Configuration Space
- Compatible with 3.3V and 5V PCI signaling
- Supports PCI Power Management

Serial Port

- Four 16C 450 / 550 / Extended 550 compatible UARTs
- Supports RS232, RS485 & RS422 modes
- Bi-directional Speeds from 50 bps to 16 Mbps / Port
- Full Serial modem control
- Supports Hardware, Software flow control
- 5, 6, 7, 8, 9-bit Serial format support
- Even, Odd, None, Space & Mark parity supported
- Custom BAUD rate support with external clock / by programming internal PLL
- On Chip deep 256 Byte FIFOs in Transmit & Receive paths of each Serial Port
- Supports remote wakeup and power management features
- Serial Port transceiver shutdown support
- Supports Slow IrDA on all Serial Ports

IEEE1284 Parallel Port

- Multi-mode IEEE1284 compliant controller (SPP, PS2, EPP, ECP)
- Faster data rates up to 1.5Mbytes/sec for parallel port

ISA

- ISA style I/O interface for extending UARTs & Parallel Ports
- 8 bit data bus @ 8Mhz

Miscellaneous

- On-Chip Dual Voltage Regulator (5V to 3.3V & 1.8V)
- Two-Wire I^2C Interface for EEPROM
- EEPROM read / write through PCI
- Four bi-directional multi-function GPIO lines
- On chip oscillator

3. Applications

- Serial Attached Devices
- Serial Networking / Monitoring Equipment
- Data Acquisition System
- POS Terminal & Industrial PC
- Parallel / Printer Port based applications
- Add-On I/O Cards – Serial / Parallel
- Embedded systems – For I/O expansion

4. Ordering information

- Part Number : MCS9865IV-AA
- 128 Pin LQFP, ROHS
- Industrial Grade, -40 to +85 ^{o}C

5. Application Schematic

- PCI to 2S + 1 Parallel
- PCI to 6S (2S + ISA - 4S)
- PCI to 1P
- PCI to 1S
- PCI to 2P
- PCI to 4S+1P (2S + ISA – 2S1P)
- PCI to 2S+2P (2S + ISA – 2P)

6. Evaluation Board

- MCS9865- EVB – Combo

7. Software Support

SW Driver Support

- DoS 6.22
- Windows 32bit 2000 / XP / 2003 Server
- Windows 64bit XP / 2003 Server
- Windows Vista 32 & 64bit
- Linux Kernel 2.6.14 & above

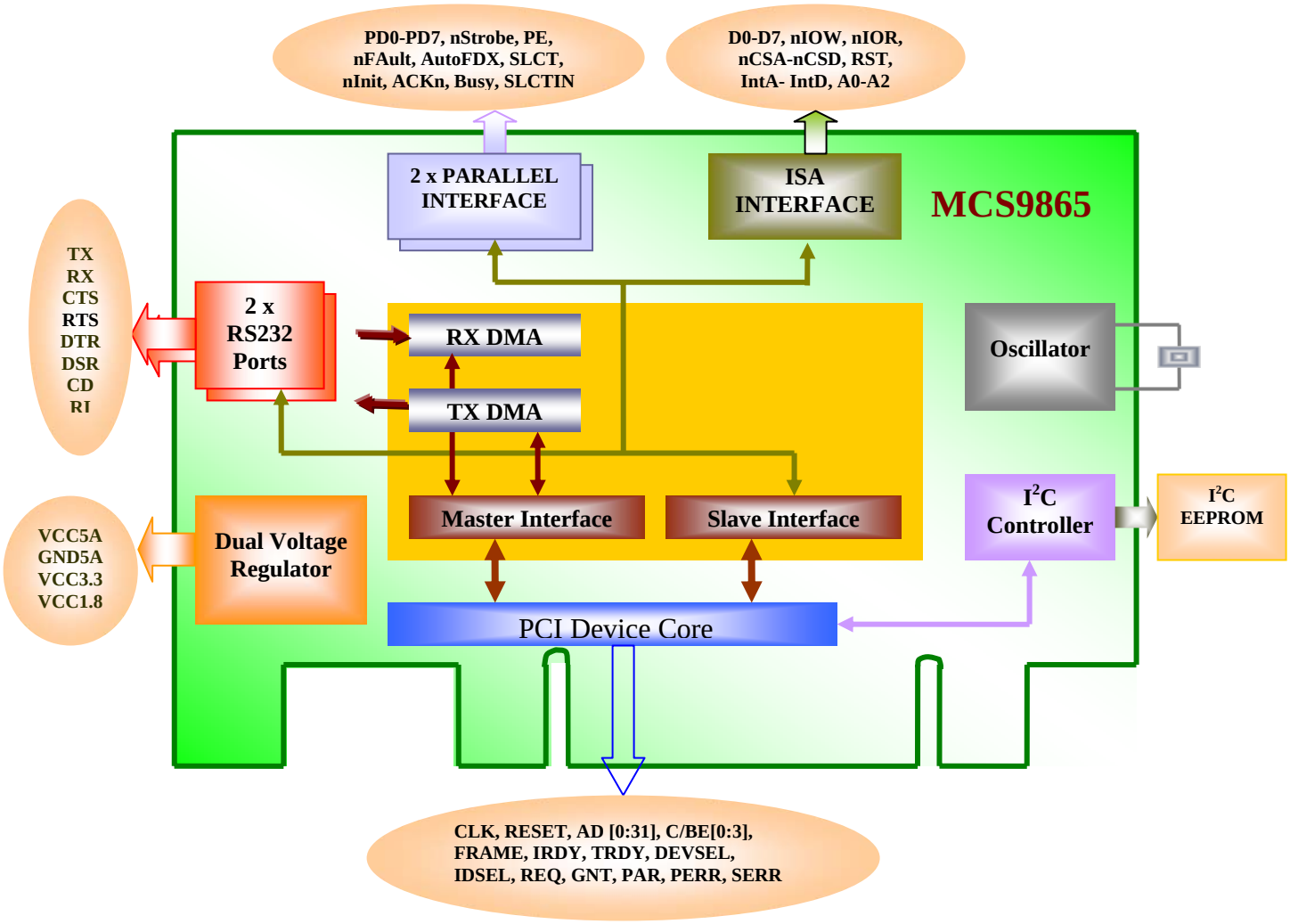
SW Utility Support

- Windows XP based EEPROM Utility
- Windows XP based Diagnostic Utility
- DoS based Diagnostic Utility

8. Certifications

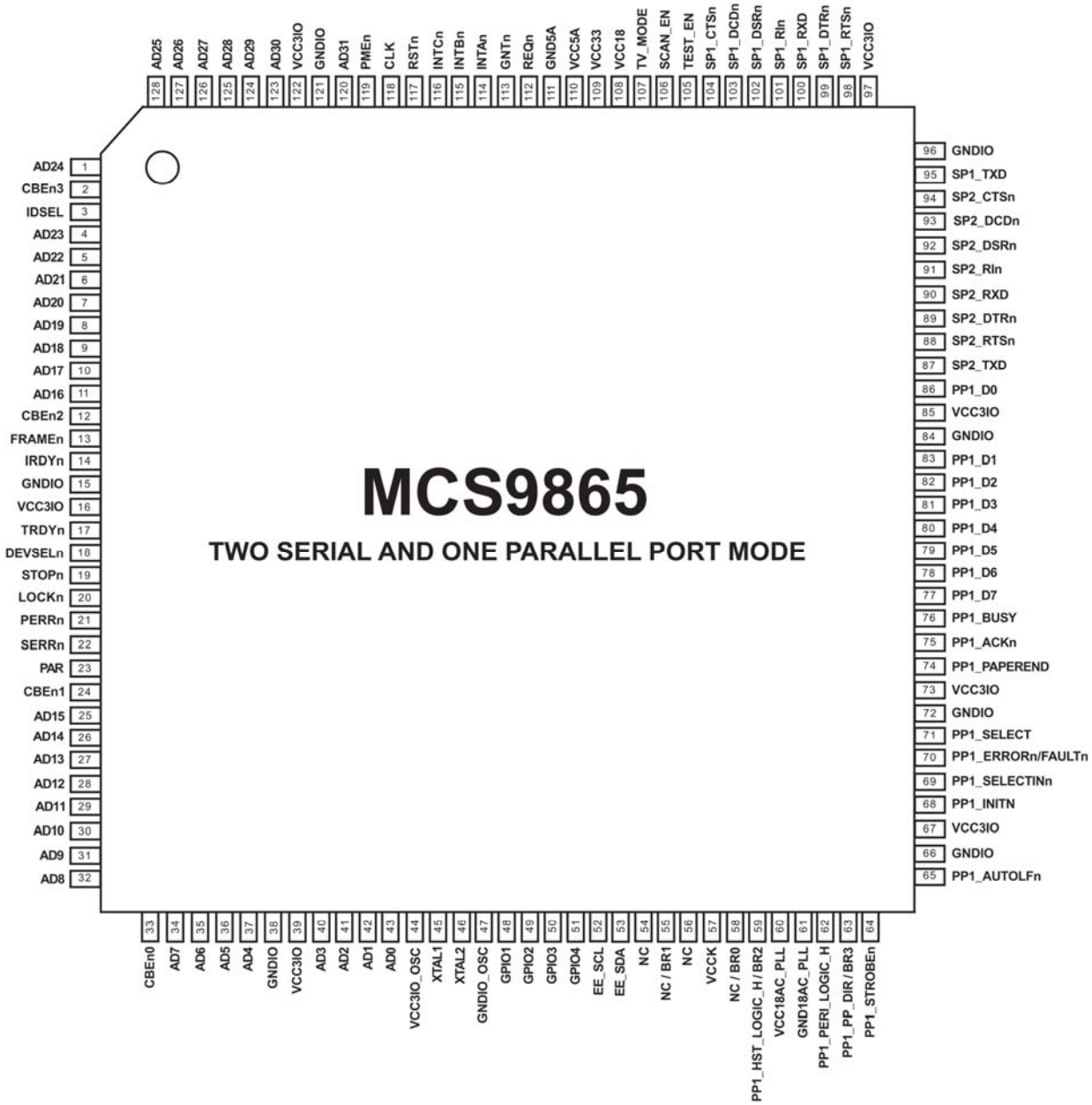
- WHQL Certification for Win XP / Vista device drivers

9. Block Diagram

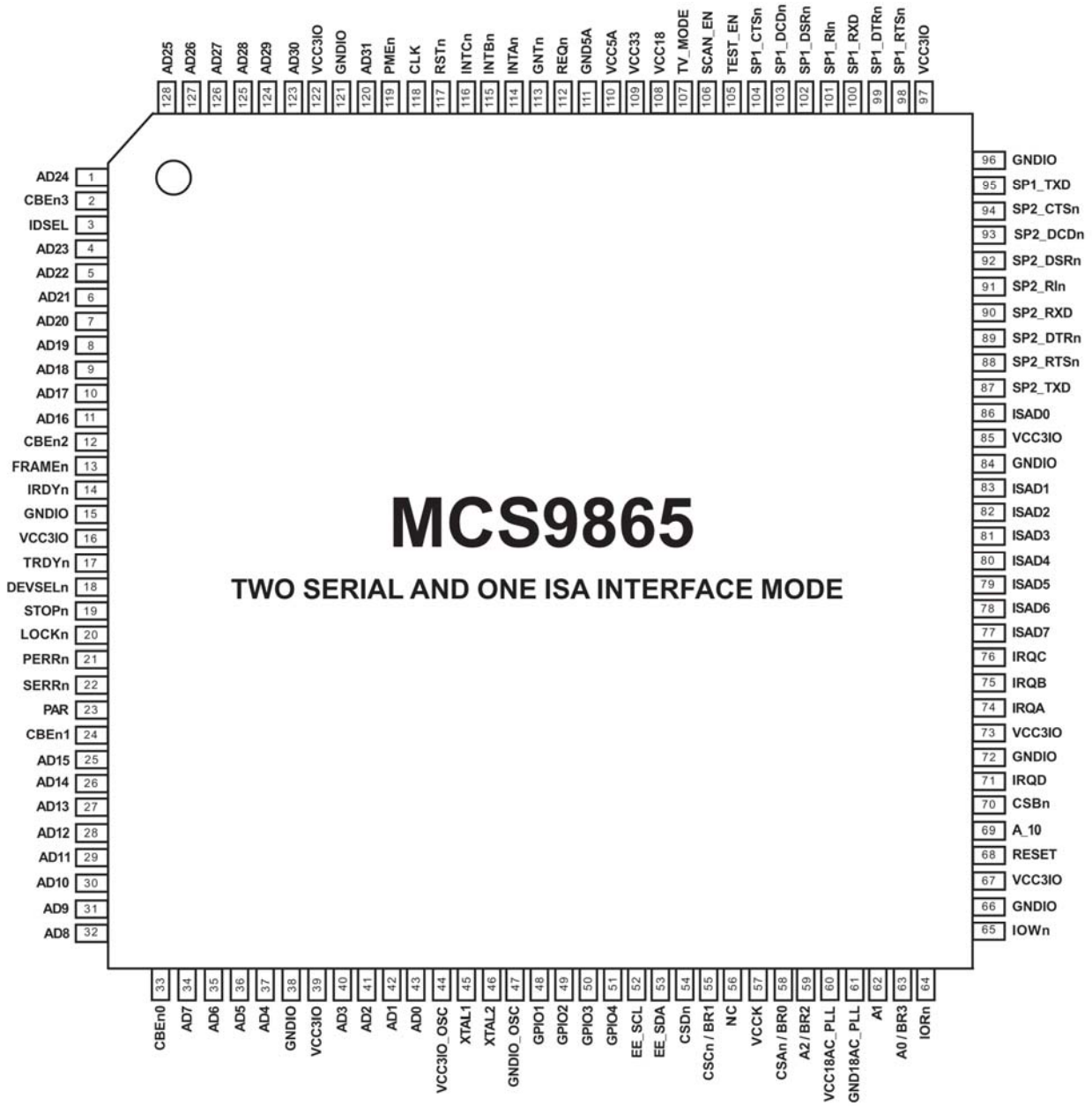


10. Pin Out Diagrams

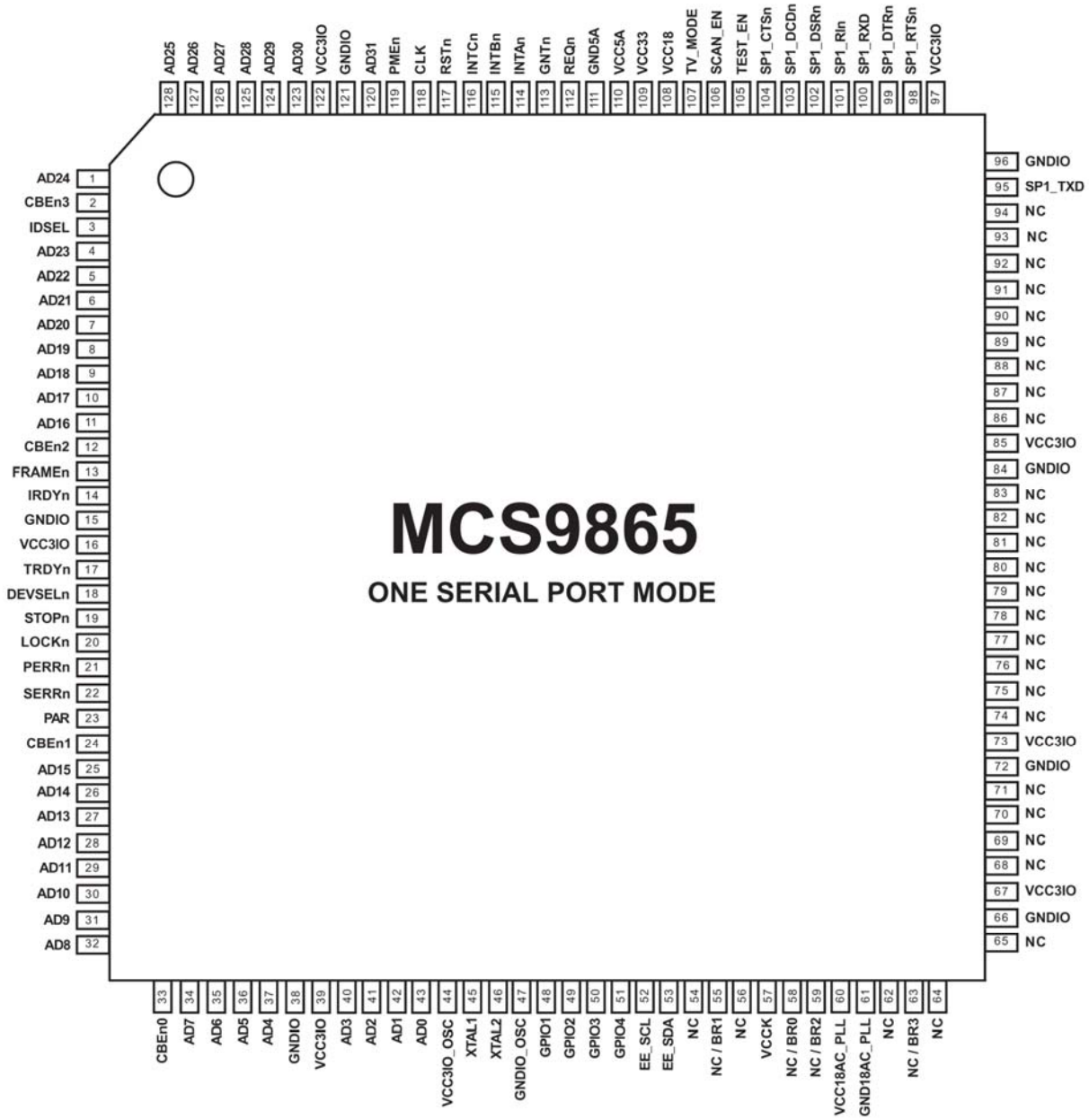
10.1 Pin Out Diagram : 2SP-1PP



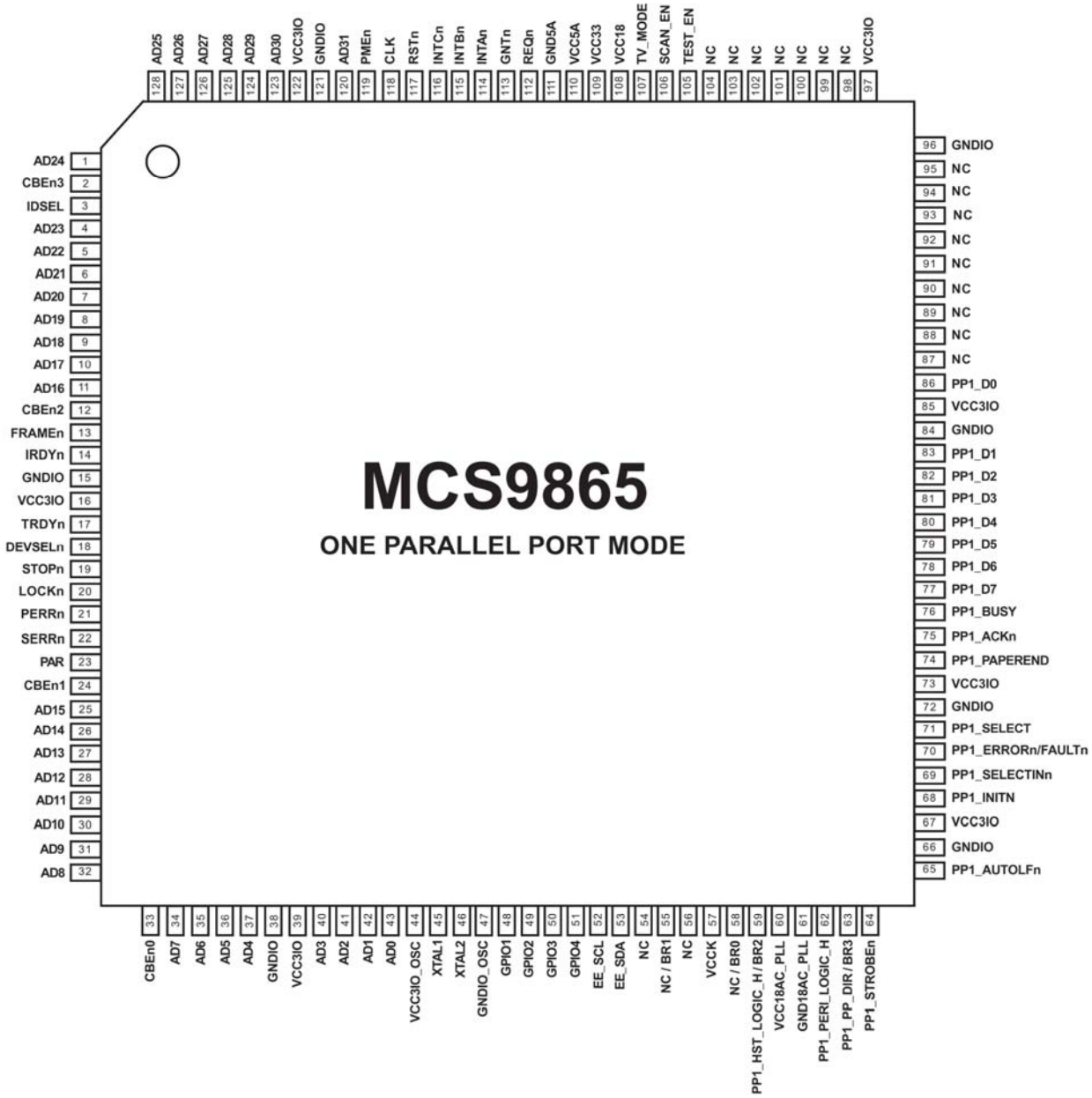
10.2 Pin Out Diagram : 2SP-ISA



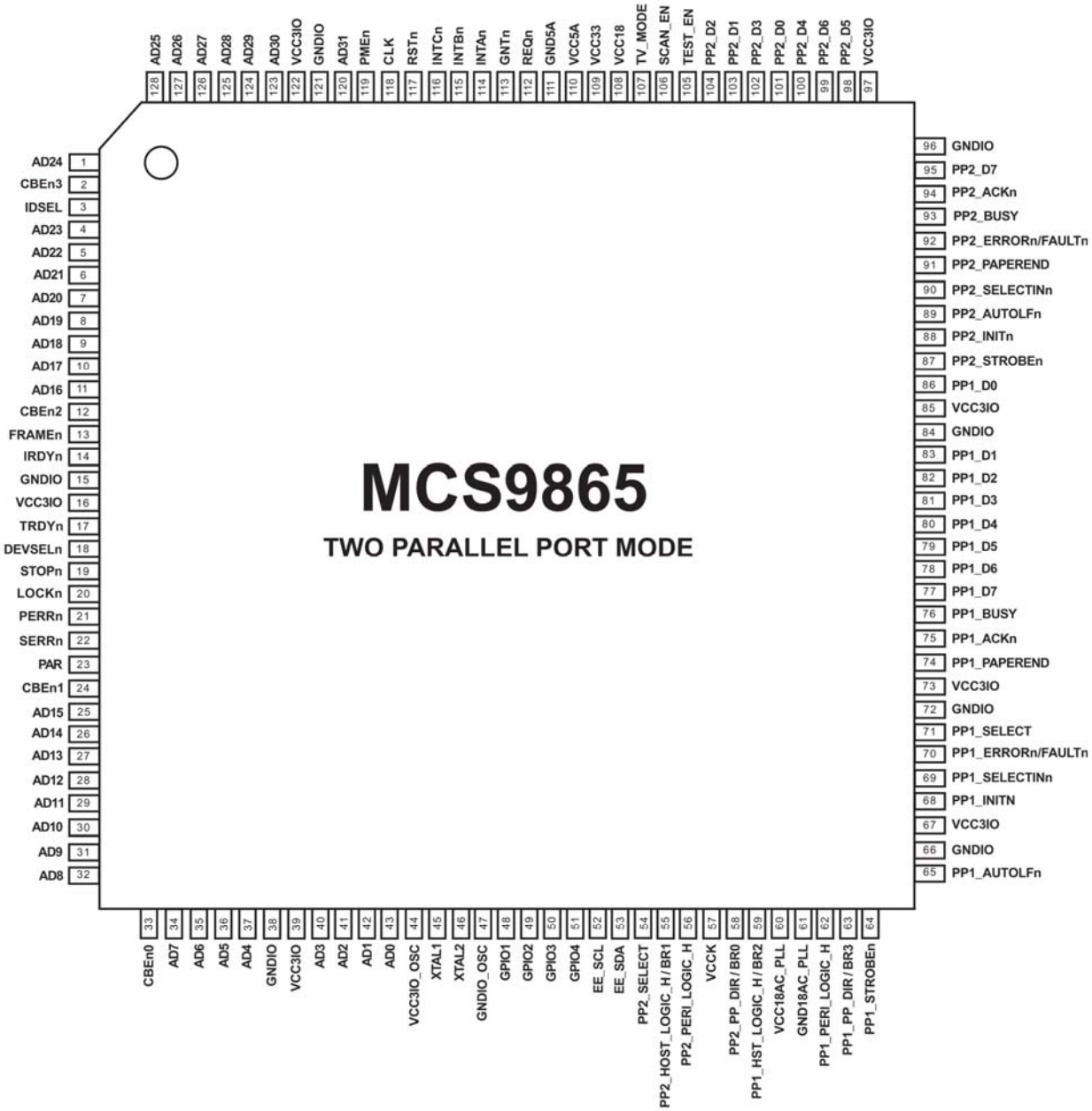
10.3 Pin Out Diagram : 1SP



10.4 Pin Out Diagram : 1PP



10.5 Pin Out Diagram : 2PP



11. Pin Descriptions

This section provides information on each pin of MCS9865. To facilitate detailing, pin descriptions are classified into 4 different groups

- PCI Signals
- Multiplexed Interface Signals
- GPIO, Clock and Miscellaneous Signals
- Power and Ground Signals

11.1 PCI Signals

Table 1: PCI Signals

Pin Number	Pin Name	Type	Description
120	AD31	I/O	Multiplexed PCI Address/Data bus. During the address phase, AD[31:0] contains a physical address. Data is stable and valid when IRDYn and TRDYn are asserted (active low).
123-128	AD[30:25]	I/O	See AD31 description.
1	AD24	I/O	See AD31 description.
4-11	AD[23:16]	I/O	See AD31 description.
25-32	AD[15:8]	I/O	See AD31 description.
34-37	AD[7:4]	I/O	See AD31 description.
40-43	AD[3:0]	I/O	See AD31 description.
2,12 , 24, 33	CBEn[3:0]	I/O	Bus Command and Byte Enable : During the address phase of a transaction, CBEn[3:0] defines the bus command. During the data phase, CBEn [3:0] are used as Byte Enables.
23	PAR	I/O	Parity : Even Parity is applied across AD [31:0] and CBEn [3:0]. PAR is stable and valid one clock after the address phase. For the data phase, PAR is stable and valid one clock after either IRDYn is asserted on a write transaction, or TRDYn is asserted on a read transaction.

Table 1 : PCI Signals (Contd)

Pin Number	Pin Name	Type	Description
13	FRAMEn	I/O	FRAMEn is asserted by the current Bus Master to indicate the beginning of a transfer. FRAMEn remains active low until the last Byte of the transfer is to be processed.
17	TRDYn	I/O	Target Ready (three-state). Asserted when the target is ready to complete the current data phase.
14	IRDYn	I/O	Initiator Ready. During a write, IRDYn asserted indicates that the initiator is driving valid data onto the data bus. During a read, IRDYn asserted indicates that the initiator is ready to accept data from the target device
19	STOPn	I/O	Asserted to indicate that the target wishes the initiator to stop the transaction in process on the current data phase.
18	DEVSELn	I/O	Device Select (three-state). Asserted when the target has decoded one of its addresses.
3	IDSEL	I	Initialization Device Select. Used as a chip select during configuration read and write transactions.
21	PERRn	I/O	Parity Error (three-state). Used to report parity errors during all PCI transactions except a special cycle. The minimum duration of PERRn is one clock cycle.
22	SERRn	I/O	System Error (open drain). This pin goes low when address parity errors are detected.
20	LOCKn	I	Indicates an atomic operation that may require multiple transactions to complete.

Table 1 : PCI Signals (Contd)

Pin Number	Pin Name	Type	Description
119	PMEn	O	The Power Management Event signal is an optional signal that can be used by a device to request a change in the device or system power state. The assertion and de-assertion of PMEn is asynchronous to CLK.
114	INTAn	O	PCI active low interrupt output (open-drain). This signal goes low (active) when an interrupt condition occurs.
115	INTBn	O	PCI active low interrupt output (open-drain). This signal goes low (active) when an interrupt condition occurs.
116	INTCn	O	PCI active low interrupt output (open-drain). This signal goes low (active) when an interrupt condition occurs.
112	REQn	O	Request indicates to the arbiter that this agent desires use of the bus. This is a point-to-point signal. Every master has its own REQn which must be tri-stated while RSTn is asserted.
113	GNTn	I	Gran*t* indicates to the agent that access to the bus has been granted. This is a point-to-point signal. Every master has its own GNTn which must be ignored while RSTn is asserted.
118	CLK	I	33 MHz PCI System Clock input.
117	RSTn	I	PCI system Reset (active low). Resets all internal registers, sequencers, and signals to a consistent state. During reset condition, AD (31:0) and SERRn are tri-stated.

11.2 Multiplexed Interface Signals

Table 2 lists the Multiplexed Interface Signal description for the concerned pin numbers. The functionality of multiplexed signal depends on the settings of mode select pins. The operation of MCS9865 is broadly classified into 5 different modes. This classification is detailed in Table 2, below.

Specific details of mode select pins can be seen in Table 5. Detailed description of multiplexed signals is listed in Table 6 (E.g.: Detailed description of signal “SP1_TXD”).

Table 2: Multiplexed Interface Signals

Pin Number	Multiplexed Interface Signal Descriptions as per Selected Mode				
	1SP	2SP-1PP	2SP-ISA	1PP	2PP
104	SP1_CTSn	SP1_CTSn	SP1_CTSn	NC	PP2_D[2]
103	SP1_DCDn	SP1_DCDn	SP1_DCDn	NC	PP2_D[1]
102	SP1_DSRn	SP1_DSRn	SP1_DSRn	NC	PP2_D[3]
101	SP1_RIn	SP1_RIn	SP1_RIn	NC	PP2_D[0]
100	SP1_RXD	SP1_RXD	SP1_RXD	NC	PP2_D[4]
99	SP1_DTRn	SP1_DTRn	SP1_DTRn	NC	PP2_D[6]
98	SP1_RTSn	SP1_RTSn	SP1_RTSn	NC	PP2_D[5]
95	SP1_TXD	SP1_TXD	SP1_TXD	NC	PP2_D[7]
94	NC	SP2_CTSn	SP2_CTSn	NC	PP2_ ACKn
93	NC	SP2_DCDn	SP2_DCDn	NC	PP2_ BUSY
92	NC	SP2_DSRn	SP2_DSRn	NC	PP2_ ERRORn/ FAULTn
91	NC	SP2_RIn	SP2_RIn	NC	PP2_ PAPEREND
90	NC	SP2_RXD	SP2_RXD	NC	PP2_ SELECTINn
89	NC	SP2_DTRn	SP2_DTRn	NC	PP2_ AUTOLFn
88	NC	SP2_RTSn	SP2_RTSn	NC	PP2_INITn
87	NC	SP2_TXD	SP2_TXD	NC	PP2_ STROBEn
86	NC	PP1_D [0]	ISAD [0]	PP1_D [0]	PP1_D [0]
83	NC	PP1_D [1]	ISAD [1]	PP1_D [1]	PP1_D [1]

Table 2: Multiplexed Interface Signals (Contd)

Pin Number	Multiplexed Interface Signal Descriptions as per Selected Mode				
	1SP	2SP-1PP	2SP-ISA	1PP	2PP
82	NC	PP1_D [2]	ISAD [2]	PP1_D [2]	PP1_D [2]
81	NC	PP1_D [3]	ISAD [3]	PP1_D [3]	PP1_D [3]
80	NC	PP1_D [4]	ISAD [4]	PP1_D [4]	PP1_D [4]
79	NC	PP1_D [5]	ISAD [5]	PP1_D [5]	PP1_D [5]
78	NC	PP1_D [6]	ISAD [6]	PP1_D [6]	PP1_D [6]
77	NC	PP1_D [7]	ISAD [7]	PP1_D [7]	PP1_D [7]
76	NC	PP1_BUSY	IRQC	PP1_BUSY	PP1_BUSY
75	NC	PP1_ACKn	IRQB	PP1_ACKn	PP1_ACKn
74	NC	PP1_PAPEREND	IRQA	PP1_PAPEREND	PP1_PAPEREND
71	NC	PP1_SELECT	IRQD	PP1_SELECT	PP1_SELECT
70	NC	PP1_ERRORn/ FAULTn	CSBn	PP1_ERRORn/ FAULTn	PP1_ERRORn/ FAULTn
69	NC	PP1_SELECTINn	A10	PP1_SELECTINn	PP1_SELECTINn
68	NC	PP1_INITn	RESET	PP1_INITn	PP1_INITn
65	NC	PP1_AUTOLFn	IOWn	PP1_AUTOLFn	PP1_AUTOLFn
64	NC	PP1_STROBEn	IORn	PP1_STROBEn	PP1_STROBEn
63	NC / BR3	PP1_PP_DIR / BR3	A[0] / BR3	PP1_PP_DIR / BR3	PP1_PP_DIR / BR3
62	NC	PP1_PERI_LOGIC_H	A[1]	PP1_PERI_LOGIC_H	PP1_PERI_LOGIC_H
59	NC / BR2	PP1_HOST_LOGIC_H / BR2	A[2] / BR2	PP1_HOST_LOGIC_H / BR2	PP1_HOST_LOGIC_H / BR2
58	NC / BR0	NC / BR0	CSAn / BR0	NC / BR0	PP2_PP_DIR / BR0
56	NC	NC	NC	NC	PP2_PERI_LOGIC_H
55	NC / BR1	NC / BR1	CSCn / BR1	NC / BR1	PP2_HOST_LOGIC_H / BR1
54	NC	NC	CSDn	NC	PP2_SELECT

Note: SP - Serial Port; PP - Parallel Port; ISA - Industry Standard Architecture.

Refer to Table 5 for details on BR0, BR1, BR2, BR3.

11.3 GPIO, Clock and Miscellaneous Signals

Table 3: GPIO, Clock and Miscellaneous Signals

Pin Number	Pin Name	Type	Drive Strength	Description
45	XTAL1	I	8 mA	Crystal oscillator input. This input signal is used in conjunction with XTAL2 to form a feedback circuit for the internal timing. Two external capacitors connected from Ground to XTAL1, XTAL2 are required to form a crystal oscillator circuit
46	XTAL2	I/O	8 mA	Crystal oscillator output. See XTAL1 description.
48-51	GPIO [1:4]	I/O	4 mA	General purpose I/O Pins. These pins are GPIOs in all modes.
52	EE_SCL	I/O	4 mA	2-Wire EEPROM Clock. Connect this pin to 3.3V through 2.2K resistor
53	EE_SDA	I/O	4 mA	2-Wire EEPROM Data in/out. Connect this pin to 3.3V through 2.2K resistor
105	TEST_EN	I	-	Test enable pin. It should be No Connect at System Level, for normal functionality
106	SCAN_EN	I	-	Scan enable pin. It should be No Connect at System Level, for normal functionality
107	TV_MODE	I	-	Test Vector mode pin. It should be No Connect at System Level, for normal functionality

11.4 Power and Ground Signals

Table 4: Power and Ground Signals

Pin Number	Pin Name	Type	Description
15, 38, 121	GNDIO	Ground	I/O ground- Digital
66, 72, 84, 96	GNDIO	Ground	I/O ground- Digital
47	GNDIO_OSC	Ground	I/O Oscillator ground
61	GND18AC_PLL	Ground	Analog PLL ground
16, 39, 122	VCC3IO	Power	I/O Power Input - 3.3V Digital
44	VCC3IO_OSC	Power	I/O Oscillator Power input - 3.3V Digital-Osc
57	VCCK	Power	Core Power input - 1.8V Digital
60	VCC18AC_PLL	Power	PLL Power input - 1.8V PLL
67, 73, 85, 97	VCC3IO	Power	I/O Power input - 3.3V Digital
109	VCC33	Power	Regulator Power output 3.3V – Refer to note1
108	VCC18	Power	1.8V Power Output / Input - Refer to note1
110	VCC5A	Power	5 V Power input – Refer to note1
111	GND5A	Ground	Analog ground for 5 V input

Note1 :

A) When PIN-110 is powered from 5V, PIN-108(VCC18) will act as 1.8V Power output & PIN109 will act as 3.3V Power output.

B) When PIN-110 is NC, PIN-108(VCC18) acts as Power input. Under this condition external 1.8V needs to be connected PIN-108.

In this condition PIN109 will not give 3.3V output & leave this pin as No Connect. 3.3V needs to be generated externally for MCS9865 functionality in this condition.

C) Instructions given above are important for Mini-PCI based system designs, contact techsupport@moschip.com for any additional data or queries.

12. Mode Selection – System level settings

The Mode selections are controlled via a bootstrap register. The bootstrap register is loaded with values based on the logic levels of the bootstrap pins immediately after reset is inactivated. BR0 to BR4, are Boot Strap pins.

Table 5: Mode Selection – System Level settings

Configuration	BR3 Pin # 63	BR2 Pin # 59	BR1 Pin # 55	BR0 Pin # 58
1SP	PD	PU	PD	PD
2SP-1PP	PD	PU	PU	PD
2SP-ISA	PD	PU	PD	PU
1PP	PD	PD	PU	PU
2PP	PD	PD	PU	PD

In Above Table “PD” refers to particular pin being connected to “GNDIO through 10K Resistor” and “PU” refers to particular pin being connected to “VCC3IO through 10K Resistor”

13. Description of Multiplexed Signals

Table 6: Multiplexed Signals Description

Signal Name	Group	Type	Drive Strength	Description
SP1_ CTSn	SP	I	12 mA	Serial Port 1 Clear To Send (in serial protocol), active low
SP1_ DCDn	SP	I	12 mA	Serial Port 1 Data Carrier Detect (in serial protocol), active low
SP1_ DSRn	SP	I	12 mA	Serial Port 1 Data Set Ready (in serial protocol), active low
SP1_DTRn	SP	O	12 mA	Serial Port 1 Data Terminal Ready (in serial protocol), active low
SP1_RIn	SP	I	12 mA	Serial Port 1 Ring Indicator, active low
SP1_RTSn	SP	O	12 mA	Serial Port 1 Request To Send (in serial protocol), active low
SP1_RXD	SP	I	12 mA	Serial Port 1 Serial Receive Data in from transceiver or IrDA data in from IrDA detector

Table 6: Multiplexed Signals Description (Contd)

Signal Name	Group	Type	Drive Strength	Description
SP1_TXD	SP	O	12 mA	Serial Port 1 Transmit Data out to transceiver, or IrDA data out to IR LED
SP2_ CTSn	SP	I	4 mA	Serial Port 2 Clear To Send (in serial protocol), active low
SP2_ DCDn	SO	I	4 mA	Serial Port 2 Data Carrier Detect (in serial protocol), active low
SP2_ DSRn	SP	I	4 mA	Serial Port 2 Data Set Ready (in serial protocol), active low
SP2_ DTRn	SP	O	12 mA	Serial Port 2 Data Terminal Ready (in serial protocol), active low
SP2_ RTSn	SP	O	12 mA	Serial Port 2 Request To Send (in serial protocol), active low
SP2_ RXD	SP	I	12 mA	Serial Port 2 Serial Receive Data in from transceiver or IrDA data in from IrDA detector
SP2_ TXD	SP	O	12 mA	Serial Port 2 Transmit Data out to transceiver, or IrDA data out to IR LED
SP2_RIn	SP	I	4 mA	Serial Port 2 Ring Indicator, active low
PP1_STROBEn	PP	O	12 mA	Set active low by the host to transfer data into the input latch of the peripheral. Data are valid while STROBEn is low
PP1_AUTOLFn	PP	O	12 mA	The interpretation of this signal varies from peripheral to peripheral. Set low by host to put some printers into auto-line feed mode
PP1_INITn	PP	O	12 mA	Initialize the Peripheral / printer (open drain, active low). When set low, the peripheral or printer starts it's initialization routine
PP1_SELECTINn	PP	O	12 mA	Set low by host to select peripheral
PP1_ACKn	PP	I	4 mA	Pulsed low by the peripheral to acknowledge transfer of a data byte from the host

Table 6: Multiplexed Signals Description (Contd)

Signal Name	Group	Type	Drive Strength	Description
PP1_BUSY	PP	I	4 mA	Driven high by the peripheral to indicate that it is not ready to receive data
PP1_PAPEREND	PP	I	4 mA	Driven high by the peripheral to indicate that is has encountered an error in its paper path. The meaning of this signal varies from peripheral to peripheral. Peripherals shall set ERRORn/ FAULTn low whenever PAPEREND is set high
PP1_SELECT	PP	I	4 mA	Set high to indicate that the peripheral is online
PP1_ERRORn/ FAULTn	PP	I	4 mA	Set low by the peripheral to indicate that an error has occurred. The meaning of this signal varies from peripheral to peripheral
PP1_D [7:0]	PP	I/O	12 mA	Driven by the host in Compatibility Mode and the negotiation phase, not used in Nibble Mode, and bidirectional in all other modes
PP1_PP_DIR	PP	O	8 mA	Set low to indicate a data transfer direction of peripheral to host and set high to indicate a data transfer direction of host to peripheral
PP1_PERI_LOGIC_H	PP	I	8 mA	Set high to indicate that all other signals sourced by the peripheral are in a valid state. Set low to indicate that the peripheral power is off or that peripheral-driven interface signals are otherwise in an invalid state.
PP1_HOST_LOGIC_H	PP	O	8 mA	Set high to indicate that all other signals sourced by the host are in a valid state. Set low to indicate the host power is off or host-driven interface signals are otherwise in an invalid state
PP2_STROBEn	PP	O	12 mA	Set active low by the host to transfer data into the input latch of the peripheral. Data are valid while STROBEn is low
PP2_AUTOLFn	PP	O	12 mA	The interpretation of this signal varies from peripheral to peripheral. Set low by host to put some printers into auto-line feed mode

Table 6: Multiplexed Signals Description (Contd)

Signal Name	Group	Type	Drive Strength	Description
PP2_INITn	PP	O	12 mA	Initialize the Peripheral / printer (open drain, active low). When set low, the peripheral or printer starts it's initialization routine
PP2_SELECTINn	PP	O	12 mA	Set low by host to select peripheral
PP2_ACKn	PP	I	4 mA	Pulsed low by the peripheral to acknowledge transfer of a data byte from the host
PP2_BUSY	PP	I	4 mA	Driven high by the peripheral to indicate that it is not ready to receive data
PP2_PAPEREND	PP	I	4 mA	Driven high by the peripheral to indicate that is has encountered an error in its paper path. The meaning of this signal varies from peripheral to peripheral. Peripherals shall set ERRORn/ FAULTn low whenever PAPEREND is set high
PP2_SELECT	PP	I	8 mA	Set high to indicate that the peripheral is online
PP2_ERRORn/ FAULTn	PP	I	4 mA	Set low by the peripheral to indicate that an error has occurred. The meaning of this signal varies from peripheral to peripheral
PP2_D [7:0]	PP	I/O	12 mA	Driven by the host in Compatibility Mode and the negotiation phase, not used in Nibble Mode, and bidirectional in all other modes
PP2_PP_DIR	PP	O	8 mA	Set low to indicate a data transfer direction of peripheral to host and set high to indicate a data transfer direction of host to peripheral
PP2_PERI_LOGIC_H	PP	I	8 mA	Set high to indicate that all other signals sourced by the peripheral are in a valid state. Set low to indicate that the peripheral power is off or that peripheral-driven interface signals are otherwise in an invalid state.
PP2_HOST_LOGIC_H	PP	O	8 mA	Set high to indicate that all other signals sourced by the host are in a valid state. Set low to indicate the host power is off or host-driven interface signals are otherwise in an invalid state

Table 6: Multiplexed Signals Description (Contd)

Signal Name	Group	Type	Drive Strength	Description
A [2:0]	ISA	O	8 mA	External Peripheral Address Lines
IORn	ISA	O	12 mA	Active-low external peripheral I/O read signal
IOWn	ISA	O	12 mA	Active-low external peripheral I/O write signal
CSAn	ISA	O	8 mA	Chip select line to select one of the ports of external peripheral
CSBn	ISA	O	4 mA	Chip select line to select one of the ports of external peripheral
CSCn	ISA	O	8 mA	Chip select line to select one of the ports of external peripheral
CSDn	ISA	O	8 mA	Chip select line to select one of the ports of external peripheral
IRQA	ISA	I	4 mA	Interrupt line for one of the ports of external peripheral
IRQB	ISA	I	4 mA	Interrupt line for one of the ports of external peripheral
IRQC	ISA	I	4 mA	Interrupt line for one of the ports of external peripheral
IRQD	ISA	I	4 mA	Interrupt line for one of the ports of external peripheral
RESET	ISA	O	12 mA	External Peripheral Reset Signal.
A_10	ISA	O	12 mA	Reserved Pin
ISAD [7:0]	ISA	I/O	12 mA	External Peripheral Data Bus
NC	-	-	-	No connection.

14. Architectural overview

14.1 Brief description of block diagram

MCS9865 consists of 3 major blocks namely PCI Target Controller, Bridge (MSIF and TSIF) and Device core.

Device core consists following major blocks and Peripherals:

- TXDMA block
- RXDMA block
- 2 Serial ports
- 2 Parallel port
- ISA

14.2 PCI Target Controller

PCI controller is a 33 MHz 32-bit PCI 2.3 Complaint Target controller. The execution of PCI Bus transactions take place in broadly five stages: address phase; transaction claiming; data phase(s); final data transfer; and transaction completion.

14.3 Bridge

Main function of bridge is to maintain link between PCI and device core including all the peripherals configured on the other side of PCI. Bridge also takes care of all the interrupt logics i.e. generation, acknowledgments, etc. It includes mainly two blocks to form a channel between PCI and device core i.e. Master Interface (MSIF) & Application Slave Interface (TSIF).

Master slave Interface (MSIF) is the block between the device core and PCI Core and it converts all the device core transactions to the PCI compatible. It forms the header for the DMA transactions. It will generate the interrupts on INTA, INTB, INTC, and INTD and also generates interrupts through MSI (Message Signal Interrupt) mechanism.

Target Slave Interface (TSIF) is used to configure the registers of the peripherals.

14.4 Device Core

Device core contains all the peripherals i.e. two serial ports, two parallel ports, ISA interface, and TXDMA & RXDMA.

14.4.1 TXDMA Block

This block transfers data from system memory to peripherals.

14.4.2 RXDMA Block

This block transfers data from peripherals to system memory.

14.4.3 Serial Port

Serial port implemented in the MCS9865 is compatible with 16C 450 / 550 / Ex 550 UART modes. Serial port controllers can be interfaced to external RS232 / RS422 / RS485 transceivers. Serial port module consists of TxDMA, RxDMA and UART core. TxDMA requests the data from system memory through DMA. Data, which is coming from system memory, will go into TX FIFO. 8 bit data from the TX FIFO controllers goes to the UART core. UART core will convert 8 bit data to serial data.

Similarly RXDMA enables data transfer from peripheral to System memory. Data coming from peripheral, will go into RX FIFO and then into System memory.

256 Bytes of TX FIFO & 256 Bytes of RX FIFO are used in MCS9865 for each Serial Port. These deep FIFO enable faster device operation & less CPU Load.

14.4.4 Parallel Port

The parallel port of MCS9865 implements the IEEE 1284 compliant standard parallel port. Accordingly, all of the various IEEE1284 modes are supported:

- Nibble Mode
- Byte Mode
- Enhanced Parallel Port (EPP 1.9)
- Extended Capability Port (ECP) with and without RLE
- FIFO mode(Buffered SPP modes)

14.4.5 ISA Interface

An ISA Bridge allows the product designer to increase the number of I/O Ports through the use of external components. Additional UARTs and Parallel Ports are easy to attach and configure. ISA bus operates at 8MHz with an 8-bit Data Bus. ISA interface supports both Intel & Motorola mode of data bus.

Following I/O expansion is feasible through MCS9865 ISA Interface, by using appropriate ISA Peripheral at system level :

- 1 Serial Port
- 2 Serial Ports
- 3 Serial Ports
- 4 Serial Ports
- 1 Serial + 1 Parallel Port
- 2 Serial + 1 Parallel Port
- 2 Parallel Ports

15. EEPROM Contents

EEPROM contents shared through separate application note. Write to techsupport@moschip.com for EEPROM data.

16. Extended Modes through EEPROM

As explained in the earlier sections, MCS9865 can support 5 Peripheral configurations through mode select pins without using external EEPROM. These 5 Peripheral configurations are tabulated below.

S.No	Possible product Configuration	Is EEPROM Must?	Is Mode selection at system level required?
1	PCI to 1 Serial	No	Yes
2	PCI to 2 Serial + 1 Parallel	No	Yes
3	PCI to 6 Serial = PCI to 2 Serial + ISA (4 Serial)	No	Yes
4	PCI to 1 Parallel	No	Yes
5	PCI to 2 Parallel	No	Yes

By using external EEPROM, more Peripheral configurations can be derived with MCS9865. A few such configurations are listed below:

S.No	Possible product Configuration	Is EEPROM Must?	Is Mode selection at system level required?
1	PCI to 1 Serial + 1 Parallel	Yes	Yes
2	PCI to 1 Serial + 2 Parallel = PCI to 1 Serial + ISA (2 Parallel)	Yes	Yes
3	PCI to 2 Serial + 2 Parallel = PCI to 2 Serial + ISA (2 Parallel)	Yes	Yes
4	PCI to 3 Serial = PCI to 2 Serial + ISA (1 Serial)	Yes	Yes
5	PCI to 4 Serial = PCI to 2 Serial + ISA (2 Serial)	Yes	Yes
6	PCI to 5 Serial = PCI to 2 Serial + ISA (3 Serial)	Yes	Yes
7	PCI to 3 Serial + 1 Parallel = PCI to 2 Serial + ISA (1 Serial + 1 Parallel)	Yes	Yes
8	PCI to 4 Serial + 1 Parallel = PCI to 2 Serial + ISA (2 Serial + 1 Parallel)	Yes	Yes

Vendor ID and Product ID customizations can also be implemented in the MCS9865, through external EEPROM.

17. General Purpose IO lines

Up to four General Purpose I/O (GPIO) pins are present in the device for system control. Refer to GPIO application note for details. Write to techsupport@moschip.com for further details.

18. Electrical Specifications

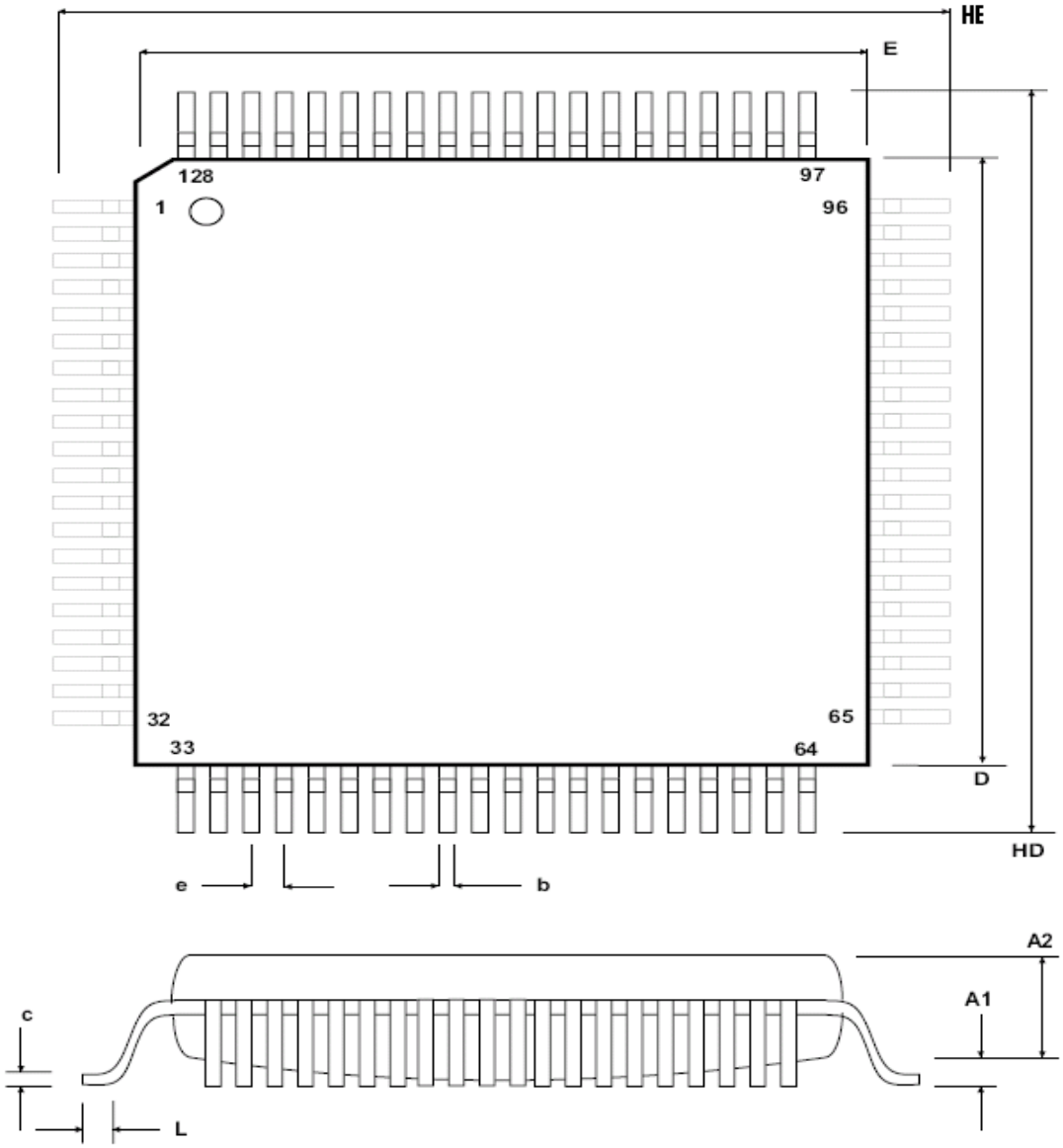
Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
VCC_K	Core Power Supply	-0.3 to 2.0	V
VCC_{3IO}	Power Supply of 3.3V I/O	-0.3 to 3.7	V
Vin_3	Input Voltage of 3.3V I/O	-0.3 to 3.7	V
Vin_5	Input Voltage of 5V Tolerant I/O	-0.3 to 5.5	V
T_O	Operating Temperature	-40 to +85	^oC
T_s	Storage Temperature	-40 to +150	^oC
ESD HBM	MIL-STD 883E Method 3015-7 Class 2	2000	V
ESD MM	JEDEC EIA/JESD22 A115-A	200	V
CDM	JEDEC/JESD22 C101-A	500	V
Latch-up	JESD No. 78, March 1997	200mA, 1.5 x VCC	
T_J	Junction Temperature	110	^oC

Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
VCC_{5A}	5V Power Supply Input	4.5	5.0	5.5	V
I_{VCC5}	5V Current w/o Peripheral Load, when internal 3.3V & 1.8 Regulators are used		30		mA
VCC_K	Core Power Supply Input	1.62	1.8	1.98	V
I_{VCC18}	Core Current w/o Peripheral Load		25		mA
VCC_{3IO}	IO Power Supply Input	2.97	3.3	3.63	V
I_{VCC3IO}	IO Current w/o Peripheral Load		25		mA
Vin – I/O	Input Voltage of 3.3V I/O which is 5V Tolerant (Peripheral I/O pins of Serial, Parallel, ISA & PCI interfaces)	0	3.3	5	V
	Input Voltage of $3.3V_{only}$ I/O (XTAL1 & XTAL2)	0	3.3	3.63	V
VCC18	1.8V Regulator Output	1.71	1.8	1.89	V
I_{Reg18}	1.8V Regulator Current			70	mA
VCC33	3.3V Regulator Output	3.14	3.3	3.46	V
I_{Reg33}	3.3V Regulator Current			250	mA

19. Mechanical Specifications – LQFP 128



128-PIN LQFP
Package Dimensions

Symbol	Min	Millimeters Typ	Max
A1	0.05		-
A2	1.35		1.45
b	0.13		0.23
c	0.09		0.20
e		0.40	
L	0.45		0.75
HD	15.85	16	16.15
D	13.90	14	14.10
HE	15.85	16	16.15
E	13.90	14	14.10

20. Contact information

For Commercial information & availability write to: sales@moschip.com

For Technical information write to: techsupport@moschip.com

Revision history

Date	Reason for change	Version
17th Dec 2007	Initial Draft	0.1
14th Feb 2008	Pin Numbers are added in PIN Description and Mechanical dimensions are added	0.2
12th Mar 2008	PIN 110 & 108 description Updated	0.3
20th Mar 2008	Aesthetic changes made for Pin Description Table formatting & Operating temperature changed to -40 to +85 deg C	0.4
12th April 2008	Pin Out diagrams added for 5 Modes	0.5
9th May 2008	Preliminary text removed from Footer, Software Support updated & Ordering Part Number changed from MCS9865CV-AA to MCS9865IV-AA	1.0