MCS9845

PCI Dual UART with ISA Bridge

Features

- 5V Operation
- Low Power
- PCI compatible dual UART
  - 16-Byte Transmit & Receive FIFOs
  - Programmable Baud Rate Generators
  - Modem Control Signals
  - 5, 6, 7, & 8-bit Characters
  - Even, Odd, No Parity, or Force Parity
  - Status report capability
  - Compatible with 16C550
  - Supports serial data rates up to 115 Kbps
- ISA Bridge for External I/O
  - 3 Address Lines
  - 4 Active-High Interrupts
  - 1 Active-Low Interrupt
  - 4 External Chip Selects
- Re-map function for Legacy Ports
- 128-pin “Lead Free” QFP Package

Applications

- I/O Bridge
- Portable Backup Units
- Embedded Applications
- High Speed Modems
- Monitoring Equipment
- Add-on I/O Cards
- Serial Networking

Application Notes

- AN-9845-4S1P-PCI5V
- AN-9845-4S-PCI5V
- AN-9845-6S-PCI5V

Evaluation Board

- MCS9845-EVB

Ordering Information		
Commercial Grade (0 °C to +70 °C)		
MCS9845CV	128-QFP	RoHS

General Description

The MCS9845 is a PCI based dual-channel high performance UART, plus a PCI to ISA Bridge.

The MCS9845 offers 16-Byte transmit and receive FIFOs for each UART channel. The MCS9845 performs serial-to-parallel conversions on data received from a peripheral device, and parallel-to-serial conversions on data received from its CPU. Both UARTs are fully compatible with the 16C550.

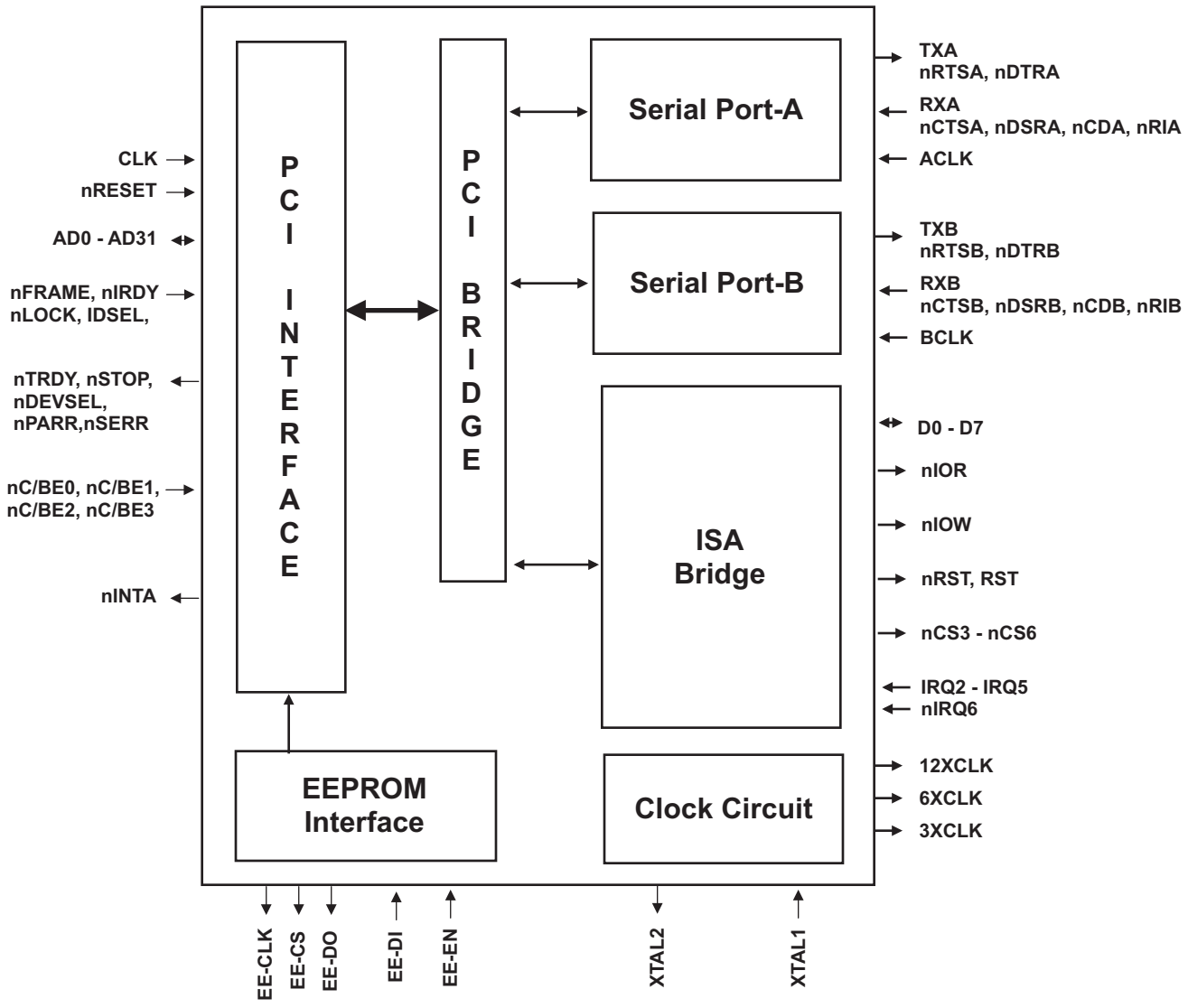
The ISA Bridge allows adding external ISA style components. These can be used to add additional Serial or Parallel Ports.

The MCS9845 is ideally suited for PC applications, such as high speed COM ports and parallel ports. The MCS9845 is available in a 128-pin QFP package. It is fabricated using an advanced submicron CMOS process to achieve low drain power and high-speed requirements.

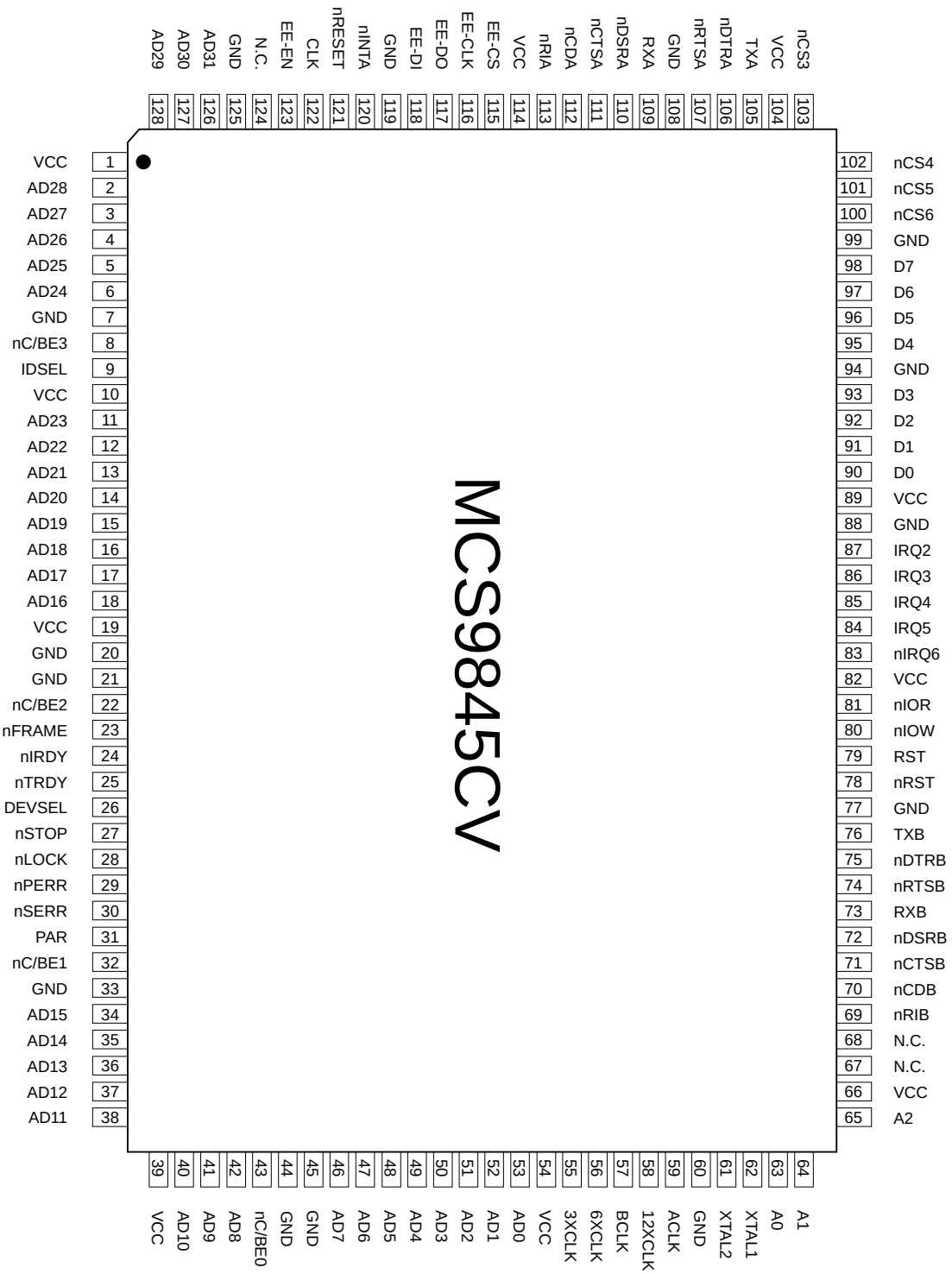
The MCS9845 is a pin-compatible replacement for the previous Nm9845. The Nm9845 is no longer offered.

MosChip Semiconductor ♦ 3335 Kifer Rd, Santa Clara, CA 95051 ♦ Tel (408) 737-7141 ♦ Fax (408) 737-7708

Block Diagram



Pin-Out


MCS9845CV
1 VCC
2 AD28
3 AD27
4 AD26
5 AD25
6 AD24
7 GND
8 nC/BE3
9 IDSEL
10 VCC
11 AD23
12 AD22
13 AD21
14 AD20
15 AD19
16 AD18
17 AD17
18 AD16
19 VCC
20 GND
21 GND
22 nC/BE2
23 nFRAME
24 nIRDY
25 nTRDY
26 DEVSEL
27 nSTOP
28 nLOCK
29 nPERR
30 nSERR
31 PAR
32 nC/BE1
33 GND
34 AD15
35 AD14
36 AD13
37 AD12
38 AD11
39 VCC
40 AD10
41 AD9
42 AD8
43 nC/BE0
44 GND
45 GND
46 AD7
47 AD6
48 AD5
49 AD4
50 AD3
51 AD2
52 AD1
53 AD0
54 VCC
55 3XCLK
56 6XCLK
57 BCLK
58 12XCLK
59 ACLK
60 GND
61 XTAL2
62 XTAL1
63 A0
64 A1
65 A2
66 VCC
67 N.C.
68 N.C.
69 nRIB
70 nCDB
71 nCTSB
72 nDSRB
73 RXB
74 nRTSB
75 nDTRB
76 TXB
77 GND
78 nRST
79 RST
80 nIOW
81 nIOR
82 VCC
83 nIRQ6
84 IRQ5
85 IRQ4
86 IRQ3
87 IRQ2
88 GND
89 VCC
90 D0
91 D1
92 D2
93 D3
94 GND
95 D4
96 D5
97 D6
98 D7
99 GND
100 nCS6
101 nCS5
102 nCS4
103 nCS3
104 VCC
105 TXA
106 nDTRA
107 nRTSA
108 GND
109 RXA
110 nDSRA
111 nCTSA
112 nCDA
113 nRIA
114 VCC
115 EE-CS
116 EE-CLK
117 EE-DO
118 EE-DI
119 GND
120 nINTA
121 nRESET
122 CLK
123 EE-EN
124 N.C.
125 GND
126 AD31
127 AD30
128 AD29

Pin Assignments

Name	Pin	Type	Description
CLK	122	I	33 MHz PCI System Clock input.
nRESET	121	I	PCI system Reset (active low). Resets all internal registers, sequencers, and signals to a consistent state. During reset condition, AD31-0 and nSER are tri-stated.
AD31-29	126-128	I/O	Multiplexed PCI Address/Data bus. During the address phase, AD31-0 contain a physical address. Data is stable and valid when nIRDY and nTRDY are asserted (active).
AD28-24	2-6	I/O	See AD31-29 description.
AD23-16	11-18	I/O	See AD31-29 description.
AD15-11	34-38	I/O	See AD31-29 description.
AD10-8	40-42	I/O	See AD31-29 description.
AD7-0	46-53	I/O	See AD31-29 description.
nFRAME	23	I	nFRAME is asserted by the current Bus Master to indicate the beginning of an transfer. nFRAME remains active until the last Byte of the transfer is to be processed.
nIRDY	24	I	Initiator Ready. During a write, nIRDY asserted indicates that the initiator is driving valid data onto the data bus. During a read, nIRDY asserted indicates that the initiator is ready to accept data from the target device.
nTRDY	25	O	Target Ready (three-state). Asserted when the target is ready to complete the current data phase.
nSTOP	27	O	Asserted to indicate that the target wishes the initiator to stop the transaction in process on the current data phase.
nLOCK	28	I	Indicates an atomic operation that may require multiple transactions to complete.
IDSEL	9	I	Initialization Device Select. Used as a chip select during configuration read and write transactions.
nDEVSEL	26	O	Device Select (three-state). Asserted when the target has decoded one of its addresses.
nPERR	29	O	Parity Error (three-state). Used to report parity errors during all PCI transactions except a special cycle. The minimum duration of nPERR is one clock cycle.
nSERR	30	O	System Error (open drain). This pin goes low when address parity errors are detected.
PAR	31	I/O	Parity. Even Parity is applied across AD31-0 and nC/BE3-0. PAR is stable and valid one clock after the address phase. For the data phase, PAR is stable and valid one clock after either nIRDY is asserted on a write transaction, or nTRDY is asserted on a read transaction.

Name	Pin	Type	Description
nC/BE3	8	I	Bus Command and Byte Enable. During the address phase of a transaction, nC/BE3-0 defines the bus command. During the data phase, nC/BE3-0 are used as Byte Enables. nC/BE3 applies to Byte “3”.
nC/BE2	22	I	Bus Command and Byte Enable. During the address phase of a transaction, nC/BE3-0 defines the bus command. During the data phase, nC/BE3-0 are used as Byte Enables. nC/BE3 applies to Byte “2”.
nC/BE1	32	I	Bus Command and Byte Enable. During the address phase of a transaction, nC/BE3-0 defines the bus command. During the data phase, nC/BE3-0 are used as Byte Enables. nC/BE3 applies to Byte “1”.
nC/BE0	43	I	Bus Command and Byte Enable. During the address phase of a transaction, nC/BE3-0 defines the bus command. During the data phase, nC/BE3-0 are used as Byte Enables. nC/BE3 applies to Byte “0”.
nINTA	120	O	PCI active low interrupt output (open-drain). This signal goes low (active) when an interrupt condition occurs.
EE-CS	115	O	External EEPROM chip select (active high). After Power-On Reset, the EEPROM is read, and the read-only configuration registers are filled sequentially from the first 64 Bytes in the EEPROM.
EE-CLK	116	O	External EEPROM clock.
EE-DI	118	I	External EEPROM data input.
EE-DO	117	O	External EEPROM data output.
EE-EN	123	I	Enable EEPROM (active high, internal pull-up). The external EEPROM can be disabled when this pin is tied to GND or pulled low. When the EEPROM is disabled, default values for PCI configuration registers will be used.
XTAL1	62	I	Crystal oscillator input or external clock input pin (22.1184 MHz). This signal input is used in conjunction with XTAL2 to form a feedback circuit for the internal timing. Two external capacitors (10pF) connected from each side of the XTAL1 and XTAL2 to GND are required to form a crystal oscillator circuit.
XTAL2	61	O	Crystal oscillator output. See XTAL1 description.
12XCLK	58	O	Master clock divided by 12 (1.8432 MHz) Standard UART clock for 115.2K data rate.
6XCLK	56	O	Master clock divided by 6 (3.6864 MHz) Reserved pin. No connection.
3XCLK	55	O	Master clock divided by 3 (7.3728 MHz) Reserved pin. No connection.
ACLK	59	I	UART-A clock input. ACLK should be connected to the 12XCLK output pin.

Name	Pin	Type	Description
BCLK	57	I	UART-B clock input. BCLK should be connected to the 12XCLK output pin.
TXA	105	O	UART-A serial Data Output.
nRTSA	107	O	UART-A Request-To-Send signal. It is set high (inactive) after a hardware Reset or during internal Loop-Back mode. When low, this indicates that UART-A is ready to transfer data. nRTSA has no effect on the transmitter or receiver.
nDTRA	106	O	UART-A Data-Terminal-Ready signal. It is set high (inactive) after a hardware Reset or during internal Loop-Back mode. When low, this output indicates to the modem or data set that UART-A is ready to establish a communication link. nDTRA has no effect on the transmitter or receiver.
RXA	109	I	UART-A, serial Data Input.
nCTSA	111	I	UART-A Clear-To-Send signal. When low, this indicates that the modem or data set is ready to exchange data. nCTSA has no effect on the transmitter.
nDSRA	110	I	UART-A Data-Set-Ready signal. When low, this indicates the modem or data set is ready to establish a communication link.
nCDA	112	I	UART-A Carrier-Detect signal. When low, this indicates the modem or data set has detected the data carrier. nCDA has no effect on the transmitter.
nRIA	113	I	UART-A Ring-detect signal.
TXB	76	O	UART-B serial Data Output.
nRTSB	74	O	UART-B Request-To-Send signal. It is set high (inactive) after a hardware Reset or during internal Loop-Back mode. When low, this indicates UART-B is ready to exchange data. nRTSB has no effect on the transmitter or receiver.
nDTRB	75	O	UART-B Data-Terminal-Ready signal. It is set high (inactive) after a hardware Reset or during internal Loop-Back mode. When low, this indicates to the modem or data set that UART-B is ready to establish a communication link. nDTRB has no effect on the transmitter or receiver.
RXB	73	I	UART-B, serial Data Input.
nCTSB	71	I	UART-B Clear-To-Send signal. When low, this indicates the modem or data set is ready to exchange data. nCTSB has no effect on the transmitter.
nDSRB	72	I	UART-B Data-Set-Ready signal. When low, this indicates the modem or data set is ready to establish a communication link.

Name	Pin	Type	Description
nCDB	70	I	UART-B Carrier-Detect signal. When low, this indicates the modem or data set has detected the Data Carrier. nCDB has no effect on the transmitter.
nRIB	69	I	UART-B ring-detect signal.
nCS3	103	O	Chip Select 3 (Active-Low).
nCS4	102	O	Chip Select 4 (Active-Low).
nCS5	101	O	Chip Select 5 (Active-Low).
nCS6	100	O	Chip Select 6 (Active-Low).
IRQ5-2	84-87	I	Active-High Interrupt inputs. All unused interrupts must be connected to GND for proper operation.
nIRQ6	83	I	Active-Low Interrupt input. This pin should be tied to Vcc if it is not used.
nIOR	81	O	External Peripheral Read signal (Active-Low).
nIOW	80	O	External Peripheral Write signal (Active-Low).
RST	79	O	External Peripheral Reset Signal (Active-High).
nRST	78	O	External Peripheral Reset Signal (Active-Low).
A0-2	63-65	O	External Peripheral Address Lines.
D7-D4	98-95	I/O	External Peripheral Data Bus.
D3-D0	93-90	I/O	External Peripheral Data Bus.
GND	7,20,21, 33,44,45, 60,77,88, 94,99,108 119,125	Pwr	Power and signal ground.
Vcc	1,10,19, 39,54,66, 82,89,104, 114	Pwr	Supply. Voltage

PCI Bus Operation:
The execution of PCI Bus transactions take place in broadly five stages: address phase; transaction claiming; data phase(s); final data transfer; and transaction completion.

Address Phase:
Every PCI transaction starts with an address phase, one PCI clock period in duration. During the address phase the initiator (also known as the current Bus Master) identifies the target device (via the address) and type of transaction (via the command). The initiator drives the 32-bit address onto the Address/Data Bus, and a 4-bit command onto the Command/Byte-Enable Bus. The initiator also asserts the nFRAME signal during the same clock cycle to indicate the presence of valid address and transaction information on those buses. The initiator supplies the starting address and command type for one PCI clock cycle. The target generates the subsequent sequential addresses for burst transfers. The Address/Data Bus becomes the Data Bus, and the Command/Byte-Enable Bus becomes the Byte-Enable Bus for the remainder of the clock cycles in that transaction. The target latches the address and command type on the next rising edge of PCI clock, as do all other devices on that PCI bus. Each device then decodes the address and determines whether it is the intended target, and also decodes the command to determine the type of transaction.

Claiming The Transaction:
When a device determines that it is the target of a transaction, it claims the transaction by asserting nDEVSEL.

Data Phase(s):
The data phase of a transaction is the period during which a data object is transferred between the initiator and the target. The number of data Bytes to be transferred during a data phase is determined by the number of Command/Byte-Enable signals that are asserted by the initiator during the data phase. Each data phase is at least one PCI clock period in duration. Both initiator and target must indicate that they are ready to complete a data phase. If not, the data phase is extended by a wait state of one clock period in duration. The initiator and the target indicate this by asserting nIRDY and nTRDY respectively and the data transfer is completed at the rising edge of the next PCI clock.

Transaction Duration:
The initiator, as stated earlier, gives only the starting address during the address phase. It does not tell the number of data transfers in a burst transfer transaction. The target will automatically generate the addresses for subsequent Data Phase transfers. The initiator indicates the completion of a transaction by asserting nIRDY and de-asserting nFRAME during the last data transfer phase. The transaction does not actually complete until the target has also asserted the nTRDY signal and the last data transfer takes place. At this point the nTRDY and nDEVSEL are de-asserted by the target.

Transaction Completion:
When all of nIRDY, nTRDY, nDEVSEL, and nFRAME are in the inactive state (high state), the bus is in idle state. The bus is then ready to be claimed by another Bus Master.

PCI Resource Allocation

PCI devices do not have "Hard-Wired" assignments for memory or I/O Ports like ISA devices do. PCI devices use "Plug & Play" to obtain the required resources each time the system boots up. Each PCI device can request up to six resource allocations. These can be blocks of memory (RAM) or blocks of I/O Registers. The size of each resource block requested can also be specified, allowing great flexibility. Each of these resource blocks is accessed by means of a Base-Address-Register (BAR). As the name suggests, this is a pointer to the start of the resource. Individual registers are then addressed using relative offsets from the Base-Address-Register contents. The important thing to note is: plugging the same PCI card into different machines will not necessarily result in the same addresses being assigned to it. For this reason, software (drivers, etc.) must always obtain the specific addresses for the device from the PCI System.

Each PCI device is assigned an entry in the PCI System's shared "Configuration Space". Every device is allocated 256 Bytes in the Configuration Space. The first 64 Bytes must follow the conventions of a standard PCI Configuration "Header". There are several pieces of information the device must present in specific fields within the header to allow the PCI System to properly identify it. These include the Vendor-ID, Device-ID and Class-Code. These three fields should provide enough information to allow the PCI System to associate the correct software driver with the hardware device. Other fields can be used to provide additional information to further refine the needs and capabilities of the device.

As part of the Enumeration process (discovery of which devices are present in the system) the Base-Address-Registers are configured for each device. The device tells the system how many registers (etc.) it requires, and the system maps that number into the system's resource space, reserving them for exclusive use by that particular device. No guarantees are made that any two requests for resources will have any predictable relationship to each other. Each PCI System is free to use its own allocation strategy when managing resources.

Multi-Function Devices

MosChip uses the Subsystem-ID field to indicate how many Serial Ports and Parallel Ports are provided by the current implementation. By changing the data in the Subsystem-ID field, and stuffing only the appropriate number of external components, the same board could be used for products with either one or two Ports. The least significant Hexadecimal digit of the Subsystem-ID field indicates the number of Serial Ports that are currently being provided by the device. The next higher digit indicates the number of Parallel Ports being provided. The table below shows several different combinations and the types of Ports that would be enabled. Some MosChip devices provide Serial Ports, some provide Parallel Ports, and some provide both types of Ports. This field is used as an aid to the software Drivers, allowing them to easily determine how many of each Port type to configure.

Subsystem-ID	Parallel Ports	Serial Ports
0001	0	1
0010	1	0
0012	1	2

This use of the term "Multi-Function Device" should not be confused with the more generic use of that term by the PCI System. Each "Function" within a "Unit" (physical device) gets its own Configuration Space Header. MosChip's devices do not need this extra layer of complexity, the six Base Address Registers provided by one PCI "Function" are more than adequate to allocate all of the desired resources.

External EEPROM

Data is read from the EEPROM immediately after a Hardware Reset, and the values obtained are used to update the Configuration before the PCI System first sees the device on the Bus. This allows a vendor to substitute their own ID codes in place of the MosChip codes for example. If no EEPROM is detected after a Hardware Reset, MosChip's default values for the configuration are provided by the chip itself.

PCI Configuration Space Header
Default values for several key fields are shown in the table below.

AD 31-23	AD 22-16	AD 15-8	AD 7-0	Offset (Hex)
Device ID (9845)		Vendor ID (9710)		00
Status		Command		04
Class Code (078000)			Revision ID (01)	08
BIST	Header Type	Latency Timer	Cache Size (08)	0C
Base Address Register (BAR) 0 – “UART-A” (U1)				10
Base Address Register (BAR) 1 – “UART-B” (U2)				14
Base Address Register (BAR) 2 – “nCS3” (E3)				18
Base Address Register (BAR) 3 – “nCS4” (E4)				1C
Base Address Register (BAR) 4 – “nCS5” (E5)				20
Base Address Register (BAR) 5 – “nCS6” (E6)				24
Reserved				28
Subsystem ID (0014)		Subsystem Vendor ID (1000)		2C
Reserved				30
Reserved				34
Reserved				38
Max Latency (00)	Min Grant (00)	Interrupt Pin (01)	Interrupt Line	3C

Internal Address Select Configuration
The MCS9845 uses two Base Address Registers for its UARTs, and four for the ISA Bridge.
These essentially act as internal “Chip Select” logic.
Registers are addressed by using one of the Base Addresses plus an offset.

BAR	I/O Address Offset	Function
0 (U1)	00-07	UART-A
1 (U2)	00-07	UART-B
2 (E3)	00-07	External Chip Select 3
3 (E4)	00-07	External Chip Select 4
4 (E5)	00-07	External Chip Select 5
5 (E6)	00-07	External Chip Select 6

MCS9845CV EEPROM Contents (16-bit mode)

EEPROM Address Location	Hex Data (Word)	Description of Content	EEPROM Address Location	Hex Data (Word)	Description
0x00	9845	Device ID	0x20	0000	
0x01	0000		0x21	0000	
0x02	9710	Vendor ID	0x22	0000	
0x03	0000		0x23	0000	
0x04	0000		0x24	0000	
0x05	0000		0x25	0000	
0x06	0000		0x26	0000	
0x07	0000		0x27	0000	
0x08	0780	Class Code (23-8)	0x28	0000	
0x09	0000		0x29	0000	
0x0A	0001	Revision ID	0x2A	0000	
0x0B	0000		0x2B	0000	
0x0C	0000	Header	0x2C	0014	Subsystem ID
0x0D	0000		0x2D	0000	
0x0E	0000		0x2E	1000	Subsystem Vendor ID
0x0F	0000		0x2F	0000	
0x10	0000		0x30	0000	
0x11	0000		0x31	0000	
0x12	0000		0x32	0000	
0x13	0000		0x33	0000	
0x14	0000		0x34	0000	
0x15	0000		0x35	0000	
0x16	0000		0x36	0000	
0x17	0000		0x37	0000	
0x18	0000		0x38	0000	
0x19	0000		0x39	0000	
0x1A	0000		0x3A	0000	
0x1B	0000		0x3B	0000	
0x1C	0000		0x3C	0000	
0x1D	0000		0x3D	0000	
0x1E	0000		0x3E	0100	Interrupt Pin
0x1F	0000		0x3F	0000	

EEPROM Key Locations

Description	EEPROM Address Location	Word/Byte Data
Device ID	0x00	9845
Vendor ID	0x02	9710
Class Code	0x08	0780
Class Code Interface	0x0A (MS Byte)	00
Revision ID	0x0A (LS Byte)	01
Header Type	0x0C (LS Byte)	00
Subsystem ID	0x2C	0014
Subsystem Vendor ID	0x2E	1000
Interrupt Pin	0x3E	01

The MCS9820 EEPROM controller reads the least significant byte first and then the most significant byte in 16-bit format. Therefore, when writing to the EEPROM, the least significant byte is written first, followed by the most significant byte. For example, the value 9845 would be written as 45 98.

Changing the Device ID, Vendor ID, and Subsystem Vendor ID values requires corresponding changes in the device drivers to ensure proper functioning of the MCS9845CV. These fields can be customized to meet user requirements. The Subsystem Vendor ID value can be changed to arrive at a different product configuration using the EEPROM as shown below.

Product Type: Subsystem Vendor ID

PCI to 2 Serial (2S): 0002
PCI to 4 Serial (4S): 0004
PCI to 6 Serial (6S): 0006
PCI to 4 Serial and 1 Parallel (4S1P): 0014 (default)

Use default values for all other locations in the EEPROM.

UART Register Table

CS	A2	A1	A0	Register	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Un	0	0	0	RHR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Un	0	0	0	THR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Un	0	0	1	IER	0	0	0	0	Modem Status Interrupt	Receive Line Status Interrupt	Transmit Holding Register	Receive Holding Register
Un	0	1	0	FCR	RCVR Trigger (MSB)	RCVR Trigger (LSB)	0	0	0	XMIT FIFO Reset	RCVR FIFO Reset	FIFO Enable
Un	0	1	0	IIR	0/ FIFO Enabled	0/ FIFO Enabled	0	0	Interrupt Priority (Bit-2)	Interrupt Priority (Bit-1)	Interrupt Priority (Bit-0)	Interrupt Status
Un	0	1	1	LCR	Divisor Latch Enable	Set Break	Set Parity	Even Parity	Parity Enable	Stop Bits	Word Length (Bit-1)	Word Length (Bit-0)
Un	1	0	0	MCR	0	0	Hardware Flow Control	Loop Back	Interrupt Enable (nOP2)	(nOP1)	nRTS	nDTR
Un	1	0	1	LSR	0/ FIFO Error	XMIT Empty	XMIT Holding Empty	Break Interrupt	Framing Error	Parity Error	Overrun Error	Receive Data Ready
Un	1	1	0	MSR	nCD	nRI	nDSR	nCTS	Delta nCD	Delta nRI	Delta nDSR	Delta nCTS
Un	1	1	1	SPR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Un	0	0	0	DLL	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Un	0	0	1	DLM	Bit-15	Bit-14	Bit-13	Bit-12	Bit-11	Bit-10	Bit-9	Bit-8

DLL and DLM are accessible only when LCR Bit-7=1.
U1: Internal UART-A chip select
U2: Internal UART-B chip select (if two UARTs are present)

Master Reset Conditions

Register	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
RHR	0	0	0	0	0	0	0	0
THR	X	X	X	X	X	X	X	X
IER	0	0	0	0	0	0	0	0
FCR	0	0	0	0	0	0	0	0
IIR	0	0	0	0	0	0	0	1
LCR	0	0	0	0	0	0	0	0
MCR	0	0	0	0	0	0	0	0
LSR	0	1	1	0	0	0	0	0
MSR	X	X	X	X	0	0	0	0
SPR	0	0	0	0	0	0	0	0

UART Register Descriptions

Transmitter Holding Register (THR)
The transmitter section consists of a Transmitter Holding Register (THR) and a Transmitter Shift Register (TSR). The THR is actually a 16-Byte FIFO. Transmitter control is a function of the Line Control Register (LCR). The THR receives data off the internal data bus, and when the shift register is idle, moves it into the TSR. The TSR serializes the data and outputs it at TX. In the 16C450 mode, if the THR is empty and the Transmitter Holding Register Empty (THRE) interrupt is enabled (IER-1=1), an interrupt is generated. This interrupt is cleared when a character is loaded into the Transmitter Holding Register. In the FIFO (16C550) mode, the interrupts are generated based on the control setup in the FIFO Control Register (FCR).

Receiver Holding Register (RHR)
The receiver section consists of a Receiver Shift Register (RSR) and a Receiver Holding Register (RHR). The RHR is actually a 16-Byte FIFO. Timing for the Receiver Shift Register is supplied by the 16x-receiver clock. Receiver control is a function of the Line Control Register (LCR). The RSR receives serial data from RX. The RSR then concatenates the data and moves it into the RHR FIFO. In the 16C450 mode, when a character is placed in the Receiver Holding Register and the *Received Data Available* interrupt is enabled (IER-0=1), an interrupt is generated. This interrupt is cleared when the data is read out of the Receiver Holding Register. In the FIFO (16C550) mode, the interrupts are generated based on the control setup in the FIFO Control Register (FCR).

Interrupt Enable Register (IER)
The Interrupt Enable Register enables each of the five types of interrupts and INT pin response to an interrupt generation. The Interrupt Enable Register can also be used to disable the interrupt system by setting bits 0-3 to logic 0. The contents of this register are described below:

IER Bit-0:
0 = Disables the Received Data Available interrupt.
1 = Enables the Received Data Available interrupt.

IER Bit-1:
0 = Disables the Transmitter Holding Register Empty interrupt.
1 = Enables the Transmitter Holding Register Empty interrupt.

IER Bit-2:
0 = Disables the Receiver Line Status interrupt.
1 = Enables the Receiver Line Status interrupt.

IER Bit-3:
0 = Disables the Modem Status interrupt.
1 = Enables the Modem Status interrupt.

IER Bits 7-4:
These bits are not used (always set to 0).

Interrupt Identification Register (IIR)
An on-chip interrupt generation and prioritization capability permits a flexible interface with most popular microprocessors.

IIR Bit-0:
0 = An interrupt is pending. Used either in a hardware prioritized or polled interrupt system.
1 = No interrupt is pending.

IIR Bits 3-1:
There are five prioritized levels of interrupts:

Priority 1 - Receiver Line Status (highest priority)
Priority 2 - Receiver Data Ready
Priority 3 - Receiver Character Time-Out
Priority 4 - Transmitter Holding Register Empty
Priority 5 - Modem Status (lowest priority)

When an interrupt is generated, the Interrupt Identification Register indicates that an interrupt is pending and encodes the type of interrupt in its four least significant bits (bits 0, 1, 2, and 3).

Interrupt Priority Decode				
Bit-3	**Bit-2**	**Bit-1**	**Bit-0**	**Interrupt Source**
0	1	1	0	Receive Data Error
0	1	0	0	Receive Data Ready
1	1	0	0	Receive Time-Out
0	0	1	0	Transmitter Holding Register Empty
0	0	0	0	Modem Status Change

Bits 3, 2, & 1 are used to identify the highest priority interrupt pending.

Bit-0 will clear to “1” when no interrupt is pending.

To clear the interrupts, specific registers must be read or written. The actions needed to clear each type of interrupt are listed below:

Receive Data Error:
Reading the LSR will clear this interrupt. Software should save the LSR value after reading the register if it needs to remember the error condition.

Receive Data Ready:
Reading the RHR until the FIFO becomes empty will clear this interrupt.

Receive Timeout:
Reading entire characters from RHR will clear this interrupt.

Transmitter Holding Register Empty:
Writing a character into the THR or reading the IIR (if source of interrupt) will clear this interrupt.

Modem Status Change:
Reading the MSR will clear this interrupt.

IIR Bit 4:
This bit is not used (always 0).

IIR Bit 5:
This bit is not used (always 0).

IIR Bits 7-6:
0 = In the 16C450 mode.
1 = When FCR-0 is equal to 1.

FIFO Control Register (FCR)

The FIFO Control Register (FCR) is a write only register. The FCR enables and clears the FIFOs, as well as setting the receive FIFO trigger level.

FCR Bit-0:

0 = 16C450 mode, disables the transmitter and receiver FIFO.

1 = Enables the transmitter and receiver FIFOs. This bit must be set to 1 when other FCR bits are written to or they are not programmed. Changing this bit clears the FIFOs.

FCR Bit-1:

0 = Normal operation

1 = Clears all Bytes in the receiver FIFO and resets its counter logic to 0. The shift register is not cleared. The one that is written to this bit position is self-clearing.

FCR Bit-2:

0 = Normal operation

1 = Clears all Bytes in the transmitter FIFO and resets its counter logic to 0. The shift register is not cleared. The one that is written to this bit position is self-clearing.

FCR Bit 5-3:

Not used (Always 0).

FCR Bits 7-6:

These bits are used to set the trigger level for receive FIFO interrupts.

Receive Trigger Level (Bytes)		
Bit-7	**Bit-6**	**RX FIFO Trigger Level**
0	0	1
0	1	4
1	0	8
1	1	14

Line Control Register (LCR)

The system programmer controls the format of the asynchronous data communication exchange through the Line Control Register. In addition, the programmer is able to retrieve, inspect, and modify the contents of the Line Control Register; this eliminates the need for separate storage of the line characteristics in system memory.

LCR Bits 1-0:

These two bits specify the number of bits in each transmitted or received serial character.

Bit-1	Bit-0	Word Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

LCR Bit-2:

This bit specifies 1, 1-1/2, or 2 stop bits in each transmitted character. When bit-2 is reset to 0, one stop bit is generated in the data. When bit-2 is set to 1, the number of stop bits generated is dependent on the word length selected with bits 0 and 1. The receiver clocks only the first stop bit regardless of the number of stop bits selected. The number of stop bits generated in relation to word length and bit-2 are shown below:

Bit-2	Word Length	Stop Bit(s)
0	Any	1
1	5 bits	1-1/2
1	6 bits	2
1	7 bits	2
1	8 bits	2

LCR Bit-3:

0 = Parity is disabled. No parity is generated or checked.

1 = Parity bit is generated in transmitted data between the last data word bit and the first stop bit. In received data, parity is checked.

LCR Bit-4:

0 = ODD parity select bit. When parity is enabled by bit-3, a 0 in bit-4 produces Odd Parity (an odd number of 1s in the data and parity bits).

1 = EVEN parity select bit. When parity is enabled by bit-3, a 1 in bit-4 produces even parity (an even number of 1s in the data and parity bits).

LCR Bit-5:

0 = Stick parity is disabled.

1 = Stick parity bit. When bits 3-5 are set to 1 the parity bit is transmitted and checked as a 0. When bits-3 and 5 are 1s and bit-4 is a 0, the parity bit is transmitted and checked as 1.

Parity Selection			
Bit-5	**Bit-4**	**Bit-3**	**Parity type**
X	X	0	No parity
0	0	1	Odd parity
0	1	1	Even parity
1	0	1	Forced parity “1”
1	1	1	Forced parity “0”

LCR Bit-6:

0 = Normal operation. Break condition is disabled and has no effect on the transmitter logic.

1 = Force a break condition. TX is forced to the space (low) state.

LCR Bit-7:

0 = Normal operation.

1 = Divisor Latch Enable. Must be set to 1 to access the divisor latches of the Baud Rate Generator during a read or write. Bit-7 must be reset to 0 during a read or write to any of the other UART registers (Receiver Holding Register, Transmitter Holding Register, Interrupt Enable Register, etc.).

Modem Control Register (MCR)
The Modem Control Register is an 8-bit register that controls an interface with a modem, data set, or peripheral device that is emulating a modem.

MCR Bit-0:
0 = Sets the nDTR output pin to high.
1 = Sets the nDTR output pin to low.

MCR Bit-1:
0 = Sets the nRTS output pin to high.
1 = Sets the nRTS output pin to low.

MCR Bit-2:
0 = Sets the nOP1 to high during loop-back mode.
1 = Sets the nOP1 to low during loop-back mode.

MCR Bit-3:
0 = Disables UART interrupts. Sets the nOP2 to high during loop-back mode.
1 = Enables UART interrupts. This bit is gated with IER Bits 0-3. Sets the nOP2 to low during loop-back mode.

MCR Bit-4:
0 = Normal operation.
1 = Internal Loop-Back mode. Provides a local loop-back feature for diagnostic testing. When LOOP is set to 1, the following occurs:

- The transmitter TX pin is set to high.
- The receiver RX pin is disconnected.
- The output of the transmitter shift register is looped back into the receiver shift register input.
- The four modem inputs (nCTS, nDSR nCD and nRI) pins are disconnected.
- The four modem outputs (nDTR, nRTS, nOP1, and nOP2) pins are internally connected to the four modem inputs. The four modem outputs are forced to the high levels.

In the diagnostic mode, data that is transmitted is immediately received. This allows the processor to verify transmit and receive data paths. The receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational, but the modem control interrupt sources are now the lower four bits of the modem control register instead of the four modem control inputs. All interrupts are still controlled by the interrupt enable register.

MCR Bit-5:
0 = 16C450/550 mode.
Hardware flow control is disabled.
1 = Enable hardware flow control (nRTS/nCTS).

MCR Bit-5	MCR Bit-1	Flow Control
1	1	Auto RTS/CTS
1	0	Auto CTS only
0	X	Disabled

nRTS becomes active (low) when the receiver is empty or the threshold has not been reached. When the receiver FIFO level reaches the trigger level (1, 4, 8, or 14), nRTS is de-asserted (high). nRTS is automatically reasserted once the receiver FIFO is empty by reading the Receive Holding Register (RHR).

The transmitter circuitry checks nCTS before sending the next Data Byte. When nCTS is active (low), the transmitter sends the next Byte. To stop the transmitter from sending the next Byte, nCTS must be released before the middle of the last stop bit that is currently being sent.

MCR bits 7-6:
These bits are not used (Always 0).

Line Status Register (LSR)

The Line Status Register provides information concerning the status of data transfers. The Line Status Register is intended for read operations only. Writing to this register is not recommended. Bits 1-4 are the error conditions that produce a *Receiver Line Status* interrupt.

LSR Bit-0:

0 = No data in Receiver Holding Register or FIFO.

1 = Data Ready indicator for the receiver. This bit is set to 1 whenever a complete incoming character has been received and transferred into the Receiver Holding Register or the FIFO. It is reset to 0 by reading all of the data in the Receiver Holding Register or the FIFO.

LSR Bit-1:

0 = Normal operation. No overrun error.

1 = Before the character in the Receiver Holding Register was read, it was over written by the next character transferred into the register. This bit is reset every time the CPU reads the contents of the Line Status Register. If FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error occurs only after the FIFO is full and the next character has been completely received in the shift register. An overrun error is indicated as soon as it happens. The character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR Bit-2:

0 = Normal operation. No parity error.

1 = The parity of the received character does not match the parity selected in the Line Control Register. This bit is reset every time the CPU reads the contents of the Line Status Register. In FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is reported when its associated character is at the top of the FIFO.

LSR Bit-3:

0 = Normal operation. No framing error.

1 = The received character did not have a valid stop bit. This bit is reset every time the CPU reads the contents of the Line Status Register. In FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is reported when its associated character is at the top of the FIFO. An attempt to re-synchronize is made after a framing error occurs. It is assumed that the framing error is due to the next start bit.

LSR Bit-4:

0 = Normal operation.

1 = The receiver data input was held in the logic low state for longer than a full word transmission time. A full word transmission time is defined as the total time to transmit the start, data, parity, and stop bits. This bit is reset every time the CPU reads the contents of the Line Status Register. In FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is reported when its associated character is at the top of the FIFO. When a break occurs, only one 0 character is loaded into the FIFO.

LSR Bit-5:

0 = At least one character is in the transmitter FIFO or Transmitter Holding Register.

1 = The Transmitter Holding Register is empty. The device is ready to accept a new character. If the *THRE* interrupt is enabled when THRE is set to 1, an interrupt is generated. THRE is set to 1 when the last character in the Transmitter Holding Register is transferred to the Transmitter Shift Register.

LSR Bit-6:

0 = When either the Transmitter Holding Register or the Transmitter Shift Register contains a data character.

1 = The Transmitter Holding Register and the Transmitter Shift Register are both empty.

LSR Bit-7:

0 = In the 16C450 mode, this bit is always reset to 0.

1 = In the FIFO (16C550) mode, at least one parity, framing, or break error exists in the FIFO. It is cleared when the microprocessor reads the LSR and there are no subsequent errors in the FIFO.

Modem Status Register (MSR)

The Modem Status Register is an 8-bit register that provides information about the current state of the control lines from the modem, data set, or peripheral device to the CPU. Additionally, four bits of this register provide change information. When input from the modem changes state, the appropriate bit is set to 1. All four bits are reset to 0 when the CPU reads the Modem Status Register.

MSR Bit-0:

0 = No change to nCTS input.

1 = The nCTS input has changed state since the last time it was read by the CPU. When the interrupt is enabled, a *Modem Status* interrupt is generated.

MSR Bit-1:

0 = No change to nDSR input.

1 = The nDSR input has changed state since the last time it was read by the CPU. When the interrupt is enabled, a *Modem Status* interrupt is generated.

MSR Bit-2:

0 = No change to nRI input.

1 = The nRI input has changed from a low to a high level. When nRI is set to 1 and the interrupt is enabled, a *Modem Status* interrupt is generated.

MSR Bit-3:

0 = No change to nCD input.

1 = The nCD input has changed state since the last time it was read by the CPU. When the interrupt is enabled, a *Modem Status* interrupt is generated.

MSR Bit-4:

Complement of the Clear To Send (nCTS) input. When in the diagnostic test mode, this bit is equal to nRTS.

MSR Bit-5:

Complement of the Data Set Ready (nDSR) input. When in the diagnostic test mode, this bit is equal to nDTR.

MSR Bit-6:

Complement of the Ring Indicator (nRI) input. When in the diagnostic test mode, this bit is equal to nOP1.

MSR Bit-7:

Complement of the Data Carrier Detect (nCD) input. When in the diagnostic test mode, this bit is equal to nOP2.

Scratch Pad Register (SPR)

The scratch pad register is an 8-bit register that can be used by the programmer to store any data without affecting any other registers or device operation. The contents of this register are volatile, the data will be lost when the device is reset, or when power is removed.

Programmable Baud-Rate Generator

A programmable Baud Rate Generator is provided that typically takes a clock input of 1.8432 MHz and divides it by a divisor in the range between 1 and (2^{16}-1). The output frequency of the Baud Rate Generator is 16 times the desired Baud Rate. Two 8-bit registers, called Divisor Latches, store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during the device's initialization in order to ensure correct operation of the Baud Rate Generator. When either of the Divisor Latches is altered, an internal 16-bit Baud Counter is also updated to prevent long counts on the initial load.

Baud Rate Generator programming table for the default 1.8432 MHz clock (12XCLK).

Baud Out	DLM (hex)	DLL (hex)
115.2K	00	01
57.6K	00	02
38.4K	00	03
19.2K	00	06
9600	00	0C
4800	00	18
2400	00	30
1200	00	60
600	00	C0
300	01	80
150	03	00
50	09	00

MosChip devices with Serial Ports provide the 12XCLK output signal that can be used as the input clock for the UART. 12XCLK is the standard 1.8432 MHz clock. Using this signal as the clock input will generate the expected Baud Rates as shown in the table above.

FIFO Interrupt Mode Operation

When the receiver FIFO and receiver interrupts are enabled (FCR-0=1, IER-0=1, IER-2=1), a receiver interrupt occurs as follows:

The *Received Data Available* interrupt is issued when the FIFO has reached its programmed trigger level. It is cleared when the FIFO drops below its programmed trigger level. The IIR Receive Data Available indication also occurs when the FIFO trigger level is reached, and like the interrupt, it is cleared when the FIFO drops below the trigger level.

The receiver *Line Status Interrupt* has higher priority than the *Received Data Available* interrupt. The data ready bit (LSR-0) is set when a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

When the receiver FIFO and receiver interrupts are enabled, the *FIFO Time-Out* interrupt occurs when the following conditions exist:

- At least one character is in the FIFO.
- The most recent serial character was received more than four continuous character times ago (if two stop bits are programmed, the second one is included in this time delay).
- The most recent microprocessor read of the FIFO occurred more than five continuous character times ago.

When a *Time-Out* interrupt has occurred, it is cleared and the timer is reset when the microprocessor reads one character from the receiver FIFO. Even if a *Time-Out* interrupt has not occurred, the time-out timer is reset each time a new character is received or when the microprocessor reads the receiver FIFO.

Character *Time-Out* and receiver *FIFO Trigger-Level* interrupts have the same priority as the current *Receiver Data Available* interrupt.

When the transmitter FIFO and *THRE* interrupt are enabled (FCR-0=1, IER-1=1), transmit interrupts occur as follows:

The occurrence of the *Transmitter Holding Register Empty* interrupt is delayed one character time minus the last stop bit time when there have not been at least two Bytes in the transmitter FIFO at the same time since the last time the transmitter FIFO was empty. It is cleared as soon as the Transmitter Holding Register is written to (1 to 16 characters may be written to the transmit FIFO while servicing this interrupt) or the IIR is read. The first transmitter interrupt after changing the FCR is immediate if it is enabled.

The Transmitter Empty indicator is delayed one character time when there has not been at least two Bytes in the transmitter FIFO at the same time since the last time that TEMT=1. TEMT is set after the stop bit has been completely shifted out.

The Transmitter FIFO Empty indicator is not delayed, it is reported as soon as the condition occurs.

ISA Bridge
A PCI to ISA Bridge allows the product designer to increase the number of I/O Ports through the use of external components. Additional UARTs and Parallel Ports are easy to attach and configure.

Chip Selects
Four external Chip Select signals (nCS3-nCS6) are provided. Each Chip Select has its own Base Address Register (BAR) in the PCI Configuration Space. The Base Address Registers each point to a block of eight I/O registers. When any of the eight registers in the block assigned to one of the Base Address Registers are accessed, the Chip Select signal for that group will be activated. The following table shows the relationship between the Base Address Registers and the external Chip Select signals.

BAR	Offset	Chip Select
2 (E3)	00-07	nCS3
3 (E4)	00-07	nCS4
4 (E5)	00-07	nCS5
5 (E6)	00-07	nCS6

If BAR-3 contains the address 0xD800, then accessing any address between 0xD800 and 0xD807 will activate the nCS4 Chip Select line.

Common I/O Control Signals
In addition to the Chip Select signals, the other required ISA signals are also present. Separate nIOR (I/O Read) and nIOW (I/O Write) signals are provided, simplifying the interface to external components. An 8-bit bi-directional Data Bus is provided. Both Active-High and Active-Low Reset signals are provided, simplifying the connection to external devices. Three Address Lines (A0-2) allow each Chip Select to control eight registers.

Interrupts
ISA style devices typically use Active-High Interrupt Request signals. Four Active-High Interrupt Request inputs (IRQ2-5) are provided. A single Active-Low Interrupt Request input (nIRQ6) is also available providing even more flexibility. There is no mechanism provided to directly associate any of the Interrupt Request signals with any of the external Chip Select signals. The Interrupt Requests are simply passed on to the PCI system. All I/O Ports or devices (including those inside the chip) share a single PCI Interrupt Request line. The software Driver must poll all of the devices to determine which one is the source of an interrupt.

Other Devices
While the primary purpose of the ISA Bridge is to allow products to provide additional UARTs or Parallel Ports, it is not necessarily restricted to such devices. The signals provided should allow the inclusion of most ISA style components into a custom design. If custom (or other standard ISA) components are used, a custom software Driver will probably be required as well. The MosChip Drivers only support additional UARTs and Parallel Ports. Simple custom devices that always have the CPU initiate reads or writes to the device may work without any additional Drivers, but any design that adds external components that generate Interrupt Requests will definitely require custom Drivers.

Electrical Characteristics

Absolute Maximum Ratings

Supply Voltage	6 Volts
Voltage at any pin	GND - 0.3 V to V_{CC} + 0.3 V
Operating Temperature	0 °C to +70 °C
Storage Temperature	-40 °C to +150 °C
ESD HBM (MIL-STD 883E Method 3015-7 Class 2)	2000V
ESD MM (JEDEC EIA/JESD22 A115-A)	200V
CDM (JEDEC/JESD22 C101-A)	500V
Latch-up (JESD No. 78, March 1997)	200 mA, 1.5 x VCC
Junction Temperature (Tj)	115 °C

Recommended Operating Conditions for 5V Operation

Symbol	Parameter	Min	Typ	Max	Unit	Condition
Vcc	Supply Voltage	4.5	5.0	5.5	V	
Vin	Input Voltage	0		Vcc	V	
Icc	Operating Current		70		mA	

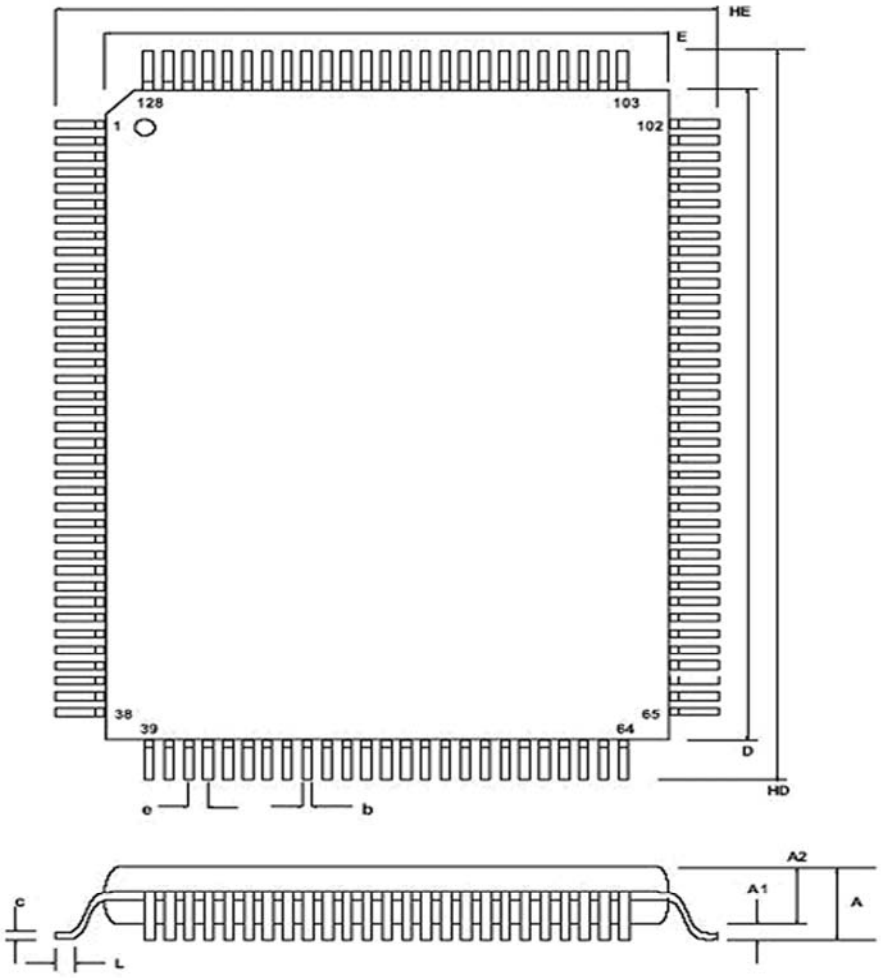
General DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Condition
	Package Dissipation			500	mW	
Ii_L	Input Leakage Current	-1		1	µA	No Pull-Up or Pull-Down
Io_Z	Tri-State Leakage Current	-10		10	µA	
Cin	Input Capacitance		3		pF	
Cout	Output Capacitance		3		pF	
Cbid	Bi-Directional Buffer Capacitance		3		pF	

DC Electrical Characteristics (5V Operation)
Ambient Temp = 0 to +70 °C, V_{CC} = 4.75 to 5.25 V, Tj = 0 to +115 °C unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Condition
Vi_L	Input Voltage (Low)			0.3 * Vcc	V	CMOS
Vi_H	Input Voltage (High)	0.7 * Vcc			V	CMOS
Vi_L	Input Voltage (Low)			0.8	V	TTL
Vi_H	Input Voltage (High)	2.0			V	TTL
Vt-	Schmitt Trigger Negative-Going Threshold Voltage		1.84		V	CMOS
Vt+	Schmitt Trigger Positive-Going Threshold Voltage		3.22		V	CMOS
Vt-	Schmitt Trigger Negative-Going Threshold Voltage		1.10		V	TTL
Vt+	Schmitt Trigger Positive-Going Threshold Voltage		1.87		V	TTL
Vo_L	Output Voltage (Low)			0.4	V	Io_L = 2 to 24 mA
Vo_H	Output Voltage (High)	3.5			V	Io_H = 2 to 24 mA
Ri	Input Pull-Up/Pull-Down Resistance		50		KΩ	Vi_L = 0V or Vi_H = Vcc

Mechanical Specifications – QFP 128



128-Pin QFP
Package Dimensions

Symbol	Milimeters		
	Min	Typ	Max
A	-	-	3.40
A1	0.10	-	-
A2	2.50		2.97
b	0.17		0.27
c	0.09		0.23
e		0.50	
L	0.70		1.03
HD	23.00		23.40
D	19.90		20.10
HE	17.00		17.40
E	13.90		14.10

IMPORTANT NOTICE

MosChip Semiconductor Technology, LTD products are not authorized for use as critical components in life support devices or systems. Life support devices are applications that may involve potential risks of death, personal injury or severe property or environmental damages. These critical components are semiconductor products whose failure to perform can be reasonably expected to cause the failure of the life support systems or device, or to adversely impact its effectiveness or safety. The use of MosChip Semiconductor Technology LTD's products in such devices or systems is done so fully at the customer risk and liability.

As in all designs and applications it is recommended that the customer apply sufficient safeguards and guard bands in both the design and operating parameters. MosChip Semiconductor Technology LTD assumes no liability for customer's applications assistance or for any customer's product design(s) that use MosChip Semiconductor Technology, LTD's products.

MosChip Semiconductor Technology, LTD warrants the performance of its products to the current specifications in effect at the time of sale per MosChip Semiconductor Technology, LTD standard limited warranty. MosChip Semiconductor Technology, LTD imposes testing and quality control processes that it deems necessary to support this warranty. The customer should be aware that not all parameters are 100% tested for each device. Sufficient testing is done to ensure product reliability in accordance with MosChip Semiconductor Technology LTD's warranty.

MosChip Semiconductor Technology, LTD believes the information in this document to be accurate and reliable but assumes no responsibility for any errors or omissions that may have occurred in its generation or printing. The information contained herein is subject to change without notice and no responsibility is assumed by MosChip Semiconductor Technology, LTD to update or keep current the information contained in this document, nor for its use or for infringement of patent or other rights of third parties. MosChip Semiconductor Technology, LTD does not warrant or represent that any license, either expressed or implied, is granted to the user.

Revision History

Revision	Changes	Date
1.0	Initial Release	Jul-2000
2.0	Revised Data Sheet Format	22-May-2006
2.1	Switched to new Page-1 Layout	1-Jun-2006
2.2	Corrected BAUD Rate Divisor Table	21-Jun-2006
2.3	Removed text about 5V tolerant serial and PCI interfaces	25-July-2007
2.4	Updated Features list. Added EEPROM contents tables Updated Electrical Characteristics section Package dimensions in inches removed.	01-August-2007
2.5	Mechanicals dimensions updated	20-May-2009