Data Sheet

NVIDIA C51G
Integrated Graphics Processor

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PLATFORM PROCESSORS

C51G Document Change History

Version	Date	Responsible	Reason for Change
1.0	04/04/05	JK, DV, AS, JT, MH, BH	Initial release
1.1	04/08/05	KK, DV	Minor edits
1.2	06/13/05	KK	Pin AD23 corrected from HT_MCP_TXD11_P to HT_MCP_TXD1_P in Table 26, Ball Listing by Package Ball
1.3	06/27/05	AS, AK, DV	Removed references to HDTV encoder
1.4	06/29/05	AT, DV	Minor edits
1.5	07/05/05	AT, DV	Table 8 : Changed description of +2.5V_IFPA and +2.5V_IFPB: From "It should be pulled down to GND through a 4.7 kΩ resistor" to "It should be connected to +2.5V_CORE".
1.6	07/27/05		Edits
1.7	10/03/05	AT, DV	Added Programmable PureVideo processor information to document.
1.8	10/18/05	AT, DV	Updated System and Block Diagram (Figure 1) from CRT DAC to TV/CRT DAC and External CRT to External SDTV or CRT

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Preface

This document is targeted to motherboard designers and is intended to provide them with the information necessary to design an NVIDIA® C51G motherboard. It contains a features list, signal description, signal states, power sequencing and RESET information, package information, AC/DC specifications, and the ball map. The information contained in this data sheet is preliminary and subject to change.

Chapter 1. Introduction

The NVIDIA® C51G is the desktop industry's first solution for providing enthusiast-class graphics features, a dedicated video processor , and power management features for every desktop consumer. Paired with an Athlon 64/Athlon 64 FX or Sempron 939-/754-pin CPU, and a media and communications processor (MCP), all the key features needed for computing, displaying, storing, and communicating information come together in the C51G.

Product Overview

The NVIDIA C51G includes the following features:

- Integrated Programmable Shader model 3.0 DirectX 9 graphics processor
  - Shader model 3.0 vertex processor
  - Shader model 3.0 pixel processor
  - NVIDIA® CineFX™ 3.0 architecture
  - NVIDIA® Intellisample™ AA technology
- Programmable NVIDIA® PureVideo™ processor
- Integrated 300 MHz DAC for external desktop displays
- Primary HyperTransport link up to 1.0 GHz to the CPU
- Secondary HyperTransport link, up to 1.0 GHz
- PCI Express 16 lane link interface for external graphics processors
- Dual PCI Express single lane link interface, with dedicated controller for other peripherals.
- Active power management
- Programmable clock synthesizer
- 25 mm × 25 mm, 1.0 mm ball pitch PBGA

Based on the award-winning NVIDIA nForce4 processor and GeForce 6 processor, the C51G is the ideal solution for mainstream desktop computers.

System and Block Diagram

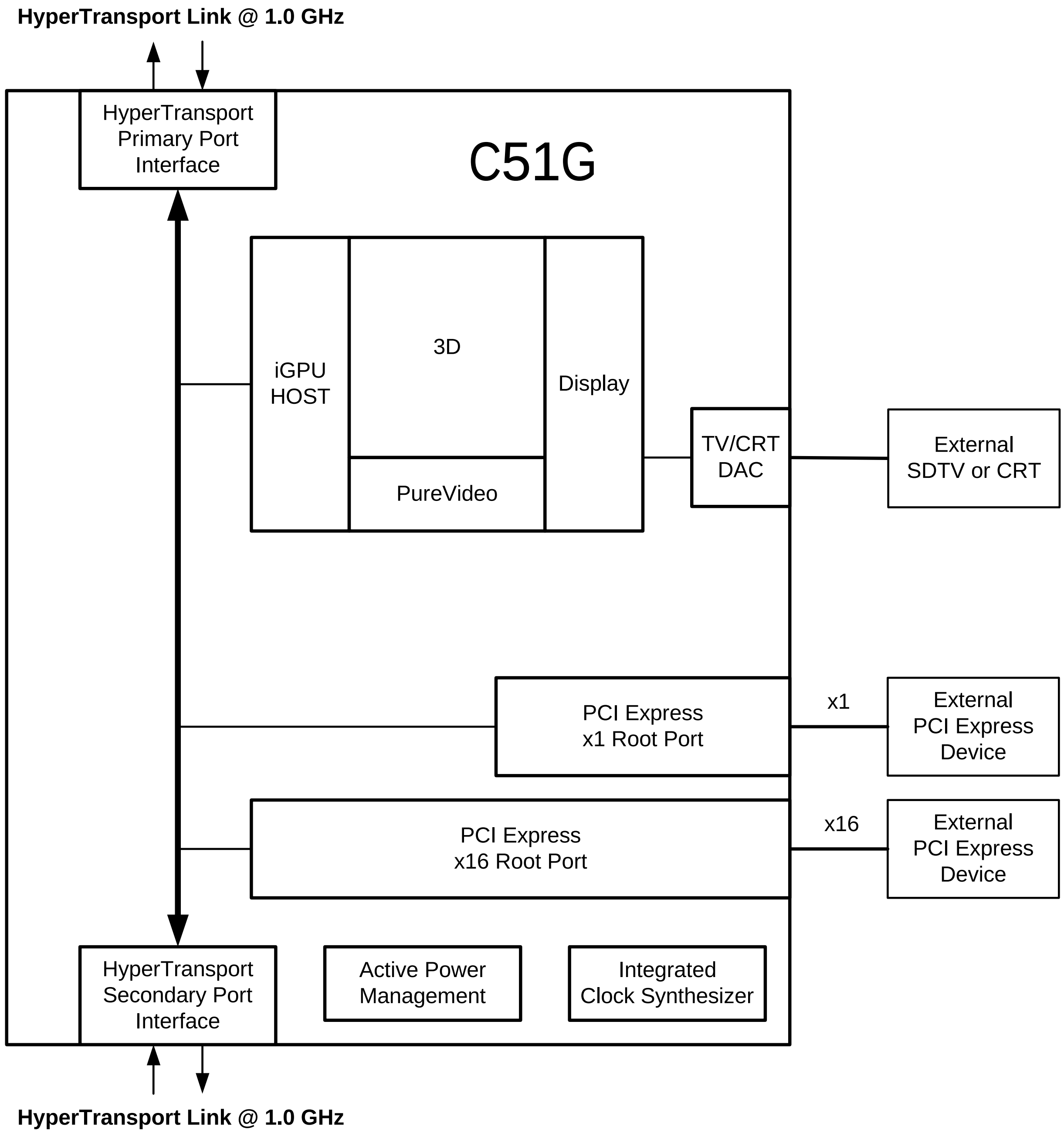


Figure 1. C51G System and Block Diagram

Features and Functions

Primary HyperTransport Link (to CPU)

- High-speed, differential, low voltage interface
- Communicates with the AMD Athlon 64/Athlon 64 FX or Sempron 939-/754-pin CPUs
- ×8, ×16 up and ×8, ×16 downstream data paths
- Up to 1.0 GHz, for a total bandwidth of up to 8.0 GT/s
- Supports coherent and non-coherent data types
- Supports isochronous and non-isochronous data channels
- Supports real-time link reconnect/disconnect
- Clock spread spectrum capability

PCI Express Interface

- Two separate PCI Express controllers with 17 total lanes, configured as one ×16 and one ×1 PCI Express lanes
- WAKE# function is supported for power management
- 2.5 GHz support, for a total bandwidth of 2.5 Gb/s per direction per lane
- Clock spread spectrum capability

DirectX 9.0c Shader Model 3.0 Graphics Processing Unit

- CineFX 3.0 Shading Architecture
  - Vertex Shaders
    - Supports Microsoft DirectX 9.0 Vertex Shader 3.0
    - Displacement mapping
    - Geometry instancing
    - Infinite length vertex programs
  - Pixel Shaders
    - Supports DirectX 9.0 Pixel Shader 3.0
    - Full pixel branching support
    - Supports Multiple Render Targets (MRTs)
    - Infinite length pixel programs
  - GeForce6-Class Texture Engine
    - Up to 16 textures per rendering pass
    - Supports 16-bit floating point format and 32-bit floating point format
    - Supports non-power of two textures
    - Supports sRGB texture format for gamma textures
    - DirectX and S3TC texture compression
    - Full 128-bit studio-quality floating point precision through the entire rendering pipeline with native hardware support for 32 bpp, 64 bpp, and 128 bpp rendering modes
- Intellisample 3.0 Technology2
    - Advanced 16× anisotropic filtering

- Blistering-fast antialiasing and compression performance
- New rotated-grid antialiasing removes jagged edges for incredible edge quality
- Supports advanced lossless compression algorithms for color, texture, and z-data, at even higher resolutions and frame rates
- Fast z-clear

- NVIDIA® UltraShadow™ technology; designed to enhance the performance of shadow-intensive games, like id Software Doom 3
- Advanced thermal management and thermal monitoring

Programmable PureVideo Processor

- Sixteen-way VLIW SIMD vector processor
- Separate scaling controller and coefficient generator
- Up to 96 operations per clock
- MPEG video decode
- WMV9 decode acceleration
- Video scaling and filtering
- Hardware accelerated MPEG-2 decode exposed through DirectX Video Acceleration (DXVA)
- Microsoft Video Mixing Renderer (VMR) supports multiple video windows with full video quality and features in each window

Display Controller

- Full NVIDIA® nView™ multi-display technology capability, with independent display controllers for the CRT
- Each controller can drive same or different display contents to different resolutions and refresh rates

Video Mixing Renderer Scaling Pipeline

- Four-tap horizontal by five-tap vertical scaling
- Arbitrary number of video streams can be scaled simultaneously
- Scaled output can be directed to overlay, display, or FB for compositing

Video DAC

- 300 MHz RAMDAC for display resolutions up to and including 1920 × 1440 at 75 Hz

Secondary HyperTransport Link

- High-speed, differential, low voltage interface
- ×4, ×8, ×16 upstream and ×4, ×8, ×16 downstream data paths
- Up to 1.0 GHz operation

- Supports coherent and non-coherent data types
- Supports isochronous and non-isochronous data channels
- Supports real-time link reconnect/disconnect
- Clock spread spectrum capability

Integrated Clock Synthesizer

- Generates all necessary internal and external clock frequencies
  - Based on a single 25 MHz reference clock input from the MCP51
  - Generates clocks for HyperTransport link, PCI Express, Athlon 64/Athlon 64 FX, or Sempron 939-/754-pin CPUs
- Spread spectrum capable on the following clocks: CPU + upstream HyperTransport link, PCI Express, and downstream HyperTransport link clocks
- Simplifies system design and motherboard layout

System and Power Management

Power Management

- Supports instantly available PC (IAPC), ACPI 2.0, and PCI PM 1.1
- PME message support on PCI Express links
- Active clock generator management
- Active clock tree gating and PLL power-down
- Integrated thermal sensor
- Thermal event detection (alarm)
- Power On Suspend (POS) or ACPI S1 support
- Suspend to RAM (STR) or ACPI S3 support
- Suspend to Disk (STD) or ACPI S4/S5 support
- Supports C0, C1, C2, and C3 states
- Supports HyperTransport link disconnect and STOP/REQ protocol
- Supports FID/VID cycles for CPU P-state transition and AMD Cool'n'Quiet

Chapter 2.
Signal Descriptions

This chapter contains the signal descriptions for the NVIDIA C51G. See Appendix A for signal listings by ball location and signal name and Appendix B for the ballout.

This chapter contains the following information:

- Conventions
- Primary HyperTransport Interface to the CPU
- Secondary HyperTransport Interface
- PCI Express Interface
- Power Supply
- Clocks
- TEST/JTAG Interface

Conventions

Following are the conventions used in describing the signals for the NVIDIA C51G:

- Signal Names
  Signal names use a mnemonic to represent the function of the signal. Active low single-ended signals are identified by a pound sign (#) after the signal name. Active high signals do not have the pound sign (#) after the signal names. Differential signals have _P (positive) or _N (complementary) suffixes to indicate the polarity within the pair.
- I/O Type
  The signal I/O type is represented as a code to indicate the operational characteristics of the signal. lists the I/O codes used in the signal description tables.

Table 1. Signal Type Codes

Item	Description
A	Analog
DIFF I/O	Differential input/output
DIFF IN	Differential input
DIFF OUT	Differential output
I	Input
I/O	Bidirectional input/output
O	Output
OC	Open collector output
OD	Open drain output
P	Power

Note: Signals can be part of more than one interface.

Primary HyperTransport Interface to CPU

Table 2. Primary HyperTransport Interface Signals to the CPU

Signal	I/O	Definition
HT_CPU_REQ#	I	**HyperTransport Link Request** This asynchronous signal indicates that an external master wishes to send a transaction and the HyperTransport link should be reconnected. This signal should be an input tied to a motherboard pull-up. Please refer to the *NVIDIA C51 and MCP51 Design Guide.*
HT_CPU_RX_CLK[1:0]_P **HT_CPU_RX_CLK[1:0]_N**	DIFF IN	**HyperTransport Link Differential Receive Clocks** These signals are the differential pairs used as the timing reference for **HT_CPU_RXD[15:0]** and **HT_CPU_RXCTL**. **HT_CPU_RX_CLK1_P/ HT_CPU_RX_CLK1_N** is used for **HT_CPU_RXD[15:8]** and **HT_CPU_RX_CLK0_P/HT_CPU_RX_CLK0_N** is used for **HT_CPU_RXD[7:0]** and **HT_CPU_RXCTL**. When interfacing to a link-width smaller than the full 16 bits, please refer to the *NVIDIA C51 and MCP51 Design Guide* for more details.
HT_CPU_RXCTL_P **HT_CPU_RXCTL_N**	DIFF IN	**HyperTransport Link Differential Receive Control** These signals receive link control signals.
HT_CPU_RXD[15:0]_P **HT_CPU_RXD[15:0]_N**	DIFF IN	**HyperTransport Link Differential Receive Data** These signals are the differential pairs used to receive the high-speed 16 bits of information from the upstream CPU. C51G supports HyperTransport link widths of 8 and 16 bits. When interfacing to a link width smaller than the full 16-bits, please refer to the *NVIDIA C51 and MCP51 Design Guide* for more details.
HT_CPU_STOP#	OD	**HyperTransport Link Disconnect** This signal enables and disables the HyperTransport link during system state transitions. Please refer to the *NVIDIA C51 and MCP51 Design Guide.*
HT_CPU_TX_CLK[1:0]_P **HT_CPU_TX_CLK[1:0]_N**	DIFF OUT	**HyperTransport Link Differential Transmit Clocks** These signals are the differential pairs used as the timing reference for **HT_CPU_TXD[15:0]** and **HT_CPU_TXCTL. HT_CPU_TXCLK1_P/ HT_CPU_TXCLK1_N** is used for **HT_CPU_TXD[15:8]** and **HT_CPU_TXCLK0_P/HT_ CPU_TXCLK0_N** is used for **HT_CPU_TXD[7:0]** and **HT_CPU_TXCTL**. These clock pairs are spread spectrum capable for EMI reduction. When interfacing to a link width smaller than the full 16 bits, please refer to the *NVIDIA C51 and MCP51 Design Guide* for more details.
HT_CPU_TXCTL_P **HT_CPU_TXCTL_N**	DIFF OUT	**HyperTransport Link Differential Transmit Control** These signals transmit the link control signals.
HT_CPU_TXD[15:0]_P **HT_CPU_TXD[15:0]_N**	DIFF OUT	**HyperTransport Link Differential Transmit Data** These signals are the differential pairs used to transmit the high-speed 16 bits of information to the upstream CPU. The C51G supports HyperTransport link widths of 8 bits and 16 bits. When interfacing to a link-width smaller than the full 16-bits, please refer to the *NVIDIA C51 and MCP51 Design Guide* for more details.
HT_CPU_PWRGD	OD	**CPU Power OK** This signal is the Power Good/Cold Reset control for the upstream HyperTransport device. Typically, this connects to an Athlon 64/Athlon 64 FX, or Sempron 939-/754-pin CPU. Please refer to the *NVIDIA C51 and MCP51 Design Guide*.
HT_CPU_RST#	OD	**CPU Reset** This signal is the warm reset signal control for the upstream HyperTransport device. Typically, this connects to an Athlon 64/Athlon 64 FX, or Sempron 939-/754-pin CPU. Please refer to the *NVIDIA C51 and MCP51 Design Guide*.

Table 2. Primary HyperTransport Interface Signals to the CPU (continued)

Signal	I/O	Definition
HT_CPU_CAL_1P2V	A	**HyperTransport Calibration** Used for HyperTransport link interface pads calibration. Please refer to the *NVIDIA C51 and MCP51 Design Guide*.
HT_CPU_CAL_GND	A	**HyperTransport Calibration** Used for HyperTransport link interface pads calibration. Please refer to the *NVIDIA C51 and MCP51 Design Guide.*

Secondary HyperTransport Interface

Table 3. Secondary HyperTransport Interface Signals

Signal	I/O	Definition
HT_MCP_REQ#	OD	**HyperTransport Link Request** This asynchronous signal indicates that a maste,r internal to the C51G, wishes to send a transaction and the HyperTransport link should be reconnected. C51G asserts this signal when its primary or secondary links have a transaction pending, irrespective of the current link state. Please refer to the *NVIDIA C51 and MCP51 Design Guide*.
HT_MCP_RX_CLK[1:0]_P **HT_MCP_RX_CLK[1:0]_N**	DIFF IN	**HyperTransport Link Differential Receive Clocks** These signals are the differential pairs used as the timing reference for **HT_MCP_RXD[15:0]** and **HT_MCP_RXCTL. HT_MCP_RX_CLK1_P/ HT_MCP_RX_CLK1_N** is used for **HT_MCP_RXD[15:8]** and **HT_MCP_RX_CLK0_P/HT_MCP_RX_CLK0_N** is used for **HT_MCP_RXD[7:0]** and **HT_MCP_RXCTL**. When interfacing to a link width smaller than the full 16 bits, please refer to the *NVIDIA C51 and MCP51 Design Guide*.
HT_MCP_RXCTL_P **HT_MCP_RXCTL_N**	DIFF IN	**HyperTransport Link Differential Receive Control** These signals receive link control signals.
HT_MCP_RXD[15:0]_P **HT_MCP_RXD[15:0]_N**	DIFF IN	**HyperTransport Link Differential Receive Data** These signals are the differential pairs used to receive the high-speed 16 bits of information from the downstream MCP51. C51G supports HyperTransport link widths of 4 bits, 8 bits, and 16 bits. When interfacing to a link width smaller than the full 16-bits, please refer to the *NVIDIA C51 and MCP51 Design Guide.*
HT_MCP_STOP#	I	**HyperTransport Link Disconnect** This signal enables and disables the HyperTransport link during system state transitions. Please refer to the *NVIDIA C51 and MCP51 Design Guide*.
HT_MCP_TX_CLK[1:0]_P **HT_MCP_TX_CLK[1:0]_N**	DIFF OUT	**HyperTransport Link Differential Transmit Clocks** These signals are the differential pairs used as the timing reference for **HT_MCP_TXD[15:0]** and **HT_MCP_TXCTL**. **HT_MCP_TX_CLK1_P/HT_MCP_TX_CLK1_N** is used for **HT_MCP_TXD[15:8]** and **HT_MCP_TX_CLK0_P/HT_MCP_TX_CLK0_N** is used for **HT_MCP_TXD[7:0]** and **HT_MCP_TXCTL**. These clock pairs are capable of tracking a spread spectrum input reference for EMI reduction. When interfacing to a link width smaller than the full 16 bits, please refer to the *NVIDIA C51 and MCP51 Design Guide.*
HT_MCP_TXCTL_P **HT_MCP_TXCTL_N**	DIFF OUT	**HyperTransport Link Differential Transmit Control** These signals transmit the link control signals.
HT_MCP_TXD[15:0]_P **HT_MCP_TXD[15:0]_N**	DIFF OUT	**HyperTransport Link Differential Transmit Data** These signals are the differential pairs used to transmit the high-speed 16 bits of information to the downstream HyperTransport device. The C51G supports HyperTransport link widths of 4 bits, 8 bits, and 16 bits. When interfacing to a link width smaller than the full 16 bits, please refer to the *NVIDIA C51 and MCP51 Design Guide*.
HT_MCP_PWRGD	I	**MCP Power Good** This signal is the Power Good/Cold Reset control for the upstream HyperTransport device. Typically this connects to the C51GC51G. Please refer to the *NVIDIA C51 and MCP51 Design Guide*.
HT_MCP_RESET#	I	**MCP Reset** This signal is the warm reset signal control for the upstream HyperTransport device. Typically this connects to the MCP51. Please refer to the *NVIDIA C51 and MCP51 Design Guide*.

Table 3. Secondary HyperTransport Interface Signals (continued)

Signal	I/O	Definition
HT_MCP_CAL_1P2V	A	**HyperTransport Calibration** This signal is used for HyperTransport Link interface pads calibration. Please refer to the *NVIDIA C51 and MCP51 Design Guide.*
HT_MCP_CAL_GND	A	**HyperTransport Calibration** This signal is used for HyperTransport Link interface pads calibration. Please refer to the *NVIDIA C51 and MCP51 Design Guide.*

PCI Express Interface

Table 4. PCI Express x16 Interface Signals

Signal	I/O	Definition
PE0_PRSNT#	I	**PCI Express x 16 Presence Detect** This signal is the presence/hot plug presence detect of a device on the ×16 PCI Express link.
PE0_REFCLK_P **PE0_REFCLK_N**	DIFF OUT	**PCI Express x16 Reference Clock** These signals are the 100 MHz differential reference clock pair for the ×16 PCI Express link.
PE0_RX[15:0]_P **PE0_RX[15:0]_N**	DIFF IN	**PCI Express x16 Receive Data** These signals are the ×16 differential receive data pairs of the PCI Express link.
PE0_TX[15:0]_P **PE0_TX[15:0]_N**	DIFF OUT	**PCI Express x16 Transmit Data** These signals are the ×16 differential transmit data pairs of the PCI Express link.

Table 5. PCI Express1 x1 Interface Signals

Signal	I/O	Definition
PE1_CLKREQ#	I	**PCI Express x1 Reference Clock Request** This signal is used by a PCI Express device to indicate it needs the **PE1_REFCLK_P** and **PE1_REFCLK_N** to actively drive the 100 MHz reference clock.
PE1_PRSNT#	I	**PCI Express x1 Presence Detect** This signal is the hot plug presence detect of a device on a ×1 PCI Express link.
PE1_REFCLK_P **PE1_REFCLK_N**	DIFF OUT	**PCI Express x1 Reference Clock** These signals are the 100 MHz differential reference clock pair for the first ×1 PCI Express link.
PE1_RX_P **PE1_RX_N**	DIFF IN	**PCI Express x1 Receive Data** These signals are the ×1 differential receive data pair of the first ×1 PCI Express link.
PE1_TX_P **PE1_TX_N**	DIFF OUT	**PCI Express x1 Transmit Data** These signals are the ×1 differential transmit data pair of the first ×1 PCI Express link.

Table 6. PCI Express Interface Signals

Signal	I/O	Definition
PE_RESET#	I	**PCI Express Reset** This signal is used for Reset PCI Express links.
PE_CTERM_GND	I	**PCI Express Termination** Please refer to the *NVIDIA C51 and MCP51 Design Guide*.
PE_REFCLKIN_N **PE_REFCLKIN_P**	DIFF IN	P**CI Express Reference Clock Input** These signals are the 100 MHz differential reference clock pair input for the PCI Express link.
PE_TSTCLK_N **PE_TXTCLK_P**	DIFF OUT	**PCI Express Test Clock Output** These signals are the differential test clock pair of the PCI Express link.

Video DAC/TV Out Signals

Table 7. Video DAC/TV Out Signals

Signal	I/O	Description
DAC_RED **DAC_GREEN** **DAC_BLUE** **Chrominance (DAC_RED)** **Luminance (DAC_GREEN)** **Composite (DAC_BLUE)** **Pr (DAC_RED)** **Y (DAC_GREEN)** **Pb (DAC_BLUE)**	O	**Red, Green, and Blue Outputs** These signals are the RGB display monitor outputs. Software configures these signals to drive either a doubly terminated or singly terminated 75-ohm load. **TV Chrominance, Luminance, and Composite Outputs** These signals are also the S-video analog chrominance and luminance outputs, as well as the standard composite output. **HDTV Component Outputs** These signals are also the HDTV component outputs. The above TV out signal mapping is the default but is fully programmable. The type of output is determined by an output load detect algorithm. Please refer to the *NVIDIA C51 and MCP51 Design Guide* for the specific application.
DAC_IDUMP	P	**DAC Ground Reference** Local GND reference for the internal triple DACs.
DAC_HSYNC	I/O	**Horizontal Sync** Horizontal sync supplied to the display monitor. Output level is 3.3V.
DAC_RSET	A	**DAC Reference Current Set** A precision resistor placed between this pin and **GND** sets the full-scale video DAC current. Refer to the *NVIDIA C51 and MCP51 Design Guide* for the suggested value and tolerance of this resistor.
DAC_VREF	A	**DAC Reference Voltage** A capacitor should be placed between this pin and **GND**. Refer to the *NVIDIA C51 and MCP51 Design Guide* for the suggested value and tolerance of this capacitor.
DAC_VSYNC	I/O	**Vertical Sync** Vertical sync supplied to the display monitor. Output level is 3.3V.
XTAL_IN **XTAL_OUT**	I/O	**TV Encoder Reference Clock Input** A 27.0 MHz series resonant crystal is connected between these two points to provide the reference clock for the TV Encoder. Alternately, an external LVTTL clock oscillator output may be driven in on signal **XTAL_IN**, leaving **XTAL_OUT** unconnected. If the internal TV Encoder is not used then **XTAL_IN** should be connected to **GND** leaving **XTAL_OUT** unconnected. Refer to the *NVIDIA C51 and MCP51 Design Guide* for crystal frequency and tolerance.

Power Supply

Table 8. Power Supply Interface

Signal	I/O	Description
+1.2V_CORE	P	**Core Power Rail** This voltage powers the core logic of the C51G. It is derived from the main silver box "PS_ON" power supply rails.
+1.2V_HT	P	**Isolated HyperTransport Power Rail** Since the **+1.2V_CORE** power rail is enabled simultaneously with the **+3.3V** main power supply rail and before the CPU power is valid, the enable of this rail must be delayed to honor the AMD power sequence. Most NVIDIA MCP devices have timed digital sequencer outputs. These can be used to accurately control this sequence in accordance with AMD regulations and without using highly variable RC timing circuits.
+1.2V_HTMCP	P	**HyperTransport to MCP Power Rail** This voltage powers the HyperTranport interface between the C51G and the MCP51. Refer to the *NVIDIA C51 and MCP51 Design Guide*.
+1.2V_PEA	P	**+1.2V PCI Express Analog Voltage** This is a filtered version of the **+1.2V_CORE** power supply and is used to power the analog circuits of the PCI Express block. Refer to the *NVIDIA C51 and MCP51 Design Guide* for details of the filter design.
+1.2V_PED	P	**+1.2V PCI Express Digital Voltage** This is a filtered version of the **+1.2V_CORE** power supply and is used to power the digital circuits of the PCI Express block. Refer to the *NVIDIA C51 and MCP51 Design Guide* for details of the filter design.
+1.2V_PLL	P	**+1.2V PLL Voltage** This is a filtered version of the **+1.2V_CORE** power supply and is used to power some of the internal PLLs. Refer to the *NVIDIA C51 and MCP51 Design Guide* for details of the filter design.
+1.2V_PLLCORE	P	**+1.2V Core PLL Voltage** This voltage powers the PLL of the core logic. It is a filtered version of the **+1.2V_CORE** voltage. Refer to the *NVIDIA C51 and MCP51 Design Guide* for details of the filter design.
+1.2V_PLLHTCPU	P	**+1.2V CPU HT PLL Voltage** This voltage powers the PLL of the HyperTransport interface to the CPU. It is a filtered version of the **+1.2V_CORE** voltage. Refer to the *NVIDIA C51 and MCP51 Design Guide* for details of the filter design.
+1.2V_PLLHTMCP	P	**+1.2V MCP HT PLL Voltage** This voltage powers the PLL of the HyperTransport interface to the MCP. It is a filtered version of the **+1.2V_CORE** voltage. Refer to the *NVIDIA C51 and MCP51 Design Guide* for details of the filter design.
+1.2V_PLLIFP	P	**+1.2V Voltage** This is a filtered version of the **+1.2V_CORE** voltage. Refer to the *NVIDIA C51 and MCP51 Design Guide* for details of the filter design.
+1.2V_PLLGPU	P	**+1.2V GPU PLL Voltage** This voltage powers the PLL of the integrated GPU. It is a filtered version of the **+1.2V_CORE** voltage. Refer to the *NVIDIA C51 and MCP51 Design Guide* for details of the filter design.
+2.5V_CORE	P	**2.5V Core Voltage** This voltage is used to power the core logic of the C51G. It is derived from the main silver box "PS_ON" power supply rails.

Table 8. Power Supply Interface (continued)

Signal	I/O	Description
+2.5V_PLLCORE	P	**+2.5V Core PLL Voltage** This voltage powers the core PLL. It is a filtered version of the **+2.5V_CORE** voltage. Refer to the *NVIDIA C51 and MCP51 Design Guide* for details of the filter design.
+2.5V_PLLGPU		**+2.5V GPU PLL Voltage** This voltage powers the PLL of the integrated GPU. It is a filtered version of the **+2.5V_CORE** voltage. Refer to the *NVIDIA C51 and MCP51 Design Guide* for details of the filter design.
+2.5V_PLLHTCPU	P	**+2.5V CPU HT PLL Voltage** This voltage powers the PLL of the HyperTransport interface to the CPU. It is a filtered version of the **+2.5V_CORE** voltage. Refer to the *NVIDIA C51 and MCP51 Design Guide* for details of the filter design.
+2.5V_PLLIFP	P	**+2.5V IFP PLL Voltage** This is a filtered version of the **+2.5V_CORE** voltage. Refer to the *NVIDIA C51 and MCP51 Design Guide* for details of the filter design.
+3.3V	P	**+3.3V Voltage** This voltage is the **+3.3V** rail supplied by the main silver box power supply. It is used to power the +3.3V I/Os.
+3.3V_DAC	P	**+3.3V DAC Voltage** This voltage power the video output DAC. It is a filtered version of the **+3.3V** power supply. Refer to the *NVIDIA C51 and MCP51 Design Guide* for details on the filter design.
+2.5V_IFPA	P	**+2.5V Voltage** This voltage rail is not used by C51G. It should be connected to **+2.5V_CORE**.
+2.5V_IFPB	P	**+2.5V Voltage** This voltage rail is not used by C51G. It should be connected to **+2.5V_CORE**.
GND	P	**Ground**
PE_GND	P	**Ground**

Clocks

Table 9. Clock Signal Descriptions

Signal	I/O	Description
CLKIN_25MHZ	I	**Non-Spread Reference Clock Input** Typically, this clock is a buffered version of the 25 MHz crystal from the downstream MCP51. It is used as the reference for the iGPU, PCI Express, and upstream HyperTransport PLLs.
CLKIN_200MHZ_P **CLKIN_200MHZ_N**	DIFF IN	**Clock In 200 MHz** This is the reference clock input for the PLL of the downstream HyperTransport link to the MCP51. It is spread spectrum capable.
CLKOUT_PRI_200MHZ_P **CLKOUT_PRI_200MHZ_N** **CLKOUT_SEC_200MHZ_P** **CLKOUT_SEC_200MHZ_N**	DIFF OUT	**Clock Out 200 MHz** These spread-spectrum capable differential clock outputs provide the HT reference inputs to the CPUs and other HT devices in the system.
SCLKIN_MCLKOUT_200MHZ_P **SCLKIN_MCLKOUT_200MHZ_N**	DIFF IN/ OUT	**Master Clock Out 200 MHz** These output clokcs behave identically to the **CLKOUT_PRI_200MHz/ CLKOUT_SEC_200MHz** signal pairs.
CLKOUT_CTERM_GND	A	**200 MHz Clock Out Termination** Please refer to the *NVIDIA C51 and MCP51 Design Guide.*

TEST/JTAG Interface

Table 10. TEST Interface Signals

Signal	I/O	Description
TEST_MODE_EN	I	This signal is pulled down to **GND** for normal operations. Please refer to the *NVIDIA C51 and MCP51 Design Guide.*
PKG_TEST	I	This signal is pulled down to **GND** for normal operations. Please refer to the *NVIDIA C51 and MCP51 Design Guide*.
JTAG_TCK	I	**JTAG Clock** This signal must be pulled down to **GND** through a resistor for normal operation. Please refer to the *NVIDIA C51 and MCP51 Design Guide.*
JTAG_TDI	I	**JTAG Serial Data Input** This signal must be pulled up to **+3.3 V** through a resistor for normal operation. Please refer to the *NVIDIA C51 and MCP51 Design Guide*.
JTAG_TDO	O	**JTAG Serial Data Output** This signal must be left as a no-connect for normal operation. Please refer to the *NVIDIA C51 and MCP51 Design Guide*.
JTAG_TMS	I	**JTAG Mode Select** This signal must be pulled up to **+3.3 V** through a resistor for normal operation. Please refer to the *NVIDIA C51 and MCP51 Design Guide*.
JTAG_TRST#	I	JTAG Reset This signal must be pulled down to **GND** through a resistor for normal operation. Please refer to the *NVIDIA C51 and MCP51 Design Guide*.

No-Connect Interface

Table 11. No-Connect Interface Signals

Signal	Description
NC	These signals should be left as a no-connect for normal operation. Please refer to the *NVIDIA C51 and MCP51 Design Guide*.

Chapter 3. Clock Domains

Clocking

The following figure shows the clocks that are used or generated by the NVIDIA C51G to and from the various peripherals. Table 12 lists the signals.

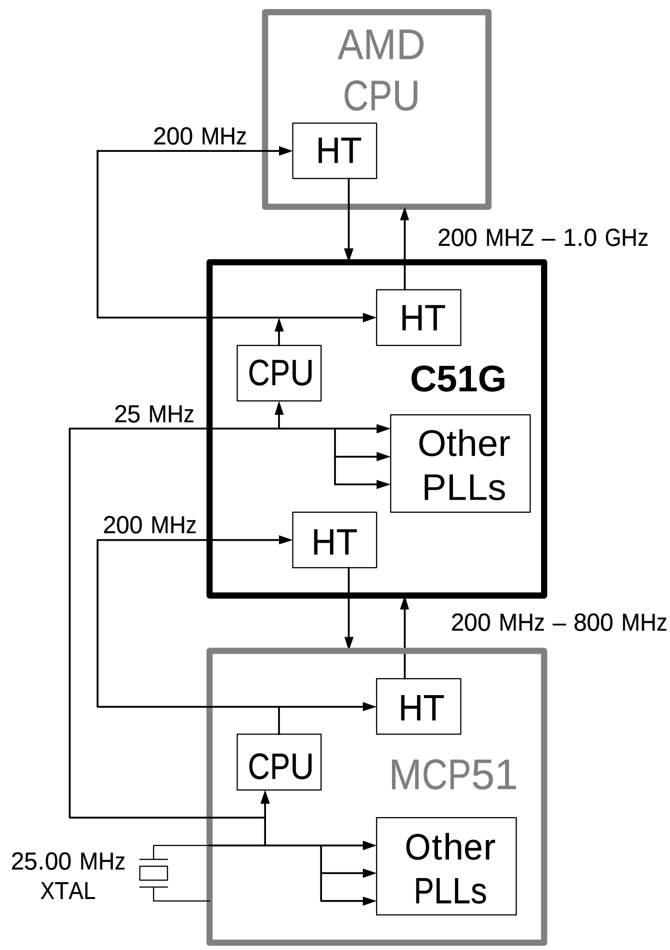


Figure 2. C51G Simple Clock Block Diagram

Table 12. Clock Signals

Clock Signal	Frequency (in MHz unless noted)	I/O	Description
HT_CPU_TX_CLK[1:0]	Variable 200 - 1000	DIFF OUT	**HyperTransport Link Differential Transmit Clocks** These clocks are used to synchronize the transmission of data to the upstream CPU.
HT_CPU_RX_CLK[1:0]	Variable 200 - 1000	DIFF IN	**HyperTransport Link Differential Receive Clocks** These clocks are used to synchronize the reception of data from the upstream CPU.
HT_MCP_TX_CLK[1:0]	Variable 200 - 1000	DIFF OUT	**HyperTransport Link Differential Transmit Clocks** These clocks are used to synchronize the transmission of data to the downstream MCP.
HT_MCP_RX_CLK[1:0]	Variable 200 - 1000	DIFF IN	**HyperTransport Link Differential Receive Clocks** These clocks are used to synchronize the reception of data from the downstream MCP.
PE[1:0]_REFCLK	100	DIFF OUT	**PCI Express Reference Clocks** These are the 100 MHz differential reference clock pairs for the x1 and ×16 PCI Express links.
CLKIN_25MHZ	25.000	I	**25 MHz Clock In** This is the non-spread reference clock input. Typically, this clock is a buffered version of the 25 MHz crystal from the downstream MCP51. It is used as the reference for the iGPU, PCI Express, and upstream HyperTransport PLLs.
CLKIN _200MHZ	200	DIFF IN	**Clock In 200 MHz** This is the spread-spectrum capable reference input clock for the PLL of the downstream HyperTransport link to the MCP51.
CLKOUT_PRI_200MHZ **CLKOUT_SEC_200MHz**	200	DIFF OUT	**Clock Out 200 MHz** These spread-spectrum capable differential clock outputs provide the HyperTransport reference inputs to the CPUs and other HyperTransport devices in the system.
SCLKIN_MCLKOUT_200MHZ	200	DIFF I/O	**Slave Clock In 200 MHz/Master Clock Out 200 MHz** When the C51G is in master mode, this becomes an output clock which behaves identically to the **CLKOUT_PRI_200MHZ/CLKOUT_SEC_200MHZ** signals**.** When the C51G is in slave mode, this becomes the spread-spectrum capable reference clock input for the PLL of the upstream HyperTransport link to the CPU.
PE_REFCLKIN	100 MHz	DIFF IN	**PCI Express Reference Clock Input** **T**hese signals are the 100 MHz differential reference clock pair input for the PCI Express link.
PE_TSTCLK	100 MHz	DIFF OUT	**PCI Express Test Clock Output** These signals are the differential test clock pair of the PCI Express link.
JTAG_TCK	Variable	I	**JTAG Clock** This signal must be pulled down to **GND** through a resistor for normal operation.

Chapter 4.
Power Sequencing and Reset

Power Sequencing and Reset Information

Please refer to the *NVIDIA C51and MCP51 Design Guide* for information, because the Power Sequencing and RESET are dependent upon motherboard design implementations.

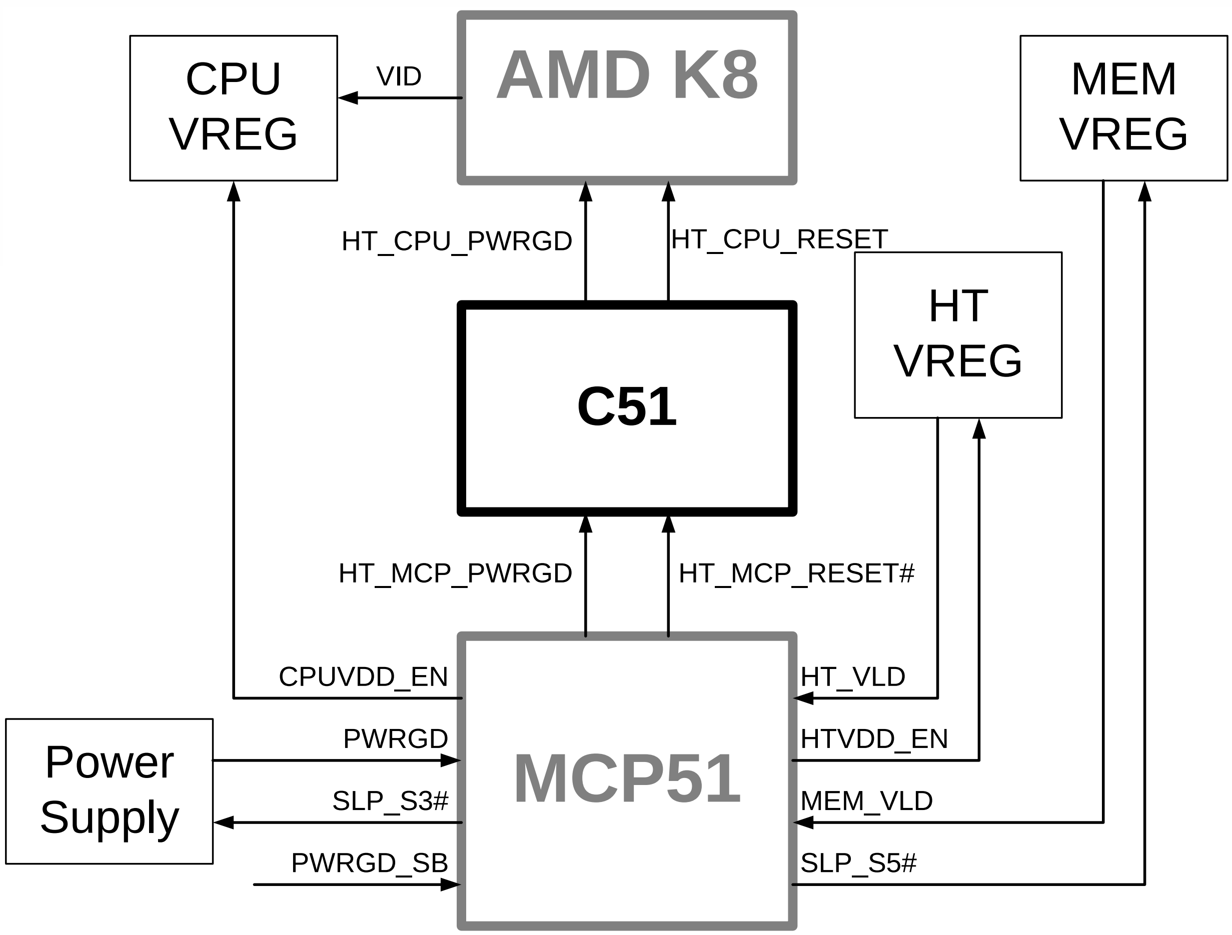


Figure 3. C51 Power Sequencing

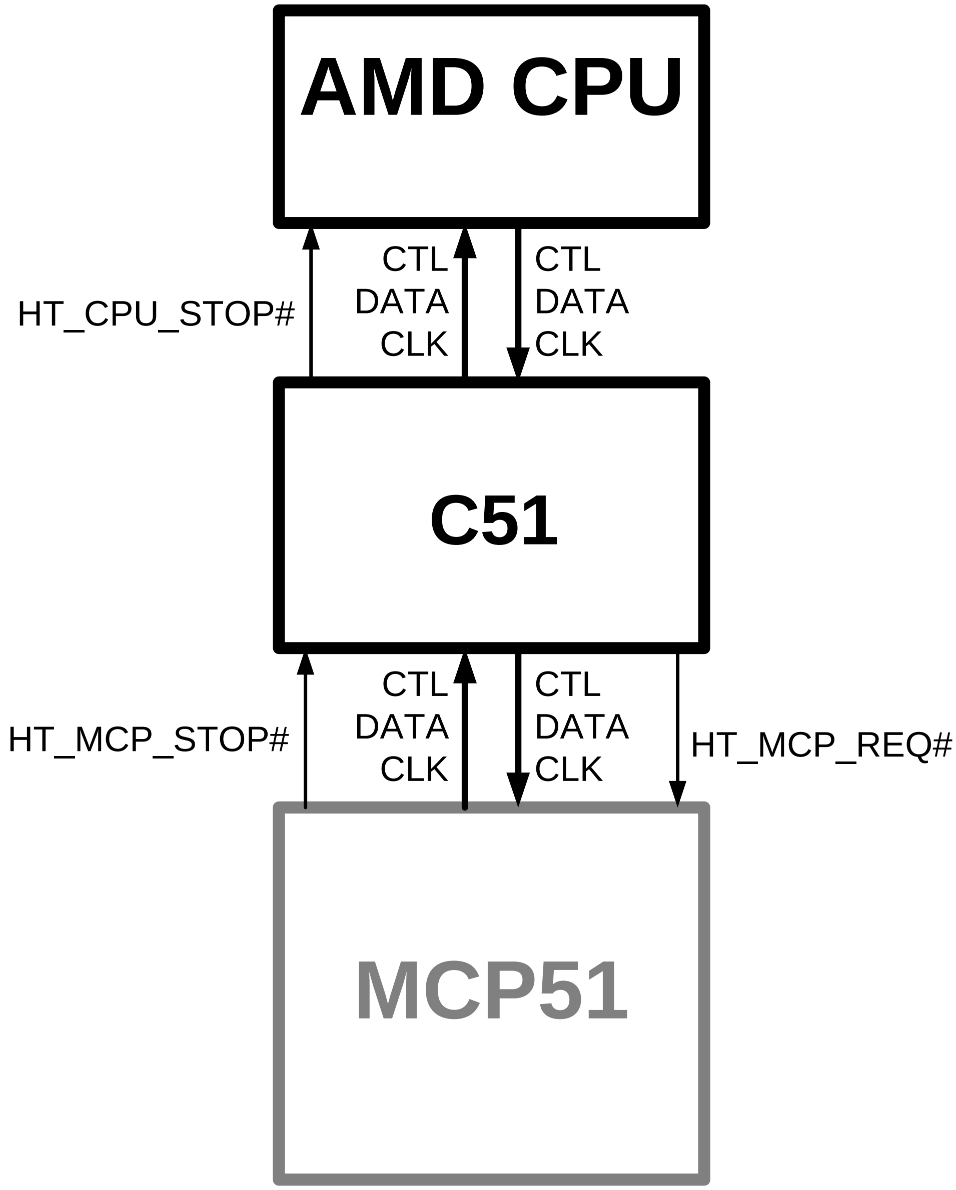


Figure 4. C51 HyperTransport Link Sequencing

Chapter 5.
Pin States

Signal Connections

Table 13 lists the signal connections and Table 14 list the signal states.

Table 13. Signal Connections

Notes: I/O = Bidirectional OD = Open Drain I = Input O = Output OC = Open Collector			
Signal	**I/O**	**Voltage Tolerance Rail**	**Voltage Drive Rail**
HT_CPU_REQ#	I	+2.5V	
HT_CPU_STOP#	OD	+2.5V	
HT_CPU_RX_CLK[1:0]	DIFF IN	+1.2V_HT	
HT_CPU_RXCTL	DIFF IN	+1.2V_HT	
HT_CPU_RXD[15:0]	DIFF IN	+1.2V_HT	
HT_CPU_TX_CLK[1:0]	DIFF OUT	+1.2V_HT	+1.2V_HT
HT_CPU_TXCTL	DIFF OUT	+1.2V_HT	+1.2V_HT
HT_CPU_TXD[15:0]	DIFF OUT	+1.2V_HT	+1.2V_HT
HT_CPU_PWRGD	OD	+2.5V	+2.5V
HT_CPU_RESET#	OD	+2.5V	+2.5V
HT_MCP_REQ#	OD	+2.5V	
HT_MCP_STOP#	I	+3.3V	
HT_ MCP_RX_CLK[1:0]	DIFF IN	+1.2V_HTMCP	
HT_ MCP_RX_CTL	DIFF IN	+1.2V_HTMCP	
HT_ MCP_RXD[15:0]	DIFF IN	+1.2V_HTMCP	
HT_ MCP_TX_CLK[1:0]	DIFF OUT	+1.2V_HTMCP	+1.2V_HTMCP
HT_ MCP_TX_CTL	DIFF OUT	+1.2V_HTMCP	+1.2V_HTMCP
HT_ MCP_TXD[15:0]	DIFF OUT	+1.2V_HTMCP	+1.2V_HTMCP
HT_ MCP_PWRGD	I	+3.3V	
HT_ MCP_RESET#	I	+3.3V	
PE0_PRSNT#	I	+3.3V	

Table 13. Signal Connections (continued)

Notes: I/O = Bidirectional OD = Open Drain I = Input O = Output OC = Open Collector

Signal	I/O	Voltage Tolerance Rail	Voltage Drive Rail
PE0_REFCLK	DIFF OUT		+1.2V
PE0_RX[15:0]	DIFF IN	+1.5V_PE_A	
PE0_TX[15:0]	DIFF OUT	+1.5V_PE_A	+1.5V_PE_A
PE1_CLKREQ#	I	+3.3V	
PE1_PRSNT#	I	+3.3V	
PE1_REFCLK	DIFF OUT		+1.2V
PE1_RX	DIFF IN	+1.5V_PE_A	
PE1_TX	DIFF OUT	+1.5V_PE_A	+1.5V_PE_A
PE_REFCLKIN	DIFF IN	+1.5V_PE_A	
PE_RESET#	O	+3.3V	+3.3V
DAC_RED **DAC_GREEN** **DAC_BLUE**	O	+3.3V +3.3V +3.3V	+3.3V +3.3V +3.3V
DAC_HSYNC	I/O	+3.3V	+3.3V
DAC_VSYNC	I/O	+3.3V	+3.3V
CLKIN_25MHZ	I	+3.3V	
CLKIN_200MHZ	DIFF IN	+3.3V	
CLKOUT_PRI_200MHZ	DIFF OUT	+2.5V	+2.5V
CLKOUT_SEC_200MHZ	DIFF OUT	+2.5V	+2.5V
SCLKIN_MCLKOUT_ 200MHZ	DIFF I/O	+2.5V	+2.5V

Signal States

Table 14. Signal States

Notes: Z = Tri-state I/O = Bidirectional I = Input O = Output OC = Open Collector OD = Open Drain U = Unpowered L = Low H=High

Signal	During Reset	After RST (SO)	S1 (POS)	S3 (STR)	S4/S5 (SOFF)
HT_CPU_REQ#	I	I	I	U	U
HT_CPU_STOP#	H	O	L	U	U
HT_CPU_RX_CLK[1:0]	I	I	I	U	U
HT_CPU_RXCTL	I	I	I	U	U
HT_CPU_RXD[15:0]	I	I	I	U	U
HT_CPU_TX_CLK[1:0]	O	O	Z	U	U
HT_CPU_TXCTL	Z	O	Z	U	U
HT_CPU_TXD[15:0]	Z	O	Z	U	U
HT_CPU_PWRGD	L/H	H	H	U	U
HT_CPU_RESET#	L	H	H	U	U
HT_MCP_REQ#	H	O	O	U	U
HT_MCP_STOP#	De-asserted at least 1 uS before HT_RESET	I	I	U	U
HT_ MCP_RX_CLK[1:0]	O	O	O	U	U
HT_ MCP_RX_CTL	O	O	O	U	U
HT_ MCP_RXD[15:0]	O	O	O	U	U
HT_ MCP_TX_CLK[1:0]	O	O	Z	U	U
HT_ MCP_TX_CTL	Z	O	Z	U	U
HT_ MCP_TXD[15:0]	Z	O	Z	U	U
HT_ MCP_PWRGD	I	I	I	U	U
HT_ MCP_RESET#	I	I	I	U	U
PE0_PRSNT#	I	I	I	U	U
PE0_REFCLK	O	O	O	U	U
PE0_RX[15:0]	I	I	I	U	U
PE0_TX[15:0]	Z	O	O	U	U
PE1_CLKREQ#	I	I	I	U	U
PE1_PRSNT#	I	I	I	U	U
PE1_REFCLK	O	O	O	U	U
PE1_RX	I	I	I	U	U
PE1_TX	Z	O	O	U	U

Notes: Z = Tri-state I/O = Bidirectional I = Input O = Output OC = Open Collector OD = Open Drain U = Unpowered L = Low H=High

Signal	During Reset	After RST (SO)	S1 (POS)	S3 (STR)	S4/S5 (SOFF)
PE_REFCLKIN	I	I	I	U	U
PE_RESET#	L	O	O	U	U
DAC_RED **DAC_GREEN** **DAC_BLUE**	O O O	O O O	O O O	U U U	U U U
DAC_HSYNC	O	O	O	U	U
DAC_VSYNC	O	O	O	U	U
CLKIN_25MHZ	I	I	I	U	U
CLKIN_200MHZ	I	I	I	U	U
CLKOUT_PRI_200MHZ	O	O	O	U	U
CLKOUT_SEC_200MHZ	O	O	O	U	U
SCLKIN_MCLKOUT_ 200MHZ	Z	I/O	I/O	U	U

Chapter 6. Mechanical Specifications

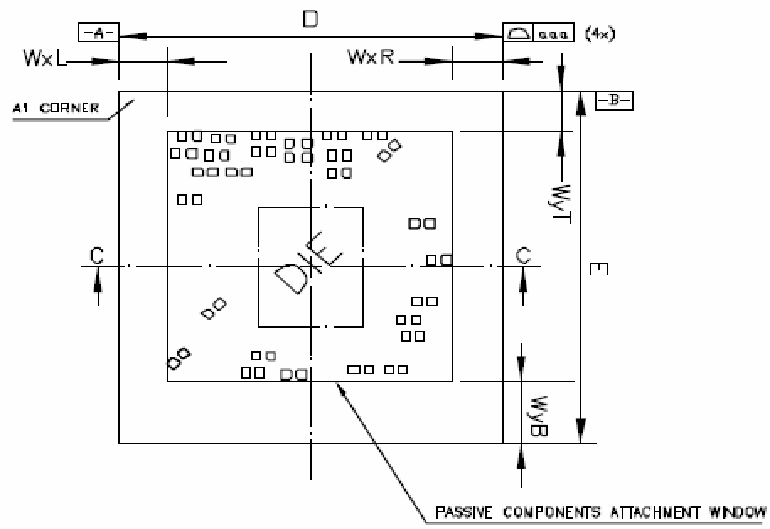
Dimention (P.37~P.38)

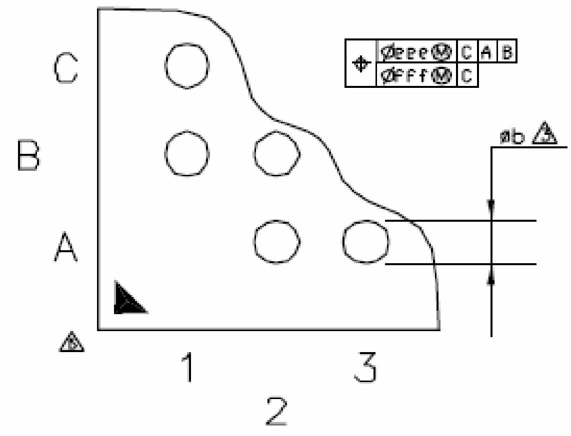
The C51G is a 25 × 25 package with 468 balls with a 1mm ball pitch. Table 15 lists the package dimensions and Figure 5 shows the package drawings.

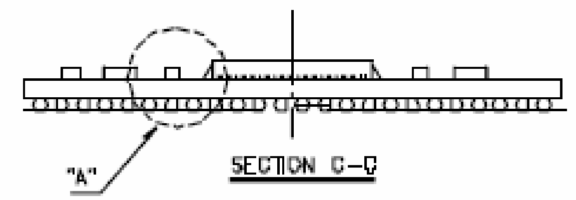
Table 15. PBGA Package Dimensions

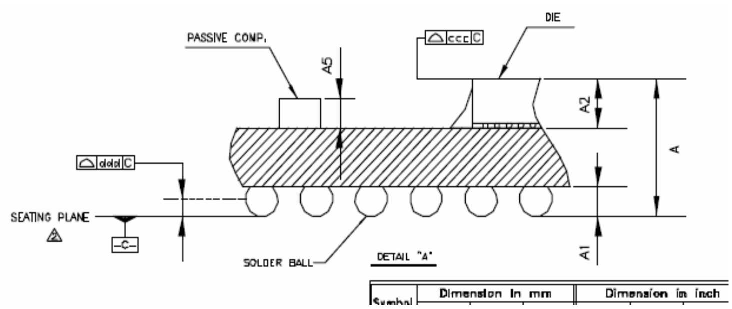
Ref	Dimensions in Millimeter			Dimensions in Inches		
	Min	Nom	Max	Min	Nom	Max
A	2.25	2.50	2.65	0.089	0.098	0.104
A1	0.43	0.52	0.60	0.017	0.020	0.024
A2	0.82	0.87	0.95	0.032	0.034	0.037
A5	0.46	0.53	0.58	0.018	0.021	0.023
D/E	24.30	24.50	24.70	0.857	0.985	0.972
D1/E1	23.00 Basic			0.906 Basic		
WxL	3.1 Basic			0.12 Basic		
WxR	3.5 Basic			0.14 Basic		
WyT	3.1 Basic			0.12 Basic		
WyB	4.6 Basic			0.18 Basic		
e	1.00 Basic			0.039 Basic		
b	0.51	0.60	0.74	0.020	0.024	0.029
aaa	0.20			0.006		
ccc	0.35			0.014		
ddd	0.20			0.006		
eee	0.30			0.012		
fff	0.10			0.004		
	Total Number of Balls: 436					
	Package Size: 25 mm × 25 mm					

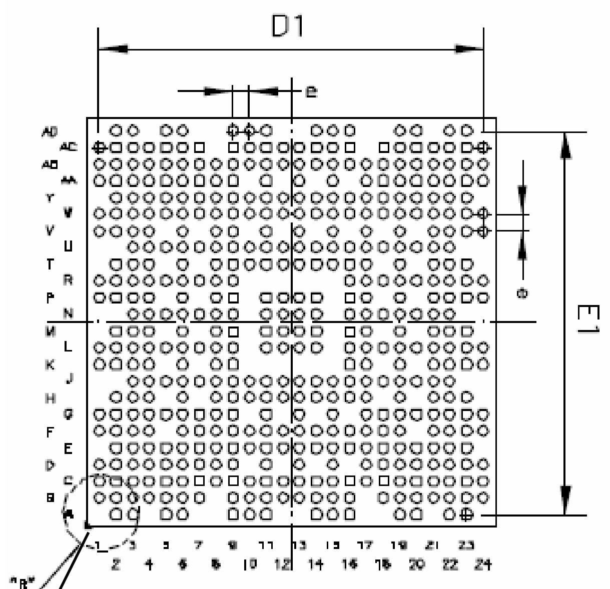
Top View











Bottom View

1. Controlling dimension: Millimeter
2. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary datum C.
4. There must be a minimum clearance of 0.15 mm (0.060 in.) between the edge of the solder ball and the body edge.
5. Die size approximately 6.7 x 8.3 mm (0.26 x 0.33 in.)
6. Die pattern of pin 1 fiducial is for reference only.
7. All passive locations shown. Some or all locations may not be populated.
8. Drawing not to scale.

Figure 5. PBGA Package Drawing

Chapter 7.
AC/DC Specifications

Absolute Ratings

The NVIDIA C51G should not be subjected to conditions exceeding the absolute maximum ratings listed in Table 16 Absolute Ratings. Exceeding these conditions can damage the functionality and affect the long-term reliability of the part.

Table 16. Absolute Ratings

Parameter	Min	Max
Case temperature under bias	0 °C	110 °C
Storage temperature	-50 °C	150 °C
Voltage on any 1.2 V pin with respect to ground	-0.5 V	1.3 V
Voltage on any 2.5 V pin with respect to ground	-0.5 V	2.7 V
Voltage on any 3.3 V pin with respect to ground	-0.5 V	3.6 V
1.2 V supply	-0.5 V	1.3 V
2.5V supply	-0.5 V	2.7 V
3.3 V supply	-0.5 V	3.6 V

Table 17. Maximum Power Dissipation

Power Dissipation	Maximum
C51PV and C51G	10 W to 14 W

Note: These maximum power numbers are estimates.

Thermal Operations

The thermal operating temperature range is given in Table 18..

Table 18. Thermal Operating Temperature

Characteristic	Range
Thermal operating temperature (TCASE)	0º C to TBD

DC Voltage Characteristics

Table 19 lists the voltage characteristics for NVIDIA C51G.

Table 19. Voltage Characteristics

Signal	Min	Max	Range
+1.2V_CORE	1.14 V	1.26 V	± 0.06 V
+1.2V_HT	1.14 V	1.26 V	± 0.06 V
+1.2V_HTMCP	1.14 V	1.26 V	± 0.06 V
+1.2V_PEA	1.14 V	1.26 V	± 0.06 V
+1.2V_PED	1.14 V	1.26 V	± 0.06 V
+1.2V_PLL	1.14 V	1.26 V	± 0.06 V
+1.2V_PLLCORE	1.14 V	1.26 V	± 0.06 V
+1.2V_PLLHTMCP	1.14 V	1.26 V	± 0.06 V
+1.2V_PLLIFP	1.14 V	1.26 V	± 0.06 V
+2.5V_CORE	2.3 V	2.7 V	± 0.20 V
+2.5V_PLLCORE	2.3 V	2.7 V	± 0.20 V
+2.5V_PLLGPU	2.3 V	2.7 V	± 0.20 V
+2.5V_PLLHTCPU	2.3 V	2.7 V	± 0.20 V
+2.5V_PLLIFP	2.3 V	2.7 V	± 0.20 V
+3.3V	3.0 V	3.3 V	± 0.3 V
+3.3V_DAC	3.0 V	3.3 V	± 0.3 V
+2.5V_IFPA	2.3V/3.0V	2.7V/3.3V	± 0.20 V/±0.30V
+2.5V_IFPB	2.3V/3.0V	2.7V/3.3V	± 0.20 V/±0.30V

AC Characteristics

This section contains the following AC specifications:

- Input clock characteristics
- Output clock characteristics
- Interface characteristics
  - HyperTransport Interface
  - PCI Express Interface

Input Clock Characteristics

Table 20 provides the input clock characteristics.

Table 20. Input Clock Characteristics

Clock	Characteristic	Min	Typical	Max	Comments
CLKIN_25MHZ	Clock frequency		25 MHz		
	Clock period		40 ns		
	Clock high time	18 ns		22 ns	55/45 duty cycle
	Clock low time	18 ns		22 ns	55/45 duty cycle
	Clock rise time	1 ns		4 ns	
	Clock fall time	1 ns		4 ns	
CLKIN_200MHZ	Clock frequency		200 MHz		
	Clock period		5 ns		
	Clock high time	2.25 ns		2.75 ns	55/45 duty cycle
	Clock low time	2.25 ns		2.75 ns	55/45 duty cycle
PE_REFCLKIN	Clock frequency		100 MHz		
	Clock period		10 ns		
	Clock high time	4.5 ns		5.5 ns	55/45 duty cycle
	Clock low time	4.5 ns		5.5 ns	55/45 duty cycle

Output Clock Characteristics

Table 21 lists the AC output clock characteristics and Figure 6 shows clock timing.

Table 21. AC Output Clock Characteristics

Clock	Characteristic	Min	Typical	Max	Comments
CLKOUT_PRI_200MHZ CLKOUT_SEC_200MHZ	Clock frequency		200 MHz		
	Clock period		5 ns		
	Clock high time	2.25 ns		2.75 ns	55/45 duty cycle
	Clock low time	2.25 ns		2.75 ns	55/45 duty cycle
	Clock rise time	TBD		TBD	
	Clock fall time	TBD		TBD	
PE[1:0]_REFCLK	Clock frequency		100 MHz		
	Clock period		10 ns		
	Clock high time	4.5 ns		5.5 ns	55/45 duty cycle
	Clock low time	4.5 ns		5.5 ns	55/45 duty cycle
SCLKIN_MCLKOUT_ 200 MHZ	Clock frequency		200 MHz		
	Clock period		5 ns		
	Clock high time	2.25 ns		2.75 ns	55/45 duty cycle
	Clock low time	2.25 ns		2.75 ns	55/45 duty cycle
	Clock rise time	TBD		TBD	
	Clock fall time	TBD		TBD	

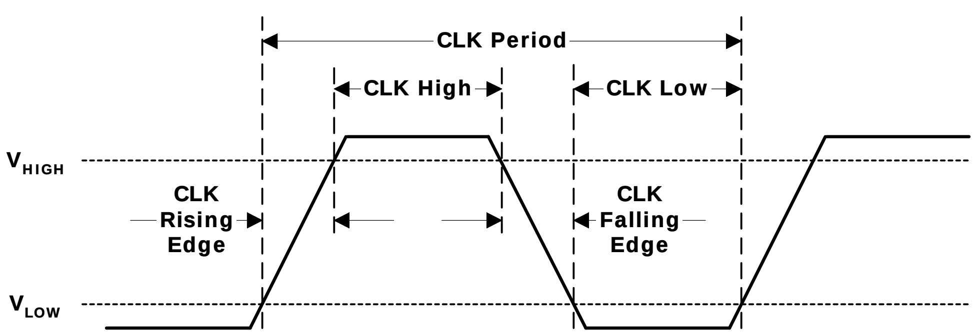


Figure 6. Clock Timing Diagram

Interface Characteristics

The AC interface characteristics are explained in the following diagrams and tables.

HyperTransport Interface

The HyperTransport interface is compliant with the *HyperTransport I/O Link Specification* published by the HyperTransport Technology Consortium. Refer to that document for full details of the interface timing.

The NVIDIA C51G meets the timing requirements for transmit and receive up to a link speed of 4000 MT/s.

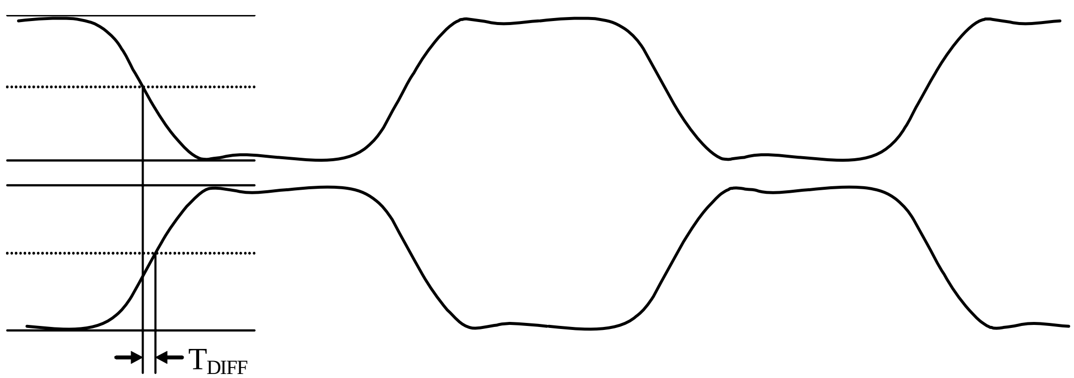


Figure 7. HyperTransport Bus T_{DIFF}

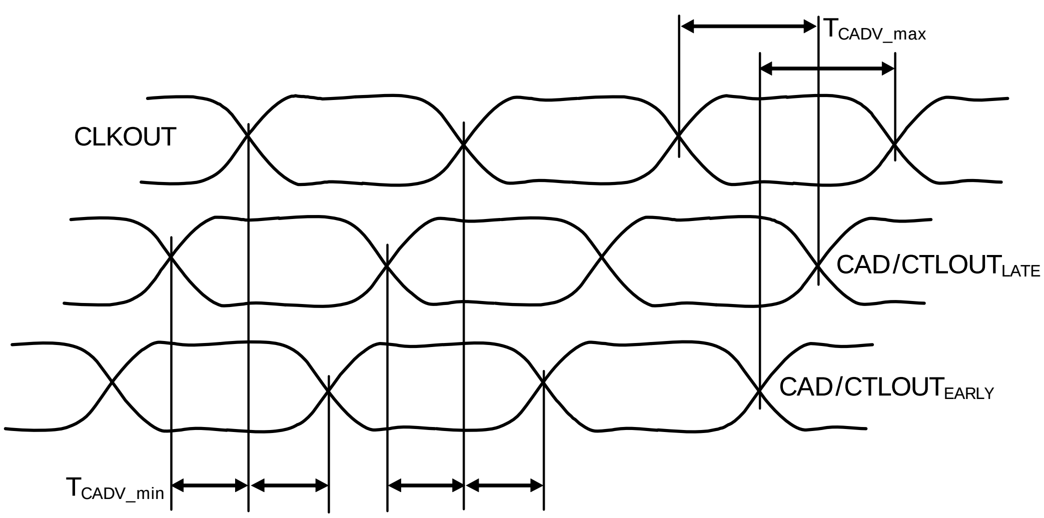


Figure 8. HyperTransport Bus T_{CAD}

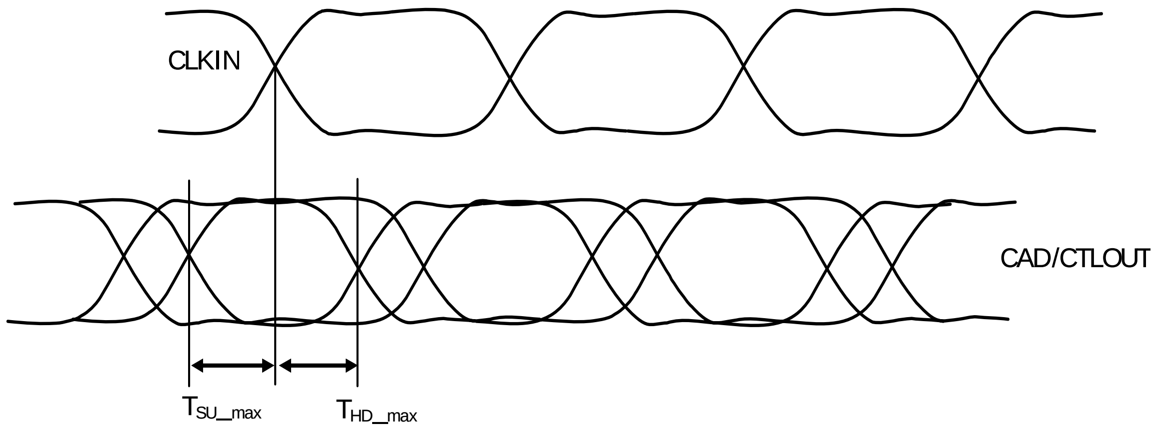


Figure 9. HyperTransport Bus T_{SU} and T_{HD}

Table 22. HyperTransport Bus

Symbol	Characteristic	Link Speed	Min	Max	Comments
T_{ODIFF}	Output differential skew	800 MT/s 1200 MT/s 1600 MT/s 2000 MT/s 2400 MT/s 3200 MT/s 4000 MT/s		70 ps 70 ps 70 ps 60 ps 60 ps 60 ps	
T_{IDIFF}	Input differential skew	800 MT/s 1200 MT/s 1600 MT/s 2000 MT/s 2400 MT/s 3200 MT/s 4000 MT/s		90 ps 90 ps 90 ps 65 ps 65 ps 65 ps	
T_{CADV}	Transmitter output CAD/ CTLOUT valid relative to CLKOUT	800 MT/s 1200 MT/s 1600 MT/s 2000 MT/s 2400 MT/s 3200 MT/s 4000 MT/s	695 ps 467 ps 345 ps 280 ps 213 ps 166 ps 140 ps	1805 ps 1200 ps 905 ps 720 ps 620 ps 459 ps	
T_{CADVRS}	Receiver input CADIN valid time to CLKIN	800 MT/s 1200 MT/s 1600 MT/s 2000 MT/s 2400 MT/s 3200 MT/s 4000 MT/s	460 ps 312 ps 225 ps 194 ps 166 ps 116 ps		

Table 22. HyperTransport Bus (continued)

Symbol	Characteristic	Link Speed	Min	Max	Comments
T_{CADVRH}	Receiver input CADIN valid time from CLKIN	800 MT/s 1200 MT/s 1600 MT/s 2000 MT/s 2400 MT/s 3200 MT/s 4000 MT/s	460 ps 312 ps 225 ps 194 ps 166 ps 116 ps		
T_{SU}	Receiver input setup time	800 MT/s 1200 MT/s 1600 MT/s 2000 MT/s 2400 MT/s 3200 MT/s 4000 MT/s		250 ps 215 ps 175 ps 153 ps 138 ps 110 ps 70 ps	
T_{HD}	Receiver input hold time	800 MT/s 1200 MT/s 1600 MT/s 2000 MT/s 2400 MT/s 3200 MT/s 4000 MT/s		250 ps 215 ps 175 ps 153 ps 138 ps 110 ps 70 ps	

PCI Express Interface

The PCI Express interface is compliant with the PCI Express Base Specification published by the PCI SIG. Refer to that document for full details of the interface timing.

The NVIDIA C51G meets the timing requirements for transmit and receive at a link speed of 2.5 Gb/s.

Table 23. Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400ps +/-300ppm. UI does not account for SSC (spread spectrum clock) dictated variations.xxxSee Note 1.
$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	0.800		1.2	V	V TX-DIFFp-p = 2*|V TX-D+ - V TX-D-|.xxxSee Note 2.
$V_{TX-DE-RATIO}$	De-emphasized differential output voltage (ratio)	-3.0	-3.5	-4.0	dB	This is the ratio of the V TX-DIFFp-p of the second and following bits after a transition divided by the xxxV TX -DIFFp-p of the first bit after a transition.xxxSee Note 2.
V_{TX-EYE}	Minimum TX eye width	0.70			UI	The maximum transmitter jitter can be derived as T TX-MAX JITTER = 1 - T TX-EYE = 0.3 UI.xxxSee Notes 2 and 3.
$V_{TX-EYE-MEDIAN-TO-MAX-JITTER}$	Maximum time between jitter median and maximum deviation from the median			0.15	UI	Jitter is defined as the measurement variation of the crossing points (V TX-DIFFp-p = 0 V) in relation to an appropriate average TX UI.xxxSee Notes 2 and 3.
$V_{TX-RISE}$ $V_{TX-FALL}$	D+/D- TX output rise/fall time	0.125			UI	See Notes 2 and 5.
$V_{TX-CM-ACp}$	AC peak common mode output voltage			20	mV	V TX-CM-ACp = |V TX-D+ + V TX-D-|/2 - V TX-CM-DCxxxV TX-CM-DC = DC(avg) of |V TX-D+ + V TX-D-|/2 during L0.xxxSee Note 2.
$V_{TX-CM-DC-ACIVE-IDLE-DELTA}$	Absolute delta of DC common mode voltage during L0 and electrical idle	0		100	mV	|V TX-CM-DC [during L0] - V TX-CM-IDLE-DC[during Electrical Idle]| <= 100 mVxxxV TX-CM-DC = DC(avg) of |V TX-D+ + V TX-D-|/2 [L0]xxxV TX-CM-IDLE-DC = DC(avg) of |V TX-D+ + V TX-D-|/2 [Electrical Idle]. xxxSee Note 2.
$V_{TX-CM-DC-LINE-DELTA}$	Absolute delta of DC common mode voltage between D+ and D-	0		25	mV	|V TX-CM-DC-D+ [during L0] - V TX-CM-IDLE-DC-D-[during L0]| <= 25 mV xxxV TX-CM-DC-D+ = DC(avg) of |V TX-D+| [during L0] xxxV TX-CM-DC-D- = DC(avg) of |V TX-D-| [during L0]. xxxSee Note 2.
$V_{TX-IDLE-DIFFp}$	Electrical idle differential peak output voltage	0		20	mV	V TX-IDLE-DIFFp = |V TX-IDLE-D+ - V TX-IDLE-D-| <= 20 mV xxxSee Note 2.

Table 23. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during receiver detection			600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present.xxxSee Figure 8.
$V_{TX-IDLE-MIN}$	Minimum time spec in electrical idle	50			UI	Minimum time a transmitter must be electrical idle.
$V_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set			20	UI	After sending an electrical idle ordered-set, the transmitter must meet all electrical idle specifications within this time.
$V_{TX-IDLE-RCVDETECT-MAX}$	Maximum time spent in electrical idle before initiating a receiver detect sequence			100	ms	Maximum time spent in electrical idle before initiating a receiver detect sequence.xxxSee Figure 8.
$RL_{TX-DIFF}$	Differential return loss	12			dB	Measured over 50 MHz to 1.25 GHz.xxxSee Note 4.
RL_{TX-CM}	Common mode return loss	6			dB	Measured over 50 MHz to 1.25 GHz.xxxSee Note 4.
$Z_{TX-DIFF-DC}$	DC differential TX impedance	80	100	120	?	TX DC differential mode low impedance.
$Z_{TX-COM-High-IMP-DC}$	Transmitter common mode high impedance state (DC)	5		20	K?	TX DC high impedance.
$L_{TX-SKEW}$	Lane-to-lane skew			500	ps	Between any two lanes within a single transmitter.

Table 23. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
C_{TX}	AC coupling capacitor	75		200	pF	All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.

Notes:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-31 of the PCI Express Base Specification Revision 1.0 and measured over any 250 consecutive TX UIs. (Also refer to the Transmitter Compliance Eye Diagram shown in Figure 4-30 of the PCI Express Base Specification Revision 1.0.)
3. A TTX-EYE = 0.70 UI provides for a total sum of deterministic and random jitter budget of TTX-JITTER-MAX =0.30 UI for the transmitter collected over any 250 consecutive TX UIs. The TTX-EYE-MEDIAN-TO-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the average time value.
4. The transmitter output impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 ohms to ground for both the D+ and D- line (i.e., as measured by a Vector Network Analyzer with 50 ohm probes - see Figure 4-31 of the PCI Express Base Specification Revision 1.0). Note that the series capacitor CTX is optional for the return loss measurement.
5. Measured between 20%-80% at transmitter package pins into a test load as shown in Figure 4-31 for both VTX-D+ and VTX-D-.

Table 24. Differential Transmitter (RX) Output Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400ps +/-300 ppm. UI does not account for SSC dictated variations.
$V_{RX\text{-}DIFFp\text{-}p}$	Differential input peak-to-peak voltage	0.175		1.2	V	$V_{RX\text{-}DIFFp\text{-}p} = 2*\lvert V_{RX\text{-}D+} - V_{RX\text{-}D-}\rvert$. See Note 7.
$V_{RX\text{-}EYE}$	Minimum RX eye width	0.40			UI	The maximum interconnect media and transmitter jitter can be tolerated by the receiver can be derived as $T_{RX\text{-}MAX\ JITTER} = 1 - T_{RX\text{-}EYE} = 0.6$ UI. See Notes 7 and 8.
$V_{TX\text{-}EYE\text{-}MEDIAN\text{-}TO\text{-}MAX\text{-}JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX\text{-}DIFFp\text{-}p} = 0$ V) in relation to an appropriate average TX UI. See Notes 7 and 8.
$V_{RX\text{-}CM\text{-}ACp}$	AC peak common mode input voltage			150	mV	$V_{RX\text{-}CM\text{-}ACp} = \lvert V_{RX\text{-}D+} + V_{RX\text{-}D-}\rvert/2 - V_{RX\text{-}CM\text{-}DC}$ $V_{RX\text{-}CM\text{-}DC}$ = DC(avg) of $\lvert V_{RX\text{-}D+} + V_{RX\text{-}D-}\rvert/2$ during L0. See Note 7.
$RL_{RX\text{-}DIFF}$	Differential return loss	15			dB	Measured over 50 MHz to 1.25 GHz. See Note 9.
$R_{RX\text{-}CM}$	Common mode return loss	6			dB	Measured over 50 MHz to 1.25 GHz. See Note 9.
$Z_{RX\text{-}DIFF\text{-}DC}$	DC differential RX impedance	80	100	120	?	RX DC differential mode low impedance. See Note 10.
$Z_{RX\text{-}COM\text{-}DC}$	DC input common mode input impedance	40	50	60	?	RX DC common mode impedance 50 ohms +/-20% tolerance. See Note 7 and 10.
$Z_{RX\text{-}COM\text{-}INITIAL\text{-}DC}$	Initial DC input common mode input impedance	5	50	60	?	RX DC common mode impedance allowed when the receiver terminations are first powered on. See Note 11
$Z_{RX\text{-}COM\text{-}HIGH\text{-}IMP\text{-}DC}$	Powered down DC input common mode input impedance	200			K?	RX DC common mode impedance when the receiver terminations are not powered (i.e., no power). See Note 12
$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$	Electrical idle threshold	65		175	mV	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p} = 2*\lvert V_{RX\text{-}D+} - V_{RX\text{-}D-}\rvert$ Measured at the package pins of the receiver.

Table 24. Differential Transmitter (RX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$T_{RX\text{-}IDLE\text{-}DET\text{-}OFF\text{-}ENTERTIME}$	Unexpected electrical idle enter detect threshold integration time			10	ms	An unexpected electrical idle ($V_{RX\text{-}DIFFp\text{-}p} < V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$) must be recognized no longer than $V_{RX\text{-}IDLE\text{-}DET\text{-}OFF\text{-}ENTERTIME}$ to signal an unexpected idle condition.
$L_{TX\text{-}SKEW}$	Lane-to-lane skew			20	ns	Across all lanes on a port. This includes variation in the length of a skip ordered-set (e.g., COM and 1 to 5 SKP symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:

6. No test load is necessarily associated with this value.
7. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-31 of the PCI Express Base Specification Revision 1.0 and measured over any 250 consecutive TX UIs. (Also refer to the Transmitter Compliance Eye Diagram shown in Figure 4-30 of the PCI Express Base Specification Revision 1.0.)
8. A TTX-EYE = 0.70 UI provides for a total sum of deterministic and random jitter budget of TTX-JITTER-MAX =0.30 UI for the transmitter collected over any 250 consecutive TX UIs. The TTX-EYE-MEDIAN-TO-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the average time value.
9. The transmitter output impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 ohms to ground for both the D+ and D- line (i.e., as measured by a Vector Network Analyzer with 50 ohm probes - see Figure 4-31 of the PCI Express Base Specification Revision 1.0). Note that the series capacitor CTX is optional for the return loss measurement.
10. Measured between 20%-80% at transmitter package pins into a test load as shown in Figure 4-31 for both VTX-D+ and VTX-D-.

Industry Standards

The following industry standard documents are referenced in this document. You should reference these as well as this document.

- *HyperTransport I/O Link Specification*
  Revision 1.03, HyperTransport Technology Consortium
- *EIA/JEDEC Standard EIA/JESD8-5*
  October 1995
- *PCI Express Base Specification*
  Revision 1.0a

Appendix A.
Pin Listing

Table 25 provides the ball listing by package ball and Table 26 provides the ball listing by the signal name

Ball Listing by Signal Name

Table 25. Ball Listing by Signal Name

Ball	Signal Name
A2	+1.2V_PLL
A3	+1.2V_PEA
A5	DAC_RED
A6	DAC_BLUE
A9	+3.3V_DAC
A19	JTAG_TRST#
A20	SCLKIN_MCLKOUT_ 200MHZ_P
A22	CLKOUT_SEC_ 200MHZ_P
A23	GND
B1	GND
B2	+1.2V_PLL
B3	+1.2V_PEA
B4	+1.2V_PED
B5	+1.2V_CORE
B6	DAC_GREEN
B7	DAC_HSYNC
B16	+2.5V_CORE
B18	JTAG_TMS
B19	JTAG_TDI
B20	SCLKIN_MCLKOUT_ 200MHZ_N
B21	CLKOUT_SEC__20 0MHZ_N
B22	CLKOUT_ CTERM_GND
B23	CLKOUT_PRI_ 200MHZ_N
B24	CLKOUT_PRI_ 200MHZ_P
C1	GND
C2	+1.2V_PLL
C3	+1.2V_PLL
C4	+1.2V_PEA
C5	+1.2V_PED
C6	+1.2V_CORE
C7	DAC_VSYNC

Ball	Signal Name
C8	DAC_IDUMP
C10	+3.3V
C11	GND
C16	+2.5V_CORE
C17	TEST_MODE_EN
C18	JTAG_TCK
C19	JTAG_TDO
C20	GND
C21	+1.2V_HT
C22	GND
C23	HT_CPU_TXD0_P
C24	HT_CPU_TXD0_N
D1	PE0_PRSNT#
D2	PE_CTERM_GND
D3	PE1_CLKREQ#
D4	+1.2V_PLL
D5	+1.2V_PEA
D6	+1.2V_PED
D7	+1.2V_CORE
D8	DAC_RSET
D9	DAC_VREF
D11	GND
D17	PKG_TEST
D18	+3.3V
D19	GND
D20	HT_CPU_RESET#
D21	HT_CPU_TXD8_P
D22	HT_CPU_TXD8_N
D23	HT_CPU_TXD1_P
D24	HT_CPU_TXD1_N
E2	PE1_PRSNT#
E5	+1.2V_PLL
E6	+1.2V_PEA
E7	+1.2V_PED
E8	+1.2V_CORE
E9	+1.2V_CORE
E10	+1.2V_CORE

Ball	Signal Name
E11	NC
E12	GND
E15	GND
E16	+2.5V_PLLIFP
E17	NC
E18	GND
E19	HT_CPU_PWRGD
E20	HT_CPU_TXD9_N
E21	HT_CPU_TXD10_N
E22	HT_CPU_TXD2_P
E23	HT_CPU_TXD2_N
F1	PE_TSTCLK_P
F2	PE_TSTCLK_N
F3	PE_GND
F4	PE_GND
F6	+1.2V_PLL
F7	+1.2V_PEA
F8	+1.2V_PEA
F9	+1.2V_PEA
F10	+1.2V_CORE
F11	+1.2V_CORE
F12	NC
F16	GND
F17	NC
F18	HT_CPU_REQ#
F19	HT_CPU_TXD9_P
F21	HT_CPU_TXD10_P
F22	GND
F23	HT_CPU_TXD3_P
F24	HT_CPU_TXD3_N
G1	PE_RESET#
G2	PE1_REFCLK_P
G3	PE1_REFCLK_N
G4	PE1_TX_P
G5	PE1_TX_N
G6	PE1_RX_P
G7	+1.2V_PLL

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Ball	Signal Name
G8	+1.2V_PLL
G9	+1.2V_PLL
G11	+1.2V_CORE
G13	GND
G15	+2.5V_IFPA
G17	NC
G18	HT_CPU_STOP#
G19	HT_CPU_TXD11_N
G20	HT_CPU_TXD11_P
G21	HT_CPU_TX_CLK1_N
G22	HT_CPU_TX_CLK1_P
G23	HT_CPU_TX_CLK0_P
G24	HT_CPU_TX_CLK0_N
H6	PE1_RX_N
H8	PE_GND
H9	PE_GND
H10	+1.2V_PLL
H11	+1.2V_CORE
H12	+2.5V_PLLCORE
H13	+2.5V_PLLGPU
H14	GND
H15	+2.5V_IFPB
H16	+1.2V_PLLIFP
H17	+1.2V_HT
H19	GND
H21	GND
H22	HT_CPU_TXD4_P
H23	HT_CPU_TXD4_N
J5	PE0_RX1_N
J6	PE0_RX1_P
J7	PE0_RX0_N
J8	PE0_RX0_P
J9	PE0_RX2_N
J10	+1.2V_PLL
J11	+1.2V_CORE
J12	+1.2V_CORE
J13	+1.2V_CORE
J14	+1.2V_CORE

Ball	Signal Name
J15	GND
J16	GND
J17	GND
J18	HT_CPU_TXD12_N
J19	HT_CPU_TXD12_P
J20	+1.2V_HT
J21	HT_CPU_TXD5_P
J22	HT_CPU_TXD5_N
K1	PE0_REFCLK_P
K2	PE0_REFCLK_N
K4	PE_GND
K6	PE_GND
K8	PE_GND
K9	PE0_RX2_P
K16	+1.2V_HT
K17	HT_CPU_TXD13_N
K19	HT_CPU_TXD14_N
K21	HT_CPU_TXD6_P
K22	HT_CPU_TXD6_N
K23	HT_CPU_TXD7_P
K24	HT_CPU_TXD7_N
L1	PE0_TX0_P
L2	PE0_TX0_N
L3	PE0_TX1_P
L4	PE0_TX2_P
L5	PE0_RX3_N
L6	PE0_RX3_P
L7	PE0_RX4_P
L8	PE0_RX4_N
L9	PE_GND
L11	GND
L12	GND
L13	GND
L14	GND
L16	+2.5V_PLLHTCPU
L17	HT_CPU_TXD13_P
L18	HT_CPU_TXD15_P
L19	HT_CPU_TXD15_N
L20	HT_CPU_TXD14_P
L21	GND
L22	GND

Ball	Signal Name
L23	HT_CPU_TXCTL_P
L24	HT_CPU_TXCTL_N
M2	PE0_TX1_N
M3	PE0_TX2_N
M4	PE0_TX3_P
M6	PE_GND
M8	PE0_RX5_N
M9	PE0_RX5_P
M11	GND
M12	GND
M13	GND
M14	GND
M16	+1.2V_HT
M17	HT_CPU_RXD15_P
M19	GND
M21	+1.2V_HT
M22	HT_CPU_RXCTL_N
M23	HT_CPU_RXCTL_P
N3	PE0_TX3_N
N4	PE_GND
N5	PE0_RX7_N
N6	PE0_RX7_P
N7	PE0_RX6_N
N8	PE0_RX6_P
N9	PE_GND
N11	GND
N12	GND
N13	GND
N14	GND
N16	+1.2V_PLLHTCPU
N17	GND
N18	HT_CPU_RXD15_N
N19	HT_CPU_RXD14_N
N20	HT_CPU_RXD14_P
N21	HT_CPU_RXD7_N
N22	HT_CPU_RXD7_P
P1	PE0_TX4_P
P2	PE0_TX4_N
P3	PE0_RX9_P
P4	PE0_RX9_N
P6	PE_GND

Ball	Signal Name
P8	PE_GND
P9	+1.2V_PLLCORE
P11	GND
P12	GND
P13	GND
P14	GND
P16	HT_CPU_RXD13_P
P17	HT_CPU_RXD13_N
P19	GND
P21	HT_CPU_RXD6_N
P22	HT_CPU_RXD6_P
P23	HT_CPU_RXD5_N
P24	HT_CPU_RXD5_P
R1	PE0_TX5_P
R2	PE0_TX5_N
R3	PE0_TX6_P
R4	PE0_TX7_P
R5	PE0_RX8_N
R6	PE0_RX8_P
R7	PE0_RX10_N
R8	PE0_RX10_P
R9	+1.2V_PLLGPU
R16	+1.2V_HT
R17	GND
R18	HT_CPU_RXD12_P
R19	HT_CPU_RXD12_N
R20	HT_CPU_RX_CLK1_N
R21	HT_CPU_RX_CLK1_P
R22	GND
R23	HT_CPU_RXD4_N
R24	HT_CPU_RXD4_P
T2	PE0_TX6_N
T3	PE0_TX7_N
T4	PE_GND
T6	PE_GND
T8	PE0_RX12_P
T9	PE0_RX12_N
T10	HT_MCP_RX_CLK1_N
T11	+1.2V_PLLPE
T12	GND
T13	+1.2V_PLLHTMCP
T14	GND
T15	+1.2V_HTMCP
T16	+1.2V_HT
T17	GND
T19	GND
T21	HT_CPU_RXD11_P
T22	HT_CPU_RX_CLK0_N
T23	HT_CPU_RX_CLK0_P
U3	PE0_TX8_N
U4	PE0_TX8_P
U5	PE0_RX11_N
U6	PE0_RX11_P
U7	PE0_RX13_P
U8	PE0_RX13_N
U9	PE_GND
U10	HT_MCP_RX_CLK1_P
U11	+1.2V_HTMCP
U12	GND
U13	+1.2V_HTMCP
U14	GND
U15	+1.2V_HTMCP
U16	+1.2V_HTMCP
U17	+1.2V_HT
U18	GND
U19	GND
U20	HT_CPU_RXD11_N
U21	HT_CPU_RXD3_N
U22	HT_CPU_RXD3_P
V1	PE0_TX9_P
V2	PE0_TX9_N
V3	PE0_RX14_N
V4	PE0_RX14_P
V6	PE_GND
V8	PE_GND
V9	HT_MCP_RXD11_P
V11	HT_MCP_RXD14_P
V13	HT_MCP_RXD15_N
V15	HT_MCP_TXD12_N
V17	HT_MCP_TXD11_N
V19	GND
V21	HT_CPU_RXD9_P
V22	GND
V23	HT_CPU_RXD2_N
V24	HT_CPU_RXD2_P
W1	PE0_TX10_P
W2	PE0_TX10_N
W3	PE0_TX11_P
W4	PE_GND
W5	CLKIN_200MHZ_N
W6	PE_GND
W7	HT_MCP_RXD9_P
W8	PE_GND
W9	HT_MCP_RXD11_N
W10	HT_MCP_RXD12_N
W11	HT_MCP_RXD14_N
W12	HT_MCP_RXD15_P
W13	HT_MCP_TXD15_P
W14	HT_MCP_TXD14_N
W15	HT_MCP_TXD12_P
W16	+1.2V_HTMCP
W17	HT_MCP_TX_CLK1_N
W18	HT_MCP_TXD11_P
W19	HT_CPU_CAL_1P2V
W20	HT_CPU_RXD9_N
W21	HT_CPU_RXD10_P
W22	HT_CPU_RXD10_N
W23	HT_CPU_RXD1_N
W24	HT_CPU_RXD1_P
Y2	PE0_TX11_N
Y3	PE0_RX15_P
Y4	PE_GND
Y5	CLKIN_200MHZ_P
Y6	HT_MCP_RXD8_N

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Ball	Signal Name
Y7	HT_MCP_RXD9_N
Y8	HT_MCP_RXD10_P
Y9	+1.2V_HTMCP
Y10	HT_MCP_RXD12_P
Y11	GND
Y12	HT_MCP_RXD13_N
Y13	HT_MCP_TXD15_N
Y14	HT_MCP_TXD14_P
Y15	HT_MCP_TXD13_N
Y16	GND
Y17	HT_MCP_TX_CLK1_P
Y18	GND
Y19	HT_CPU_CAL_GND
Y20	HT_CPU_RXD8_N
Y21	HT_CPU_RXD8_P
Y22	HT_CPU_RXD0_N
Y23	HT_CPU_RXD0_P
AA1	PE0_TX12_P
AA2	PE0_TX12_N
AA3	PE0_RX15_N
AA4	GND
AA5	HT_MCP_STOP#
AA6	HT_MCP_RXD8_P
AA7	HT_MCP_RXD10_N
AA8	HT_MCP_RXD2_P
AA9	HT_MCP_RXD3_P
AA11	HT_MCP_RXD13_P
AA13	GND
AA15	HT_MCP_TXD13_P
AA17	HT_MCP_TXD5_P
AA18	+1.2V_HTMCP
AA19	HT_MCP_TXD10_N
AA20	HT_MCP_TXD9_N
AA21	GND
AA22	GND
AA23	GND
AA24	GND
AB1	PE0_TX13_P
AB2	PE0_TX13_N

Ball	Signal Name
AB3	PE_REFCLKIN_N
AB4	GND
AB5	HT_MCP_REQ#
AB6	GND
AB7	HT_MCP_RXD1_N
AB8	HT_MCP_RXD2_N
AB9	HT_MCP_RXD3_N
AB10	GND
AB11	+1.2V_HTMCP
AB12	HT_MCP_RXD6_N
AB13	HT_MCP_RXD7_N
AB14	GND
AB15	HT_MCP_TXD6_N
AB16	HT_MCP_TXD6_P
AB17	HT_MCP_TXD5_N
AB18	HT_MCP_TXD4_P
AB19	HT_MCP_TXD10_P
AB20	HT_MCP_TXD9_P
AB21	HT_MCP_TXD8_P
AB22	HT_MCP_TXD8_N
AB23	HT_MCP_CAL_1P2V
AB24	HT_MCP_CAL_GND
AC1	PE0_TX14_P
AC2	PE0_TX14_N
AC3	PE_REFCLKIN_P
AC4	CLKIN_25MHZ
AC5	HT_MCP_RESET#
AC6	HT_MCP_RXD0_N
AC7	HT_MCP_RXD1_P
AC9	HT_MCP_RX_CLK0_N
AC10	HT_MCP_RXD4_N
AC11	HT_MCP_RXD5_N
AC12	HT_MCP_RXD6_P
AC13	HT_MCP_RXD7_P
AC14	HT_MCP_RXCTL_N
AC15	HT_MCP_TXCTL_P
AC16	HT_MCP_TXD7_P
AC18	HT_MCP_TXD4_N

Ball	Signal Name
AC19	HT_MCP_TX_CLK0_P
AC20	HT_MCP_TXD3_P
AC21	HT_MCP_TXD2_N
AC22	HT_MCP_TXD2_P
AC23	HT_MCP_TXD0_N
AC24	HT_MCP_TXD0_P
AD2	PE0_TX15_P
AD3	PE0_TX15_N
AD5	HT_MCP_PWRGD
AD6	HT_MCP_RXD0_P
AD9	HT_MCP_RX_CLK0_P
AD10	HT_MCP_RXD4_P
AD11	HT_MCP_RXD5_P
AD14	HT_MCP_RXCTL_P
AD15	HT_MCP_TXCTL_N
AD16	HT_MCP_TXD7_N
AD19	HT_MCP_TX_CLK0_N
AD20	HT_MCP_TXD3_n
AD22	HT_MCP_TXD1_N
AD23	HT_MCP_TXD1_P

Ball Listing by Package Ball

Table 26. Ball Listing by Package Ball

Signal Name	Ball
+1.2V_CORE	B5
+1.2V_CORE	C6
+1.2V_CORE	D7
+1.2V_CORE	E8
+1.2V_CORE	E9
+1.2V_CORE	E10
+1.2V_CORE	F10
+1.2V_CORE	F11
+1.2V_CORE	G11
+1.2V_CORE	H11
+1.2V_CORE	J11
+1.2V_CORE	J12
+1.2V_CORE	J13
+1.2V_CORE	J14
+1.2V_HT	K16
+1.2V_HT	M16
+1.2V_HT	R16
+1.2V_HT	M21
+1.2V_HT	J20
+1.2V_HT	T16
+1.2V_HT	U17
+1.2V_HT	C21
+1.2V_HT	H17
+1.2V_HTMCP	Y9
+1.2V_HTMCP	U11
+1.2V_HTMCP	AB11
+1.2V_HTMCP	U13
+1.2V_HTMCP	T15
+1.2V_HTMCP	U15
+1.2V_HTMCP	U16
+1.2V_HTMCP	W16
+1.2V_HTMCP	AA18
+1.2V_PEA	A3
+1.2V_PEA	B3
+1.2V_PEA	C4
+1.2V_PEA	D5

Signal Name	Ball
+1.2V_PEA	E6
+1.2V_PEA	F7
+1.2V_PEA	F8
+1.2V_PEA	F9
+1.2V_PED	B4
+1.2V_PLL	B2
+1.2V_PLL	C2
+1.2V_PLL	C3
+1.2V_PLL	D4
+1.2V_PLL	E5
+1.2V_PLL	F6
+1.2V_PLL	G7
+1.2V_PLL	G8
+1.2V_PED	C5
+1.2V_PED	D6
+1.2V_PED	E7
+1.2V_PLL	A2
+1.2V_PLL	G9
+1.2V_PLL	H10
+1.2V_PLL	J10
+1.2V_PLLCORE	P9
+1.2V_PLLGPU	R9
+1.2V_PLLHTCPU	N16
+1.2V_PLLHTMCP	T13
+1.2V_PLLIFP	H16
+1.2V_PLLPE	T11
+2.5V_CORE	C16
+2.5V_CORE	B16
+2.5V_IFPA	G15
+2.5V_IFPB	H15
+2.5V_PLLCORE	H12
+2.5V_PLLGPU	H13
+2.5V_PLLHTCPU	L16
+2.5V_PLLIFP	E16
+3.3V	C10
+3.3V	D18
+3.3V_DAC	A9

Signal Name	Ball
CLKIN_25MHZ	AC4
CLKOUT_CTERM_GND	B22
CLKOUT_PRI_200MHZ_N	B23
CLKOUT_PRI_200MHZ_P	B24
CLKOUT_SEC_200MHZ_N	B21
CLKOUT_SEC_200MHZ_P	A22
DAC_BLUE	A6
DAC_GREEN	B6
DAC_HSYNC	B7
DAC_IDUMP	C8
DAC_RED	A5
DAC_RSET	D8
DAC_VREF	D9
DAC_VSYNC	C7
GND	C1
GND	AA21
GND	AA13
GND	U14
GND	H14
GND	C11
GND	AB4
GND	AA4
GND	J15
GND	E12
GND	AB10
GND	Y18
GND	E18
GND	U18
GND	E15
GND	Y11
GND	U19
GND	N17
GND	F16

PROPRIETARY INFORMATION

Signal Name	Ball
GND	J17
GND	L13
GND	B1
GND	T17
GND	D11
GND	T12
GND	J16
GND	D19
GND	H19
GND	L21
GND	M19
GND	P19
GND	T19
GND	V19
GND	T14
GND	C20
GND	R17
GND	AB14
GND	U12
GND	G13
GND	Y16
GND	H21
GND	C22
GND	AB6
GND	F22
GND	L22
GND	R22
GND	V22
GND	AA22
GND	A23
GND	AA23
GND	AA24
GND	L11
GND	M11
GND	N11
GND	P11
GND	M12
GND	N12
GND	P12
GND	M13
GND	N13

Signal Name	Ball
GND	P13
GND	M14
GND	N14
GND	P14
GND	L14
GND	L12
HT_CPU_CAL_1P2V	W19
HT_CPU_CAL_GND	Y19
HT_CPU_PWRGD	E19
HT_CPU_REQ#	F18
HT_CPU_RESET#	D20
HT_CPU_RX_CLK0_N	T22
HT_CPU_RX_CLK0_P	T23
HT_CPU_RX_CLK1_N	R20
HT_CPU_RX_CLK1_P	R21
HT_CPU_RXCTL_N	M22
HT_CPU_RXCTL_P	M23
HT_CPU_RXD0_N	Y22
HT_CPU_RXD0_P	Y23
HT_CPU_RXD1_N	W23
HT_CPU_RXD1_P	W24
HT_CPU_RXD2_N	V23
HT_CPU_RXD2_P	V24
HT_CPU_RXD3_N	U21
HT_CPU_RXD3_P	U22
HT_CPU_RXD4_N	R23
HT_CPU_RXD4_P	R24
HT_CPU_RXD5_N	P23
HT_CPU_RXD5_P	P24
HT_CPU_RXD6_N	P21
HT_CPU_RXD6_P	P22
HT_CPU_RXD7_N	N21
HT_CPU_RXD7_P	N22
HT_CPU_RXD8_N	Y20
HT_CPU_RXD8_P	Y21
HT_CPU_RXD9_N	W20
HT_CPU_RXD9_P	V21
HT_CPU_RXD10_N	W22

Signal Name	Ball
HT_CPU_RXD10_P	W21
HT_CPU_RXD11_N	U20
HT_CPU_RXD11_P	T21
HT_CPU_RXD12_N	R19
HT_CPU_RXD12_P	R18
HT_CPU_RXD13_N	P17
HT_CPU_RXD13_P	P16
HT_CPU_RXD14_N	N19
HT_CPU_RXD14_P	N20
HT_CPU_RXD15_N	N18
HT_CPU_RXD15_P	M17
HT_CPU_STOP#	G18
HT_CPU_TX_CLK0_N	G24
HT_CPU_TX_CLK0_P	G23
HT_CPU_TX_CLK1_N	G21
HT_CPU_TX_CLK1_P	G22
HT_CPU_TXCTL_N	L24
HT_CPU_TXCTL_P	L23
HT_CPU_TXD0_N	C24
HT_CPU_TXD0_P	C23
HT_CPU_TXD1_N	D24
HT_CPU_TXD1_P	D23
HT_CPU_TXD2_N	E23
HT_CPU_TXD2_P	E22
HT_CPU_TXD3_N	F24
HT_CPU_TXD3_P	F23
HT_CPU_TXD4_N	H23
HT_CPU_TXD4_P	H22
HT_CPU_TXD5_N	J22
HT_CPU_TXD5_P	J21
HT_CPU_TXD6_N	K22
HT_CPU_TXD6_P	K21
HT_CPU_TXD7_N	K24
HT_CPU_TXD7_P	K23
HT_CPU_TXD8_N	D22
HT_CPU_TXD8_P	D21
HT_CPU_TXD9_N	E20
HT_CPU_TXD9_P	F19
HT_CPU_TXD10_N	E21
HT_CPU_TXD10_P	F21

Signal Name	Ball
HT_CPU_TXD11_N	G19
HT_CPU_TXD11_P	G20
HT_CPU_TXD12_N	J18
HT_CPU_TXD12_P	J19
HT_CPU_TXD13_N	K17
HT_CPU_TXD13_P	L17
HT_CPU_TXD14_N	K19
HT_CPU_TXD14_P	L20
HT_CPU_TXD15_N	L19
HT_CPU_TXD15_P	L18
HT_MCP_CAL_1P2V	AB23
HT_MCP_CAL_GND	AB24
HT_MCP_PWRGD	AD5
HT_MCP_REQ#	AB5
HT_MCP_RESET#	AC5
HT_MCP_RX_CLK0_N	AC9
HT_MCP_RX_CLK0_P	AD9
HT_MCP_RX_CLK1_N	T10
HT_MCP_RX_CLK1_P	U10
HT_MCP_RXCTL_N	AC14
HT_MCP_RXCTL_P	AD14
HT_MCP_RXD0_N	AC6
HT_MCP_RXD0_P	AD6
HT_MCP_RXD1_N	AB7
HT_MCP_RXD1_P	AC7
HT_MCP_RXD2_N	AB8
HT_MCP_RXD2_P	AA8
HT_MCP_RXD3_N	AB9
HT_MCP_RXD3_P	AA9
HT_MCP_RXD4_N	AC10
HT_MCP_RXD4_P	AD10
HT_MCP_RXD5_N	AC11
HT_MCP_RXD5_P	AD11
HT_MCP_RXD6_N	AB12
HT_MCP_RXD6_P	AC12
HT_MCP_RXD7_N	AB13
HT_MCP_RXD7_P	AC13
HT_MCP_RXD8_N	Y6

Signal Name	Ball
HT_MCP_RXD8_P	AA6
HT_MCP_RXD9_N	Y7
HT_MCP_RXD9_P	W7
HT_MCP_RXD10_N	AA7
HT_MCP_RXD10_P	Y8
HT_MCP_RXD11_N	W9
HT_MCP_RXD11_P	V9
HT_MCP_RXD12_N	W10
HT_MCP_RXD12_P	Y10
HT_MCP_RXD13_N	Y12
HT_MCP_RXD13_P	AA11
HT_MCP_RXD14_N	W11
HT_MCP_RXD14_P	V11
HT_MCP_RXD15_N	V13
HT_MCP_RXD15_P	W12
HT_MCP_STOP#	AA5
HT_MCP_TX_CLK0_N	AD19
HT_MCP_TX_CLK0_P	AC19
HT_MCP_TX_CLK1_N	W17
HT_MCP_TX_CLK1_P	Y17
HT_MCP_TXCTL_N	AD15
HT_MCP_TXCTL_P	AC15
HT_MCP_TXD0_N	AC23
HT_MCP_TXD0_P	AC24
HT_MCP_TXD1_N	AD22
HT_MCP_TXD1_P	AD23
HT_MCP_TXD2_N	AC21
HT_MCP_TXD2_P	AC22
HT_MCP_TXD3_N	AD20
HT_MCP_TXD3_P	AC20
HT_MCP_TXD4_N	AC18
HT_MCP_TXD4_P	AB18
HT_MCP_TXD5_N	AB17
HT_MCP_TXD5_P	AA17
HT_MCP_TXD6_N	AB15
HT_MCP_TXD6_P	AB16
HT_MCP_TXD7_N	AD16
HT_MCP_TXD7_P	AC16

Signal Name	Ball
HT_MCP_TXD8_N	AB22
HT_MCP_TXD8_P	AB21
HT_MCP_TXD9_N	AA20
HT_MCP_TXD9_P	AB20
HT_MCP_TXD10_N	AA19
HT_MCP_TXD10_P	AB19
HT_MCP_TXD11_N	V17
HT_MCP_TXD11_P	W18
HT_MCP_TXD12_N	V15
HT_MCP_TXD12_P	W15
HT_MCP_TXD13_N	Y15
HT_MCP_TXD13_P	AA15
HT_MCP_TXD14_N	W14
HT_MCP_TXD14_P	Y14
HT_MCP_TXD15_N	Y13
HT_MCP_TXD15_P	W13
JTAG_TCK	C18
JTAG_TDI	B19
JTAG_TDO	C19
JTAG_TMS	B18
JTAG_TRST#	A19
NC	F12
NC	E11
NC	E17
NC	F17
NC	G17
PE_CTERM_GND	D2
PE_GND	F3
PE_GND	L9
PE_GND	P8
PE_GND	N9
PE_GND	K4
PE_GND	N4
PE_GND	T4
PE_GND	W4
PE_GND	Y4
PE_GND	U9
PE_GND	V8
PE_GND	K6
PE_GND	M6
PE_GND	P6

Signal Name	Ball
PE_GND	T6
PE_GND	W6
PE_GND	W8
PE_GND	H8
PE_GND	K8
PE_GND	V6
PE_GND	F4
PE_GND	H9
PE_REFCLKIN_N	AB3
PE_REFCLKIN_P	AC3
PE_RESET#	G1
PE_TSTCLK_N	F2
PE_TSTCLK_P	F1
PE0_PRSNT#	D1
PE0_REFCLK_N	K2
PE0_REFCLK_P	K1
PE0_RX0_N	J7
PE0_RX0_P	J8
PE0_RX1_N	J5
PE0_RX1_P	J6
PE0_RX2_N	J9
PE0_RX2_P	K9
PE0_RX3_N	L5
PE0_RX3_P	L6
PE0_RX4_N	L8
PE0_RX4_P	L7
PE0_RX5_N	M8
PE0_RX5_P	M9
PE0_RX6_N	N7
PE0_RX6_P	N8
PE0_RX7_N	N5
PE0_RX7_P	N6
PE0_RX8_N	R5
PE0_RX8_P	R6
PE0_RX9_N	P4
PE0_RX9_P	P3
PE0_RX10_N	R7
PE0_RX10_P	R8
PE0_RX11_N	U5
PE0_RX11_P	U6
PE0_RX12_N	T9

Signal Name	Ball
PE0_RX12_P	T8
PE0_RX13_N	U8
PE0_RX13_P	U7
PE0_RX14_N	V3
PE0_RX14_P	V4
PE0_RX15_N	AA3
PE0_RX15_P	Y3
PE0_TX0_N	L2
PE0_TX0_P	L1
PE0_TX1_N	M2
PE0_TX1_P	L3
PE0_TX2_N	M3
PE0_TX2_P	L4
PE0_TX3_N	N3
PE0_TX3_P	M4
PE0_TX4_N	P2
PE0_TX4_P	P1
PE0_TX5_N	R2
PE0_TX5_P	R1
PE0_TX6_N	T2
PE0_TX6_P	R3
PE0_TX7_N	T3
PE0_TX7_P	R4
PE0_TX8_N	U3
PE0_TX8_P	U4
PE0_TX9_N	V2
PE0_TX9_P	V1
PE0_TX10_N	W2
PE0_TX10_P	W1
PE0_TX11_N	Y2
PE0_TX11_P	W3
PE0_TX12_N	AA2
PE0_TX12_P	AA1
PE0_TX13_N	AB2
PE0_TX13_P	AB1
PE0_TX14_N	AC2
PE0_TX14_P	AC1
PE0_TX15_N	AD3
PE0_TX15_P	AD2
PE1_CLKREQ#	D3
PE1_PRSNT#	E2

Signal Name	Ball
PE1_REFCLK_N	G3
PE1_REFCLK_P	G2
PE1_RX_N	H6
PE1_RX_P	G6
PE1_TX_N	G5
PE1_TX_P	G4
PKG_TEST	D17
SCLKIN_MCLKOUT_200MHZ_N	B20
SCLKIN_MCLKOUT_200MHZ_P	A20
TEST_MODE_EN	C17

Appendix B. Ballout

This appendix contains the ballout for the NVIDIA C51G.

- Ball Locations
  - Ballout (Top Left View)
  - Ballout (Top Right View)

Ballout (Top Left View)

	1	2	3	4	5	6	7	8	9	10	11	12
A		+1.2V_PLL	+1.2V_PEA		DAC_RED	DAC_BLUE			+3.3V_DAC			
B	GND	+1.2V_PLL	+1.2V_PEA	+1.2V_PED	+1.2V_CORE	DAC_GREEN	DAC_HSYNC					
C	GND	+1.2V_PLL	+1.2V_PLL	+1.2V_PEA	+1.2V_PED	+1.2V_CORE	DAC_VSYNC	DAC_IDUMP		+3.3V	GND	
D	PE0_PRSNT#	PE_CTERM_GND	PE1_CLKREQ#	+1.2V_PLL	+1.2V_PEA	+1.2V_PED	+1.2V_CORE	DAC_RSET	DAC_VREF		GND	
E		PE1_PRSNT#			+1.2V_PLL	+1.2V_PEA	+1.2V_PED	+1.2V_CORE	+1.2V_CORE	+1.2V_CORE	NC	GND
F	PE_TSTCLK_P	PE_TSTCLK_N	PE_GND	PE_GND		+1.2V_PLL	+1.2V_PEA	+1.2V_PEA	+1.2V_PEA	+1.2V_CORE	+1.2V_CORE	NC
G	PE_RESET#	PE1_REFCLK_P	PE1_REFCLK_N	PE1_TX_P	PE1_TX_N	PE1_RX_P	+1.2V_PLL	+1.2V_PLL	+1.2V_PLL		+1.2V_CORE	
H						PE1_RX_N		PE_GND	PE_GND	+1.2V_PLL	+1.2V_CORE	+2.5V_PLLCORE
J					PE0_RX1_N	PE0_RX1_P	PE0_RX0_N	PE0_RX0_P	PE0_RX2_N	+1.2V_PLL	+1.2V_CORE	+1.2V_CORE
K	PE0_REFCLK_P	PE0_REFCLK_N		PE_GND		PE_GND		PE_GND	PE0_RX2_P			
L	PE0_TX0_P	PE0_TX0_N	PE0_TX1_P	PE0_TX2_P	PE0_RX3_N	PE0_RX3_P	PE0_RX4_P	PE0_RX4_N	PE_GND		GND	GND
M		PE0_ TX1_N	PE0_TX2_N	PE0_TX3_P		PE_GND		PE0_RX5_N	PE0_RX5_P		GND	GND
N			PE0_TX3_N	PE_GND	PE0_RX7_N	PE0_RX7_P	PE0_RX6_N	PE0_RX6_P	PE_GND		GND	GND
P	PE0_TX4_P	PE0_TX4_N	PE0_RX9_P	PE0_RX9_N		PE_GND		PE_GND	+1.2V_PLLCORE		GND	GND
R	PE0_TX5_P	PE0_TX5_N	PE0_TX6_P	PE0_TX7_P	PE0_RX8_N	PE0_RX8_P	PE0_RX10_N	PE0_RX10_P	+1.2V_PLLGPU			
T		PE0_TX6_N	PE0_TX7_N	PE_GND		PE_GND		PE0_RX12_P	PE0_RX12_N	HT_MCP_RX_CLK1_N	+1.2V_PLLPE	GND
U			PE0_TX8_N	PE0_TX8_P	PE0_RX11_N	PE0_RX11_P	PE0_RX13_P	PE0_RX13_N	PE_GND	HT_MCP_RX_CLK1_P	+1.2V_HT MCP	GND
V	PE0_TX9_P	PE0_TX9_N	PE0_RX14_N	PE0_RX14_P		PE_GND		PE_GND	HT_MCP_RXD11_P		HT_MCP_RXD14_P	
W	PE0_TX10_P	PE0_TX10_N	PE0_TX11_P	PE_GND	CLKIN_200MHZ_N	PE_GND	HT_MCP_RXD9_P	PE_GND	HT_MCP_RXD11_N	HT_MCP_RXD12_N	HT_MCP_RXD14_N	HT_MCP_RXD15_P
Y		PE0_TX11_N	PE0_RX15_P	PE_GND	CLKIN_200MHZ_P	HT_MCP_RXD8_N	HT_MCP_RXD9_N	HT_MCP_RXD10_P	+1.2V_HTMCP	HT_MCP_RXD12_P	GND	HT_MCP_RXD13_N
AA	PE0_TX12_P	PE0_TX12_N	PE0_RX15_N	GND	HT_MCP_STOP#	HT_MCP_RXD8_P	HT_MCP_RXD10_N	HT_MCP_RXD2_P	HT_MCP_RXD3_P		HT_MCP_RXD13_P	
AB	PE0_TX13_P	PE0_TX13_N	PE_REFCLKIN_N	GND	HT_MCP_REQ#	GND	HT_MCP_RXD1_N	HT_MCP_RXD2_N	HT_MCP_RXD3_N	GND	+1.2V_HTMCP	HT_MCP_RXD6_N
AC	PE0_TX14_P	PE0_TX14_N	PE_REFCLKIN_P	CLKIN_25MHZ	HT_MCP_RESET#	HT_MCP_RXD0_N	HT_MCP_RXD1_P		HT_MCP_RX_CLK0_N	HT_MCP_RXD4_N	HT_MCP_RXD5_N	HT_MCP_RXD6_P
AD		PE0_TX15_P	PE0_TX15_N		HT_MCP_PWRGD	HT_MCP_RXD0_P			HT_MCP_RX_CLK0_P	HT_MCP_RXD4_P	HT_MCP_RXD5_P	
	1	2	3	4	5	6	7	8	9	10	11	12

Ballout (Top Right View)

13	14	15	16	17	18	19	20	21	22	23	24	
						JTAG_TRST#	SCLKIN_MCLKOUT_200MHZ_P		CLKOUT_SEC_200MHZ_P	GND		A
			+2.5V_CORE		JTAG_TMS	JTAG_TDI	SCLKIN_MCLKOUT_200MHZ_N	CLKOUT_SEC_200MHZ_N	CLKOUT_CTERM_GND	CLKOUT_PRI_200MHZ_N	CLKOUT_PRI_200MHZ_P	B
			+2.5V_CORE	TEST_MODE_EN	JTAG_TCK	JTAG_TDO	GND	+1.2V_HT	GND	HT_CPU_TXD0_P	HT_CPU_TXD0_N	C
				PKG_TEST	+3.3V	GND	HT_CPU_RESET#	HT_CPU_TXD8_P	HT_CPU_TXD8_N	HT_CPU_TXD1_P	HT_CPU_TXD1_N	D
		GND	+2.5V_PLLIFP	NC	GND	HT_CPU_PWRGD	HT_CPU_TXD9_N	HT_CPU_TXD10_N	HT_CPU_TXD2_P	HT_CPU_TXD2_N		E
			GND	NC	HT_CPU_REQ#	HT_CPU_TXD9_P		HT_CPU_TXD10_P	GND	HT_CPU_TXD3_P	HT_CPU_TXD3_N	F
GND		+2.5V_IFPA		NC	HT_CPU_STOP#	HT_CPU_TXD11_N	HT_CPU_TXD11_P	HT_CPU_TX_CLK1_N	HT_CPU_TX_CLK1_P	HT_CPU_TX_CLK0_P	HT_CPU_TX_CLK0_N	G
+2.5V_PLLGPU	GND	+2.5V_IFPB	+1.2V_PLLIFP	+1.2V_HT		GND		GND	HT_CPU_TXD4_P	HT_CPU_TXD4_N		H
+1.2V_CORE	+1.2V_CORE	GND	GND	GND	HT_CPU_TXD12_N	HT_CPU_TXD12_P	+1.2V_HT	HT_CPU_TXD5_P	HT_CPU_TXD5_N			J
			+1.2V_HT	HT_CPU_TXD13_N		HT_CPU_TXD14_N		HT_CPU_TXD6_P	HT_CPU_TXD6_N	HT_CPU_TXD7_P	HT_CPU_TXD7_N	K
GND	GND		+2.5V_PLLHTCPU	HT_CPU_TXD13_P	HT_CPU_TXD15_P	HT_CPU_TXD15_N	HT_CPU_TXD14_P	GND	GND	HT_CPU_TXCTL_P	HT_CPU_TXCTL_N	L
GND	GND		+1.2V_HT	HT_CPU_RXD15_P		GND		+1.2V_HT	HT_CPU_RXCTL_N	HT_CPU_RXCTL_P		M
GND	GND		+1.2V_PLLHTCPU	GND	HT_CPU_RXD15_N	HT_CPU_RXD14_N	HT_CPU_RXD14_P	HT_CPU_RXD7_N	HT_CPU_RXD7_P			N
GND	GND		HT_CPU_RXD13_P	HT_CPU_RXD13_N		GND		HT_CPU_RXD6_N	HT_CPU_RXD6_P	HT_CPU_RXD5_N	HT_CPU_RXD5_P	P
			+1.2V_HT	GND	HT_CPU_RXD12_P	HT_CPU_RXD12_N	HT_CPU_RX_CLK1_N	HT_CPU_RX_CLK1_P	GND	HT_CPU_RXD4_N	HT_CPU_RXD4_P	R
+1.2V_PLLHTMCP	GND	+1.2V_HTMCP	+1.2V_HT	GND		GND		HT_CPU_RXD11_P	HT_CPU_RX_CLK0_N	HT_CPU_RX_CLK0_P		T
+1.2V_HTMCP	GND	+1.2V_HTMCP	+1.2V_HTMCP	+1.2V_HT	GND	GND	HT_CPU_RXD11_N	HT_CPU_RXD3_N	HT_CPU_RXD3_P			U
HT_MCP_RXD15_N		HT_MCP_TXD12_N		HT_MCP_TXD11_N		GND		HT_CPU_RXD9_P	GND	HT_CPU_RXD2_N	HT_CPU_RXD2_P	V
HT_MCP_TXD15_P	HT_MCP_TXD14_N	HT_MCP_TXD12_P	+1.2V_HTMCP	HT_MCP_TX_CLK1_N	HT_MCP_TXD11_P	HT_CPU_CAL_1P2V	HT_CPU_RXD9_N	HT_CPU_RXD10_P	HT_CPU_RXD10_N	HT_CPU_RXD1_N	HT_CPU_RXD1_P	W
HT_MCP_TXD15_N	HT_MCP_TXD14_P	HT_MCP_TXD13_N	GND	HT_MCP_TX_CLK1_P	GND	HT_CPU_CAL_GND	HT_CPU_RXD8_N	HT_CPU_RXD8_P	HT_CPU_RXD0_N	HT_CPU_RXD0_P		Y
GND		HT_MCP_TXD13_P		HT_MCP_TXD5_P	+1.2V_HTMCP	HT_MCP_TXD10_N	HT_MCP_TXD9_N	GND	GND	GND	GND	AA
HT_MCP_RXD7_N	GND	HT_MCP_TXD6_N	HT_MCP_TXD6_P	HT_MCP_TXD5_N	HT_MCP_TXD4_P	HT_MCP_TXD10_P	HT_MCP_TXD9_P	HT_MCP_TXD8_P	HT_MCP_TXD8_N	HT_MCP_CAL_1P2V	HT_MCP_CAL_GND	AB
HT_MCP_RXD7_P	HT_MCP_RXCTL_N	HT_MCP_TXCTL_P	HT_MCP_TXD7_P		HT_MCP_TXD4_N	HT_MCP_TX_CLK0_P	HT_MCP_TXD3_P	HT_MCP_TXD2_N	HT_MCP_TXD2_P	HT_MCP_TXD0_N	HT_MCP_TXD0_P	AC
	HT_MCP_RXCTL_P	HT_MCP_TXCTL_N	HT_MCP_TXD7_N			HT_MCP_TX_CLK0_N	HT_MCP_TXD3_N		HT_MCP_TXD1_N	HT_MCP_TXD1_P		AD
13	14	15	16	17	18	19	20	21	22	23	24	