Product Brief

FW643

PCI Express® 1394b PHY/Link Open Host Controller Interface

FEATURES

Core

- Single-chip link and PHY enables smaller, simpler, more efficient mother board, and add-in card designs, thereby lowering overall system cost.
- Leverages proven 1394b-2002 PHY core design.
- Demonstrated compatibility with current Microsoft® Windows® , MacOS®, Linux® drivers, and common applications.
- Demonstrated interoperability with existing, as well as older, 1394-1995 and 1394a consumer electronics and peripherals products.
- Supports low-power system designs with 579 mW typical power dissipation and extensive power management features.
- Single external 24.576 MHz crystal (or crystal oscillator for TI® compatibility) for high-speed 1394 clock generation.
- Small, 7 mm x 7 mm form factor 127-Ball VTFSBGA package. (0.5 mm pitch).
- 11 mm x 11 mm form factor 139-Ball FSBGA package. (0.8 mm pitch).
- Optional register configuration through a serial EEPROM interface or back-door BIOS access. Default configuration does not require external EEPROM.
- Fabricated in cost-effective 0.13 µm technology with a single 3.3 V power supply requirement.
- Scan, BIST, and NAND-tree-based design for testability (DFT) support.

PCI Express

- Fully compliant with revision 1.1 base specification.
- Multiple virtual channel (VC0, VC1) support for differentiating 1394 isochronous traffic.
- Supports eight user-programmable traffic classes.
- 64-bit and 32-bit platform support.
- Interrupts via legacy INTx interface or message signaled interrupt (MSI).
- Supports PCI Express clock power management via CLKREQN signal for form factors that support this protocol.
- Supports all link power management states (L0, L0s, L1, and L2/L3) and active state power management (ASPM).
- Supports wake-up from a low-power state via in-band beacon signaling and side-band WAKE_N signal.

The LSI FW643 device is specifically designed for compliance with PCI Express technology. It combines an OHCI (open host controller interface) with LSI's TrueFIRE™ technology and a high-performance, standards-compliant PCI Express 1.1 host system inter-face to provide S800 1394b-2002 compliant throughput in a small footprint and low power dissipation.

Multiple VCs (virtual channels) on the PCI Express link provide native support for QoS (quality of service) transmission for real-time and multimedia applications in a standards-based framework, ensuring compatibility with current and future operating systems. Active-state power management allows dynamic power management during periods of reduced network activity.

The FW643 is comprised of the following major functional sections:

- PCI Express subsystem, consisting of PHY, link, and transport layers.
- OHCI core with isochronous and asynchronous DMA engines.
- 1394b link core.
- 1394b PHY core with three bilingual 1394b ports.

OHCI (Open Host Controller Interface)

- Enhanced with the OHCI 1.2 draft specification for 1394b-2002 PHY full operational compliance.
- OHCI 1.0 backwards compatible. Configurable via EEPROM to operate in either OHCI 1.0 or OHCI 1.1 mode.
- 8 Kbyte isochronous transmit FIFO.
- 4 Kbyte asynchronous transmit FIFO.
- 8 Kbyte isochronous receive FIFO.
- 8 Kbyte asynchronous receive FIFO.
- Dedicated asynchronous and isochronous descriptorbased DMA engines.
- Eight isochronous transmit contexts.
- Eight isochronous receive contexts.
- Supports parallel processing of incoming physical read and write requests.
- Supports up to 48-bit addressing per OHCI specification for the physical DMA transfers.

1394b-2002 Link

- CycleCycle master and isochronous resource manager capable.
- Supports 1394a-2000 and 1394b-2002 acceleration features.

1394b-2002 PHY

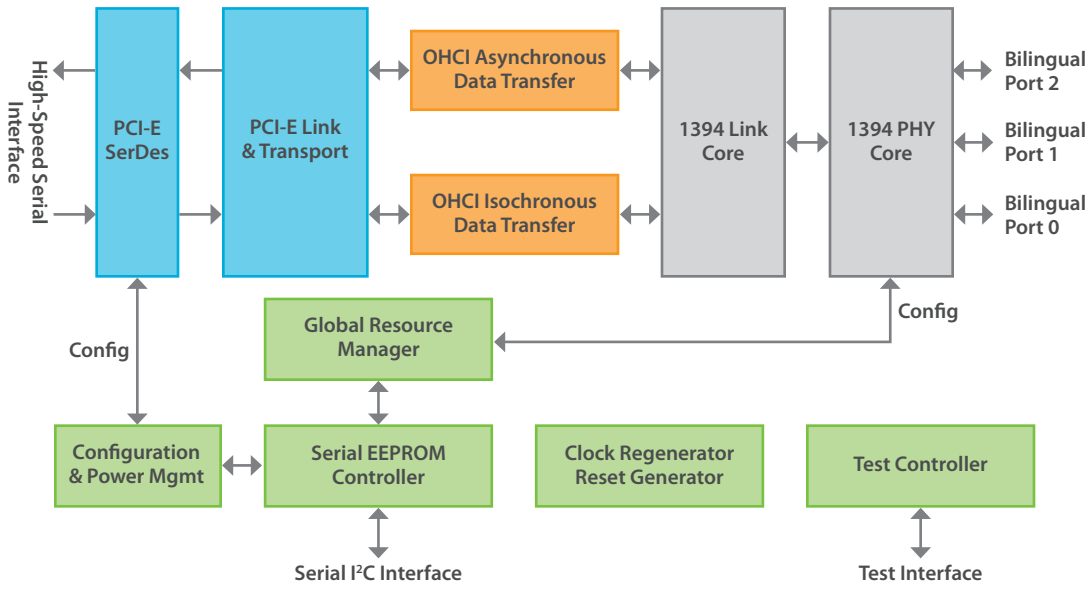
- Provides three IEEE® 1394b-2002 compliant ports supporting 1394b-2002 speeds of 800 Mbits/s and 400 Mbits/s while maintaining backward compatibility to IEEE 1394a-2000 speeds of 100 Mbits/s, 200 Mbits/s, and 400 Mbits/s over 4.5 m copper.
- Fully supports provisions of IEEE 1394a-2000 and 1394-1995 standards for high-performance serial bus.
- Link is not required for hub operation.
- Supports extended BIAS_HANDSHAKE time for enhanced interoperability with camcorders.
- Does not require external filter capacitor for PLL.
- Supports arbitrated short bus reset to improve utilization of the bus.
- Supports ack-accelerated arbitration and fly-by concatenation.
- Supports PHY pinging and remote PHY access packets.
- Fully supports suspend/resume.

Reports cable power fail interrupt when voltage at CPS ball falls below 7.5 V.

ORDERING INFORMATION

Device Code	Comcode
L-FW643-06-DB	711017885
L-FW643-06-BP-DB	711017886

Functional Block Diagram



For more information and sales office locations, please visit the LSI web sites at: lsi.com lsi.com/contacts

January 2007
PB07-022CMPR-2