

LMC1982

Digitally-Controlled Stereo Tone and Volume Circuit with Two Selectable Stereo Inputs

General Description

The LMC1982 is a monolithic integrated circuit that provides volume, balance, tone (bass and treble), enhanced stereo, and loudness controls and selection between two pairs of stereo inputs. These functions are digitally controlled through a three-wire communication interface. There are two digital inputs for easy interface to other audio peripherals such as stereo decoders. The LMC1982 is designed for line level input signals (300 mV–2V) and has a maximum gain of –0.5 dB. Volume is set at minimum and tone controls are flat when supply voltage is first applied.

Low noise and distortion result from using analog switches and poly-silicon resistor networks in the signal path.

Additional tone control can be achieved using the LMC835 stereo 7-band graphic equalizer connected to the LMC1982's SELECT OUT/SELECT IN external processor loop.

Features

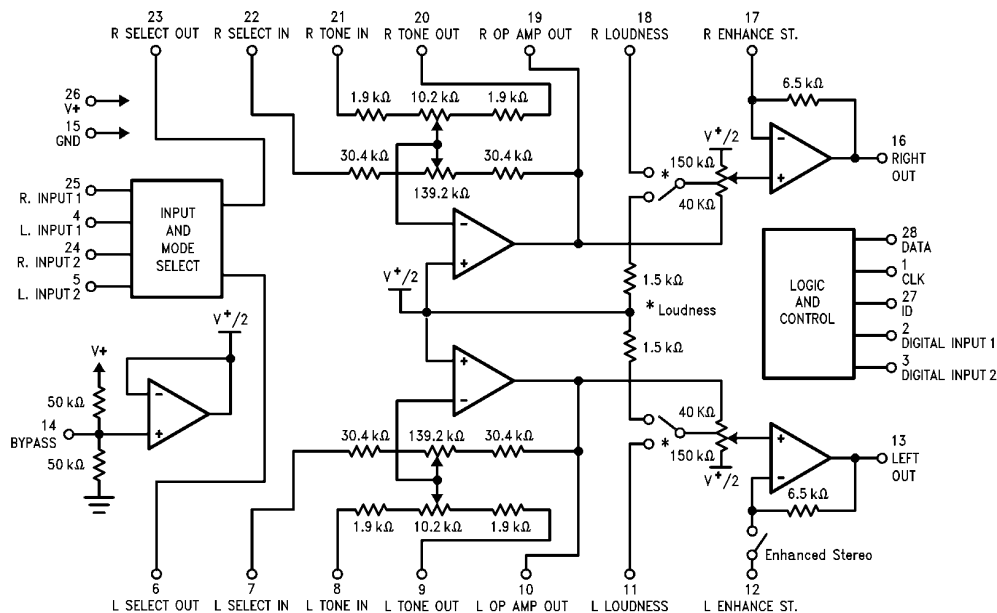
- Low noise and distortion
- Two pairs of stereo inputs

- Enhanced stereo function
- Loudness compensation
- 40 position 2 dB/step volume attenuator plus mute
- Independent left and right volume controls
- Low noise-suitable for use with DNR® and Dolby® noise reduction
- External processor loop
- Signal handling suitable for compact discs
- Pop-free switching
- Serially programmable: INTERMETAL bus (IM) interface
- 6V to 12V single supply operation
- 28 Pin DIP or PLCC package

Applications

- Stereo television
- Music reproduction systems
- Sound reinforcement systems
- Electronic music (MIDI)
- Personal computer audio control

Block and Connection Diagrams



DNR® is a registered trademark of National Semiconductor Corporation.
Dolby® is a registered trademark of Dolby Labs.

TL/H/11028-1

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - GND$)	15V
Voltage at any Pin	$GND - 0.2V$ to $V^+ + 0.2V$
Input Current at any Pin (Note 3)	5 mA
Package Input Current (Note 3)	20 mA
Power Dissipation (Note 4)	500 mW
Junction Temperature	+ 125°C

Storage Temperature	-65°C to + 150°C
Lead Temperature	
N Package, (Soldering, 10 Seconds)	+ 260°C
V Package, (Vapor Phase, 60 Seconds)	215°C
Infrared, (15 Seconds)	220°C
ESD Susceptability (Note 5)	2 kV

Operating Ratings (Notes 1 and 2)

Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$
LMC1982CIN, LMC1982CIV	-40°C $\leq T_A \leq$ +85°C
Supply Voltage Range ($V^+ - V^-$)	6V to 12V

Electrical Characteristics The following specifications apply for $V^+ = 9V$, $f_{IN} = 1$ kHz, input signal (300 mV) applied to INPUT 1, volume = 0 dB, bass = 0 dB, treble = 0 dB, enhanced stereo is off, and loudness is off unless otherwise specified. All limits apply for $T_A = T_J = +25^\circ C$.

Symbol	Parameter	Conditions	Typical (Note 6)	Limit (Note 7)	Unit (Limit)
I_S	Supply Current		15	25	mA (max)
V_{IN}	Input Voltage	Clipping Level (1.0% THD), Select Out (Pins 6, 23)	2.3	2.0	V_{rms} (min)
THD	Total Harmonic Distortion	Left and Right channels; Output Pins 13, 16 $V_{IN} = 0.3 V_{rms}$; $f_{IN} = 100$ Hz, 1 kHz, 10 kHz	0.008	0.1	% (max)
		$V_{IN} = 2.0 V_{rms}$; $f_{IN} = 100$ Hz, 1 kHz	0.4	1.0	% (max)
		$V_{IN} = 2.0 V_{rms}$; $f_{IN} = 10$ kHz	0.5	1.0	% (max)
		$V_{IN} = 0.5 V_{rms}$; Bass and Treble Tone Controls Set at Maximum	0.07	0.5	% (max)
		$V_{IN} = 0.3 V_{rms}$; Volume Attenuator at -20 dB, Bass and Treble Tone Controls Set at Maximum	0.06	0.15	% (max)
	DC Shifts	$V_{IN} = 0.3 V_{rms}$; Between Any Two Adjacent Control Settings	2.0	4.0	mV (max)
		$V_{IN} = 0.3 V_{rms}$; All Mode and Input Positions	18	20	mV (max)
R_{OUT}	AC Output Impedance	Pins 6, 23, (470 Ω to Ground at Input)	150	200	Ω (max)
		Pins 13, 16	26	40	Ω (max)
R_{IN}	AC Input Impedance	Pins 4, 5, 24, 25	50	72	k Ω (max)
				35	k Ω (min)
	Volume Attenuator Range	Pins 13, 16; Volume Attenuation at 0100010XXX000000 (0 dB) 0100010XXX101XXX (80 dB); (Relative to Attenuation at the 0 dB Setting)	0.5	1.5	dB (max)
			80	78	dB (min)
				82	dB (max)
	Volume Step Size	All Volume Attenuation Settings from 0100010XXX101XXX (80 dB) to 0100010XXX000000 (0 dB) (Note 9)	2.0	1.5	dB (min)
				2.5	dB (min)
	Channel-to-Channel Volume Tracking Error	All Volume Attenuation Settings from 0100010XXX101XXX (80 dB) to 0100010XXX000000 (0 dB)	± 0.1	± 1.5	dB (min)
	Mute Attenuation	$V_{IN} = 1.0 V_{rms}$	105	86	dB (max)

Electrical Characteristics The following specifications apply for $V^+ = 9V$, $f_{IN} = 1\text{ kHz}$, input signal (300 mV) applied to INPUT 1, volume = 0 dB, bass = 0 dB, treble = 0 dB, enhanced stereo is off, and loudness is off unless otherwise specified. All limits apply for $T_A = T_J = +25^\circ\text{C}$. (Continued)

Symbol	Parameter	Conditions	Typical (Note 6)	Limit (Note 7)	Unit (Limit)
	Bass Gain Range	$f_{IN} = 100\text{ Hz}$, Pins 13, 16	± 12	± 10.0 ± 14.0	dB (min) dB (max)
	Bass Tracking Error	$f_{IN} = 100\text{ Hz}$, Pins 13, 16	± 0.1	± 1.5	dB (max)
	Bass Step Size	$f_{IN} = 100\text{ Hz}$, Pins 13, 16 (Relative to Previous Level)	2.0	1.5 2.5	dB (min) dB (max)
	Treble Gain Range	$f_{IN} = 10\text{ kHz}$, Pins 13, 16	± 12	± 10.0 ± 14.0	dB (min) dB (max)
	Treble Tracking Error	$f_{IN} = 10\text{ kHz}$, Pins 13, 16	± 0.1	± 1.5	dB (max)
	Treble Step Size	$f_{IN} = 10\text{ kHz}$, Pins 13, 16 (Relative to Previous Level)	2.0	1.5 2.5	dB (min) dB (max)
	Enhanced Stereo Cross Coupling	(Note 10)	-4.4	-2.5 -6.9	dB (min) dB (max)
	Frequency Response	V_{IN} Applied to Input 1 and Input 2; $f_{IN} = 20\text{ Hz} - 20\text{ kHz}$ (Relative to Signal Amplitude at 1 kHz)	± 0.1	± 1.0	dB (max)
	Loudness	Volume Attenuator = 40 dB, Loudness on (See Figure 5) Gain at 100 Hz (Referenced to Gain at 1 kHz) Gain at 10 kHz (Referenced to Gain at 1 kHz)	11.5 6.5	13.5 9.5 8.5 4.5	dB (max) dB (min) dB (max) dB (min)
	Signal-to-Noise Ratio	$V_{IN} = 1.0 V_{rms}$, A Weighted, Measured at 1 kHz, $R_S = 470\Omega$	95	90	dB (min)
	Channel Balance	All Volume Settings	0.2	1.0	dB (max)
	Channel Separation	Input Pins 4, 25: Output Pins 13, 16; $V_{IN} = 1.0 V_{rms}$ (Note 8)	80	60	dB (min)
	Input-Input Isolation	470Ω to AC Ground on Unused Input	95	60	dB (min)
PSSR	Power Supply Rejection Ratio	$V^+ = 9 V_{DC}$; $200 mV_{rms}$, 100 Hz Sinewave Applied to Pin 26	32	28	dB (min)
f_{CLK}	Clock Frequency		5.0	1.0	MHz (max)
$V_{IN(1)}$	Logic "1" Input Voltage	Pins 1, 27, 28 (IM Bus) Pins 2, 3	1.3 2.9	2.0 5.5	V (min) V (min)
$V_{IN(0)}$	Logic "0" Input Voltage	Pins 1, 27, 28 (IM Bus) Pins 2, 3	0.4 1.2	0.8 3.5	V (max) V (max)
$V_{OUT(1)}$	Logic "1" Output Voltage	Pin 28 (IM Bus)		2.0	V (min)
$V_{OUT(0)}$	Logic "0" Output Voltage	Pin 28 (IM Bus)	0.4	0.8	V (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are specified with respect to ground.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply voltages ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of the current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply voltages with 5 mA current limit to four.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} , θ_{JA} , and the ambient temperature T_A . The maximum allowable power dissipation is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LMC1982CIN, $T_{JMAX} = +125^\circ\text{C}$, and the typical junction-to-ambient thermal resistance, when board mounted, is 67°C/W .

Note 5: Human body model; 100 pF discharged through a 1.5 k Ω resistor.

Note 6: Typical values are at $T_J = +25^\circ\text{C}$ and represent the most likely parametric norm.

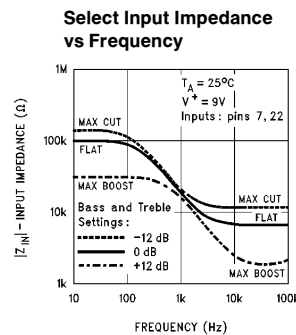
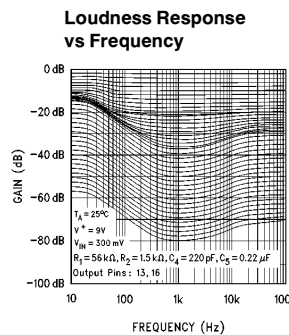
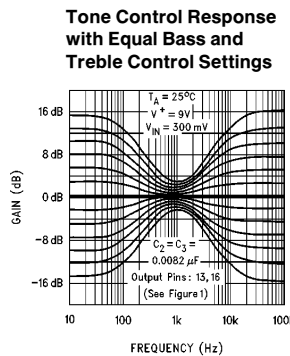
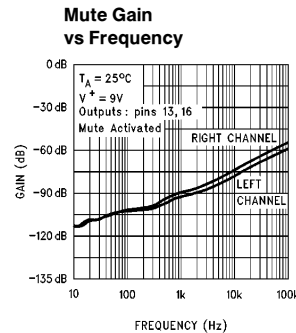
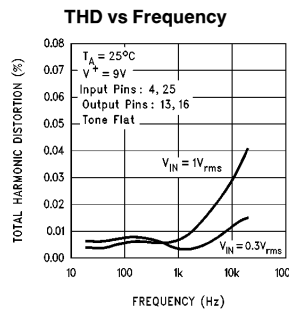
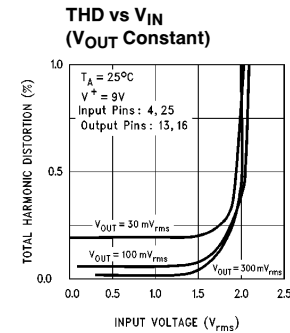
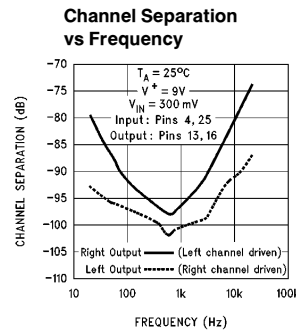
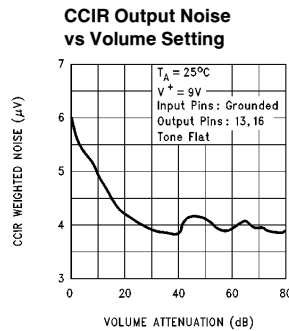
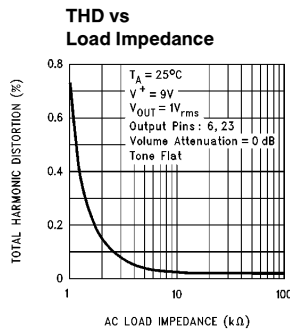
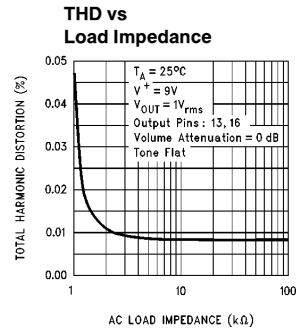
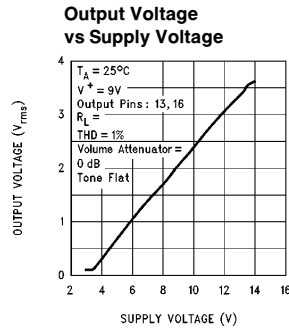
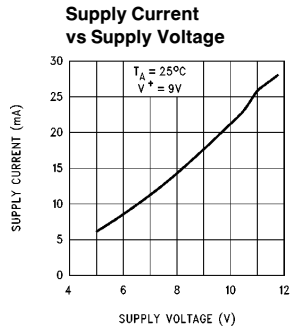
Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: The Input-Input Isolation is tested by driving one input and measuring the output when the undriven input are selected.

Note 9: The Volume Step Size is defined as the change in attenuation between any two adjacent volume attenuation settings. The nominal Volume Step Size is 2 dB.

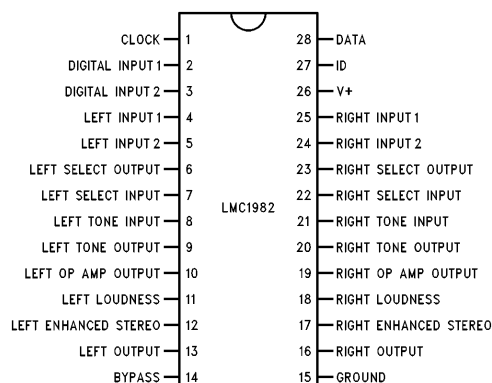
Note 10: Enhanced Stereo Cross Coupling is a measure of the ratio between the undriven right channel output signal and the driven left channel output signal. It is measured by driving the left inputs with a 300 mV $_{rms}$ signal while the right inputs are grounded.

Typical Performance Characteristics



TL/H/11028-3

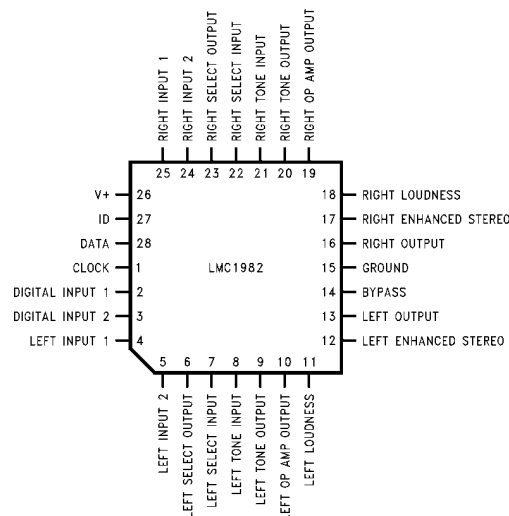
Connection Diagram



TL/H/11028-2

Top View

Order Number LMC1982CIN
See NS Package Number N28B



TL/H/11028-12

Top View

Order Number LMC1982CIV
See NS Package Number V28A

Pin Description

CLK (1)	The INTERMETAL (IM) Bus clock is applied to the CLOCK pin. This input accepts a TTL or CMOS level signal. The input is used to clock the DATA signal. A data bit must be valid on the rising clock edge.	TONE OUT (9, 20)	Tone control amplifier output. See the Application Information section titled "Tone Control Response".
DIGITAL INPUT 1 & 2 (2, 3)	Internally tied high to V^+ through a 30 k Ω pull-up resistor, these inputs allow a peripheral device to place any single-bit, active low digital information onto the IM Bus. It is then sent out to the controlling device through the DATA pin. Examples of such information could include indication of the presence of a Second Audio Program (SAP) or an FM stereo carrier.	OP AMP OUT (10, 19)	These outputs are used with external tone control capacitors. Internally, this output is applied to the volume attenuators.
INPUTS 1 & 2 (4, 25; 5, 24)	These are the LMC1982's two stereo input pairs.	LOUDNESS (11, 18)	The output signal on these pins is a voltage taken from the volume attenuator's -40 dB tap point. An external R-C network is connected to these pins.
SELECT OUT (6, 23)	The selected INPUT signal is available at this output. This feature allows external signal processors such as noise reduction or graphic equalizers to be used. This output can typically sink 1 mA. These pins should be capacitively coupled to pins 7 and 22, respectively, if no external processor is used.	ENHANCED STEREO (12, 17)	An external R-C network is connected across these pins. This provides left-right channel cross-coupling and cancellation to create an enhanced stereo channel separation effect.
SELECT IN (7, 22)	These are the inputs that an external signal processor uses to return a signal to the LMC1982. These pins should be capacitively coupled to pins 6 and 23, respectively, if no external processor is used.	MAIN OUTPUT (13, 16)	The output signal from these pins drives a stereo power amplifier. The output can typically sink 1 mA.
TONE IN (8, 21)	These are the inputs to the tone control amplifier. See the Application Information section titled "Tone Control Response".	BYPASS (14)	A 10 μ F capacitor is connected between this pin and ground to provide an AC ground for the internal half-supply voltage reference.
		GROUND (15)	This pin is connected to analog ground.
		V^+ (26)	This is the power supply connection. The LMC1982 is operational with supply voltages from 6V to 12V. This pin should be bypassed to ground through a 1.0 μ F capacitor.

Pin Description (Continued)

ID (27)

This is the IDENTITY digital input that, when low, signals the LMC1982 to receive, from a controlling device, a device address (40_H–47_H), present on the DATA line.

DATA (28)

This is the serial data input for communications sent by a controller. The controller must have open drain outputs used with external pull-up resistors. The data rate has a maximum frequency of 1 MHz. The LMC1982 requires 16 bits of data to control or change a function: the first 8 bits select the LMC1982 and one of eight functions. The final eight bits set the function to a desired value. The data must be valid on the rising edge of the CLOCK input signal.

TABLE I. IM Bus Programming Codes for LMC1982

Address (A7–A0)	Function	Data	Function Selected
01000000	Input Select + Mute	XXXXXX00 XXXXXX01 XXXXXX10 XXXXXX11	INPUT1 INPUT2 N/A MUTE
01000001	Loudness, Enhanced Stereo	XXXXXX00 XXXXXX01 XXXXXX10 XXXXXX11	Loudness OFF Enhanced Stereo OFF Loudness ON Enhanced Stereo OFF Loudness OFF Enhanced Stereo ON Loudness ON Enhanced Stereo ON
01000010	Bass	XXXX0000 XXXX0011 XXXX0110 XXXX1001 XXXX11XX	– 12 dB – 6 dB FLAT + 6 dB + 12 dB
01000011	Treble	XXXX0000 XXXX0011 XXXX0110 XXXX1001 XXXX11XX	– 12 dB – 6 dB FLAT + 6 dB + 12 dB
01000100	Left Volume	XX000000 XX010100 XX101XXX XX11XXXX	0 dB – 40 dB – 80 dB – 80 dB
01000101	Right Volume	XX000000 XX010100 XX101XXX XX11XXXX	0 dB – 40 dB – 80 dB – 80 dB
01000110	Mode Select	XXXXXX100 XXXXXX101 XXXXXX11X	Left Mono Stereo Right Mono
01000111	Read Digital Input 1 or Digital Input 2 on IM Bus	XXXXXXD1D0	D0 = Digital Input 1 D1 = Digital Input 2

General Information

The LMC1982 is a CMOS/bipolar building block intended for high fidelity audio signal processing. It is designed for line level inputs signals (300 mV – 2V) and has a maximum gain of –0.5 dB. While the LMC1982 is manufactured with CMOS processing, NPN transistors are used to build low noise op amps. The combination of CMOS switches, bipolar op amps, and poly-silicon resistors make it possible to achieve an order of magnitude quality improvement over other bipolar circuits that use analog multipliers to accomplish gain adjustment. Internal circuits set the volume to minimum, tone controls to flat, the mute to on, and all other functions off when power is first applied. Individual left and right volume controls are software programmed to achieve

the stereo balance function. *Figure 1* shows the connection diagram of a typical LMC1982 application.

The LMC1982 has internal decoding logic that allows a microprocessor (μ P) or microcontroller (μ C) to communicate directly to the audio control circuitry through an INTERMET-AL (IM) Bus interface. This three-wire interface consists of a bi-directional DATA line, a Clock (CLK) input line, and an Identity (ID) line. Address and function selection data (8 bits) are serially shifted from the controller to the LMC1982. This is followed by 8 bits of function value data. Data present in the internal shift register is latched and the instruction is executed.

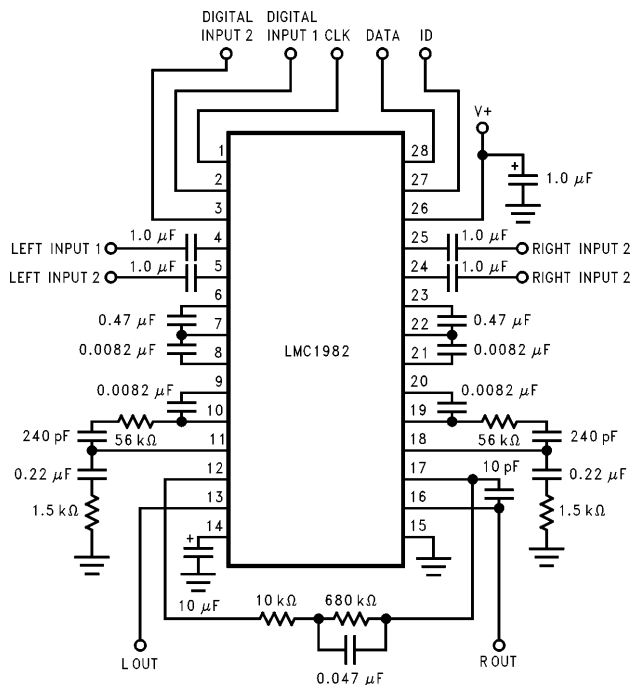


FIGURE 1. Typical Application

TL/H/11028-5

Application Information

INPUT SELECTOR

The LMC1982's input selector and mode control are shown in *Figure 2*. The input selector selects one of two stereo signal sources or a mute function with typical attenuation of 100 dB. The selected signals are then sent to a mode control matrix. As shown in Table 1, the matrix provides normal stereo or can direct either channel to both LEFT or RIGHT SELECT OUTPUTs. The third matrix mode is normal stereo. The control matrix output is buffered and appears on each channel's respective SELECT OUT pin (6, 23). Switching noise is kept to a minimum when mute is selected by using a 50 k Ω bias resistor.

Noise performance is optimized through the use of emitter followers in the mode control matrix's output. Internal 50 k Ω resistors are connected to each input selector pin to provide the proper bias point for the emitter follower buffers. Each internal 50 k Ω bias resistor is connected to a common half-supply ($V^+/2$) source. This produces a voltage at pins 6 and 23 (SELECT OUT) that is 1.4V below $V^+/2$ (typically 3.1V with $V^+ = 9V$). Since a DC voltage is present at the input pins (4, 5, 24, and 25), input signal should be AC coupled through a 1 μF capacitor.

The output signal at pins 6 and 23 can be used to drive external audio processing circuits such as noise reduction (LM1894–DNR or Dolby) or graphic equalizers (LMC835). It is important that if any noise reduction is used it be placed ahead of any tone controls or equalizers in the external circuit path to preserve the frequency spectrum of the selected input signal. Otherwise, any frequency equalization could prevent the proper operation of the noise reduction circuit. If no external processor is used, a capacitor should be used to

couple the SELECT OUT signals directly to pins 7 and 22, respectively.

MINIMUM LOAD IMPEDANCE

The LMC1982 employs emitter-followers to buffer the selected stereo channels. The buffered signals are available at pins 6 and 23 (SELECT OUT). The SELECT OUT buffers operate with a typical bias current 1 mA.

The Electrical Specifications table lists a maximum input signal of 2.0 V_{rms} (2.5 V_{peak}) for 1% THD at the SELECT OUT pins. This distortion level is achieved when the minimum AC load impedance seen by the SELECT OUT pins is 2.5 k Ω (2.5V/1 mA). Using lower load impedances results in clipping at lower output levels. If the load impedance is DC-coupled, an increased quiescent current can flow. Latch-up may occur if the total emitter current exceeds 5 mA. Thus, maximum output voltage can be increased and much lower distortion levels can be achieved using load impedances of at least 25 k Ω .

INPUT IMPEDANCE

The input impedance of pins 4, 5, 24 and 25 is defined by internal bias resistors and is typically 50 k Ω .

The SELECT IN pins have an input impedance that varies with the BASE and TREBLE control settings. The input impedance is 100 k Ω at DC and 19 k Ω at 1 kHz when the controls are set at 0 dB. Minimum input impedance of 30.4 k Ω at DC and 16 k Ω at 1 kHz occurs when maximum boost is selected. At 10 kHz the minimum input impedance, with the tone controls flat, is 6.8 k Ω and, with the tone controls at maximum boost, is 2.5 k Ω .

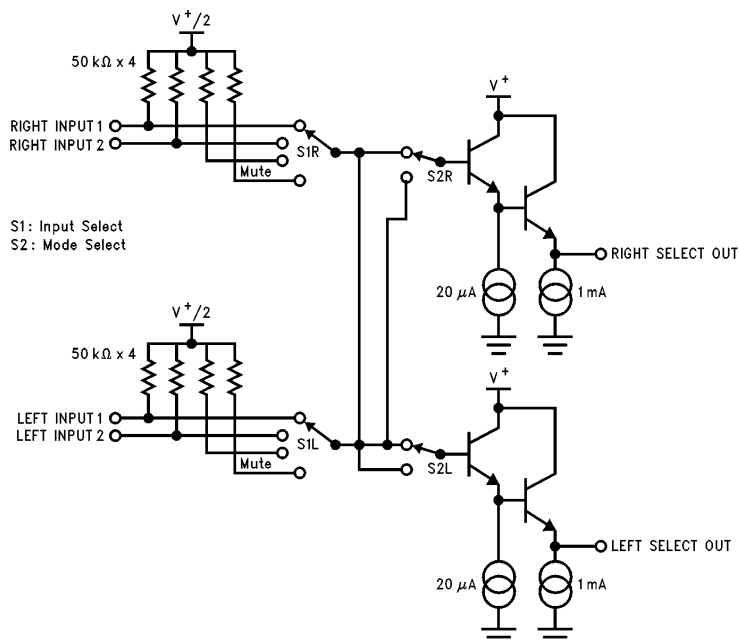


FIGURE 2. Input and Mode Select Circuitry

TL/H/11028-6

Application Information (Continued)

EXTERNAL SIGNAL PROCESSING

The SELECT OUT pins (6 and 23) enable greater system design flexibility by providing a means to implement an external processing loop. This loop can be used for noise reduction circuits such as DNR (LM1894) or multi-band graphic equalizers (LMC835). If both are used, it is important to ensure that the noise reduction circuitry precede the equalization circuits. Failure to do so results in improper operation of the noise reduction circuits. The system shown in *Figure 3* utilizes the external loop to include DNR and a multi-band equalizer.

tone control response

Bass and treble tone controls are included in the LMC1982. The tone controls used just two external capacitors for each stereo channel. Each has a corner frequency determined by the value of C2 and C3 (see *Figure 4*) and internal resistors in the feedback loop of the internal tone amplifier. The maximum-boost or cut is determined by the data sent to the LMC1982 (see Table I).

The typical tone control response shown in Typical Performance Curves were generated with $C2 = C3 = 0.0082 \mu\text{F}$ and show the response for each step. When modifying the tone control response it is important to note that the ratio of C3 and C2 sets the mid-frequency gain. Symmetrical tone

response is achieved when $C2 = C3$. However, with $C2 = 2(C3)$ and the tone controls set to "flat", the frequency response will be flat at 20 Hz and 20 kHz, and +6 dB at 1 kHz.

The frequency where a tone control begins to deviate from a flat response is referred to as the turn-over frequency. With $C = C2 = C3$, the LMC1982's treble turn-over frequency is nominally

$$f_{TT} = \frac{1}{2\pi C(14 \text{ k}\Omega)}$$

The bass turn-over frequency is nominally

$$f_{BT} = \frac{1}{2\pi C(30.4 \text{ k}\Omega)}$$

when maximum boost is chosen. The inflection points (the frequencies where the boost or cut is within 3 dB of the final value) are for treble and bass

$$f_{TI} = \frac{1}{2\pi C(1.9 \text{ k}\Omega)}$$

$$f_{BI} = \frac{1}{2\pi C(169.6 \text{ k}\Omega)}$$

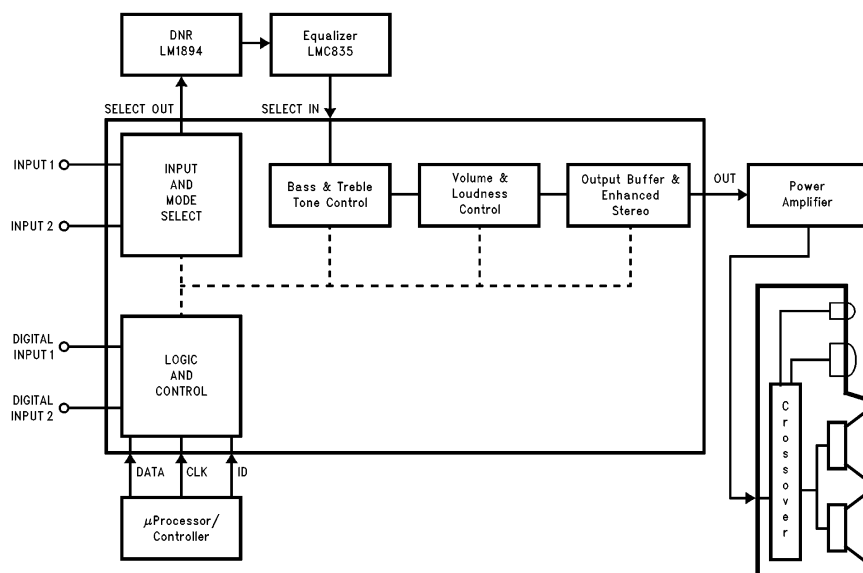


FIGURE 3. System Block Diagram Utilizing the External Processing Loop (One Channel Shown)

TL/H/11028-7

Application Information (Continued)

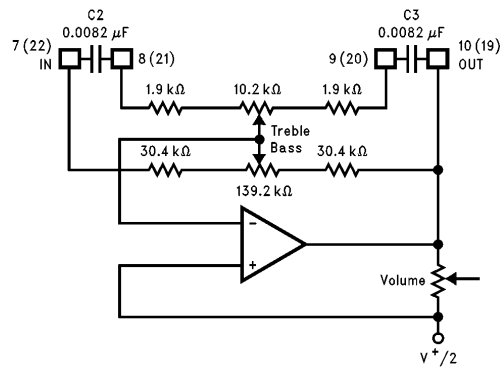


FIGURE 4. The Tone Control Amplifier

Increasing the values of C2 and C3 decreases the turnover and inflection frequencies: i.e., the Tone Control Response Curves shown in Typical Performance Curves will shift left when C2 and C3 are increased and shift right when C2 and C3 are decreased. With C2 = C3 = 0.0082 μF, 2 dB steps are achieved at 100 Hz and 10 kHz. Changing C2 and C3 to 0.01 μF shifts the 2 dB per step frequency to 72 Hz and 8.3 kHz. If the tone control capacitors size is decreased these frequencies will increase. With C2 = C3 = 0.0068 μF the 2 dB steps take place at 130 Hz and 11.2 kHz.

LOUDNESS

The human ear has less sensitivity to high and low frequencies relative to its sensitivity to mid-range frequencies between 2 kHz and 6 kHz for any given acoustic level. The low and high frequency sensitivity decreases faster than the sensitivity to the mid-range frequencies as the acoustic level drops. The LMC1982's loudness function can be used to help compensate for the decreased sensitivity by boosting the gain at low and high frequencies as the volume control attenuation increases (see the curve labeled "Gain vs Frequency with Loudness Active").

The LMC1982's loudness function uses external components R1, R2, C4 and C5, as shown in Figure 5, to select the frequencies where bass and treble boost begin. The amount of boost is dependent on the volume attenuator's setting. The loudness characteristic, with the volume attenuator set at 40 dB, has a transfer function of

$$\frac{V_O}{V_I} = \frac{(sC5R2 + 1)(sC4(R1 + 156k) + 1)}{(s^2)C4C5R2(163k) + s[C4(156k) + C5(4.9R2 + 156k)] + 1}$$

The external components R1 and C4 can be eliminated and pin 10(19) left open if bass boost is the only desired loudness characteristic.

As shown in Table I, loudness and enhanced stereo are controlled through the same address. It is important to remember to set both functions to the correct value any time either of these functions is updated.

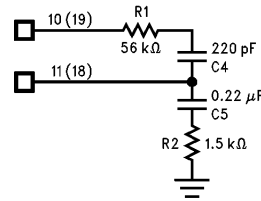


FIGURE 5. Loudness Control Circuit

ENHANCED STEREO

The LMC1982 has an enhanced stereo effect that can be achieved by cross-coupling reverse phase information between the left and right stereo channels. This feature can help improve the apparent stereo channel separation when, because of cabinet or equipment limitations, the left and right speakers are closer to each other than optimum.

Enhanced stereo is created by connecting an external frequency shaping RC network between the OUTPUT operational amplifiers' inverting inputs through an internal CMOS switch (see Figure 6). The external network couples 60% of each channel's output to the opposite channel's inverting input. This cancels a portion of the signal common to both channels.

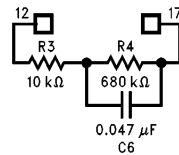


FIGURE 6. Enhanced Stereo Circuit

The desired 60% cross-coupling is accomplished through the internal 6.5 kΩ feedback resistor and an external 10 kΩ resistor. Bass frequency cancellation is prevented by using a 0.047 μF coupling capacitor to couple only frequencies above 330 Hz. Switching noise is eliminated by using a 680 kΩ resistor across the 0.047 μF. R3, R4 and C6 can be eliminated if enhanced stereo is not desired.

As shown in Table I, enhanced stereo and loudness are controlled through the same address. It is important to remember to set both functions to the correct value any time either of these functions is updated.

SERIAL DATA COMMUNICATION

Table I also details the serial data structure, range, and bit assignments that sets each function's operating point. The volume and tone controls' function control data binarily increments from zero to maximum as the function's operating point changes from 80 dB attenuation to 0 dB attenuation (volume) or -12 dB to $+12$ dB (tone controls). Note that

DIGITAL I/O

According to Table I, the logic state of DIGITAL INPUT 1 and DIGITAL INPUT 2 is latched and can be retrieved over the IM Bus using the read command (47H). The single-bit information sent on the IM Bus is active low since these lines are internally pulled high.

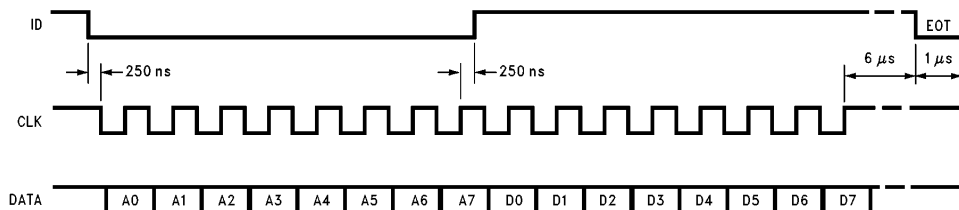
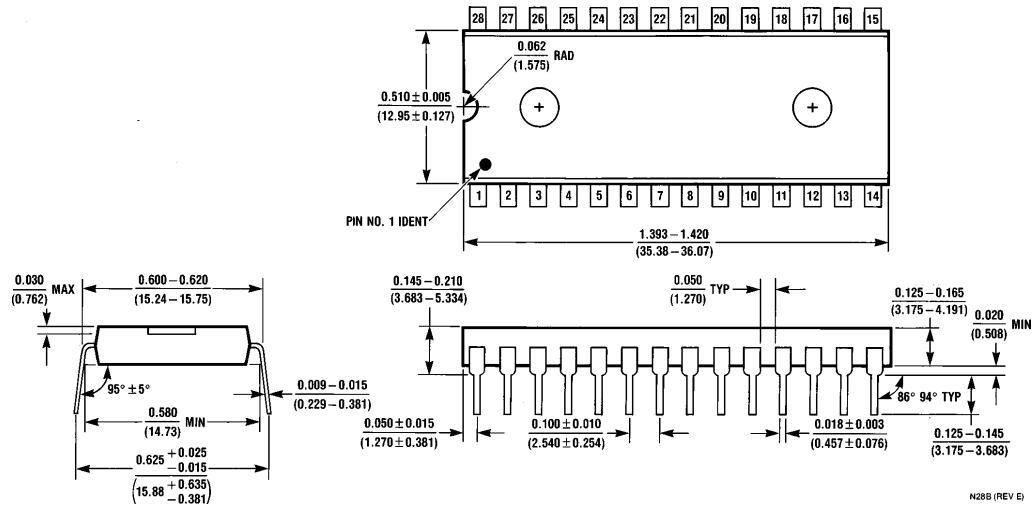


FIGURE 7. LMC1982's INTERMETAL Serial Bus Timing

TL/H/11028-11

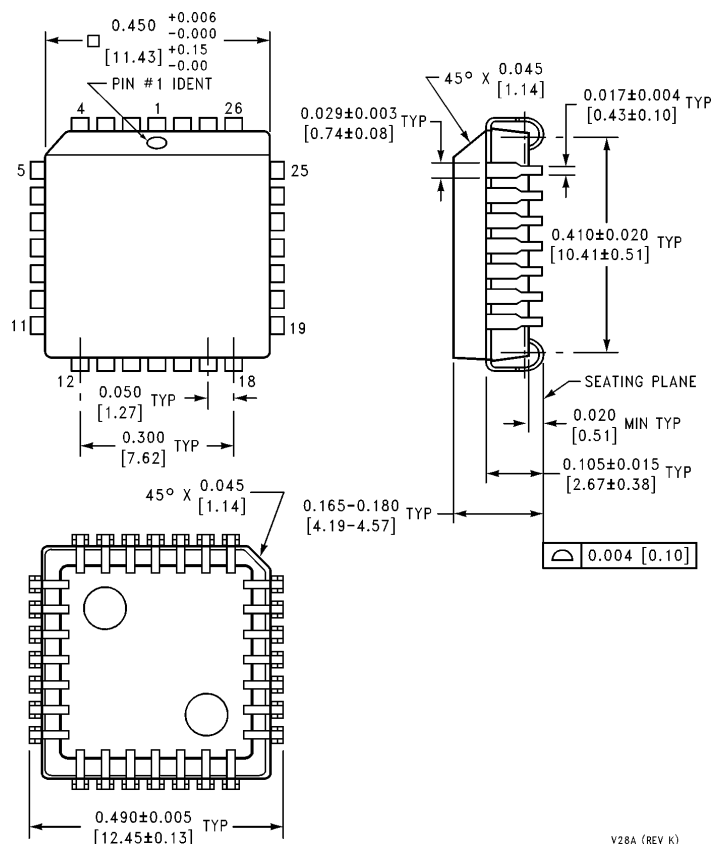


Physical Dimensions inches (millimeters)



LMC1982 Digitally-Controlled Stereo Tone and Volume Circuit with Two Selectable Stereo Inputs

Physical Dimensions inches (millimeters) (Continued)



Order Number LMC1982CIV
NS Package Number V28A

V28A (REV K)

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: (408) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livy-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527849
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihamu-Ku
Chiba-City,
Chiba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semicondutores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty. Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottingham, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.