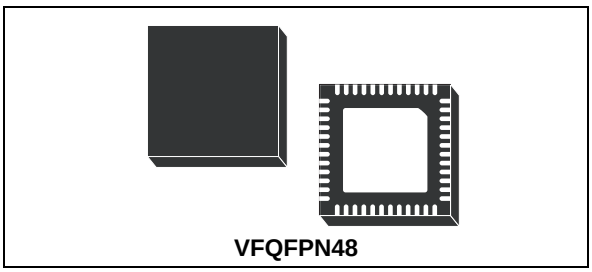
L6717A

High-efficiency hybrid controller with I^{2}C interface and embedded drivers

Datasheet - production data



VFQFPN48

Features

- Hybrid controller for both PVI and SVI CPUs G34 compliant
- Dual controller with embedded high current drivers: 2 phases for CPU CORE + 2 PWM for ext drivers, 1 phase for NB
- Dynamic phase management (DPM)
- I^{2}C interface to control offset, switching frequency and PSI_L
- Dual-edge asynchronous architecture with LTB Technology®
- PSI management to increase efficiency in light-load conditions
- Dual overcurrent protection: total and per-phase compatible with Itdc and IddSpike
- Voltage positioning
- Dual remote sense
- Feedback disconnection protection
- Programmable OV protection
- Oscillator internally fixed at 200 kHz externally adjustable
- LSLess startup to manage pre-biased output
- VFQFPN48 package

Applications

- Hybrid high-current VRM / VRD for desktop / server / workstation / IPC CPUs supporting PVI and SVI interface
- High-density DC-DC converters

Description

L6717A is a hybrid CPU power supply controller embedding 2 high-current drivers for the CORE section and 1 driver for the NB section - requiring up to 2 external drivers when the CORE section works at 4 phase to optimize the application over-all cost.

I^{2}C interface is provided to manage offset for CORE section, switching frequency and dynamic phase management saving in component count and space consumption.

Dynamic phase management automatically adjusts phase-count according to CPU load optimizing the system efficiency under all load conditions.

The dual-edge asynchronous architecture is optimized by LTB technology® allowing fast load-transient response minimizing the output capacitor and reducing the total BOM cost.

Fast protection against load overcurrent is provided for both the sections. Feedback disconnection protection prevents from damaging the load in case of misconnections in the system board. L6717A is available in VFQFPN48 package.

Table 1. Device summary

Order codes	Package	Packing
L6717A	VFQFPN48	Tray
L6717ATR		Tape and reel

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1 Typical application circuit and block diagram

1.1 Application circuit

Figure 1. Typical 4+1 application circuit

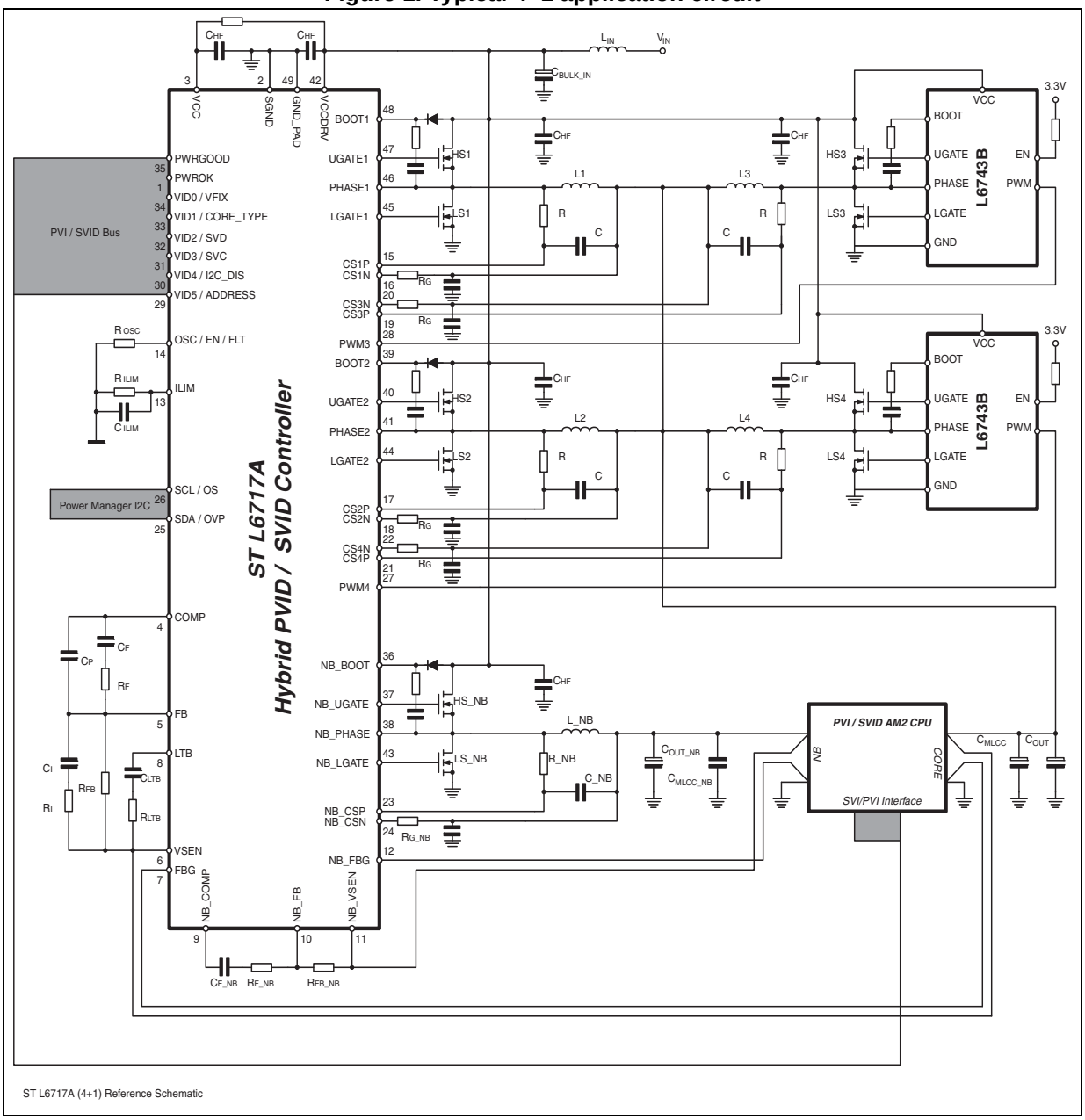


Figure 2. Typical 3+1 application circuit

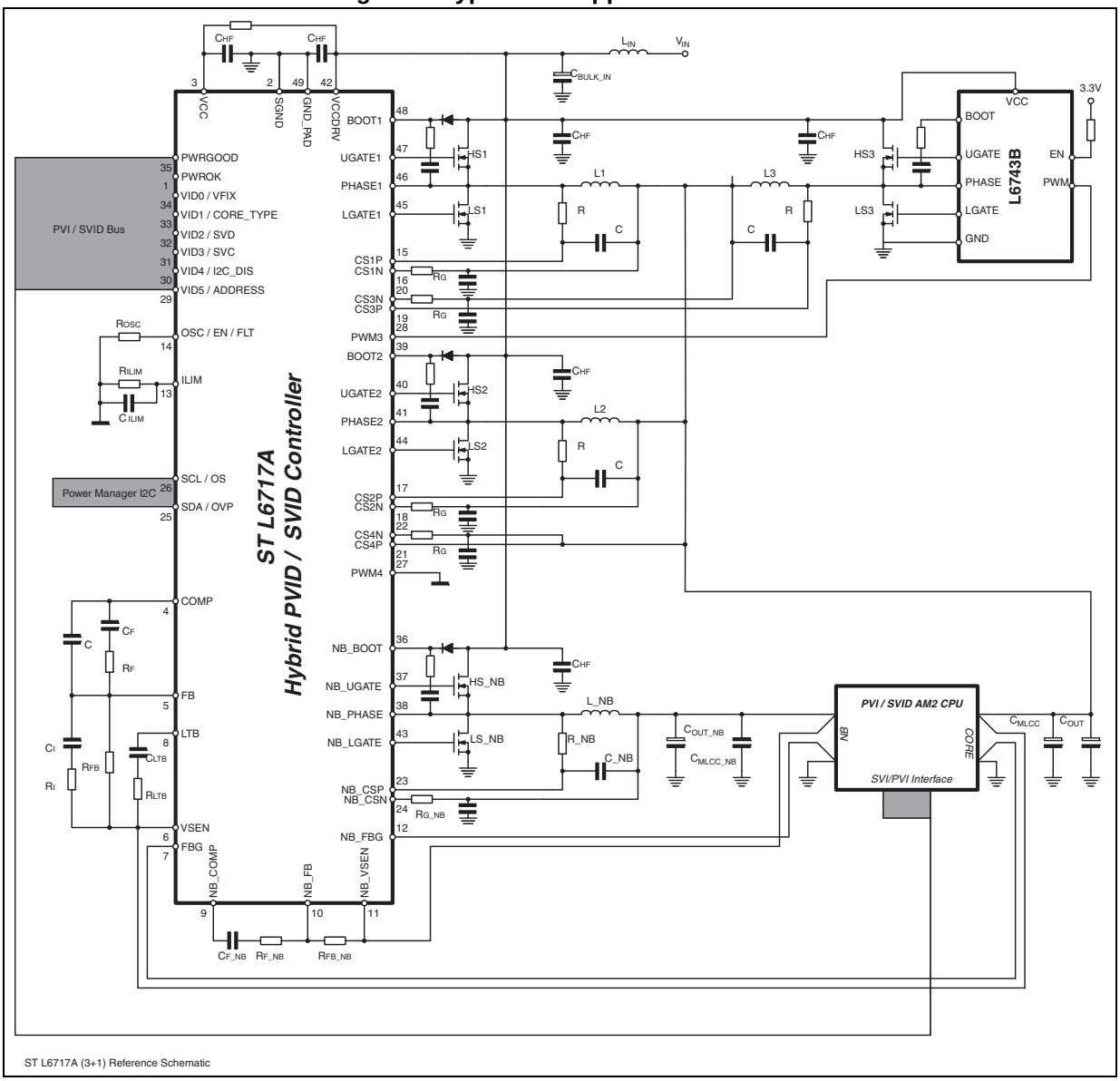
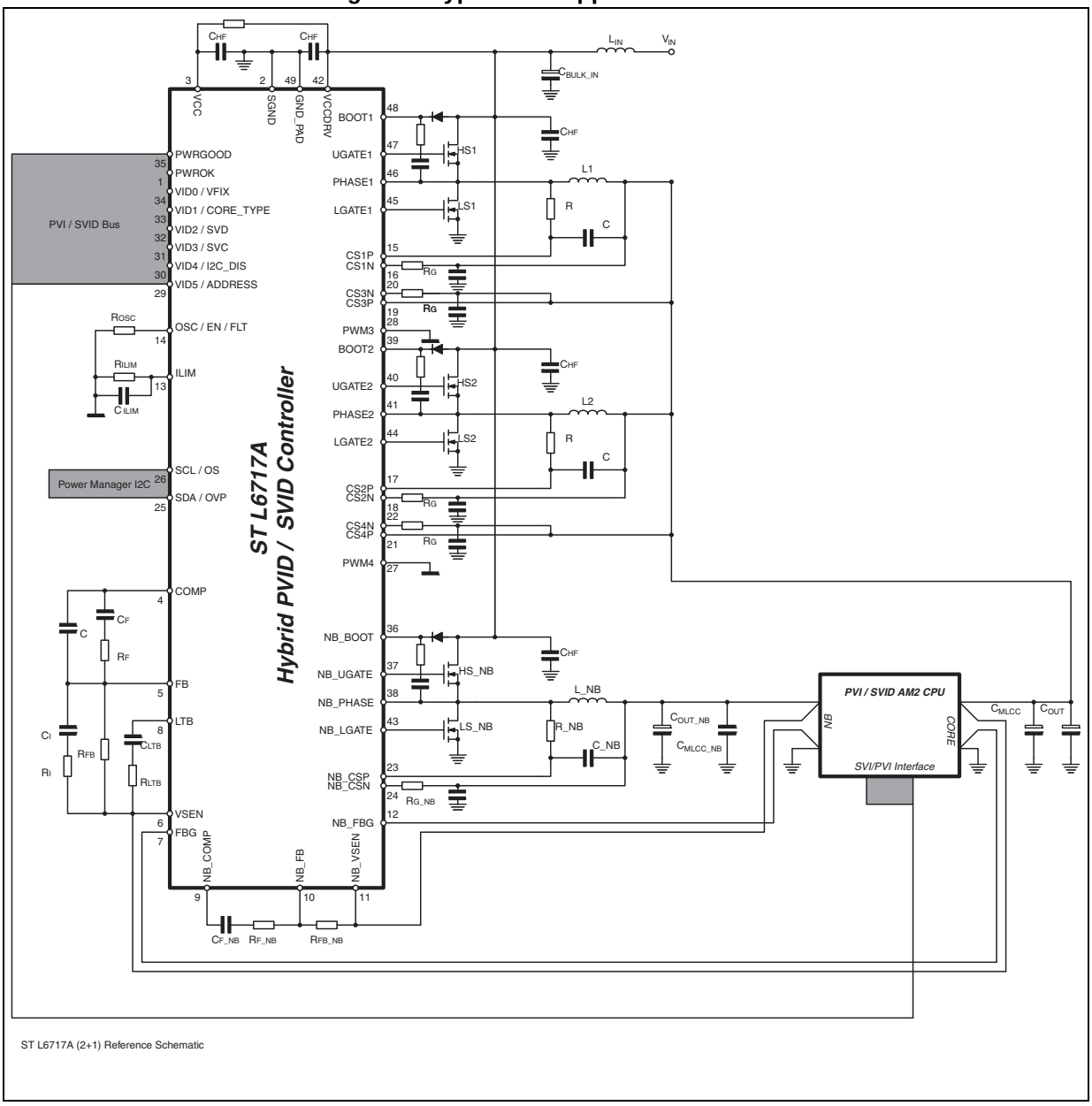


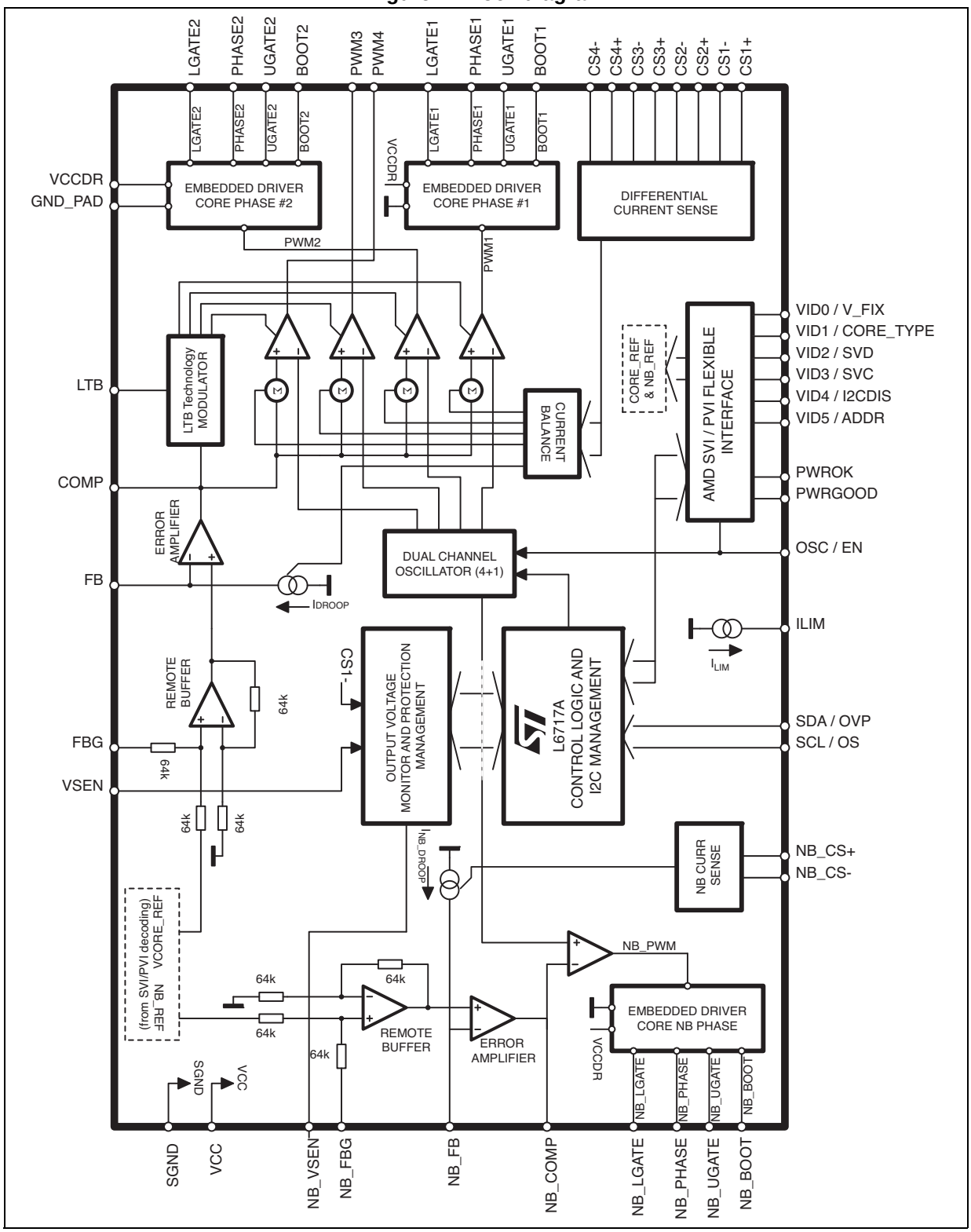
Figure 3. Typical 2+1 application circuit



ST L6717A (2+1) Reference Schematic

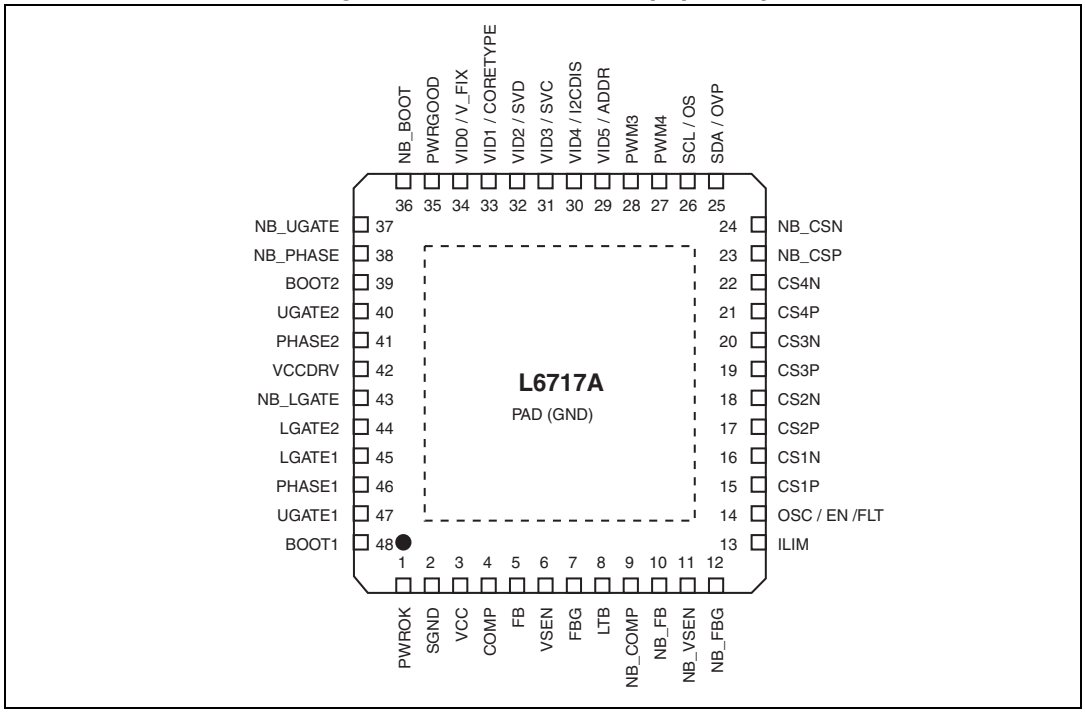
1.2 Block diagram

Figure 4. Block diagram



2 Pins description and connection diagrams

Figure 5. Pins connection (top view)



2.1 Pin descriptions

Table 2. Pin description

Pin#		Name	Function
1		PWROK	System-wide power good input (Ignored in PVI mode). Internally pulled-low by 10µA. When low, the device will decode the two SVI bits SVC and SVD to determine the *Pre-PWROK Metal VID*. When high, the device will actively run the SVI protocol. *Pre-PWROK Metal VID* are latched after EN is asserted and re-used in case of PWROK de-assertion. Latch is reset by VCC or EN cycle.
2		SGND	Device signal ground. All the internal references are referred to this pin. Connect to the PCB signal ground.
3		VCC	Device power supply. Operative voltage is 12 ±15%. Filter with 1µF MLCC to SGND.
4	CORE section	COMP	CORE error amplifier output. Connect with an R_F - C_F to FB. The CORE section and/or the device cannot be disabled by grounding this pin.

Table 2. Pin description (continued)

Pin#		Name	Function
5	CORE section	FB	CORE error amplifier inverting input. Connect with a resistor R_{FB} to VSEN and with an R_F - C_F to COMP. Droop current for voltage positioning is sourced from this pin.
6		VSEN	CORE output voltage monitor. It manages OVP and UVP protections and PWRGOOD. Connect to the positive side of the load for remote sensing. See *Section 8* for details.
7		FBG	CORE remote ground sense. Connect to the negative side of the load for remote sensing. See *Section 11* for proper layout of this connection.
8		LTB	LTB Technology® input pin. Connect through an R_{LTB} - C_{LTB} network to the regulated voltage (CORE section) to detect load transient. See *Section 12* for details.
9	NB section	NB_COMP	NB error amplifier output. Connect with an R_{F_NB} - C_{F_NB} to NB_FB. The NB section and/or the device cannot be disabled by grounding this pin.
10		NB_FB	NB error amplifier inverting input. Connect with a resistor R_{FB_NB} to NB_VSEN and with an R_{F_NB} - C_{F_NB} to NB_COMP. Droop current for Voltage Positioning is sourced from this pin.
11		NB_VSEN	NB output voltage monitor. It manages OVP and UVP protections and PWRGOOD. Connect to the positive side of the NB load to perform remote sensing. See *Section 11* for proper layout of this connection.
12		NB_FBG	NB remote ground sense. Connect to the negative side of the load to perform remote sense. See *Section 11* for proper layout of this connection.
13	CORE section	ILIM	CORE overcurrent pin. A current I_{LIM}=DCR/R_G*I_{OUT} proportional to the current delivered by the CORE section is sourced from this pin. The OC threshold is programmed by connecting a resistor R_{ILIM} to SGND. When the generated voltage crosses the OC_TOT threshold (V_{OC_TOT} = 2.5V Typ) the device latches with all MOSFETs OFF (to recover, cycle VCC or the EN pin). This pin is monitored for dynamic phase management. Filter with proper capacitor to provide OC masking time (0.5mSec typ time constant). See *Section 8.4.1* for details.
14		OSC / EN / FLT	*OSC*: It allows programming the switching frequency F_{SW} of both Sections. Switching frequency can be increased according to the resistor R_{OSC} connected to SGND with a gain of 10kHz/μA (see *Section 9* for details). If floating, the switching frequency is 200kHz per phase. *EN*: Pull-low to disable the device. When set free, the device immediately checks for the VID1 status to determine the SVI / PVI protocol to be adopted and configures itself accordingly. *FLT*: The pin is forced high (3.3V) in case of an OV / UV fault. To recover from this condition, cycle VCC or the EN pin. Drive with open drain circuit. See *Section 8* for details.

Table 2. Pin description (continued)

Pin#		Name	Function
5	CORE section	FB	CORE error amplifier inverting input. Connect with a resistor R_{FB} to VSEN and with an R_F - C_F to COMP. Droop current for voltage positioning is sourced from this pin.
6		VSEN	CORE output voltage monitor. It manages OVP and UVP protections and PWRGOOD. Connect to the positive side of the load for remote sensing. See *Section 8* for details.
7		FBG	CORE remote ground sense. Connect to the negative side of the load for remote sensing. See *Section 11* for proper layout of this connection.
8		LTB	LTB Technology® input pin. Connect through an R_{LTB} - C_{LTB} network to the regulated voltage (CORE section) to detect load transient. See *Section 12* for details.
9	NB section	NB_COMP	NB error amplifier output. Connect with an R_{F_NB} - C_{F_NB} to NB_FB. The NB section and/or the device cannot be disabled by grounding this pin.
10		NB_FB	NB error amplifier inverting input. Connect with a resistor R_{FB_NB} to NB_VSEN and with an R_{F_NB} - C_{F_NB} to NB_COMP. Droop current for Voltage Positioning is sourced from this pin.
11		NB_VSEN	NB output voltage monitor. It manages OVP and UVP protections and PWRGOOD. Connect to the positive side of the NB load to perform remote sensing. See *Section 11* for proper layout of this connection.
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14		OSC / EN / FLT	*OSC*: It allows programming the switching frequency F_{SW} of both Sections. Switching frequency can be increased according to the resistor R_{OSC} connected to SGND with a gain of 10kHz/μA (see *Section 9* for details). If floating, the switching frequency is 200kHz per phase. *EN*: Pull-low to disable the device. When set free, the device immediately checks for the VID1 status to determine the SVI / PVI protocol to be adopted and configures itself accordingly. *FLT*: The pin is forced high (3.3V) in case of an OV / UV fault. To recover from this condition, cycle VCC or the EN pin. Drive with open drain circuit. See *Section 8* for details.

Table 2. Pin description (continued)

Pin#		Name	Function
15	CORE section	CS1P	Channel 1 current sense positive input. Connect through an R-C filter to the phase-side of the channel 1 inductor. See *Section 11* for proper layout of this connection.
16		CS1N	Channel 1 current sense negative input. Connect through a R_G resistor to the output-side of the channel inductor. Filter the Vout-side of R_G resistor with 100nF to GND. See *Section 11* for proper layout of this connection.
17		CS2P	Channel 2 current sense positive input. Connect through an R-C filter to the phase-side of the channel 2 inductor. See *Section 11* for proper layout of this connection.
18		CS2N	Channel 2 current sense negative input. Connect through a R_G resistor to the output-side of the channel inductor. Filter the Vout-side of R_G resistor with 100nF to GND. See *Section 11* for proper layout of this connection.
19		CS3P	Channel 3 current sense positive input. Connect through an R-C filter to the phase-side of the channel 3 inductor. When working at 2 phase, directly connect to V_{out_CORE}. See *Section 11* for proper layout of this connection.
20		CS3N	Channel 3 current sense negative input. Connect through a R_G resistor to the output-side of the channel inductor. When working at 2 phase, connect through R_G to CS3+. Filter the Vout-side of R_G resistor with 100nF to GND. See *Section 11* for proper layout of this connection.
21		CS4P	Channel 4 current sense positive input. Connect through an R-C filter to the phase-side of the channel 4 inductor. When working at 2 or 3 phase, directly connect to V_{out_CORE}. See *Section 11* for proper layout of this connection.
22		CS4N	Channel 4 current sense negative input. Connect through a R_G resistor to the output-side of the channel inductor. When working at 2 or 3 phase, connect through R_G to CS4+.Filter the Vout-side of R_G resistor with 100nF to GND. See *Section 11* for proper layout of this connection.
23	NB section	NB_CSP	NB channel current sense positive input. Connect through an R-C filter to the phase-side of the NB channel inductor. See *Section 11* for proper layout of this connection.
24		NB_CSN	NB channel current sense negative input. Connect through a R_G resistor to the output-side of the channel inductor. Filter the Vout-side of R_G resistor with 100nF to GND. See *Section 11* for proper layout of this connection.

Table 2. Pin description (continued)

Pin#		Name	Function
25	Power manager I^2C	SDA / OVP	*SDA - power manager I^2C data*. When power manager I^2C is enabled, this is the data connection. See *Section 6* for details. *OVP - over voltage setting*. When power manager I^2C is disabled (VID4 / I2CDIS to 3.3V) this pin sources a constant 10µA current. By connecting a resistor R_{OVP} to GND, the OV threshold for both Sections is defined. See *Section 8.1* for details.
26		SCL / OS	*SCL - power manager I^2C clock*. When power manager I^2C is enabled, this is the clock connection. See *Section 6* for details. *OS - CORE section offset*. When power manager I^2C is disabled (VID4 / I2CDIS to 3.3V) this pin is internally set to 1.24V(2.0V): connecting a R_{OS} resistor to GND (3.3V) allows setting a current that is mirrored into FB pin in order to program a positive (negative) offset according to the selected R_{FB}. Short to GND to disable the function. See *Section 7.4* for details.
27, 28		PWM4, PWM3	PWM output for external drivers. Connect to external drivers PWM inputs. The device is able to manage HiZ status by setting the pins floating. By shorting to GND PWM4 or PWM3 and PWM4, it is possible to program the CORE section to work at 3 or 2 phase respectively. See *Section 5.4.4* for details about HiZ management.
29	SVI / PVI interface	VID5 / ADDR	Voltage identification pin - I^2C address pin. Internally pulled-low by 10µA, it programs the output voltage in PVI mode. In SVI mode, the pin is monitored on the EN pin rising-edge to modify the I^2C address. See *Section 5* for details.
30		VID4 / I2CDIS	Voltage identification pin - I^2C disable pin. Internally pulled-low by 10µA, it programs the output voltage in PVI mode. In SVI mode, the pin is monitored on the EN pin rising-edge to enable/disable the I^2C. See *Section 5* for details.
31		VID3 / SVC	Voltage IDentification Pin - SVI Clock Pin. Internally pulled-low by 10µA, it programs the output voltage in both SVI and PVI modes. In SVI mode, the 10µA pull down is disabled. See *Section 5* for details.
32		VID2 / SVD	Voltage identification pins - SVI data pin. Internally pulled-low by 10µA, it programs the output voltage in both SVI and PVI modes. In SVI mode, the 10µA pull down is disabled. See *Section 5* for details.
33	SVI / PVI interface	VID1 / CORETYPE	Voltage identification pin. Internally pulled-low by 10µA, it programs the output voltage in PVI mode. The pin is monitored on the EN pin rising-edge to define the operative mode of the controller (SVI or PVI). See *Section 5* for details.
34		VID0 / VFIX	Voltage identification pin. Internally pulled-low by 10µA, it programs the output voltage in PVI mode. If the pin is pulled to 3.3V, the device enters V_FIX mode and SVI commands are ignored. See *Section 5* for details.

Table 2. Pin description (continued)

Pin#		Name	Function
35		PWRGOOD	VCORE and NB power good. It is an open-drain output set free after SS as long as both the voltage planes are within specifications. Pull-up to 3.3V (typ) or lower, if not used it can be left floating. When in PVI mode, it monitors the CORE section only.
36	Embedded drivers	NB_BOOT	NB section high-side driver supply. This pin supplies the high-side floating driver. Connect through C_{BOOT} capacitor to the NB_PHASE pin. See *Section 10* for guidance in designing the capacitor value.
37		NB_UGATE	NB Section High-Side Driver Output. Connect to NB Section High-Side MOSFET gate. A small series resistor may help in reducing NB_PHASE pin negative spike as well as cooling the device.
38		NB_PHASE	NB section high-side driver return path. Connect to the NB section high-side MOSFET source. This pin is also monitored for the adaptive dead-time management.
39		BOOT2	CORE section, phase 2 high-side driver supply. This pin supplies the high-side floating driver. Connect through C_{BOOT} capacitor to the PHASE2 pin. See *Section 10* for guidance in designing the capacitor value.
40		UGATE2	High-Side Driver Output. Connect to Phase2 High-Side MOSFET gate. A small series resistor may help in reducing PHASE2 pin negative spike as well as cooling the device.
41		PHASE2	CORE section, phase 2 high-side driver return path. Connect to the phase2 high-side MOSFET source. This pin is also monitored for the adaptive dead-time management.
42		VCCDRV	Supply voltage for low-side embedded drivers. Operative voltage is flexible from 5V ±5% to 12 ±15%. Filter with 1µF MLCC to GND.
43 to 45	Embedded drivers	NB_LGATE, LGATE2, LGATE1	Low-side driver output. Connect directly to the low-side MOSFET gate of the related section. A small series resistor can be useful to reduce dissipated power especially in high frequency applications.
46		PHASE1	CORe section, phase 1 high-side driver return path. Connect to the phase1 high-side MOSFET source. This pin is also monitored for the adaptive dead-time management.
47		UGATE1	High-side driver output. Connect to phase1 high-side MOSFET gate. A small series resistor may help in reducing PHASE1 pin negative spike as well as cooling the device.
48		BOOT1	CORE section, phase 1 high-side driver supply. This pin supplies the high-side floating driver. Connect through C_{BOOT} capacitor to the PHASE1 pin. See *Section 10* for guidance in designing the capacitor value.
Thermal PAD		GND	All internal references, logic, and the silicon substrate are referenced to this pin. Connect to the PCB GND ground plane by multiple vias to improve heat dissipation.

2.2 Thermal data

Table 3.Thermal data

Symbol	Parameter	Value	Unit
R_{THJA}	Thermal resistance junction to ambient (Device soldered on 2s2p PC board)	40	°C/W
R_{THJC}	Thermal resistance junction to case	1	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction temperature range	0 to 125	°C

3 Electrical specifications

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}, V_{CCDRV}	to GND	-0.3 to 15	V
V_{BOOTx}, V_{UGATEx}	to GND to PHASEx	41 15	V
V_{PHASEx}	(VCC=VCCDR=12V) To GND Negative spike to GND, t < 400ns Positive spike to GND, t < 200 ns	-0.3 to 26 -8 30	V
V_{LGATEx}	to GND to GND, t < 100nsec.	-0.3 to VCCDRV + 0.3 -3	V
	All other pins to GND	-0.3 to 3.6	V
	Maximum withstanding voltage range test condition: CDF-AEC-Q100-002- “Human Body Model” acceptance “Normal Performance”	±1750	V

3.2 Electrical characteristics

V_{CC}=12V±15%, T_J = 0°C to 70°C unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current and power-on						
I_{CC}	VCC supply current	OSC = GND		15		mA
I_{CCDR}	VCCDR supply current			4		mA
I_{BOOTx}	BOOTx supply current			1.5		mA
$UVLO_{VCC}$	VCC turn-ON	VCC rising			4.5	V
	VCC turn-OFF	VCC falling	4			V
Oscillator						
F_{SW}	Main oscillator accuracy		180	200	220	kHz
	Oscillator adjustability	R_{OSC} = 36kΩ	425	500	575	kHz
ΔV_{OSC}	PWM ramp amplitude	CORE and NB section		1.5		V
FAULT	Voltage at Pin OSC	OVP, UVP latch active	3		3.6	V
EN	Turn-OFF threshold	OSC/EN falling	0.3			V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
PVI / SVI interface						
PWROK	Input high		1.3			V
	Input low				0.80	V
VID2,/SVD VID3/SVC	Input high	(SVI mode)	0.95			V
	Input low	(SVI mode)			0.65	V
SVD	Voltage low (ACK)	I_{SINK} = -5mA			250	mV
VID0 to VID5	Input high	(PVI mode)	1.3			V
	Input low	(PVI mode)			0.80	V
V_FIX	Entering V_FIX mode	VID0/V_FIX rising	3			V
Power manager I^2C						
SDA, SCL	Input high		1.3			V
	Input low				0.8	V
SDA	Voltage low (ACK)	I_{SINK} = -5mA			250	mV
Voltage positioning (CORE and NB section)						
CORE	Output voltage accuracy	VSEN to V_{CORE}; FBG to GND_{CORE}	-8		8	mV
NB		NBVSEN to V_{NB}; NBFBG to GND_{FB}	-10		10	mV
OS	OFFSET bias voltage	I2DIS=3.3V, I_{OS} = 0 to 250µA	1.190	1.24	1.290	V
	OFFSET current range	I2DIS=3.3V	0		250	µA
	OFFSET - I_{FB} accuracy	I2DIS=3.3V, I_{OS} = 0µA	-2.25		2.25	µA
		I2DIS=3.3V, I_{OS} = 250µA	-9		9	µA
DROOP	DROOP accuracy	I_{DROOP} = 0 to 25µA, k_{DRP} = 1/4	-3		3	µA
		I_{NB_DROOP} = 0 to 6µA, k_{NBDRP} = 1/4	-1		1	µA
A_0	EA DC gain			100		dB
SR	Slew rate	COMP, NB_COMP to SGND = 10pF		20		V/µs
PWM outputs (CORE only) and embedded drivers						
PWM3, PWM4	Output high	I = 1mA	3		3.6	V
	Output low	I = -1mA			0.2	V
I_{PWMx}	Test current			10		µA
High current embedded drivers						
R_{HIHS}	HS source resistance	BOOT - PHASE = 12V; 100mA		2.3	2.8	Ω
I_{UGATE}	HS source current	BOOT - PHASE = 12V; (1) C_{UGATE} to PHASE = 3.3nF		2		A
R_{LOHS}	HS sink resistance	BOOT - PHASE = 12V; 100mA		2	2.5	Ω
R_{HILS}	LS source resistance	100mA		1.3	1.8	Ω

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{LGATE}	LS source current	C_{LGATE} to GND = 5.6nF; (1)		3		A
R_{LOLS}	LS sink resistance	100mA		1	1.5	Ω
Protections						
OVP	Overvoltage protection	I^2C enabled, no commands issued, wrt VID, CORE & NB section	+200	+250	+300	mV
		I^2C enabled, V_FIX mode; VSEN, NB_VSEN rising		1.800		V
	SDA/OVP bias current	I2CDIS = 3.3V	9	11	13	µA
UVP	Undervoltage protection	VSEN, NB_VSEN falling; wrt Ref.	-450	-400	-350	mV
PWRGOOD	PGOOD threshold	VSEN, NB_VSEN falling; wrt Ref	-285	-250	-215	mV
	Voltage low	$I_{PWRGOOD}$ = -4mA			0.4	V
$V_{FB-DISC}$	FB disconnection	V_{CSN} rising, above VSEN CORE and NB sections		600		mV
$V_{FBG\ DISC}$	FBG disconnection	EA NI input wrt VID		500		mV
V_{OC_TOT}	CORE OC		2.425	2.500	2.575	V
kI_{ILIM}		I_{LIM} = 0µA	0		4	µA
		I_{LIM} = 100µA		100		µA

1. Parameter(s) guaranteed by designed, not fully tested in production

4 Device description and operation

L6717A is a hybrid CPU power supply controller compatible with both parallel (PVI) and serial (SVI) protocols for AMD processors. The device provides complete control logic and protections for a high-performance step-down DC-DC voltage regulator, optimized for advanced microprocessor power supply supporting both PVI and SVI communication. It embeds two independent controllers for CPU CORE and the integrated NB, each one with its own set of protections. NB phase (when enabled) is automatically phase-shifted with respect to the CORE phases in order to reduce the total input rms current amount.

The device features an additional power manager I^2C interface to easy the system design for enthusiastic application where the main parameters of the voltage regulator have to be modified. L6717A is able to adjust the regulated voltage, the switching frequency and also the OV protection threshold through the power manager I^2C bus while the application is running assuring fast and reliable transitions.

Dynamic phase management (DPM) allows the device to automatically adjust the phase count according to the current delivered to the load. This feature allow the system to keep alive only the phases really necessary to sustain the load saving in power dissipation so optimizing the efficiency over the whole current range of the application. DPM can be enabled through the power manager I^2C bus.

L6717A is able to detect which kind of CPU is connected in order to configure itself to work as a single-plane PVI controller or dual-plane SVI controller.

The controller performs a single-phase control for the NB section and a programmable 2-to-4 phase control for the CORE section featuring dual-edge non-latched architecture: this allows fast load-transient response optimizing the output filter consequently reducing the total BOM cost. Further reduction in output filter can be achieved by enabling LTB Technology®.

PSI_L Flag is sent to the VR through the SVI bus. The controller monitors this flag and selectively modifies the phase number in order to optimize the system efficiency when the CPU enters low-power states. This causes the over-all efficiency to be maximized at light loads so reducing losses and system power consumption.

Both sections feature programmable overvoltage protection and adjustable constant overcurrent protection. Voltage positioning (LL) is possible thanks to an accurate fully-differential current-sense across the main inductors for both sections.

L6717A features dual remote sensing for the regulated outputs (CORE and NB) in order to recover from PCB voltage drops also protecting the load from possible feedback network disconnections.

LSLess start-up function allows the controller to manage pre-biased start-up avoiding dangerous current return through the main inductors as well as negative undershoot on the output voltage if the output filter is still charged before start-up.

L6717A supports V_FIX mode for system debugging: in this particular configuration the SVI bus is used as a static bus configuring 4 operative voltages for both the sections and ignoring any serial-VID command.

When working in PVI mode, the device features On-the-Fly VID management: VID code is continuously sampled and the reference update according to the variation detected,

L6717A is available in VFQFPN48 package.

5 Hybrid CPU support and CPU_TYPE detection

L6717A is able to detect the type of the CPU-core connected and to configure itself accordingly. At system Start-up, on the rising-edge of the EN signal, the device monitors the status of VID1 and configures the PVI mode (VID1 = 1) or SVI mode (VID1 = 0).

When in PVI mode, L6717A uses the information available on the VID[0: 5] bus to address the CORE section output voltage according to *Table 6*. NB section is kept in HiZ mode, both MOSFETs are kept OFF.

When in SVI mode, L6717A DAC ignores the information available on VID0, VID4 and VID5 and uses VID2 and VID3 as a SVI bus addressing the CORE and NB sections according to the SVI protocol. The device supports 3.4MHz bus rate frequency.

Caution: To avoid any risk of errors in CPU type detection (i.e. detecting SVI CPU when PVI CPU is installed on the socket and vice versa), it is recommended to carefully control the start-up sequencing of the system hosting L6717A in order to ensure than on the EN rising-edge, VID1 is in valid and correct state. Typical connections consider VID1 connected to CPU CORE_TYPE through a resistor to correctly address the CPU detection.

5.1 PVI - parallel interface

PVI is a 6-bit-wide parallel interface used to address the CORE section reference. According to the selected code, the device sets the CORE section reference and regulates its output voltage as reported into *Table 6*.

NB section is always kept in HiZ; no activity is performed on this section and both the high-side and low-side of this section are kept OFF. Furthermore, PWROK information is ignored as well since the signal only applies to the SVI protocol.

5.2 PVI start-up

Once the PVI mode has been detected, the device uses the whole code available on the VID[0:5] lines to define the reference for the CORE section. NB section is kept in HiZ. Soft-start to the programmed reference is performed regardless of the state of PWROK.

See *Section 7.8* for details about soft-start.

Figure 6. System start-up: SVI (to Metal-VID; left) and PVI (right)

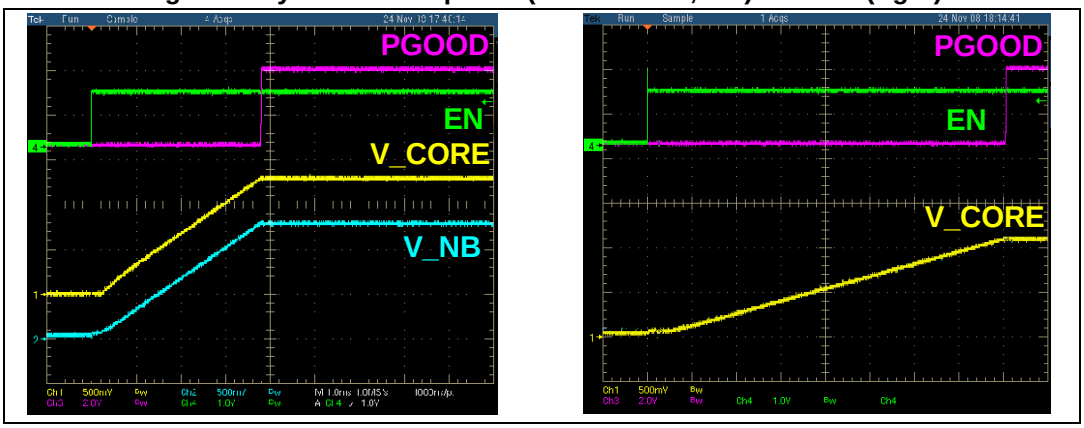


Table 6. Voltage identifications (VID) codes for PVI mode

VID5	VID4	VID3	VID2	VID1	VID0	Output voltage	VID5	VID4	VID3	VID2	VID1	VID0	Output voltage
0	0	0	0	0	0	1.5500	1	0	0	0	0	0	0.7625
0	0	0	0	0	1	1.5250	1	0	0	0	0	1	0.7500
0	0	0	0	1	0	1.5000	1	0	0	0	1	0	0.7375
0	0	0	0	1	1	1.4750	1	0	0	0	1	1	0.7250
0	0	0	1	0	0	1.4500	1	0	0	1	0	0	0.7125
0	0	0	1	0	1	1.4250	1	0	0	1	0	1	0.7000
0	0	0	1	1	0	1.4000	1	0	0	1	1	0	0.6875
0	0	0	1	1	1	1.3750	1	0	0	1	1	1	0.6750
0	0	1	0	0	0	1.3500	1	0	1	0	0	0	0.6625
0	0	1	0	0	1	1.3250	1	0	1	0	0	1	0.6500
0	0	1	0	1	0	1.3000	1	0	1	0	1	0	0.6375
0	0	1	0	1	1	1.2750	1	0	1	0	1	1	0.6250
0	0	1	1	0	0	1.2500	1	0	1	1	0	0	0.6125
0	0	1	1	0	1	1.2250	1	0	1	1	0	1	0.6000
0	0	1	1	1	0	1.2000	1	0	1	1	1	0	0.5875
0	0	1	1	1	1	1.1750	1	0	1	1	1	1	0.5750
0	1	0	0	0	0	1.1500	1	1	0	0	0	0	0.5625
0	1	0	0	0	1	1.1250	1	1	0	0	0	1	0.5500
0	1	0	0	1	0	1.1000	1	1	0	0	1	0	0.5375
0	1	0	0	1	1	1.0750	1	1	0	0	1	1	0.5250
0	1	0	1	0	0	1.0500	1	1	0	1	0	0	0.5125
0	1	0	1	0	1	1.0250	1	1	0	1	0	1	0.5000
0	1	0	1	1	0	1.0000	1	1	0	1	1	0	0.4875
0	1	0	1	1	1	0.9750	1	1	0	1	1	1	0.4750
0	1	1	0	0	0	0.9500	1	1	1	0	0	0	0.4625
0	1	1	0	0	1	0.9250	1	1	1	0	0	1	0.4500
0	1	1	0	1	0	0.9000	1	1	1	0	1	0	0.4375
0	1	1	0	1	1	0.8750	1	1	1	0	1	1	0.4250
0	1	1	1	0	0	0.8500	1	1	1	1	0	0	0.4125
0	1	1	1	0	1	0.8250	1	1	1	1	0	1	0.4000
0	1	1	1	1	0	0.8000	1	1	1	1	1	0	0.3875
0	1	1	1	1	1	0.7750	1	1	1	1	1	1	0.3750

5.3 SVI - serial interface

SVI is a two wire, clock and data, bus that connects a single master (CPU) to one slave (L6717A). The master initiates and terminates SVI transactions and drives the clock, SVC, and the data, SVD, during a transaction. The slave receives the SVI transactions and acts accordingly. SVI wire protocol is based on fast-mode I^2C.

SVI interface also considers two additional signal needed to manage the system start-up. These signals are EN and PWROK. The device return a PWRGOOD signal if the output voltages are in regulation.

5.4 SVI start-up

Once the SVI mode has been detected on the EN rising-edge, L6717A checks for the status of the two serial VID pins, SVC and SVD, and stores this value as the *Pre-PWROK Metal VID*. The controller initiate a soft-start phase regulating both CORE and NB voltage planes to the voltage level prescribed by the *Pre-PWROK Metal VID*. See *Table 7* for details about *Pre-PWROK Metal VID* codifications. The stored *Pre-PWROK Metal VID* value are re-used in any case of PWROK de-assertion.

After bringing the output rails into regulation, the controller asserts the PWRGOOD signal and waits for PWROK to be asserted. Until PWROK is asserted, the controller regulates to the *Pre-PWROK Metal VID* ignoring any commands coming from the SVI interface.

After PWROK is asserted, the processor has initialized the serial VID interface and L6717A waits for commands from the CPU to move the voltage planes from the *Pre-PWROK Metal VID* values to the operative VID values. As long as PWROK remains asserted, the controller will react to any command issued through the SVI interface according to SVI protocol.

See *Section 7.8* for details about soft-start.

Table 7. V_FIX mode and *Pre-PWROK MetalVID*

SVC	SVD	Output voltage [V]	
		Pre-PWROK Metal VID	V_FIX mode
0	0	1.1V	1.4V
0	1	1.0V	1.2V
1	0	0.9V	1.0V
1	1	0.8V	0.8V

5.4.1 Set VID command

The *set VID command* is defined as the command sequence that the CPU issues on the SVI bus to modify the voltage level of the CORE Section and/or the NB section.

During a *set VID Command*, the processor sends the start (START) sequence followed by the address of the Section which the *set VID command* applies. The processor then sends the write (WRITE) bit. After the write bit, the voltage regulator (VR) sends the acknowledge (ACK) bit. The processor then sends the VID bits code during the *data phase*. The VR sends the acknowledge (ACK) bit after the data phase. Finally, the processor sends the stop (STOP) sequence. After the VR has detected the stop, it performs an On-the-Fly VID

transition for the addressed section(s) or, more in general, react to the sent command accordingly. Refer to *Figure 7*, *Table 8* and *Table 9* for details about the *set VID command.*

L6717A is able to manage individual power OFF for both the sections. The CPU may issue a serial VID command to power OFF or power ON one section while the other one remains powered. In this case, the PWRGOOD signal remains asserted.

Figure 7. SVI communications - send byte

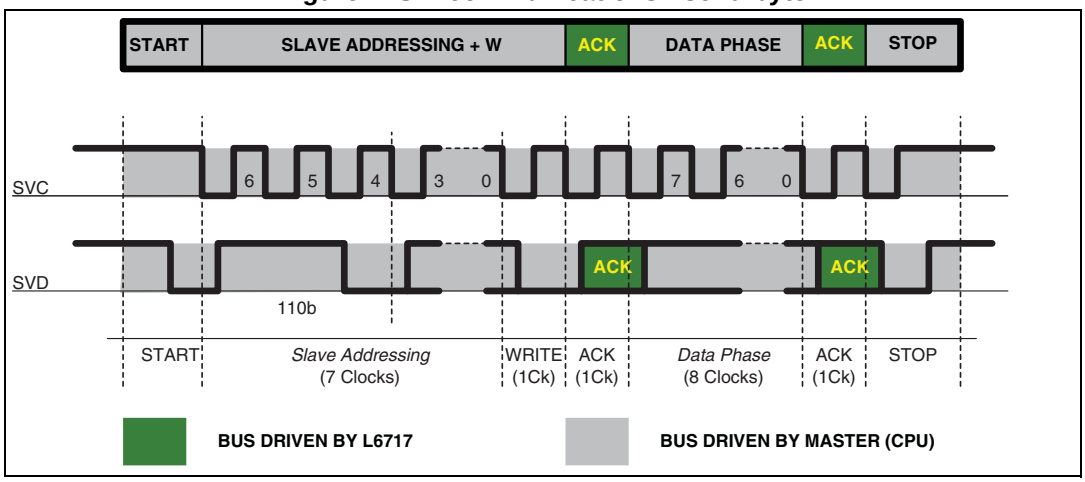


Table 8. SVI send byte - address and data phase description

bits	Description
Address phase	
6:4	Always 110b.
3	Not applicable, ignored.
2	Not applicable, ignored.
1	CORE section(1). If set then the following data byte contains the VID code for CORE section.
0	NB section(1). If set then the following data byte contains the VID code for NB section.
Data phase	
7	PSI_L flag (Active low).When asserted, the VR is allowed to enter power-saving mode. See *Section 5.4.3*.
6:0	VID code. See *Table 9*.

1. Assertion in both bit 1 and 0 will address the VID code to both CORE and NB simultaneously.

Table 9. Data phase - serial VID codes

SVI [6:0]	Output voltage	SVI [6:0]	Output voltage	SVI [6:0]	Output voltage	SVI [6:0]	Output voltage
000_0000	1.5500	010_0000	1.1500	100_0000	0.7500	110_0000	0.3500
000_0001	1.5375	010_0001	1.1375	100_0001	0.7375	110_0001	0.3375
000_0010	1.5250	010_0010	1.1250	100_0010	0.7250	110_0010	0.3250
000_0011	1.5125	010_0011	1.1125	100_0011	0.7125	110_0011	0.3125
000_0100	1.5000	010_0100	1.1000	100_0100	0.7000	110_0100	0.3000
000_0101	1.4875	010_0101	1.0875	100_0101	0.6875	110_0101	0.2875
000_0110	1.4750	010_0110	1.0750	100_0110	0.6750	110_0110	0.2750
000_0111	1.4625	010_0111	1.0625	100_0111	0.6625	110_0111	0.2625
000_1000	1.4500	010_1000	1.0500	100_1000	0.6500	110_1000	0.2500
000_1001	1.4375	010_1001	1.0375	100_1001	0.6375	110_1001	0.2375
000_1010	1.4250	010_1010	1.0250	100_1010	0.6250	110_1010	0.2250
000_1011	1.4125	010_1011	1.0125	100_1011	0.6125	110_1011	0.2125
000_1100	1.4000	010_1100	1.0000	100_1100	0.6000	110_1100	0.2000
000_1101	1.3875	010_1101	0.9875	100_1101	0.5875	110_1101	0.1875
000_1110	1.3750	010_1110	0.9750	100_1110	0.5750	110_1110	0.1750
000_1111	1.3625	010_1111	0.9625	100_1111	0.5625	110_1111	0.1625
001_0000	1.3500	011_0000	0.9500	101_0000	0.5500	111_0000	0.1500
001_0001	1.3375	011_0001	0.9375	101_0001	0.5375	111_0001	0.1375
001_0010	1.3250	011_0010	0.9250	101_0010	0.5250	111_0010	0.1250
001_0011	1.3125	011_0011	0.9125	101_0011	0.5125	111_0011	0.1125
001_0100	1.3000	011_0100	0.9000	101_0100	0.5000	111_0100	0.1000
001_0101	1.2875	011_0101	0.8875	101_0101	0.4875	111_0101	0.0875
001_0110	1.2750	011_0110	0.8750	101_0110	0.4750	111_0110	0.0750
001_0111	1.2625	011_0111	0.8625	101_0111	0.4625	111_0111	0.0625
001_1000	1.2500	011_1000	0.8500	101_1000	0.4500	111_1000	0.0500
001_1001	1.2375	011_1001	0.8375	101_1001	0.4375	111_1001	0.0375
001_1010	1.2250	011_1010	0.8250	101_1010	0.4250	111_1010	0.0250
001_1011	1.2125	011_1011	0.8125	101_1011	0.4125	111_1011	0.0125
001_1100	1.2000	011_1100	0.8000	101_1100	0.4000	111_1100	OFF
001_1101	1.1875	011_1101	0.7875	101_1101	0.3875	111_1101	OFF
001_1110	1.1750	011_1110	0.7750	101_1110	0.3750	111_1110	OFF
001_1111	1.1625	011_1111	0.7625	101_1111	0.3625	111_1111	OFF

5.4.2 PWROK de-assertion

Anytime PWROK de-asserts while EN is asserted, the controller uses the previously stored *Pre-PWROK Metal VID* and regulates all the planes to that level performing an on-the-fly transition to that level.

PWRGOOD is treated appropriately being de-asserted in case the *Pre-PWROK Metal VID* voltage is out of the initial voltage specifications.

5.4.3 PSI_L and efficiency optimization at light-load

PSI_L is an active-low flag (i.e. low logic level when asserted) that can be set by the CPU to allow the VR to enter power-saving mode to maximize the system efficiency when in light-load conditions. The status of the flag is communicated to the controller through the SVI bus.

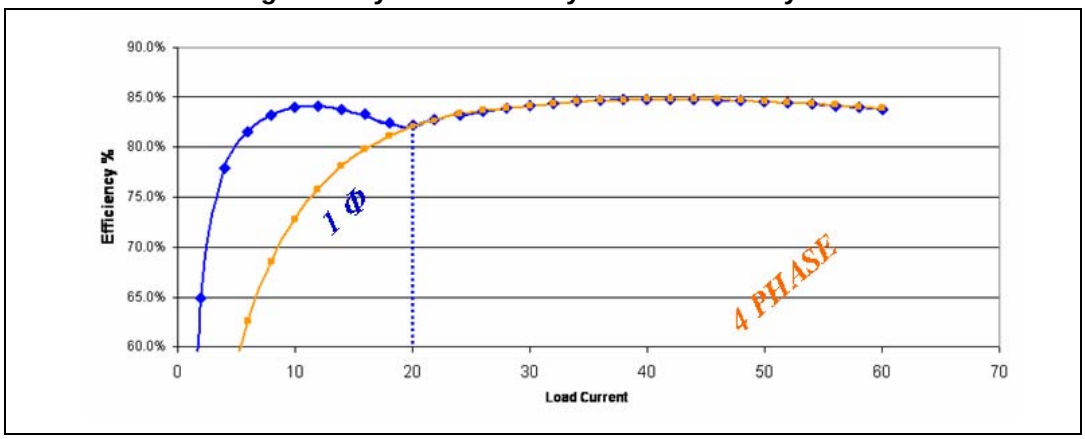
When the PSI_L flag is asserted by the CPU through the SVI bus, the device adjusts the phase number and interleaving according to the strategy programmed. Default strategy, when enabled, consists in working in single phase. PSI strategy can be disabled as well as re-configured through specific power manager I^2C commands. See *Section 6* for details.

In case the phase number is changed, the device will set HiZ on the related phase and re-configure internal phase-shift to maintain the interleaving. Furthermore, the internal current-sharing will be adjusted to consider the phase number reduction.

When PSI_L is de-asserted, the device will return to the original configuration. Start-up is performed with all the configured phases enabled. In case of on-the-fly VID transitions, the device will maintain the phase configuration set before.

NB section is not impacted by PSI_L status change. *Figure 8* shows an example of the efficiency improvement that can be achieved by enabling the PSI management.

Figure 8. System efficiency enhancement by PSI



5.4.4 HiZ management

L6717A is able to manage HiZ for internal drivers and for the external drivers through the PWMx signals. When the controller wants to set in high impedance the output of one section, it sets the relative PWM floating and, at the same time, turn OFF the embedded drivers of the related section.

5.4.5 Hardware jumper override - V_FIX

Anytime the pin VID0/V_FIX is driven high, the controller enters V_FIX mode.

When in V_FIX mode, both NB and CORE Section voltages are governed by the information shown in *Table 7*. Regardless of the state of PWROK, the device will work in SVI mode. SVC and SVD are considered as static VID and the output voltage will change according to their status. Dynamic SVC/SVD-change management is provided in this condition.

V_FIX mode is intended for system debug only.

Protection management differs in this case, see *Section 8.1* for details.

6 Power manager I²C

L6717A features a secondary power manager I²C bus to easy the implementation of power management features as well as overspeeding for “enthusiastic” users. The power manager I²C bus is operative after the PWRGOOD signal is driven high at the end of the soft-start.

Power manager I²C is a two wire, SCL (Clock) and SDA (Data), bus that connects a single master to one or more slaves (L6717A) separately addressable. The master initiates and terminates I²C transactions and drives the clock, SCL, and the data, SDA, during a transaction. The slave receives the I²C transactions and acts accordingly. Power manager I²C wire protocol is based on fast-mode I²C.

Power manager I²C Address configuration can be programmed through ADDR pin while I2CDIS pin allow disabling the bus See *Table 10*.

Power manager I²C and SVI bus are two independent buses working in parallel. In case two commends are issued in the same time on the two buses, L6717A performs them in the same time.

Table 10. Power manager I²C configuration

I2CDIS	ADDR	Description
3.3V	n/a	Power manager I²C disabled. SDA/OVP now becomes OVP to program the OV threshold for both Sections. SCL/OS now becomes OS to program offset for the CORE Section.
OPEN	3.3V	It sets I²C address to 1100111.
	OPEN	It sets I²C address to 1100110 (default).

6.1 Power manager commands

Power manager I²C master issues different command sequences to modify several parameters in the CORE section and/or the NB section of L6717A. In the same way, power manager I²C command are able to configure DPM and other power-saving-related features. During a *power manager command*:

- The bus master sends the start (START) sequence followed by the *Address* of the Controller which the *power manager command* applies. The bus master then sends the write (WRITE) bit. After the write bit, the voltage regulator (VR, L6717A) sends the acknowledge (ACK) bit.
- The bus master sends the command code during the *command phase*. The VR (L6717A) sends the acknowledge (ACK) bit after the command phase.
- The bus master sends the *data stream* related to the command phase previously issued (if applicable). The VR (L6717A) sends the acknowledge (ACK) bit after the data stream. Finally, the bus master sends the stop (STOP) sequence.
- After the VR (L6717A) has detected the STOP sequence, it performs operations according to the command issued by the bus master.

Refer to *Figure 9*, *Table 11* and *Table 12* for details.

Figure 9. Power manager I²C communication format

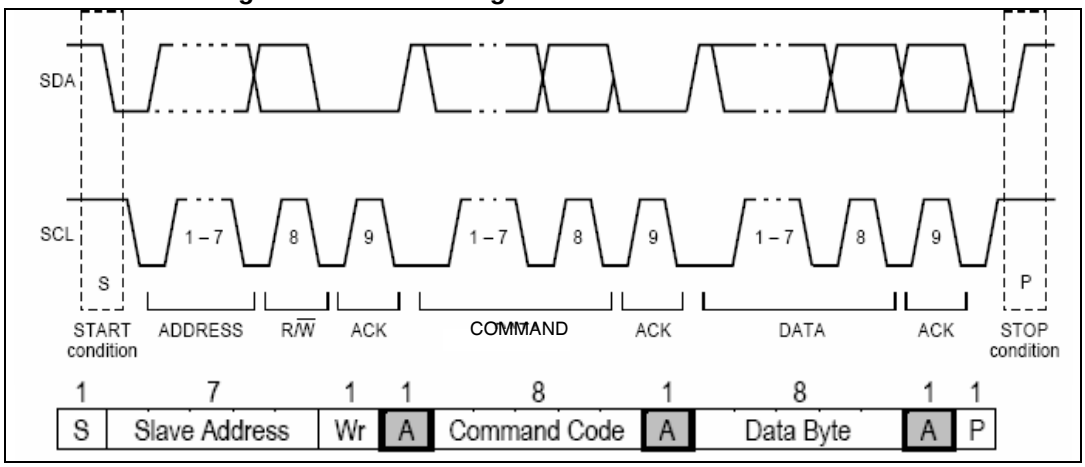


Table 11. Power manager I²C - address and command phase description

bits	Description
Address phase	
1:6	Always 110011b.
7	Slave address. According to ADDR connection, the device will act if addressed by 0b or 1b. Default address bit is 0b.
8	WRITE bit.
COMMAND PHASE	
1:3	Not applicable, ignored.
4:6	Command code
7, 8	Not applicable, ignored.

Table 12. Power manager I²C command phase and data stream

Command code [4:6]	Data stream [1:8]	Description
1CN	[1:2] xx [3] SIGN [4:8] OVRSPD	*OVERSPEEDING*: Adds a positive/negative offset to the regulation according to the SIGN bit with 50mV LSB and 5bit resolution. [3] SIGN: 1b for positive offset, 0b for negative offset. Negative offset is applicable only to CORE section (NB does not react to negative OS commad) [4:8] OVRSPD: 5bit code (4:LSB to 8:MSB), defines the offset to add to the already programmed reference (VID). Maximum CORE output voltage reachable is limited to 2.8V. Maximum NB output voltage reachable is limited by the Maximum NB Offset: +600mV (over VID) “CN” bits in *command code* address CORE section (“C” bit) or NB section (“N” bit) if set to 1b. Asserting both C and N bits will apply the command to both CORE and NB section. See *Table 13* for details about OVRSPD codification.
000	[1:4] xxxx [5:6] OV_NB [7:8] OV_CORE	*OV_SET*: Overvoltage threshold setup for CORE and/or NB sections. Sets the OV threshold above the programmed VID (including OVRSPD) in with three 200mV steps from + 250mV up to +850mV. [1:4]: ignored [5:6] OV_NB: *NorthBridge OVP*. 2bit code, defines the OV threshold for the NB section above the already programmed reference (VID). [7:8] OV_CORE: *Core OVP*. 2bit code, defines the OV threshold for the CORE section above the already programmed reference (VID). Default OV threshold is +250mV above reference for both sections. See *Table 14* for details about OV_SET codification.
001	[1:5] xxxxx [6:8] FSW	*FSW_ADJ:* Switching frequency adjustment. Modifies the switching frequency programmed through OSC pin according to FSW code by +/- 10% or +/-20%. [1:5]: ignored [6:8]: FSW: *Switching frequency adjustment*. 3 bits code to adjust the switching frequency with respect programmed voltage. See *Table 15* for details about FSW_ADJ codification.

Table 12. Power manager I²C command phase and data stream (continued)

Command code [4:6]	Data stream [1:8]	Description
010	[1:4] xxxx [5:6] k_{DRP} [7:8] k_{DRPNB}	*DRP_ADJ:* Droop function adjustment. Modifies the slope of the output voltage implemented through the droop function. [1:4]: ignored [5:6]: k_{DRP}. Defines the k_{DRP} factor for CORE section. [7:8]:k_{DRPNB}. Defines the k_{DRPNB} factor for NB section. Default value is k_{DRPx} = 1/4 for both sections. See *Table 16* for details about DRP_ADJ codification and *Section 7.3* and *Section 7.6* for LoadLine definition.
011	[1:3] 000b [4:5] DPMTH [6] PSI_A [7] PSI_EN [8] DPM_ON	*Power management flags:* Set of three flags to define power management actions of the controller. [1:3]: 000b. [4:5]: DPM Thresholds. Default is 00b. [6] PSI_A: *PSI Action*. It defines the action to take when PSI_L flag is asserted by SVI bus. The same action is considered by DPM. Send 0b to work in single phase (default) or 1b to work at two phases. [7] PSI_EN: *PSI Enable*. It enables or disables the PSI management. Set to 1b to manage PSI_L according to PSI_A or set to 0b (default) to ignore PSI_L flag sent through SVI bus. [8] DPM_ON: *Dynamic Phase Management*. It enables or disables the DPM mode. Set to 1b (default) to enable DPM or set to 0b to disable it. When enabled DPM acts automatically cutting phases according to PSI Action flag at light load. See *Section 6.2* for details about DPM.

6.1.1 Overspeeding command (OVRSPD)

This command allows adding a variable positive/negative offset to the reference programmed by the SVI bus in order to overspeed the CPU. L6717A allows adding up to 1.550 V in 50 mV steps to the reference.

The maximum possible output voltage is internally limited to 2.8 V. In case the SVI programmed reference plus the offset set through the OVRSPD command exceed this value, the reference for the regulation will default to 2.8 V.

The minimum possible output voltage is internally limited to 0.5 V. In case the SVI programmed reference minus the offset set through the OVRSPD command exceed this value, the reference for the regulation will default to 0.5 V.

Once the controller acknowledges the command and recognizes the OVRSPD command, the reference will step up or down until reaching the target offset performing a DVID transition. In case a new overspeed command is issued while the output voltage is not yet stabilized (i.e. the reference is still stepping to the target), the target is updated according to the new offset defined.

The command address both sections through two separate bits in the command code (“CN” bits - See *Table 12*). By asserting the relative bit, the subsequent data stream will apply to the identified section. Asserting both bits (CN = 11b) will address both sections. CN = 00b will be ignored regardless of the data stream provided.

See *Table 12* and *Table 13* for details about the codification of the command and the data stream.

Table 13. OVRSPD command - offset codification (1) (2)

Data stream [4:8]	Offset to reference [V]	Data stream [4:8]	Offset to reference [V]	Data stream [4:8]	Offset to reference [V]	Data stream [4:8]	Offset to reference [V]
00000	0.00	01000	0.40	10000	0.80	11000	1.20
00001	0.05	01001	0.45	10001	0.85	11001	1.25
00010	0.10	01010	0.50	10010	0.90	11010	1.30
00011	0.15	01011	0.55	10011	0.95	11011	1.35
00100	0.20	01100	0.60	10100	1.00	11100	1.40
00101	0.25	01101	0.65	10101	1.05	11101	1.45
00110	0.30	01110	0.70	10110	1.10	11110	1.50
00111	0.35	01111	0.75	10111	1.15	11111	1.55

1. Offset is added with an OTF VID transition above the already programmed VID.
2. Maximum regulated output voltage is internally limited to 2.8 Vmax/0.5 Vmin regardless the offset would let the IC regulate to higher/lower voltage.

6.1.2 Overvoltage threshold adjustment (OV_SET)

This command allows to adjust the overvoltage threshold independently for CORE and NB Sections. The threshold is adjustable, from the default value of +250 mV, in 200 mV steps up to +800 mV above the reference.

See *Table 12* and *Table 14* for details about the codification of the command and the data stream.

Table 14. OVP_SET command - threshold codification

Data stream [5:6] and [7:8]	OVP threshold [V]
00	+250mV (Default)
01	+400mV
10	+600mV
11	+800mV

6.1.3 Switching frequency adjustment (FSW_ADJ)

This command allows to adjust the switching frequency for the system in +/-10% steps across the main level defined by the OSC pin. Modifying the switching frequency may result in benefit for the application from a thermal point of view.

See *Table 12* and *Table 15* for details about the codification of the command and the data stream.

Table 15. FSW_ADJ command - switching frequency adjustment codification

Data stream [6:8]	Fsw adjustment	Data stream [6:8]	Fsw adjustment
000	Reset to frequency programmed by OSC	100	Reset to frequency programmed by OSC
001	-10%	101	+10%
010	-20%	110	+20%
011	Ignored	111	Ignored

6.1.4 Droop function adjustment (DRP_ADJ)

This command allows to adjust the slope for the output voltage load line once the external components are fixed by modifying the k_{DRP} and k_{DRPNB} parameters defined in *Section 7.3* and *Section 7.6*.

See *Table 12* and *Table 16* for details about the codification of the command and the data stream.

Table 16. DRP_ADJ command - droop function adjustment codification

Data stream [5:6] and [7:8]	DRP adjustment k_{DRP} and k_{DRPNB}
00	1/4
01	1/2
10	Droop disabled
11	

6.1.5 Power management flags

This command allows to set several flags to configure L6717A power management. The flags allows to define:

- PSI_A. This flag defines the strategy to adopt as a consequence of PSI_L assertion in the SVI command. It is possible to program the device to work in single phase (PSI_A = 0b - default) or two phase (PSI_A = 1b) when PSI_L is asserted through the SVI bus. The same strategy is used for DPM mode.
  See *Section 5.4.3* for details about PSI management and light-load efficiency optimizations. See *Section 6.2* for details about DPM.
- PSI_EN. This flag defines whether to enable or not the PSI_L management. Default is to manage PSI_L flag assertion through SVI bus (PSI_EN = 1b).
- DPM_ON. This flag defines whether to enable or not the DPM mode. The strategy adopted by DPM is defined through the PSI_A flag. See *Section 6.2* for details about DPM. DPM is disabled by default (DPM_ON = 0h).
- DPMTH. Allow to program up to 4 different strategies for DPM mode by properly adjusting the V_{DPM} threshold. See *Section 6.2* for details about DPM.

See *Table 12*, *Table 17* and *Table 19* for details about the codification of the Command and the Data Stream.

Table 17. Power management flags

Data Stream bit	Flag	Description
[1:3]	n/a	000b.
[4:5]	DPMTH	DPM threshold. Allow to define 4 different values for V_{DPM}. See *Section 6.2* for code/thresholds correspondence.
[6]	PSI_A	0b (default): IC working in single phase when PSI_L asserted. 1b:IC working in two phase when PSI_L asserted.
[7]	PSI_EN	0b (default): PSI_L flag in SVI ignored. 1b: PSI_L flag in SVI monitored and phase dropping enabled according to PSI_A.
[8]	DPM_ON	0b: DPM disabled. 1b (default): DPM enabled.

6.2 Dynamic phase management (DPM)

Dynamic phase management allows to adjust the number of working phases according to the delivered current still maintaining the benefits of the multiphase regulation.

Phase number is reduced by monitoring the voltage level across ILIM pin: L6717A reduces the number of working phase according to the strategy defined by the PSI_A flag when the voltage across ILIM pin is lower than V_{DPM}. In the same way, phase number is restored to the original value when the voltage across ILIM pin exceeds V_{DPM}.

V_{DPM} threshold is selected through the DPMTH command. See *Section 6.1*.

The current at which the transition happens (I_{DPM}) can be estimated as:

$$I_{DPM} = \frac{V_{DPM}}{R_{ILIM}} \cdot \frac{R_G}{DCR}$$

V_{DPM} thresholds are defined as a percentage of the voltage on ILIM pin corresponding to the thermal design current of the application.
1.8 V on ILIM pin corresponds to 100% of the load and DPM threshold are defined as a percentage of 1.8 V (see *Table 18* for details).
An hysteresis (5 % typ) is provided for each threshold in order to avoid multiple DPM actions triggering in steady load conditions.

Table 18. V_{DPM} thresholds (I_{LIM} rising - 5% hyst)

CODE	1/2 phase transition	2/3 phase transition	3/4 phase transition
00 (default)	15%	25%	40%
01	20%	30%	45%
10	25%	35%	50%
11	30%	40%	55%

DPM is enabled by default; to disable it proper command must be sent through the power manager I^2C bus. Once enabled, L6717A starts monitoring the ILIM voltage for phase

number modification after PWRGOOD rises to logic level “1”: the soft-start is then implemented in interleaving mode with all the available phases enabled.

DPM is reset in case of DVID transition, SVI command that affects the CORE Section and when LTB Technology® detects a load transient. After being reset, if the voltage across ILIM is compatible, DPM is re-enabled after proper delay.

Delay in the intervention of DPM can be adjusted by properly sizing the filer across ILIM pin. Increasing the capacitance results in increased delay in the DPM intervention.

Filter ILIM with 0.5 msec Typ.

Table 19. DPM, PSI and PSI_A Interactions

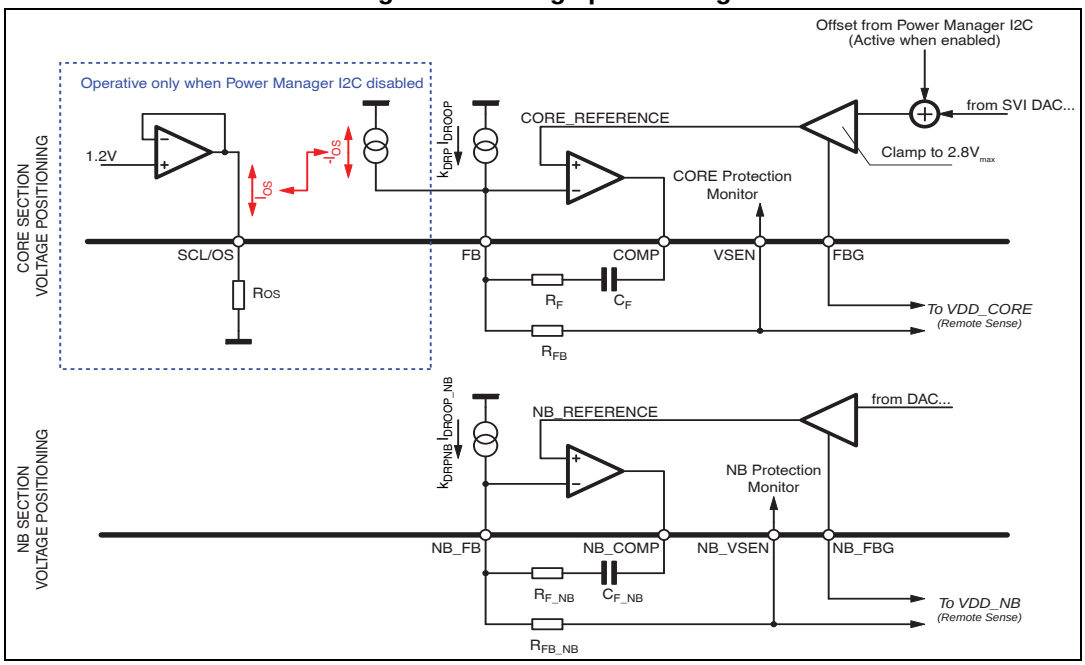
PSI_A	PSI_ON	DPM_ON	Working mode	Comments
0	0	1	FullDPM1	Automatic phase number adjustment (4/3/2/1) according to the load conditions. PSI flag is ignored. Default condition.
1	0	1	FullDPM2	Automatic phase number adjustment (4/3/2) according to the load conditions. PSI flag is ignored.
0	1	1	AutoPSI1	Automatic PSI according to the load conditions (4/1). PSI flag is ignored.
1	1	1	AutoPSI2	Automatic PSI according to the load conditions (4/2). PSI flag is ignored.
x	0	0	No Power Management	DPM OFF, AutoPSI OFF, PSI PFlag ignored.
0	1	0	PSI1	DPM and AutoPSI disabled. PSI Flag, when asserted, makes the IC working in single phase.
1	1	0	PSI2	DPM and AutoPSI disabled. PSI Flag, when asserted, makes the IC working in dual phase.

7 Output voltage positioning

Output voltage positioning is performed by selecting the controller operative-mode (*SVI, PVI* and *V_FIX*) and by programming the droop function and offset to the reference of both the sections (See *Figure 10*). The controller reads the current delivered by each section by monitoring the voltage drop across the DCR inductors. The current (I_{DROOP} / I_{DROOP_NB}) sourced from the FB / NB_FB pin, directly proportional to the read current, causes the related section output voltage to vary according to the external R_{FB} / R_{FB_NB} resistor so implementing the desired load-line effect.

L6717A embeds a dual Remote-Sense Buffer to sense remotely the regulated voltage of each Section without any additional external components. In this way, the output voltage programmed is regulated compensating for board and socket losses. Keeping the sense traces parallel and guarded by a power plane results in common mode coupling for any picked-up noise.

Figure 10. Voltage positioning



7.1 CORE section - phase # programming

CORE section implements a flexible 2 to 4 interleaved-phase converter. To program the desired number of phase, simply short to GND the PWMx signal that is not required to be used according to *Table 20*. For three phase operation, short PWM4 to GND while for two phase operation, short PWM3 and PWM4 to GND.

Caution: For the disabled phase(s), the current reading pins need to be properly connected to avoid errors in current-sharing and voltage-positioning: CSxP needs to be connected to the regulated output voltage while CSxN needs to be connected to CSxP through the same R_G resistor used for the active phases. See *Figure 2* and *Figure 3* for details in 3-phase and 2-phase connections.

Table 20. CORE section - phase number programming

Phase number	PWM3	PWM4
2	GND	GND
3	To Driver	GND
4	To Driver	To Driver

7.2 CORE section - current reading and current sharing loop

L6717A embeds a flexible, fully-differential current sense circuitry for the CORE section that is able to read across inductor parasitic resistance or across a sense resistor placed in series to the inductor element. The fully-differential current reading rejects noise and allows placing sensing element in different locations without affecting the measurement's accuracy. The trans-conductance ratio is issued by the external resistor R_G placed outside the chip between CSxN pin toward the reading points. The current sense circuit always tracks the current information, the pin CSxP is used as a reference keeping the CSxN pin to this voltage. To correctly reproduce the inductor current an R-C filtering network must be introduced in parallel to the sensing element. The current that flows from the CSxN pin is then given by the following equation (See *Figure 11*):

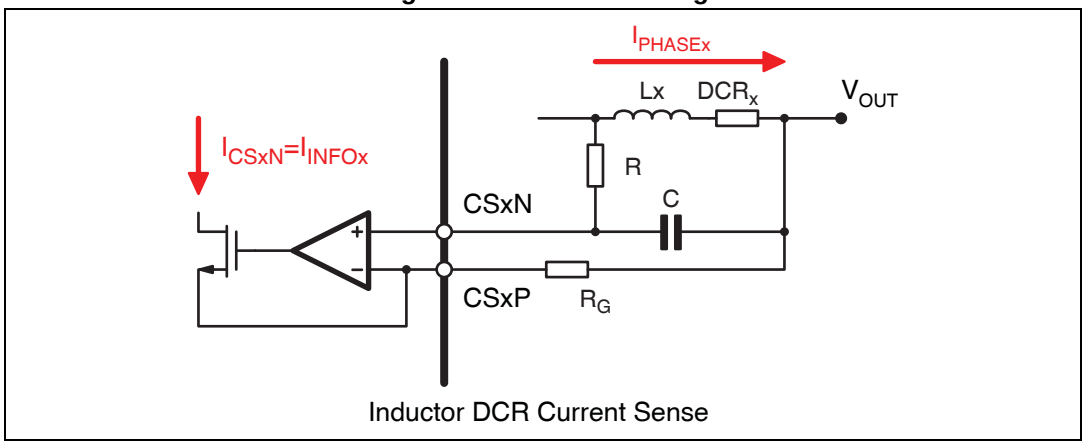
$$I_{CSxN} = \frac{DCR}{R_G} \cdot \frac{1 + s \cdot L/DCR}{1 + s \cdot R \cdot C} \cdot I_{PHASEx}$$

Considering now to match the time constant between the inductor and the R-C filter applied (Time constant mismatches cause the introduction of poles into the current reading network causing instability. In addition, it is also important for the load transient response and to let the system show resistive equivalent output impedance) it results:

$$\frac{L}{DCR} = R \cdot C \quad \Rightarrow \quad I_{CSxN} = \frac{R_L}{R_G} \cdot I_{PHASEx} = I_{INFOx}$$

R_G resistor is typically designed in order to have an information current I_{INFOx} in the range of about 35µA (I_{OCTH}) at the OC Threshold.

Figure 11. Current reading



The current read through the CSxP / CSxN pairs is converted into a current I_{INFOx} proportional to the current delivered by each phase and the information about the average current $I_{AVG} = \Sigma I_{INFOx} / N$ is internally built into the device (N is the number of working phases). The error between the read current I_{INFOx} and the reference I_{AVG} is then converted into a voltage that with a proper gain is used to adjust the duty cycle whose dominant value is set by the voltage error amplifier in order to equalize the current carried by each phase.

7.3 CORE section - defining load-line

L6717A introduces a dependence of the output voltage on the load current recovering part of the drop due to the output capacitor ESR in the load transient. Introducing a dependence of the output voltage on the load current, a static error, proportional to the output current, causes the output voltage to vary according to the sensed current.

Figure 11 shows the current sense circuit used to implement the load-line. The current flowing across the inductor(s) is read through the R - C filter across CSxP and CSxN pins. R_G programs a trans-conductance gain and generates a current I_{CSx} proportional to the current of the phase. The sum of the I_{CSx} current, with proper gain defined by the DRP_ADJ command (k_{DRP}), is then sourced by the FB pin ($k_{DRP}I_{DROOP}$). R_{FB} gives the final gain to program the desired load-line slope (*Figure 10*).

Time constant matching between the inductor (L / DCR) and the current reading filter (RC) is required to implement a real equivalent output impedance of the system so avoiding over and/or under shoot of the output voltage as a consequence of a load transient. See *Section 7.2*. The output characteristic vs. load current is then given by:

$$V_{CORE} = VID - R_{FB} \cdot k_{DRP} \cdot I_{DROOP} = VID - k_{DRP} \cdot R_{FB} \cdot \frac{DCR}{R_G} \cdot I_{OUT} = VID - R_{LL} \cdot I_{OUT}$$

Where R_{LL} is the resulting load-line resistance implemented by the CORE section. k_{DRP} value is determined by the power manager I^2C and its default value is 1/4.

R_{FB} resistor can be then designed according to the R_{LL} specifications and DRP_ADJ setting as follow:

$$R_{FB} = \frac{R_{LL}}{k_{DRP}} \cdot \frac{R_G}{DCR}$$

See *Section 6.2* for details about DRP_ADJ command.

7.4 CORE section - analog offset (Optional - I2CDIS = 3.3 V)

When power manager I^2C is disabled (I2CDIS = 3.3 V), L6717A still provide the way to add positive/negative offset to the CORE section. In this particular conditions, the pin SCL/OS becomes a virtual ground and allows programming a positive/negative offset (V_{OS}) for the CORE section output voltage by connecting a resistor R_{OS} to SGND/VCC. The pin is internally fixed at 1.240 V (2.0 V in case of negative offset, R_{OS} tied to VCC) so a current is programmed by connecting the resistor R_{OS} between the pin and SGND/VCC: this current is mirrored and then properly sunk/sourced from the FB pin as shown in *Figure 10*. Output voltage is then programmed as follow:

$$V_{CORE} = VID - R_{FB} \cdot (k_{DRP} \cdot I_{DROOP} - I_{OS})$$

Offset resistor can be designed by considering the following relationship (R_{FB} is be fixed by the droop effect):

$$R_{OS} = \frac{1.240V}{V_{OS}} \cdot R_{FB} \quad \text{(positive offset)}$$

$$R_{OS} = \frac{VCC - 2.0V}{V_{OS}} \cdot R_{FB} \quad \text{(negative offset)}$$

Caution: Offset implementation is optional, in case it is not desired, simply short the pin to GND.

Note: In the above formulas, R_{FB} has to be considered being the total resistance connected between FB pin and the regulated voltage. k_{DRP} has to be considered having its default value since power manager I^2C is disabled.

7.5 NB section - current reading

NB section performs the same differential current reading across DCR as the CORE Section. According to *Section 7.2*, the current that flows from the NB_CSN pin is then given by the following equation (See *Figure 11*):

$$I_{NB\_CSN} = \frac{DCR(NB)}{R_{G\_NB}} \cdot I_{NB} = I_{DROOP\_NB}$$

R_{G_NB} resistor is typically designed according to the OC threshold. See *Section 8.4* for details.

7.6 NB section - defining load-line

This method introduces a dependence of the output voltage on the load current recovering part of the drop due to the output capacitor ESR in the load transient. Introducing a dependence of the output voltage on the load current, a static error, proportional to the output current, causes the output voltage to vary according to the sensed current.

Figure 11 shows the current sense circuit used to implement the load-line. The current flowing across the inductor DCR is read through R_{G_NB}. R_{G_NB} programs a trans-conductance gain and generates a current I_{DROOP_NB} proportional to the current delivered by the NB section that is then sourced from the NB_FB pin with proper gain defined by the DRP_ADJ command (k_{DRPNB}). R_{FB_NB} gives the final gain to program the desired load-line

slope (*Figure 10*).

The output characteristic vs. load current is then given by:

$$V_{OUT\_NB} = VID - R_{FB\_NB} \cdot k_{DRPNB} \cdot I_{DROOP\_NB}$$

$$VID - R_{FB\_NB} \cdot k_{DRPNB} \cdot \frac{DCR}{R_{G\_NB}} \cdot I_{OUT} = VID - R_{LL\_NB} \cdot I_{OUT\_NB}$$

Where R_{LL_NB} is the resulting load-line resistance implemented by the NB section. k_{DRPNB} value is determined by the power manager I^2C and its default value is 1/4.

R_{FB_NB} resistor can be then designed according to the R_{LL_NB} specifications and DRP_ADJ setting as follow:

$$R_{FB\_NB} = \frac{R_{LL\_NB}}{k_{DRPNB}} \cdot \frac{R_{ISEN}}{R_{dsON}}$$

7.7 On-the-fly VID transitions

L6717A manages on-the-fly VID Transitions that allow the output voltage of both sections to modify during normal device operation for CPU power management purposes. OV, UV and PWRGOOD signals are masked during every OTF-VID Transition and they are re-activated with a 16 clock cycle delay to prevent from false triggering.

When changing dynamically the regulated voltage (OTF-VID), the system needs to charge or discharge the output capacitor accordingly. This means that an extra-current $I_{OTF\text{-}VID}$ needs to be delivered (especially when increasing the output regulated voltage) and it must be considered when setting the over current threshold of both the sections. This current results:

$$I_{OTF\text{-}VID} = C_{OUT} \cdot \frac{dV_{OUT}}{dT_{VID}}$$

where dV_{OUT} / dT_{VID} depends on the operative mode (7 mV/µsec. in SVI or externally driven in PVI).

Overcoming the OC threshold during the dynamic VID causes the device latch and disable.

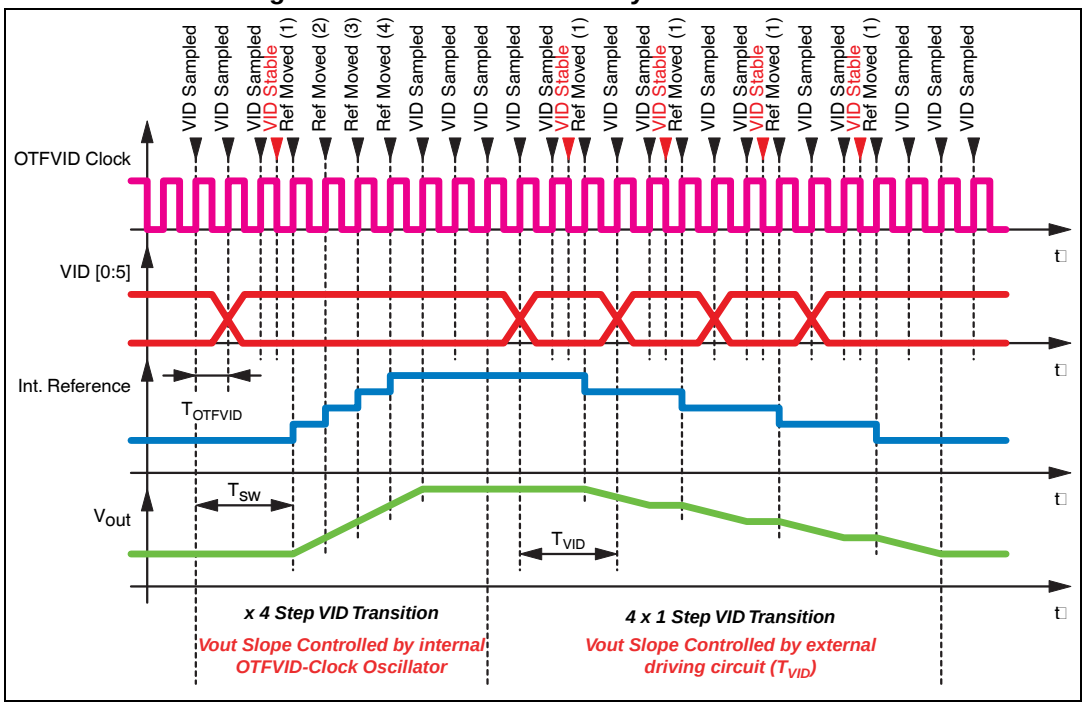
Dynamic VID transition is managed in different ways according to the device operative mode:

- PVI mode.

  L6717A checks for VID code modifications (See *Figure 12*) on the rising-edge of an internal additional OTFVID-clock and waits for a confirmation on the following falling edge. Once the new code is stable, on the next rising edge, the reference starts stepping up or down in LSB increments every two OTFVID-clock cycle until the new VID code is reached. During the transition, VID code changes are ignored; the device re-starts monitoring VID after the transition has finished on the next rising-edge available. OTFVID-clock frequency (F_{OTFVID}) is 500 kHz.

  If the new VID code is more than 1 LSB different from the previous, the device will execute the transition stepping the reference with the OTFVID-clock frequency F_{OTFVID} until the new code has reached. The output voltage rate of change will be of 12.5 mV / 4 µsec. = 3.125 mV/µsec.

Figure 12. PVI mode - on-the-fly VID transitions



- SVI mode.

  As soon as the controller receives a new valid command to set the VID level for one (or both) of the two sections, the reference of the involved section steps up or down according to the Target-VID with a 7 mV/µsec. slope (Typ). until the new VID code is reached.

  If a new valid command is issued during the transition, the device updates the Target-VID level and performs the on-the-fly transition up to the new code.Pre-PWROK Metal VID

  OTF-VID are not managed in this case because the *Pre-PWROK Metal VID* are stored after EN is asserted.

- V_FIX mode.

  L6717A checks for SVC/SVD modifications and, once the new code is stable, it steps the reference of both sections up or down according to the Target-VID with a 7 mV/µsec. slope (Typ). until the new VID code is reached.

OV, UV and PWRGOOD are masked during the transition and re-activated with a 16 clock cycle delay after the end of the transition to prevent from false triggering.

7.8 Soft-start

L6717A implements a soft-start to smoothly charge the output filter avoiding high in-rush currents to be required to the input power supply. In SVI mode, soft-start time is intended as the time required by the device to set the output voltages to the *Pre-PWROK Metal VID*. During this phase, the device increases the reference of the enabled section(s) from zero up to the programmed reference in closed loop regulation. Soft-start is implemented only when VCC is above UVLO threshold and the EN pin is set free. See *Section 5* for details about the SVI interface and how SVC/SVD are interpreted in this phase.

At the end of the digital soft-start, PWRGOOD signal is set free.

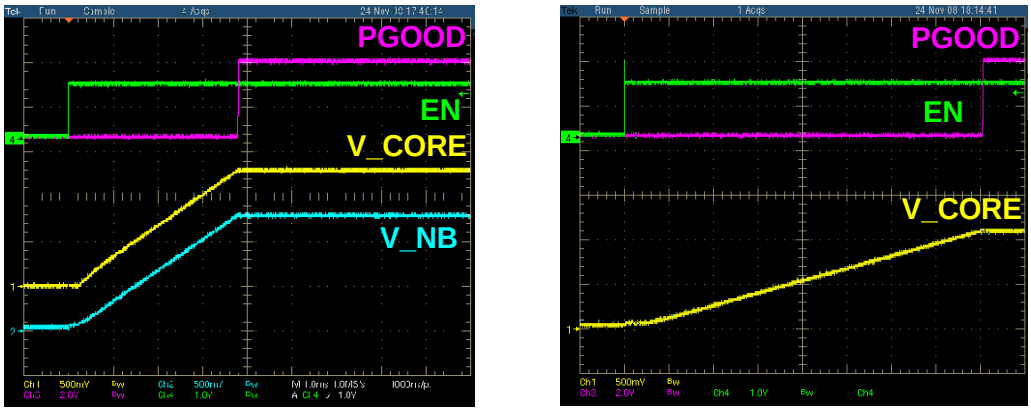
Protections are active during this phase as follow:

– Undervoltage is enabled when the reference voltage reaches 0.5 V.
– Overvoltage is always enabled according to the programmed threshold (by R_{OVP}).
– FBDisconnection is enabled.

Reference is increased with fixed dV/dt; Soft-Start time depends on the programmed voltage as follow:

$$T_{SS}[ms] = Target\_VID \cdot 2.56$$

Figure 13. System start-up: SVI (left) and PVI (right)



7.8.1 LS-Less start-up

In order to avoid any kind of negative undershoot on the load side during start-up, L6717A performs a special sequence in enabling the drivers for both sections: during the soft-start phase, the LS MOSFET is kept OFF (PWMx set to HiZ and ENDRV = 0) until the first PWM pulse. After the first PWM pulse, the PWMx outputs switches between logic “0” and logic “1” and ENDRV are set to logic “1”.

This particular sequence avoids the dangerous negative spike on the output voltage that can happen if starting over a pre-biased output especially when exiting from a CORE-OFF state.

Low-side MOSFET turn-on is masked only from the control loop point of view: protections are still allowed to turn-ON the low-side MOSFET in case of over voltage if needed.

8 Output voltage monitoring and protections

L6717A monitors the regulated voltage of both sections through pin VSEN and NB_VSEN in order to manage OV, UV and PWRGOOD. The device shows different thresholds when in different operative conditions but the behavior in response to a protection event is still the same as described below.

Protections are active also during soft-start (See *Section 7.8*) while they are masked during OTF-VID transitions with an additional delay to avoid false triggering.

Table 21.L6717A protection at a glance

L6717A	Section	
	CORE	**North bridge**
Overvoltage (OV)	*SVI / PVI:* +250mV above reference, programmable by power manager I^2C bus. I2CDIS = 3.3V: Programmable through SDA/OVP pin. *V_FIX:* Fixed to 1.8V. ***Action:*** IC latch; LS=ON & PWMx = 0 (if applicable); Other section (SVI only): HiZ; FLT driven high.	
Undervoltage (UV)	VSEN, NB_VSEN = VID -400mV. Active after Ref > 500mV ***Action:*** IC latch; both sections HiZ; FLT driven high.	
PWRGOOD	PWRGOOD is the logic AND between internal CORE and NB PGOOD in SVI mode while is the CORE section PGOOD in PVI mode. Each PGOOD is set to zero when the related voltage falls below the programmed reference -250mV. ***Action:*** Section(s) continue switching, PWRGOOD driven low.	
VSEN, NB_VSEN disconnection	Set when VSEN > CS1N +600mV. ***Action:*** UV-Like	Set when VSEN > NB_CSN +600mV. ***Action:*** UV-Like (SVI only)
FBG, NB_FBG disconnection	Internal comparator across the opamp to recover from GND losses. ***Action:*** UV-Like	
Overcurrent (OC)	Current monitor across inductor DCR. Dual protection, per-phase and average. ***Action:*** UV-Like	Current monitor across inductor DCR. Constant current. ***Action:*** UV-Like
On-the-fly VID	Protections masked with the exception of OC with additional 16 clock delay to prevent from false triggering (both SVI and PVI).	

8.1 Programmable overvoltage (I2DIS = 3.3 V)

When power manager I^2C is disabled, L6717A provides the possibility to adjust OV threshold (common for both Sections) through the SDA/OVP pin. Connecting the pin to SGND through a resistor R_{OVP}, the OVP threshold becomes the voltage present at the pin. Since the SDA/OVP pin sources a constant I_{OVP}=10µA current, the programmed over voltage threshold will be $OVP_{TH}=R_{OVP}*10\mu A$.

When the voltage sensed by VSEN and/or NB_VSEN overcomes the OV threshold, the controller:

- Permanently sets the PWM of the involved section to zero keeping ENDRV of that section high in order to keep all the Low-Side MOSFETs on to protect the load of the Section in OV condition.
- Permanently sets the PWM of the non-involved section to HiZ while keeping ENDRV of the non-involved section low in order to realize an HiZ condition of the non-involved section.
- Drives the OSC/ FLT pin high.
- Power supply or EN pin cycling is required to restart operations.

Filter OVP pin with 100 pF(typ) to SGND.

8.2 Feedback disconnection

L6717A provides both CORE and NB sections with FB disconnection protection. This feature acts in order to stop the device from regulating dangerous voltages in case the remote sense connections are left floating. The protection is available for both the sections and operates for both the positive and negative sense.

According to *Figure 14*, the protection works as follow:

- CORE section:

  Positive sense is performed monitoring the CORE output voltage through both VSEN and CS1N. As soon as CS1N is more than 600 mV higher than VSEN, the device latches in HiZ. FLT pin is driven high. A 50 µA pull-down current on the VSEN forces the device to detect this fault condition.

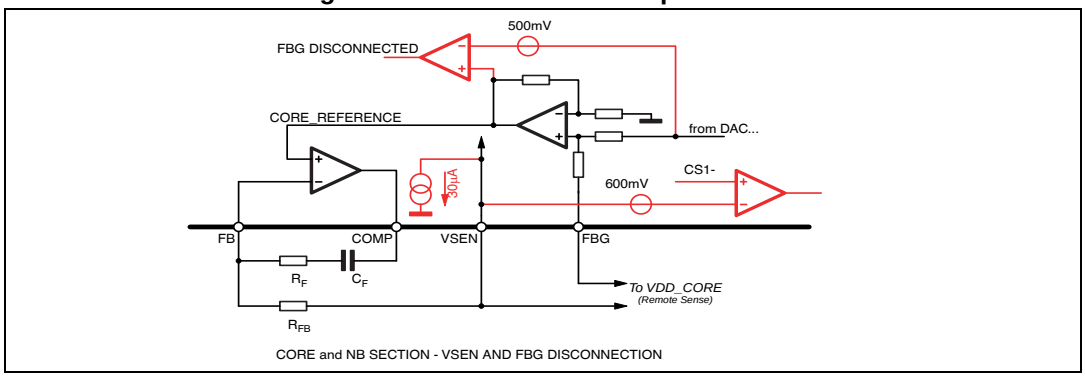
  Negative sense is performed monitoring the internal opamp used to recover the GND losses by comparing its output and the internal reference generated by the DAC. As soon as the difference between the output and the input of this opamp is higher than 500 mV, the device latches in HiZ. FLT pin is driven high.
- NB section (SVI only)

  Positive sense is performed monitoring the NB output voltage through both NB_VSEN and NB_CSN. As soon as NB_CSN is more than 600 mV higher than NB_VSEN, the device latches in HiZ. FLT pin is driven high. A 50 µA pull-down current on the NB_VSEN forces the device to detect this fault condition.

  Negative sense is performed monitoring the internal opamp used to recover the GND losses by comparing its output and the internal reference generated by the DAC. As soon as the difference between the output and the input of this opamp is higher than 500 mV, the device latches in HiZ. FLT pin is driven high.

To recover from a latch condition, cycle VCC or EN.

Figure 14. FB disconnection protection



8.3 PWRGOOD

It is an open-drain signal set free after the soft-start sequence has finished; it is the logic AND between the internal CORE and NB PGOOD (or just the CORE PGOOD in PVI mode). It is pulled low when the output voltage of one of the two sections drops 250 mV below the programmed voltage. It is masked during on-the-fly VID transitions as well as when the CORE section is set to OFF (from SVI bus) while the NB section is still operative.

8.4 Overcurrent

The Overcurrent threshold has to be programmed to a safe value, in order to be sure that each section doesn't enter OC during normal operation of the device. This value must take into consideration also the extra current needed during the OTF-VID Transition ($I_{OTF-VID}$) and the process spread and temperature variations of the sensing elements (Inductor DCR).

Moreover, since also the internal threshold spreads, the design has to consider the minimum/maximum values of the threshold. Considering the reading method, the two sections will show different behaviors in OC.

8.4.1 CORE section

L6717A performs two different OC protections for the CORE section: it monitors both the total current and the per-phase current and allows to set an OC threshold for both.

- Per-Phase OC.
  Maximum information current per-phase (I_{INFOx}) is internally limited to 35 µA. This end-of-scale current (I_{OC_TH}) is compared with the information current generated for each phase (I_{INFOx}). If the current information for the single phase exceed the end-of-scale current (i.e. if $I_{INFOx} > I_{OC\_TH}$), the device will turn-on the LS MOSFET until the threshold is re-crossed (i.e. until $I_{INFOx} < I_{OC\_TH}$). After 4 consecutive events, the IC latches with all the MOSFETs of all the sections OFF (HiZ).
- Total current OC.
  ILIM pin allows to define a maximum total output current for the system (I_{OC_TOT}). I_{LIM} current is sourced from the ILIM pin (not altered by DRP_ADJ command). By connecting a resistor R_{ILIM} to SGND, a load indicator with 2.5V (V_{OC_TOT}) end-of-scale can be implemented. When the voltage present at the ILIM pin crosses

V_{OC_TOT}, the device detects an OC and immediately latches with all the MOSFETs of all the sections OFF (HiZ).

Typical design considers the intervention of the total current OC before the Per-Phase OC, leaving this last one as an extreme-protection in case of hardware failures in the external components. Typical design flow is the following:

- Define the maximum total output current (I_{OC_TOT}) according to system requirements
- Design Per-Phase OC and R_G resistor in order to have $I_{INFOx} = I_{OC\_TH}$ (35µA) when I_{OUT} is about 10% higher than the I_{OC_TOT} current. It results:

$$R_G = \frac{(1.1 \cdot I_{OC\_TOT}) \cdot DCR}{N \cdot I_{OCTH}}$$

where N is the number of phases and DCR the DC resistance of the inductors. R_G should be designed in worst-case conditions.

- Design the total current OC and R_{ILIM} in order to have the ILIM pin voltage to V_{OC_TOT} at the desired maximum current I_{OC_TOT}. It results:

$$R_{ILIM} = \frac{V_{OC\_TOT} \cdot R_G}{I_{OC\_TOT} \cdot DCR} \qquad \left(I_{LIM} = \frac{DCR}{R_G} \cdot I_{OUT}\right)$$

where V_{OC_TOT} is typically 2.5V and I_{OC_TOT} is the total current OC threshold desired.

- Adjust the defined values according to bench-test of the application.
- An additional capacitor in parallel to R_{ILIM} can be considered to add a delay in the protection intervention.

Note: What previously listed is the typical design flow. Custom design and specifications may require different settings and ratios between the Per-Phase OC threshold and the total current OC threshold. Applications with huge ripple across inductors may be required to set Per-Phase OC to values different than 110%: design flow should be modified accordingly.

DRP_ADJ command from power manager I^2C does not alter the current information used for Per-Phase OC and total current OC.

8.4.2 IddSpike and IddTDC support

L6717A supports G34 processors and as a consequence, allows dual level OCP supporting IddSpike and IddTDC (refer to CPU related documents for details about IddSpike and IddTDC levels).

Proper design of the per-phase and Total Current OC is required to meet these specifications:

- per-phase OC is used to face with IddSpike: set to 120% (Typ) of IddSpike;
- Total current OC is used to face with IddTDC: set to 120% (Typ) of IddTDC and provide proper filtering.

G34 design flow is the following:

- Define the maximum total output current (I_{OC_TOT}) according to system requirements: I_{OC_TOT} = 120% x IddTDC (Typ)
- Design Per-Phase OC and R_G resistor in order to have $I_{INFOx} = I_{OC\_TH}$ (35 µA) when I_{OUT} is 120% higher than the IddSpike current. It results:

$$R_G = \frac{(1.2 \cdot IddSpike) \cdot DCR}{N \cdot I_{OCTH}}$$

where N is the number of phases and DCR the DC resistance of the inductors. R_G should be designed in worst-case conditions.

- Design the total current OC and R_{ILIM} in order to have the ILIM pin voltage to V_{OC_TOT} at the desired maximum current I_{OC_TOT}. It results:

$$R_{ILIM} = \frac{V_{OC\_TOT} \cdot R_G}{I_{OC\_TOT} \cdot DCR} = \frac{V_{OC\_TOT} \cdot R_G}{1.2 \cdot IddTDC \cdot DCR} \qquad \left(I_{LIM} = \frac{DCR}{R_G} \cdot I_{OUT}\right)$$

where V_{OC_TOT} is typically 2.5 V and I_{OC_TOT} = 120% x IddTDC is the Total Current OC threshold desired.

- Provide filtering capacitor for ILIM pin in order to properly filter IddSpike (1.5 mSec Typ time-constant).
- Adjust the defined values according to bench-test of the application.

8.4.3 NB section

NB Section performs per-phase over current: its maximum information current (I_{INFO_NB}) is internally limited to I_{OCTH_NB} (35µA typ). If the current information for the NB phase exceeds the end-of-scale current (i.e. if $I_{INFO\_NB} > I_{OCTH\_NB}$), the device will turn-on the Low-Side MOSFET, also skipping clock cycles, until the threshold is re-crossed (i.e. until $I_{INFO\_NB} < I_{OCTH\_NB}$). After exiting the OC condition, the low-side MOSFET is turned off and the high-side is turned on with a duty cycle driven by the PWM comparator.

Design R_{G_NB} resistor in order to have $I_{DROOP\_NB} = I_{OCTH\_NB}$ (35µA) at the I_{OC_NBmax} current. It results:

$$R_G = \frac{I_{OC\_NBmax} \cdot DCR}{I_{OCTH\_NB}}$$

Note: DRP_ADJ command from power manager I^2C does not alter the current information used for Per-Phase OC.

9 Main oscillator

The controller embeds a dual-oscillator: one section is used for the CORE and it is a multiphase programmable oscillator managing equal phase-shift among all phases and the other section is used for the NB section. Phase-shift between the CORE and NB ramps is automatically adjusted according to the CORE phase # programmed.

The internal oscillator generates the triangular waveform for the PWM charging and discharging with a constant current an internal capacitor. The switching frequency for each channel, F_{SW}, is internally fixed at 200 kHz: the resulting switching frequency for the CORE section at the load side results in being multiplied by N (number of configured phases).

The current delivered to the oscillator is typically 20 µA (corresponding to the free running frequency F_{SW}=200 kHz) and it may be varied using an external resistor (R_{OSC}) typically connected between the OSC pin and SGND. Since the OSC pin is fixed at 1.240 V, the frequency is varied proportionally to the current sunk from the pin considering the internal gain of 10 kHz/µA (See *Figure 15*).

Connecting R_{OSC} to SGND the frequency is increased (current is sunk from the pin), according to the following relationships:

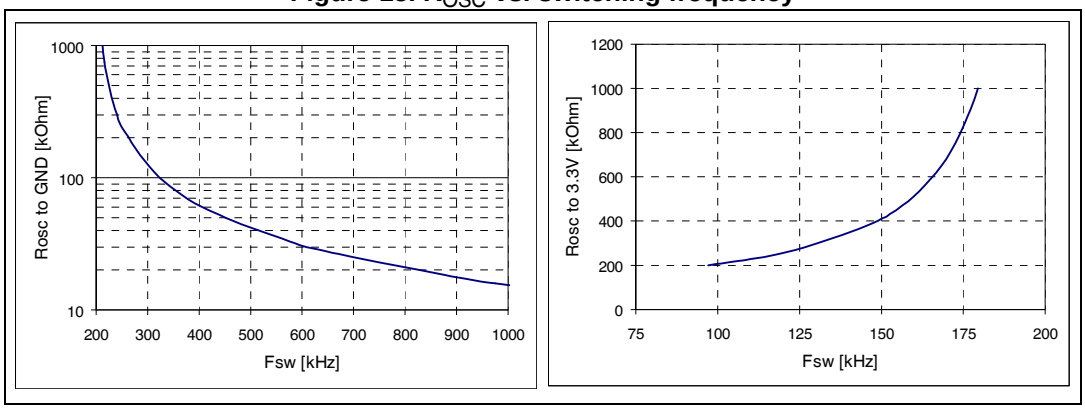
$$F_{SW} = 200kHz + \frac{1.240V}{R_{OSC}} \cdot 10\frac{kHz}{\mu A}$$

Connecting R_{OSC} to a positive voltage the frequency is reduced (current is forced into the pin), according to the following relationships:

$$F_{SW} = 200kHz - \frac{+V - 1.240}{R_{OSC}} \cdot 10\frac{kHz}{\mu A}$$

where +V is the positive voltage which the R_{OSC} resistor is connected.

Figure 15. R_{OSC} vs. switching frequency



10 High current embedded drivers

L6717A provides high-current driving control for CORE and NB sections. The driver for the high-side MOSFET use BOOTx pin for supply and PHASEx pin for return. The driver for the low-side MOSFET use the VCCDR pin for supply and GND pin for return.

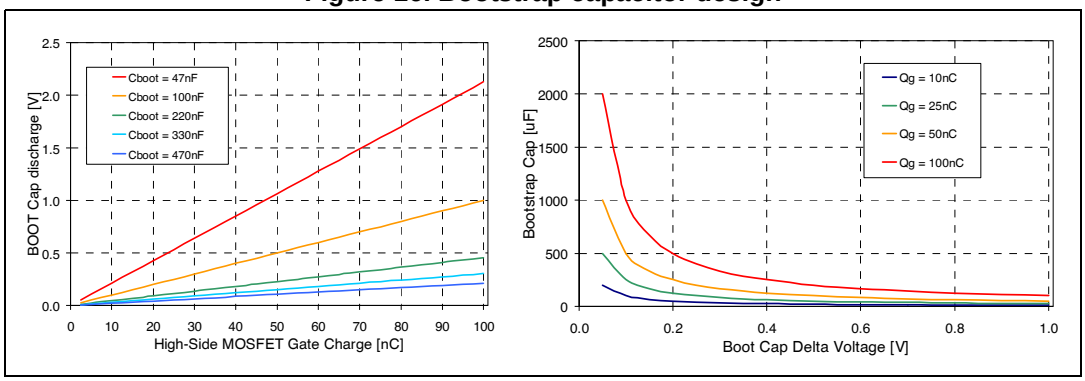
The embedded driver embodies an anti-shoot-through and adaptive dead-time control to minimize low-side body diode conduction time maintaining good efficiency saving the use of Schottky diodes: when the high-side MOSFET turns off, the voltage on its source begins to fall; when the voltage reaches about 2 V, the low-side MOSFET gate drive voltage is suddenly applied. When the low-side MOSFET turns off, the voltage at LGATE pin is sensed. When it drops below about 1 V, the high-side MOSFET gate drive voltage is suddenly applied. If the current flowing in the inductor is negative, the source of high-side MOSFET will never drop. To allow the low-side MOSFET to turn-on even in this case, a watchdog controller is enabled: if the source of the high-side MOSFET doesn't drop, the low-side MOSFET is switched on so allowing the negative current of the inductor to recirculate. This mechanism allows the system to regulate even if the current is negative.

10.1 Boot capacitor design

Bootstrap capacitor needs to be designed in order to show a negligible discharge due to the high-side MOSFET turn-on. In fact it must give a stable voltage supply to the high-side driver during the MOSFET turn-on also minimizing the power dissipated by the embedded boot diode. *Figure 16* gives some guidelines on how to select the capacitance value for the bootstrap according to the desired discharge and depending on the selected MOSFET.

To prevent bootstrap capacitor to extra-charge as a consequence of large negative spikes, an external series resistance R_{BOOT} (in the range of few ohms) may be required in series to BOOT pin.

Figure 16. Bootstrap capacitor design



10.2 Power dissipation

It is important to consider the power that the device is going to dissipate in driving the external MOSFETs in order to avoid overcoming the maximum junction operative temperature.

Two main terms contribute in the device power dissipation: bias power and drivers' power.

- Device power (P_{DC}) depends on the static consumption of the device through the supply pins and it is simply quantifiable as follow:

  $$P_{DC} = V_{CC} \cdot I_{CC} + V_{VCCDR} \cdot I_{VCCDR}$$

- Drivers' power is the power needed by the driver to continuously switch ON and OFF the external MOSFETs; it is a function of the switching frequency and total gate charge of the selected MOSFETs. It can be quantified considering that the total power P_{SW} dissipated to switch the MOSFETs dissipated by three main factors: external gate resistance (when present), intrinsic MOSFET resistance and intrinsic driver resistance. This last term is the important one to be determined to calculate the device power dissipation.

  The total power dissipated to switch the MOSFETs for each phase featuring embedded driver results:

  $$P_{SWx} = F_{SW} \cdot (Q_{GHSx} \cdot VCCDR + Q_{GLSx} \cdot VBOOTx)$$

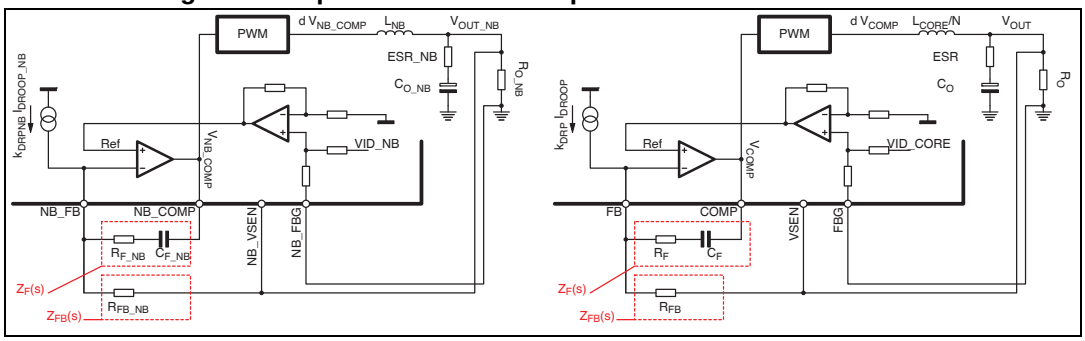
  Where Q_{GHSx} is the total gate charge of the HS MOSFETs and Q_{GLSx} is the total gate charge of the LS MOSFETs for both CORE and NB sections (only Phase1 and Phase2 for CORE section); VBOOTx is the driving voltage for the HSx MOSFETs.

11 System control loop compensation

The device embeds two separate and independent control loops for CORE and NB section. The control loop for NB section is a simple Voltage-Mode control loop with (optional) voltage positioning featured when DROOP pin is shorted with FB. The control loop for the CORE section also features a current-sharing loop to equalize the current carried by each of the configured phases.

The CORE control system can be modeled with an equivalent single-phase converter whose only difference is the equivalent inductor L/N (where each phase has an L inductor and N is the number of the configured phases). See *Figure 17*.

Figure 17. Equivalent control loop for NB and CORE sections



This means that the same analysis can be used for both the sections with the only exception of the different equivalent inductor value ($L=L_{NB}$ for NB Section and $L=L_{CORE}/N$ for the CORE section) and the current reading gain (DCR/R_{G_NB} for NB Section and DCR/R_G for the CORE section).

The control loop gain results (obtained opening the loop after the COMP pin):

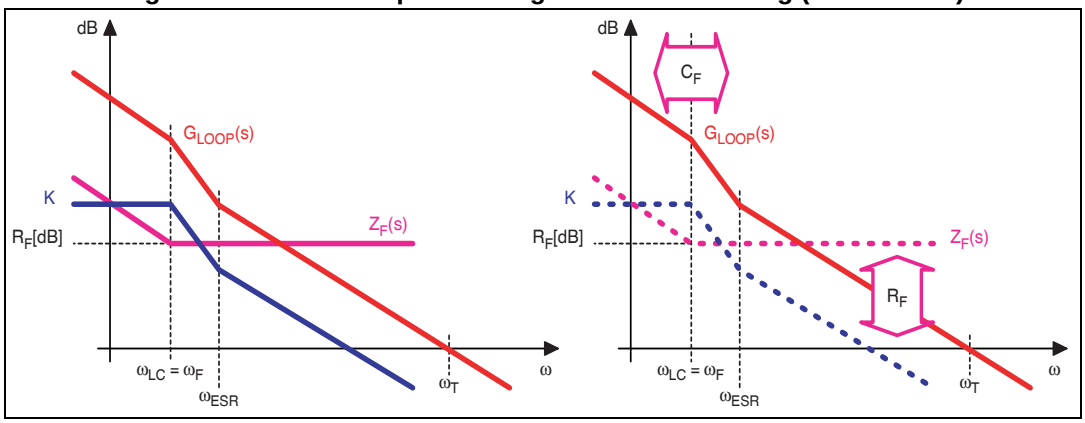
$$G_{LOOP}(s) = -\frac{PWM \cdot Z_F(s) \cdot (R_{LL} + Z_P(s))}{[Z_P(s) + Z_L(s)] \cdot \left[\frac{Z_F(s)}{A(s)} + \left(1 + \frac{1}{A(s)}\right) \cdot R_{FB}\right]}$$

Where:

- R_{LL} is the equivalent output resistance determined by the droop function;
- $Z_P(s)$ is the impedance resulting by the parallel of the output capacitor (and its ESR) and the applied load R_O;
- $Z_F(s)$ is the compensation network impedance;
- $Z_L(s)$ is the equivalent inductor impedance;
- $A(s)$ is the error amplifier gain;
- $PWM = \frac{3}{5} \cdot \frac{V_{IN}}{\Delta V_{OSC}}$ is the PWM transfer function.

The control loop gain for each section is designed in order to obtain a high DC gain to minimize static error and to cross the 0dB axes with a constant -20dB/Dec. slope with the desired crossover frequency ω_T. Neglecting the effect of $Z_F(s)$, the transfer function has one zero and two poles; both the poles are fixed once the output filter is designed (LC filter resonance ω_{LC}) and the zero (ω_{ESR}) is fixed by ESR and the droop resistance.

Figure 18. Control loop bode diagram and fine tuning (not in scale)



To obtain the desired shape an R_F-C_F series network is considered for the $Z_F(s)$ implementation. A zero at $\omega_F=1/R_FC_F$ is then introduced together with an integrator. This integrator minimizes the static error while placing the zero ω_F in correspondence with the L-C resonance assures a simple -20dB/Dec. shape of the gain.

In fact, considering the usual value for the output filter, the LC resonance results to be at frequency lower than the above reported zero.

Compensation network can be simply designed placing $\omega_F=\omega_{LC}$ and imposing the cross-over frequency ω_T as desired obtaining (always considering that ω_T might be not higher than 1/10th of the switching frequency F_{SW}):

$$R_F = \frac{R_{FB} \cdot \Delta V_{OSC}}{V_{IN}} \cdot \frac{3}{5} \cdot \omega_T \cdot \frac{L}{N \cdot (R_{LL} + ESR)}$$

$$C_F = \frac{\sqrt{C_O \cdot L}}{R_F}$$

11.1 Compensation network guidelines

The compensation network design assures to having system response according to the cross-over frequency selected and to the output filter considered: it is anyway possible to further fine-tune the compensation network modifying the bandwidth in order to get the best response of the system as follow (See *Figure 18*):

- Increase R_F to increase the system bandwidth accordingly;
- Decrease R_F to decrease the system bandwidth accordingly;
- Increase C_F to move ω_F to low frequencies increasing as a consequence the system phase margin.

Having the fastest compensation network gives not the confidence to satisfy the requirements of the load: the inductor still limits the maximum dI/dt that the system can afford. In fact, when a load transient is applied, the best that the controller can do is to “saturate” the duty cycle to its maximum (d_{MAX}) or minimum (0) value. The output voltage dV/dt is then limited by the inductor charge / discharge time and by the output capacitance. In particular, the most limiting transition corresponds to the load removal since the inductor results being discharged only by V_{OUT} (while it is charged by $d_{MAX}V_{IN}$-V_{OUT} during a load appliance).

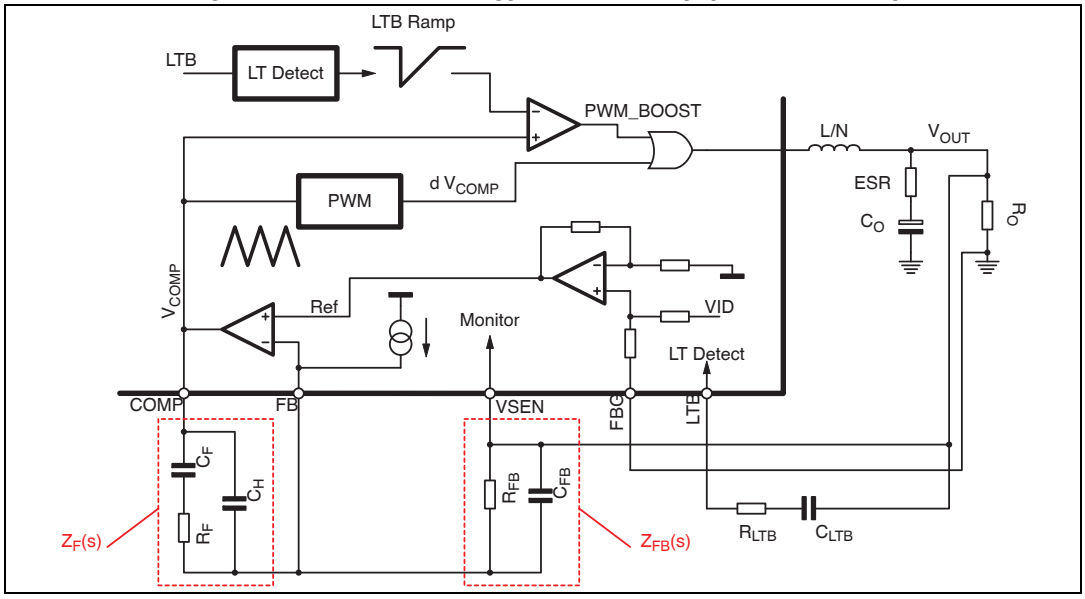
12 LTB Technology®

LTB Technology® further enhances the performance of dual-edge asynchronous systems by reducing the system latencies and immediately turning ON all the phases to provide the correct amount of energy to the load. By properly designing the LTB network as well as the LTB gain, the undershoot and the ring-back can be minimized also optimizing the output capacitors count. LTB Technology® applies only to the CORE Section.

LTB Technology® monitors the output voltage through a dedicated pin detecting load-transients with selected dV/dt, it cancels the interleaved phase-shift, turning-on simultaneously all phases. it then implements a parallel, independent loop that reacts to load-transients bypassing E/A latencies.

LTB Technology® control loop is reported in *Figure 19*.

Figure 19. LTB Technology® control loop (CORE section)



The LTB detector is able to detect output load transients by coupling the output voltage through an R_{LTB} - C_{LTB} network. After detecting a load transient, the LTB Ramp is reset and then compared with the COMP pin level. The resulting duty-cycle programmed is then OR-ed with the PWMx signal of each phase by-passing the main control loop. All the phases will then be turned-on together and the EA latencies results bypassed as well.
Sensitivity of the load transient detector can be programmed in order to control precisely both the undershoot and the ring-back.
R_{LTB} - C_{LTB} is designed according to the output voltage deviation dV_{OUT} which is desired the controller to be sensitive as follow:

$$R_{LTB} = \frac{dV_{OUT}}{25\mu A} \qquad C_{LTB} = \frac{1}{2\pi \cdot N \cdot R_{LTB} \cdot F_{SW}}$$

LTB technology® design tips.

- Decrease R_{LTB} to increase the system sensitivity making the system sensitive to smaller dV_{OUT}.
- Increase C_{LTB} to increase the system sensitivity making the system sensitive to higher dV/dt.

13 Layout guidelines

Layout is one of the most important things to consider when designing high current applications. A good layout solution can generate a benefit in lowering power dissipation on the power paths, reducing radiation and a proper connection between signal and power ground can optimize the performance of the control loops.

Two kind of critical components and connections have to be considered when laying-out a VRM based on L6717A: power components and connections and small signal components connections.

13.1 Power components and connections

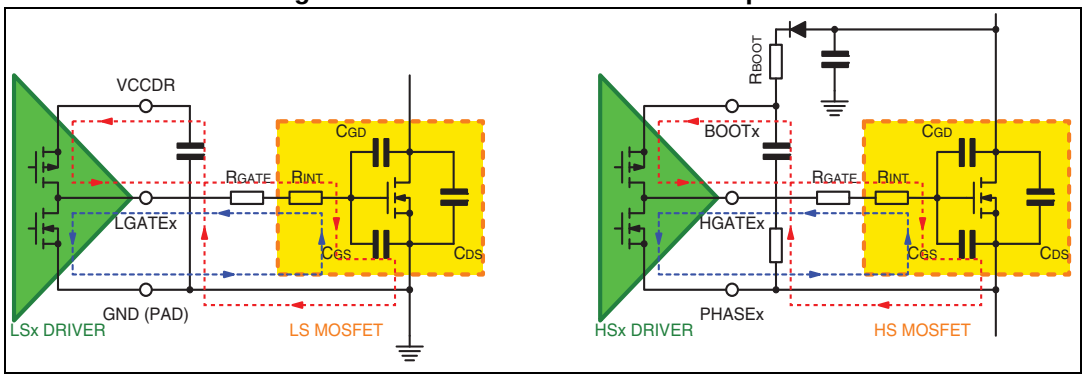
These are the components and connections where switching and high continuous current flows from the input to the load. The first priority when placing components has to be reserved to this power section, minimizing the length of each connection and loop as much as possible. To minimize noise and voltage spikes (EMI and losses) these interconnections must be a part of a power plane and anyway realized by wide and thick copper traces: loop must be anyway minimized. The critical components, i.e. the power transistors, must be close one to the other. The use of multi-layer printed circuit board is recommended.

Traces between the driver section and the MOSFETs should be wide to minimize the inductance of the trace so minimizing ringing in the driving signals. Moreover, VIAs count needs to be minimized to reduce the related parasitic effect.

Locate the bypass capacitor (VCC, VCCDR and BOOT capacitors) close to the device with the shortest possible loop and use wide copper traces to minimize parasitic inductance.

Systems that do not use Schottky diodes in parallel to the low-side MOSFET might show big negative spikes on the phase pin. This spike can be limited as well as the positive spike but it causes the bootstrap capacitor to be over-charged. This extra-charge can cause, in the worst case condition of maximum input voltage and during particular transients, that boot-to-phase voltage overcomes the abs.max.ratings also causing device failures. It is then suggested in this cases to limit this extra-charge by adding a small resistor R_{BOOT} in series to the boot capacitor or the boot diode. The use of R_{BOOT} also contributes in the limitation of the spike present on the BOOT pin.

Figure 20. Driver turn-on and turn-off paths



For heat dissipation, place copper area under the IC. This copper area must be connected with internal copper layers through several VIAs to improve the thermal conductivity. The

combination of copper pad, copper plane and VIAs under the controller allows the device to reach its best thermal performance.

13.2 Small signal components and connections

These are small signal components and connections to critical nodes of the application as well as bypass capacitors for the device supply. Locate the bypass capacitor close to the device and refer sensible components such as frequency set-up resistor R_{OSC}, offset resistor and OVP resistor R_{OVP} to SGND (when applicable). Star grounding is suggested: use the device exposed PAD as a connection point.

VSEN pin filtered vs. SGND helps in reducing noise injection into device and EN pin filtered vs. SGND helps in reducing false trip due to coupled noise: take care in routing driving net for this pin in order to minimize coupled noise.

Remote buffer connection must be routed as parallel nets from the FBG/FBR pins to the load in order to avoid the pick-up of any common mode noise. Connecting these pins in points far from the load will cause a non-optimum load regulation, increasing output tolerance.

Locate current reading components close to the device. The PCB traces connecting the reading point must use dedicated nets, routed as parallel traces in order to avoid the pick-up of any common mode noise. It's also important to avoid any offset in the measurement and, to get a better precision, to connect the traces as close as possible to the sensing elements. Symmetrical layout is also suggested. Small filtering capacitor can be added, near the controller, between V_{OUT} and SGND, on the CSxN line when reading across inductor to allow higher layout flexibility.

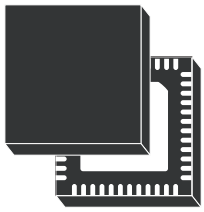
14 VFQFPN48 mechanical data and package dimensions

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

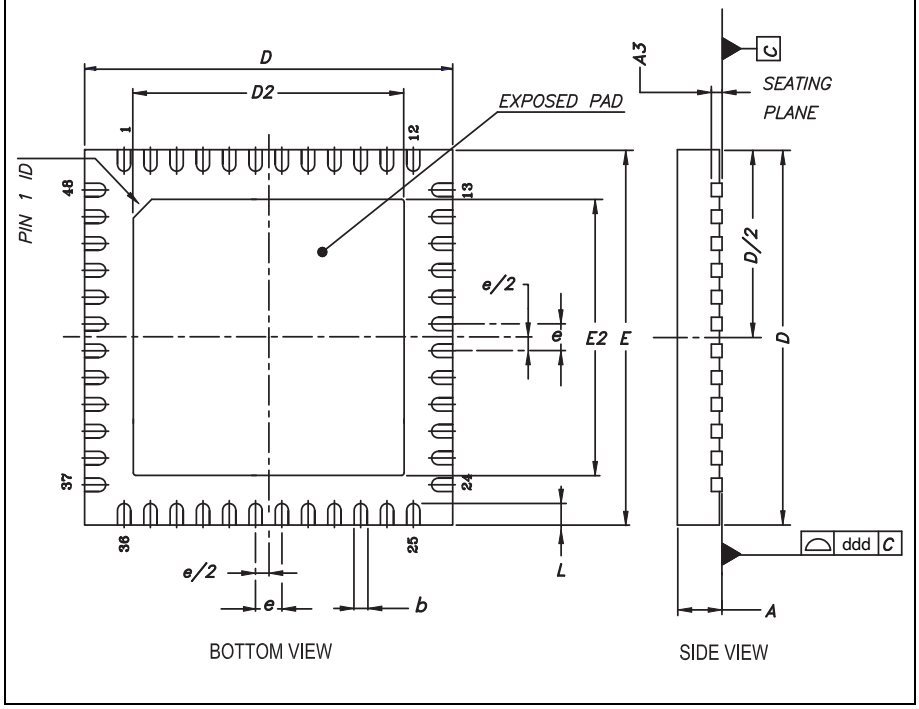
Figure 21. VFQFPN48 mechanical data and package dimensions

DIM.	mm			mils		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.800	0.900	1.000	31.50	35.43	39.37
A3		0.200			7.874	
b	0.180	0.250	0.300	7.087	9.843	11.81
D	6.900	7.000	7.100	271.6	275.6	279.5
D2	5.050	5.150	5.250	198.8	202.7	206.7
E	6.900	7.000	7.100	271.6	275.6	279.5
E2	5.050	5.150	5.250	198.8	202.7	206.7
e		0.500			19.68	
L	0.300	0.400	0.500	11.81	15.75	19.68
ddd			0.080			3.150

OUTLINE AND MECHANICAL DATA



VFQFPN-48 (7x7x1.0mm)
Very **F**ine **Q**uad **F**lat **P**ackage **N**o lead



15 Revision history

Table 22. Document revision history

Date	Revision	Changes
22-Apr-2013	1	Initial release.

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