VT8366

KT266 Athlon™ North Bridge

Single-Chip North Bridge
for Socket-A Based Athlon™ CPUs
with 266 MHz Front Side Bus
for Desktop PC Systems
with AGP4x and V-Link
plus Advanced ECC Memory Controller
supporting PC133 / PC100 SDR SDRAM & VCM
and PC2100 / PC1600 DDR SDRAM

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VIA TECHNOLOGIES, INC.

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- **High Performance and High Integration Athlon AGP 4x / DDR Chipset with Advanced System Power Management**
  - **KT266** Chipset: **VT8366** system controller and **VT8233** V-Link south bridge
  - Single chip Athlon system controller with 64-bit Socket-A Athlon CPU, 64-bit SDR/DDR system memory, 266 MB/sec high bandwidth V-Link NB/SB, and 32-bit AGP interfaces
  - V-Link south bridge chip includes UltraDMA-33/66/100 EIDE, 6 USB Ports, 10/100 Fast Etherlet LAN controller, AC97 / MC97 link (for Audio and Modem support), LPC, SMBus, Power Management, and Keyboard / PS2-Mouse Interfaces plus RTC / CMOS on chip
  - Supports separately powered 3.3V (5V tolerant) interface to system memory and AGP
  - Modular power management and clock control for advanced system power management
- **High Performance Athlon CPU Interface**
  - Supports Socket-A (Socket-462) AMD Athlon processors
  - HSTL-like 1.5V high-speed transceiver logic signal levels
  - Support independent address, data, and snoop interfaces
  - 100/133 MHz DDR (Double Data Rate) transfer on Athlon CPU address and data buses
  - Built-in PLL (Phase Lock Loop) circuitry for optimal skew control within and between clocking regions
  - Four-entry command queue to accommodate maximum CPU throughput
  - Four-entry probe queue to stores probes from the system to the processor
  - Twenty four-entry processor system data and control queue to store system data control commands in two separate read and write buffers for data movement in and out of processor interface
  - Supports WC (Write Combining) cycles
  - Sleep mode support
  - System management interrupt, memory remap and STPCLK mechanism

- **Full Featured Accelerated Graphics Port (AGP) Controller**
  - Synchronous and pseudo-synchronous with the host CPU bus with optimal skew control

V-Link	AGP	CPU	Mode
66 MHz	66 MHz	100 MHz DDR	Pseudo synchronous
66 MHz	66 MHz	133 MHz DDR	Synchronous

  - AGP v2.0 compliant
  - Supports SideBand Addressing (SBA) mode (non-multiplexed address / data)
  - Supports 66 MHz 1x, 2x and 4x modes for AD and SBA signaling
  - Pipelined split-transaction long-burst transfers up to 1GB/sec
  - Thirty-two level read request queue
  - Four level posted-write request queue
  - Thirty-two level (quadwords) read data FIFO (256 bytes)
  - Sixteen level (quadwords) write data FIFO (128 bytes)
  - Intelligent request reordering for maximum AGP bus utilization
  - Supports Flush/Fence commands
  - Graphics Address Relocation Table (GART)
    - One level TLB structure
    - Sixteen entry fully associative page table
    - LRU replacement scheme
  - Windows 95 OSR-2 VXD and integrated Windows 98 / Windows 2000 miniport driver support

- **High Bandwidth 266MB/S 8-bit V-Link Host Controller**
  - Supports 66MHz V-Link Host interface with peak bandwidth of 266MB/S
  - V-Link operates at 2X or 4X modes
  - Full duplex commands with separate STB/CMD
  - Request/Data split transaction
  - Configurable outstanding transaction queue for Host to V-Link Client accesses
  - Supports Defer/Defer-Reply transaction
  - Transaction assurance for V-Link Host to Client access. Eliminate V-Link Host-Client Retry cycles
  - Intelligent V-Link transaction protocol to eliminate data wait-state/throttle transfer latency. All V-Link transaction both Host and Client have consistent view of transaction data depth and buffer size to avoid data overflow.
  - High efficient V-Link arbitration with minimum overhead. All V-Link transaction with predictable cycle length with known CMD/Date duration.

- **Advanced High-Performance SDR/DDR DRAM Controller**
  - DRAM interface synchronous with host CPU (100/133 MHz) or AGP (66MHz) for most flexible configuration
  - DRAM interface may be faster than CPU by 33 MHz to allow use of 133 MHz memory with 100 MHz FSB
  - DRAM interface may be slower than CPU by 33 MHz to allow use of 100 MHz memory with 133 MHz FSB
  - Concurrent CPU, AGP, and V-Link access
  - Supports SDR / VCM SDRAM, or DDR SDRAM memory types
  - SDR and VCM SDRAM types may be used in mixed combinations in a SDR DRAM design
  - Different DRAM timing for each bank
  - Dynamic Clock Enable (CKE) control for SDRAM power reduction in high speed systems
  - Mixed 1M / 2M / 4M / 8M / 16M / 32M /64MxN DRAMs
  - Supports 8 banks up to 4 GB DRAMs (512Mb x8/x16 DRAM technology) for register SDR/DDR SDRAM module
  - Supports 6 banks up to 3 GB DRAMs (512Mb x8/x16 DRAM technology) for unbuffered SDR/DDR SDRAM module
  - Flexible row and column addresses. 64-bit data width only
  - LVTTL 3.3V DRAM interface with 5V-tolerant inputs for SDR SDRAM and 2.5V SSTL-2 DRAM interface for DDR SDRAM
  - Programmable I/O drive capability for MA, command, and MD signals
  - Dual copies of MA signals for improved drive
  - Optional bank-by-bank ECC (single-bit error correction and multi-bit error detection) or EC (error checking only) for DRAM integrity
  - Two-bank interleaving for 16Mbit SDRAM support
  - Two-bank and four bank interleaving for 64Mbit SDRAM support
  - Supports maximum 8-bank interleave (i.e., 8 pages open simultaneously); banks are allocated based on LRU
  - Independent SDRAM control for each bank
  - Seamless DRAM command scheduling for maximum DRAM bus utilization (e.g., precharge other banks while accessing the current bank)
  - Four cache lines (16 quadwords) of CPU to DRAM write buffers
  - Four cache lines of CPU to DRAM read prefetch buffers
  - Read around write capability for non-stalled CPU read
  - Speculative DRAM read before snoop result
  - Burst read and write operation
  - x-1-1-1-1-1-1-1 back-to-back accesses for SDR/VCM SDRAM, or x-1/2-1/2-1/2-1-1/2-1/2-1/2 back-to-back accesses for DDR SDRAM
  - Supports DDR SDRAM CL 2/2.5/3 and 1T/per command
  - Decoupled and burst DRAM refresh with staggered RAS timing. CAS before RAS or self refresh
- **Advanced System Power Management Support**
  - Dynamic power down of SDRAM (CKE)
  - PCI and AGP bus clock run and clock generator control
  - VTT suspend power plane preserves memory data
  - Suspend-to-DRAM and Self-Refresh operation
  - SDRAM self-refresh power down
  - 8 bytes of BIOS scratch registers
  - Low-leakage I/O pads
- **Built-in NAND-tree pin scan test capability**
- **3.3V, 0.35um, high speed / low power CMOS process**
- **35 x 35 mm, 552 pin BGA Package**

OVERVIEW

The **KT266 / VT8366 and VT8233** chipset is a high performance, cost-effective and energy efficient system controller for the implementation of AGP / PCI desktop personal computer systems based on 64-bit Socket-A (AMD Athlon) processors.

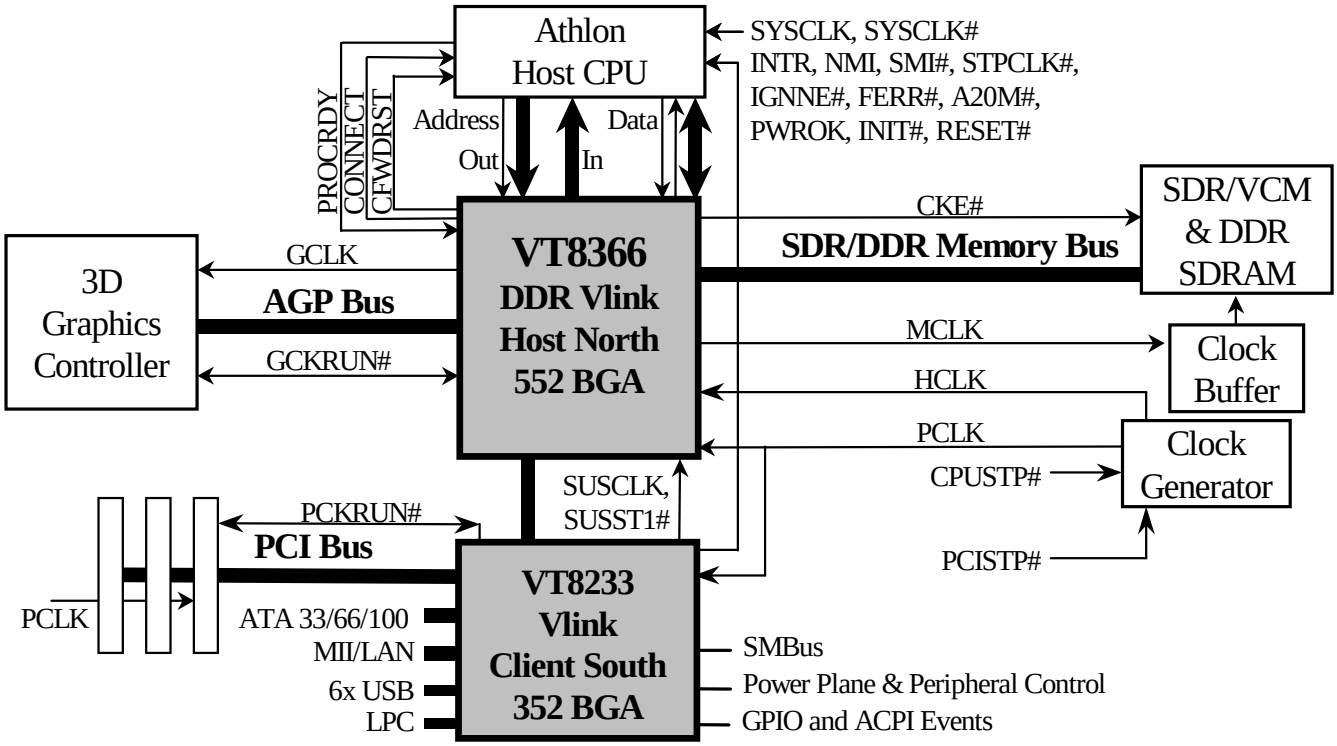

Figure 1. KT266 System Block Diagram Using the VT8233 V-Link South Bridge

The KT266 chip set consists of the VT8366 system controller (552 pin BGA) and the VT8233 V-Link south bridge (376 pin BGA). The VT8366 Host system controller provides superior performance between the CPU, DRAM, AGP bus, and V-Link bus with pipelined, burst, and concurrent operation. The VT8233 V-Link Client controller is a highly integrated PCI / LPC controller. Its internal bus structure is based on 66 MHz PCI bus that provides 2x bandwidth compare to previous generation PCI / ISA bridge chips. The VT8233 also provides a 266MB/sec bandwidth Host/Client V-Link interface with V-Link-PCI and V-Link-LPC controllers. It supports five PCI slots of arbitration and decoding for all integrated functions and LPC bus.

The VT8366 supports eight banks of SDR/DDR SDRAMs up to 4 GB. The DRAM controller supports standard Synchronous DRAM (SDRAM), and Virtual Channel SDRAM (VC SDRAM) SDRAM in a flexible mix / match manner, or it can be configured to support Double-Data-Rated (DDR) SDRAM mode. The SDR/DDR DRAM interface allows zero wait state bursting between the DRAM and the data buffers at 66 / 100 / 133 MHz. The eight banks of DRAM can be composed of an arbitrary mixture of 1M / 2M / 4M / 8M / 16M / 32M / 64M xN DRAMs. The DRAM controller also supports optional ECC (single-bit error correction and multi-bit detection) or EC (error checking) capability separately selectable on a bank-by-bank basis. The DRAM controller can run either synchronous or pseudo-synchronous mode with the host CPU bus frequency (66 / 100 / 133 MHz).

The VT8366 Host system controller also supports full AGP v2.0 capability for maximum bus utilization including 2x and 4x mode transfers, SBA (SideBand Addressing), Flush/Fence commands, and pipelined grants. An eight level request queue plus a four level post-write request queue with thirty-two and sixteen quadwords of read and write data FIFO's respectively are included for deep pipelined and split AGP transactions. A single-level GART TLB with 16 full associative entries and flexible CPU / AGP / PCI remapping control is also provided for operation under protected mode operating environments. Both Windows-95 VXD and

Windows-98 / NT5 miniport drivers are supported for interoperability with major AGP-based 3D and DVD-capable multimedia accelerators.

The VT8366 Host system controller supports two 32-bit 3.3 system buses (one AGP and one V-Link) that are synchronous / pseudo-synchronous to the CPU bus. The chip also contains a built-in bus-to-bus bridge to allow simultaneous concurrent operations on each bus. Five levels (doublewords) of post write buffers are included to allow for concurrent CPU and V-Link operation. For V-Link Host operation, forty-eight levels (doublewords) of post write buffers and sixteen levels (doublewords) of prefetch buffers are included for concurrent V-Link bus and DRAM/cache accesses. When combined the V-Link Host / Client controllers, it realizes a complete PCI sub-system and supports enhanced PCI bus commands such as Memory-Read-Line, Memory-Read-Multiple and Memory-Write-Invalid commands to minimize snoop overhead. In addition, advanced features are supported such as snoop ahead, snoop filtering, L1 write-back forward to PCI master, and L1 write-back merged with PCI post write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction and read caching mechanisms are also implemented for further improvement of overall system performance.

The 376-pin Ball Grid Array VT8233 Client V-Link PCI / LPC controller supports four levels (doublewords) of line buffers, type F DMA transfers and delay transaction to allow efficient PCI bus utilization and (PCI-2.1 compliant). The VT8233 integrated PCI controller and PCI arbitration for up to five PCI slots. One of the PCI REQ / GNT pair can be configured as high-priority to better support a low latency PCI bus master device. The VT8233 integrated networking MAC controller with standard MII interface to an external PHY for 10/100Mb base-T Ethernet or 1/10Mb PNA home networking.

The VT8233 also includes an integrated keyboard controller with PS2 mouse support, integrated DS12885 style real time clock with extended 256 byte CMOS RAM, integrated master mode enhanced IDE controller with full scatter / gather capability and extension to UltraDMA-33/66/100 for 33/66/100 MB/sec transfer rate, integrated USB interface with root hubs and six function ports with built-in physical layer transceivers, Distributed DMA support, and OnNow / ACPI compliant advanced configuration and power management interface.

For sophisticated power management, the Apollo KT266 chipset provides independent clock stop control for the CPU / SDRAM, PCI, and AGP buses and Dynamic CKE control for powering down of the SDRAM. A separate suspend-well plane is implemented for the SDRAM control signals for Suspend-to-DRAM operation. Coupled with the VT8233 south bridge chip, a complete power conscious PC main board can be implemented with no external TTLs.

The Apollo KT266 chipset is ideal for high performance, high quality, high energy efficient and high integration desktop and notebook AGP / PCI / LPC computer systems.