INTEGRATED TECHNOLOGY EXPRESS, INC.

IT8712F

Environment Control – Low Pin Count Input / Output (EC-LPC I/O)

Preliminary SCR Programming Guide V0.2

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Revision History

Section	Revision	Page No.
2	• Figure 2-1. IT8712F Smart Card Reader Flow Chart was revised.	7

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1. Smart Card Reader

1.1 Features

As an IFD (InterFace Device) built in IT8712, the Smart Card Reader (SCR) includes a standard UART (Either Serial Port 1 or Serial Port 2 is set in SCR mode) to control Smart Card interface handshaking and then performs data transfers, and can be connected to smart card socket directly. The Smart Card is capable of providing secured storage facilities for sensitive personal information (such as Private keys, Account numbers, Passwords, Medical information, … etc.). Then the SCR can be used for a broad range of applications in GSM, ID, pay TV, banking (refer to EMV96 Spec.), … and so forth. It also provides a Smart Card clock divider for those ICC (Integrated Circuit Card) without internal clocks.

1.2 Operation

The SCR is a low-power consumption design. Whenever the IFD is inactive, the clock divider will turn off internal clocks even when the clock of IFD controlling / monitoring state machine is turned off to save power consumption. Also it could be waked up immediately when IC card is removed in case of emergency or when the FET control function is turned on/off.

The VCC power of IC card interface is powered from an external FET to protect the smart card interface. Also, the charge/discharge time for FET to reach 5V/0V is programmable, and FET performs automatically to meet ISO 7816 activation and deactivation sequences. The UART's modem control lines: DTR#, RTS# and DCD# are used for controlling FET on/off, Smart Card Reset signal and IC card insertion detection respectively. When an IC card is being inserted, it will switch the SCRPRES# (Smart Card Present Detect#) and then cause the DCD# signal to trigger an interrupt to the system. Then in the Smart Card interrupt service routine, the driver can assert the DTR# signal to power on the external FET (SCRPFET#) and the RTS# signal to control the Smart Card Reset signal (SCRRST). In the mean time, IT8712 will generate a proper clock frequency to allow the IC card using default serial transfer baud rate to send back an ATR (Answer-To-Reset) sequence. The interface signals are enabled after VCC reaches enough voltage level. Then transfer protocol may be negotiated to promote more efficient transfers. In the same way, when the IC card is removed in case of emergency or when the ICC processing is finished, the driver can de-assert the DTR# to turn off the FET power. But before the FET power-off and the reset, clock and data signals will be de-active, followed by a sufficient FET discharge time guaranteed to protect IC card and IFD.

1.3 Connection of IFD to ICC Socket

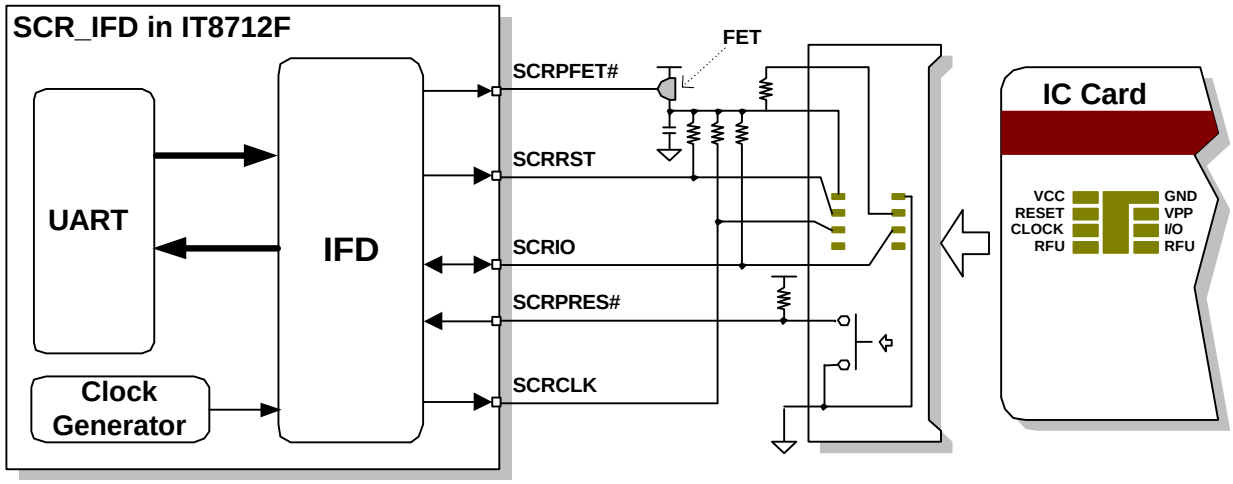


Figure 1-1. Smart Card Reader Application

1.4 Baud Rate Relationship Between UART and Smart Card Interface

To perform serial transfers correctly, the baud rate of UART must be set in ways similar to the ICC card.

- **Formula (Variation < 2%)**

$$\text{Baud Rate} = \frac{\text{UART}}{\frac{\frac{24\ \text{MHz}}{13}}{16 * N}} \approx \frac{\text{Smart Card}}{\frac{SCRCLK * D}{F}}$$

N =Divisor of UART, assigned by programming the DLM (Divisor Latch MSB) and DLL (Divisor Latch LSB).
F =Clock Rate Conversion Factor, default = 372.
D =Bit Rate Adjustment Factor, Default is 1.
SCRCLK duty cycle is 45%-55%.

- **ICC With Internal Clock**

ICC may use built-in internal clock, then the Baud rate is 9600 baud, just programming the Divisor Latch Registers of UART in the IT8712 for SCR IFD.

- **ICC Without Internal Clock**

Baud rate is SCRCLK/372 before negotiating, and SCRCLK is limited within 1 MHz - 5MHz. During the ATR sequence, the default F value (Clock Rate Conversion Factor) is 372, and the default D value (Bit Rate Adjustment Factor) is 1.

1.5 Waveform Relationship

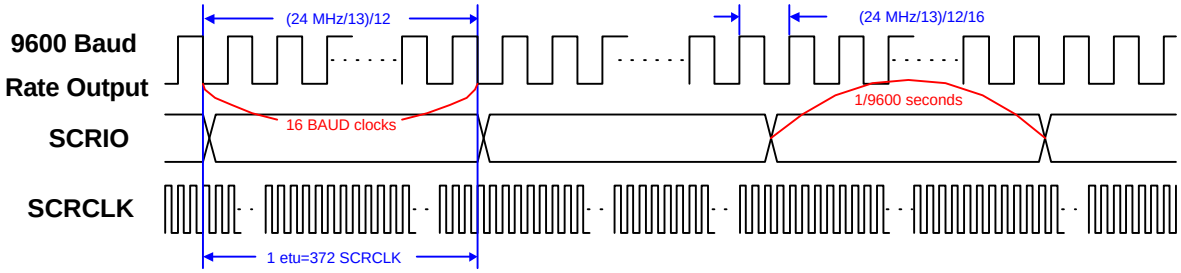


Figure 1-2. 9600 Baud Rate Example

1.6 Clock Divider

The SCRCLK is generated as the selection of SCR_CLKSEL1-0, which are determined in the S1 Special Configuration register 3 (LDN1_F2h) or S2 Special Configuration register 3 (LDN2_F2h).

Table 1-1. SCRCLK Selections

SCR_CLKSEL1-0	Selections
00	Stop
01	3.5 MHz
10	7.1 MHz
11	96 MHz / SCR DIV96M [Note]

Note: SCR DIV96M is determined by S1 Special Configuration Register 4 (LDN1_F3h) or S2 Special Configuration Register 4 (LDN2_F3h).

1.7 Waveform Example of Activation/Deactivation Sequence

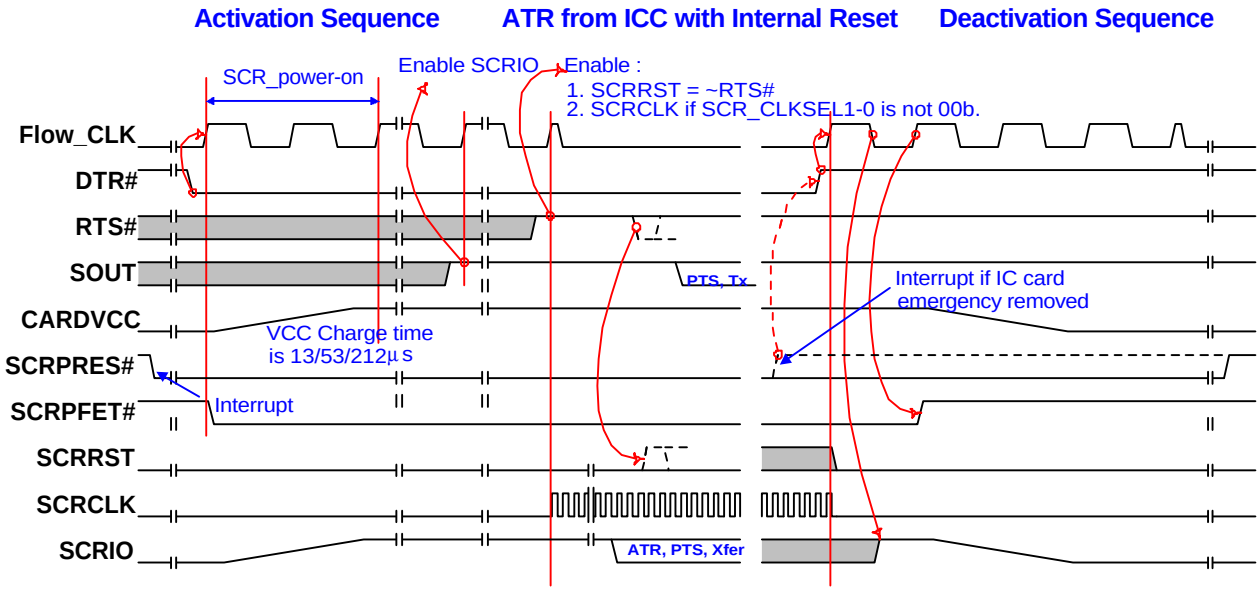


Figure 1-3. Waveform Example of IFD

- **Activation Sequence**

Refer to the waveform above. The SCR IFD in the IT8712 will make sure the IFD is in data receive mode (i.e. the SOUT from UART is high), and the RTS# should be programmed to high. The SCRCLK is then enabled to output to the IC card (which means that the IC card can count SCRCLK clock numbers to start ATR responses), the data transfer is then enabled, and the SCRRST is the inverse logic state of RTS#. Also, the operation procedure guarantees the correct activation sequence even if the driver cannot program the SCRCLK and SCRRST in the precise time points. In this way, the hardware meets the ICC specification.

- **ATR**

For the IC card with its own internal reset, its ATR begins within 400-40000 SCRCLK cycles. If no ATR is detected, the Smart Card IFD driver can then program the RTS# to low, and cause the SCRRST to high.

For some types of IC cards without internal reset signals, it will check out the SCRRST as active low reset, and begins its ATR within 400-40000 SCRCLK cycles from the time point of SCRRST rising edge.

The IT8712 does not support the type of IC Card that may send synchronous ATRs.

- **Deactivation and PTS Structure**

Whenever the IC card is removed or when the IFD driver intends to power off the SCR interface, the IFD will enter the deactivation sequence.

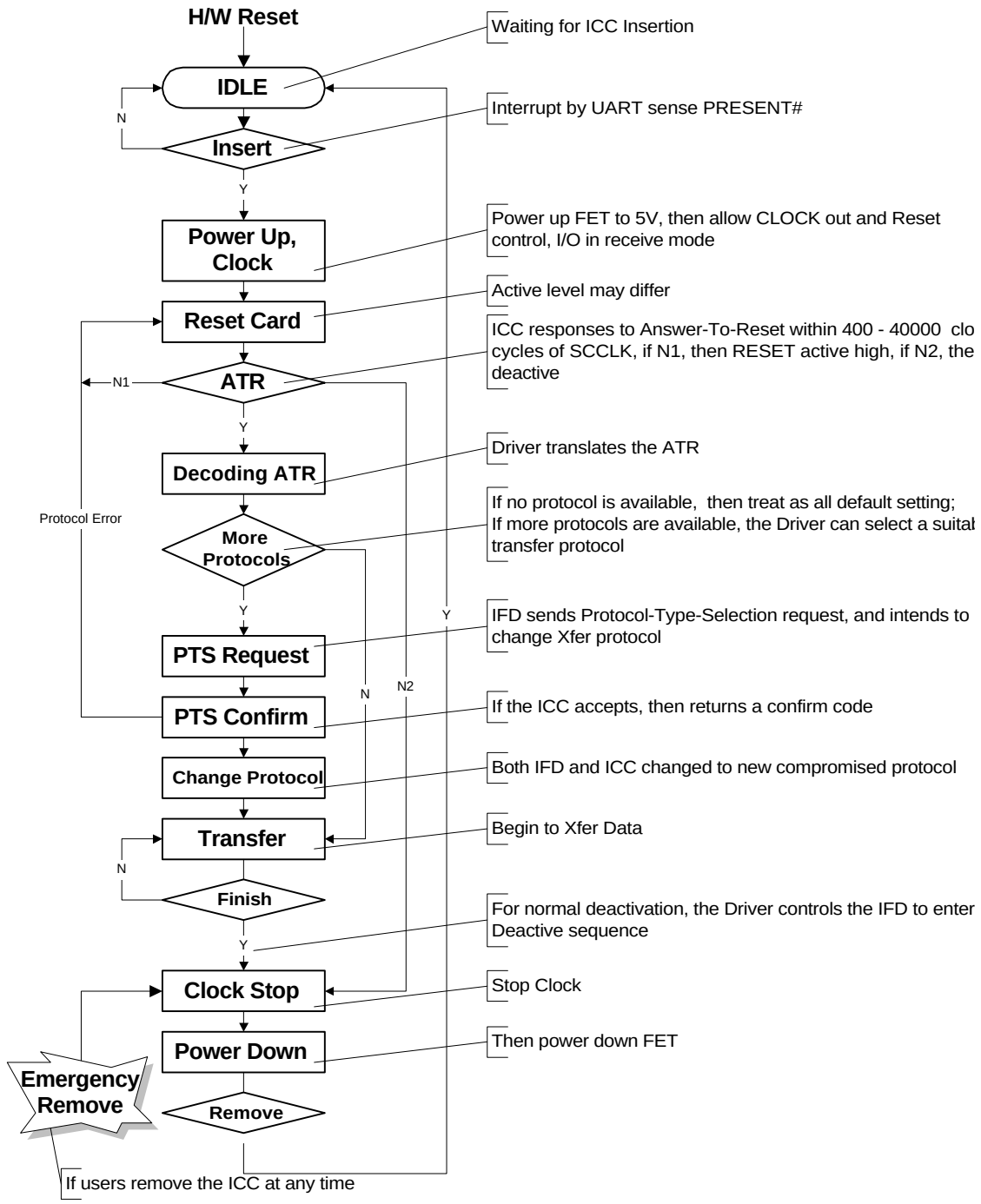
1.8 ATR and PTS Structure

The contents of the ATR (Answer-To-Reset) and PTS (Protocol-Type-Select) are defined in ISO/IEC 7816-X standards, which must be fully communicated by the ICC Resource manager, the ICC Service provider or the ICC application software.

After finalizing the coherent protocol, the SCR IFD enters the normal transfer mode. Since the SCRIO is the only data channel for both data transmit and receive as defined in the ICC Specification, the IT8712 can only support the half-duplex function. The SCRRST can be resent when a data transfer error occurs, and then the IFD driver will select a safer, lower-speed protocol to perform the data transfers again.

NOTE: ATR (Answer-To-Reset) is a string of characters returned from the card to the reader following the successful completion of the power-up sequence. The first byte of ATR should be "3Bh" or "3Fh".

1.9 Smart Card Operating Sequence Example



2. Flow Chart for IT8712 Smart Card Reader

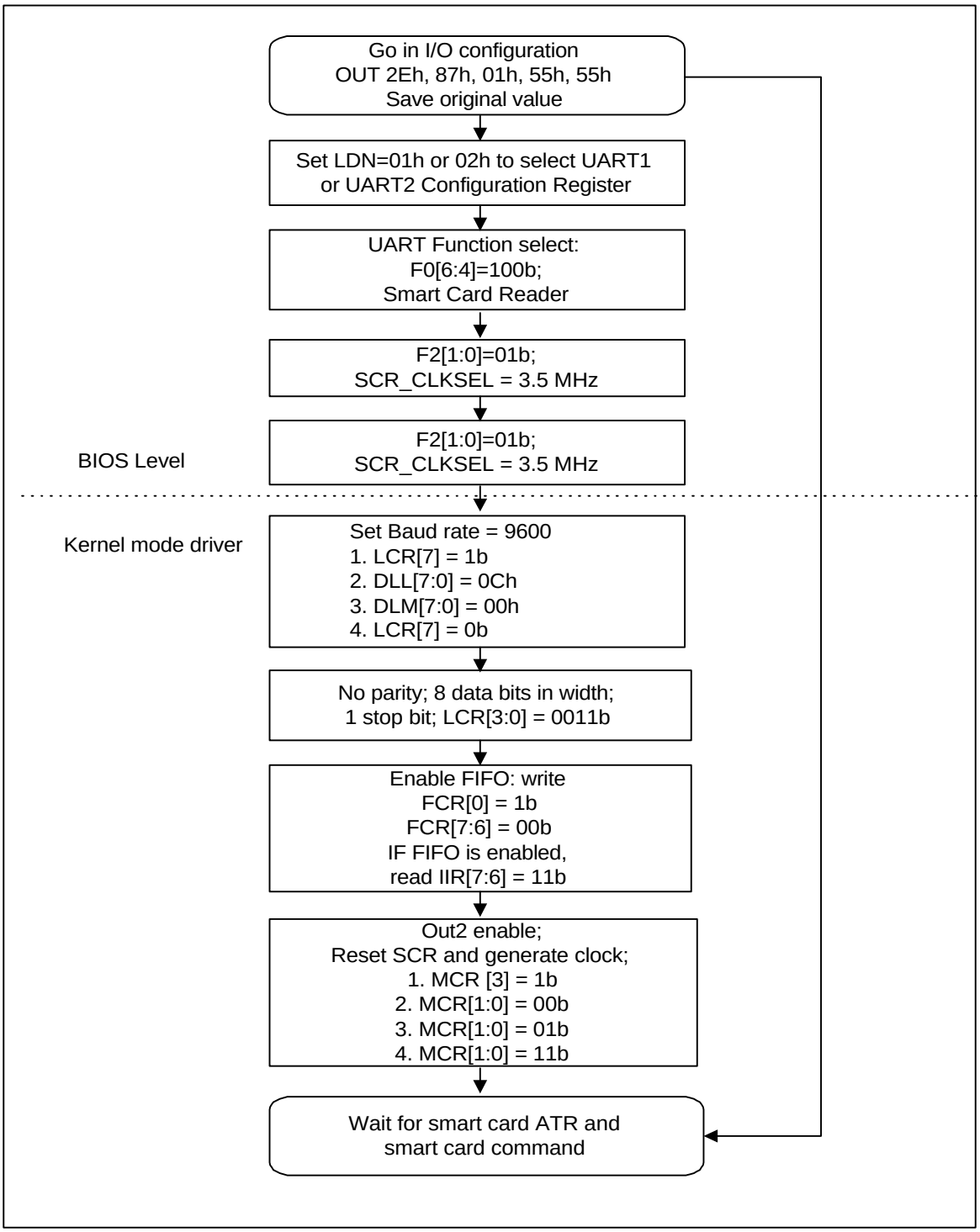


Figure 2-1. IT8712F Smart Card Reader Flow Chart

3. Serial Port Configuration Registers

The IT8712F smart card reader can be set on serial port 1 and serial port 2. If users choose the serial port1, then LDN=01h, or serial port 2, LDN=02h.

3.1 Serial Port Activate (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	Serial Port Enable. 1: Enabled. 0: Disabled.

3.2 Serial Port Base Address MSB Register (Index=60h)

Bit	Description
7-4	**Read only** as '0h" for Base Address[15:12].
3-0	**Read/write**, mapped as Base Address[11:8].

3.3 Serial Port Base Address LSB Register (Index=61h)

Bit	Description
7-3	**Read/write**, mapped as Base Address[7:3].
2-0	**Read only** as '000b."

3.4 Serial Port Interrupt Level Select (Index=70h)

Bit	Description
7-4	Reserved with default '0h."
3-0	Select the interrupt level [Note] for Serial Port 1.

Note: Interrupt level mapping

Fh-Dh: not valid
Ch: IRQ12
.
.
3h: IRQ3
2h: not valid
1h: IRQ1
0h: no interrupt selected

3.5 Serial Port Special Configuration Register 1 (Index=F0h, Default=00h)

Bit	Description
7	Reserved
6-4	Serial Port Mode [Note] 000: Standard (default) 001: IrDA 1.0 (HP SIR) 010: ASKIR 100: Smart Card Reader (SCR) else: Reserved
3	Reserved with default "0."
2-1	Clock Source. 00: 24 MHz/13 (Standard) 01: 24 MHz/12 (MIDI) 10: Reserved 11: Reserved
0	1: IRQ sharing. 0: Normal.

Note: Except the standard mode, COM1 and COM2 cannot be selected in the same time mode.

3.6 Serial Port Special Configuration Register 2 (Index=F1h, Default=50h)

Bit	Description
7	1: No transmission delay (40 bits) when the SIR or ASKIR is switched from RX mode to TX mode. 0: Transmission delay (40 bits) when the SIR or ASKIR is switched from RX mode to TX mode.
6	1: No reception delay (40 bits) when the SIR or ASKIR is switched from TX mode to RX mode. 0: Reception delay (40 bits) when the SIR or ASKIR is switched from TX mode to RX mode.
5	Single Mask Mode: When set, the RX of UART is masked under TX transmission.
4	1: Half Duplex (default). 0: Full Duplex.
3-0	Reserved

3.7 Serial Port Special Configuration Register 3 (Index=F2h, Default=00h)

This register is valid only when Serial Port's Mode is Smart Card Reader.

Bit	Description
7-3	Reserved
2	SCRPFET# polarity.
1-0	SCR_CLKSEL1-0. 00: Stop 01: 3.5 MHz 10: 7.1 MHz ¡ I 11: Special Divisor (96 MHz/DIV96M)

3.8 Serial Port Special Configuration Register 4 (Index=F3h, Default=7Fh)

This register is valid only when Serial Port's Mode is Smart Card Reader.

Bit	Description
7	Reserved
6-0	SCR DIV96M6-0.

3.9 Serial Port Register Description

Register	DLAB*	Address	READ	WRITE
Data	0	Base + 0h	RBR (Receiver Buffer Register)	TBR (Transmitter Buffer Register)
Control	0	Base + 1h	IER (Interrupt Enable Register)	IER
	x	Base + 2h	IIR (Interrupt Identification Register)	FCR (FIFO Control Register)
	x			
	x	Base + 3h	LCR (Line Control Register)	LCR
	x	Base + 4h	MCR (Modem Control Register)	MCR
	1	Base + 0h	DLL (Divisor Latch LSB)	DLL
	1	Base + 1h	DLM (Divisor Latch MSB)	DLM
Status	x	Base + 5h	LSR (Line Status Register)	LSR
	x	Base + 6h	MSR (Modem Status Register)	MSR
	x	Base + 7h	SCR (Scratch Pad Register)	SCR

* DLAB is bit 7 of the Line Control Register.

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