INTEGRATED TECHNOLOGY EXPRESS, INC.

IT8712F

Preliminary CIR Programming Guide V0.1

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1. Overview

The CIR driver consists of three main elements: User Interface, protocol decode, and device driver control. Diagram 1 below illustrates the working relationship among the three elements. The gray area – CIR device control module, is the focused discussion that will be covered in the document hereafter.

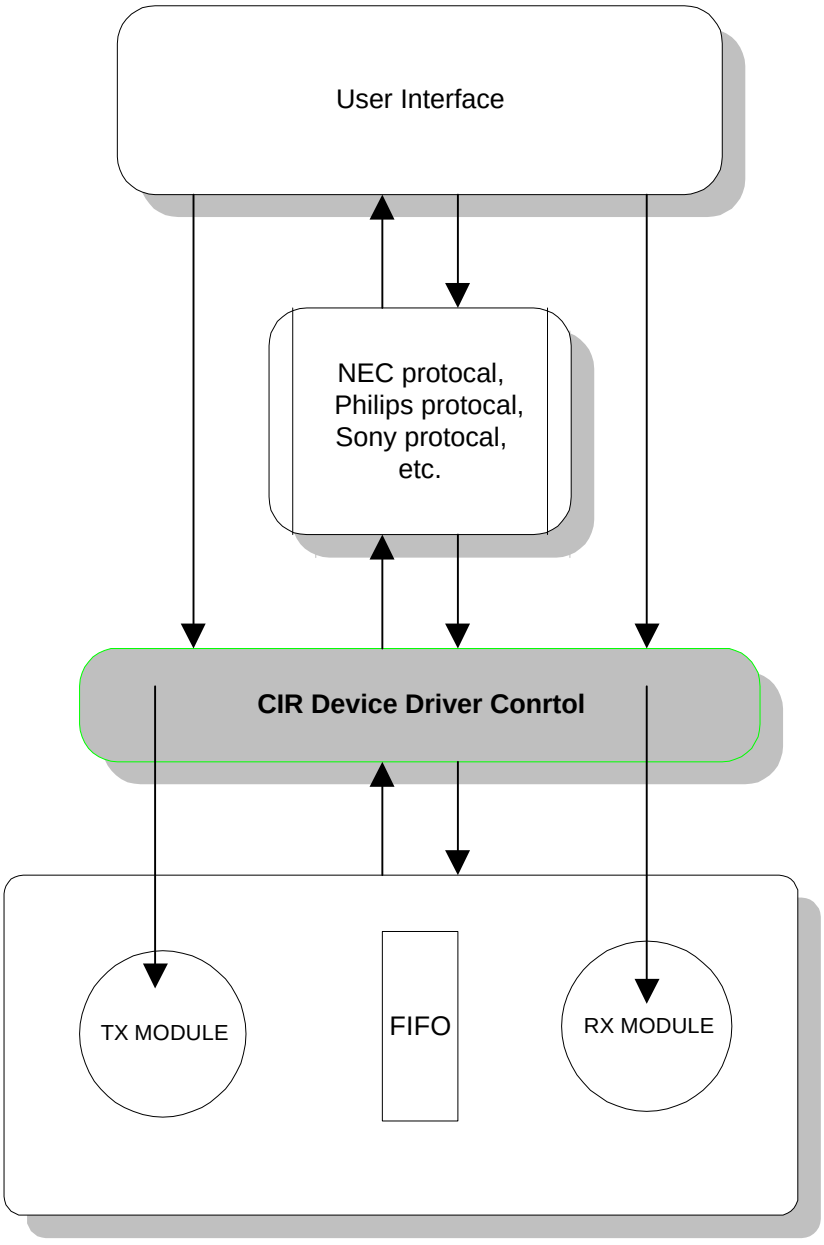

Figure 1-1. CIR Block Diagram

2. Flow Chart

After the user interface are dealt and the decode argument of the desired protocol are completed, the CIR register in CIR module must be set to enable the transferred data send /receive to/from the CIR FIFO. Figure 2-1 below illustrates the CIR module mechanism. TX /RX coding flow charts are illustrated respectively in Figure 2-2 and Figure 2-3 on the next pages.

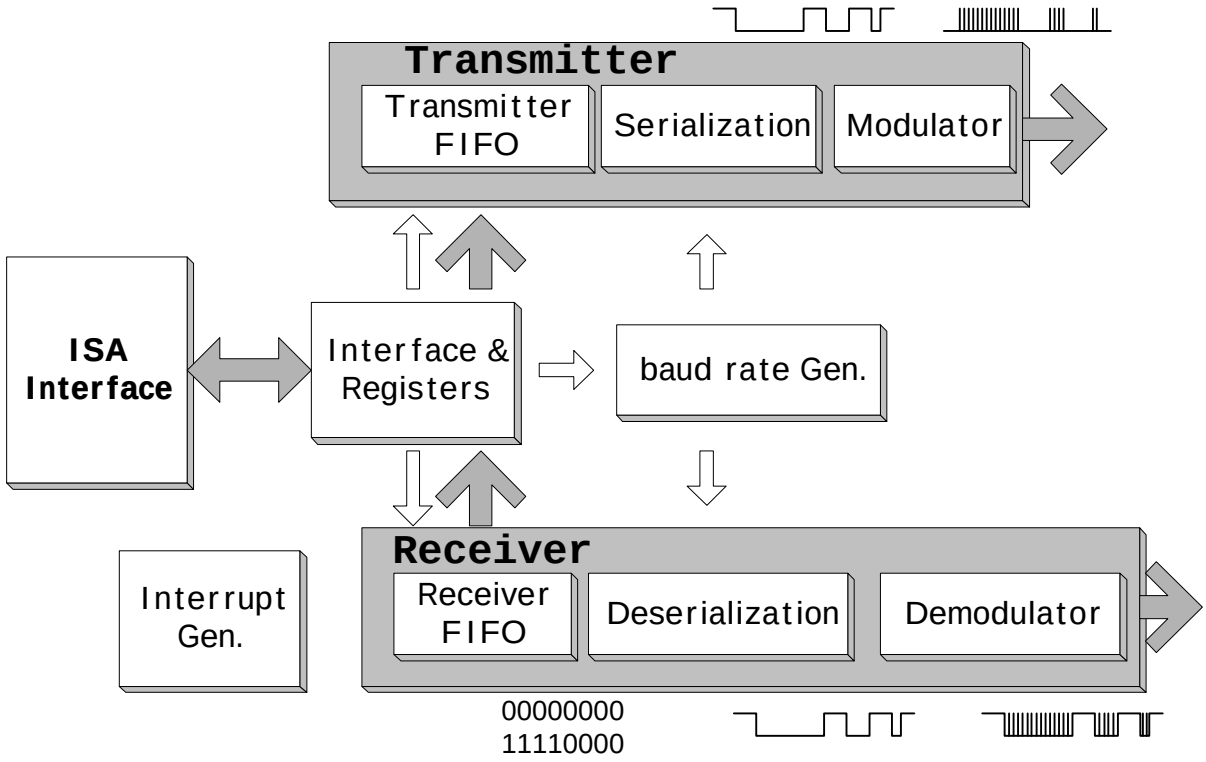

Figure 2-1. CIR Module Mechanism

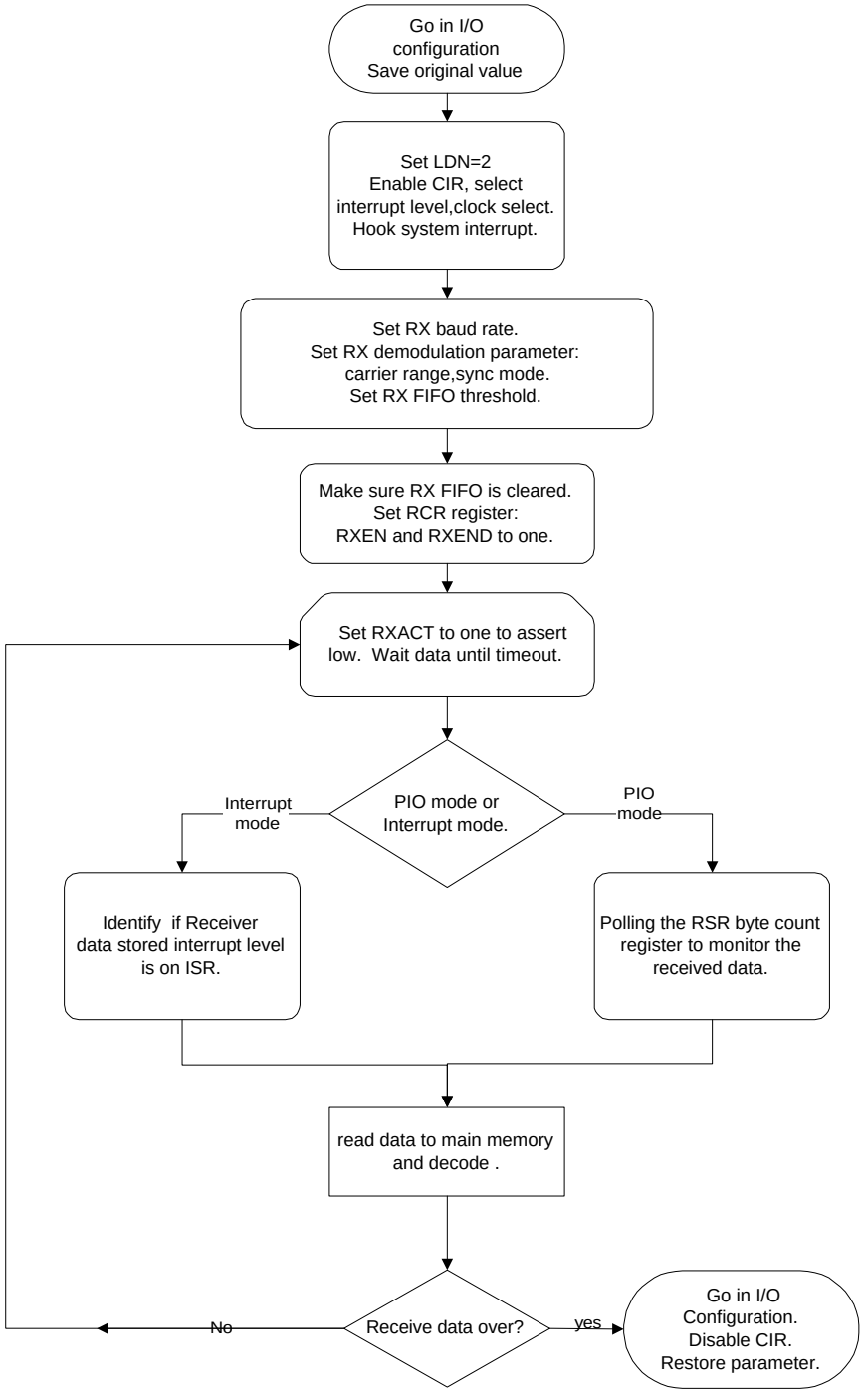

Figure 2-2. CIR RX Flow Chart

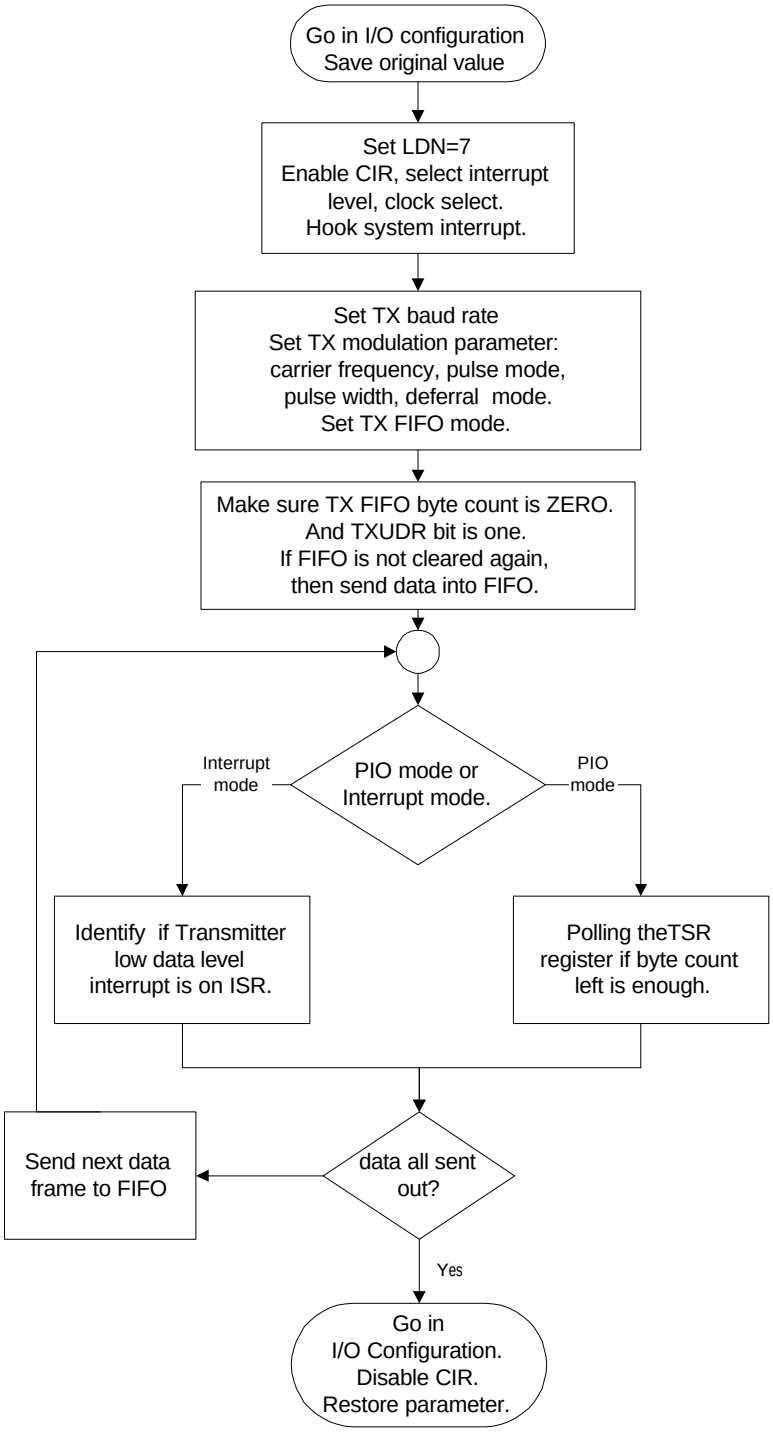

Figure 2-3. CIR TX Flow Chart

3. Programming Guide

a. Set configuration registers: The configuration registers must be set first: set LDN=07h, Active the Consumer IR. Select the base address from Consumer IR Base Address MSB register (Index: 60h) and Base Address LSB register (Index=61h). Select the CIR interrupt level from the register of Consumer IR Interrupt Level Select (Index: 70h). Make sure to hook the operation system interrupt and create the interrupt service routine too.

Table 3-1. Consumer IR Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
07h	30h	R/W	00h	Consumer IR Activate.
07h	60h	R/W	03h	Consumer IR Base Address MSB Register.
07h	61h	R/W	10h	Consumer IR Base Address LSB Register.
07h	70h	R/W	0Bh	Consumer IR Interrupt Level Select.
07h	F0h	R/W	00h	Consumer IR Special Configuration Register.

b. Set CIR Registers:

TX: baud rate, frequency, pulse width, pulse mode, deferral mode, RLE mode and FIFO threshold.
RX: Baud rate frequency range, sync mode and FIFO threshold.

c. Begin to Transmit/Receive Data:

TX: Before transmitting any data, the TX FIFO must be cleared first. The device then starts to transmit one frame data into the FIFO. During data transmit, the TX FIFO byte count must be monitored closely to ensure the byte count is remained below the maximum FIFO value, for FIFO to receive further data. It is recommended to clear the FIFO data before the next frame data transmission can be started.

RX: Before transmitting any data, the RX FIFO must be cleared first. RXEN and RXEND are then enabled, and RXACT is asserted low by writing one to clear this bit, as illustrated in the diagram on the next page.

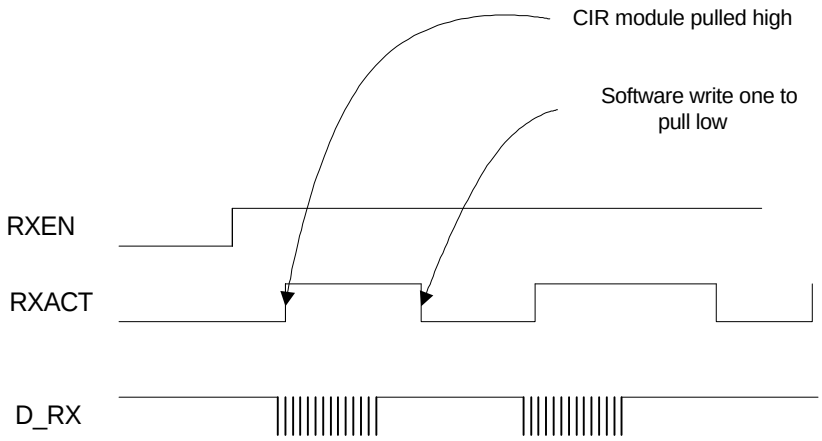

Figure 3-1. RXACT Relationship

After asserting RXACT low, the device waits data to enter FIFO for data receive. CIR mechanism will perform demodulation when the RX data bits become low. It indicates that the first bit of data frame must be a low bit to simulate CIR mechanism. In PIO mode, the data are received when the byte count value does not equal zero. In interrupt mode, the data are received during interrupt service routine when FIFO data go beyond the threshold, causing an interrupt to occur. After one frame data are received, RXACT will be asserted low by writing one to the bit. The CIR will not stop the demodulation by itself and will transmit 0xff continuously to FIFO if RXACT is not asserted low.

d. Stop TX/RX Action:

TX: After all frame data transmissions have been completed, several steps need to follow to stop the TX action: (1) disable the CIR in the configuration register; (2) restore the original setting; (3) unhook the interrupt.

RX: If further data reception is not required, several steps are required to disable the interrupt switch: (1) disable the CIR in the configuration register; (2) restore the original setting; (3) unhook the interrupt.

e. Register Description:

Register 0: DR

Bit	7	6	5	4	3	2	1	0
Bit Name	DR[7:0]							
Initial Value	FF							
R/W	Rx/Tx							

Register 1: IER

Bit	7	6	5	4	3	2	1	0
Bit Name	TM_EN	-	RESET	BR	IEE	RFOIE	RDAIE	TLDLIE
Initial Value	0	-	0	0	0	0	0	0
R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W

Do not set TM_EN (Test Mode Enable) bit to one
If bits IRFOV_EN, IRDS_EN or ITLDL_EN need to be set to one, IEE must set to one too.
If bit 5 Reset is set to one, all values will be reset to default values

Register 2: RCR

Bit	7	6	5	4	3	2	1	0
Bit Name	RDWOS	HCFS	RXEN	RXEND	RXACT	RXDCRG[2:0]		
Initial Value	0	0	0	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R		

Write one to clear bit 3 RXACT.

Register 3: TCR1

Bit	7	6	5	4	3	2	1	0
Bit Name	FIFOCLR	ILE	FIFOTL[1:0]		TXRLE	TXENDF	TXPM[1:0]	
Initial Value	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Write 1 to enable bit 7 FIFOCLR.

Register 4: TCR2

Bit	7	6	5	4	3	2	1	0
Bit Name	CFQ[4:0]					TXPW[2:0]		
Initial Value	0	1	0	1	1	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register 5: TSR

Bit	7	6	5	4	3	2	1	0
Bit Name	-	--	TXFBC[5:0]					
Initial Value	-	-	0					
R/W	-	-	R					

Register 5: BRDL

Bit	7	6	5	4	3	2	1	0
Bit Name	BRDL[7:0]							
Initial Value	0							
R/W	R/W							

Baud rate divisor =115200/baud rate.

Register 6: RSR

Bit	7	6	5	4	3	2	1	0
Bit Name	RXFTO	--	RXFTO[5:0]					
Initial Value	0	-	0					
R/W	R	-	R					

Register 6: BRDH

Bit	7	6	5	4	3	2	1	0
Bit Name	BRDH[7:0]							
Initial Value	0							
R/W	R/W							

Register 7: IIR

Bit	7	6	5	4	3	2	1	0
Bit Name	-	-	-	-	-	IID1	IID0	IIP
Initial Value	-	-	-	-	-	0	0	1
R/W	-	-	-	-	-	R	R	R

IID[1:0]:
00: No interrupt.
01: Transmitter Low Data Level Interrupt.
10: Receiver Data Stored Interrupt.
11: Receiver FIFO Overrun Interrupt.

Register 7: TM

Bit	7	6	5	4	3	2	1	0
Bit Name	IL_SEL	-	Test Mode Reg[5:0]					
Initial Value	0	-	0					
R/W	R/W	-	R/W					

Please note that baud rate must be no less than 4 times of carrier signal frequency.
Ex: Baud rate=9600→1/9600=104.2us.
Carrier freqency=35kHz→1/35kHz=28.6us
28.6us * 4>104.2us.→It may **not** work properly.
Baud rate divisor=115200/baud rate.
Ex1.2400bps→115200/2400=48→48(d)=0030(h)
BDHR=00(h), BDLR=30(h)
Ex2.bit width=0.565ms→1770bps→115200/1770=65(d)=41(h)
BDHR=00(h), BDLR=41(h).

Table 3-2. Receiver Demodulation Low Frequency (HFC = 0)

RANGE	001		010		011		100		101		110		
CFQ	min.	max.	min.	max.	min.	max.	min.	max.	min.	max.	min.	max.	(Hz)
00001	26.25	29.75	24.5	31.5	22.75	33.25	21	35	19.25	36.75	17.5	38.5	28k
00010	27.19	30.81	25.38	32.63	23.56	34.44	21.75	36.25	19.94	38.06	18.13	39.88	29k
00011	28.13	31.88	26.25	33.75	24.38	35.63	22.5	37.5	20.63	39.38	18.75	41.25	30k
00100	29.06	32.94	27.13	34.88	25.19	36.81	23.25	38.75	21.31	40.69	19.38	42.63	31k
00101	30	34	28	36	26	38	24	40	22	42	20	44	32k
00110	30.94	35.06	28.88	37.13	26.81	39.19	24.75	41.25	22.69	43.31	20.63	45.38	33k
00111	31.88	36.13	29.75	38.25	27.63	40.38	25.5	42.5	23.38	44.63	21.25	46.75	34k
01000	32.81	37.19	30.63	39.38	28.44	41.56	26.25	43.75	24.06	45.94	21.88	48.13	35k
01001	33.75	38.25	31.5	40.5	29.25	42.75	27	45	24.75	47.25	22.5	49.5	36k
01010	34.69	39.31	32.38	41.63	30.06	43.94	27.75	46.25	25.44	48.56	23.13	50.88	37k
01011	**35.63**	**40.38**	**33.25**	**42.75**	**30.88**	**45.13**	**28.5**	**47.5**	**26.13**	**49.88**	**23.75**	**52.25**	**38k**
01100	36.56	41.44	34.13	43.88	31.69	46.31	29.25	48.75	26.81	51.19	24.38	53.63	39k
01101	37.5	42.5	35	45	32.5	47.5	30	50	27.5	52.5	25	55	40k
01110	38.44	43.56	35.88	46.13	33.31	48.69	30.75	51.25	28.19	53.81	25.63	56.38	41k
01111	39.38	44.63	36.75	47.25	34.13	49.88	31.5	52.5	28.88	55.13	26.25	57.75	42k
10000	40.31	45.69	37.63	48.38	34.94	51.06	32.25	53.75	29.56	56.44	26.88	59.13	43k
10001	41.25	46.75	38.5	49.5	35.75	52.25	33	55	30.25	57.75	27.5	60.5	44k
10010	42.19	47.81	39.38	50.63	36.56	53.44	33.75	56.25	30.94	59.06	28.13	61.88	45k
10011	43.13	48.88	40.25	51.75	37.38	54.63	34.5	57.5	31.63	60.38	28.75	63.25	46k
10100	44.06	49.94	41.13	52.88	38.19	55.81	35.25	58.75	32.31	61.69	29.38	64.63	47k
10101	45	51	42	54	39	57	36	60	33	63	30	66	48k
10110	45.94	52.06	42.88	55.13	39.81	58.19	36.75	61.25	33.69	64.31	30.63	67.38	49k
10111	46.88	53.13	43.75	56.25	40.63	59.38	37.5	62.5	34.38	65.63	31.25	68.75	50k
11000	47.81	54.19	44.63	57.38	41.44	60.56	38.25	63.75	35.06	66.94	31.88	70.13	51k
11001	49.18	54.55	46.88	57.69	44.78	61.22	42.86	65.22	41.1	69.77	39.47	75	52k
11010	49.69	56.31	46.38	59.63	43.06	62.94	39.75	66.25	36.44	69.56	33.13	72.88	53k
11011	50.63	57.38	47.25	60.75	43.88	64.13	40.5	67.5	37.13	70.88	33.75	74.25	54k
11100	51.56	58.44	48.13	61.88	44.69	65.31	41.25	68.75	37.81	72.19	34.38	75.63	55k
11101	52.5	59.5	49	63	45.5	66.5	42	70	38.5	73.5	35	77	56k
11110	53.44	60.56	49.88	64.13	46.31	67.69	42.75	71.25	39.19	74.81	35.63	78.38	57k

Table 3-3. Receiver Demodulation High Frequency (HCFS = 1)

RANGE	001		010		011		100		101		110		
CFQ	min.	max.	min.	max.	min.	max.	min.	max.	min.	max.	min.	max.	(kHz)
00011	375	425	350	450	325	475	300	500	275	525	250	550	400k
01000	421.9	478.1	393.8	506.3	365.6	534.4	337.5	562.5	309.4	590.6	281.3	618.8	450k
01011	450	510	420	540	390	570	360	600	330	630	300	660	**480k**
01011	468.8	531.3	437.5	562.5	406.3	593.8	375	625	343.8	656.3	312.5	687.5	500k

Table 3-4. Transmitter Modulation Carrier Frequency

CFQ	Low Frequency (HCFS =0)	High Frequency (HCFS = 1)
00000	27 kHz	-
00010	29 kHz	-
00011	30 kHz	400 kHz
00100	31 kHz	-
00101	32 kHz	-
00110	33 kHz	-
00111	34 kHz	-
01000	35 kHz	450 kHz
01001	36 kHz	-
01010	37 kHz	-
01011	**38kHz**	**480 kHz**
01100	39kHz	-
01101	40kHz	500kHz
01110	41 kHz	-
01111	42 kHz	-
10000	43 kHz	-
10001	44kHz	-
10010	45kHz	-
10011	46kHz	-
10100	47kHz	-
10101	48kHz	-
10110	49kHz	--
10111	50kHz	-
11000	51kHz	-
11001	52 kHz	-
11010	53 kHz	-
11011	54 kHz	-
11100	55kHz	-
11101	56kHz	-
11110	57kHz	-
11111	58kHz	-

f. Power-on Setting:

Just like turning on a television set, you can use a transmitter to power on the computer via the following setting.

1. See Table 3-5. In LDN=04h setting, Index (30h) Bit 0 and Index (F0h) Bit 0 must be on to enable the CIR power-on function.

2. In LDN=04h setting, Index (F5h)=0x20, Index (F6h)=CIR code byte count.
   CIR code byte count format→ Wake up sleeping mode's byte count decrease 3: short code bits [7:4].
   Power-on mode's byte count decrease 3: long code bits[3:0].

3. Setting Index (F5h)=01h, Index (F6h)=1st key code pattern.
   Index (F5h)=02h, Index (F6h)=2nd key code pattern.
   ….
   . ….

EX:

```
Outportb(cfg_index,0xf5);
Outportb(cfg_data  ,0x20);
Outportb(cfg_index,0xf6);
Temp=(ShortByteCount-3)+((LongByteCount-3)<<4);
Outportb(cfg_data,Temp)
```

4. Setting the CIR register at receiving data mode according to Figure 2-2. CIR RX Flow Chart..
   Then you can power on the computer by CIR transmitter, and see if in LDN=04h Index (F1h) Bit 0 is on as a re-check.

Table3-5. Environment Controller Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
04h	30h	R/W	00h	Environment Controller Activate
04h	60h	R/W	02h	Environment Controller Primary Base Address MSB Register
04h	61h	R/W	90h	Environment Controller Primary Base Address LSB Register
04h	62h	R/W	02h	PME Direct Access Base Address MSB Register
04h	63h	R/W	30h	PME Direct Access Base Address LSB Register
04h	70h	R/W	09h	Environment Controller Interrupt Level Select
04h	F0h	R/W	00h	APC/PME Event Enable Register
04h	F1h	R/W	00h	APC/PME Status Register
04h	F2h	R/W	00h	APC/PME Control Register 1
04h	F3h	R/W	00h	Environment Controller Special Configuration Register
04h	F4h	R-R/W	00h	APC/PME Control Register 2
04h	F5h	R/W	-	APC/PME Special Code Index Register
04h	F6h	R/W	-	APC/PME Special Code Data Register

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8. INDEMNIFICATION

Seller will, at its own expense, assist Buyer with technical support and information in connection with any claim that any parts as shipped by Seller under this purchase order infringe any valid and enforceable copyright, or trademark, provided however, that Buyer (i) gives immediate written notice to Seller, (ii) permits Seller to participate and to defend if Seller requests to do so, and (iii) gives Seller all needed information, assistance and authority. However, Seller will not be responsible for infringements resulting from anything not entirely manufactured by Seller, or from any combination with products, equipment, or materials not furnished by Seller. Seller will have no liability with respect to intellectual property matters arising out of products made to Buyer's specifications, code, or designs.
Except as expressly stated in this Paragraph 8 or in another writing signed by an authorized officer, Seller makes no representations and/or warranties with respect to intellectual and/or industrial property and/or with respect to claims of infringement. Except as to claims Seller agrees in writing to defend, BUYER WILL INDEMNIFY, DEFEND AND HOLD HARMLESS SELLER FROM ALL CLAIMS, COSTS, LOSSES, AND DAMAGES (INCLUDING ATTORNEYS FEES) AGAINST AND/OR ARISING OUT OF GOODS SOLD AND/OR SHIPPED HEREUNDER.

9. NO CONFIDENTIAL INFORMATION

Seller shall have no obligation to hold any information in confidence except as provided in a separate non-disclosure agreement signed by both parties.

10. ENTIRE AGREEMENT

(a) These terms and conditions are the entire agreement and the only representations and understandings between Seller and Buyer, and no addition, deletion or modification shall be binding on Seller unless expressly agreed to in a writing signed by an officer of Seller.
(b) Buyer is not relying upon any warranty or representation except for those specifically stated here.

11. APPLICABLE LAW

The contract and all performance and disputes arising out of or relating to goods involved will be governed where Seller is ITE Taiwan by the laws of Taiwan, Republic of China or, where Seller is ITE California, by the laws of California and the United States of America, in either event without reference to the U.N. Convention on Contracts for the International Sale of Goods or to conflict of laws principles. Buyer agrees at its sole expense to comply with all applicable laws in connection with the purchase, use or sale of the goods provided hereunder and to indemnify Seller from any failure by Buyer to so comply. Without limiting the foregoing, Buyer certifies that no technical data or direct products thereof will be made available or re-exported, directly or indirectly, to any country to which such export or access is prohibited or restricted under U.S. law or regulations, unless prior authorization is obtained from the appropriate officials and agencies of the government as required under U.S. laws and regulations.

12. JURISDICTION AND VENUE

Where Seller is ITE Taiwan, the courts located in Hsinchu, Taiwan, Republic of China, will have the sole and exclusive jurisdiction and venue over any dispute arising out of or relating to the contract or any sale of goods hereunder. Where Seller is ITE California, the courts located in Santa Clara County, California, USA, will have the sole and exclusive jurisdiction and venue over any dispute arising out of or relating to the contract or any sale of goods hereunder. Buyer hereby consents to the jurisdiction of such courts.

13. ATTORNEYS' FEES

Reasonable attorneys' fees and costs will be awarded to the prevailing party in the event of litigation involving and/or relating to the enforcement or interpretation of the contract and/or any goods sold under it.

INTEGRATED TECHNOLOGY EXPRESS, INC.

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