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ITE Tech. Inc.

IT8702F

Super – Low Pin Count Input / Output
(LPC I/O)

Preliminary Specification V0.5

ITE TECH. INC.

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Revision History

Section	Revision	Page No.
4	- Added a PCIRST5# function.	7, 8
5	- Added ATXPG pin and revised the PWROK circuit to add two AND inputs, SUSB# and ATXPG.	19
5	- Added 2 extra sets FAN_TAC4, 5 and FAN_CTL4, 5.	7, 8, 10, 11
5	- Changed the pad types of MCLK, MDAT, KCLK and KDATA from DIOD16 to DIOD24.	18
6	- Changed the chip version register from 06h to 07h.	34
6	- Added a PWROK1/2 delay time selection register for option.	35
6	- Changed the default value of the pin multi-function selection of pin-84.	38
6	- Changed the default value of FAN_CTL's PWM clock into 22~27Khz.	75
11	- Figure 11-12 was revised.	153

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1. Features

- **Low Pin Count Interface**
  - Comply with Intel Low Pin Count Interface Specification Rev. 1.0
  - Supports LDRQ#, SERIRQ protocols
  - Supports PCI PME# Interfaces

- **ACPI & LANDesk Compliant**
  - ACPI V. 1.0 compliant
  - Register sets compatible with “Plug and Play ISA Specification V. 1.0a”
  - LANDesk 3.X compliant
  - Supports 12 logical devices

- **EC Controller**
  - 1 chassis open detection input with low power Flip-Flop backed by the battery
  - Watch Dog comparison of all monitored values
  - Provides VID0 – VID5 support for the CPU

- **Fan Speed Controller**
  - Provides fan on-off and PWM control
  - Supports 5 programmable Pulse Width Modulation (PWM) outputs
  - 128 steps of PWM modes
  - Monitors 5 fan tachometer inputs

- **Two 16C550 UARTs**
  - Supports two standard Serial Ports
  - Supports IrDA 1.0/ASKIR protocols
  - Supports Smart Card Reader protocols

- **Smart Card Reader**
  - Compliant with Personal Computer Smart Card (PC/SC) Working Group standard
  - Compliant with smart card (ISO 7816) protocols
  - Supports card present detect
  - Supports Smart Card insertion power-on feature
  - Supports one programmable clock frequency, and 7.1 MHz and 3.5 MHz (Default) card clocks

- **Consumer Remote Control (TV remote) IR with power-up feature**

- **IEEE 1284 Parallel Port**
  - Standard mode -- Bi-directional SPP compliant
  - Enhanced mode -- EPP V. 1.7 and V. 1.9 compliant
  - High speed mode -- ECP, IEEE 1284 compliant
  - Back-drive current reduction
  - Printer power-on damage reduction
  - Supports POST (Power-On Self Test) Data Port

- **Floppy Disk Controller**
  - Supports two 360K/ 720K/ 1.2M/ 1.44M/ 2.88M floppy disk drives
  - Enhanced digital data separator
  - 3-Mode drives supported
  - Supports automatic write protection via software

- **Keyboard Controller**
  - 8042 compatible for PS/2 keyboard and mouse
  - 2KB of custom ROM and 256-byte data RAM
  - GateA20 and Keyboard reset output
  - Supports any key, or 2-5 sequential keys, or 1-3 simultaneous keys keyboard power-on events
  - Supports mouse double-click and/or mouse move power on events
  - Supports Keyboard and Mouse I/F hardware auto-swap

- **Game Port**
  - Built-in 558 quad timers and buffer chips
  - Supports direct connection of two joysticks
- **Dedicated MIDI Interface**
  - MPU-401 UART mode compatible
- **38 General Purpose I/O Pins**
  - Input mode supports either switch de-bounce or programmable external IRQ input routing
  - Output mode supports 2 sets of programmable LED blinking periods
- **External IRQ Input Routing Capability**
  - Provides IRQ input routing through GPIO input mode
  - Programmable registers for IRQ routing
- **Watch Dog Timer**
  - Time resolution 1 minute or 1 second, maximum 255 minutes or 255 seconds
  - Output to KRST# when expired
- **ITE innovative automatic power-failure resume and power button de-bounce**
- **Dedicated Infrared pins**
- **VCCH and Vbat Supported**
- **Built-in 32.768 KHz Oscillator**
- **Single 24/48 MHz Clock Input**
- **+5V Power Supply**
- **128-pin QFP**

2. General Description

The IT8702F is a Low Pin Count Interface-based highly integrated Super I/O. The IT8702F provides the most commonly used legacy Super I/O functionality plus the Fan Speed Controller and Smart Card Reader Interface. The device's LPC interface complies with Intel "LPC Interface Specification Rev. 1.0". The IT8702F is ACPI & LANDesk compliant.

The IT8702F features a PC/SC and ISO 7816 compliant Smart Card Reader. The IT8702F contains one game port which supports 2 joysticks, 1 MIDI port, and 1 Fan Speed Controller. The fan speed controller is responsible to control 5 fan speeds through three 128 steps of Pulse Width Modulation (PWM) output pins and to monitor five FANs' Tachometer inputs. It also features two 16C550 UARTs, one IEEE 1284 Parallel Port, one Floppy Disk Controller and one 8042 Keyboard Controller.

The IT8702F has integrated 12 logical devices. One high-performance 2.88MB floppy disk controller, with digital data separator, supports two 360K/ 720K/ 1.2M/ 1.44M/ 2.88M floppy disk drives. One multi-mode high-performance parallel port features the bi-directional Standard Parallel Port (SPP), the Enhanced Parallel Port (EPP V. 1.7 and EPP V. 1.9 are supported), and the IEEE 1284 compliant Extended Capabilities Port (ECP). Two 16C550 standard compatible enhanced UARTs perform asynchronous communication, and also support either IR or MIDI interfaces. One game port with built-in 558 quad timers and buffer chips supports direct connection of 2 joysticks. The device also features one MPU-401 UART mode compatible MIDI port, one fan speed controller responsible for controlling / monitoring 5 fans and 5 GPIO ports (38 GPIO pins). The IT8702F also has an integrated 8042 compatible Keyboard Controller with 2KB of programmable ROM for customer application.

These 12 logical devices can be individually enabled or disabled via software configuration registers. The IT8702F utilizes power-saving circuitry to reduce power consumption, and once a logical device is disabled the inputs are gated inhibit, the outputs are tri-state, and the input clock is disabled. The device requires a single 24/48 MHz clock input and operates with +5V power supply. The IT8702F is available in 128-pin QFP (Quad Flat Package).

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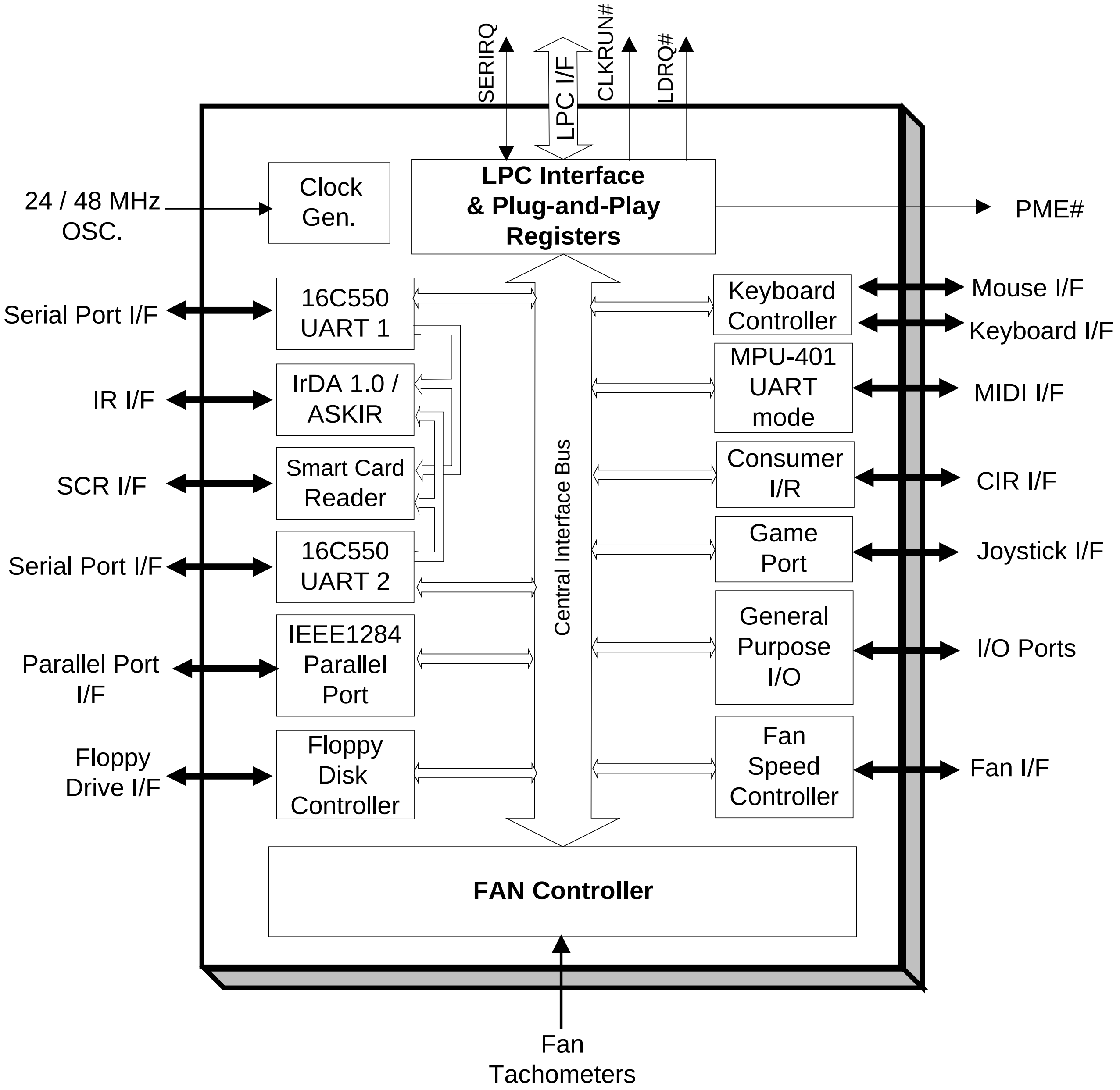
3. Block Diagram


SERIRQ
LPC I/F
CLKRUN#
LDRQ#
24 / 48 MHz OSC.
Clock Gen.
LPC Interface & Plug-and-Play Registers
PME#
Serial Port I/F
16C550 UART 1
IR I/F
IrDA 1.0 / ASKIR
SCR I/F
Smart Card Reader
Serial Port I/F
16C550 UART 2
Parallel Port I/F
IEEE1284 Parallel Port
Floppy Drive I/F
Floppy Disk Controller
Central Interface Bus
Keyboard Controller
Mouse I/F
Keyboard I/F
MPU-401 UART mode
MIDI I/F
Consumer I/R
CIR I/F
Game Port
Joystick I/F
General Purpose I/O
I/O Ports
Fan Speed Controller
Fan I/F
FAN Controller
Fan Tachometers

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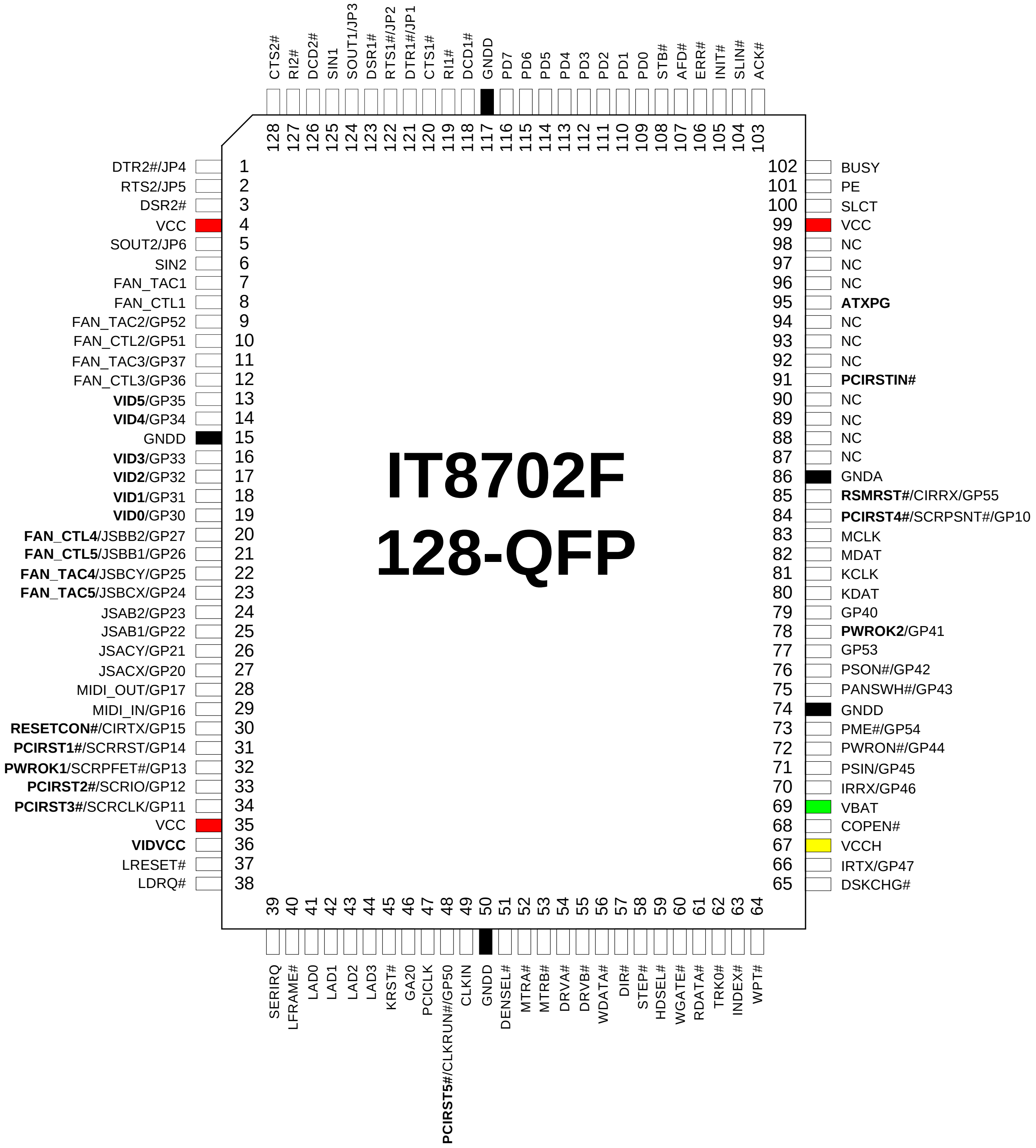
4. Pin Configuration


IT8702F
128-QFP
1 DTR2#/JP4
2 RTS2/JP5
3 DSR2#
4 VCC
5 SOUT2/JP6
6 SIN2
7 FAN_TAC1
8 FAN_CTL1
9 FAN_TAC2/GP52
10 FAN_CTL2/GP51
11 FAN_TAC3/GP37
12 FAN_CTL3/GP36
13 **VID5**/GP35
14 **VID4**/GP34
15 GNDD
16 **VID3**/GP33
17 **VID2**/GP32
18 **VID1**/GP31
19 **VID0**/GP30
20 **FAN_CTL4**/JSBB2/GP27
21 **FAN_CTL5**/JSBB1/GP26
22 **FAN_TAC4**/JSBCY/GP25
23 **FAN_TAC5**/JSBCX/GP24
24 JSAB2/GP23
25 JSAB1/GP22
26 JSACY/GP21
27 JSACX/GP20
28 MIDI_OUT/GP17
29 MIDI_IN/GP16
30 **RESETCON#**/CIRTX/GP15
31 **PCIRST1#**/SCRRST/GP14
32 **PWROK1**/SCRPFET#/GP13
33 **PCIRST2#**/SCRIO/GP12
34 **PCIRST3#**/SCRCLK/GP11
35 VCC
36 **VIDVCC**
37 LRESET#
38 LDRQ#
39 SERIRQ
40 LFRAME#
41 LAD0
42 LAD1
43 LAD2
44 LAD3
45 KRST#
46 GA20
47 PCICLK
48 **PCIRST5#**/CLKRUN#/GP50
49 CLKIN
50 GNDD
51 DENSEL#
52 MTRA#
53 MTRB#
54 DRVA#
55 DRVB#
56 WDATA#
57 DIR#
58 STEP#
59 HDSEL#
60 WGATE#
61 RDATA#
62 TRK0#
63 INDEX#
64 WPT#
65 DSKCHG#
66 IRTX/GP47
67 VCCH
68 COPEN#
69 VBAT
70 IRRX/GP46
71 PSIN/GP45
72 PWRON#/GP44
73 PME#/GP54
74 GNDD
75 PANSWH#/GP43
76 PSON#/GP42
77 GP53
78 **PWROK2**/GP41
79 GP40
80 KDAT
81 KCLK
82 MDAT
83 MCLK
84 **PCIRST4#**/SCRPSNT#/GP10
85 **RSMRST#**/CIRRX/GP55
86 GNDA
87 NC
88 NC
89 NC
90 NC
91 **PCIRSTIN#**
92 NC
93 NC
94 NC
95 **ATXPG**
96 NC
97 NC
98 NC
99 VCC
100 SLCT
101 PE
102 BUSY
103 ACK#
104 SLIN#
105 INIT#
106 ERR#
107 AFD#
108 STB#
109 PD0
110 PD1
111 PD2
112 PD3
113 PD4
114 PD5
115 PD6
116 PD7
117 GNDD
118 DCD1#
119 RI1#
120 CTS1#
121 DTR1#/JP1
122 RTS1#/JP2
123 DSR1#
124 SOUT1/JP3
125 SIN1
126 DCD2#
127 RI2#
128 CTS2#

Top View

Table 4-1. Pins Listed in Numeric Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	DTR2#/JP4	33	PCIRST2#/SCRIO/GP12	65	DSKCHG#	97	NC
2	RTS2#/JP5	34	PCIRST3#/SCRCLK/GP11	66	IRTX/GP47	98	NC
3	DSR2#	35	VCC	67	VCCH	99	VCC
4	VCC	36	VIDVCC	68	COPEN#	100	SLCT
5	SOUT2/JP6	37	LRESET#	69	VBAT	101	PE
6	SIN2	38	LDRQ#	70	IRRX/GP46	102	BUSY
7	FAN_TAC1	39	SERIRQ	71	GP45	103	ACK#
8	FAN_CTL1	40	LFRAME#	72	PWRON#/GP44	104	SLIN#
9	FAN_TAC2/GP52	41	LAD0	73	PME#/GP54	105	INIT#
10	FAN_CTL2/GP51	42	LAD1	74	GNDD	106	ERR#
11	FAN_TAC3/GP37	43	LAD2	75	PANSWH#/GP43	107	AFD#
12	FAN_CTL3/GP36	44	LAD3	76	PSON#/GP42	108	STB#
13	VID5/GP35	45	KRST#	77	GP53	109	PD0
14	VID4/GP34	46	GA20	78	PWROK2/GP41	110	PD1
15	GNDD	47	PCICLK	79	GP40	111	PD2
16	VID3/GP33	48	PCIRST5#/CLKRUN#/GP50	80	KDAT	112	PD3
17	VID2/GP32	49	CLKIN	81	KCLK	113	PD4
18	VID1/GP31	50	GNDD	82	MDAT	114	PD5
19	VID0/GP30	51	DENSEL#	83	MCLK	115	PD6
20	FAN_CTL4/JSBB2/GP27	52	MTRA#	84	PCIRST4#/SCRPSNT#/GP10	116	PD7
21	FAN_CTL5/JSBB1/GP26	53	MTRB#	85	RSMRST#/CIRRX/GP55	117	GNDD
22	FAN_TAC4/JSBCY/GP25	54	DRVA#	86	GNDA	118	DCD1#
23	FAN_TAC5/JSBCX/GP24	55	DRVB#	87	NC	119	RI1#
24	JSAB2/GP23	56	WDATA#	88	NC	120	CTS1#
25	JSAB1/GP22	57	DIR#	89	NC	121	DTR1#/JP1
26	JSACY/GP21	58	STEP#	90	NC	122	RTS1#/JP2
27	JSACX/GP20	59	HDSEL#	91	PCIRSTIN#	123	DSR1#
28	MIDI_OUT/GP17	60	WGATE#	92	NC	124	SOUT1/JP3
29	MIDI_IN/GP16	61	RDATA#	93	NC	125	SIN1
30	RESETCON#/CIRTX/GP15	62	TRK0#	94	NC	126	DCD2#
31	PCIRST1#/SCRRST/GP14	63	INDEX#	95	ATXPG	127	RI2#
32	PWROK1/SCRPFET#/GP13	64	WPT#	96	NC	128	CTS2#

5. IT8702F Pin Descriptions

Table 5-1. Pin Description of Supplies Signals

Pin(s) No.	Symbol	Attribute	Power	Description
4, 35, 99	**VCC**	PWR	-	***+5V Power Supply.***
67	**VCCH**	PWR	-	***+5V VCC Help Supply.***
69	**VBAT**	PWR	-	***+3.3V Battery Supply.***
36	**VIDVCC**	PWR	-	***VID power supply. (1.2 or 3.3V)***
15, 50, 74, 117	**GNDD**	GND	-	***Digital Ground.***
86	**GNDA**	GND	-	***Analog Ground.***

Table 5-2. Pin Description of LPC Bus Interface Signals

Pin(s) No.	Symbol	Attribute	Power	Description
37	**LRESET#**	DI	VCC	***LPC RESET #.***
38	**LDRQ#**	DO16	VCC	***LPC DMA Request #.*** An encoded signal for DMA channel select.
39	**SERIRQ**	DIO16	VCC	***Serial IRQ.***
40	**LFRAME#**	DI	VCC	***LPC Frame #.*** This signal indicates the start of LPC cycle.
41 – 44	**LAD[0:3]**	DIO16	VCC	***LPC Address/Data 0 - 3.*** 4-bit LPC address/bi-directional data lines. LAD0 is the LSB and LAD3 is the MSB.
47	**PCICLK**	DI	VCC	***PCI Clock.*** 33 MHz PCI clock input for LPC I/F and SERIRQ.
48	**PCIRST5#/CLKRUN#/GP50**	DO16/DIOD16/ DIOD16	VCC	***PCI Reset 5 # / Clock Run # / General Purpose I/O 50.*** • The first function of this pin is PCI Reset 5 #. It is a buffer output of LRESET# if bit1 of Index 2Ch is 0. It will be (LRESET# AND PCIRSTIN#) if bit1 of Index 2Ch is 1. • The second function of this pin is the clock run #. This is an open-drain output and also an input. The IT8702F uses this signal to request starting (or speed up) the clock. CLKRUN# also indicates the clock status. • The third function of this pin is the General Purpose I/O 50. • The function configuration of this pin is decided by the software configuration registers.
73	**PME#/GP54**	DOD8/ DIOD8	VCCH	***Power Management Event # / General Purpose I/O 54.*** • The first function of this pin is the power management event #. It supports the PCI PME# interface. This signal allows the peripheral to request the system to wake up from the D3 (cold) state. • The second function of this pin is the General Purpose I/O Port 5 Bit 4. • The function configuration of this pin is determined by programming the software configuration registers.

Table 5-3. Pin Description of MIDI Interface Signals

Pin(s) No.	Symbol	Attribute	Power	Description
28	**MIDI_OUT/ GP17**	DO8/ DIOD8	VCC	***MIDI Output / General Purpose I/O 17.*** • The first function of this pin is MIDI Output. • The second function of this pin is the General Purpose I/O Port 1 Bit 7. • The function configuration of this pin is determined by programming the software configuration registers.
29	**MIDI_IN/ GP16**	DI/ DIOD8	VCC	***MIDI Input / General Purpose I/O 16.*** • The first function of this pin is MIDI Input. • The second function of this pin is the General Purpose I/O Port 1 Bit 6. • The function configuration of this pin is determined by programming the software configuration registers.

Table 5-4. Pin Description of Game Port Signals

Pin(s) No.	Symbol	Attribute	Power	Description
27	**JSACX/ GP20**	DIOD8/ DIOD8	VCC	***Joystick A Coordinate X / General Purpose I/O 20.*** • The first function of this pin is Joystick A Coordinate X. • The second function of this pin is the General Purpose I/O Port 2 Bit 0. • The function configuration of this pin is determined by programming the software configuration registers.
26	**JSACY/ GP21**	DIOD8/ DIOD8	VCC	***Joystick A Coordinate Y / General Purpose I/O 21.*** • The first function of this pin is Joystick A Coordinate Y. • The second function of this pin is the General Purpose I/O Port 2 Bit 1. • The function configuration of this pin is determined by programming the software configuration registers.
25	**JSAB1/ GP22**	DI/ DIOD8	VCC	***Joystick A Button 1 / General Purpose I/O 22.*** • The first function of this pin is Joystick A Button 1. • The second function of this pin is the General Purpose I/O Port 2 Bit 2. • The function configuration of this pin is determined by programming the software configuration registers.
24	**JSAB2/ GP23**	DI/ DIOD8	VCC	***Joystick A Button 2 / General Purpose I/O 23.*** • The first function of this pin is Joystick A Button 2. • The second function of this pin is the General Purpose I/O Port 2 Bit 3. • The function configuration of this pin is determined by programming the software configuration registers.
23	**FAN_TAC5/ JSBCX/ GP24**	DI/ DIOD8/ DIOD8	VCC	***Joystick B Coordinate X / General Purpose I/O 24.*** • The first function of this pin is Fan Tachometer Input 5. 0 to +5V amplitude fan tachometer input. • The second function of this pin is Joystick B Coordinate X. • The third function of this pin is the General Purpose I/O Port 2 Bit 4. • The function configuration of this pin is determined by programming the software configuration registers.

Pin(s) No.	Symbol	Attribute	Power	Description
22	**FAN_TAC4/ JSBCY/ GP25**	DI/ DIOD8/ DIOD8	VCC	***Joystick B Coordinate Y / General Purpose I/O 25.*** • The first function of this pin is Fan Tachometer Input 4. 0 to +5V amplitude fan tachometer input. • The second function of this pin is Joystick B Coordinate Y. • The third function of this pin is the General Purpose I/O Port 2 Bit 5. • The function configuration of this pin is determined by programming the software configuration registers.
21	**FAN_CTL5/ JSBB1/ GP26**	DOD8 DI/ DIOD8	VCC	***Joystick B Button 1 / General Purpose I/O 26.*** • The first function of this pin is Fan Control Output 5. (PWM output signal to Fan's FET.) • The second function of this pin is Joystick B Button 1. • The third function of this pin is the General Purpose I/O Port 2 Bit 6. • The function configuration of this pin is determined by programming the software configuration registers.
20	**FAN_CTL4/ JSBB2/ GP27**	DOD8/ DI/ DIOD8	VCC	***Joystick B Button 2 / General Purpose I/O 27.*** • The first function of this pin is Fan Control Output 4. (PWM output signal to Fan's FET.) • The second function of this pin is Joystick B Button 2. • The third function of this pin is the General Purpose I/O Port 2 Bit 7. • The function configuration of this pin is determined by programming the software configuration registers.

Table 5-5. Pin Description of Fan Controller Signals

Pin(s) No.	Symbol	Attribute	Power	Description
8	**FAN_CTL1**	DOD8	VCC	***Fan Control Output 1.*** (PWM output signal to Fan's FET.)
10	**FAN_CTL2/ GP51**	DOD8/ DIOD8	VCC	***Fan Control Output 2 / General Purpose I/O 51.*** • The first function of this pin is Fan Control Output 2. (PWM output signal to Fan's FET.) • The second function of this pin is the General Purpose I/O Port 5 Bit 1. • The function configuration of this pin is determined by programming the software configuration registers.
12	**FAN_CTL3/ GP36**	DOD8/ DIOD8	VCC	***Fan Control Output 3 / General Purpose I/O 36.*** • The first function of this pin is Fan Control Output 3. (PWM output signal to Fan's FET.) • The second function of this pin is the General Purpose I/O Port 3 Bit 6. • The function configuration of this pin is determined by programming the software configuration registers.
7	**FAN_TAC1**	DI	VCC	***Fan Tachometer Input 1.*** 0 to +5V amplitude fan tachometer input.
9	**FAN_TAC2/ GP52**	DI/ DIOD8	VCC	***Fan Tachometer Input 2 / General Purpose I/O 52.*** • The first function of this pin is Fan Tachometer Input 2. 0 to +5V amplitude fan tachometer input. • The second function of this pin is the General Purpose I/O Port 5 Bit 2. • The function configuration of this pin is determined by programming the software configuration registers.

Pin(s) No.	Symbol	Attribute	Power	Description
11	**FAN_TAC3/ GP37**	DI/ DIOD8	VCC	***Fan Tachometer Input 3 / General Purpose I/O 37.*** • The first function of this pin is Fan Tachometer Input 3. 0 to +5V amplitude fan tachometer input. • The second function of this pin is the General Purpose I/O Port 5 Bit 2. • The function configuration of this pin is determined by programming the software configuration registers.

Table 5-6. Pin Description of Infrared Port Signals

Pin(s) No.	Symbol	Attribute	Power	Description
30	**RESETCON#/ CIRTX/ GP15**	DI/ DOD8/ DIOD8	VCC	***Reset Connect # / Consumer Infrared Transmit Output / General Purpose I/O 15.*** • The first function of this pin is Reset Connect #. It connects to reset button, and also other reset source on the motherboard. • The second function of this pin is Consumer Infrared Transmit Output. • The Third function of this pin is the General Purpose I/O Port 1 Bit 5. • The function configuration of this pin is determined by programming the software configuration registers.
85	**RSMRST#/ CIRRX/ GP55**	DOD8/ DI/ DIOD8	VCCH	***Resume Reset # / Consumer Infrared Receive Input / General Purpose I/O 55.*** • The first function of this pin is Resume Reset #. It is power good signal of VCCH. The high threshold is 4V ± 0.2V, and the low threshold is 3.5V ± 0.2V • The second function of this pin is Consumer Infrared Receive Input. • The Third function of this pin is the General Purpose I/O Port 5 Bit 5. • The function configuration of this pin is determined by programming the software configuration registers.
70	**IRRX/ GP46**	DI/ DIOD8	VCCH	***Infrared Receive Input / General Purpose I/O 46.*** • The first function of this pin is Infrared Receive Input. • The second function of this pin is the General Purpose I/O Port 4 Bit 6. • The function configuration of this pin is determined by programming the software configuration registers.
66	**IRTX/ GP47**	DO8/ DIOD8	VCC	***Infrared Transmit Output / General Purpose I/O 47.*** • The first function of this pin is Infrared Transmit output. • The second function of this pin is the General Purpose I/O Port 4 Bit 7. • The function configuration of this pin is determined by programming the software configuration registers.

Table 5-7. Pin Description of Serial Port 1 Signals

Pin(s) No.	Symbol	Attribute	Power	Description
125	**SIN1**	DI	VCC	***Serial Data Input 1.*** This input receives serial data from the communications link.
124	**SOUT1/ JP3**	DO8/ DI	VCC	***Serial Data Output 1.*** This output sends serial data to the communications link. This signal is set to a marking state (logic 1) after a Master Reset operation or when the device is in one of the Infrared communications modes. During LRESET#, this pin is input for JP3 power-on strapping option
123	**DSR1#**	DI	VCC	***Data Set Ready 1 #.*** When the signal is low, it indicates that the MODEM or data set is ready to establish a communications link. The DSR# signal is a MODEM status input whose condition can be tested by reading the MSR register.
122	**RTS1#/**	DO8/	VCC	***Request to Send 1 #.***

Pin(s) No.	Symbol	Attribute	Power	Description
	JP2	DI		When this signal is low, this output indicates to the MODEM or data set that the device is ready to send data. RTS# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, RTS# is set to its inactive state. *During LRESET#, this pin is input for JP2 power-on strapping option*
121	**DTR1#/ JP1**	DO8/ DI	VCC	***Data Terminal Ready 1 #.*** DTR# is used to indicate to the MODEM or data set that the device is ready to exchange data. DTR# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, DTR# is set to its inactive state. *During LRESET#, this pin is input for JP1 power-on strapping option*
120	**CTS1#**	DI	VCC	***Clear to Send 1 #.*** When the signal is low, it indicates that the MODEM or data set is ready to accept data. The CTS# signal is a MODEM status input whose condition can be tested by reading the MSR register.
119	**RI1#**	DI	VCC	***Ring Indicator 1 #.*** When the signal is low, it indicates that a telephone ring signal has been received by the MODEM. The RI# signal is a MODEM status input whose condition can be tested by reading the MSR register.
118	**DCD1#**	DI	VCC	***Data Carrier Detect 1 #.*** When the signal is low, it indicates that the MODEM or data set has detected a carrier. The DCD# signal is a MODEM status input whose condition can be tested by reading the MSR register.

Table 5-8. Pin Description of Serial Port 2 Signals

Pin(s) No.	Symbol	Attribute	Power	Description
6	**SIN2**	DI	VCC	***Serial Data In 2.*** This input receives serial data from the communications link.
5	**SOUT2/JP6**	DO8/DI	VCC	***Serial Data Out 2.*** This output sends serial data to the communications link. This signal is set to a marking state (logic 1) after a Master Reset operation or when the device is in one of the Infrared communications modes. *During LRESET#, this pin is input for JP6 power-on strapping option*
3	**DSR2#**	DI	VCC	***Data Set Ready 2 #.*** When low, indicates that the MODEM or data set is ready to establish a communications link. The DSR# signal is a MODEM status input whose condition can be tested by reading the MSR register.
2	**RTS2#/JP5**	DO8/DI	VCC	***Request to Send 2 #.*** When low, this output indicates to the MODEM or data set that the device is ready to send data. RTS# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, RTS# is set to its inactive state. *During LRESET#, this pin is input for JP5 power-on strapping option*
1	**DTR2#/ JP4**	DO8/DI	VCC	***Data Terminal Ready 2 #.*** DTR# is used to indicate to the MODEM or data set that the device is ready to exchange data. DTR# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, DTR# is set to its inactive state.

Pin(s) No.	Symbol	Attribute	Power	Description
				During LRESET#, this pin is input for JP4 power-on strapping option
128	**CTS2#**	DI	VCC	***Clear to Send 2 #.*** When low, indicates that the MODEM or data set is ready to accept data. The CTS# signal is a MODEM status input whose condition can be tested by reading the MSR register.
127	**RI2#**	DI	VCC	***Ring Indicator 2 #.*** When low, indicates that a telephone ring signal has been received by the MODEM. The RI# signal is a MODEM status input whose condition can be tested by reading the MSR register.
126	**DCD2#**	DI	VCC	***Data Carrier Detect 2 #.*** When low, indicates that the MODEM or data set has detected a carrier. The DCD# signal is a MODEM status input whose condition can be tested by reading the MSR register.

Table 5-9. Pin Description of Parallel Port Signals

Pin(s) No.	Symbol	Attribute	Power	Description
100	**SLCT**	DI	VCC	***Printer Select.*** This signal goes high when the line printer has been selected.
101	**PE**	DI	VCC	***Printer Paper End.*** This signal is set high by the printer when it runs out of paper.
102	**BUSY**	DI	VCC	***Printer Busy.*** This signal goes high when the line printer has a local operation in progress and cannot accept data.
103	**ACK#**	DI	VCC	***Printer Acknowledge #.*** This signal goes low to indicate that the printer has already received a character and is ready to accept another one.
104	**SLIN#**	DIO24	VCC	***Printer Select Input #.*** When the signal is low, the printer is selected. This signal is derived from the complement of bit 3 of the printer control register.
105	**INIT#**	DIO24	VCC	***Printer Initialize #.*** When the signal is low, the printer is selected. This signal is derived from the complement of bit 3 of the printer control register.
106	**ERR#**	DI	VCC	***Printer Error #.*** When the signal is low, it indicates that the printer has encountered an error. The error message can be read from bit 3 of the printer status register.
107	**AFD#**	DIO24	VCC	***Printer Auto Line Feed #.*** When the signal is low, it is derived from the complement of bit 1 of the printer control register and is used to advance one line after each line is printed.
108	**STB#**	DI	VCC	***Printer Strobe #.*** When the signal is low, it is the complement of bit 0 of the printer control register and is used to strobe the printing data into the printer.
109 – 116	**PD[0:7]**	DIO24	VCC	***Parallel Port Data [0:7].*** This bus provides a byte-wide input or output to the system. The eight lines are held in a high impedance state when the port is deselected.

Table 5-10. Pin Description of Floppy Disk Controller Signals

Pin(s) No.	Symbol	Attribute	Power	Description
51	**DENSEL#**	DO40	VCC	***FDD Density Select #.*** DENSEL# is high for high data rates (500 Kbps, 1 Mbps). DENSEL# is low for low data rates (250 Kbps, 300 Kbps).
52	**MTRA#**	DO40	VCC	***FDD Motor A Enable #.*** This signal is active low.
53	**MTRB#**	DO40	VCC	***FDD Motor B Enable #.*** • The function of this pin is FDD Motor B #. This signal is active low.
54	**DRVA#**	DO40	VCC	***FDD Drive A Enable #.*** This signal is active low.
55	**DRVB#**	DO40	VCC	***FDD Drive B Enable #.*** This signal is active low.
56	**WDATA#**	DO40	VCC	***FDD Write Serial Data to the Drive #.*** This signal is active low.
57	**DIR#**	DO40	VCC	***FDD Head Direction #.*** Step in when this signal is low and step out when high during a SEEK operation.
58	**STEP#**	DO40	VCC	***FDD Step Pulse #.*** This signal is active low.
59	**HDSEL#**	DO40	VCC	***FDD Head Select #.*** This signal is active low.
60	**WGATE#**	DO40	VCC	***FDD Write Gage Enable #.*** This signal is active low.
61	**RDATA#**	DI	VCC	***FDD Read Disk Data #.*** This signal is active low. It is serial data input from FDD.
62	**TRK0#**	DI	VCC	***FDD Track 0 #.*** This signal is active low. It indicates that the head of the selected drive is on track 0.
63	**INDEX#**	DI	VCC	***FDD Index #.*** This signal is active low. It indicates the beginning of a disk track.
64	**WPT#**	DI	VCC	***FDD Write Protect #.*** This signal is active low. It indicates that the disk of the selected drive is write-protected.
65	**DSKCHG#**	DI	VCC	***FDD Disk Change #.*** This signal is active low. It senses whether the drive door has been opened or a diskette has been changed.

Table 5-11. Pin Description of Smart Card Reader Interface Signals

Pin(s) No.	Symbol	Attribute	Power	Description
31	**PCIRST1#/ SCRRST/ GP14**	DOD8[Note1]/ DOD8/ DIOD8	VCC	***PCI Reset 1 # / Smart Card Reset / General Purpose I/O 13.*** • The first function of this pin is PCI Reset 1 #. It is a buffer of LRESET#. • The second function of this pin is Smart Card Reset. • The third function of this pin is the General Purpose I/O Port 1 Bit 4. • The function configuration of this pin is determined by programming the software configuration registers.

Pin(s) No.	Symbol	Attribute	Power	Description
32	**PWROK1/ SCRPFET#/ GP13**	DOD8/ DOD8/ DIOD8	VCC	***Power OK 1 of VCC / Smart Card Power FET Control Output # / General Purpose I/O 13.*** • The first function of this pin is Power OK 1 of VCC. • The second function of this pin is Smart Card Power FET Control Output #. The Smart Card Reader interface requires this pin to drive an external Power FET to supply the current for the Smart Card. • The third function of this pin is the General Purpose I/O Port 1 Bit 3. • The function configuration of this pin is determined by programming the software configuration registers.
33	**PCIRST2#/ SCRIO / GP12**	DOD8^{Note1}/ DIOD8/ DIOD8	VCC	***PCI Reset 2 # / Smart Card Serial Data I/O / General Purpose I/O 12.*** • The first function of this pin is PCI Reset 2 #. It is a buffer of LRESET#. • The second function of this pin is Smart Card Serial Data I/O. • The third function of this pin is the General Purpose I/O Port 1 Bit 2. • The function configuration of this pin is determined by programming the software configuration registers.
34	**PCIRST3#/ SCRCLK / GP11**	DOD8^{Note1}/ DOD8/ DIOD8	VCC	***PCI Reset 3 # / Smart Card Clock / General Purpose I/O 11.*** • The first function of this pin is PCI Reset 3 #. It is a buffer of LRESET#. It is a buffer output of LRESET# if bit1 of Index 2Ch is 0. It will be (LRESET# AND PCIRSTIN#) if bit1 of Index 2Ch is 1. • The second function of this pin is Smart Card Clock. Three different card clocks are selectable from this pin: high speed (7.1 MHz), low speed (Default: 3.5 MHz) and a programmable card clock. • The third function of this pin is the General Purpose I/O Port 1 Bit 1. • The function configuration of this pin is determined by programming the software configuration registers.
84	**PCIRST4#/ SCRPSNT#/ GP10**	DOD8^{Note1}/ DI/ DIOD8	VCCH	***PCI Reset 4 # / Smart Card Present Detect # / General Purpose I/O 10.*** • The first function of this pin is PCI Reset 4 #. It is a buffer of LRESET#. • The second function of this pin is Smart Card Present Detect #. This pin provides the Smart Card insertion detection for the Smart Card Reader interface. Upon detecting the insertion of the Smart Card, this pin will trigger the power-on event. • The third function of this pin is the General Purpose I/O Port 1 Bit 0. • The function configuration of this pin is determined by programming the software configuration registers.

Table 5-12. Pin Description of Keyboard Controller Signals

Pin(s) No.	Symbol	Attribute	Power	Description
80	**KDAT**	DIOD24	VCCH	***Keyboard Data.***
81	**KCLK**	DIOD24	VCCH	***Keyboard Clock.***
82	**MDAT**	DIOD24	VCCH	***PS/2 Mouse Data.***
83	**MCLK**	DIOD24	VCCH	***PS/2 Mouse Clock.***
45	**KRST#**	DO16	VCC	***Keyboard Reset #.***
46	**GA20**	DO16	VCC	***Gate Address 20.***

Table 5-13. Pin Description of Miscellaneous Signals

Pin(s) No.	Symbol	Attribute	Power	Description
49	**CLKIN**	DI	VCC	***24 or 48 MHz Clock Input.***
72	**PWRON#/ GP44**	DOD8/ DIOD8	VCCH	***Power On Request Output # / General Purpose I/O 34.*** • The first function of this pin is Power On Request Output #. • The second function of this pin is the General Purpose I/O Port 4 Bit 4. • The function configuration of this pin is determined by programming the software configuration registers.
75	**PANSWH#/ GP43**	DI/ DIOD8	VCCH	***Main Power Switch Button Input # / General Purpose I/O 43.*** • The first function of this pin is Main Power Switch Button Input #. • The second function of this pin is the General Purpose I/O Port 4 Bit 3. • The function configuration of this pin is determined by programming the software configuration registers.
76	**PSON#/ GP42**	DOD8/ DIOD8	VCCH	***Power Supply On-Off Output # / General Purpose I/O 42.*** • The first function of this pin is Power Supply On-Off Control Output #. • The second function of this pin is the General Purpose I/O Port 4 Bit 2. • The function configuration of this pin is determined by programming the software configuration registers.
71	**PSIN/ GP45**	DI/ DIOD8	VCCH	***PSIN Input / General Purpose I/O 45.*** • The first function of this pin is PSIN Input. • The second function of this pin is the General Purpose I/O Port 4 Bit 5. • The function configuration of this pin is determined by programming the software configuration registers.
77	**GP53**	DIOD8	VCCH	***General Purpose I/O 53.*** • The first function of this pin is the General Purpose I/O Port 5 Bit 3. • The function configuration of this pin is determined by programming the software configuration registers.
78	**PWROK2/ GP41**	DOD8/ DIOD8	VCCH	***Power OK 2 of VCC / General Purpose I/O 41.*** • The first function of this pin is Power OK 2 of VCC. • The second function of this pin is the General Purpose I/O Port 4 Bit 1. • The function configuration of this pin is determined by programming the software configuration registers.

Pin(s) No.	Symbol	Attribute	Power	Description
79	**GP40**	DIOD8	VCCH	***General Purpose I/O 40.*** • The first function of this pin is the General Purpose I/O Port 4 Bit 0. • The function configuration of this pin is determined by programming the software configuration registers.
95	**ATXPG**	DI	VCC	***ATX Power Good.*** • ATX Power Good. PWROK1/2 will be (VCC power-level-detect **AND** RESETCON# **AND** PSIN **AND** ATXPG) if bit0 of Index 2Ch is 1, or (VCC power-level-detect **AND** RESETCON# **AND** PSIN) if the bit is 0.
91	**PCIRSTIN#**	DI	VCC	***PCI Reset Input #.*** • PCI Reset Input **#**.
19	**VID0/GP30**	DIO8/ DIOD8	VCC	***Voltage ID 0 / General Purpose I/O 30.*** • The first function of this pin is Voltage ID Input 0. The Voltage ID is the voltage supply readouts from the CPU. This value is read in the VID register. The input threshold can be selected by the power-on strapping of JP6 (pin 2). (2.0/0.8V when JP6=1, 0.8/0.4V when JP6=0) • The second function of this pin is the General Purpose I/O 30. • The function configuration of this pin is decided by the software configuration registers.
18	**VID1/GP31**	DIO8/ DIOD8	VCC	***Voltage ID 1 / General Purpose I/O 31.*** • The first function of this pin is Voltage ID Input 1. The Voltage ID is the voltage supply readouts from the CPU. This value is read in the VID register. The input threshold can be selected by the power-on strapping of JP6 (pin 2). (2.0/0.8V when JP6=1, 0.8/0.4V when JP6=0) • The second function of this pin is the General Purpose I/O 31. • The function configuration of this pin is decided by the software configuration registers.
17	**VID2/GP32**	DIO8/ DIOD8	VCC	***Voltage ID 2 / General Purpose I/O 32.*** • The first function of this pin is Voltage ID Input 2. The Voltage ID is the voltage supply readouts from the CPU. This value is read in the VID register. The input threshold can be selected by the power-on strapping of JP6 (pin 2). (2.0/0.8V when JP6=1, 0.8/0.4V when JP6=0) • The second function of this pin is the General Purpose I/O 32. • The function configuration of this pin is decided by the software configuration registers.
16	**VID3/GP33**	DIO8/ DIOD8	VCC	***Voltage ID 3 / General Purpose I/O 33.*** • The first function of this pin is Voltage ID Input 3. The Voltage ID is the voltage supply readouts from the CPU. This value is read in the VID register. The input threshold can be selected by the power-on strapping of JP6 (pin 2). (2.0/0.8V when JP6=1, 0.8/0.4V when JP6=0)

Pin(s) No.	Symbol	Attribute	Power	Description
				• The second function of this pin is the General Purpose I/O 33. • The function configuration of this pin is decided by the software configuration registers.
14	**VID4/GP34**	DIO8/ DIOD8	VCC	***Voltage ID 4 / General Purpose I/O 34.*** • The first function of this pin is Voltage ID Input 4. The Voltage ID is the voltage supply readouts from the CPU. This value is read in the VID register. The input threshold can be selected by the power-on strapping of JP6 (pin 2). (2.0/0.8V when JP6=1, 0.8/0.4V when JP6=0) • The second function of this pin is the General Purpose I/O 34. • The function configuration of this pin is decided by the software configuration registers.
13	**VID5/GP35**	DIO8/ DIOD8	VCC	***Voltage ID 5 / General Purpose I/O 35.*** • The first function of this pin is Voltage ID Input 5. The Voltage ID is the voltage supply readouts from the CPU. This value is read in the VID register. The input threshold can be selected by the power-on strapping of JP6 (pin 2). (2.0/0.8V when JP6=1, 0.8/0.4V when JP6=0) • The second function of this pin is the General Purpose I/O 35. • The function configuration of this pin is decided by the software configuration registers.
68	**COPEN#**	DIOD8	VCCH or VBAT	***Case Open Detection #.*** • The Case Open Detection is connected to a specially designed low power CMOS flip-flop backed by the battery for case open state preservation during power loss.

Note 1: If the power-on strapping input JP4 is low, the output attributes of these pins will be push-pull.

IO Cell:
DO8: 8mA Digital Output buffer
DOD8: 8mA Digital Open-Drain Output buffer
DO16: 16mA Digital Output buffer
DO24: 24mA Digital Output buffer
DO40: 48mA Digital Output buffer

DIO8: 8mA Digital Input/Output buffer
DIOD8: 8mA Digital Open-Drain Input/Output buffer
DIO16: 16mA Digital Input/Output buffer
DIOD16: 16mA Digital Open-Drain Input/Output buffer
DIO24: 24mA Digital Input/Output buffer
DIOD24: 24mA Digital Open-Drain Input/Output buffer

DI: Digital Input
AI: Analog Input
AO: Analog Output

6. List of GPIO Pins

Table 6-1. General Purpose I/O Group 1 (Set 1)

Pin(s) No.	Symbol	Attribute	Description
84	**PCIRST4#/ SCRPSNT#/ GP10**	DOD8/ DI/DIOD8	***PCI Reset 4 # / Smart Card Present Detect # / General Purpose I/O 10.***
34	**PCIRST3#/ SCRCLK/ GP11**	DOD8/ DOD8/ DIOD8	***PCI Reset 3 # / Smart Card Clock / General Purpose I/O 11.***
33	**PCIRST2#/ SCRIO/GP12**	DOD8/DIOD8/DIOD8	***PCI Reset 2 # / Smart Card Serial Data I/O / General Purpose I/O 12.***
32	**PWROK1/ SCRPFET#/ GP13**	DOD8/ DOD8/ DIOD8	***Power OK 1 of VCC / Smart Card Power FET Control Output # / General Purpose I/O 13.***
31	**PCIRST1#/ SCRRST/ GP14**	DOD8/ DOD8/ DIOD8	***PCI Reset 1 # /Smart Card Reset / General Purpose I/O 14.***
30	**RESETCON# /CIRTX/GP15**	DI/DOD8/ DIOD8	***Reset Connect # /Consumer Infrared Transmit Output / General Purpose I/O 15.***
29	**MIDI_IN/ GP16**	DI/DIOD8	***MIDI Input / General Purpose I/O 16.***
28	**MIDI_OUT/ GP17**	DO8/ DIOD8	***MIDI Output / General Purpose I/O 17.***

Table 6-2. General Purpose I/O Group 2 (Set 2)

Pin(s) No.	Symbol	Attribute	Description
27	**JSACX/ GP20**	DIOD8/ DIOD8	***Joystick A Coordinate X / General Purpose I/O 20.***
26	**JSACY/ GP21**	DIOD8/ DIOD8	***Joystick A Coordinate Y / General Purpose I/O 21.***
25	**JSAB1/ GP22**	DI/DIOD8	***Joystick A Button 1 / General Purpose I/O 22.***
24	**JSAB2/ GP23**	DI/DIOD8	***Joystick A Button 2 / General Purpose I/O 23.***
23	**FAN_TAC5/ JSBCX/ GP24**	DI/ DIOD8/ DIOD8	***Joystick B Coordinate X / General Purpose I/O 24.***
22	**FAN_TAC4/ JSBCY/ GP25**	DI/ DIOD8/ DIOD8	***Joystick B Coordinate Y / General Purpose I/O 25.***
21	**FAN_CTL5/ JSBB1/ GP26**	DOD8/ DI/ DIOD8	***Joystick B Button 1 / General Purpose I/O 26.***
20	**FAN_CTL4/ JSBB2/ GP27**	DOD8/ DI/ DIOD8	***Joystick B Button 2 / General Purpose I/O 27.***

Table 6-3. General Purpose I/O Group 3 (Set 3)

Pin(s) No.	Symbol	Attribute	Description
19	**VID0/GP30**	DIO8/DIOD8	***Voltage ID 0 / General Purpose I/O 30.***
18	**VID1/GP31**	DIO8/DIOD8	***Voltage ID 1 / General Purpose I/O 31.***
17	**VID2/GP32**	DIO8/DIOD8	***Voltage ID 2 / General Purpose I/O 32.***

Pin(s) No.	Symbol	Attribute	Description
16	**VID3/GP33**	DIO8/DIOD8	***Voltage ID 3 / General Purpose I/O 33.***
14	**VID4/GP34**	DIO8/DIOD8	***Voltage ID 4 / General Purpose I/O 34.***
13	**VID5/GP35**	DIO8/DIOD8	***Voltage ID 5 / General Purpose I/O 35.***
12	**FAN_CTL3/GP36**	DOD8/ DIOD8	***Fan Control Output 3 / General Purpose I/O 36.***
11	**FAN_TAC3/GP37**	DI/DIOD8	***Fan Tachometer Input 3 / General Purpose I/O 37.***

Table 6-4. General Purpose I/O Group 4 (Set 4)

Pin(s) No.	Symbol	Attribute	Description
79	**GP40**	DIOD8	***General Purpose I/O 40.***
78	**PWROK2/ GP41**	DOD8/DIOD8	***Power OK 2 of VCC / General Purpose I/O 41.***
76	**PSON#/ GP42**	DOD8/ DIOD8	***Power Supply On-Off Control Output # / General Purpose I/O 42.***
75	**PANSWH#/GP43**	DI/DIOD8	***Main Power Switch Button Input # / General Purpose I/O 43.***
72	**PWRON#/ GP44**	DOD8/ DIOD8	***Power On Request Output # / General Purpose I/O 44.***
71	**PSIN/GP45**	DI/DIOD8	***PSIN Input / General Purpose I/O 45.***
70	**IRRX/GP46**	DI/DIOD8	***Infrared Receive Input / General Purpose I/O 46.***
66	**IRTX/GP47**	DO8/ DIOD8	***Infrared Transmit Output / General Purpose I/O 47.***

Table 6-5. General Purpose I/O Group 5 (Set 5)

Pin(s) No.	Symbol	Attribute	Description
48	**PCIRST5#/ CLKRUN#/ GP50**	DO8/ DIOD16/ DIOD16	***PCIRST5#/Clock Run # / General Purpose I/O 50.***
10	**FAN_CTL2/GP51**	DOD8/ DIOD8	***Fan Control Output 2 / General Purpose I/O 51.***
9	**FAN_TAC2/GP52**	DI/DIOD8	***Fan Tachometer Input 2 / General Purpose I/O 52.***
77	**GP53**	DIOD8	***General Purpose I/O 53.***
73	**PME#/GP54**	DOD8/ DIOD8	***Power Management Event # / General Purpose I/O 54.***
85	**RSMRST#/ CIRRX /GP55**	DOD8/ DI / DIOD8	***Resume Reset # / Consumer Infrared Receive Input / General Purpose I/O 55.***

7. Power On Strapping Options and Special Pin Routings

Table 7-1. Power On Strapping Options

	Symbol	Value	Description
JP1	KBCEN	1	KBC is enabled.
		0	KBC is disabled.
JP2	KBC_IROM	1	KBC's ROM is built in.
		0	KBC's ROM is external. This is used for custom code verification. A special application circuit is required.
JP3	CHIP_SEL	--	Chip selection in Configuration.
JP4	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# and PCIRST5# are enhanced open-drain. It drives high about 10~20 ns when the signal transits from low to high, and then Hi-Z.
		0	The output buffers are push-pull.
JP5	FAN_CTL_SEL	1	The default value of FAN Controller Index 15h/16h/17h is 00h.
		0	The default value of FAN Controller Index 15h/16h/17h is 40h.
JP6	VID_ISEL	1	The threshold voltage of VID is 2.0/0.8V.
		0	The threshold voltage of VID is 0.8/0.4V.

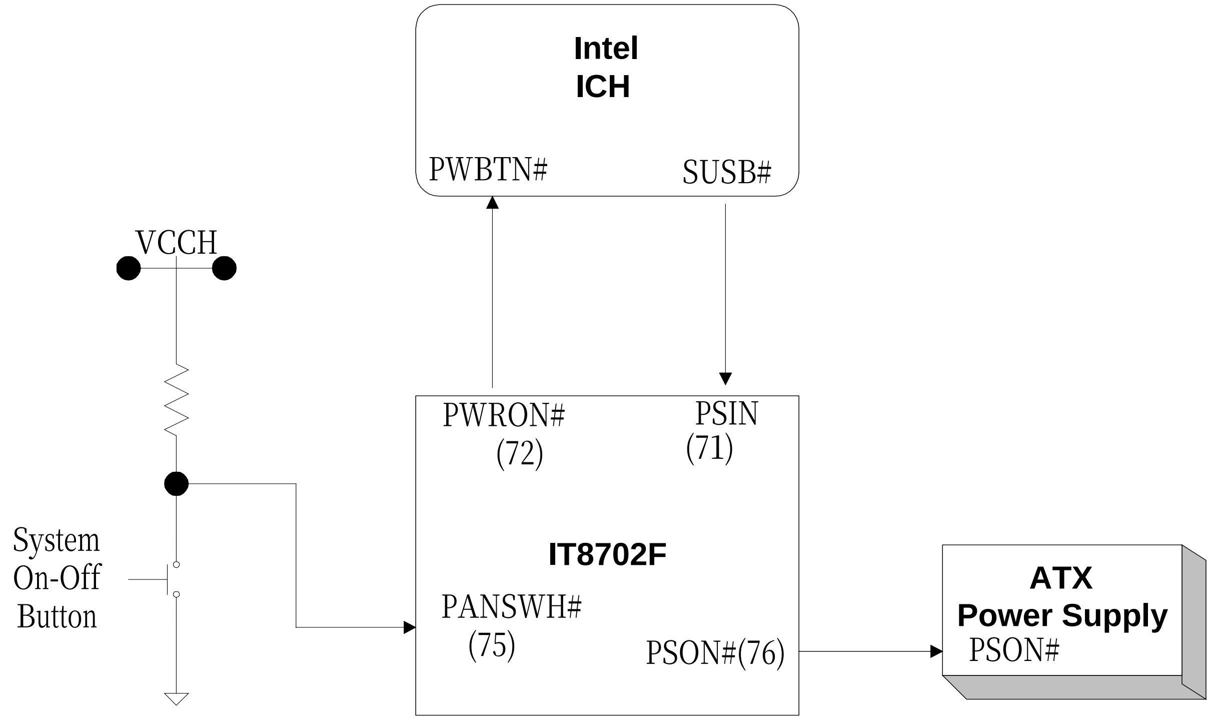

Intel
ICH
PWBTN#
SUSB#
VCCH
System
On-Off
Button
PWRON#
(72)
PSIN
(71)
IT8702F
PANSWH#
(75)
PSON#(76)
ATX
Power Supply
PSON#

Figure 7-1. IT8702F Special Applications Circuitry for Intel ICH

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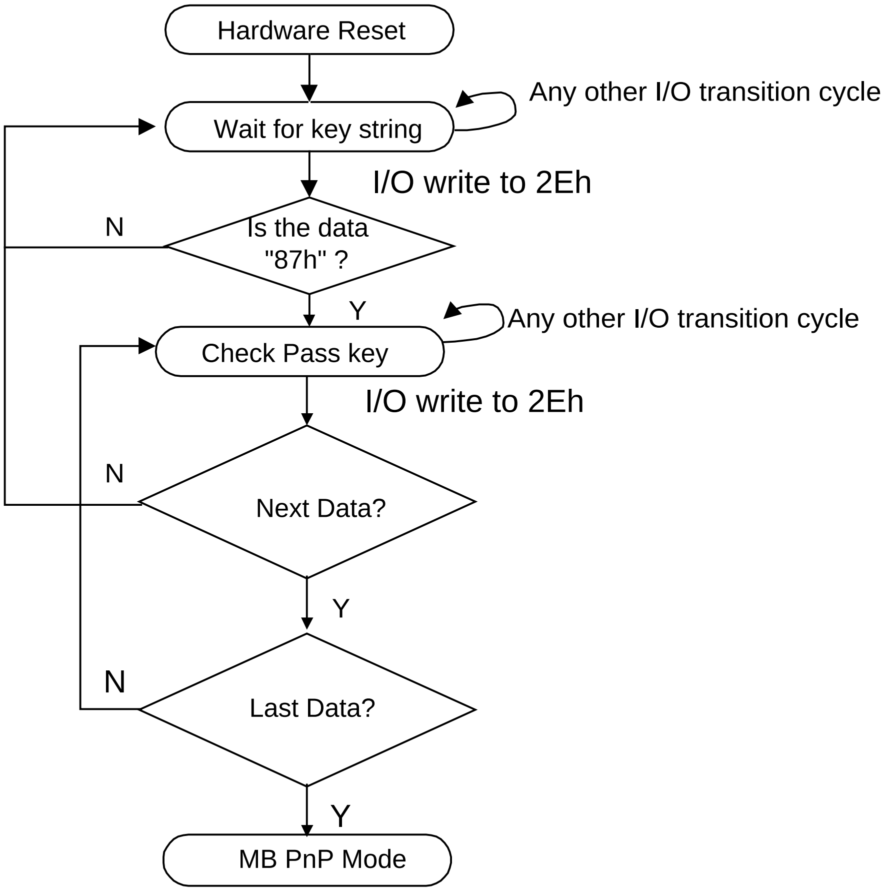
8. Configuration

8.1 Configuring Sequence Description

After the hardware reset or power-on reset, the IT8702F enters the normal mode with all logical devices disabled except KBC. The initial state (enable bit) of this logical device (KBC) is determined by the state of pin 121 (DTR1#) at the falling edge of the system reset during power-on reset.


Hardware Reset
Any other I/O transition cycle
Wait for key string
I/O write to 2Eh
N
Is the data "87h" ?
Y
Any other I/O transition cycle
Check Pass key
I/O write to 2Eh
N
Next Data?
Y
N
Last Data?
Y
MB PnP Mode

There are three steps to completing the configuration setup: (1) Enter the MB PnP Mode; (2) Modify the data of configuration registers; (3) Exit the MB PnP Mode. Undesired result may occur if the MB PnP Mode is not exited normally.

(1) Enter the MB PnP Mode

To enter the MB PnP Mode, four special I/O write operations are to be performed during Wait for Key state. To ensure the initial state of the key-check logic, it is necessary to perform four write operations to the Special Address port (2Eh). Two different enter keys are provided to select configuration ports (2Eh/2Fh or 4Eh/4Fh) of the next step.

	Address port	Data port
87h, 01h, 55h, 55h;	2Eh	2Fh
or 87h, 01h, 55h, AAh;	4Eh	4Fh

(2) Modify the Data of the Registers

All configuration registers can be accessed after entering the MB PnP Mode. Before accessing a selected register, the content of Index 07h must be changed to the LDN to which the register belongs, except some Global registers.

(3) Exit the MB PnP Mode

Set bit 1 of the configure control register (Index=02h) to “1” to exit the MB PnP Mode.

8.2 Description of the Configuration Registers

All the registers except APC/PME’ registers will be reset to the default state when RESET is activated.

Table 8-1. Global Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
All	02h	W	NA	Configure Control
All	07h	R/W	NA	Logical Device Number (LDN)
All	20h	R	87h	Chip ID Byte 1
All	21h	R	02h	Chip ID Byte 2
All	22h	W-R	07h	Configuration Select and Chip Version
All	23h	R/W	00h	Clock Selection Register
All	24h	R/W	00h	Software Suspend
07h Note1	25h	R/W	01h	GPIO Set 1 Multi-Function Pin Selection Register
07h Note1	26h	R/W	00h	GPIO Set 2 Multi-Function Pin Selection Register
07h Note1	27h	R/W	00h	GPIO Set 3 Multi-Function Pin Selection Register
07h Note1	28h	R/W	40h	GPIO Set 4 Multi-Function Pin Selection Register
07h Note1	29h	R/W	00h	GPIO Set 5 Multi-Function Pin Selection Register
07h Note1	2Ah	R/W	00h	Extended 1 Multi-Function Pin Selection Register
All	2Bh	R/W	00h	Logical Block Configuration Lock Register
07h Note1	2Ch	R/W	00h	Extended 2 Multi-Function Pin Selection Register
F4h Note1	2Eh	R/W	00h	Test 1 Register
F4h Note1	2Fh	R/W	00h	Test 2 Register

Table 8-2. FDC Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
00h	30h	R/W	00h	FDC Activate
00h	60h	R/W	03h	FDC Base Address MSB Register
00h	61h	R/W	F0h	FDC Base Address LSB Register
00h	70h	R/W	06h	FDC Interrupt Level Select
00h	74h	R/W	02h	FDC DMA Channel Select
00h	F0h	R/W	00h	FDC Special Configuration Register 1
00h	F1h	R/W	00h	FDC Special Configuration Register 2

Table 8-3. Serial Port 1 Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
01h	30h	R/W	00h	Serial Port 1 Activate
01h	60h	R/W	03h	Serial Port 1 Base Address MSB Register
01h	61h	R/W	F8h	Serial Port 1 Base Address LSB Register
01h	70h	R/W	04h	Serial Port 1 Interrupt Level Select
01h	F0h	R/W	00h	Serial Port 1 Special Configuration Register 1

LDN	Index	R/W	Reset	Configuration Register or Action
01h	F1h	R/W	50h	Serial Port 1 Special Configuration Register 2
01h	F2h	R/W	00h	Serial Port 1 Special Configuration Register 3
01h	F3h	R/W	7Fh	Serial Port 1 Special Configuration Register 4

Table 8-4. Serial Port 2 Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
02h	30h	R/W	00h	Serial Port 2 Activate
02h	60h	R/W	02h	Serial Port 2 Base Address MSB Register
02h	61h	R/W	F8h	Serial Port 2 Base Address LSB Register
02h	70h	R/W	03h	Serial Port 2 Interrupt Level Select
02h	F0h	R/W	00h	Serial Port 2 Special Configuration Register 1
02h	F1h	R/W	50h	Serial Port 2 Special Configuration Register 2
02h	F2h	R/W	00h	Serial Port 2 Special Configuration Register 3
02h	F3h	R/W	7Fh	Serial Port 2 Special Configuration Register 4

Table 8-5. Parallel Port Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
03h	30h	R/W	00h	Parallel Port Activate
03h	60h	R/W	03h	Parallel Port Primary Base Address MSB Register
03h	61h	R/W	78h	Parallel Port Primary Base Address LSB Register
03h	62h	R/W	07h	Parallel Port Secondary Base Address MSB Register
03h	63h	R/W	78h	Parallel Port Secondary Base Address LSB Register
03h	70h	R/W	07h	Parallel Port Interrupt Level Select
03h	74h	R/W	03h	Parallel Port DMA Channel Select [Note2]
03h	F0h	R/W	03h [Note3]	Parallel Port Special Configuration Register

Table 8-6. FAN Controller Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
04h	30h	R/W	00h	FAN Controller Activate
04h	60h	R/W	02h	FAN Controller Base Address MSB Register
04h	61h	R/W	90h	FAN Controller Base Address LSB Register
04h	62h	R/W	02h	PME Direct Access Base Address MSB Register
04h	63h	R/W	30h	PME Direct Access Base Address LSB Register
04h	70h	R/W	09h	FAN Controller Interrupt Level Select
04h	F0h	R/W	00h	APC/PME Event Enable Register
04h	F1h	R/W	00h	APC/PME Status Register
04h	F2h	R/W	00h	APC/PME Control Register 1

LDN	Index	R/W	Reset	Configuration Register or Action
04h	F3h	R/W	00h	FAN Controller Special Configuration Register
04h	F4h	R-R/W	00h	APC/PME Control Register 2
04h	F5h	R/W	-	APC/PME Special Code Index Register
04h	F6h	R/W	-	APC/PME Special Code Data Register

Table 8-7. KBC(Keyboard) Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
05h	30h	R/W	[Note4]	KBC Activate
05h	60h	R/W	00h	KBC Data Base Address MSB Register
05h	61h	R/W	60h	KBC Data Base Address LSB Register
05h	62h	R/W	00h	KBC Command Base Address MSB Register
05h	63h	R/W	64h	KBC Command Base Address LSB Register
05h	70h	R/W	01h	KBC Interrupt Level Select
05h	71h	R-R/W	02h	KBC Interrupt Type [Note5]
05h	F0h	R/W	00h	KBC Special Configuration Register

Table 8-8. KBC(Mouse) Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
06h	30h	R/W	00h	KBC (Mouse) Activate
06h	70h	R/W	0Ch	KBC (Mouse) Interrupt Level Select
06h	71h	R-R/W	02h	KBC (Mouse) Interrupt Type [Note5]
06h	F0h	R/W	00h	KBC (Mouse) Special Configuration Register

Table 8-9. GPIO Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
07h	60h	R/W	00h	SMI# Normal Run Access Base Address MSB Register
07h	61h	R/W	00h	SMI# Normal Run Access Base Address LSB Register
07h	62h	R/W	00h	Simple I/O Base Address MSB Register
07h	63h	R/W	00h	Simple I/O Base Address LSB Register
07h	64h	R/W	00h	Panel Button De-bounce Base Address MSB Register
07h	65h	R/W	00h	Panel Button De-bounce Base Address LSB Register
07h	70h	R/W	00h	Panel Button De-bounce Interrupt Level Select Register
07h	71h	R/W	00h	Watch Dog Timer Control Register
07h	72h	R/W	00h	Watch Dog Timer Configuration Register
07h	73h	R/W	00h	Watch Dog Timer Time-out Value Register
07h	B0h	R/W	00h	GPIO Set 1 Pin Polarity Register
07h	B1h	R/W	00h	GPIO Set 2 Pin Polarity Register
07h	B2h	R/W	00h	GPIO Set 3 Pin Polarity Register
07h	B3h	R/W	00h	GPIO Set 4 Pin Polarity Register
07h	B4h	R/W	00h	GPIO Set 5 Pin Polarity Register
07h	B8h	R/W	00h	GPIO Set 1 Pin Internal Pull-up Enable Register
07h	B9h	R/W	00h	GPIO Set 2 Pin Internal Pull-up Enable Register
07h	BAh	R/W	00h	GPIO Set 3 Pin Internal Pull-up Enable Register
07h	BBh	R/W	00h	GPIO Set 4 Pin Internal Pull-up Enable Register
07h	BCh	R/W	00h	GPIO Set 5 Pin Internal Pull-up Enable Register
07h	C0h	R/W	01h	Simple I/O Set 1 Enable Register
07h	C1h	R/W	00h	Simple I/O Set 2 Enable Register
07h	C2h	R/W	00h	Simple I/O Set 3 Enable Register
07h	C3h	R/W	40h	Simple I/O Set 4 Enable Register
07h	C4h	R/W	00h	Simple I/O Set 5 Enable Register
07h	C8h	R/W	01h	Simple I/O Set 1 Output Enable Register
07h	C9h	R/W	00h	Simple I/O Set 2 Output Enable Register
07h	CAh	R/W	00h	Simple I/O Set 3 Output Enable Register
07h	CBh	R/W	40h	Simple I/O Set 4 Output Enable Register
07h	CCh	R/W	00h	Simple I/O Set 5 Output Enable Register

Table 8-10. GPIO Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
07h	D0h	R/W	00h	Panel Button De-bounce Control Register
07h	D1h	R/W	00h	Panel Button De-bounce Set 1 Enable Register
07h	D2h	R/W	00h	Panel Button De-bounce Set 2 Enable Register
07h	D3h	R/W	00h	Panel Button De-bounce Set 3 Enable Register
07h	D4h	R/W	00h	Panel Button De-bounce Set 4 Enable Register
07h	D5h	R/W	00h	Panel Button De-bounce Set 5 Enable Register
07h	E3h	R/W	00h	IRQ3 External Routing Input Pin Mapping Register
07h	E4h	R/W	00h	IRQ4 External Routing Input Pin Mapping Register
07h	E5h	R/W	00h	IRQ5 External Routing Input Pin Mapping Register
07h	E6h	R/W	00h	IRQ6 External Routing Input Pin Mapping Register
07h	E7h	R/W	00h	IRQ7 External Routing Input Pin Mapping Register
07h	E9h	R/W	00h	IRQ9 External Routing Input Pin Mapping Register
07h	EAh	R/W	00h	IRQ10 External Routing Input Pin Mapping Register
07h	EBh	R/W	00h	IRQ11 External Routing Input Pin Mapping Register
07h	ECh	R/W	00h	IRQ12 External Routing Input Pin Mapping Register
07h	EEh	R/W	00h	IRQ14 External Routing Input Pin Mapping Register
07h	EFh	R/W	00h	IRQ15 External Routing Input Pin Mapping Register
07h	F0h	R/W	00h	SMI# Control Register 1
07h	F1h	R/W	00h	SMI# Control Register 2
07h	F2h	R/W	00h	SMI# Status Register 1
07h	F3h	R/W	00h	SMI# Status Register 2
07h	F4h	R/W	00h	SMI# Pin Mapping Register
07h	F5h	R/W	00h	Hardware Monitor Thermal Output Pin Mapping Register
07h	F6h	R/W	00h	Hardware Monitor Alert Beep Pin Mapping Register
07h	F7h	R/W	00h	Keyboard Lock Pin Mapping Register
07h	F8h	R/W	00h	GP LED Blinking 1 Pin Mapping Register
07h	F9h	R/W	00h	GP LED Blinking 1 Control Register
07h	FAh	R/W	00h	GP LED Blinking 2 Pin Mapping Register
07h	FBh	R/W	00h	GP LED Blinking 2 Control Register
07h	FCh	R/W-R	--h	VID Input Register
07h	FDh	R/W	00h	VID Output Register

Table 8-11. MIDI Port Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
08h	30h	R/W	00h	MIDI Port Activate
08h	60h	R/W	03h	MIDI Port Base Address MSB Register
08h	61h	R/W	00h	MIDI Port Base Address LSB Register
08h	70h	R/W	0Ah	MIDI Port Interrupt Level Select
08h	F0h	R/W	00h	MIDI Port Special Configuration Register

Table 8-12. Game Port Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
09h	30h	R/W	00h	Game Port Activate
09h	60h	R/W	02h	Game Port Base Address MSB Register
09h	61h	R/W	01h	Game Port Base Address LSB Register

Table 8-13. Consumer IR Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
0Ah	30h	R/W	00h	Consumer IR Activate
0Ah	60h	R/W	03h	Consumer IR Base Address MSB Register
0Ah	61h	R/W	10h	Consumer IR Base Address LSB Register
0Ah	70h	R/W	0Bh	Consumer IR Interrupt Level Select
0Ah	F0h	R/W	00h	Consumer IR Special Configuration Register

Note 1: All these registers can be read from all LDNs.
Note 2: When the ECP mode is not enabled, this register is **read only** as “04h”, and cannot be written.
Note 3: When the bit 2 of the Primary Base Address LSB Register of Parallel Port is set to 1, the EPP mode cannot be enabled. Bit 0 of this register is always 0.
Note 4: The initial value of the activate bit of KBC is determined by the latched state of DTR1# at the rising edge of the LRESET# signal.
Note 5: These registers are **read only** unless the write enable bit (Index=F0h) is asserted.

8.2.1 Logical Device Base Address

The base I/O range of logical devices shown below is located in the base I/O address range of each logical device.

Table 8-14. Base Address of Logical Devices

Logical Devices	Address	Notes
LDN=0 FDC	Base + (2 - 5) and + 7	
LDN=1 SERIAL PORT 1	Base + (0 -7)	
LDN=2 SERIAL PORT 2	Base1 + (0 -7)	COM port

Logical Devices	Address	Notes
LDN=3 PARALLEL PORT	Base1 + (0 -3) Base1 + (0 -7) Base1 + (0 -3) and Base2 + (0 -3) Base1 + (0 -7) and Base2 + (0 -3) Base3	SPP SPP+EPP SPP+ECP SPP+EPP+ECP POST data port
LDN=4 FAN Controller	Base1 + (0 -7) Base2 + (0 -3)	FAN Controller PME#
LDN=5 KBC	Base1 + Base2	KBC
LDN=8 MIDI port	Base + (0 -1)	
LDN=9 Game Port	Base	
LDN=A Consumer IR	Base + (0 -7)	

8.3 Global Configuration Registers (LDN: All)

8.3.1 Configure Control (Index=02h)

This register is **write only**. Its values are not sticky; that is to say, a hardware reset will automatically clear the bits, and does not require the software to clear them.

Bit	Description
7-2	**Reserved**
1	Returns to the "Wait for Key" state. This bit is used when the configuration sequence is completed.
0	Resets all logical devices and restores configuration registers to their power-on states.

8.3.2 Logical Device Number (LDN, Index=07h)

This register is used to select the current logical devices. By reading from or writing to the configuration of I/O, Interrupt, DMA and other special functions, all registers of the logical devices can be accessed. In addition, ACTIVATE command is only effective for the selected logical devices. This register is **read/write**.

8.3.3 Chip ID Byte 1 (Index=20h, Default=87h)

This register is the Chip ID Byte 1 and is **read only**. Bits [7:0]=87h when read.

8.3.4 Chip ID Byte 2 (Index=21h, Default=02h)

This register is the Chip ID Byte 2 and is **read only**. Bits [7:0]=02h when read.

8.3.5 Configuration Select and Chip Version (Index=22h, Default=07h)

Bit	Description
7	**Configuration Select** This bit is used to select the chip, which needs to be configured. When there are two IT8702F chips in a system, and a "1" is written, this bit will select JP3=1 (power-on strapping value of SOUT1) to be configured. The chip with JP3=0 will exit the configuration mode. To write "0", the chip with JP3=0 will be configured and the chip with JP3=0 will exit. If no write operations occur on this register, both chips will be configured.
6-4	**Reserved**
3-0	**Version** 4h = Version D 5h = Version G 6h = Version H 7h = Version I See **Application Note** that shows how to built a single design which accepts any versions of this chip.

8.3.6 Clock Selection Register (Index=23h, Default=00h)

Bit	Description
7-6	**XLOCK select** These two bits determine XLOCK function. 00: Software XLOCK (default) 01: Reserved

Bit	Description
	10: Pin 48 (GP50) **11: Pin 11 (GP37)**
5	**Reserved**
4	**Clock Source Select of Watch Dog Timer** 0: Internal oscillating clock (default) 1: External CLKIN
3	Selects the delay of PWROK1/2. 0: POWOK1/2 will be delayed 300 ~600ms from VCC5V > 4.0V. 1: POWOK1/2 will be delayed 150 ~300ms from VCC5V > 4.0V.
2-1	**Reserved**
0	**CLKIN Frequency** 0: 48 MHz. 1: 24 MHz.

8.3.7 Software Suspend (Index=24h, Default=00h, MB PnP)

This register is the Software Suspend register. When the bit 0 is set, the IT8702F enters the “Software Suspend” state. All the devices, except KBC, remain inactive until this bit is cleared or when the wake-up event occurs. The wake-up event occurs at any transition on signals RI1# (pin 119) and RI2# (pin 127).

8.3.8 GPIO Set 1 Multi-Function Pin Selection Register (Index=25h, Default=01h)

If the enabled bits are not set, the multi-function pins will perform the original functions. On the other hand, if they are set, they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	**Function Selection of pin 28** 0: MIDI Output (MIDI_OUT) 1: General Purpose I/O 17 (GP17)
6	**Function Selection of pin 29** 0: MIDI Input (MIDI_IN) 1: General Purpose I/O 16 (GP16)
5	**Function Selection of pin 30, if bit5 of index 2A is 1.** 0: Consumer Infrared Transmit Output (CIRTX) 1: General Purpose I/O 15 (GP15)
4	**Function Selection of pin 31, if bit4 of index 2A is 1.** 0: Smart Card Reset (SCRRST) 1: General Purpose I/O 14 (GP14)
3	**Function Selection of pin 32, if bit3 of index 2A is 1.** 0: Smart Card Power FET Control Output # 1: General Purpose I/O 13 (GP13)
2	**Function Selection of pin 33, if bit2 of index 2A is 1.** 0: Smart Card Serial Data I/O (SCRIO) 1: General Purpose I/O 12 (GP12)
1	**Function Selection of pin 34, if bit1 of index 2A is 1.** 0: Smart Card Clock (SCRCLK) 1: General Purpose I/O 11 (GP11)
0	**Function Selection of pin 84, if bit0 of index 2A is 1.** 0: Smart Card Present Detect# (SCRPSNT#) 1: General Purpose I/O 10 (GP10)

8.3.9 GPIO Set 2 Multi-Function Pin Selection Register (Index=26h, Default=00h)

If the enabled bits are not set, the multi-function pins will perform the original functions. On the other hand, if they are set, they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	**Function Selection of pin 20** 0: Joystick B Button 2 (JSBB2) 1: General Purpose I/O 27 (GP27)
6	**Function Selection of pin 21** 0: Joystick B Button 1 (JSBB1) 1: General Purpose I/O 26 (GP26)
5	**Function Selection of pin 22** 0: Joystick B Coordinate Y (JSBCY) 1: General Purpose I/O 25 (GP25)
4	**Function Selection of pin 23** 0: Joystick B Coordinate X (JSBCX) 1: General Purpose I/O 24 (GP24)
3	**Function Selection of pin 24** 0: Joystick A Button 2 (JSAB2) 1: General Purpose I/O 23 (GP23)
2	**Function Selection of pin 25** 0: Joystick A Button 1 (JSAB1) 1: General Purpose I/O 22 (GP22)
1	**Function Selection of pin 26** 0: Joystick A Coordinate Y (JSACY) 1: General Purpose I/O 21 (GP21)
0	**Function Selection of pin 27** 0: Joystick A Coordinate X (JSACX) 1: General Purpose I/O 20 (GP20)

8.3.10 GPIO Set 3 Multi-Function Pin Selection Register (Index=27h, Default=00h)

If the enabled bits are not set, the multi-function pins will perform the original functions. On the other hand, if they are set, they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	**Function Selection of pin 11** 0: Fan Tachometer Input 3 (FAN_TAC3) 1: General Purpose I/O 37 (GP37)
6	**Function Selection of pin 12** 0: Fan Control Output 3 (FAN_CTL3) 1: General Purpose I/O 36 (GP36)
5	**Function Selection of pin 13** 0: Voltage ID5 (VID5) 1: General Purpose I/O 35 (GP35)
4	**Function Selection of pin 14** 0: Voltage ID4 (VID4) 1: General Purpose I/O 34 (GP34)
3	**Function Selection of pin 16**

Bit	Description
	0: Voltage ID3 (VID3) 1: General Purpose I/O 33 (GP33)
2	**Function Selection of pin 17** 0: Voltage ID2 (VID2) 1: General Purpose I/O 32 (GP32)
1	**Function Selection of pin 18** 0: Voltage ID1 (VID1) 1: General Purpose I/O 31 (GP31)
0	**Function Selection of pin 19** 0: Voltage ID0 (VID0) 1: General Purpose I/O 30 (GP30)

8.3.11 GPIO Set 4 Multi-Function Pin Selection Register (Index=28h, Default=40h)

If the enabled bits are not set, the multi-function pins will perform the original functions. On the other hand, if they are set, they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	**Function Selection of pin 66** 0: Infrared Transmit Output (IRTX). 1: General Purpose I/O 47 (GP47).
6	**Function Selection of pin 70** 0: Infrared Receive Input (IRRX). 1: General Purpose I/O 46 (GP46).
5	**Function Selection of pin 71** 0: PSIN (SUSB#) 1: General Purpose I/O 45 (GP45).
4	**Function Selection of pin 72** 0: Power On Request Output # (PWRON#). 1: General Purpose I/O 44 (GP44).
3	**Function Selection of pin 75** 0: Main Power Switch Button Input # (PANSWH#). 1: General Purpose I/O 43 (GP43).
2	**Function Selection of pin 76** 0: Power Supply ON-Off Control Output # (PSON#). 1: General Purpose I/O 42 (GP42).
1	**Function Selection of pin 78** 0: PWROK2. 1: General Purpose I/O 41 (GP41).
0	**Function Selection of pin 79** 0: Reserved. 1: General Purpose I/O 40 (GP40).

8.3.12 GPIO Set 5 Multi-Function Pin Selection Register (Index=29h, Default=00h)

If the enabled bits are not set, the multi-function pins will perform the original functions. On the other hand, if they are set, they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	**Reserved**

Bit	Description
6	**Reserved.**
5	**Function Selection of pin 85.** 0: Consumer Infrared Receive Input (CIRRX) or RSMRST#. RSMRST# is an open-drain output function, which is active low about 16ms when VCCH5V is power-on. 1: General Purpose I/O 55 (GP55).
4	**Function Selection of pin 73.** 0: Power Management Event # (PME#). 1: General Purpose I/O 54 (GP54).
3	**Function Selection of pin 77.** 0: Reserved. 1: General Purpose I/O 53 (GP53).
2	**Function Selection of pin 9.** 0: Fan Tachometer Input 2 (FAN_TAC2). 1: General Purpose I/O 52 (GP52).
1	**Function Selection of pin 10.** 0: Fan Control Output 2 (FAN_CTL2). 1: General Purpose I/O 51 (GP51).
0	**Function Selection of pin 48.** 0: Clock Run # (CLKRUN#) or PCIRST5#**, selected by bit2 of index 2C.** 1: General Purpose I/O 50 (GP50).

8.3.13 Extended 1 Multi-Function Pin Selection Register (Index=2Ah, Default=00h)

This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	**Reserved.**
6	**Multi-function selection of pin 53.** 0: MTRB#. 1: Thermal Output #.
5	**Extended multi-function selection of 30.** 0: RESETCON#. 1: Determined by bit5 of GPIO Set 1 Multi-function Selection Register (Index 25h).
4	**Extended multi-function selection of pin 31.** 0: PCIRST1#. 1: Determined by bit4 of GPIO Set 1 Multi-function Selection Register (Index 25h).
3	**Extended multi-function selection of pin 32.** 0: PWROK1. 1: Determined by bit3 of GPIO Set 1 Multi-function Selection Register (Index 25h).
2	**Extended multi-function selection of pin 33.** 0: PCIRST2#. 1: Determined by bit2 of GPIO Set 1 Multi-function Selection Register (Index 25h).
1	**Extended multi-function selection of pin 34.** 0: PCIRST3#. 1: Determined by bit1 of GPIO Set 1 Multi-function Selection Register (Index 25h).
0	**Extended multi-function selection of pin 84.** 0: PCIRST4#. 1: Determined by bit0 of GPIO Set 1 Multi-function Selection Register (Index 25h).

8.3.14 Logical Block Lock Register (Index=2Bh, Default=00h)

When lock function is enabled (bit7=1 or XLOCK# is low), configuration registers of the selected logical block and Clock Selection register (index = 23h), and this register will be read-only.

Bit	Description
7	**Software Lock Enable. Once this bit is set to 1 by software, it can be only cleared by hardware reset.** 0: Configuration lock is controlled by XLOCK#. (Default) 1: Configuration registers Logic Blocks selected by bits 6-0 and this register is read-only.
6	**GPIO Select. (LDN7)** 0: GPIO Configuration registers are programmable. 1: GPIO Configuration registers are read-only if LOCK is enabled.
5	**KBC (Keyboard) and KBC (Mouse) Select. (LDN5 and LDN6)** 0: KBC (Keyboard) and KBC (Mouse) Configuration registers are programmable. 1: KBC (Keyboard) and KBC (Mouse) Configuration registers are read-only if LOCK is enabled.
4	**FAN Controller Select. (LDN4)** 0: FAN Controller Configuration registers are programmable. 1: FAN Controller Configuration registers are read-only if LOCK is enabled.
3	**Parallel Port Select. (LDN3)** 0: Parallel Port Configuration registers are programmable. 1: Parallel Port Configuration registers are read-only if LOCK is enabled.
2	**Serial Port 2 Select. (LDN2)** 0: Serial Port 2 Configuration registers are programmable. 1: Serial Port 2 Configuration registers are read-only if LOCK is enabled.
1	**Serial Port 1 Select. (LDN1)** 0: Serial Port 1 Configuration registers are programmable. 1: Serial Port 1 Configuration registers are read-only if LOCK is enabled.
0	**FDC Select. (LDN0) The lock function will not affect bit0 of FDC Special Configuration register (software write protect).** 0: FDC Configuration registers are programmable. 1: FDC Configuration registers are read-only (except Software Write Protect bit) if LOCK is enabled.

8.3.15 Extended 2 Multi-Function Pin Selection Register (Index=2Ch, Default=1Fh)

This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7-5	**Reserved**
4	**Extended multi-function selection of pin 21, 23.** 0: Disable FAN_CTL/FAN_TAC set 5. 1: Enable FAN_CTL/FAN_TAC set 5. (Game port should disable.)
3	**Extended multi-function selection of pin 20, 22.** 0: Disable FAN_CTL/FAN_TAC set 4. 1: Enable FAN_CTL/FAN_TAC set 4. (Game port should disable.)
2	**Extended multi-function selection of pin 48 if bit0 of Index 29h is 0.** 0: Clock Run # (CLKRUN#). 1: PCIRST5#.
1-0	**Reserved.** Must be set to “11b”.

8.3.16 Test 1 Register (Index=2Eh, Default=00h)

This register is the Test 1 Register and is reserved for ITE. It should not be set.

8.3.17 Test 2 Register (Index=2Fh, Default=00h)

This register is the Test 2 Register and is reserved for ITE. It should not be set.

8.4 FDC Configuration Registers (LDN=00h)

8.4.1 FDC Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**FDC Enable** 1: Enabled. 0: Disabled.

8.4.2 FDC Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Read only**, with “0h” for Base Address [15:12].
3-0	Mapped as Base Address [11:8].

8.4.3 FDC Base Address LSB Register (Index=61h, Default=F0h)

Bit	Description
7-3	**Read/write**, mapped as Base Address [7:3].
2-0	**Read only** as “000b.”

8.4.4 FDC Interrupt Level Select (Index=70h, Default=06h)

Bit	Description
7-4	**Reserved** with default “0h.”
3-0	Select the interrupt level [Note1] for FDC.

8.4.5 FDC DMA Channel Select (Index=74h, Default=02h)

Bit	Description
7-3	**Reserved** with default “00h.”
2-0	Select the DMA channel [Note2] for FDC.

8.4.6 FDC Special Configuration Register 1 (Index=F0h, Default=00h)

Bit	Description
7-4	**Reserved** with default “00h.”
3	1: IRQ sharing. 0: Normal IRQ.
2	1: Swap Floppy Drives A, B. 0: Normal.
1	1: 3-mode. 0: AT-mode.
0	1: Software Write Protect. 0: Normal.

8.4.7 FDC Special Configuration Register 2 (Index=F1h, Default=00h)

Bit	Description
7-4	**Reserved** with default “00h.”
3-2	FDD B Data Rate Table Select (DRT1-0).
1-0	FDD A Data Rate Table Select (DRT1-0).

8.5 Serial Port 1 Configuration Registers (LDN=01h)

8.5.1 Serial Port 1 Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**Serial Port 1 Enable** 1: Enabled. 0: Disabled.

8.5.2 Serial Port 1 Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Read only** as “0h” for Base Address[15:12].
3-0	**Read/write**, mapped as Base Address[11:8].

8.5.3 Serial Port 1 Base Address LSB Register (Index=61h, Default=F8h)

Bit	Description
7-3	**Read/write**, mapped as Base Address[7:3].
2-0	**Read only** as “000b.”

8.5.4 Serial Port 1 Interrupt Level Select (Index=70h, Default=04h)

Bit	Description
7-4	**Reserved** with default “0h.”
3-0	Select the interrupt level [Note1] for Serial Port 1.

8.5.5 Serial Port 1 Special Configuration Register 1 (Index=F0h, Default=00h)

Bit	Description
7	**Reserved**
6-4	**Serial Port 1 Mode** [Note3] 000: Standard (default) 001: IrDA 1.0 (HP SIR) 010 : ASKIR 100 : Smart Card Reader (SCR) else : Reserved
3	**Reserved** with default “0.”
2-1	**Clock Source.** 00: 24 MHz/13 (Standard) 01: 24 MHz/12 (MIDI) 10: Reserved 11: Reserved
0	1: IRQ sharing. 0: Normal.

8.5.6 Serial Port 1 Special Configuration Register 2 (Index=F1h, Default=50h)

Bit	Description
7	1: No transmissions delay (40 bits) when the SIR or ASKIR is switched from RX mode to TX mode. 0: Transmission delays (40 bits) when the SIR or ASKIR is switched from RX mode to TX mode.
6	1: No receptions delay (40 bits) when the SIR or ASKIR is switched from TX mode to RX mode. 0: Reception delays (40 bits) when the SIR or ASKIR is switched from TX mode to RX mode.
5	Single Mask Mode: When set, the RX of UART is masked under TX transmission.
4	1: Half Duplex (default). 0: Full Duplex.
3	**SIR RX polarity** 1: Active low 0: Active high
2-0	**Reserved**

8.5.7 Serial Port 1 Special Configuration Register 3 (Index=F2h, Default=00h)

This register is valid only when Serial Port 1's Mode is Smart Card Reader.

Bit	Description
7-3	**Reserved**
2	**SCRPFET# polarity** 1: Active high 0: Active low
1-0	**SCR_CLKSEL1-0** 00: Stop 01: 3.5 MHz 10: 7.1 MHz 11: Special Divisor (96 MHz/DIV96M)

8.5.8 Serial Port 1 Special Configuration Register 4 (Index=F3h, Default=7Fh)

This register is valid only when Serial Port 1's Mode is Smart Card Reader.

Bit	Description
7	**SCRPSNT# Active Phase Control** 1: Active high 0: Active low
6-0	**SCR DIV96M6-0**

8.6 Serial Port 2 Configuration Registers (LDN=02h)

8.6.1 Serial Port 2 Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**Serial Port 2 Enable** 1: Enabled 0: Disabled

8.6.2 Serial Port 2 Base Address MSB Register (Index=60h, Default=02h)

Bit	Description
7-4	**Read only** with “0h” for Base Address [15:12].
3-0	**Read/write**, mapped as Base Address[11:8].

8.6.3 Serial Port 2 Base Address LSB Register (Index=61h, Default=F8h)

Bit	Description
7-3	**Read/write**, mapped as Base Address [7:3].
2-0	**Read only** as “000b.”

8.6.4 Serial Port 2 Interrupt Level Select (Index=70h, Default=03h)

Bit	Description
7-4	**Reserved** with default “0h.”
3-0	Select the interrupt level [Note1] for Serial Port 2.

8.6.5 Serial Port 2 Special Configuration Register 1 (Index=F0h, Default=00h)

Bit	Description
7	**Reserved**
6-4	**Serial Port 2 Mode** [Note3] 000: Standard (default) 001: IrDA 1.0 (HP SIR) 010 : ASKIR 100 : Smart Card Reader (SCR) else : Reserved
3	**Reserved** with default “0.”
2-1	**Clock Source** 00: 24 MHz/13 (Standard) 01: 24 MHz/12 (MIDI) 10: Reserved 11: Reserved
0	1: IRQ sharing 0: Normal

8.6.6 Serial Port 2 Special Configuration Register 2 (Index=F1h, Default=50h)

Bit	Description
7	1: No transmission delay (40 bits) when the SIR or ASKIR is switched from RX mode to TX mode. 0: Transmission delay (40 bits) when the SIR or ASKIR is switched from RX mode to TX mode.
6	1: No reception delay (40 bits) when the SIR or ASKIR is switched from TX mode to RX mode. 0: Reception delay (40 bits) when the SIR or ASKIR is switched from TX mode to RX mode.
5	Single Mask Mode: When set, the RX of UART is masked under TX transmission.
4	1: Half Duplex (default). 0: Full Duplex.
3	**SIR RX polarity** 1: Active low 0: Active high
2-0	**Reserved**

8.6.7 Serial Port 2 Special Configuration Register 3 (Index=F2h, Default=00h)

This register is valid only when Serial Port 2’s Mode is Smart Card Reader.

Bit	Description
7-3	**Reserved**
2	**SCRPFET# polarity.** 1: Active high 0: Active low
1-0	**SCR_CLKSEL1-0.** 00: Stop 01: 3.5 MHz 10: 7.1 MHz 11: Special Divisor (96 MHz/DIV96M)

8.6.8 Serial Port 2 Special Configuration Register 4 (Index=F3h, Default=7Fh)

This register is valid only when Serial Port 2’s Mode is Smart Card Reader.

Bit	Description
7	**SCRPSNT# Active Phase Control** 1: Active high 0: Active low
6-0	**SCR DIV96M6-0**

8.7 Parallel Port Configuration Registers (LDN=03h)

8.7.1 Parallel Port Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**Parallel Port Enable** 1: Enabled 0: Disabled

8.7.2 Parallel Port Primary Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Read only** as “0h” for Base Address[15:12]
3-0	**Read/write**, mapped as Base Address[11:8]

8.7.3 Parallel Port Primary Base Address LSB Register (Index=61h, Default=78h)

If the bit 2 is set to 1, the EPP mode is disabled automatically.

Bit	Description
7-2	**Read/write**, mapped as Base Address[7:2]
1-0	**Read only** as “00b.”

8.7.4 Parallel Port Secondary Base Address MSB Register (Index=62h, Default=07h)

Bit	Description
7-4	**Read only** as “0h” for Base Address[15:12]
3-0	**Read/write**, mapped as Base Address[11:8]

8.7.5 Parallel Port Secondary Base Address LSB Register (Index=63h, Default=78h)

Bit	Description
7-2	**Read/write**, mapped as Base Address[7:2]
1-0	**Read only** as “00b.”

8.7.6 Parallel Port Interrupt Level Select (Index =70h, Default=07h)

Bit	Description
7-4	**Reserved** with default “0h.”
3-0	**Select the interrupt level** [Note1] **for Parallel Port**

8.7.7 Parallel Port DMA Channel Select (Index=74h, Default=03h)

Bit	Description
7-3	**Reserved** with default “00h.”
2-0	**Select the DMA channel** [Note2] **for Parallel Port.**

8.7.8 Parallel Port Special Configuration Register (Index=F0h, Default=03h)

Bit	Description
7-4	**Reserved**
3	1: POST Data Port Disable 0: POST Data Port Enable
2	1: IRQ sharing 0: Normal
1-0	**Parallel Port Modes** 00 : Standard Parallel Port mode (SPP) 01 : EPP mode 10 : ECP mode 11 : EPP mode & ECP mode

If the bit 1 is set, ECP mode is enabled. If the bit 0 is set, EPP mode is enabled. These two bits are independent. However, according to the EPP spec., when Parallel Port Primary Base Address LSB Register bit 2 is set to 1, the EPP mode cannot be enabled.

8.8 FAN Controller Configuration Registers (LDN=04h)

8.8.1 FAN Controller Activate Register (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**FAN Controller Enable.** 1: Enabled 0: Disabled This is a **read/write** register.

8.8.2 FAN Controller Base Address MSB Register (Index=60h, Default=02h)

Bit	Description
7-4	**Read only** as “0h” for Base Address[15:12].
3-0	**Read/write**, mapped as Base Address[11:8].

8.8.3 FAN Controller Base Address LSB Register (Index=61h, Default=90h)

Bit	Description
7-3	**Read/write**, mapped as Base Address[7:3].
2-0	**Read only** as “000b.”

8.8.4 PME Direct Access Base Address MSB Register (Index=62h, Default=02h)

Bit	Description
7-4	**Read only** as “0h” for Base Address[15:12]
3-0	**Read/write**, mapped as Base Address[11:8]

8.8.5 PME Direct Access Base Address LSB Register (Index=63h, Default=30h)

Bit	Description
7-3	**Read/write**, mapped as Base Address[7:3]
2-0	**Read only** as “000b.”

8.8.6 FAN Controller Interrupt Level Select (Index=70h, Default=09h)

Bit	Description
7-4	**Reserved** with default “0h.”
3-0	**Select the interrupt level** [Note1] **for FAN Controller**

8.8.7 APC/PME Event Enable Register (PER) (Index=F0h, Default=00h)

Bit	Description
7	It is set to 1 when VCCH is off. Write 1 to clear this bit. This bit is ineffective if a 0 is written to this bit.
6	0: Smart Card Reader card detect event disabled. 1: Smart Card Reader card detect event enabled.
5	**Reserved** with default “0h.”
4	0: PS/2 Mouse event disabled.

Bit	Description
	1: PS/2 Mouse event enabled.
3	0: Keyboard event disabled. 1: Keyboard event enabled.
2	0: RI2# event disabled. 1: RI2# event enabled.
1	0: RI1# event disabled. 1: RI1# event enabled.
0	0:CIR event disabled. 1:CIR event enabled.

8.8.8 APC/PME Status Register (PSR) (Index=F1h, Default=00h)

Bit	Description
7	It is set to 1 when VCC is ON at previous AC power failure and 0 when VCC is OFF.
6	0: No Smart Card Reader card detect event Detected. 1: Smart Card Reader card detect event Detected.
5	Reserved
4	0: No PS/2 Mouse Event Detected. 1: PS/2 Mouse Event Detected.
3	0: No Keyboard Event Detected. 1: Keyboard Event Detected.
2	0: No RI2# Event Detected. 1: RI2# Event Detected.
1	0: No RI1# Event Detected. 1: RI1# Event Detected.
0	0: No CIR event Detected. 1: CIR event Detected.

8.8.9 APC/PME Control Register 1 (PCR 1) (Index=F2h, Default=00h)

Bit	Description
7	PER and PSR normal run access enable
6	**PME# output control** 0: Enabled 1: Disabled
5	This bit is restored automatically to the previous VCC state before power failure occurs
4	Disables all APC events after the power failure occurs, excluding PANSWH#
3	**Keyboard event mode selection when VCC is ON** 1: Determined by PCR 2 0: Pulse falling edge on KCLK
2	**Mouse event when VCC is OFF** 1: Click Key twice sequentially 0: Pulse falling edge on MCLK
1	**Mouse event when VCC is ON** 1: Click Key twice sequentially 0: Pulse falling edge on MCLK
0	Reserved

8.8.10 FAN Controller Special Configuration Register (Index=F3h, Default=00h)

Bit	Description
7-1	**Reserved**
0	1: IRQ sharing. 0: Normal.

8.8.11 APC/PME Control Register 2 (PCR 2) (Index=F4h, Default=00h)

Bit	Description
7	**Disable KCLK/KDAT and MCLK/MDAT auto-swap** 0: Enabled. 1: Disabled.
6	**Reserved.**
5	**PSON# state when VCCH is switched from OFF to ON** 0: High-Z (default power OFF). 1: Inverting of PSIN.
4	**Masks PANSWH# power-on event.**
3-2	**Key Number of the Keyboard power-up event** 00: 5 (Key string mode), 3 (Stroke keys at same time mode) 01: 4 (Key string mode), 2 (Stroke keys at same time mode) 10: 3 (Key string mode), 1 (Stroke keys at same time mode) 11: 2 (Key string mode), Reserved (Stroke keys at same time mode)
1-0	**Keyboard power-up event mode selection** 00: KCLK falling edge 01: Key string mode 10: Stroke keys at same time mode 11: Reserved

8.8.12 APC/PME Special Code Index Register (Index=F5h)

Bit	Description
7-6	Reserved (should be “00”).
5-0	Indicate which Identification Key Code or CIR code register is to be read/written via 0xF6.

8.8.13 APC/PME Special Code Data Register (Index=F6h)

There are 5 bytes for Key String mode, 3 bytes for Stroke Keys at same time mode and CIR event codes.

8.9 KBC (keyboard) Configuration Registers (LDN=05h)

8.9.1 KBC (keyboard) Activate (Index=30h, Default=01h or 00h)

Bit	Description
7-1	**Reserved**
0	**KBC (keyboard) Enable** 1: Enabled 0: Disabled This is a **read/write** register. The default value depends on the state of the DTR1# when LRESET# is activated. The default value is 1b for the High state of DTR1# when LRESET# is activated. It is 0b for the low state of DTR1# when LRESET# is activated.

8.9.2 KBC (keyboard) Data Base Address MSB Register (Index=60h, Default=00h)

Bit	Description
7-4	**Read only** as “0h” for Base Address [15:12].
3-0	**Read/write,** mapped as Base Address [11:8].

8.9.3 KBC (keyboard) Data Base Address LSB Register (Index=61h, Default=60h)

Bit	Description
7-0	**Read/write**, mapped as Base Address[7:0]

8.9.4 KBC (keyboard) Command Base Address MSB Register (Index=62h, Default=00h)

Bit	Description
7-4	**Read only** as “0h” for Base Address[15:12]
3-0	**Read/write**, mapped as Base Address[11:8]

8.9.5 KBC (keyboard) Command Base Address LSB Register (Index=63h, Default=64h)

Bit	Description
7-0	**Read/write**, mapped as Base Address[7:0]

8.9.6 KBC (keyboard) Interrupt Level Select (Index=70h, Default=01h)

Bit	Description
7-4	**Reserved** with default “0h.”
3-0	**Select the interrupt level** [Note1] **for KBC (keyboard)**

8.9.7 KBC (keyboard) Interrupt Type (Index=71h, Default=02h)

This register indicates the type of interrupt set for KBC (keyboard) and is **read only** as "02h" when bit 0 of the KBC (keyboard) Special Configuration Register is cleared. When bit 0 is set, this type of interrupt can be selected as level or edge trigger.

Bit	Description
7-2	**Reserved**
1	1: High Level 0: Low Level
0	1: Level Type 0: Edge Type

8.9.8 KBC (keyboard) Special Configuration Register (Index=F0h, Default=00h)

Bit	Description
7-5	**Reserved**
4	1: IRQ sharing. 0: Normal.
3	1: KBC's clock 8 MHz. 0: KBC's clock 12 MHz.
2	1: Key lock enabled. 0: Key lock disabled.
1	1: Type of interrupt of KBC (keyboard) can be changed. 0: Type of interrupt of KBC (keyboard) is fixed.
0	1: Enables the External Access ROM of 8042. 0: Internal built-in ROM is used.

8.10 KBC (mouse) Configuration Registers (LDN=06h)

8.10.1 KBC (mouse) Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**KBC (mouse) Enable** 1: Enabled 0: Disabled

8.10.2 KBC (mouse) Interrupt Level Select (Index=70h, Default=0Ch)

Bit	Description
7-4	**Reserved** with default "0h."
3-0	**Select the interrupt level [Note1] for KBC (mouse).**

8.10.3 KBC (mouse) Interrupt Type (Index=71h, Default=02h)

This register indicates the type of interrupt used for KBC (mouse) and is **read only** as "02h" when bit 0 of the KBC (mouse) Special Configuration Register is cleared. When bit 0 is set, the type of interrupt can be selected as level or edge trigger.

Bit	Description
7-2	**Reserved**
1	1: High Level

Bit	Description
	0: Low Level
0	1: Level Type 0: Edge Type

8.10.4 KBC (mouse) Special Configuration Register (Index=F0h, Default=00h)

Bit	Description
7-2	**Reserved** with default “00h.”
1	1: IRQ sharing. 0: Normal.
0	1: Type of interrupt of KBC (mouse) can be changed. 0: Type of interrupt of KBC (mouse) is fixed.

8.11 GPIO Configuration Registers (LDN=07h)

8.11.1 SMI# Normal Run Access Base Address MSB Register (Index=60h, Default=00h)

Bit	Description
7-4	**Read only** as “0h” for Base Address [15:12].
3-0	**Read/write**, mapped as Base Address [11:8].

8.11.2 SMI# Normal Run Access Base Address LSB Register (Index=61h, Default=00h)

Bit	Description
7-0	**Read/write**, mapped as Base Address[7:0].

8.11.3 Simple I/O Base Address MSB Register (Index=62h, Default=00h)

Bit	Description
7-4	**Read only** as “0h” for Base Address [15:12].
3-0	**Read/write**, mapped as Base Address [11:8].

8.11.4 Simple I/O Base Address LSB Register (Index=63h, Default=00h)

Bit	Description
7-0	**Read/write**, mapped as Base Address[7:0].

8.11.5 Panel Button De-bounce Base Address MSB Register (Index=64h, Default=00h)

Bit	Description
7-4	**Read only** as “0h” for Base Address [15:12].
3-0	**Read/write**, mapped as Base Address [11:8].

8.11.6 Panel Button De-bounce Base Address LSB Register (Index=65h, Default=00h)

Bit	Description
7-0	**Read/write**, mapped as Base Address[7:0].

8.11.7 Panel Button De-bounce Interrupt Level Select Register (Index=70h, Default=00h)

Bit	Description
7-4	**Reserved**
3-0	Select the interrupt level [Note1] for Panel Button De-bounce.

8.11.8 Watch Dog Timer Control Register (Index=71h, Default=00h)

Bit	Description
7	**WDT is reset upon a CIR interrupt**
6	**WDT is reset upon a KBC (mouse) interrupt**
5	**WDT is reset upon a KBC (keyboard) interrupt**
4	**WDT is reset upon a read or a write to the Game Port base address**
3-2	**Reserved**
1	**Force Time-out**

Bit	Description
	This bit is self-clearing
0	**WDT Status** 1: WDT value reaches 0. 0: WDT value is not 0.

8.11.9 Watch Dog Timer Configuration Register (Index=72h, Default=00h)

Bit	Description
7	**WDT Time-out value select 1** 1: Second 0: Minute
6	**WDT output through KRST (pulse) enable** 1: Enable. **0: disable**
5	**WDT Time-out value Extra select** 1: 64 ms. 0: Determine by WDT Time-out value select 1 (bit 7 of this register).
4	**WDT output through PWROK1/PWROK2 (pulse) enable** 1: Enable. 0: disable
3-0	**Select the interrupt level [Note1] for WDT**

8.11.10 Watch Dog Timer Time-Out Value Register (Index=73h, Default=00h)

Bit	Description
7-0	**WDT time-out value 7-0**

8.11.11 GPIO Pin Set 1, 2, 3, 4 and 5 Polarity Registers (Index=B0h, B1h, B2h, B3h and B4h, Default=00h)

These registers are used to program the GPIO pin type as polarity inverting or non-inverting.

Bit	Description
7-0	1: Inverting 0: Non-inverting

8.11.12 GPIO Pin Set 1, 2, 3, 4 and 5 Pin Internal Pull-up Enable Registers (Index=B8h, B9h, BAh, BBh and BCh, Default=00h)

These registers are used to enable the GPIO pin internal pull-up.

Bit	Description
7-0	1: Enabled. 0: Disabled.

8.11.13 Simple I/O Set 1, 2, 3, 4 and 5 Enable Registers (Index=C0h, C1h, C2h, C3h and C4h, Default=01h, 00h, 00h, 40h, and 00h)

These registers are used to select the function as the Simple I/O function or the Alternate function.

Bit	Description
7-0	1: Simple I/O function 0: Alternate function

8.11.14 Simple I/O Set 1, 2, 3, 4 and 5 Output Enable Registers (Index=C8h, C9h, CAh, CBh and CCh, Default=01h, 00h, 00h, 40h, and 00h)

These registers are used to determine the direction of the Simple I/O.

Bit	Description
7-0	0: Input mode 1: Output mode

8.11.15 Panel Button De-bounce Control Register (Index=D0h, Default=00h)

Bit	Description
7-5	**Reserved**
4	**IRQ Sharing Enable**
3	**IRQ Output Type**
2	**IRQ Output Enable** 1: Enabled **0: Disabled**
1-0	**De-bounce Time Selection** 00: 8 ms (6 ms ignored, 8 ms passed) 01: 16 ms (12 ms ignored, 16 ms passed) 10: 32 ms (24 ms ignored, 32 ms passed) 11: 64 ms (48 ms ignored, 64 ms passed)

8.11.16 Panel Button De-bounce Set 1, 2, 3, 4 and 5 Enable Registers (Index=D1h, D2h, D3h, D4h and D5h, Default=00h)

These registers are used to enable Panel Button De-bounce for each pin.

Bit	Description
7-0	1: Enabled 0: Disabled

8.11.17 IRQ3-7, 9-12 and 14-15 External Routing Input Pin Mapping Registers (Index=E3h-E7h, E9h-ECh and EEh-EFh, Default=00h)

These registers are used to determine the external routing input pin mappings of IRQ3-7, 9-12 and 14-15.

Bit	Description
7	**Reserved**
6	**IRQ Sharing Enable**
5-0	**Input pin Location. Please see Location mapping table** [Note4]

8.11.18 SMI# Control Register 1 (Index=F0h, Default=00h)

Bit	Description
7	Enables the generation of an SMI# due to MIDI's IRQ (EN_MIDI).
6	Enables the generation of an SMI# due to KBC (Mouse)'s IRQ (EN_MIRQ).
5	Enables the generation of an SMI# due to KBC (Keyboard)'s IRQ (EN_KIRQ).

Bit	Description
4	Enables the generation of an SMI# due to FAN Controller's IRQ (EN_ECIRQ).
3	Enables the generation of an SMI# due to Parallel Port's IRQ (EN_PIRQ).
2	Enables the generation of an SMI# due to Serial Port 2's IRQ (EN_S2IRQ).
1	Enables the generation of an SMI# due to Serial Port 1's IRQ (EN_S1IRQ).
0	Enables the generation of an SMI# due to FDC's IRQ (EN_FIRQ).

8.11.19 SMI# Control Register 2 (Index=F1h, Default=00h)

Bit	Description
7	Forces to clear all the SMI# status register bits, non-sticky.
6	0: Edge trigger 1: Level trigger.
5-3	**Reserved**
2	Enables the generation of an SMI# due to WDT's IRQ (EN_WDT).
1	Enables the generation of an SMI# due to CIR's IRQ (EN_CIR).
0	Enables the generation of an SMI# due to PBD's IRQ (EN_PBD).

8.11.20 SMI# Status Register 1 (Index=F2h, Default=00h)

This register is used to read the status of SMI# inputs.

Bit	Description
7	**MIDI's IRQ**
6	**KBC (PS/2 Mouse)'s IRQ**
5	**KBC (Keyboard)'s IRQ**
4	**FAN Controller's IRQ**
3	**Parallel Port's IRQ**
2	**Serial Port 2's IRQ**
1	**Serial Port 1's IRQ**
0	**FDC's IRQ**

8.11.21 SMI# Status Register 2 (Index=F3h, Default=00h)

This register is used to read the status of SMI# inputs.

Bit	Description
7-3	**Reserved**
2	**WDT's IRQ**
1	**CIR's IRQ**
0	**PBD's IRQ**

8.11.22 SMI# Pin Mapping Register (Index=F4h, Default=00h)

Bit	Description
7-6	**Reserved**
5-0	**SMI# Pin Location** **Please see Location mapping table** [Note4]**.**

8.11.23 Reserved Register (Index=F5h, Default=00h)

8.11.24 Reserved Register (Index=F6h, Default=00h)

8.11.25 Keyboard Lock Pin Mapping Register (Index=F7h, Default=00h)

Bit	Description
7-6	**Reserved**
5-0	**Keyboard Lock Pin Location** **Please see Location mapping table** Note4**.**

8.11.26 GP LED Blinking 1 Pin Mapping Register (Index=F8h, Default=00h)

Bit	Description
7-6	**Reserved**
5-0	**GP LED Blinking 1 Location** **Please see Location mapping table** Note4**.**

8.11.27 GP LED Blinking 1 Control Register (Index=F9h, Default=00h)

Bit	Description
7-4	**Reserved**
3	**GP LED Blinking 1 short low pulse enabled**
2-1	**GP LED 1 Frequency Control.** 00: 4 Hz 01: 1 Hz 10: 1/4 Hz 11: 1/8 Hz
0	**GP LED Blinking 1 Output low enabled**

8.11.28 GP LED Blinking 2 Pin Mapping Register (Index=FAh, Default=00h)

Bit	Description
7-6	**Reserved**
5-0	**GP LED Blinking 2 Location** **Please see Location mapping table** Note4**.**

8.11.29 GP LED Blinking 2 Control Register (Index=FBh, Default=00h)

Bit	Description
7-4	**Reserved**
3	**GP LED Blinking 2 short low pulse enabled.**
2-1	**GP LED 2 Frequency Control.** 00: 4 Hz 01: 1 Hz 10: 1/4 Hz 11: 1/8 Hz
0	**GP LED Blinking 2 Output low enabled.**

8.11.30 VID Input Register (Index=FCh, Default=--h)

Bit	Description
7-6	**Reserved**
5-0	**VID 5-0 inputs** They are read-only. The inputs' thresholds for VID inputs are not TTL level (0.4V for low, 2.2V for high), but special CMOS level (1.5V for low, 2.5V for high)

8.11.31 VID Output Register (Index=FDh, Default=00h)

Bit	Description
7	**VID_OE. VID output enable** 1: output 0: input
6	**Reserved**
5-0	**VID 5-0 output values**

8.12 MIDI Port Configuration Registers (LDN=08h)

8.12.1 MIDI Port Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**MIDI Port Enable** 1: Enabled 0: Disabled

8.12.2 MIDI Port Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Read only** with “0h” for Base Address[15:12].
3-0	**Read/write**, mapped as Base Address[11:8].

8.12.3 MIDI Port Base Address LSB Register (Index=61h, Default=00h)

Bit	Description
7-3	**Read/write**, mapped as Base Address[7:3].
2-0	**Read only** as “000b.”

8.12.4 MIDI Port Interrupt Level Select (Index=70h, Default=0Ah)

Bit	Description
7-4	**Reserved** with default “0h.”
3-0	**Select the interrupt level** [Note1] **for MIDI Port.**

8.12.5 MIDI Port Special Configuration Register (Index=F0h, Default=00h)

Bit	Description
7-1	**Reserved** with default “00h.”
0	1: IRQ sharing. 0: Normal.

8.13 Game Port Configuration Registers (LDN=09h)

8.13.1 Game Port Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**Game Port Enable** 1: Enabled. (If enable, the multi function pin20, 21,22,23 will change to Game port function.) 0: Disabled.

8.13.2 Game Port Base Address MSB Register (Index=60h, Default=02h)

Bit	Description
7-4	**Read only** with “0h” for Base Address[15:12].
3-0	**Read/write**, mapped as Base Address[11:8].

8.13.3 Game Port Base Address LSB Register (Index=61h, Default=01h)

Bit	Description
7-0	**Read/write**, mapped as Base Address[7:0].

8.14 Consumer IR Configuration Registers (LDN=0Ah)

8.14.1 Consumer IR Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**Consumer IR Enable** 1: Enabled. 0: Disabled.

8.14.2 Consumer IR Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Read only** with "0h" for Base Address[15:12].
3-0	**Read/write**, mapped as Base Address[11:8].

8.14.3 Consumer IR Base Address LSB Register (Index=61h, Default=10h)

Bit	Description
7-3	**Read/write**, mapped as Base Address[7:3].
2-0	**Read only** as "000b."

8.14.4 Consumer IR Interrupt Level Select (Index=70h, Default=0Bh)

Bit	Description
7-4	**Reserved** with default "0h."
3-0	**Select the interrupt level [Note1] for Consumer IR.**

8.14.5 Consumer IR Special Configuration Register (Index=F0h, Default=00h)

Bit	Description
7-1	**Reserved** with default "00h."
0	1: IRQ sharing. 0: Normal.

Note 1:

Interrupt level mapping
Fh-Dh: not valid
Ch: IRQ12

3h: IRQ3
2h: not valid
1h: IRQ1
0h: no interrupt selected

Note 2:

DMA channel mapping
7h-5h: not valid
4h: no DMA channel selected
3h: DMA3
2h: DMA2
1h: DMA1
0h: DMA0

Note 3:

Except the standard mode, COM1 and COM2 cannot be selected in the same mode.

Note 4: The Location mapping table

Location	Description
001 000	GP10 (pin 84). Powered by VCCH.
001 001	GP11 (pin 34).
001 010	GP12 (pin 33).
001 011	GP13 (pin 32).
001 100	GP14 (pin 31).
001 101	GP15 (pin 30).
001 110	GP16 (pin 29).
001 111	GP17 (pin 28).
010 000	GP20 (pin 27).
010 001	GP21 (pin 26).
010 010	GP22 (pin 25).
010 011	GP23 (pin 24).
010 100	GP24 (pin 23).
010 101	GP25 (pin 22).
010 110	GP26 (pin 21).
010 111	GP27 (pin 20).
011 000	GP30 (pin 19).
011 001	GP31 (pin 18).
011 010	GP32 (pin 17).
011 011	GP33 (pin 16).
011 100	GP34 (pin 14).
011 101	GP35 (pin 13).
011 110	GP36 (pin 12).
011 111	GP37 (pin 11).
100 000	GP40 (pin 79). Powered by VCCH.
100 001	GP41 (pin 78). Powered by VCCH.
100 010	GP42 (pin 76). Powered by VCCH.
100 011	GP43 (pin 75). Powered by VCCH.
100 100	GP44 (pin 72). Powered by VCCH.
100 101	GP45 (pin 71). Powered by VCCH.
100 110	GP46 (pin 70). Powered by VCCH.
100 111	GP47 (pin 66).
101 000	GP50 (pin 48).
101 001	GP51 (pin 10).
101 010	GP52 (pin 9).
101 011	GP53 (pin 77). Powered by VCCH.
101 100	GP54 (pin 73). Powered by VCCH.
101 101	GP55 (pin 85). Powered by VCCH.
else	**Reserved**

9. Functional Description

9.1 LPC Interface

The IT8702F supports the peripheral site of the LPC I/F as described in the LPC Interface Specification Rev.1.0 (Sept. 29, 1997). In addition to the required signals (LAD3-0, LFRAME#, LRESET#, LCLK (LCLK is the same as PCICLK.)), the IT8702F also supports LDRQ#, SERIRQ and PME#.

9.1.1 LPC Transactions

The IT8702F supports some parts of the cycle types described in the LPC I/F specification. Memory read and Memory write cycles are used for the Flash I/F. I/O read and I/O write cycles are used for the programmed I/O cycles. DMA read and DMA write cycles are used for DMA cycles. All of these cycles are characteristic of the single byte transfer.

For LPC host I/O read or write transactions, the Super I/O module processes a positive decoding, and the LPC interface can respond to the result of the current transaction by sending out SYNC values on LAD[3:0] signals or leave LAD[3:0] tri-state depending on its result.

For DMA read or write transactions, the LPC interface will make reactions according to the DMA requests from the DMA devices in the Super I/O modules, and decides whether to ignore the current transaction or not.

The FDC and ECP are 8-bit DMA devices, so if the LPC Host initializes a DMA transaction with data size of 16/32 bits, the LPC interface will process the first 8-bit data and response with a SYNC ready (0000b) which will terminate the DMA burst. The LPC interface will then re-issue another LDRQ# message to assert DREQn after finishing the current DMA transaction.

9.1.2 LDRQ# Encoding

The Super I/O module provides two DMA devices: the FDC and the ECP. The LPC Interface provides LDRQ# encoding to reflect the DREQ[3:0] status. Two LDRQ# messages or different DMA channels may be issued back-to-back to trace DMA requests quickly. But, four PCI clocks will be inserted between two LDRQ# messages of the same DMA channel to guarantee that there is at least 10 PCI clocks for one DMA request to change its status. (The LPC host will decode these LDRQ# messages, and send those decoded DREQn to the legacy DMA controller which runs at 4 MHz or 33/8 MHz).

9.2 Serialized IRQ

The IT8702F follows the specification of Serialized IRQ Support for PCI System, Rev. 6.0, September 1, 1995, to support the serialized IRQ feature, and is able to interface most PC chipsets. The IT8702F encodes the parallel interrupts to an SERIRQ which will be decoded by the chipset with built-in Interrupt Controllers (two 8259 compatible modules).

9.2.1 Continuous Mode

When in the Continuous mode, the SIRQ host initiates the Start frame of each SERIRQ sequence after sending out the Stop frame by itself. (The next Start frame may or may not begin immediately after the turn-around state of current Stop frame.) The SERIRQ is always activated and SIRQ host keeps polling all the IRQn and system events, even though no IRQn status is changed. The SERIRQ enter the Continuous mode following a system reset.

9.2.2 Quiet Mode

In the Quiet mode, when one SIRQ Slave detects its input IRQn/events have been changed, it may initiate the first clock of Start frame. The SIRQ host can then follow to complete the SERIRQ sequence. In the Quiet mode, the SERIRQ has no activity following the Stop frame until it is initiated by SIRQ Slave, which implies low activity = low mode power consumption.

9.2.3 Waveform Samples of SERIRQ Sequence

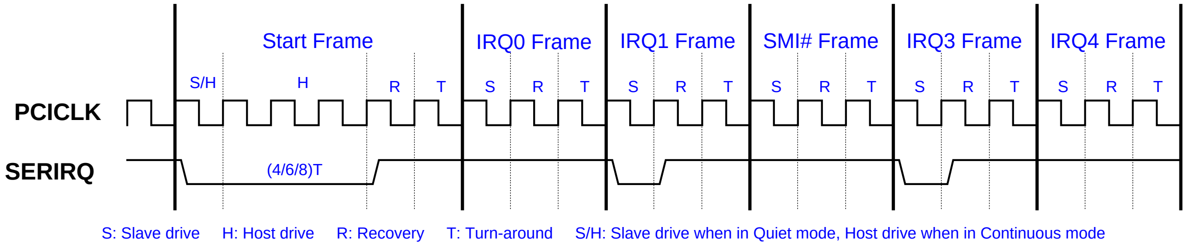

Start Frame
IRQ0 Frame
IRQ1 Frame
SMI# Frame
IRQ3 Frame
IRQ4 Frame
S/H
H
R
T
S
PCICLK
SERIRQ
(4/6/8)T
S: Slave drive
H: Host drive
R: Recovery
T: Turn-around
S/H: Slave drive when in Quiet mode, Host drive when in Continuous mode

Figure 9-1. Start Frame Timing

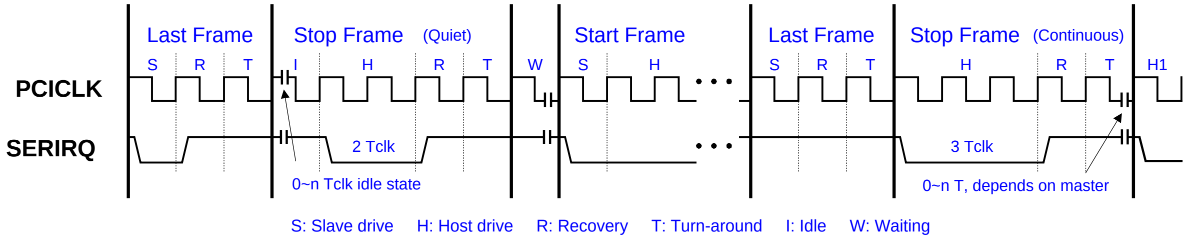

Last Frame
Stop Frame
(Quiet)
Start Frame
Last Frame
Stop Frame
(Continuous)
S
R
T
I
H
W
H1
PCICLK
SERIRQ
2 Tclk
3 Tclk
0~n Tclk idle state
0~n T, depends on master
S: Slave drive
H: Host drive
R: Recovery
T: Turn-around
I: Idle
W: Waiting

Figure 9-2. Stop Frame Timing

9.2.4 SERIRQ Sampling Slot

Slot Number	IRQn/ Events	#of Clocks Past Start	IT8702F
1	IRQ0	2	-
2	IRQ1	5	Y
3	SMI#	8	Y
4	IRQ3	11	Y
5	IRQ4	14	Y
6	IRQ5	17	Y
7	IRQ6	20	Y
8	IRQ7	23	Y
9	IRQ8	26	Y
10	IRQ9	29	Y
11	IRQ10	32	Y
12	IRQ11	35	Y
13	IRQ12	38	Y
14	IRQ13	41	-
15	IRQ14	44	Y
16	IRQ15	47	Y
17	IOCHCK#	50	-
18	INTA#	53	-
19	INTB#	56	-
20	INTC#	59	-
21	INTD#	62	-
32:22	Unassigned	95 / 65	-

9.3 General Purpose I/O

The IT8702F provides five sets of flexible I/O control and special functions for the system designers via a set of multi-functional General Purpose I/O pins (GPIO). The GPIO functions will not be performed unless the related enable bits of the GPIO Multi-function Pin Selection registers (Index 25h, 26h, 27h, 28h and 29h of the Global Configuration Registers) are set. The GPIO functions include the simple I/O function and alternate function, and the function selection is determined by the Simple I/O Enable Registers (LDN=07h, Index=C0h, C1h, C2h, C3h and C4h).

The Simple I/O function includes a set of registers, which correspond to the GPIO pins. All control bits are divided into five registers. The accessed I/O ports are programmable and are five consecutive I/O ports (Base Address+0, Base Address+1, Base Address+2, Base Address+3, Base Address+4). Base Address is programmed on the registers of GPIO Simple I/O Base Address LSB and MSB registers (LDN=07h, Index=60h and 61h).

The Alternate Function provides several special functions for users, including Watch Dog Timer, SMI# output routing, External Interrupt routing, Panel Button De-bounce, Keyboard Lock input routing, LED Blinking, Thermal output routing, and Beep output routing. The last two are the sub-functions of Hardware Monitor.

The Panel Button De-bounce is an input function. After the panel button de-bounce is enabled, a related status bit will be set when an active low pulse is detected on the GPIO pin. The status bits will be cleared by writing 1's to them. Panel Button De-bounce Interrupt will be issued if any one of the status bit is set. However, the new setting status will not issue another interrupt unless the previous status bit is cleared before being set.

The Key Lock function locks the keyboard to inhibit the keyboard interface. The programming method is to set bit 2 on the register Index F0h of KBC (keyboard) (LDN=5). The pin location mapping, Index F7h must also be programmed correctly.

The Blinking function provides a low frequency blink output. By connecting to some external components, it can be used to control a power LED. There are several frequencies that can be selected.

The Watch Dog Timer (WDT) function is constituted by a time counter, a time-out status register, and the timer reset control logic. The time-out status bit may be mapped to an interrupt or KRST# through the WDT Configuration register. The WDT has a programmable time-out range from 1 to 255 minutes or 1 to 255 seconds. The units are also programmable, either a minute or a second, via bit7 of the WDT Configuration register. When the WDT Time-out Value register is set to a non-zero value, the WDT loads the value and begin counting down from the value. When the value reaches to 0, the WDT status register will be set. There are many system events that can reload the non-zero value into the WDT, which include a CIR interrupt, a Keyboard Interrupt, a Mouse Interrupt, or I/O reads/writes to the Game Port base address. The effect on the WDT for each of the events may be enabled or disabled through bits in the WDT control register. No matter what value in the time counter is, the host may force a time-out to occur by writing a "1" to the bit 1 of the WDT Configuration register.

The External Interrupt routing function provides a useful feature for motherboard designers. Through this function, the parallel interrupts of other on-board devices can be easily re-routed into the Serial IRQ.

The SMI# is a non-maskable interrupt dedicated to the transparent power management. It consists of different enabled interrupts generated from each of the functional blocks in the IT8702F. The interrupts are redirected as the SMI# output via the SMI# Control Register 1 and SMI# Control Register 2. The SMI# Status Registers 1 and 2 are used to read the status of the SMI input events. All the SMI# Status Register bits can be cleared when the corresponding source events become invalidated. These bits can also be cleared by writing 1 to bit 7 of SMI# Control Register 2, whether the events of the corresponding sources are invalidated or not. The SMI# events can be programmed as pulse mode or level mode whenever an SMI# event occurs. The logic equation of the SMI# event is described below:

SMI# event = (EN_FIRQ and FIRQ) or (EN_S1IRQ and S1IRQ) or (EN_S2IRQ and S2IRQ) or (EN_PIRQ and PIRQ) or (EN_EC and EC_SMI) or (EN_PBDIRQ or PBDIRQ).

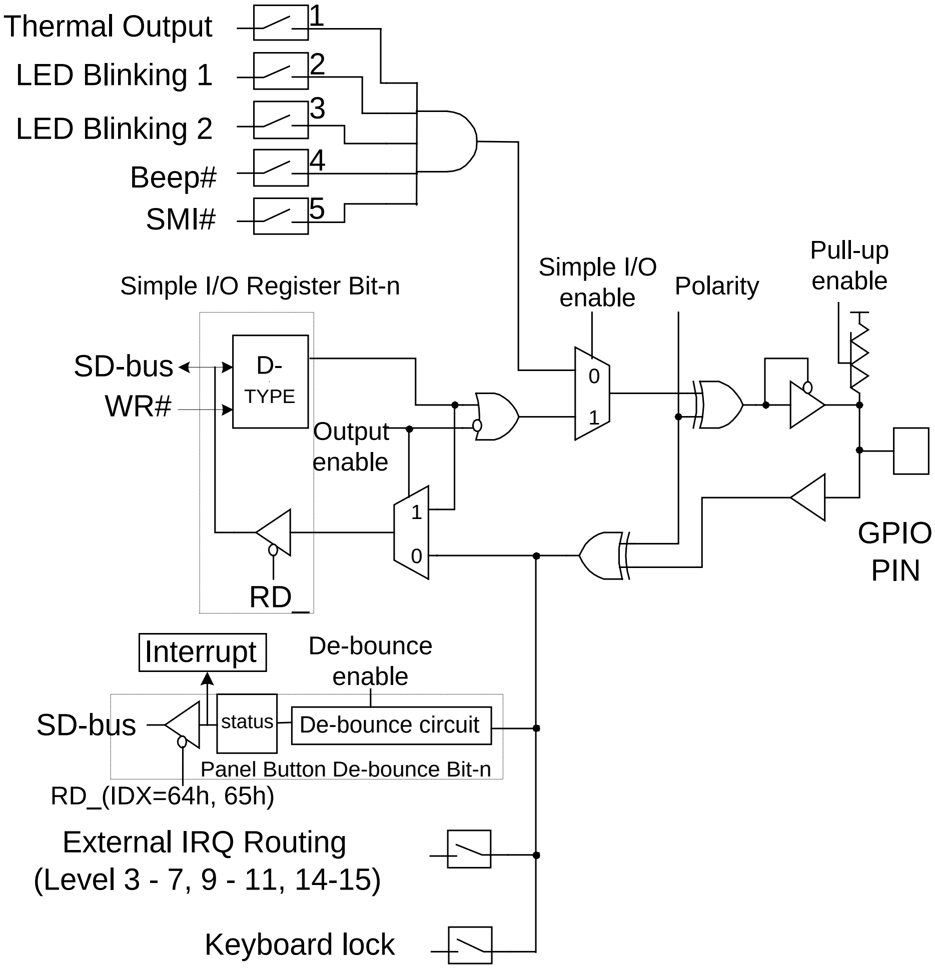

Thermal Output
LED Blinking 1
LED Blinking 2
Beep#
SMI#
1
2
3
4
5
Simple I/O Register Bit-n
Simple I/O enable
Polarity
Pull-up enable
SD-bus
WR#
D-
TYPE
Output enable
0
1
1
0
RD_
GPIO PIN
Interrupt
De-bounce enable
SD-bus
status
De-bounce circuit
Panel Button De-bounce Bit-n
RD_(IDX=64h, 65h)
External IRQ Routing
(Level 3 - 7, 9 - 11, 14-15)
Keyboard lock

Figure 9-3. General Logic of GPIO Function

9.4 Advanced Power Supply Control and Power Management Event (PME#)

The circuit for advanced power supply control (APC) provides five power-up events, Keyboard, Mouse, CIR, and Smart Card Reader card detect. When any of these five events is true, PWRON# will perform a low state until VCC is switched to ON state. The five events include the followings:

1. Detection of KCLK edge or special pattern of KCLK and KDAT. The special pattern of KCLK means pressing pre-set key string sequentially, and KDAT means pressing pre-set keys simultaneously
2. Detection of MCLK edge or special pattern of MCLK and MDAT. The special pattern of MCLK and MDAT means clicking on any mouse button twice sequentially.
3. Receiving CIR patterns are matched the previous stored pattern stored at the APC/PME Special Code Index and Data Register
4. Detection of the Smart Card Reader Card Detect pulse on the SCRPSNT# input pin

The PANSWH# and PSON# are especially designed for the system. PANSWH# serves as a main power switch input which is wire-AND to the APC output PWRON#. PSON# is the ATX Power control output, which is a power-failure gating circuit. The power-failure gating circuit is responsible for gating the PSIN input until PANSWH# becomes active when the VCCH is switched from OFF to ON.

The power-failure gating circuit can be disabled by setting the APC/PME Control Register 2 (LDN=04h, index F4h, bit 5). The gating circuit also provides an auto-restore function. When the bit 5 of PCR1 is set, the previous PSON# state will be restored when the VCCH is switched from OFF to ON.

The Mask PWRON# Activation bit (bit 4 of PCR 1) is used to mask all Power-up events except Switch on event when the VCCH state is just switched from FAIL to OFF. In other words, when this bit is set and the power state is switched from FAIL to OFF, the only validated function is PANSWH#.

The PCR2 register is responsible for determining the Keyboard power up events and APC conditions. Bit 4 is used to mask the PANSWH# power-on event on the PWRON# pin. To enable this bit, the keyboard power-up event should be enabled and set by (1) pressing pre-set key string sequentially or (2) stroking pre-set keys simultaneously. The APC/PME# special code index and data registers are used to specify the special key codes in the special power-up events of (1) pressing pre-set key string sequentially or (2) stroking pre-set keys simultaneously.

A CIR event is generated if the input CIR RX pattern is the same as the previous stored pattern stored at PME Special Code Index and Data Registers (LDN=04h, Index=F5h and F6h). The total maximum physical codes are nineteen bytes (from Index 20h to 32h). The first byte (Index 20h) is used to specify the pattern length (in bytes). Bits[7:4] are used when VCC is on; and Bits[3:0] when VCC goes OFF. The length represented in each 4 bits will be incremented by 3 internally as the actual length to be compared. For most of the CIR protocols, the first several bytes are always the same for each key (or pattern). The differences are always placed in the last several bytes. Thus, the system designer can program the IT8702F to generate a CIR PME# event as any keys when VCC is ON and a special key (i.e. POWER-ON) when VCC is OFF.

The Smart Card Reader Card Detect event is used to power on the system when any Integrated Circuit Card is inserted in the Smart Card Reader. When inserted, a pulse will be generated on the SCRPSNT# input pin. If the relative enabled bit is enabled, the power-up event will be also generated.

All APC registers (Index=F0h, F2h, F4h, F5h and F6h) are powered by back-up power (VBAT) when VCCH is OFF.

PME# is used to wake up the system from low-power states (S1-S5). Except the five events of the APC's, there will be another events to generate PME#: RI1# and RI2# events. RI1# and RI2# are Ring Indicator of Modem status at ACPI S1 or S2 state. A falling edge on these pins issues PME# events if the enable bits are set.

9.5 FAN Controller

The FAN Controller, built in the IT8702F, includes three FAN Tachometer inputs and three sets of advanced FAN Speed Controllers. FAN Tachometer inputs are digital inputs with an acceptable input range of 0V to 5V, and are responsible for measuring the FAN's Tachometer pulse periods. FAN_TAC1 and FAN_TAC2 include programmable divisors, and can be used to measure different fan speed ranges. FAN_TAC3 also includes programmable divisors, but can be used to measure two fan speed ranges only.

9.5.1 Interfaces

LPC Bus: The FAN Controller of the IT8702F decodes two addresses.

Table 9-1. Address Map on the LPC Bus

Registers or Ports	Address
Address register of the FAN Controller	Base+05h
Data register of the FAN Controller	Base+06h

Note 1: The Base Address is determined by the Logical Device configuration registers of the FAN Controller (LDN=04h, registers index=60h, 61h).

To access a FAN Controller register, the address of the register is written to the address port (Base+05h). Read or write data from or to that register via data port (Base+06h).

9.5.2 Registers

9.5.2.1 Address Port (Base+05h, Default=00h):

Bit	Description
7	**Outstanding; Read only** This bit is set when a data write is performed to Address Port via the LPC Bus.
6-0	Index: Internal Address of RAM and Registers.

Table 9-2. FAN Controller Registers

Index	R/W	Default	Registers or Action
00h	R/W	18h	Configuration
01h	R	00h	Interrupt Status 1
02h	R	00h	Reserved Register
03h	R	00h	Reserved Register
04h	R/W	00h	SMI# Mask 1
05h	R/W	00h	Reserved Register
06h	R/W	00h	Reserved Register
07h	R/W	00h	Interrupt Mask 1
08h	R/W	00h	Reserved Register
09h	R/W	00h	Reserved Register
0Ah	R	-	VID Register
0Bh	R/W	09h	Fan Tachometer Divisor Register
0Ch	R/W	00h	Fan Tachometer 16-bit Counter Enable Register
0Dh	R	-	Fan Tachometer 1 Reading Register
0Eh	R	-	Fan Tachometer 2 Reading Register
0Fh	R	-	Fan Tachometer 3 Reading Register
10h	R/W	-	Fan Tachometer 1 Limit Register
11h	R/W	-	Fan Tachometer 2 Limit Register
12h	R/W	-	Fan Tachometer 3 Limit Register
13h	R/W	00h	Fan Controller Main Control Register
14h	R/W	50h	FAN_CTL Control Register
15h	R/W	00h or 40h	FAN_CTL1 PWM Control Register
16h	R/W	00h or 40h	FAN_CTL2 PWM Control Register
17h	R/W	00h or 40h	FAN_CTL3 PWM Control Register
18h	R	-	Fan Tachometer 1 Extended Reading Register
19h	R	-	Fan Tachometer 2 Extended Reading Register
1Ah	R	-	Fan Tachometer 3 Extended Reading Register
1Bh	R/W	-	Fan Tachometer 1 Extended Limit Register
1Ch	R/W	-	Fan Tachometer 2 Extended Limit Register
1Dh	R/W	-	Fan Tachometer 3 Extended Limit Register
1E-57h	R	-	Reserved Register
58h	R	90h	ITE Vendor ID Register
59h	R/W	-	Reserved Register
5Bh	R	12h	Core ID Register
5Ch	R/W	00h	Beep Event Enable Register
5Dh	R/W	00h	Beep Frequency Divisor of Fan Event Register

Index	R/W	Default	Registers or Action
5E-5Fh	R/W	00h	Reserved Register
60-7Fh	R/W	-	Reserved Register
80h	R	-	Fan Tachometer 4 Reading LSB Register
81h	R	-	Fan Tachometer 4 Reading MSB Register
82h	R	-	Fan Tachometer 5 Reading LSB Register
83h	R	-	Fan Tachometer 5 Reading MSB Register
84h	R/W	-	Fan Tachometer 4 Limit LSB Register
85h	R/W	-	Fan Tachometer 4 Limit MSB Register
86h	R/W	-	Fan Tachometer 5 Limit LSB Register
87h	R/W	-	Fan Tachometer 5 Limit MSB Register
88h	R/W	00h	FAN_CTL4 PWM Control Register
89h	R/W	00h	FAN_CTL5 PWM Control Register
90-9Fh	R/W	-	Reserved Register

9.5.2.2 Register Description

9.5.2.2.1 Configuration Register (Index=00h, Default=18h)

Bit	R/W	Description
7	R/W	Initialization. A “1” restores all registers to their individual default values, except the Serial Bus Address register. This bit clears itself when the default value is “0.”
6	R/W	**Reserved**
5	R/W	**COPEN# cleared; Write “1” to clear COPEN#**
4	R	**Read Only**, Always “1.”
3	R/W	INT_Clear. A “1” disables the SMI# and IRQ outputs with the contents of interrupt status bits remain unchanged.
2	R/W	**IRQ enables the IRQ Interrupt output**
1	R/W	SMI# Enable. A “1” enables the SMI# Interrupt output.
0	R/W	Start. A “1” enables the startup of monitoring operations while a “0” sends the monitoring operation in the STANDBY mode.

9.5.2.2.2 Interrupt Status Register 1 (Index=01h, Default=00h)

Reading this register will clear itself following a read access.

Bit	R/W	Description
7-5	R	**Reserved**
4	R	A “1” indicates a Case Open event has occurred.
3	R	**Reserved**
2-0	R	A “1” indicates the FAN_TAC3-1 Count limit has been reached.

9.5.2.2.3 Reserved Register (Index=02h, Default=00h)

9.5.2.2.4 Reserved Register (Index=03h, Default=00h)

9.5.2.2.5 SMI# Mask Register 1 (Index=04h, Default=00h)

Bit	R/W	Description
7-6	R/W	**Reserved**
4	R/W	A “1” disables the Case Open Intrusion interrupt status bit for SMI#.
3	R/W	**Reserved**
2-0	R/W	A “1” disables the FAN_TAC3-1 interrupt status bit for SMI#.

9.5.2.2.6 Reserved Register (Index=05h, Default=00h)

9.5.2.2.7 Reserved Register (Index=06h, Default=00h)

9.5.2.2.8 Interrupt Mask Register 1 (Index=07h, Default=00h)

Bit	R/W	Description
7-5	R/W	**Reserved**
4	R/W	A “1” disables the Case Open Intrusion interrupt status bit for IRQ.
3	R/W	**Reserved**
2-0	R/W	A “1” disables the FAN_TAC3-1 interrupt status bit for IRQ.

9.5.2.2.9 Reserved Register (Index=08h, Default=00h)

9.5.2.2.10 Reserved Register (Index=09h, Default=00h)

9.5.2.2.11 VID Register (Index=0Ah)

Bit	R/W	Description
7-6	-	**Reserved**
5-0	R	**VID5-0 Inputs**

9.5.2.2.12 Fan Tachometer Divisor Register (Index=0Bh, Default=09h)

Bit	R/W	Description
7	-	**Reserved**
6	R/W	**FAN_TAC3 Counter Divisor** 0: divided by 2 1: divided by 8
5-3	R/W	**FAN_TAC2 Counter Divisor** 000: divided by 1 100: divided by 16 001: divided by 2 101: divided by 32 010: divided by 4 110: divided by 64 011: divided by 8 111: divided by 128
2-0	R/W	**FAN_TAC1 Counter Divisor** 000: divided by 1 100: divided by 16 001: divided by 2 101: divided by 32 010: divided by 4 110: divided by 64 011: divided by 8 111: divided by 128

9.5.2.2.13 Fan Tachometer 16-bit Counter Enable Register (Index=0Ch, Default=00h)

Bit	R/W	Description
7-6	-	**Reserved**
5	R/W	**FAN_TAC5 Enable** 0: disable 1: enable
4	R/W	**FAN_TAC4 Enable** 0: disable 1: enable
3	-	**Reserved**
2	R/W	**FAN_TAC3, 4, 5 16-bit Counter Divisor Enable** 0: disable 1: enable
1	R/W	**FAN_TAC2 16-bit Counter Divisor Enable** 0: disable 1: enable
0	R/W	**FAN_TAC1 16-bit Counter Enable** 0: disable 1: enable

9.5.2.2.14 Fan Tachometer 1-3 Reading Registers (Index=0Dh-0Fh)

Bit	R/W	Description
7-0	R	The number of counts of the internal clock per revolution.

9.5.2.2.15 Fan Tachometer 1-3 Limit Registers (Index=10h-12h)

Bit	R/W	Description
7-0	R/W	**Limit Value**

9.5.2.2.16 Fan Controller Main Control Register (Index=13h, Default=00h)

Bit	R/W	Description
7	R	**Reserved**
6-4	R/W	**FAN_TAC3-1 Enable** 0: disable 1: enable.
3	R/W	**Reserved.** Should write ”0”.
2-0	R/W	**FAN_CTL3-1 Output Mode Selection** 0: ON/OFF mode.

9.5.2.2.17 FAN_CTL Control Register (Index=14h, Default=50h)

Bit	R/W	Description
7	R/W	**FAN_CTL Polarity** 0: Active Low. 1: Active High.
6-4	R/W	**PWM base clock select.** 000: 48Mhz (PWM Frequency=375Khz). 001: 24Mhz(PWM Frequency=187.5Khz). 010: 12Mhz(PWM Frequency=93.75Khz)

Bit	R/W	Description
		011: 8Mhz(PWM Frequency=62.5Khz) 100: 6Mhz(PWM Frequency=46.875Khz) 101: 3Mhz(PWM Frequency=23.43Khz) 110: 1.5Mhz(PWM Frequency=11.7Khz) 111: 0.75Mhz(PWM Frequency=5.86Khz).
3	R/W	**PWM Minimum Duty Select** 0: 0 %. For a given PWM value, the actual duty is PWM/128 X 100%. 1: 20 %. For a given PWM value (not 00h), the actual duty is (PWM+32)/160 X 100%. If the given PWM value is 00h, the actual duty will be 0%.
2-0	R/W	**FAN_CTL3-1 ON/OFF Mode Control** These bits are only available when the relative output modes are selected in ON/OFF mode. 0: OFF. 1: ON.

9.5.2.2.18 FAN_CTL1 PWM Control Register (Index=15h, Default=00h or 40h)

This default value of this register is selected by JP5.

Bit	R/W	Description
7	R/W	**Reserved.** Should write ”0”.
6-0	R/W	128 steps of PWM control.

9.5.2.2.19 FAN_CTL2 PWM Control Register (Index=16h, Default=00h or 40h)

This default value of this register is selected by JP5.

Bit	R/W	Description
7	R/W	**Reserved.** Should write ”0”.
6-0	R/W	128 steps of PWM control.

9.5.2.2.20 FAN_CTL3 PWM Control Register (Index=17h, Default=00h or 40h)

This default value of this register is selected by JP5.

Bit	R/W	Description
7	R/W	**Reserved.** Should write ”0”.
6-0	R/W	128 steps of PWM control.

9.5.2.2.21 Fan Tachometer 1-3 Extended Reading Registers (Index=18h-1Ah)

Bit	R/W	Description
7-0	R	**The number of counts of the internal clock per revolution. [15:8]**

9.5.2.2.22 Fan Tachometer 1-3 Extended Limit Registers (Index=1Bh-1Dh)

Bit	R/W	Description
7-0	R	**Limit Value. [15:8]**

9.5.2.2.23 Vendor ID Register (Index=58h, Default=90h)

Bit	R/W	Description
7-0	R	**ITE Vendor ID. Read Only**

9.5.2.2.24 Code ID Register (Index=5Bh, Default=12h)

Bit	R/W	Description
7-0	R	**ITE Vendor ID. Read Only**

9.5.2.2.25 Beep Event Enable Register (Index=5Ch, Default=00h)

Bit	R/W	Description
7-1	R/W	**Reserved**
0	R/W	Enables Beep action when FAN_TACs exceed limit.

9.5.2.2.26 Beep Frequency Divisor of Fan Event Register (Index=5Dh, Default=00h)

Bit	R/W	Description
7-4	R/W	**Tone Divisor. Tone=500/(bits[7:4]+1).**
3-0	R/W	**Frequency Divisor. Frequency=10K/(bits[3:0]+1).**

9.5.2.2.27 Fan Tachometer 4-5 Reading LSB Registers (Index=80h,82h)

Bit	R/W	Description
7-0	R	The number of counts of the internal clock per revolution.

9.5.2.2.28 Fan Tachometer 4-5 Reading MSB Registers (Index=81h,83h)

Bit	R/W	Description
7-0	R	The number of counts of the internal clock per revolution.

9.5.2.2.29 Fan Tachometer 4-5 Limit LSB Registers (Index=84h,86h)

Bit	R/W	Description
7-0	R/W	**Limit Value**

9.5.2.2.30 Fan Tachometer 4-5 Limit MSB Registers (Index=85h,87h)

Bit	R/W	Description
7-0	R/W	**Limit Value**

9.5.2.2.31 FAN_CTL4 PWM Control Register (Index=88h, Default=00h)

Bit	R/W	Description

7	R	**Reserved.** Should write "0".
6-0	R/W	128 steps of PWM control.

9.5.2.2.32 FAN_CTL5 PWM Control Register (Index=89h, Default=00h)

Bit	R/W	Description
7	R	**Reserved.** Should write "0".
6-0	R/W	128 steps of PWM control.

9.5.3 Operation

9.5.3.1 Power On RESET and Software RESET

When the system power is first applied, the FAN Controller performs a "power on reset" on the registers which are returned to default values (due to system hardware reset). Except the function of the Serial Bus Interface Address register, a software reset (bit 7 of Configuration register) is able to accomplish all the functions as the hardware reset does.

9.5.3.2 Fan Tachometer

The Fan Tachometer inputs gate a 22.5 kHz clock into an 8-bit or a16-bit counter (maximum count=255 or 65535) for one period of the input signals. Several divisors, located in FAN Divisor Register, are provided for FAN_TAC1, FAN_TAC2, and FAN_TAC3, and are used to modify the monitoring range. Counts are based on 2 pulses per revolution tachometer output.

RPM = 1.35 X 10^6 / (Count X Divisor)

The maximum input signal range is from 0 to VCC. The additional application is needed to clamp the input voltage and current.

9.5.3.3 Interrupt of the FAN Controller

The FAN Controller generates interrupts as a result of each of its Limit registers on FAN monitor. All the interrupts are indicated in two Interrupt Status Registers. The IRQ and SMI# outputs have individual mask registers. These two Interrupts can also be enabled/disabled in the Configuration Register. The Interrupt Status Registers will be reset after being read. When the Interrupt Status Registers are cleared, the Interrupt lines will also be cleared. When a read operation is completed before the completion of the monitoring loop sequence, it indicates an Interrupt Status Register has been cleared. Due to slow monitoring sequence, the FAN Controller needs 1.5 seconds to allow all the FAN Controller Registers to be safely updated between completed read operations. When the bit 3 of the Configuration Register is set to high, the Interrupt lines are cleared and the monitoring loop will be stopped. The loop will resume when this bit is cleared.

9.6 Floppy Disk Controller (FDC)

9.6.1 Introduction

The Floppy Disk Controller provides the interface between a host processor and up to two floppy disk drives. It integrates a controller and a digital data separator with write precompensation, data rate selection logic, microprocessor interface, and a set of registers.

The FDC supports data transfer rates of 250 Kbps, 300 Kbps, 500 Kbps, and 1 Mbps. It operates in PC/AT mode and supports 3-mode type drives. Additionally, the FDC is software compatible with the 82077.

The FDC configuration is handled by software and a set of Configuration registers. Status, Data, and Control registers facilitate the interface between the host microprocessor and the disk drive, providing information about the condition and/or state of the FDC. These configuration registers can select the data rate, enable interrupts, drives, and DMA modes, and indicate errors in the data or operation of the FDC/FDD.

The controller manages data transfers using a set of data transfer and control commands. These commands are handled in three phases: Command, Execution, and Result. Not all commands utilize all these three phases.

9.6.2 Reset

The IT8702F device implements both software and hardware reset options for the FDC. Either type of the resets will reset the FDC, terminating all operations and placing the FDC into an idle state. A reset during a write to the disk will corrupt the data and the corresponding CRC.

9.6.3 Hardware Reset (LRESET# Pin)

When the FDC receives a LRESET# signal, all registers of the FDC core are cleared (except those programmed by the SPECIFY command). To exit the reset state, the host must clear the DOR bit.

9.6.4 Software Reset (DOR Reset and DSR Reset)

When the reset bit in the DOR or the DSR is set, all registers of the FDC core are cleared. A reset performed by setting the reset bit in the DOR has higher priority over a reset performed by setting the reset bit in the DSR. In addition, to exit the reset state, the DSR bit is self-clearing, while the host must clear the DOR bit.

9.6.5 Digital Data Separator

The internal digital data separator is comprised of a digital PLL and associated support circuitry. It is responsible for synchronizing the raw data signal read from the floppy disk drive. The synchronized signal is used to separate the encoded clock from the data pulses.

9.6.6 Write Precompensation

Write precompensation is a method that can be used to adjust the effects of bit shift on data as it is written to the disk. It is harder for the data separator to read data that has been subject to bit shifting. Soft read errors can occur due to such bit shifting. Write precompensation predicts where the bit shifting might occur within a data pattern and shifts the individual data bits back to their nominal positions.

The FDC permits the selection of write precompensation via the Data Rate Select Register (DSR) bits 2 through 4.

9.6.7 Data Rate Selection

Selecting one of the four possible data rates for the attached floppy disks is accomplished by setting the Diskette Control Register (DCR) or Data Rate Select Register (DSR) bits to 0 and 1. The data rate is determined by the last value that is written to either the DCR or the DSR. When the data rate is set, the data separator clock is scaled appropriately.

9.6.8 Status, Data and Control Registers

9.6.8.1 Digital Output Register (DOR, FDC Base Address + 02h)

This is a **read/write** register. It controls drive selection and motor enables as well as a software reset bit and DMA enable. The I/O interface reset may be used at any time to clear the DOR's contents.

Table 9-3. Digital Output Register (DOR)

Bit	Symbol	Description
7-6	-	**Reserved**
5	MOTB EN	**Drive B Motor Enable** 0: Disable Drive B motor. 1: Enable Drive B motor.
4	MOTA EN	**Drive A Motor Enable** 0: Disable Drive A motor. 1: Enable Drive A motor.
3	DMAEN	**Disk Interrupt and DMA Enable** 0: Disable disk interrupt and DMA (DRQx, DACKx#, TC and INTx). 1: Enable disk interrupt and DMA.
2	RESET#	**FDC Function Reset** 0: Reset FDC function. 1: Clear reset of FDC function. This reset does not affect the DSR, DCR or DOR.
1	-	**Reserved**
0	DVSEL	**Drive Selection** 0: Select Drive A. 1: Select Drive B.

9.6.8.2 Tape Drive Register (TDR, FDC Base Address + 03h)

This is a **read/write** register and is included for 82077 software compatibility. The contents of this register are not used internal to the device.

Table 9-4. Tape Drive Register (TDR)

Bit	Symbol	Description
7-2	-	**Undefined**
1-0	TP_SEL[1:0]	**Tape Drive Selection** TP_SEL[1:0] : Drive selected. 00: None 01: 1 10: 2 11: 3

9.6.8.3 Main Status Register (MSR, FDC Base Address + 04h)

This is a **read only** register. It indicates the general status of the FDC, and is able to receive data from the host. The MSR should be read before each byte is sent to or received from the Data register, except when in

DMA mode.

Table 9-5. Main Status Register (MSR)

Bit	Symbol	Description
7	RQM	**Request for Master** FDC Request for Master. 0: The FDC is busy and cannot receive data from the host. 1: The FDC is ready and the host can transfer data.
6	DIO	**Data I/O Direction** Indicates the direction of data transfer once a RQM has been set. 0: Write. 1: Read.
5	NDM	**Non-DMA Mode** This bit selects Non-DMA mode of operation. 0: DMA mode selected. 1: Non-DMA mode selected. This mode is selected via the SPECIFY command during the Execution phase of a command.
4	CB	**Diskette Control Busy** Indicates whether a command is in progress (the FDD is busy). 0: A command has been executed and the end of the Result phase has been reached. 1: A command is being executed.
3-2	-	**Reserved**
1	DBB	**Drive B Busy** Indicates whether Drive B is in the SEEK portion of a command. 0: Not busy. 1: Busy.
0	DAB	**Drive A Busy** Indicates whether Drive A is in the SEEK portion of a command. 0: Not busy. 1: Busy.

9.6.8.4 Data Rate Select Register (DSR, FDC Base Address + 04h)

This is a **write only** register. It is used to determine the data rate, amount of write precompensation, power down mode, and software reset. The data rate of the floppy disk controller is the most recent write of either the DSR or DCR. The DSR is unaffected by a software reset. The DSR can be set to 02h by a hardware reset. The “02h” represents the default precompensation, and 250 Kbps indicates the data transfer rate.

Table 9-6. Data Rate Select Register (DSR)

Bit	Symbol	Description
7	S/W RESET	**Software Reset** It is active high and shares the same function with the RESET# of the DOR except that this bit is self-clearing.
6	POWER DOWN	**Power Down** When this bit is written with a “1”, the floppy controller is put into manual low power mode. The clocks of the floppy controller and data separator circuits will be turned off until a software reset or the Data Register or Main Status Register is accessed.
5	-	**Undefined**

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>4-2</td><td>PRE-COMP 2-0</td><td>Precompensation Select
These three bits are used to determine the value of write precompensation that will be applied to the WDATA# pin. Track 0 is the default starting track number, which can be changed by the CONFIGURE command for precompensation.
<table>
<tr><th>PRE_COMP</th><th>Precompensation Delay</th></tr>
<tr><td>111</td><td>0.0 ns</td></tr>
<tr><td>001</td><td>41.7 ns</td></tr>
<tr><td>010</td><td>83.3 ns</td></tr>
<tr><td>011</td><td>125.0 ns</td></tr>
<tr><td>100</td><td>166.7 ns</td></tr>
<tr><td>101</td><td>208.3 ns</td></tr>
<tr><td>110</td><td>250.0 ns</td></tr>
<tr><td>000</td><td>Default</td></tr>
</table>
Default Precompensation Delays
<table>
<tr><th>Data Rate</th><th>Precompensation Delay</th></tr>
<tr><td>1 Mbps</td><td>41.7 ns</td></tr>
<tr><td>500 Kbps</td><td>125.0 ns</td></tr>
<tr><td>300 Kbps</td><td>125.0 ns</td></tr>
<tr><td>250 Kbps</td><td>125.0 ns</td></tr>
</table></td></tr>
<tr><td>1-0</td><td>DRATE1-0</td><td>Data Rate Select
<table>
<tr><th>Bits 1-0</th><th>Data Transfer Rate</th></tr>
<tr><td>00</td><td>500 Kbps</td></tr>
<tr><td>01</td><td>300 Kbps</td></tr>
<tr><td>10</td><td>250 Kbps (default)</td></tr>
<tr><td>11</td><td>1 Mbps</td></tr>
</table></td></tr>
</table>

9.6.8.5 Data Register (FIFO, FDC Base Address + 05h)

This is an 8-bit **read/write** register. It transfers command information, diskette drive status information, and the result phase status between the host and the FDC. The FIFO consists of several registers in a stack. Only one register in the stack is permitted to transfer information or status to the data bus at a time.

Table 9-7. Data Register (FIFO)

Bit	Symbol	Description
7-0		**Data** Command information, diskette drive status, or result phase status data

9.6.8.6 Digital Input Register (DIR, FDC Base Address + 07h)

This is a **read only** register and shares this address with the Diskette Control Register (DCR).

Table 9-8. Digital Input Register (DIR)

Bit	Symbol	Description
7	DSKCHG	**Diskette Change** Indicates the inverting value of the bit monitored from the input of the Floppy Disk

Bit	Symbol	Description
		Change pin (DSKCHG#).
6-0	-	**Undefined**

9.6.8.7 Diskette Control Register (DCR, FDC Base Address + 07h)

This is a **write only** register and shares this address with the Digital Input Register (DIR).
The DCR register controls the data transfer rate for the FDC.

Table 9-9. Diskette Control Register (DCR)

Bit	Symbol	Description
7-2	-	**Reserved.** Always 0
1-0	DRATE1-0	**Data Rate Select** **Bits 1-0** **Data Transfer Rate** 00 500 Kbps 01 300 Kbps 10 250 Kbps 11 1 Mbps

9.6.9 Controller Phases

The FDC handles data transfers and control commands in three phases: Command, Execution and Result. Not all commands utilize these three phases.

9.6.9.1 Command Phase

Upon reset, the FDC enters the Command phase and is ready to receive commands from the host. The host must verify that MSR bit 7 (RQM) = 1 and MSR bit 6 (DIO) = 0, indicating the FDC is ready to receive data. For each command, a defined set of command code and parameter bytes must be transferred to the FDC in a given order. See sections 11.6.11 and 11.6.12 for details on the various commands. RQM is set false (0) after each byte-Read cycle, and set true (1) when a new parameter byte is required. The Command phase is completed when this set of bytes has been received by the FDC. The FDC automatically enters the next controller phase and the FIFO is disabled.

9.6.9.2 Execution Phase

Upon the completion of the Command phase, the FDC enters the Execution phase. It is in this phase that all data transfers occur between the host and the FDC. The SPECIFY command indicates whether this data transfer occurs in DMA or non-DMA mode. Each data byte is transferred via an IRQx or DRQx# based upon the DMA mode. On reset, the CONFIGURE command can automatically enable or disable the FIFO. The Execution phase is completed when all data bytes have been received. If the command executed does not require a Result phase, the FDC is ready to receive the next command.

9.6.9.3 Result Phase

For commands that require data written to the FIFO, the FDC enters the Result phase when the IRQ or DRQ is activated. The MSR bit 7 (RQM) and MSR bit 6 (DIO) must equal 1 to read the data bytes. The Result phase is completed when the host has read each of the defined set of result bytes for the given command. Right after the completion of the phase, RQM is set to 1, DIO is set to 0, and the MSR bit 4 (CB) is cleared, indicating the FDC is ready to receive the next command.

9.6.9.4 Result Phase Status Registers

For commands that contain a Result phase, these **read only** registers indicate the status of the most recently executed command.

Table 9-10. Status Register 0 (ST0)

Bit	Symbol	Description
7-6	IC	**Interrupt Code** 00: Execution of the command has been completed correctly. 01: Execution of the command began, but failed to complete successfully. 10: INVALID command. 11: Execution of the command was not completed correctly, due to a polling error.
5	SE	**Seek End** The FDC executed a SEEK or RE-CALIBRATE command.
4	EC	**Equipment Check** The TRK0# pin was not set after a RE-CALIBRATE command was issued.
3	NU	**Not Used**
2	H	**Head Address** The current head address.
1	DSB	**Drive B Select**
0	DSA	**Drive A Select**

Table 9-11. Status Register 1 (ST1)

Bit	Symbol	Description
7	EN	**End of Cylinder** Indicates the FDC attempted to access a sector beyond the final sector of the track. This bit will be set if the Terminal Count (TC) signal is not issued after a READ DATA or WRITE DATA command.
6	NU	**Not Used**
5	DE	**Data Error** A CRC error occurred in either the ID field or the data field of a sector.
4	OR	**Overrun/ Underrun** An overrun on a READ operation or underrun on a WRITE operation occurs when the FDC is not serviced by the CPU or DMA within the required time interval.
3	NU	**Not Used**
2	ND	**No Data** No data are available to the FDC when either of the following conditions is met: The floppy disk cannot find the indicated sector while the READ DATA or READ DELETED DATA commands are executed While executing a READ ID command, an error occurs upon reading the ID field While executing a READ A TRACK command, the FDC cannot find the starting sector
1	NW	**Not Writeable** Set when a WRITE DATA, WRITE DELETED DATA, or FORMAT A TRACK command is being executed on a write-protected diskette.
0	MA	**Missing Address Mark** This flag bit is set when either of the following conditions is met: The FDC cannot find a Data Address Mark or a Deleted Data Address Mark on the specified track. The FDC cannot find any ID address on the specified track after two index pulses are detected from the INDEX# pin.

Table 9-12. Status Register 2 (ST2)

Bit	Symbol	Description
7	NU	**Not Used**
6	CM	**Control Mark** This flag bit is set when either of the following conditions is met: 1. The FDC finds a Deleted Data Address Mark during a READ DATA command 2. The FDC finds a Data Address Mark during a READ DELETED DATA command
5	DD	**Data Error in Data Field** This flag bit is set when a CRC error is found in the data field.
4	WC	**Wrong Cylinder** This flag bit is set when the track address in the ID field is different from the track address specified in the FDC.
3	SH	**Scan Equal Hit** This flag bit is set when the condition of "equal" is satisfied during a SCAN command.
2	SN	**Scan Not Satisfied** This flag bit is set when the FDC cannot find a sector on the cylinder during a SCAN command.
1	BC	**Bad Cylinder** This flag bit is set when the track address equals “FFh” and is different from the track address in the FDC.
0	MD	**Missing Data Address Mark** This flag bit is set when the FDC cannot find a Data Address Mark or Deleted Data Address Mark.

Table 9-13. Status Register 3 (ST3)

Bit	Symbol	Description
7	FT	**Fault** Indicates the current status of the Fault signal from the FDD.
6	WP	**Write Protect** Indicates the current status of the Write Protect signal from the FDD.
5	RDY	**Ready** Indicates the current status of the Ready signal from the FDD.
4	TK0	**Track 0** Indicates the current status of the Track 0 signal from the FDD.
3	TS	**Two Side** Indicates the current status of the Two Side signal from the FDD.
2	HD	**Head Address** Indicates the current status of the Head Select signal to the FDD.
1-0	US1, US0	**Unit Select** Indicates the current status of the Unit Select signals to the FDD.

9.6.10 Command Set

The FDC utilizes a defined set of commands to communicate with the host. Each command is comprised of a unique first byte, which contains the op-code, and a series of additional bytes, which contain the required set of parameters and results. The descriptions use a common set of parameter byte symbols, which are presented in Table 10-14. The FDC commands may be executed whenever the FDC is in the Command phase. The FDC checks to see that the first byte is a valid command and, if so, proceeds. An interrupt is issued if it is not a valid command.

Table 9-14. Command Set Symbol Descriptions

Symbol	Description
C	**Cylinder Number** The current/selected cylinder (track) number: 0 – 255.
D	**Data** The data pattern to be written into a sector.
DC3–DC0	**Drive Configuration Bit3-0** Designate which drives are perpendicular drives on the PERPENDICULAR MODE command.
DIR	**Direction Control** Read/Write Head Step Direction Control. 0 = Step Out; 1 = Step In.
DR0, DR1	**Disk Drive Select** The selected drive number: 0 or 1.
DTL	**Data Length** When N is defined as 00h, DTL designates the number of data bytes which users are going to read out or write into the Sector. When N is not 00h, DTL is undefined.
DFIFO	**Disable FIFO** A “1” will disable the FIFO (default). A “0” will enable the FIFO.
EC	**Enable Count** If EC=1, DTL of VERIFY command will be SC.
EIS	**Enable Implied Seek** If EIS=1, a SEEK operation will be performed before executing any READ or WRITE command that requires the C parameter.
EOT	**End of Track** The final sector number on a cylinder. During a READ or WRITE operation, the FDC stops data transfer after the sector number is equal to EOT.
GAP2	**Gap 2 Length** By PERPENDICULAR MODE command, this parameter changes Gap 2 length in the format.
GPL	**Gap Length** The length of Gap 3. During a FORMAT command, it determines the size of Gap 3.
H	**Head Address** The Head number 0 or 1, as specified in the sector ID field. (H = HD in all command words.)
HD	**Head** The selected Head number 0 or 1. Also controls the polarity of HDSEL#. (H = HD in all command words.)
HLT	**Head Load Time** The Head Load Time in the FDD (2 to 254 ms in 2 ms increments).
HUT	**Head Unload Time** The Head Unload Time after a READ or WRITE operation has been executed (16 to 240 ms in 16 ms increments).

Command Set Symbol Descriptions [cont'd]

Symbol	Description
LOCK	If LOCK=1, DFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command will not be affected by a software reset. If LOCK=0 (default), the above parameters will be set to their default values following a software reset.
MFM	**FM or MFM Mode** If MFM is low, FM Mode (single density) is selected. If MFM is high, MFM Mode (double density) is selected.
MT	**Multi-Track** If MT is high, a Multi-Track operation is to be performed. In this mode, the FDC will automatically start searching for sector 1 on side 1 after finishing a READ/WRITE operation on the last sector on side 0.
N	**Number** The number of data bytes written into a sector, where: 00: 128 bytes (PC standard) 01: 256 bytes 02: 512 bytes … 07: 16 Kbytes
NCN	**New Cylinder Number** A new cylinder number, which is to be reached as a result of the SEEK operation. Desired position of Head.
ND	**Non-DMA Mode** When ND is high, the FDC operates in the Non-DMA Mode.
OW	**Overwrite** If OW=1, DC3-0 of the PERPENDICULAR MODE command can be modified. Otherwise, those bits cannot be changed.
PCN	**Present Cylinder Number** The cylinder number at the completion of a SENSE INTERRUPT STATUS command. Position of Head at present time.
POLLD	**Polling Disable** If POLLD=1, the internal polling routine is disabled.
PRETRK	**Precompensation Starting Track Number** Programmable from track 0 –255.
R	**Record** The sector number, which will be read or written.
RCN	**Relative Cylinder Number** To determine the relative cylinder offset from present cylinder as used by the RELATIVE SEEK command.
SC	The number of sectors per cylinder.
SK	**Skip** If SK=1, the Read Data operation will skip sectors with a Deleted Data Address Mark. Otherwise, the Read Deleted Data operation only accesses sectors with a Deleted Data Address Mark.
SRT	**Step Rate Time** The Stepping Rate for the FDD (1 to 16 ms in 1 ms increments). Stepping Rate applies to all drives (F=1 ms, E=2 ms, etc.).

Command Set Symbol Descriptions [cont'd]

Symbol	Description
ST0 ST1 ST2 ST3	**Status 0** **Status 1** **Status 2** **Status 3** ST0–3 stand for one of four registers that store the status information after a command has been executed. This information is available during the Result phase after command execution. These registers should not be confused with the Main Status Register (selected by $A_0 = 0$). ST0–3 may be **read only** after a command has been executed and contain information associated with that particular command.
STP	If STP = 1 during a SCAN operation, the data in contiguous sectors are compared byte by byte with data sent from the processor (or DMA). If STP = 2, alternate sectors are read and compared.

Table 9-15. Command Set Summary

READ DATA

Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	SK	0	0	1	1	0	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and the main system
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

READ DELETED DATA

Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	SK	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and the main system
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

READ A TRACK

Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	MFM	0	0	0	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system cylinder's contents from index hole to EOT
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

WRITE DATA										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	MT	MFM	0	0	0	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and the main system
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

WRITE DELETED DATA										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	MT	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and the main system
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

FORMAT A TRACK

Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	MFM	0	0	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	N								Bytes/Sector
	W	SC								Sectors/Cylinder
	W	GPL								Gap 3
	W	D								Filler Byte
Execution	W	C								Input Sector Parameters per-sector FDC formats an entire cylinder
	W	H								
	W	R								
	W	N								
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	Undefined								
	R	Undefined								
	R	Undefined								
	R	Undefined								

SCAN EQUAL

Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	SK	1	0	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transferred from the system to controller is compared to data read from disk
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

SCAN LOW OR EQUAL										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	MT	MFM	SK	1	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transferred from the system to controller is compared to data read from disk
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

SCAN HIGH OR EQUAL										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	MT	MFM	SK	1	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transferred from the system to controller is compared to data read from disk
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

VERIFY										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	SK	1	0	1	1	0	Command Codes
	W	EC	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL/SC								
Execution										No data transfer takes place
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

READ ID										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	MFM	0	0	1	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
Execution										The first correct ID information on the Cylinder is stored in the Data Register
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information during execution phase
	R	H								
	R	R								
	R	N								

CONFIGURE										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	1	0	0	1	1	Configure Information
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	DFIFO	POLLD	FIFOTHR				
		PRETRK								
Execution										

RE-CALIBRATE										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	0	0	0	0	0	0	DR1	DR0	
Execution										Head retracted to Track 0

SEEK										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	NCN								
Execution										Head is positioned over proper cylinder on diskette

RELATIVE SEEK										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	1	DIR	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	RCN								
Execution										Head is stepped in or out a programmable number of tracks

DUMPREG										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	0	0	0	0	1	1	1	0	Command Codes
Execution										Registers placed in FIFO
Result	R	PCN-Drive 0								
	R	PCN-Drive 1								
	R	PCN-Drive 2								
	R	PCN-Drive 3								
	R	SRT				HUT				
	R	HLT							ND	
	R	SC/EOT								
	R	LOCK	0	DC3	DC2	DC1	DC0	GAP	WG	
	R	0	DIS	DFIFO	POLLD	FIFOTHR				
	R	PRETRK								

LOCK										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	LOCK	0	0	1	0	1	0	0	Command Codes
Result	R	0	0	0	LOCK	0	0	0	0	

VERSION										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	0	0	0	1	0	0	0	0	Command Codes
Result	R	1	0	0	1	0	0	0	0	Enhanced Controller

SENSE INTERRUPT STATUS										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	ST0								Status information at the end of each SEEK operation
	R	PCN								

SENSE DRIVE STATUS										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
Result	R	ST3								Status information about FDD

SPECIFY										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	SRT				HUT				
	W	HLT							ND	

PERPENDICULAR MODE										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	0	0	0	1	0	0	1	0	Command Codes
	W	OW	0	DC3	DC2	DC1	DC0	GAP	WG	

INVALID										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	Invalid codes								INVALID Command Codes (NO-OP: FDC goes into standby state)
Result	R	ST0								ST0 = 80h

9.6.11 Data Transfer Commands

All data transfer commands utilize the same parameter bytes (except for FORMAT A TRACK command) and return the same result data bytes. The only difference between them is the five bits (bit 0–bit 4) of the first byte.

9.6.11.1 Read Data

The READ DATA command contains nine command bytes that place the FDC into the Read Data mode. Each READ operation is initialized by a READ DATA command. The FDC locates the sector to be read by matching ID Address Marks and ID fields from the command with the information on the diskette. The FDC then transfers the data to the FIFO. When the data from the given sector have been read, the READ DATA command is completed and the sector address is automatically incremented by 1. The data from the next sector are read and transferred to the FIFO in the same manner. Such a continuous read function is called a "Multi-Sector Read Operation".

If a TC or an implied TC (FIFO overrun/underrun) is received, the FDC stops sending data, but continues to read data from the current sector and checks the CRC bytes until the end of the sector is reached and the READ operation is completed.

The sector size is determined by the N parameter value as calculated in the equation below:

Sector Size = $2^{(7+N\ \text{value})}$ bytes.

The DTL parameter determines the number of bytes to be transferred. Therefore, if N = 00h, setting the sector size to 128 and the DTL parameter value is less than this, the remaining bytes will be read and checked for CRC errors by the FDC. If this occurs in a WRITE operation, the remaining bytes will be filled with 0. If the sector size is not 128 (N > 00h), DTL should be set to FFh.

In addition to performing Multi-Sector Read operations, the FDC can also perform Multi-Track Read operations. When the MT parameter is set, the FDC can read both sides of a disk automatically.

The combination of N and MT parameter values determines the amount of data that can be transferred during either type of READ operation. Table 9-16 shows the maximum data transfer capacity and the final sector the FDC reads based on these parameters.

Table 9-16. Effects of MT and N Bits

MT	N	Maximum Data Transfer Capacity	Final Sector Read from Disk
0	1	256 X 26 = 6656	26 on side 0 or side 1
1	1	256 X 52 = 13312	26 on side 1
0	2	512 X 15 = 7680	15 on side 0 or side 1
1	2	512 X 30 = 15360	15 on side 1
0	3	1024 X 8 = 8192	8 on side 0 or side 1
1	3	1024 X16 =16384	16 on side 1

9.6.11.2 Read Deleted Data

The READ DELETED DATA command is the same as the READ DATA command, except that a Deleted Data Address Mark (as opposed to a Data Address Mark) is read at the beginning of the Data Field. This command is typically used to mark a bad sector on a diskette.

9.6.11.3 Read a Track

After receiving a pulse from the INDEX# pin, the READ A TRACK command reads the entire data field from each sector of the track as a continuous block. If any ID or Data Field CRC error is found, the FDC continues to read data from the track and indicates the error at the end. Because the Multi-Track [and Skip] operation[s] is[are] not allowed under this command, the MT and SK bits should be low (0) during the command execution.

This command terminates normally when the number of sectors specified by EOT has not been read. If, however, no ID Address Mark has been found by the second occurrence of the INDEX pulse, the FDC will set the IC code in the ST0 to 01, indicating an abnormal termination, and then finish the command.

9.6.11.4 Write Data

The WRITE DATA command contains nine command bytes that place the FDC into the Write Data mode. Each WRITE operation is initialized by a WRITE DATA command. The FDC locates the sector to be written by reading ID fields and matching the sector address from the command with the information on the diskette. Then the FDC reads the data from the host via the FIFO and writes the data into the sector’s data field. Finally, the FDC computes the CRC value, storing it in the CRC field and increments the sector number (stored in the R parameter) by 1. The next data field is written into the next sector in the same manner. Such a continuous write function is called a "Multi-Sector Write Operation".

If a TC or an implied TC (FIFO overrun/underrun) is received, the FDC stops writing data and fills the remaining data field with 0s. If a check of the CRC value indicates an error in the sector ID Field, the FDC will set the IC code in the ST0 to 01 and the DE bit in the ST1 to 1, indicating an abnormal termination, and then terminate the WRITE DATA command. The maximum data transfer capacity and the DTL, N, and MT parameters are the same as in the READ DATA command.

9.6.11.5 Write Deleted Data

The WRITE DELETED DATA command is the same as the WRITE DATA command, except that a Deleted Data Address Mark (instead of a Data Address Mark) is written at the beginning of the Data Field. This command is typically used to mark a bad sector on a diskette.

9.6.11.6 Format A Track

The FORMAT A TRACK command is used to format an entire track. Initialized by an INDEX pulse, it writes data to the Gaps, Address Marks, ID fields and Data fields according to the density mode selected (FM or MFM). The Gap and Data field values are controlled by the host-specified values programmed into N, SC, GPL, and D during the Command phase. The Data field is filled with the data byte specified by D. The four data bytes per sector (C, H, R, and N) needed to fill the ID field are supplied by the host. The C, R, H, and N values must be renewed for each new sector of a track. Only the R parameter value must be changed when a sector is formatted, allowing the disk to be formatted with non-sequential sector addresses. These steps are repeated until a new INDEX pulse is received, at which point the FORMAT A TRACK command is terminated.

9.6.11.7 SCAN

The SCAN command allows the data read from the disk to be compared with the data sent from the system. There are three SCAN commands:

SCAN EQUAL Disk Data = System Data

SCAN HIGH OR EQUAL Disk Data ≥ System Data

SCAN LOW OR EQUAL Disk Data ≤ System Data

The SCAN command execution continues until the scan condition has been met, or when the EOT has been reached, or if TC is asserted. Read errors on the disk have the same error condition as the READ DATA command. If the SK bit is set, sectors with Deleted Data Address Marks are ignored. If all sectors read are skipped, the command terminates with the D3 bit of the ST2 being set. The Result phase of the command is shown below:

Table 9-17. SCAN Command Result

Command	**Status Register**		**Condition**
	D2	**D3**	
SCAN EQUAL	0	1	Disk = System
	1	0	Disk ≠ System
SCAN HIGH OR EQUAL	0	1	Disk = System
	0	0	Disk > System
	1	0	Disk < System
SCAN LOW OR EQUAL	0	1	Disk = System
	0	0	Disk < System
	1	0	Disk > System

9.6.11.8 VERIFY

The VERIFY command is used to read logical sectors containing a Normal Data Address Mark from the selected drive without transferring the data to the host. This command acts like a READ DATA command except that no data are transferred to the host. This command is designed for post-format or post write verification. Data are read from the disk, as the controller checks for valid Address Marks in the Address and Data Fields. The CRC is computed and checked against the previously stored value. Because no data are transferred to the host, the TC (Terminal Count of DMA) cannot be used to terminate this command. An implicit TC will be issued to the FDC by setting the EC bit. This implicit TC will occur when the SC value has been decremented to 0. This command can also be terminated by clearing the EC bit and when the EOT value is equal to the final sector to be checked.

Table 9-18. VERIFY Command Result

MT	EC	SC/EOT	Termination Result
0	0	SC = DTL EOT ≤ # Sectors per side	No Error
0	0	SC = DTL EOT > # Sectors per side	Abnormal Termination
0	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors per side	No Error
0	1	SC > # Sectors Remaining OR EOT > # Sectors per side	Abnormal Termination
1	0	SC = DTL EOT > # Sectors per side	No Error
1	0	SC = DTL EOT > # Sectors per side	Abnormal Termination
1	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors per side	No Error
1	1	SC > # Sectors Remaining OR EOT > # Sectors per side	Abnormal Termination

9.6.12 Control Commands

The control commands do not transfer any data. Instead, these commands are used to monitor and manage the data transfer. Three of the Control commands generate an interrupt when finished — READ ID, RE-CALIBRATE and SEEK. It is strongly recommended that a SENSE INTERRUPT STATUS command be issued after these commands to capture their valuable interrupt information. The RE-CALIBRATE, SEEK, and SPECIFY commands do not return any result bytes.

9.6.12.1 READ ID

The READ ID command is used to find the actual recording head position. It stores the first readable ID field value into the FDC registers. If the FDC cannot find an ID Address Mark by the time a second INDEX pulse is received, an abnormal termination will be generated by setting the IC code in the ST0 to 01.

9.6.12.2 Configure

The CONFIGURE command determines some special operation modes of the controller. It needs not to be issued if the default values of the controller meet the system requirements.
EIS: Enable Implied Seeks. A SEEK operation is performed before a READ, WRITE, SCAN, or VERIFY command.

0 = Disabled (default).
1 = Enabled.

DFIFO: Disable FIFO.
0 = Enabled.
1 = Disabled (default).

POLLD: Disable polling of the drives.
0 = Enabled (default). When enabled, a single interrupt is generated after a reset.
1 = Disabled.

FIFOTHR: The FIFO threshold in the execution phase of data transfer commands. They are programmable from 00 to 0F hex (1 byte to 16 bytes). Defaults to 1 byte.

PRETRK: The Precompensation Start Track Number. They are programmable from track 0 to FF hex (track 0 to track 255). Defaults to track 0.

9.6.12.3 RE-CALIBRATE

The RE-CALIBRATE command retracts the FDC read/write head to the track 0 position, resetting the value of the PCN counter and checking the TRK0# status. If TRK0# is low, the DIR# pin remains low and step pulses are issued. If TRK0# is high, SE [and EC bits] of the ST0 are set high, and the command is terminated. When TRK0# remains low for 79 step pulses, the RE-CALIBRATE command is terminated by setting SE and EC bits of ST0 to high. Consequently, for disks that can accommodate more than 80 tracks, more than one RE-CALIBRATE command is required to retract the head to the physical track 0.

The FDC is in a non-busy state during the Execution phase of this command, making it possible to issue another RE-CALIBRATE command in parallel with the current command.

On power-up, software must issue a RE-CALIBRATE command to properly initialize the FDC and the drives attached.

9.6.12.4 SEEK

The SEEK command controls the FDC read/write head movement from one track to another. The FDC compares the current head position, stored in PCN, with NCN values after each step pulse to determine what direction to move the head, if required. The direction of movement is determined below:

PCN < NCN — Step In: Sets DIR# signal to 1 and issues step pulses
PCN > NCN — Step Out: Sets DIR# signal to 0 and issues step pulses
PCN = NCN — Terminate the command by setting the ST0 SE bit to 1

The impulse rate of step pulse is controlled by Stepping Rate Time (SRT) bit in the SPECIFY command. The FDC is in a non-busy state during the Execution phase of this command, making it possible to issue another SEEK command in parallel with the current command.

9.6.12.5 RELATIVE SEEK

The RELATIVE SEEK command steps the selected drive in or out in a given number of steps. The DIR bit is used to determine to step in or out. RCN (Relative Cylinder Number) is used to determine how many tracks to step the head in or out from the current track. After the step operation is completed, the controller generates an interrupt, but the command has no Result phase. No other command except the SENSE INTERRUPT STATUS command should be issued while a RELATIVE SEEK command is in progress.

9.6.12.6 DUMPREG

The DUMPREG command is designed for system run-time diagnostics, and application software development, and debug. This command has one byte of Command phase and 10 bytes of Result phase, which return the values of parameters set in other commands.

9.6.12.7 LOCK

The LOCK command allows the programmer to fully control the FIFO parameters after a hardware reset. If the LOCK bit is set to 1, the parameters DFIFO, FIFOTHR, and PRETRK in the CONFIGURE command are not affected by a software reset. If the bit is set to 0, those parameters are set to default values after a software reset.

9.6.12.8 VERSION

The VERSION command is used to determine the controller being used. In Result phase, a value of 90 hex is returned in order to be compatible with the 82077.

9.6.12.9 SENSE INTERRUPT STATUS

The SENSE INTERRUPT STATUS command resets the interrupt signal (IRQ) generated by the FDC, and identifies the cause of the interrupt via the IC code and SE bit of the ST0, as shown in Table 9-19.
It may be necessary to generate an interrupt when any of the following conditions occur:

- Before any Data Transfer or READ ID command
- After SEEK or RE-CALIBRATE commands (no result phase exists)
- When a data transfer is required during an Execution phase in the non-DMA mode

Table 9-19. Interrupt Identification

SE	IC Code	Cause of Interrupt
0	11	Polling.
1	00	Normal termination of SEEK or RE-CALIBRATE command.
1	01	Abnormal termination of SEEK or RE-CALIBRATE command.

9.6.12.10 SENSE DRIVE STATUS

The SENSE DRIVE STATUS command acquires drive status information. It has no Execution phase.

9.6.12.11 SPECIFY

The SPECIFY command sets the initial values for the HUT (Head Unload Time), HLT (Head Load Time), SRT (Step Rate Time), and ND (Non-DMA mode) parameters. The possible values for HUT, SRT, and HLT are shown in Table 10-20, Table 10-21 and Table 10-22 respectively. The FDC is operated in DMA or non-DMA mode based on the value specified by the ND parameters.

Table 9-20. HUT Values

Parameter	1 Mbps	500 Kbps	300 Kbps	250 Kbps
0	128	256	426	512
1	8	16	26.7	32
-	-	-	-	-
E	112	224	373	448
F	120	240	400	480

Table 9-21. SRT Values

Parameter	1 Mbps	500 Kbps	300 Kbps	250 Kbps
0	8	16	26.7	32
1	7.5	15	25	30
-	-	-	-	-
E	1	2	3.33	4
F	0.5	1	1.67	2

Table 9-22. HLT Values

Parameter	1 Mbps	500 Kbps	300 Kbps	250 Kbps
00	128	256	426	512
01	1	2	3.33	4
02	2	4	6.7	8
-	-	-	-	-
7E	126	252	420	504
7F	127	254	423	508

9.6.12.12 PERPENDICULAR MODE

The PERPENDICULAR MODE command is used to support the unique READ/WRITE/FORMAT commands of Perpendicular Recording disk drives (4 Mbytes unformatted capacity). This command configures each of the four logical drives as a perpendicular or conventional disk drive via the DC3-DC0 bits, or with the GAP and WG control bits. Perpendicular Recording drives operate in “Extra High Density” mode at 1 Mbps, and are downward compatible with 1.44 Mbyte and 720 kbyte drives at 500 Kbps (High Density) and 250 Kbps (Double Density) respectively. This command should be issued during the initialization of the floppy disk controller. Then, when a drive is accessed for a FORMAT A TRACK or WRITE DATA command, the controller adjusts the format or Write Data parameters based on the data rate. If WG and GAP are used (not set to 00), the operation of the FDC is based on the values of GAP and WG. If WG and GAP are set to 00, setting DCn to 1 will set drive n to the Perpendicular mode. DC3-DC0 are unaffected by a software reset, but WG and GAP are both cleared to 0 after a software reset.

Table 9-23. Effects of GAP and WG on FORMAT A TRACK and WRITE DATA Commands

GAP	WG	Mode	Length of GAP2 FORMAT FIELD	Portion of GAP2 Re-Written by WRITE DATA Command
0	0	Conventional	22 bytes	0 bytes
0	1	Perpendicular (500 Kbps)	22 bytes	19 bytes
1	0	Reserved (Conventional)	22 bytes	0 bytes
1	1	Perpendicular (1 Mbps)	41 bytes	38 bytes

Table 9-24. Effects of Drive Mode and Data Rate on FORMAT A TRACK and WRITE DATA Commands

Data Rate	Drive Mode	Length of GAP2 FORMAT FIELD	Portion of GAP2 Re-Written by WRITE DATA Command
250/300/500 Kbps	Conventional Perpendicular	22 bytes 22 bytes	0 bytes 19 bytes
1 Mbps	Conventional Perpendicular	22 bytes 41 bytes	0 bytes 38 bytes

9.6.12.13 INVALID

The INVALID command indicates when an undefined command has been sent to FDC. The FDC will set the bit 6 and the bit 7 in the Main Status Register to 1 and terminate the command without issuing an interrupt.

9.6.13 DMA Transfers

DMA transfers are enabled by the SPECIFY command and are initiated by the FDC by activating the LDRQ# cycle during a DATA TRANSFER command. The FIFO is enabled directly by asserting the LPC DMA cycles.

9.6.14 Low Power Mode

When writing a 1 to the bit 6 of the DSR, the controller is set to low power mode immediately. All the clock sources including Data Separator, Microcontroller, and Write precompensation unit, will be gated. The FDC can be resumed from the low-power state in two ways: one is a software reset via the DOR or DSR, and the other is a read or write to either the Data Register or Main Status Register. The second method is more preferred since all internal register values are retained.

9.7 Serial Port (UART) Description

The IT8702F incorporates two enhanced serial ports that perform serial to parallel conversion on received data, and parallel to serial conversion on transmitted data. Each of the serial channels individually contains a programmable baud rate generator which is capable of dividing the input clock by a number ranging from 1 to 65535. The data rate of each serial port can also be programmed from 115.2K baud down to 50 baud. The character options are programmable for 1 start bit; 1, 1.5 or 2 stop bits; even, odd, stick or no parity; and privileged interrupts.

Table 9-25. Serial Channel Registers

Register	DLAB*	Address	READ	WRITE
Data	0	Base + 0h	RBR (Receiver Buffer Register)	TBR (Transmitter Buffer Register)
Control	0	Base + 1h	IER (Interrupt Enable Register)	IER
	x	Base + 2h	IIR (Interrupt Identification Register)	FCR (FIFO Control Register)
	x	Base + 3h	LCR (Line Control Register)	LCR
	x	Base + 4h	MCR (Modem Control Register)	MCR
	1	Base + 0h	DLL (Divisor Latch LSB)	DLL
	1	Base + 1h	DLM (Divisor Latch MSB)	DLM
Status	x	Base + 5h	LSR (Line Status Register)	LSR
	x	Base + 6h	MSR (Modem Status Register)	MSR
	x	Base + 7h	SCR (Scratch Pad Register)	SCR

* DLAB is bit 7 of the Line Control Register.

9.7.1 Data Registers

The TBR and RBR individually hold from five to eight data bits. If the transmitted data are less than eight bits, it aligns to the LSB. Either received or transmitted data are buffered by a shift register, and are latched first by a holding register. The bit 0 of any word is first received and transmitted.

(1) Receiver Buffer Register (RBR) (Read only, Address offset=0, DLAB=0)

This register receives and holds the incoming data. It contains a non-accessible shift register which converts the incoming serial data stream into a parallel 8-bit word.

(2) Transmitter Buffer Register (TBR) (Write only, Address offset=0, DLAB=0)

This register holds and transmits the data via a non-accessible shift register, and converts the outgoing parallel data into a serial stream before the data transmission.

9.7.2 Control Registers: IER, IIR, FCR, DLL, DLM, LCR and MCR

(1) Interrupt Enable Register (IER) (Read/Write, Address offset=1, DLAB=0)

The IER is used to enable (or disable) four active high interrupts which activate the interrupt outputs with its lower four bits: IER(0), IER(1), IER(2), and IER(3).

Table 9-26. Interrupt Enable Register Description

Bit	Default	Description
7-4	-	**Reserved**
3	0	**Enable MODEM Status Interrupt** Sets this bit high to enable the Modem Status Interrupt when one of the Modem Status Registers changes its bit status.
2	0	**Enable Receiver Line Status Interrupt** Sets this bit high to enable the Receiver Line Status Interrupt which is caused when Overrun, Parity, Framing or Break occurs.
1	0	**Enable Transmitter Holding Register Empty Interrupt** Sets this bit high to enable the Transmitter Holding Register Empty Interrupt.
0	0	**Enable Received Data Available Interrupt** Sets this bit high to enable the Received Data Available Interrupt and Time-out interrupt in the FIFO mode.

(2) Interrupt Identification Register (IIR) (Read only, Address offset=2)

This register facilitates the host CPU to determine interrupt priority and its source. The priority of four existing interrupt levels is listed below:

1. Receiver Line Status (highest priority)
2. Received Data Ready
3. Transmitter Holding Register Empty
4. Modem Status (lowest priority)

When a privileged interrupt is pending and the type of interrupt is stored in the IIR which is accessed by the Host, the serial channel holds back all interrupts and indicates the pending interrupts with the highest priority to the Host. Any new interrupts will not be acknowledged until the Host access is completed. The contents of the IIR are described in the table on the next page.

Table 9-27. Interrupt Identification Register

FIFO Mode	Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 3	**Bit 2**	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	X	X	1	-	None	None	-
0	1	1	0	First	Receiver Line Status	OE, PE, FE, or BI	Read LSR
0	1	0	0	Second	Received Data Available	Received Data Available	Read RBR or FIFO drops below the trigger level
1	1	0	0	Second	Character Time-out Indication	No characters have been removed from or input to the RCVR FIFO during the last 4 character times and there is at least 1 character in it during this time	Read RBR
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Read IIR if THRE is the Interrupt Source Write THR
0	0	0	0	Fourth	Modem Status	CTS#, DSR#, RI#, DCD#	Read MSR

Note: X = Not Defined

IIR(7), IIR(6): Are set when FCR(0) = 1.
IIR(5), IIR(4): Always logic 0.
IIR(3): In non-FIFO mode, this bit is a logic 0. In the FIFO mode, this bit is set along with bit 2 when a time-out Interrupt is pending.
IIR(2), IIR(1): Used to identify the highest priority interrupt pending.
IR(0): Used to indicate a pending interrupt in either a hard-wired prioritized or polled environment with a logic 0 state. In such a case, IIR contents may be used as a pointer that points to the appropriate interrupt service routine.

(3) FIFO Control Register (FCR) (Write Only, Address offset=2)

This register is used to enable, clear the FIFO, and set the RCVR FIFO trigger level.

Table 9-28. FIFO Control Register Description

Bit	Default	Description
7-6	-	**Receiver Trigger Level Select** These bits set the trigger levels for the RCVR FIFO interrupt.
5-4	0	**Reserved**
3	0	This bit does not affect the Serial Channel operation. RXRDY and TXRDY functions are not available on this chip.
2	0	**Transmitter FIFO Reset** This self-clearing bit clears all contents of the XMIT FIFO and resets its related counter to 0 via a logic "1."
1	0	**Receiver FIFO Reset** Setting this self-clearing bit to a logic 1 clears all contents of the RCVR FIFO and resets its related counter to 0 (except the shift register).
0	0	**FIFO Enable** XMIT and RCVR FIFOs are enabled when this bit is set high. XMIT and RCVR FIFOs are disabled and cleared respectively when this bit is cleared to low. This bit must be a logic 1 if the other bits of the FCR are written to, or they will not be properly programmed. When this register is switched to non-FIFO mode, all its contents are cleared.

Table 9-29. Receiver FIFO Trigger Level Encoding

FCR (7)	FCR (6)	RCVR FIFO Trigger Level
0	0	1 byte
0	1	4 bytes
1	0	8 bytes
1	1	14 bytes

(4) Divisor Latches (DLL, DLM) (Read/Write, Address offset=0,1 DLAB=0)

Two 8-bit Divisor Latches (DLL and DLM) store the divisor values in a 16-bit binary format. They are loaded during the initialization to generate a desired baud rate.

(5) Baud Rate Generator (BRG)

Each serial channel contains a programmable BRG which can take any clock input (from DC to 8 MHz) to generate standard ANSI/CCITT bit rates for the channel clocking with an external clock oscillator. The DLL or DLM is a number of 16-bit format, providing the divisor range from 1 to 2^{16} to obtain the desired baud rate. The output frequency is 16X data rate.

Table 9-30. Baud Rates Using (24 MHz ÷ 13) Clock

Desired Baud Rate	Divisor Used
50	2304
75	1536
110	1047
134.5	857
150	768
300	384
600	192
1200	96
1800	64
2000	58
2400	48
3600	32
4800	24
7200	16
9600	12
19200	6
38400	3
57600	2
115200	1

(6) Scratch Pad Register (Read/Write, Address offset=7)

This 8-bit register does not control the UART operation in any way. It is intended as a scratch pad register to be used by programmers to temporarily hold general purpose data.

(7) Line Control Register (LCR) (Read/Write, Address offset=3)

LCR controls the format of the data character and supplies the information of the serial line. Its contents are described on the next page.

Table 9-31. Line Control Register Description

Bit	Default	Description
7	0	**Divisor Latch Access Bit (DLAB)** Must be set to high to access the Divisor Latches of the baud rate generator during READ or WRITE operations. It must be set low to access the Data Registers (RBR and TBR) or the Interrupt Enable Register.
6	0	**Set Break** Forces the Serial Output (SOUT) to the spacing state (logic 0) by a logic 1, and this state will be preserved until a low level resetting LCR(6), enabling the serial port to alert the terminal in a communication system.
5	0	**Stick Parity** When this bit and LCR(3) are high at the same time, the parity bit is transmitted, and then detected by receiver, in opposite state by LCR(4) to force the parity bit into a known state and to check the parity bit in a known state.
4	0	**Even Parity Select** When parity is enabled (LCR(3) = 1), LCR(4) = 0 selects odd parity, and LCR(4) = 1 selects even parity.
3	0	**Parity Enable** A parity bit, located between the last data word bit and stop bit, will be generated or checked (transmit or receive data) when LCR(3) is high.
2	0	**Number of Stop Bits** This bit specifies the number of stop bits in each serial character, as summarized in table 10-32.
1-0	00	**Word Length Select [1:0]** 11: 8 bits 10: 7 bits 01: 6 bits 00: 5 bits

Table 9-32. Stop Bits Number Encoding

LCR (2)	Word Length	No. of Stop Bits
0	-	1
1	5 bits	1.5
1	6 bits	2
1	7 bits	2
1	8 bits	2

Note: The receiver will ignore all stop bits beyond the first, regardless of the number used in transmission.

(8) MODEM Control Register (MCR) (Read/Write, Address offset=4)

Controls the interface by the modem or data set (or device emulating a modem).

Table 9-33. Modem Control Register Description

Bit	Default	Description
7-5	-	**Reserved**
4	0	**Internal Loopback** Provides a loopback feature for diagnostic test of the serial channel when it is set high. Serial Output (SOUT) is set to the Marking State Shift Register output loops back into the Receiver Shift Register. All Modem Control inputs (CTS#, DSR#, RI# and DCD#) are disconnected. The four Modem Control outputs (DTR#, RTS#, OUT1 and OUT2) are internally connected to the four Modem Control inputs, and are forced to inactive high and the transmitted data are immediately received, allowing the processor to verify the transmit and receive data path of the serial channel.
3	0	**OUT2** The Output 2 bit enables the serial port interrupt output by a logic 1.
2	0	**OUT1** This bit does not have an output pin and can only be read or written by the CPU.
1	0	**Request to Send (RTS)** Controls the Request to Send (RTS#) which is in an inverse logic state with that of MCR(1).
0	0	**Data Terminal Ready (DTR)** Controls the Data Terminal ready (DTR#) which is in an inverse logic state with that of the MCR(0).

9.7.3 Status Registers: LSR and MSR

(1) Line Status Register (LSR) (Read/Write, Address offset=5)

This register provides status indications and is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of each serial channel. The contents of the LSR are described below:

Table 9-34. Line Status Register Description

Bit	Default	Description
7	0	**Error in Receiver FIFO** In 16450 mode, this bit is always 0. In the FIFO mode, it sets high when there is at least one parity error, framing or break interrupt in the FIFO. This bit is cleared when the CPU reads the LSR, if there are no subsequent errors in the FIFO.
6	1	**Transmitter Empty** This **read only** bit indicates that the Transmitter Holding Register and Transmitter Shift Register are both empty. Otherwise, this bit is "0," and has the same function in the FIFO mode.
5	1	**Transmitter Holding Register Empty** Transmitter Holding Register Empty (THRE). This **read only** bit indicates that the TBR is empty and is ready to accept a new character for transmission. It is set high when a character is transferred from the THR into the Transmitter Shift Register, causing a priority 3 IIR interrupt which is cleared by a read of IIR. In the FIFO mode, it is set when the XMIT FIFO is empty, and is cleared when at least one byte is written to the XMIT FIFO.

Line Status Register Description [cont'd]

Bit	Default	Description
4	0	**Line Break** Break Interrupt (BI) status bit indicates that the last character received was a break character, (invalid but entire character), including parity and stop bits. This occurs when the received data input is held in the spacing (logic 0) for longer than a full word transmission time (start bit + data bits + parity + stop bit). When any of these error conditions is detected (LSR(1) to LSR(4)), a Receiver Line Status interrupt (priority 1) will be generated in the IIR, with the IER(2) previously enabled.
3	0	**Framing Error** Framing Error (FE) bit, a logic 1, indicates that the stop bit in the received character is not valid. It resets low when the CPU reads the contents of the LSR.
2	0	**Parity Error** Parity error (PE) indicates by a logic 1 that the received data character does not have the correct even or odd parity, as selected by LCR(4). It will be reset to "0" whenever the LSR is read by the CPU.
1	0	**Overrun Error** Overrun Error (OE) bit indicates by a logic 1 that the RBR has been overwritten by the next character before it had been read by the CPU. In the FIFO mode, the OE occurs when the FIFO is full and the next character has been completely received by the Shift Register. It will be reset when the LSR is read by the CPU.
0	0	**Data Ready** A "1" indicates a character has been received by the RBR. A logic "0" indicates all the data in the RBR or the RCVR FIFO have been read.

(2) MODEM Status Register (MSR) (Read/Write, Address offset=6)

This 8-bit register indicates the current state of the control lines with modems or the peripheral devices in addition to this current state information. Four of these eight bits MSR(4) - MSR(7) can provide the state change information when a modem control input changes state. It is reset low when the Host reads the MSR.

Table 9-35. Modem Status Register Description

Bit	Default	Description
7	0	**Data Carrier Detect** Data Carrier Detect - Indicates the complement status of Data Carrier Detect (DCD#) input. If MCR(4) = 1, MSR(7) is equivalent to OUT2 of the MCR.
6	0	**Ring Indicator** Ring Indicator (RI#) - Indicates the complement status to the RI# input. If MCR(4)=1, MSR(6) is equivalent to OUT1 in the MCR.
5	0	**Data Set Ready** Data Set Ready (DSR#) - Indicates that the modem is ready to provide received data to the serial channel receiver circuitry. If the serial channel is in the Loop mode (MCR(4) = 1), MSR(5) is equivalent to DTR# in the MCR.
4	0	**Clear to Send** Clear to Send (CTS#) - Indicates the complement of CTS# input. When the serial channel is in the Loop mode (MCR(4)=1), MSR(5) is equivalent to RTS# in the MCR.
3	0	**Delta Data Carrier Detect** Indicates that the DCD# input state has been changed since the last time read by the Host.
2	0	**Trailing Edge Ring Indicator** Indicates that the RI input state to the serial channel has been changed from a low to high since the last time read by the Host. The change to a logic "1" does not activate

Bit	Default	Description
		the TERI.
1	0	**Delta Data Set Ready** Delta Data Set Ready (DDSR) - A logic "1" indicates that the DSR# input state to the serial channel has been changed since the last time read by the Host.
0	0	**Delta Clear to Send** This bit indicates the CTS# input to the chip has changed state since the last time the MSR was read.

9.7.4 Reset

The reset of the IT8702F should be held to an idle mode reset high for 500 ns until initialization, which causes the initialization of the transmitter and receiver internal clock counters.

Table 9-36. Reset Control of Registers and Pinout Signals

Register/Signal	Reset Control	Reset Status
Interrupt Enable Register	Reset	All bits Low
Interrupt Identification Register	Reset	Bit 0 is high and bits 1-7 are low
FIFO Control Register	Reset	All bits Low
Line Control Register	Reset	All bits Low
Modem Control Register	Reset	All bits Low
Line Status Register	Reset	Bits 5 and 6 are high, others are low
Modem Status Register	Reset	Bits 0-3 low, bits 4-7 input signals
SOUT1, SOUT2	Reset	High
RTS1#, RTS2#, DTR1#, DTR2#	Reset	High
IRQ of Serial Port	Reset	High Impedance

9.7.5 Programming

Each serial channel of the IT8702F is programmed by control registers, whose contents define the character length, number of stop bits, parity, baud rate and modem interface. Even though the control register can be written in any given order, the IER should be the last register written because it controls the interrupt enables. After the port is programmed, these registers can still be updated whenever the port is not transferring data.

9.7.6 Software Reset

This approach allows the serial port returning to a completely known state without a system reset. This is achieved by writing the required data to the LCR, DLL, DLM and MCR. The LSR and RBR must be read before interrupts are enabled to clear out any residual data or status bits that may be invalid for subsequent operations.

9.7.7 Clock Input Operation

The input frequency of the Serial Channel is 24 MHz ÷ 13, not exactly 1.8432 MHz.

9.7.8 FIFO Interrupt Mode Operation

(1) RCVR Interrupt

When setting FCR(0)=1 and IER(0)=1, the RCVR FIFO and receiver interrupts are enabled. The RCVR interrupt occurs under the following conditions:

The receive data available interrupt will be issued only if the FIFO has reached its programmed trigger level. They will be cleared as soon as the FIFO drops below its trigger level.

The receiver line status interrupt has higher priority over the received data available interrupt.

The time-out timer will be reset after receiving a new character or after the Host reads the RCVR FIFO whenever a time-out interrupt occurs. The timer will be reset when the Host reads one character from the RCVR FIFO.

RCVR FIFO time-out Interrupt: By enabling the RCVR FIFO and receiver interrupts, the RCVR FIFO time-out interrupt will occur under the following conditions:

The RCVR FIFO time-out interrupt will occur only if there is at least one character in the FIFO whenever the interval between the most recent received serial character and the most recent Host READ from the FIFO is longer than four consecutive character times.

The time-out timer will be reset after receiving a new character or after the Host reads the RCVR FIFO whenever a time-out interrupt occurs. The timer will be reset when the Host reads one character from the RCVR FIFO.

(2) XMIT Interrupt

By setting FCR(0) and IER(1) to high, the XMIT FIFO and transmitter interrupts are enabled, and the XMIT interrupt occurs under the conditions described below:

a. The transmitter interrupt occurs when the XMIT FIFO is empty, and it will be reset if the THR is written or the IIR is read.

b. The transmitter FIFO empty indications will be delayed one character time minus the last stop bit time whenever the following condition occurs: THRE = 1 and there have not been at least two bytes in the transmitter FIFO at the same time since the last THRE = 1. The transmitter interrupt after changing FCR(0) will be immediate, if it is enabled. Once the first transmitter interrupt is enabled, the THRE indication is delayed one character time minus the last stop bit time.

The character time-out and RCVR FIFO trigger level interrupts are in the same priority order as the received data available interrupt. The XMIT FIFO empty is in the same priority as the transmitter holding register empty interrupt.

FIFO Polled Mode Operation [FCR(0)=1, and IER(0), IER(1), IER(2), IER(3) or all are 0].

Either or both XMIT and RCVR can be in this operation mode. The operation mode can be programmed by users and is responsible for checking the RCVR and XMIT status via the LSR described below:

LSR(7): RCVR FIFO error indication.
LSR(6): XMIT FIFO and Shift register empty.
LSR(5): The XMIT FIFO empty indication.
LSR(4) - LSR(1): Specify that errors have occurred. Character error status is handled in the same way as in the interrupt mode. The IIR is not affected since IER(2)=0.
LSR(0): High whenever the RCVR FIFO contains at least one byte.

No trigger level is reached or time-out condition indicated in the FIFO Polled Mode.

9.8 Smart Card Reader

9.8.1 Features

As an IFD (InterFace Device) built in IT8702F, the Smart Card Reader (SCR) includes a standard UART (Either Serial Port 1 or Serial Port 2 is set in SCR mode) to control Smart Card interface handshaking and then performs data transfers, and can be connected to smart card socket directly. The Smart Card is capable of providing secured storage facilities for sensitive personal information (such as Private keys, Account numbers, Passwords, Medical information, …etc.). Then the SCR can be used for a broad range of applications in GSM, ID, pay TV, banking (refer to EMV'96 Spec.), … and so forth. It also provides a Smart Card clock divider for those ICC (Integrated Circuit Card) without internal clocks.

9.8.2 Operation

The SCR is a low-power consumption design. Whenever the IFD is inactive, the clock divider will turn off internal clocks even when the clock of IFD controlling / monitoring state machine is turned off to save power consumption. Also it could be waked up immediately when IC card is removed in case of emergency or when the FET control function is turned on/off.

The VCC power of IC card interface is powered from an external FET to protect the smart card interface. Also, the charge/discharge time for FET to reach 5V/0V is programmable, and FET performs automatically to meet ISO 7816 activation and deactivation sequences. The UART's modem control lines: DTR#, RTS# and DCD# are used for controlling FET on/off, Smart Card Reset signal and IC card insertion detection respectively. When an IC card is being inserted, it will switch the SCRPSNT# (Smart Card Present Detect#) and then cause the DCD# signal to trigger an interrupt to the system. Then in the Smart Card interrupt service routine, the driver can assert the DTR# signal to power on the external FET (SCRPFET#) and the RTS# signal to control the Smart Card Reset signal (SCRRST). In the mean time, IT8702F will generate a proper clock frequency to allow the IC card using default serial transfer baud rate to send back an ATR (Answer-To-Reset) sequence. The interface signals are enabled after VCC reaches enough voltage level. Then transfer protocol may be negotiated to promote more efficient transfers. In the same way, when the IC card is removed in case of emergency or when the ICC processing is finished, the driver can de-assert the DTR# to turn off the FET power. But before the FET power-off and the reset, clock and data signals will be de-active, followed by a sufficient FET discharge time guaranteed to protect IC card and IFD.

9.8.3 Connection of IFD to ICC Socket

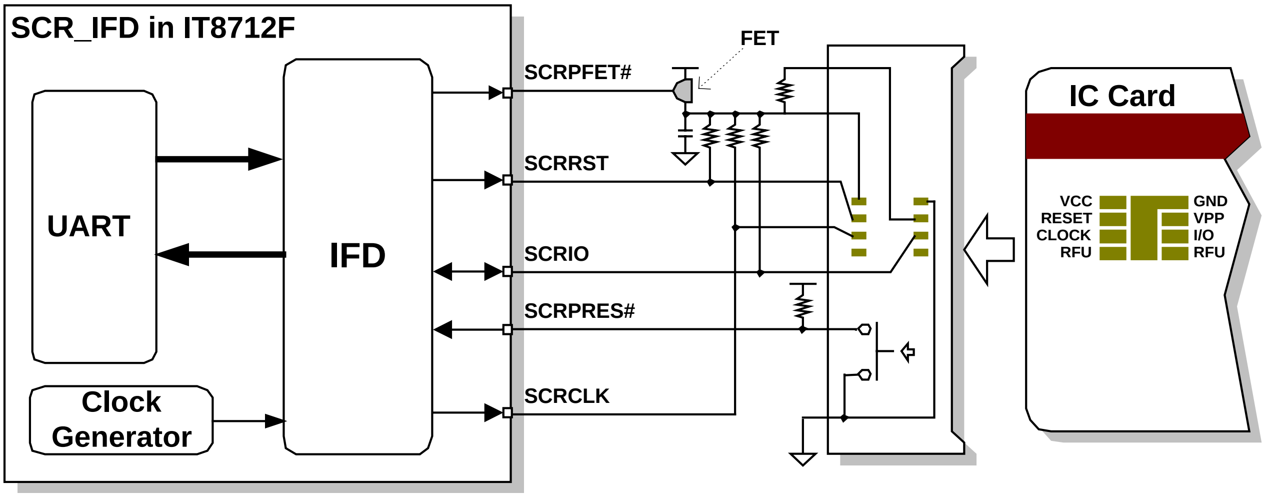


Figure 9-4. Smart Card Reader Application

9.8.4 Baud Rate Relationship Between UART and Smart Card Interface

To perform serial transfers correctly, the baud rate of UART must be set in ways similar to the ICC card.

- **Formula (Variation < 2%)**

$$\textbf{Baud Rate} = \overset{\textbf{UART}}{\frac{\frac{24\text{ MHz}}{13}}{16 * N}} \approx \overset{\textbf{Smart Card}}{\frac{\text{SCRCLK} * D}{F}}$$

N =Divisor of UART, assigned by programming the DLM (Divisor Latch MSB) and DLL (Divisor Latch LSB).
F =Clock Rate Conversion Factor, default = 372.
D =Bit Rate Adjustment Factor, Default is 1.
SCRCLK duty cycle is 45%-55%.

- **ICC With Internal Clock**

ICC may use built-in internal clock, then the Baud rate is 9600 baud, just programming the Divisor Latch Registers of UART in the IT8702F for SCR IFD.

- **ICC Without Internal Clock**

Baud rate is SCRCLK/372 before negotiating, and SCRCLK is limited within 1 MHz - 5MHz. During the ATR sequence, the default F value (Clock Rate Conversion Factor) is 372, and the default D value (Bit Rate Adjustment Factor) is 1.

9.8.5 Waveform Relationship

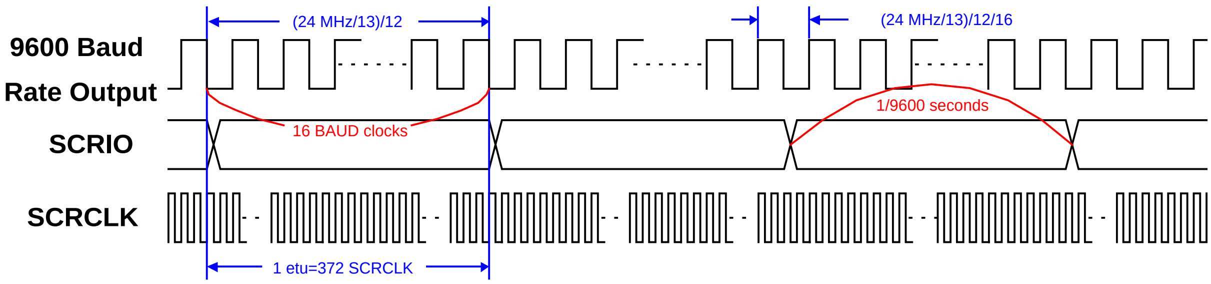


Figure 9-5. 9600 Baud Rate Example

9.8.6 Clock Divider

The SCRCLK is generated as the selection of SCR_CLKSEL1-0, which are determined in the S1 Special Configuration register 3 (LDN1_F2h) or S2 Special Configuration register 3 (LDN2_F2h).

Table 9-37. SCRCLK Selections

SCR_CLKSEL1-0	Selections
00	Stop
01	3.5 MHz
10	7.1 MHz
11	96 MHz / SCR DIV96M $^{\text{Note}}$

Note: SCR DIV96M is determined by S1 Special Configuration Register 4 (LDN1_F3h) or S2 Special Configuration Register 4 (LDN2_F3h).

9.8.7 Waveform Example of Activation/Deactivation Sequence

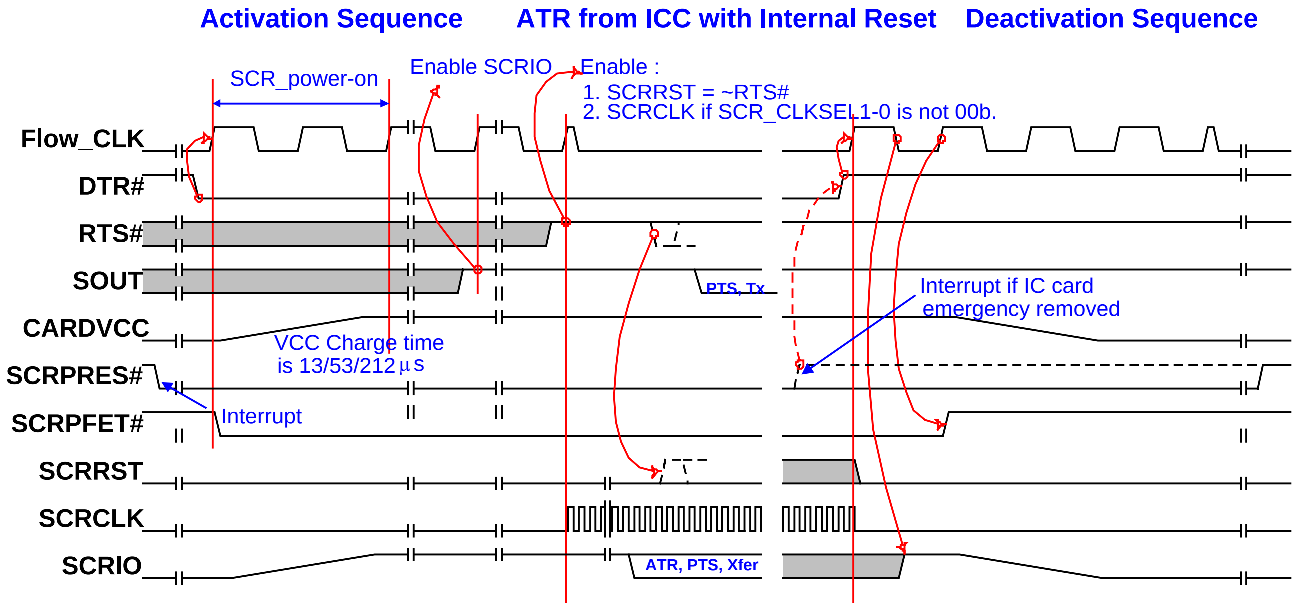

Activation Sequence
ATR from ICC with Internal Reset
Deactivation Sequence
SCR_power-on
Enable SCRIO
Enable :
1. SCRRST = ~RTS#
2. SCRCLK if SCR_CLKSEL1-0 is not 00b.
Flow_CLK
DTR#
RTS#
SOUT
CARDVCC
SCRPRES#
SCRPFET#
SCRRST
SCRCLK
SCRIO
PTS, Tx
Interrupt if IC card
emergency removed
VCC Charge time
is 13/53/212μs
Interrupt
ATR, PTS, Xfer

Figure 9-6. Waveform Example of IFD

- **Activation Sequence**

Refer to the waveform above. The SCR IFD in the IT8702F will make sure the IFD is in data receive mode (i.e. the SOUT from UART is high), and the RTS# should be programmed to high. The SCRCLK is then enabled to output to the IC card (which means that the IC card can count SCRCLK clock numbers to start ATR responses), the data transfer is then enabled, and the SCRRST is the inverse logic state of RTS#. Also, the operation procedure guarantees the correct activation sequence even if the driver cannot program the SCRCLK and SCRRST in the precise time points. In this way, the hardware meets the ICC specification.

- **ATR**

For the IC card with its own internal reset, its ATR begins within 400-40000 SCRCLK cycles. If no ATR is detected, the Smart Card IFD driver can then program the RTS# to low, and cause the SCRRST to high.

For some types of IC cards without internal reset signals, it will check out the SCRRST as active low reset, and begins its ATR within 400-40000 SCRCLK cycles from the time point of SCRRST rising edge.
The IT8702F does not support the type of IC Card that may send synchronous ATRs.

- **Deactivation and PTS Structure**

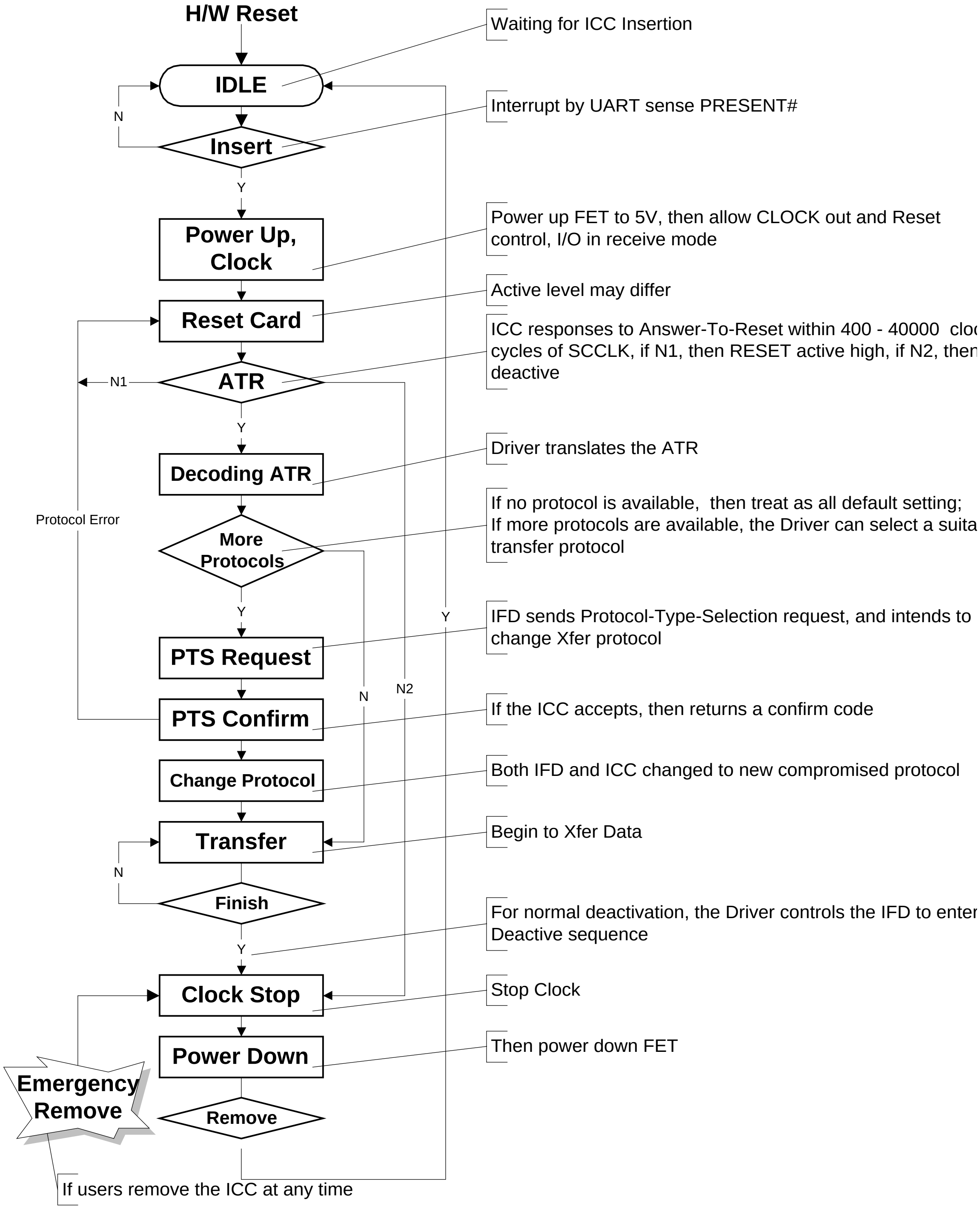
Whenever the IC card is removed or when the IFD driver intends to power off the SCR interface, the IFD will enter the deactivation sequence.

9.8.8 ATR and PTS Structure

The contents of the ATR (Answer-To-Reset) and PTS (Protocol-Type-Select) are defined in ISO/IEC 7816-X standards, which must be fully communicated by the ICC Resource manager, the ICC Service provider or the ICC application software.

After finalizing the coherent protocol, the SCR IFD enters the normal transfer mode. Since the SCRIO is the only data channel for both data transmit and receive as defined in the ICC Specification, the IT8702F can only support the half-duplex function. The SCRRST can be resent when a data transfer error occurs, and then the IFD driver will select a safer, lower-speed protocol to perform the data transfers again.

9.8.9 Smart Card Operating Sequence Example


H/W Reset
IDLE
Waiting for ICC Insertion
N
Insert
Interrupt by UART sense PRESENT#
Y
Power Up, Clock
Power up FET to 5V, then allow CLOCK out and Reset control, I/O in receive mode
Reset Card
Active level may differ
N1
ATR
ICC responses to Answer-To-Reset within 400 - 40000 cloc cycles of SCCLK, if N1, then RESET active high, if N2, then deactive
Y
Decoding ATR
Driver translates the ATR
Protocol Error
More Protocols
If no protocol is available, then treat as all default setting; If more protocols are available, the Driver can select a suita transfer protocol
Y
Y
PTS Request
IFD sends Protocol-Type-Selection request, and intends to change Xfer protocol
N
N2
PTS Confirm
If the ICC accepts, then returns a confirm code
Change Protocol
Both IFD and ICC changed to new compromised protocol
Transfer
Begin to Xfer Data
N
Finish
For normal deactivation, the Driver controls the IFD to enter Deactive sequence
Y
Clock Stop
Stop Clock
Power Down
Then power down FET
Emergency Remove
Remove
If users remove the ICC at any time

9.9 Parallel Port

The IT8702F incorporates one multi-mode high performance parallel port, which supports the IBM AT, PS/2 compatible bi-directional Standard Parallel Port (SPP), the Enhanced Parallel Port (EPP) and the Extended Capabilities Port (ECP). Please refer to the IT8702F Configuration registers and Configuration Description for information on enabling/ disabling, changing the base address of the parallel port, and operation mode selection.

Table 9-38. Parallel Port Connector in Different Modes

Host Connector	Pin No.	SPP	EPP	ECP
1	108	STB#	WRITE#	NStrobe
2-9	109-116	PD0 - 7	PD0 - 7	PD0 - 7
10	103	ACK#	INTR	nAck
11	102	BUSY	WAIT#	Busy PeriphAck(2)
12	101	PE	(NU) (1)	PError nAckReverse(2)
13	100	SLCT	(NU) (1)	Select
14	107	AFD#	DSTB#	nAutoFd HostAck(2)
15	106	ERR#	(NU) (1)	nFault nPeriphRequest(2)
16	105	INIT#	(NU) (1)	nInit nReverseRequest(2)
17	104	SLIN#	ASTB#	nSelectIn

Note1: NU: Not used.
Note 2: Fast mode.
Note 3: For more information, please refer to the IEEE 1284 standard.

9.9.1 SPP and EPP Modes

Table 9-39. Address Map and Bit Map for SPP and EPP Modes

Register	Address	I/O	D0	D1	D2	D3	D4	D5	D6	D7	Mode
Data Port	Base 1+0h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	SPP/EPP
Status Port	Base 1+1h	R	TMOUT	1	1	ERR#	SLCT	PE	ACK#	BUSY#	SPP/EPP
Control Port	Base 1+2h	R/W	STB	AFD	INIT	SLIN	IRQE	PDDIR	1	1	SPP/EPP
EPP Address Port	Base 1+3h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port0	Base 1+4h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port1	Base 1+5h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port2	Base 1+6h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port3	Base 1+7h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP

Note 1: The Base address 1 depends on the Logical Device configuration registers of Parallel Port (0X60, 0X61).

(1) Data Port (Base Address 1 + 00h)

This is a bi-directional 8-bit data port. The direction of data flow is determined by the bit 5 of the logic state of the control port register. It forwards directions when the bit is low and reverses directions when the bit is high.

(2) Status Port (Base Address 1 + 01h)

This is a **read only** register. Writing to this register has no effects. The contents of this register are latched during an IOR cycle.
Bit 7 - BUSY#: Inverse of printer BUSY signal, a logic "0" means that the printer is busy and cannot accept another character. A logic "1" means that it is ready to accept the next character.
Bit 6 - ACK#: Printer acknowledge, a logic "0" means that the printer has received a character and is ready to accept another. A logic "1" means that it is still processing the last character.
Bit 5 - PE: Paper end, a logic "1" indicates the paper end.
Bit 4 - SLCT: Printer selected, a logic "1" means that the printer is on line.
Bit 3 - ERR#: Printer error signal, a logic "0" means an error has been detected.
Bits 2, 1 - Reserved: These bits are always "1" when read.
Bit 0 - TMOUT: This bit is valid only in EPP mode and indicates that a 10-msec time-out has occurred in EPP operation. A logic "0" means no time-out occurred and a logic “1” means that a time-out error has been detected. This bit is cleared by an LRESET# or by writing a logic “1” to it. When the IT8702F is selected to non-EPP mode (SPP or ECP), this bit is always a logic "1" when read.

(3) Control Port (Base Address 1 + 02h)

This port provides all output signals to control the printer. The register can be read and written.
Bits 6, 7- Reserved: These two bits are always "1" when read.
Bit 5 - PDDIR: Data port direction control. This bit determines the direction of the data port register. Set this bit "0" to output the data port to PD bus, and "1" to input from PD bus.
Bit 4 - IRQE: Interrupt request enable. Setting this bit "1" enables the interrupt requests from the parallel port to the Host. An interrupt request is generated by a "0" to "1" transition of the ACK# signal.
Bit 3 - SLIN: Inverse of SLIN# pin. Setting this bit to "1" selects the printer.
Bit 2 - INIT: Initiate printer. Setting this bit to "0" initializes the printer.
Bit 1 - AFD: Inverse of the AFD# pin. Setting this bit to "1" causes the printer to automatically advance one line after each line is printed.
Bit 0 - STB: Inverse of the STB# pin. This pin controls the data strobe signal to the printer.

(4) EPP Address Port (Base Address 1 + 03h)

The EPP Address Port is only available in the EPP mode. When the Host writes to this port, the contents of D0 -D7 are buffered and output to PD0 - PD7. The leading edge of IOW (Internal signal, active when LPC I/O WRITE cycle is on this address) causes an EPP ADDRESS WRITE cycle. When the Host reads from this port, the contents of PD0 - PD7 are read. The leading edge of IOR (Internal signal, active when LPC I/O READ cycle is on this address) causes an EPP ADDRESS READ cycle.

(5) EPP Data Ports 0-3 (Base Address 1 + 04-07h)

The EPP Data Ports are only available in the EPP mode. When the Host writes to these ports, the contents of D0 - D7 are buffered and output to PD0 - PD7. The leading edge of IOW (Internal signal, active when LPC I/O WRITE cycle is on this address) causes an EPP DATA WRITE cycle. When the Host reads from these ports, the contents of PD0 - PD7 are read. The leading edge of IOR (Internal signal, active when LPC I/O READ cycle is on this address) causes an EPP DATA READ cycle.

9.9.2 EPP Mode Operation

When the parallel port of the IT8702F is set in the EPP mode, the SPP mode is also available. If no EPP Address/Data Port address is decoded (Base address + 03h- 07h), the PD bus is in the SPP mode, and the output signals such as STB#, AFD#, INIT#, and SLIN# are set by the SPP control port. The direction of the data port is controlled by the bit 5 of the control port register. There is a 10-msec time required to prevent the system from lockup. The time has elapsed from the beginning of the IOCHRDY (Internal signal: When active, the IT8702F will issue Long Wait in SYNC field) high (EPP READ/WRITE cycle) to WAIT# being de-asserted. If a time-out occurs, the current EPP READ/WRITE cycle is aborted and a logic "1" will be read in the bit 0 of the status port register. The Host must write 0 to bits 0, 1, 3 of the control port register before any EPP READ/WRITE cycle (EPP spec.). The pins STB#, AFD# and SLIN# are controlled by hardware for the hardware handshaking during EPP READ/WRITE cycle.

(1) EPP ADDRESS WRITE

1. The Host writes a byte to the EPP Address Port (Base address + 03h). The chip drives D0 - D7 onto PD0 - PD7.
2. The chip asserts WRITE# (STB#) and ASTB# (SLIN#) after IOW becomes active.
3. The peripheral de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts ASTB#, latches the address from D0 - D7 to PD bus, allowing the Host to complete the I/O WRITE cycle.
4. The peripheral asserts WAIT#, indicating that it acknowledges the termination of the cycle. Then, the chip de-asserts WRITE to terminate the cycle.

(2) EPP ADDRESS READ

1. The Host reads a byte from the EPP Address Port. The chip drives PD bus to tri-state for the peripheral to drive.
2. The chip asserts ASTB# after IOR becomes active.
3. The peripheral drives the PD bus valid and de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts ASTB#, latches the address from PD bus to D0 -D7, allowing the Host to complete the I/O READ cycle.
4. The peripheral drives the PD bus to tri-state and then asserts WAIT#, indicating that it acknowledges the termination of the cycle.

(3) EPP DATA WRITE

1. The host writes a byte to the EPP Data Port (Base address +04H - 07H). The chip drives D0- D7 onto PD0 -PD7.
2. The chip asserts WRITE# (STB#) and DSTB# (AFD#) after IOW becomes active.
3. The peripheral de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts DSTB#, latches the data from D0 - D7 to the PD bus, allowing the Host to complete the I/O WRITE cycle.
4. The peripheral asserts WAIT#, indicating that it acknowledges the termination of the cycle. Then, the chip de-asserts WRITE to terminate the cycle.

(4) EPP DATA READ

1. The Host reads a byte from the EPP DATA Port. The chip drives PD bus to tri-state for the peripheral to drive.
2. The chip asserts DSTB# after IOR becomes active.
3. The peripheral drives PD bus valid and de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts DSTB#, latches the data from PD bus to D0 - D7, allowing the host to complete the I/O READ cycle.
4. The peripheral tri-states the PD bus and then asserts WAIT#, indicating that it acknowledges the

termination of the cycle.

9.9.3 ECP Mode Operation

This mode is both software and hardware compatible with the existing parallel ports, allowing ECP to be used as a standard LPT port when the ECP mode is not required. It provides an automatic high-burst-bandwidth channel that supports DMA or the ECP mode in both forward and reverse directions. A 16-byte FIFO is implemented in both forward and reverse directions to smooth data flow and enhance the maximum bandwidth requirement allowed. The port supports automatic handshaking for the standard parallel port to improve compatibility and expedite the mode transfer. It also supports run-length encoded (RLE) decompression in hardware. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times a byte has been repeated. The IT8702F does not support hardware RLE compression. For a detailed description, please refer to "Extended Capabilities Port Protocol and ISA Interface Standard".

Table 9-40. Bit Map of the ECP Registers

Register	D7	D6	D5	D4	D3	D2	D1	D0
data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
ecpAFifo	Addr/RLE	Address or RLE field						
dsr	nBusy	nAck	PError	Select	nFault	1	1	1
dcr	1	1	PDDIR	IRQE	SelectIn	nInit	AutoFd	Strobe
cFifo	Parallel Port Data FIFO							
ecpDFifo	ECP Data FIFO							
tFifo	Test FIFO							
cnfgA	0	0	0	1	0	0	0	0
cnfgB	0	intrValue	0	0	0	0	0	0
ecr	mode			nErrIntrEn	dmaEn	ServiceIntr	full	empty

(1) ECP Register Definitions

Table 9-41. ECP Register Definitions

Name	Address	I/O	ECP Mode	Function
data	Base 1 +000H	R/W	000-001	Data Register
ecpAFifo	Base 1 +000H	R/W	011	ECP FIFO (Address)
dsr	Base 1 +001H	R/W	All	Status Register
dcr	Base 1 +002H	R/W	All	Control Register
cFifo	Base 2 +000H	R/W	010	Parallel Port Data FIFO
ecpDFifo	Base 2 +000H	R/W	011	ECP FIFO (DATA)
tFifo	Base 2 +000H	R/W	110	Test FIFO
cnfgA	Base 2 +000H	R	111	Configuration Register A
cnfgB	Base 2 +001H	R/W	111	Configuration Register B
ecr	Base 2 +002H	R/W	All	Extended Control Register

Note 1: The Base address 1 depends on the Logical Device configuration registers of Parallel Port (0X60, 0X61).

Note 2: The Base address 2 depends on the Logical Device configuration registers of Parallel Port (0X62, 0X63).

(2) ECP Mode Descriptions

Table 9-42. ECP Mode Descriptions

Mode	Description
000	Standard Parallel Port Mode
001	PS/2 Parallel Port Mode
010	Parallel Port FIFO Mode
011	ECP Parallel Port Mode
110	Test Mode
111	Configuration Mode

Note: Please refer to the ECP Register Description on pages 128-129 for a detailed description of the mode selection.

(3) ECP Pin Descriptions

Table 9-43. ECP Pin Descriptions

Name	Attribute	Description
nStrobe (HostClk)	O	Used for handshaking with Busy to write data and addresses into the peripheral device.
PD0-PD7	I/O	Address or data or RLE data.
nAck (PeriphClk)	I	Used for handshaking with nAutoFd to transfer data from the peripheral device to the Host.
Busy (PeriphACK)	I	The peripheral uses this signal for flow control in the forward direction (handshaking with nStrobe). In the reverse direction, this signal is used to determine whether a command or data information is present on PD0-PD7.
Perror (nAckReverse)	I	Used to acknowledge nInit from the peripheral which drives this signal low, allowing the host to drive the PD bus.
Select	I	Printer On-Line Indication.
nAutoFd (HostAck)	O	In the reverse direction, it is used for handshaking between the nAck and the Host. When it is asserted, a peripheral data byte is requested. In the forward direction, this signal is used to determine whether a command or data information is present on PD0 - PD7.
nFault (nPeriphRequest)	I	In the forward direction (only), the peripheral is allowed (but not required) to assert this signal (low) to request a reverse transfer while in ECP mode. The signal provides a mechanism for peer-to-peer communication. It is typically used to generate an interrupt to host, which has the ultimate control over the transfer direction.
nInit (nReverseRequest)	O	The host may drive this signal low to place the PD bus in the reverse direction. In the ECP mode, the peripheral is permitted to drive the PD bus when nInit is low, and nSelectIn is high.
NSelectIn (1284 Active)	O	Always inactive (high) in the ECP mode.

(4) Data Port (Base 1+00h, Modes 000 and 001)

Its contents will be cleared by a RESET. In a WRITE operation, the contents of the LPC data fields are latched by the Data Register. The contents are then sent without being inverted to PD0-PD7. In a READ operation, the contents of data ports are read and sent to the host.

(5) ecpAFifo Port (Address/RLE) (Base 1 +00h, Mode 011)

Any data byte written to this port are placed in the FIFO and tagged as an ECP Address/RLE. The hardware then automatically sends this data to the peripheral. Operation of this port is valid only in the forward direction (dcr(5)=0).

(6) Device Status Register (dsr) (Base 1 +01h, Mode All)

Bits 0, 1 and 2 of this register are not implemented. These bit states are remained at high in a READ operation of the Printer Status Register.

dsr(7): This bit is the inverted level of the Busy input.
dsr(6): This bit is the state of the nAck input.
dsr(5): This bit is the state of the PError input.
dsr(4): This bit is the state of the Select input.
dsr(3): This bit is the state of the nFault input.
dsr(2)-dsr(0): These bits are always 1.

(7) Device Control Register (dcr) (Base 1+02h, Mode All)

Bits 6 and 7 of this register have no function. They are set high during the READ operation, and cannot be written. Contents in bits 0-5 are initialized to 0 when the RESET pin is active.

dcr(7)-dcr(6): These two bits are always high.
dcr(5):Except in the modes 000 and 010, setting this bit low means that the PD bus is in output operation; setting it high, in input operation. This bit will be forced to low in mode 000.
dcr(4): Setting this bit high enables the interrupt request from peripheral to the host due to a rising edge of the nAck input.
dcr(3): It is inverted and output to SelectIn.
dcr(2): It is output to nInit without inversion.
dcr(1): It is inverted and output to nAutoFd.
dcr(0): It is inverted and output to nStrobe.

(8) Parallel Port Data FIFO (cFifo) (Base 2+00h, Mode 010)

Bytes written or DMA transferred from the Host to this FIFO are sent by a hardware handshaking to the peripheral according to the Standard Parallel Port protocol. This operation is only defined for the forward direction.

(9) ECP Data FIFO (ecpDFifo) (Base 2+00h, Mode 011)

When the direction bit dcr(5) is 0, bytes written or DMA transferred from the Host to this FIFO are sent by hardware handshaking to the peripheral according to the ECP parallel port protocol. When dcr(5) is 1, data bytes from the peripheral to this FIFO are read in an automatic hardware handshaking. The Host can receive these bytes by performing READ operations or DMA transfers from this FIFO.

(10) Test FIFO (tFifo) (Base 2+00h, Mode 110)

The host may operate READ/WRITE or DMA transfers to this FIFO in any directions. Data in this FIFO will be displayed on the PD bus without using hardware protocol handshaking. The tFifo will not accept new data after it is full. Making a READ from an empty tFifo causes the last data byte to return.

(11) Configuration Register A (cnfgA) (Base 2+00h, Mode 111)

This **read only** register indicates to the system that interrupts are ISA-Pulses compatible. This is an 8-bit implementation by returning a 10h.

(12) Configuration Register B (cnfgB) (Base 2+01h, Mode 111)

This register is **read only**.

cnfgB(7): A logic “0” read indicates that the chip does not support hardware RLE compression.
cnfgB(6): Reserved.
cnfgB(5)-cnfg(3): A value 000 read indicates that the interrupt must be selected with jumpers.
cnfgB(2)-cnfg(0): A value 000 read indicates that the DMA channel is jumpered 8-bit DMA.

(13) Extended Control Register (ecr) (Base 2+02h, Mode All)

ECP function control register.

ecr(7)-ecr(5): These bits are used for READ/WRITE and mode selection.

Table 9-44. Extended Control Register (ECR) Mode and Description

ECR	Mode and Description
000	**Standard Parallel Port Mode** The FIFO is reset and the direction bit dcr(5) is always 0 (forward direction) in this mode.
001	**PS/2 Parallel Port Mode** It is similar to the SPP mode, except that the dcr(5) is **read/write**. When dcr(5) is 1, the PD bus is tri-state. Reading the data port returns the value on the PD bus instead of the value of the data register.
010	**Parallel Port Data FIFO Mode** This mode is similar to the 000 mode, except that the Host writes or DMA transfers the data bytes to the FIFO. The FIFO data are then transmitted to the peripheral using the standard parallel port protocol automatically. This mode is only valid in the forward direction (dcr(5)=0).
011	**ECP Parallel Port Mode** In the forward direction, bytes placed into the ecpDFifo and ecpAFifo are placed in a single FIFO and automatically transmitted to the peripheral under the ECP protocol. In the reverse direction, bytes are transmitted to the ecpDFifo from the ECP port.
100, 101	**Reserved, not defined.**
110	**Test Mode** In this mode, the FIFO may be read from or written to, but it cannot be sent to the peripheral.
111	**Configuration Mode** In this mode, the cnfgA and cnfgB registers are accessible at 0x400 and 0x401.

ecr(4): nErrIntrEn, READ/WRITE, Valid in ECP(011) Mode

1: Disables the interrupt generated on the asserting edge of the nFault input.

0: Enables the interrupt pulse on the asserting edge of the nFault. An interrupt pulse will be generated if nFault is asserted, or if this bit is written from 1 to 0 in the low-level nFault.

ecr(3): dmaEn, READ/WRITE

1: Enables DMA. DMA starts when serviceIntr (ecr(2)) is 0.

0: Disables DMA unconditionally.

ecr(2): ServiceIntr, READ/WRITE

1: Disables DMA and all service interrupts.

0: Enables the service interrupts. This bit will be set to “1” by hardware when one of the three service interrupts has occurred.

Writing “1” to this bit will not generate an interrupt.

Case 1: dmaEn=1

During DMA, this bit is set to 1 (a service interrupt generated) if the terminal count is reached.

Case 2: dmaEn=0, dcr(5)=0

This bit is set to 1 (a service interrupt generated) whenever there are writeIntrThreshold or more bytes space free in the FIFO.

Case 3: dmaEn=0, dcr(5)=1

This bit is set to 1 (a service interrupt generated) whenever there are readIntrThreshold or more valid bytes to be read from the FIFO.

ecr(1): full, **read only**

1: The FIFO is full and cannot accept another byte.

0: The FIFO has at least 1 free data byte space.

ecr(0): empty, **read only**

1: The FIFO is empty.

0: The FIFO contains at least 1 data byte.

(14) Mode Switching Operation

In programmed I/O control (mode 000 or 001), P1284 negotiation and all other tasks that happen before data transmission are software-controlled. Setting mode to 011 or 010 will cause the hardware to perform an automatic control-line handshaking, transferring information between the FIFO and the ECP port.

From the mode 000 or 001, any other mode may be immediately switched to any other mode. To change direction, the mode must first be set to 001.

In the extended forward mode, the FIFO must be cleared and all the signals must be de-asserted before returning to mode 000 or 001. In ECP reverse mode, all data must be read from the FIFO before returning to mode 000 or 001. Usually, unneeded data are accumulated during ECP reverse handshaking, when the mode is changed during a data transfer. In such conditions, nAutoFd will be de-asserted regardless of the transfer state. To avoid bugs during handshaking signals, these guidelines must be followed.

(15) Software Operation (ECP)

Before the ECP operation can begin, it is first necessary for the Host to switch the mode to 000 in order to negotiate with the parallel port. During this process, the Host determines whether the peripheral supports the ECP protocol.

After this negotiation is completed, the mode is set to 011 (ECP). To enable the drivers, the direction must be set to 0. Both strobe and autoFd are set to 0, causing nStrobe and nAutoFd signals to be de-asserted.

All FIFO data transfers are PWord wide and PWord aligned. Permitted only in the forward direction, Address/RLE transfers are byte-wide. The ECP Address/RLE bytes may be automatically sent by writing to the ecpAFifo. Similarly, data PWords may be automatically sent via the ecpDFifo.

To change directions, the Host switches mode to 001. It then negotiates either the forward or reverse channel, sets the direction to 1 or 0, and finally switches mode to 001. If the direction is set to 1, the hardware performs the handshaking for each ECP data byte read, then tries to fill the FIFO. At this time, PWords may be read from the ecpDFifo while it retains data. It is also possible to perform the ECP transfers by handshaking with individual bytes under programmed control in mode = 001, or 000, even though this is a comparatively time-consuming approach.

(16) Hardware Operation (DMA)

The Standard PC DMA protocol (through LDRQ#) is followed. As in the programmed I/O case, software sets THE direction and state. Next, the desired count and memory addresses are programmed into DMA controller. The dmaEn is set to 1, and the serviceIntr is set to 0. To complete the process, the DMA channel with the DMA controller is unmasked. The contents in the FIFO are emptied or filled by DMA using the right mode and direction.

DMA is always transferred to or from the FIFO located at 0 x 400. By generating an interrupt and asserting a serviceIntr, DMA is disabled when the DMA controller reaches the terminal count. By not asserting LDRQ# for more than 32 consecutive DMA cycles, blocking of refresh requests is eliminated.

When it is necessary to disable a DMA while performing a transfer, the host DMA controller is disabled, serviceIntr is then set to 1, and dmaEn is next set to 0. If the contents in FIFO are empty or full, the DMA will start again. This is first done by enabling the host DMA controller, and then setting dmaEn to 1. Finally, serviceIntr is set to 0. Upon completion of a DMA transfer in the forward direction, the software program must wait until the contents in FIFO are empty and the busy line is low, ensuring that all data successfully reach the peripheral device.

(17) Interrupts

It is necessary to generate an interrupt when any of the following states are reached.

1. serviceIntr = 0, dmaEn = 0, direction = 0, and the number of PWords in the FIFO is greater than or equal to writeIntrThreshold.
2. serviceIntr = 0, dmaEn = 0, direction = 1, and the number of PWords in the FIFO is greater than or equal to readIntrThreshold.
3. serviceIntr = 0, dmaEn = 1, and DMA reaches the terminal count.
4. nErrIntrEn = 0 and nFault goes from high to low or when nErrIntrEn is set from 1 to 0 and nFault is asserted.
5. ackIntEn = 1. In current implementations of using existing parallel ports, the interrupt generated may be either edge or level trigger type.

(18) Interrupt Driven Programmed I/O

It is also possible to use an interrupt-driven programmed I/O to execute either ECP or parallel port FIFOs. An interrupt will occur in the forward direction when serviceIntr is 0 and the number of free PWords in the FIFO is equal to or greater than writeIntrThreshold. If either of these conditions is not met, it may be filled with writeIntrThreshold PWords. An interrupt will occur in the reverse direction when serviceIntr is 0 and the number of available PWords in the FIFO is equal to readIntrThreshold. If it is full, the FIFO can be completely emptied in a single burst. If it is not full, only a number of PWords equal to readIntrThreshold may be read from the FIFO in a single burst. In the Test mode, software can determine the values of writeIntrThreshold, readIntrThreshold, and FIFO depth while accessing the FIFO.

Any PC LPC bus implementation that is adjusted to expedite DMA or I/O transfer must ensure that the bandwidth on the ISA is maintained on the interface. Although the LPC (even PCI) bus of PC cannot be directly controlled, the interface bandwidth of ECP port can be constrained to perform at the optimum speed.

(19) Standard Parallel Port

In the forward direction with DMA, the standard parallel port is run at or close to the permitted peak bandwidth of 500 KB/sec. The state machine does not examine nAck, but just begins the next DMA based on the Busy signal.

9.10 Keyboard Controller (KBC)

The keyboard controller is implemented using an 8-bit microcontroller that is capable of executing the 8042 instruction set. For general information, please refer the description of the 8042 in the 8-bit controller handbook. In addition, the microcontroller can enter power-down mode by executing two types of power-down instructions. The 8-bit microcontroller has 256 bytes of RAM for data memory and 2 Kbytes of ROM for the program storage.

The ROM codes may come from various vendors (or users), and are programmed during the manufacturing process. To assist in developing ROM codes, the keyboard controller has an external access mode. In the external access mode, the internal ROM is disabled and the instructions executed by the microcontroller come from an externally connected ROM.

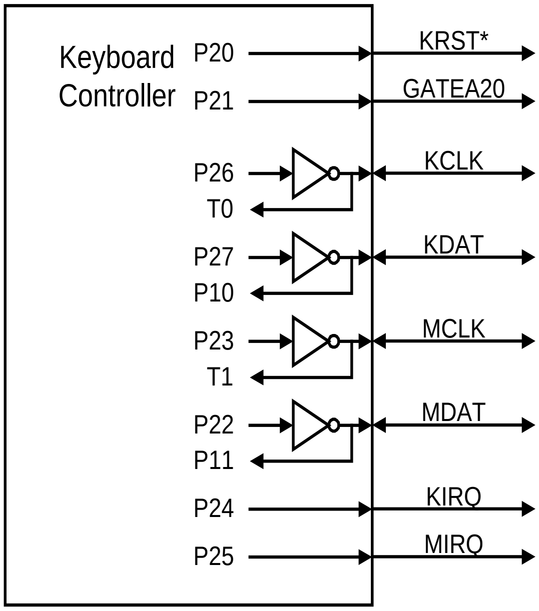

Keyboard Controller
P20
P21
P26
T0
P27
P10
P23
T1
P22
P11
P24
P25
KRST*
GATEA20
KCLK
KDAT
MCLK
MDAT
KIRQ
MIRQ

Figure 9-7. Keyboard and Mouse Interface

9.10.1 Host Interface

The keyboard controller interfaces with the system through the 8042 style host interface. The table 10-45 shows how the interface decodes the control signals.

Table 9-45. Data Register READ/WRITE Controls

Host Address Note	R/W*	Function
60h	R	READ DATA
60h	W	WRITE DATA, (Clear F1)
64h	R	READ Status
64h	W	WRITE Command, (set F1)

Note: These are the default values of the LDN5, 60h and 61h (DATA); LDN5, 62h and 63h (Command). All these registers are programmable.

READ DATA: This is an 8-bit **read only** register. When read, the KIRQ output is cleared and OBF flag in the status register is cleared.

WRITE DATA: This is an 8-bit **write only** register. When written, the F1 flag of the Status register is cleared and the IBF bit is set.

READ Status: This is an 8-bit **read only** register. Refer to the description of the Status register for more information.

WRITE Command: This is an 8-bit **write only** register. When written, both F1 and IBF flags of the Status register are set.

9.10.2 Data Registers and Status Register

The keyboard controller provides two data registers: one is DBIN for data input, and the other is DBOUT for data output. Each of the data registers is 8 bits wide. A write (microcontroller) to the DBOUT will load Keyboard Data Read Buffer, set OBF flag and set the KIRQ output. A read (microcontroller) of the DBIN will read the data from the Keyboard Data or Command Write Buffer and clear the IBF flag.

The status register holds information concerning the status of the data registers, the internal flags, and some user-defined status bits. Please refer to Table 10-46. The bit 0 OBF is set to “1” when the microcontroller writes a data into DBOUT, and is cleared when the system initiates a DATA READ operation. The bit 1 IBF is set to “1” when the system initiates a WRITE operation, and is cleared when the microcontroller executes an “IN A, DBB” instruction. The F0 and F1 flags can be set or reset when the microcontroller executes the clear and complement flag instructions. F1 also holds the system WRITE information when the system performs the WRITE operations.

Table 9-46. Status Register

7	6	5	4	3	2	1	0
ST7	ST6	ST5	ST4	F1	F0	IBF	OBF

9.10.3 Keyboard and Mouse Interface

KCLK is the keyboard clock pin. Its output is the inversion of pin P26 of the microcontroller, and the input of KCLK is connected to the T0 pin of the microcontroller. KDAT is the keyboard data pin; its output is the inversion of pin P27 of the microcontroller, and the input of KDAT is connected to the P10 of the microcontroller. MCLK is the mouse clock pin; its output is the inversion of pin P23 of the microcontroller, and the input of MCLK is connected to the T1 pin of the microcontroller. MDAT is the Mouse data pin; its output is the inversion of pin P22 of the microcontroller, and the input of MDAT is connected to the P11 of the microcontroller. KRST# is pin P20 of the microcontroller. GATEA20 is the pin P21 of the microcontroller. These two pins are used as software controlled or user defined outputs. External pull-ups may be required for these pins.

9.10.4 KIRQ and MIRQ

KIRQ is the interrupt request for keyboard (Default IRQ1), and MIRQ is the interrupt request for mouse (Default IRQ12). KIRQ is internally connected to P24 pin of the microcontroller, and MIRQ is internally connected to pin P25 of the microcontroller.

9.11 Consumer Remote Control (TV Remote) IR (CIR)

9.11.1 Overview

The CIR is used in Consumer Remote Control equipment, and is a programmable amplitude shift keyed (ASK) serial communication protocol. By adjusting frequencies, baud rate divisors and sensitivity ranges, the CIR registers are able to support the popular protocols such as RC-5, NEC, and RECS-80. Software driver programming can support new protocols.

9.11.2 Features

- Supports 30 kHz – 57 kHz (low frequency) or 400 kHz – 500 kHz (high frequency) carrier transmission
- Baud rates up to 115200 BPS (high frequency)
- Demodulation optional
- Supports transmission run-length encoding and deferral functions
- 32-byte FIFO for data transmission or data reception

9.11.3 Block Diagram

The CIR consists of the Transmitter and Receiver parts. The Transmitter part is responsible for transmitting data to the FIFO, processing the FIFO data by serialization, modulation and sending out the data through the LED device. The Receiver part is responsible for receiving data, processing data by demodulation, deserialization and storing data in the Receiver FIFO.

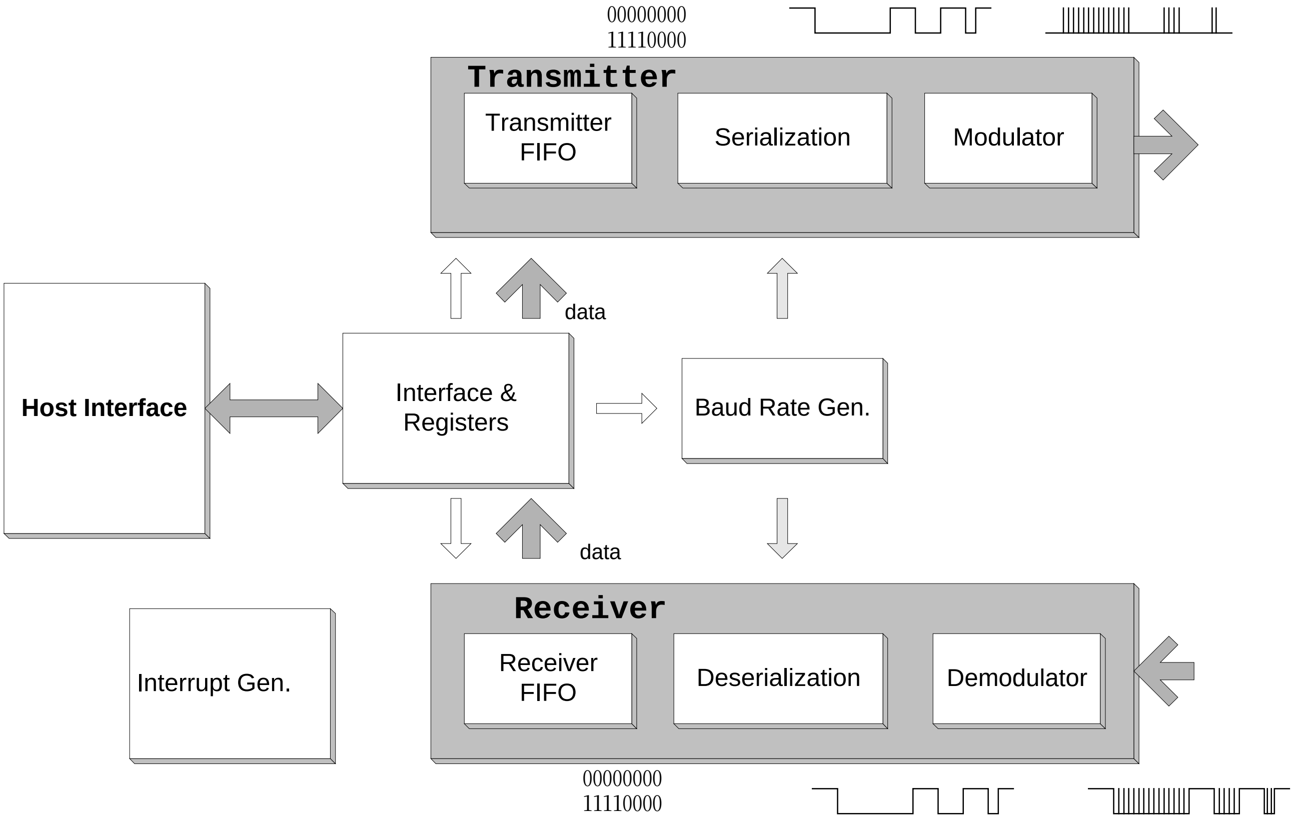

00000000
11110000
Transmitter
Transmitter FIFO
Serialization
Modulator
data
Host Interface
Interface & Registers
Baud Rate Gen.
data
Interrupt Gen.
Receiver
Receiver FIFO
Deserialization
Demodulator
00000000
11110000

Figure 9-8. CIR Block Diagram

9.11.4 Transmit Operation

The data written to the Transmitter FIFO will be exactly serialized from LSB to MSB, modulated with carrier frequency and sent to the CIRTX output. The data are either in bit-string format or run-length decode.

Before the data transmission can begin, code byte write operations must be performed to the Transmitter FIFO DR. The bit TXRLE in the TCR1 should be set to "1" before the run-length decode data can be written into the Transmitter FIFO. Set TXENDF in the TCR1 will enable the data transmission deferral, and avoid the transmitter FIFO underrun. The bit width of the serialized bit string is determined by the value programmed in the baud rate divisor registers BDLR and BDHR. When the bits HCFS and CFQ[4:0] are set, either the high-speed or low-speed carrier range is selected, and the corresponding carrier frequency will also be determined. Bits TXMPM[1:0] and TXMPW[2:0] specify the pulse numbers in a bit width and the required duty cycles of the carrier pulse according to the communication protocol. Only a logic "0" can activate the Transmitter LED in the format of a series of modulating pulses.

9.11.5 Receive Operation

The Receiver function is enabled if the bit RXEN in the RCR is set to "1". Either demodulated or modulated RX# signal is loaded in0to the Receiver FIFO, and the bit RXEND in the RCR determines the demodulation logic should be used or not. Determine the baud rate by programming the baud rate divisor registers BDLR and BDHR, and the carrier frequencies by programming the bits HCFS and CFQ[4:0]. Set RDWOS to "0" to sync. The bit RXACT in the RCR is set to "1" when the serial data or the selected carrier is incoming, and the sampled data will then be kept in the Receiver FIFO. Write "1" to the bit RXACT to stop the Receiver operation; "0" to the bit RXEN to disable the Receiver.

9.11.6 Register Descriptions and Address

Table 9-47. List of CIR Registers

Register Name	R/W	Address	Default
CIR Data Register (DR)	R/W	Base + 0h	FFh
CIR Interrupt Enable Register (IER)	R/W	Base + 1h	00h
CIR Receiver Control Register (RCR)	R/W	Base + 2h	01h
CIR Transmitter Control Register 1 (TCR1)	R/W	Base + 3h	00h
CIR Transmitter Control Register 2 (TCR2)	R/W	Base + 4h	5Ch
CIR Transmitter Status Register (TSR)	R	Base + 5h	00h
CIR Receiver Status Register (RSR)	R	Base + 6h	00h
CIR Baud Rate Divisor Low Byte Register (BDLR)	R/W	Base + 5h	00h
CIR Baud Rate Divisor High Byte Register (BDHR)	R/W	Base + 6h	00h
CIR Interrupt Identification Register (IIR)	R/W	Base + 7h	01h

9.11.6.1 CIR Data Register (DR)

The DR, an 8-bit **read/write** register, is the data port for CIR. Data are transmitted and received through this register.

Address: Base Address + 0h

Bit	R/W	Default	Description
7 – 0	R/W	FFh	**CIR Data Register (DR[7:0])** Writing data to this register causes data to be written to the Transmitter FIFO. Reading data from this register causes data to be received from the Receiver FIFO.

9.11.6.2 CIR Interrupt Enable Register (IER)

The IER, an 8-bit **read/write** register, is used to enable the CIR interrupt request.

Address: Base Address + 1h

Bit	R/W	Default	Description
7-6	-	-	**Reserved for ITE use**
5	R/W	0b	**RESET (RESET)** This bit is a software reset function. Writing a “1” to this bit resets the registers of DR, IER, TCR1, BDLR, BDHR and IIR. This bit is then cleared to initial value automatically.
4	R/W	0b	**Baud Rate Register Enable Function Enable (BR)** This bit is used to control the baud rate registers enable read/write function. Set this bit to “1” to enable the baud rate registers for CIR. Set this bit to “0” to disable the baud rate registers for CIR.
3	R/W	0b	**Interrupt Enable Function Control (IEC)** This bit is used to control the interrupt enable function. Set this bit to “1” to enable the interrupt request for CIR. Set this bit to “0” to disable the interrupt request for CIR.
2	R/W	0b	**Receiver FIFO Overrun Interrupt Enable (RFOIE)** This bit is used to control Receiver FIFO Overrun Interrupt request. Set this bit to “1” to enable Receiver FIFO Overrun Interrupt request. Set this bit to “0” to disable Receiver FIFO Overrun Interrupt request.
1	R/W	0b	**Receiver Data Available Interrupt Enable (RDAIE)** This bit is used to enable Receiver Data Available Interrupt request. The Receiver will generate this interrupt when the data available in the FIFO exceed the FIFO threshold level. Set this bit to “1” to enable Receiver Data Available Interrupt request. Set this bit to “0” to disable Receiver Data Available Interrupt request.
0	R/W	0b	**Transmitter Low Data Level Interrupt Enable (TLDLIE)** This bit is used to enable Transmitter Low Data Level Interrupt request. The Transmitter will generate this interrupt when the data available in the FIFO are less than the FIFO threshold Level. Set this bit to “1” to enable Transmitter Low Data Level Interrupt request. Set this bit to “0” to disable Transmitter Low Data Level Interrupt request.

9.11.6.3 CIR Receiver Control Register (RCR)

The RCR, an 8-bit **read/write** register, is used to control the CIR Receiver.

Address: Base Address + 2h

Bit	R/W	Default	Description
7	R/W	0b	**Receiver Data Without Sync. (RDWOS)** This bit is used to control the sync. logic for receiving data. Set this bit to "1" to obtain the receiving data without sync. logic. Set this bit to "0" to obtain the receiving data in sync. logic.
6	R/W	0b	**High-Speed Carrier Frequency Select (HCFS)** This bit is used to select Carrier Frequency between high-speed and low-speed. 0: 30-58 kHz (Default) 1: 400-500 kHz
5	R/W	0b	**Receiver Enable (RXEN)** This bit is used to enable Receiver function. Enable Receiver and the RXACT will be active if the selected carrier frequency is received. Set this bit to "1" to enable the Receiver function. Set this bit to "0" to disable the Receiver function.
4	R/W	0b	**Receiver Demodulation Enable (RXEND)** This bit is used to control the Receiver Demodulation logic. If the Receiver device can not demodulate the correct carrier, set this bit to "1". Set this bit to "1" to enable Receiver Demodulation logic. Set this bit to "0" to disable Receiver Demodulation logic.
3	R/W	0b	**Receiver Active (RXACT)** This bit is used to control the Receiver operation. This bit is set to "0" when the Receiver is inactive. This bit will be set to "1" when the Receiver detects a pulse (RXEND=0) or pulse-train (RXEND=1) with correct carrier frequency. The Receiver then starts to sample the input data when Receiver Active is set. Write a "1" to this bit to clear the Receiver Active condition and make the Receiver enter the inactive mode.
2-0	R/W	001b	**Receiver Demodulation Carrier Range (RXDCR[2:0])** These three bits are used to set the tolerance of the Receiver. Demodulation carrier frequency. See Table 10-49 and Table 10-50.

9.11.6.4 CIR Transmitter Control Register 1 (TCR1)

The TCR1, an 8-bit **read/write** register, is used to control the Transmitter.

Address: Base Address + 3h

Bit	R/W	Default	Description
7	R/W	0b	**FIFO Clear (FIFOCLR)** Writing a "1" to this bit clears the FIFO. This bit is then cleared to "0" automatically.
6	R/W	0b	**Internal Loopback Enable (ILE)** This bit is used to execute internal loopback for test and must be "0" in normal operation. Set this bit to "0" to disable the Internal Loopback mode. Set this bit to "1" to enable the Internal Loopback mode.
5 - 4	R/W	0b	**FIFO Threshold Level (FIFOTL)** These two bits are used to set the FIFO Threshold Level. The FIFO length is 32 bytes for TX or RX function (ILE = 0) in normal operation and 16 bytes for both TX and RX in internal Loopback mode (ILE = 1). **16-Byte Mode** **32-Byte Mode** **00** **1** **1 (Default)** 01 3 7 10 7 17 11 13 25
3	R/W	0b	**Transmitter Run Length Enable (TXRLE)** This bit controls the Transmitter Run Length encoding/decoding mode, which condenses a series of "1" or "0" into one byte with the bit value stored in bit 7 and number of bits minus 1 in bits 6 – 0. Set this bit to "1" to enable the Transmitter Run Length mode. Set this bit to "0" to disable the Transmitter Run Length mode.
2	R/W	0b	**Transmitter Deferral (TXENDF)** This bit is used to avoid Transmitter underrun condition. When this bit is set to "1", the Transmitter FIFO data will be kept until the transmitter time-out condition occurs, or the FIFO reaches full.
1-0	R/W	0b	**Transmitter Modulation Pulse Mode (TXMPM[1:0])** These two bits are used to define the Transmitter modulation pulse mode. **TXMPM[1:0]** **Modulation Pulse Mode** C_pls mode (Default): Pulses are generated continuously for the entire logic 0 bit time. 8_pls mode: 8 pulses are generated for each logic 0 bit. 6_pls mode: 6 pulses are generated for each logic 0 bit. 11: Reserved.

9.11.6.5 CIR Transmitter Control Register (TCR2)

The TCR2, an 8-bit **read/write** register, is used to determine the carrier frequency.

Address: Base Address + 4h

<table>
<tr><th>Bit</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td>7-3</td><td>R/W</td><td>01011b</td><td>Carrier Frequency (CFQ[4:0])
These five bits are used to determine the modulation carrier frequency. See Table 10-48.</td></tr>
<tr><td>2-0</td><td>R/W</td><td>100b</td><td>Transmitter Modulation Pulse Width (TXMPW[2:0])
These three bits are used to set the Transmitter Modulation pulse width. The duty cycle of the carrier will be determined according to the settings of Carrier Frequency and the selection of Transmitter Modulation pulse width.
<table>
<tr><th>TXMPW[2:0]</th><th>HCFS = 0</th><th>HCFS = 1</th></tr>
<tr><td>000</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>001</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>010</td><td>6 µs</td><td>0.7 µs</td></tr>
<tr><td>011</td><td>7 µs</td><td>0.8 µs</td></tr>
<tr><td>100</td><td>8.7 µs</td><td>0.9 µs (Default)</td></tr>
<tr><td>101</td><td>10.6 µs</td><td>1.0 µs</td></tr>
<tr><td>110</td><td>13.3 µs</td><td>1.16 µs</td></tr>
<tr><td>111</td><td>Reserved</td><td>Reserved</td></tr>
</table>
</td></tr>
</table>

Table 9-48. Modulation Carrier Frequency

CFQ	Low Frequency (HCFS =0)	High Frequency (HCFS = 1)
00000	27 kHz	-
00010	29 kHz	-
00011	30 kHz	400 kHz
00100	31 kHz	-
00101	32 kHz	-
00110	33 kHz	-
00111	34 kHz	-
01000	35 kHz	450 kHz
01001	36 kHz	-
01010	37 kHz	-
01011	**38 kHz (default)**	**480 kHz (default)**
01100	39 kHz	-
01101	40 kHz	500 kHz
01110	41 kHz	-
01111	42 kHz	-
10000	43 kHz	-
10001	44 kHz	-
10010	45 kHz	-
10011	46 kHz	-
10100	47 kHz	-
10101	48 kHz	-
10110	49 kHz	-
10111	50 kHz	-
11000	51 kHz	-
11001	52 kHz	-
11010	53 kHz	-
11011	54 kHz	-
11100	55 kHz	-
11101	56 kHz	-
11110	57 kHz	-
11111	58 kHz	-

Table 9-49. Receiver Demodulation Low Frequency (HCFS = 0)

RXDCR	001		010		011		100		101		110		
CFQ	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**(Hz)**
00001	26.25	29.75	24.5	31.5	22.75	33.25	21	35	19.25	36.75	17.5	38.5	28k
00010	27.19	30.81	25.38	32.63	23.56	34.44	21.75	36.25	19.94	38.06	18.13	39.88	29k
00011	28.13	31.88	26.25	33.75	24.38	35.63	22.5	37.5	20.63	39.38	18.75	41.25	30k
00100	29.06	32.94	27.13	34.88	25.19	36.81	23.25	38.75	21.31	40.69	19.38	42.63	31k
00101	30	34	28	36	26	38	24	40	22	42	20	44	32k
00110	30.94	35.06	28.88	37.13	26.81	39.19	24.75	41.25	22.69	43.31	20.63	45.38	33k
00111	31.88	36.13	29.75	38.25	27.63	40.38	25.5	42.5	23.38	44.63	21.25	46.75	34k
01000	32.81	37.19	30.63	39.38	28.44	41.56	26.25	43.75	24.06	45.94	21.88	48.13	35k
01001	33.75	38.25	31.5	40.5	29.25	42.75	27	45	24.75	47.25	22.5	49.5	36k
01010	34.69	39.31	32.38	41.63	30.06	43.94	27.75	46.25	25.44	48.56	23.13	50.88	37k
01011	**35.63**	**40.38**	**33.25**	**42.75**	**30.88**	**45.13**	**28.5**	**47.5**	**26.13**	**49.88**	**23.75**	**52.25**	**38k**
01100	36.56	41.44	34.13	43.88	31.69	46.31	29.25	48.75	26.81	51.19	24.38	53.63	39k
01101	37.5	42.5	35	45	32.5	47.5	30	50	27.5	52.5	25	55	40k
01110	38.44	43.56	35.88	46.13	33.31	48.69	30.75	51.25	28.19	53.81	25.63	56.38	41k
01111	39.38	44.63	36.75	47.25	34.13	49.88	31.5	52.5	28.88	55.13	26.25	57.75	42k
10000	40.31	45.69	37.63	48.38	34.94	51.06	32.25	53.75	29.56	56.44	26.88	59.13	43k
10001	41.25	46.75	38.5	49.5	35.75	52.25	33	55	30.25	57.75	27.5	60.5	44k
10010	42.19	47.81	39.38	50.63	36.56	53.44	33.75	56.25	30.94	59.06	28.13	61.88	45k
10011	43.13	48.88	40.25	51.75	37.38	54.63	34.5	57.5	31.63	60.38	28.75	63.25	46k
10100	44.06	49.94	41.13	52.88	38.19	55.81	35.25	58.75	32.31	61.69	29.38	64.63	47k
10101	45	51	42	54	39	57	36	60	33	63	30	66	48k
10110	45.94	52.06	42.88	55.13	39.81	58.19	36.75	61.25	33.69	64.31	30.63	67.38	49k
10111	46.88	53.13	43.75	56.25	40.63	59.38	37.5	62.5	34.38	65.63	31.25	68.75	50k
11000	47.81	54.19	44.63	57.38	41.44	60.56	38.25	63.75	35.06	66.94	31.88	70.13	51k
11001	49.18	54.55	46.88	57.69	44.78	61.22	42.86	65.22	41.1	69.77	39.47	75	52k
11010	49.69	56.31	46.38	59.63	43.06	62.94	39.75	66.25	36.44	69.56	33.13	72.88	53k
11011	50.63	57.38	47.25	60.75	43.88	64.13	40.5	67.5	37.13	70.88	33.75	74.25	54k
11100	51.56	58.44	48.13	61.88	44.69	65.31	41.25	68.75	37.81	72.19	34.38	75.63	55k
11101	52.5	59.5	49	63	45.5	66.5	42	70	38.5	73.5	35	77	56k
11110	53.44	60.56	49.88	64.13	46.31	67.69	42.75	71.25	39.19	74.81	35.63	78.38	57k

Table 9-50. Receiver Demodulation High Frequency (HCFS = 1)

RXDCR	001		010		011		100		101		110		
CFQ	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	(Hz)
00011	375	425	350	450	325	475	300	500	275	525	250	550	400k
01000	421.9	478.1	393.8	506.3	365.6	534.4	337.5	562.5	309.4	590.6	281.3	618.8	450k
01011	450	510	420	540	390	570	360	600	330	630	300	660	**480k**
01011	468.8	531.3	437.5	562.5	406.3	593.8	375	625	343.8	656.3	312.5	687.5	500k

9.11.6.6 CIR Baud Rate Divisor Low Byte Register (BDLR)

The BDLR, an 8-bit **read/write** register, is used to program the CIR Baud Rate clock.

Address: Base Address + 5h (when BR = 1)

Bit	R/W	Default	Description
7-0	R/W	00h	**Baud Rate Divisor Low Byte (BDLR[7:0])** These bits are the low byte of the register used to divide the Baud Rate clock.

9.11.6.7 CIR Baud Rate Divisor High Byte Register (BDHR)

The BDHR, an 8-bit **read/write** register, is used to program the CIR Baud Rate clock.

Address: Base Address + 6h (when BR = 1)

Bit	R/W	Default	Description
7-0	R/W	00h	**Baud Rate Divisor High Byte (BDHR[7:0])** These bits are the high byte of the register used to divide the Baud Rate clock.

Baud rate divisor = 115200 / baud rate
Ex1: 2400 bps → 115200 /2400 = 48 → 48(d) = 0030(h) → BDHR = 00h, BDLR = 30h
Ex2: bit width = 0.565 ms → 1770 bps → 115200 / 1770 = 65(d) = 0041(h) → BDHR = 00(h), BDLR = 41(h)

9.11.6.8 CIR Transmitter Status Register (TSR)

The TSR, an 8-bit **read only** register, provides the Transmitter FIFO status.

Address: Base Address + 5h

Bit	R/W	Default	Description
7-6	R	-	**Reserved**
5-0	R	000000b	**Transmitter FIFO Byte Count (TXFBC[5:0])** Return the number of bytes left in the Transmitter FIFO.

9.11.6.9 CIR Receiver FIFO Status Register (RSR)

The RSR, an 8-bit **read only** register, provides the Receiver FIFO status.

Address: Base Address + 6h

Bit	R/W	Default	Description
7	R	0b	**Receiver FIFO Time-out (RXFTO)** This bit will be set to "1" when a Receiver FIFO time-out condition occurs. The conditions that must exist for a Receiver FIFO time-out condition to occur include the followings: a. At least one byte has been in the Receiver FIFO is not empty for 64 ms more b. The receiver has been inactive (RXACT=0) for over 64 ms or more c. More than 64 ms have elapsed since the last byte was read from the Receiver FIFO by the CPU
6	-	-	**Reserved**
5-0	R	000000b	**Receiver FIFO Byte Count (RXFBC)** Return the number of bytes left in the Receiver FIFO.

9.11.6.10 CIR Interrupt Identification Register (IIR)

The IIR, an 8-bit register, is used to identify the pending interrupts.

Address: Base address + 7h

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2-1	R	00b	**Interrupt Identification** These two bits are used to identify the source of the pending interrupt. **IIR[1:0] Interrupt Source** 00 No interrupt 01 Transmitter Low Data Level Interrupt 10 Receiver Data Stored Interrupt 11 Receiver FIFO Overrun Interrupt
0	R	1b	**Interrupt Pending** This bit will be set to "1" while an interrupt is pending.

9.12 Game Port Interface

The Game Port integrates four timers for two joysticks. The IT8702F allows the Game Port base address to be located anywhere within the host I/O address space from 100h to 0FFFh. Currently, most game software assume that the Game (or Joystick) I/O port is located at 201h.

A write to the Game port base address will trigger four timers. A read from the same address returns four bits that correspond to the outputs from the four timers and four status bits corresponding to the joystick buttons. A button value of 0 indicates that the button is pressed. When the Game port base address is written, the X/Y timer bits go high. Once the Game port base address is written, each timer output remains high for a period of time specified by the current joystick position.

9.12.1 Game Port (Base+0h)

Bit	Symbol	Description
7	JSBB2	Joystick B, Button 2 (pin 20 of Joystick connector)
6	JSBB1	Joystick B, Button 1 (pin 21 of Joystick connector)
5	JSAB2	Joystick A, Button 2 (pin 24 of Joystick connector)
4	JSAB1	Joystick A, Button 1 (pin 25 of Joystick connector)
3	JSBCY	Joystick B, Coordinate Y (pin 22 of Joystick connector)
2	JSBCX	Joystick B, Coordinate X (pin 23 of Joystick connector)
1	JSACY	Joystick A, Coordinate Y (pin 26 of Joystick connector)
0	JSACX	Joystick A, Coordinate X (pin 27 of Joystick connector)

9.13 MIDI Interface

The IT8702F supports the MIDI capability by incorporating hardware to emulate the MPU-401 in the UART mode. It is software compatible with MPU-401 interface, but only supports the UART mode (non-intelligent mode). The UART is used to convert parallel data to the serial data required by MIDI. The serial data format is RS-232 like: 1 start bit, 8 data bits, and 1 stop bit. The serial data rate is fixed at 31.25K baud.

9.13.1 MPU-401 Register Interface

The MPU-401 logical device occupies two consecutive I/O spaces. The device also uses an interrupt. Both the base address and the interrupt level are programmable. MIDI Base+0 is the MIDI Data port, and MIDI Base+ 1 is the Command/Status port.

MIDI Data Port: The MIDI Data Port is used to transmit and receive MIDI data. When in UART mode, all transmit data are transferred through a 16-byte FIFO and receive data through another 16-byte FIFO.

MIDI Data Port, MIDI base+0, Read/Write

Bit	Symbol	Description
7-0	D7-D0	**MIDI data 7-0**

Command/Status Port: The Command register is used to send instructions to the MPU-401. The Status register is used to receive status information from the MPU-401. These two registers occupy the same I/O address.

Command Port, MIDI base+1, Write Only

Bit	Symbol	Description
7-0	C7-C0	**MIDI instruction command code 7-0**

Status Port, MIDI base+1, Read Only

Bit	Symbol	Description
7	RXS	**Receive Buffer Status Flag** 0: Data in Receive Buffer. 1: Receive Buffer empty.
6	TXS	**Transmit Buffer Status Flag** 0: Transmit Buffer not full. 1: Transmit Buffer full.
5-0	-	**Reserved, always report 3Fh**

9.13.2 Operation

In the IT8702F, only two MPU-401 device instructions are available: RESET (code: FFh) and UART mode command (code: 3Fh). After power-up reset, the interface is in the **Intelligent mode** (non-UART mode). In this mode, the operation is defined as follows:

1. All reads of the DATA port, MIDI base+0, return the acknowledged code (FEh). Because only two commands are available, the receive buffer is always placed an acknowledge code in the intelligent mode.
2. All writes to the DATA port, MIDI base+0, are ignored.
3. All writes to the Command port, MIDI base+1, are monitored and acknowledged as follows:
   3Fh: Sets the interface into the UART mode and loads an acknowledged code (FEh) into the receive buffer which generates an interrupt.
   FFh: Sets the interface into the initialization condition.
   Others: Not implemented.

UART Mode:

1. All reads of the DATA port, MIDI base+0, return the next byte in the receive buffer FIFO. The serial data received from the MIDI_IN pin is stored in the receive buffer FIFO. The bit 7 RXS of the Status register is updated to reflect the new receive buffer FIFO state. The receive data available interrupt will be issued only if the FIFO has reached its programmed trigger level. They will be cleared as soon as the FIFO drops below its trigger level. The trigger level is programmable by changing bits 2-1 of the MIDI port Special Configuration register, LDN8_F0h.
2. All writes to the DATA port, MIDI base+0, are placed in the transmit buffer FIFO. Whenever the transmit buffer FIFO is not empty, the data bytes are read from the buffer in turn and sent out from the MIDI_OUT pin. The bit 6 TXS of the Status register is updated to reflect the new transmit buffer FIFO state.
3. All writes to the Command port, MIDI base+1, are monitored and acknowledged as follows:
   FFh: Sets the interface into the initial condition. The interface returns to the intelligent mode.
   Others: No operation.

10. DC Electrical Characteristics

Absolute Maximum Ratings*

Applied Voltage ....-0.5V to 7.0V

Input Voltage (Vi)....................... -0.5V to VCC+0.5V

Output Voltage (Vo)................. -0.5V to VCC + 0.3V

Operation Temperature (Topt) .... 0°C to +70°C

Storage Temperature .... -55°C to +125°C

Power Dissipation 300mW

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (VCC = 5V ± 5%, Ta = 0°C to + 70°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
DO8 Buffer						
V_{OL}	Low Output Voltage	I_{OL} = 8 mA			0.4	V
V_{OH}	High Output Voltage	I_{OH} = -8 mA	2.4			V
DOD8 Buffer						
V_{OL}	Low Output Voltage	I_{OL} = 8 mA			0.4	V
DO16 Buffer						
V_{OL}	Low Output Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	High Output Voltage	I_{OH} = -16 mA	2.4			V
DO24 Buffer						
V_{OL}	Low Output Voltage	I_{OL} = 24 mA			0.4	V
V_{OH}	High Output Voltage	I_{OH} = -16 mA	2.4			V
DIO8 Type Buffer						
V_{OL}	Low Output Voltage	I_{OL} = 8 mA			0.4	V
V_{OH}	High Output Voltage	I_{OH} = -8 mA	2.4			V
V_{IL}	Low Input Voltage				0.8	V
V_{IH}	High Input Voltage		2.2			V
I_{IL}	Low Input Leakage	V_{IN} = 0		10		µA
I_{IH}	High Input Leakage	V_{IN} = VCC			-10	µA
I_{OZ}	3-state Leakage				20	µA

DC Electrical Characteristics (VCC = 5V ± 5%, Ta = 0°C to + 70°C)[cont'd]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
DIOD8 Type Buffer						
V_{OL}	Low Output Voltage	I_{OL} = 8 mA			0.4	V
V_{IL}	Low Input Voltage				0.8	V
V_{IH}	High Input Voltage		2.2			V
I_{IL}	Low Input Leakage	V_{IN} = 0		10		µA
I_{IH}	High Input Leakage	V_{IN} = VCC			-10	µA
I_{OZ}	3-state Leakage				20	µA
DIO16 Type Buffer						
V_{OL}	Low Output Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	High Output Voltage	I_{OH} = -16 mA	2.4			V
V_{IL}	Low Input Voltage				0.8	V
V_{IH}	High Input Voltage		2.2			V
I_{IL}	Low Input Leakage	V_{IN} = 0		10		µA
I_{IH}	High Input Leakage	V_{IN} = VCC			-10	µA
I_{OZ}	3-state Leakage				20	µA
DIOD16 Type Buffer						
V_{OL}	Low Output Voltage	I_{OL} = 16 mA			0.4	V
V_{IL}	Low Input Voltage				0.8	V
V_{IH}	High Input Voltage		2.2			V
I_{IL}	Low Input Leakage	V_{IN} = 0		10		µA
I_{IH}	High Input Leakage	V_{IN} = VCC			-10	µA
I_{OZ}	3-state Leakage				20	µA
DIO24 Type Buffer						
V_{OL}	Low Output Voltage	I_{OL} = 24 mA			0.4	V
V_{OH}	High Output Voltage	I_{OH} = -16 mA	2.4			V
V_{IL}	Low Input Voltage				0.8	V
V_{IH}	High Input Voltage		2.2			V
I_{IL}	Low Input Leakage	V_{IN} = 0		10		µA
I_{IH}	High Input Leakage	V_{IN} = VCC			-10	µA
I_{OZ}	3-state Leakage				20	µA
DI Type Buffer						
V_{IL}	Low Input Voltage				0.8	V
V_{IH}	High Input Voltage		2.2			V
I_{IL}	Low Input Leakage	V_{IN} = 0		10		µA
I_{IH}	High Input Leakage	V_{IN} = VCC			-10	µA

11. AC Characteristics (VCC = 5V ± 5%, Ta = 0°C to + 70°C)

11.1 Clock Input Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Clock High Pulse Width when CLKIN=48 MHz[1]	8			nsec
t_2	Clock Low Pulse Width when CLKIN=48 MHz [1]	8			nsec
t_3	Clock Period when CLKIN=48 MHz [1]	20	21	22	nsec
t_4	Clock High Pulse Width when CLKIN=24 MHz [1]	18			nsec
t_5	Clock Low Pulse Width when CLKIN=24 MHz [1]	18			nsec
t_6	Clock Period when CLKIN=24 MHz [1]	40	42	44	nsec

Not tested. Guaranteed by design.

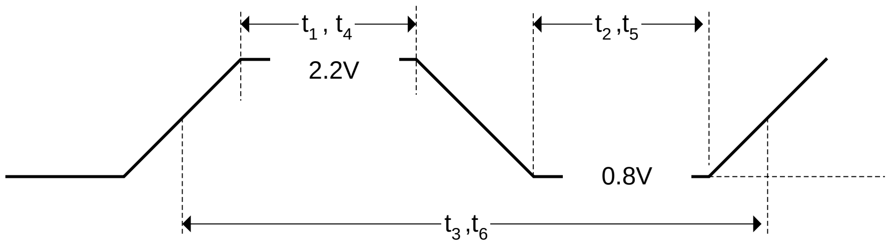


Figure 11-1. Clock Input Timings

11.2 LCLK (PCICLK) and LRESET Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	LCLK Cycle Time	28			nsec
t_2	LCLK High Time	11			nsec
t_3	LCLK Low Time	11			nsec
t_4	LRESET# Low Pulse Width	1.5			µsec

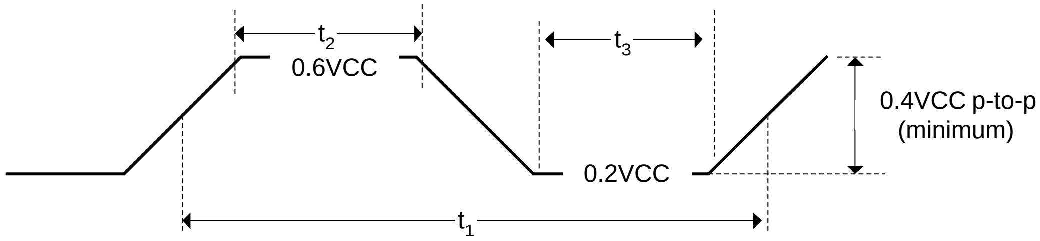


Figure 11-2. LCLK (PCICLK) and LRESET Timings

11.3 LPC and SERIRQ Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Float to Active Delay	3			nsec
t_2	Output Valid Delay			12	nsec
t_3	Active to Float Delay			6	nsec
t_4	Input Setup Time	9			nsec
t_5	Input Hold Time	3			nsec

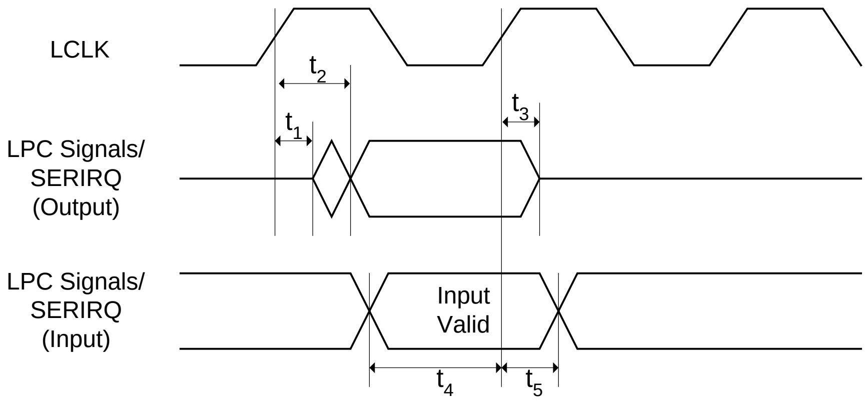

LCLK
t2
t1
t3
LPC Signals/
SERIRQ
(Output)
LPC Signals/
SERIRQ
(Input)
Input
Valid
t4
t5

Figure 11-3. LPC and SERIRQ Timings

11.4 Serial Port, ASKIR, SIR and Consumer Remote Control Timings

Symbol	Parameter	Conditions	Min.	Max.	Unit
t_1	Single Bit Time in Serial Port and ASKIR	Transmitter	t_{BTN} – 25 Note1	t_{BTN} + 25	nsec
		Receiver	t_{BTN} – 2%	t_{BTN} + 2%	nsec
t_2	Modulation Signal Pulse Width in ASKIR	Transmitter	950	1050	nsec
		Receiver	500		nsec
t_3	Modulation Signal Period in ASKIR	Transmitter	1975	2025	nsec
		Receiver	2000X(23/24)	2000X(25/24)	nsec
t_4	SIR Signal Pulse Width	Transmitter, Variable	(3/16) x t_{BTN} – 25	(3/16) x t_{BTN} + 25	nsec
		Transmitter, Fixed	1.48	1.78	µsec
		Receiver	1		µsec

Note 1: t_{BTN} is the nominal bit time in Serial Port, ASKIR, and SIR. It is determined by the setting on the Baud Rate Divisor registers.

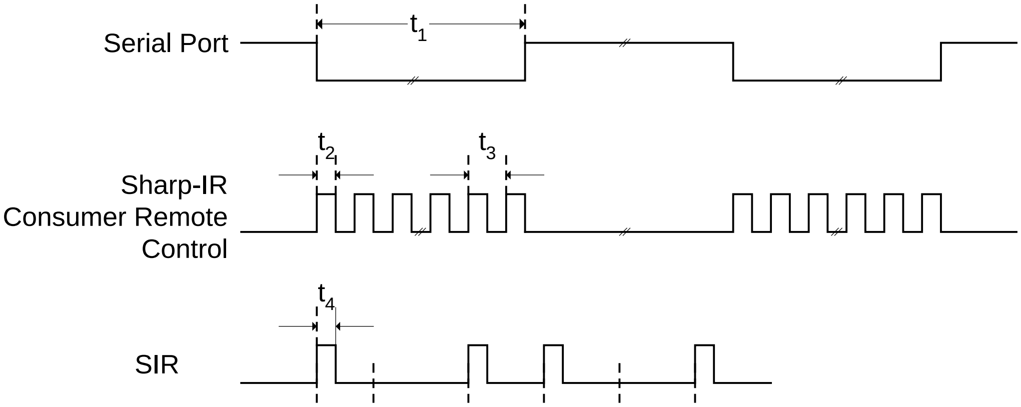

Serial Port
t_1
Sharp-IR Consumer Remote Control
t_2
t_3
SIR
t_4

Figure 11-4. Serial Port, ASKIR, SIR and Consumer Remote Control Timings

11.5 Modem Control Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Float to active delay			40	nsec

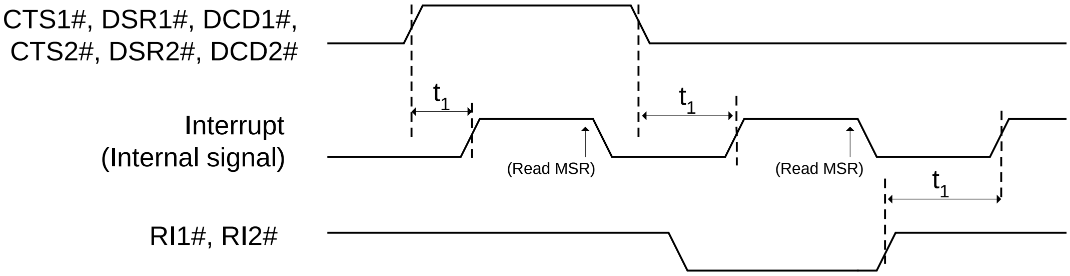

CTS1#, DSR1#, DCD1#, CTS2#, DSR2#, DCD2#
Interrupt (Internal signal)
t_1
(Read MSR)
t_1
(Read MSR)
t_1
RI1#, RI2#

Figure 11-5. Modem Control Timings

11.6 Floppy Disk Drive Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	DIR# active to STEP# low		4X t_{mclk} Note1		nsec
t_2	STEP# active time (low)		24X t_{mclk}		nsec
t_3	DIR# hold time after STEP#		t_{SRT} Note2		msec
t_4	STEP# cycle time		t_{SRT}		msec
t_5	INDEX# low pulse width	2X t_{mclk}			nsec
t_6	RDATA# low pulse width	40			nsec
t_7	WDATA# low pulse width		1X t_{mclk}		nsec

Note 1: t_{mclk} is the cycle of main clock for the microcontroller of FDC. t_{mclk} =8M/ 4M/ 2.4M/ 2M for 1M/ 500K/ 300K/ 250 Kbps transfer rates respectively.

Note 2: t_{SRT} is the cycle of the Step Rate Time. Please refer to the functional description of the SPECIFY command of the FDC.

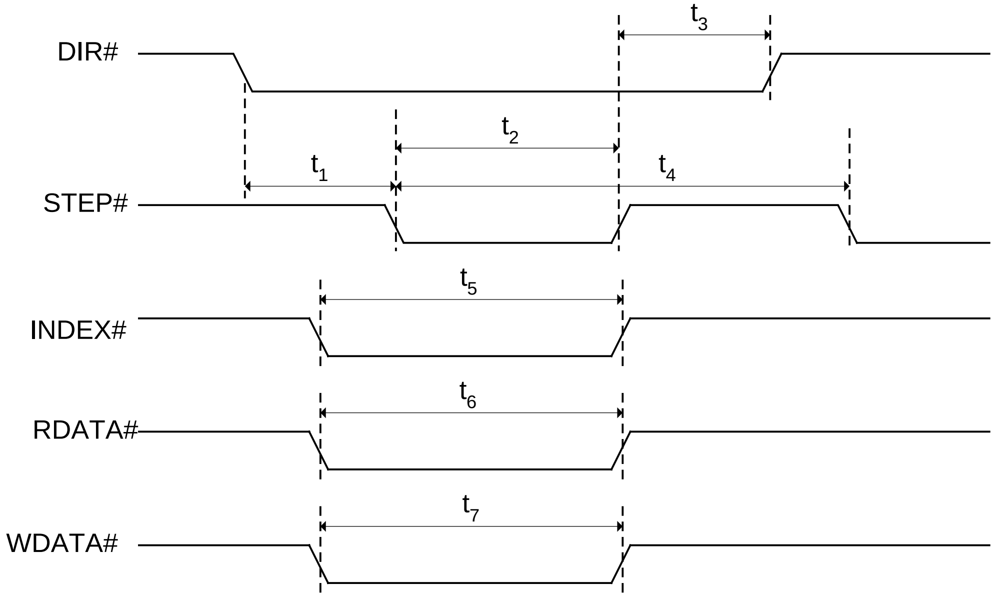


Figure 11-6. Floppy Disk Drive Timings

11.7 EPP Address or Data Write Cycle Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	WRITE# asserted to PD[7:0] valid			50	nsec
t_2	ASTB# or DSTB# asserted to WAIT# de-asserted	0		10	nsec
t_3	WAIT# de-asserted to ASTB# or DSTB# de-asserted	65		135	nsec
t_4	ASTB# or DSTB# de-asserted to WAIT# asserted	0			nsec
t_5	WAIT# asserted to WRITE# de-asserted	65			nsec
t_6	PD[7:0] invalid after WRITE# de-asserted	0			nsec

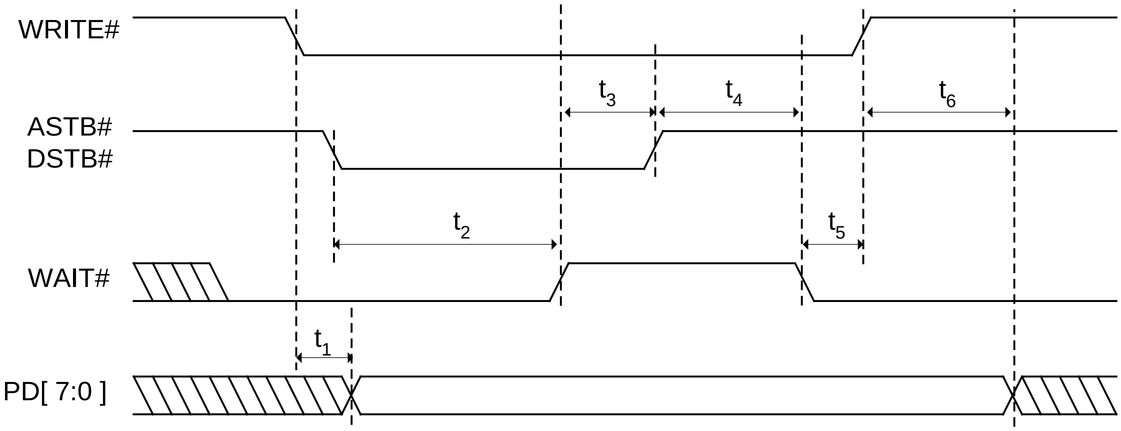


Figure 11-7. EPP Address or Data Write Cycle Timings

11.8 EPP Address or Data Read Cycle Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	ASTB# or DSTB# asserted to WAIT# de-asserted			10	nsec
t_2	ASTB# or DSTB# asserted to PD[7:0] Hi-Z	0			nsec
t_3	PD[7:0] valid to WAIT# de-asserted	0			nsec
t_4	WAIT# de-asserted to ASTB# or DSTB# de-asserted	65		135	nsec
t_5	ASTB# or DSTB# de-asserted to WAIT# asserted	0			nsec
t_6	PD[7:0] invalid after ASTB# or DSTB# de-asserted	20			nsec

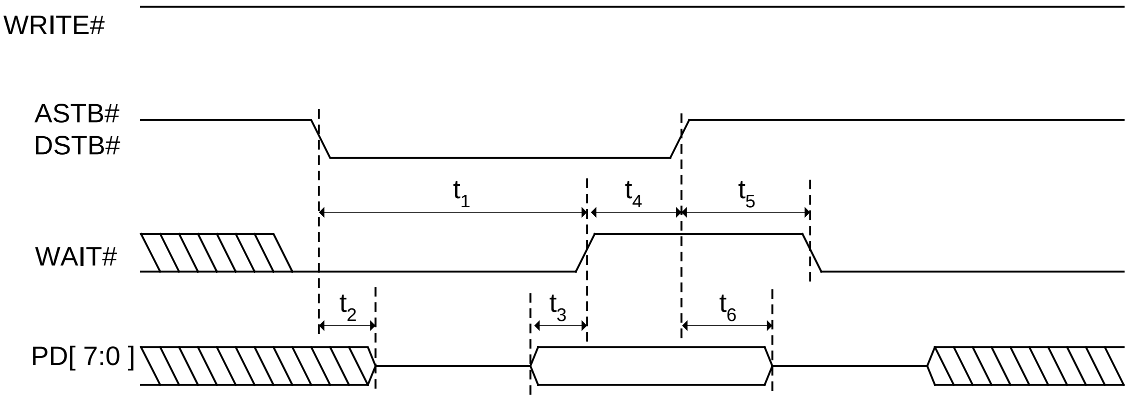


Figure 11-8. EPP Address or Data Read Cycle Timings

11.9 ECP Parallel Port Forward Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	PD[7:0] and nAutoFd valid to nStrobe asserted			50	nsec
t_2	nStrobe asserted to Busy asserted	0			nsec
t_3	Busy asserted to nStrobe de-asserted	70		170	nsec
t_4	nStrobe de-asserted to Busy de-asserted	0			nsec
t_5	Busy de-asserted to PD[7:0] and nAutoFd changed	80		180	nsec
t_6	Busy de-asserted to nStrobe asserted	70		170	nsec

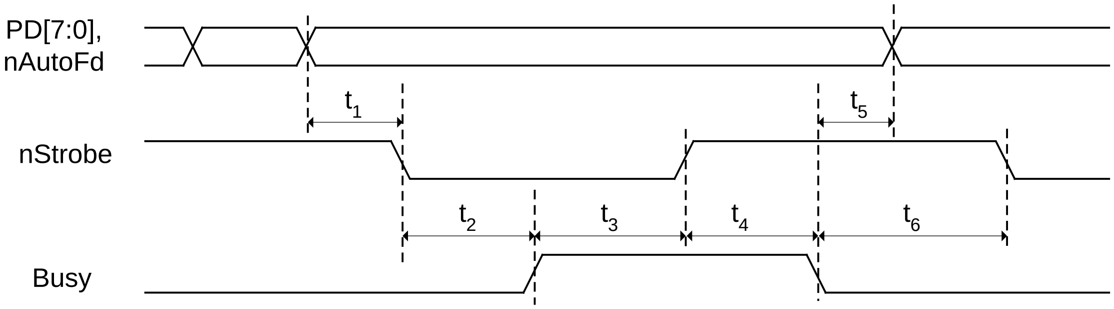


Figure 11-9. ECP Parallel Port Forward Timings

11.10 ECP Parallel Port Backward Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	PD[7:0] valid to nAck asserted	0			nsec
t_2	nAck asserted to nAutoFd asserted	70		170	nsec
t_3	nAutoFd asserted to nAck de-asserted	0			nsec
t_4	nAck de-asserted to nAutoFd de-asserted	70		170	nsec
t_5	nAutoFd de-asserted to PD[7:0] changed	0			nsec
t_6	nAutoFd de-asserted to nAck asserted	0			nsec

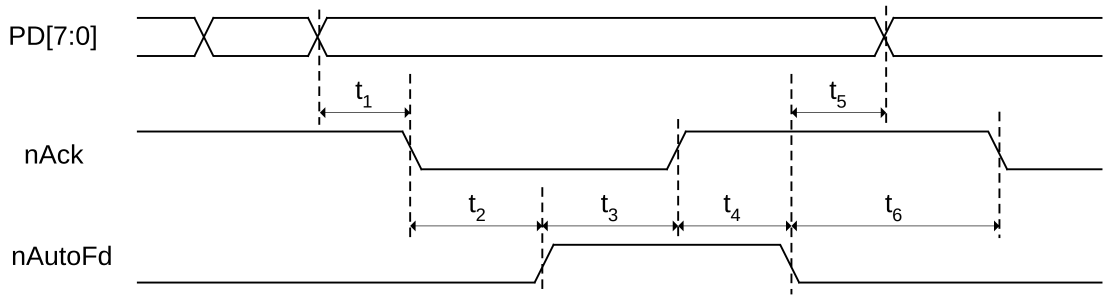

PD[7:0]
t1
t5
nAck
t2
t3
t4
t6
nAutoFd

Figure 11-10. ECP Parallel Port Backward Timings

11.11 RSMRST#, PWROK1/2, and ACPI Power Control Signals Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	RSMRST# de-actives delay from VCCH5V=4V	13	16	19	msec
t_2	PWROK1/2 active delay from VCC5V=4V	350	400	450	msec

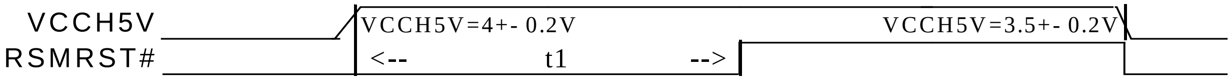

VCCH5V
RSMRST#
VCCH5V=4+- 0.2V
VCCH5V=3.5+- 0.2V
<--
t1
-->

Figure 11-11. RSMRST# Timings

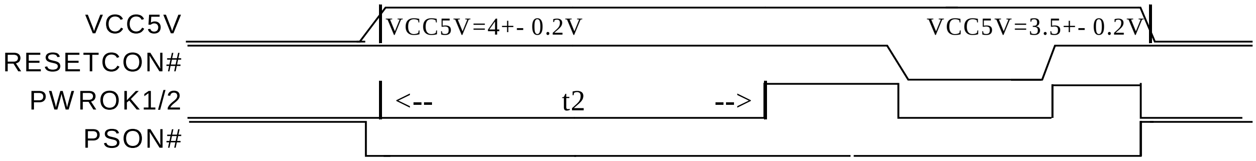

VCC5V
RESETCON#
PWROK1/2
PSON#
VCC5V=4+- 0.2V
VCC5V=3.5+- 0.2V
<--
t2
-->

Figure 11-12. PWROK1/2 Timings

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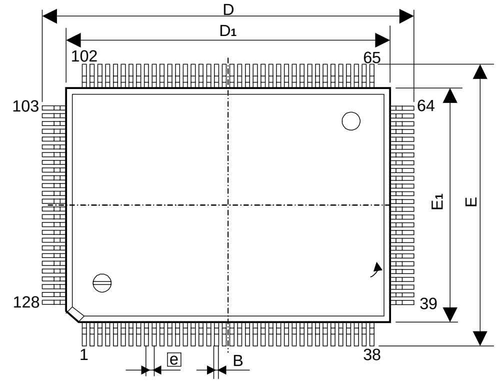
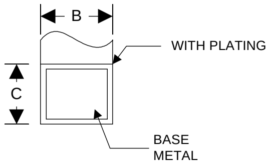
12. Package Information

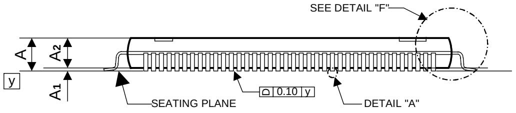
QFP 128L Outline Dimensions

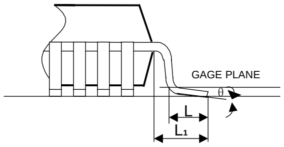
unit: inches/mm


D
D₁
102
65
103
64
E₁
E
128
39
1
38
e
B


B
WITH PLATING
C
BASE
METAL

DETAIL "A"


SEE DETAIL "F"
A
A₂
y
A₁
SEATING PLANE
0.10 y
DETAIL "A"


GAGE PLANE
θ
L
L₁

DETAIL "F"

Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.134	-	-	3.40
A**1**	0.010	-	-	0.25	-	-
A**2**	0.107	0.112	0.117	2.73	2.85	2.97
B	0.007	0.009	0.011	0.17	0.22	0.27
C	0.004	-	0.008	0.09	-	0.20
D	0.906	0.913	0.921	23.00	23.20	23.40
D_1	0.783	0.787	0.791	19.90	20.00	20.10
E	0.669	0.677	0.685	17.00	17.20	17.40
E_1	0.547	0.551	0.555	13.90	14.00	14.10
$\boxed{e}$	0.020 BSC			0.5 BSC		
L	0.029	0.035	0.041	0.73	0.88	1.03
L_1	0.063 BSC			1.60 BSC		
y	-	-	0.004	-	-	0.10
θ	0°	-	7°	0°	-	7°

Notes:

1. Dimensions D_1 and E_1 do not include mold protrusion, but mold mismatch is included.
2. Dimension B does not include dambar protrusion.
3. Controlling dimension: millimeter.

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13. Ordering Information

Part No.	**Package**
IT8702F	128 QFP