Intel® 855GM/855GME Chipset Graphics and Memory Controller Hub (GMCH)

Specification Update

October 2003

Notice: The Intel® 855GM/855GME chipset may contain design defects or errors known as errata, which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Order Number:253572-002

Contents

Revision History

Rev.	Draft/Changes	Date
-001	Initial Release	July 2003
-002	Updates include: • Added the Intel 855GME chipset	October 2003

Preface

This document is an update to the specifications contained in the *Intel® 855GM/855GME Chipset GMCH Datasheet*. It is intended for hardware system manufacturers. It contains Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the Intel 855GM/855GME chipset GMCH behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Identification via Programming Interface

The Intel 855GM/855GME chipset GMCH may be identified by the following register contents.

Component	Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
855GM/855GME	A2	8086h	3580h (Device #0)	02h

NOTES:

1. The Vendor ID corresponds to bits 15-0 of the Vendor ID Register located at offset 00-01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15-0 of the Device ID Register located at offset 02-03h in the PCI function 0 configuration space.
3. The Revision Number corresponds to bits 7-0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Component Marking Information

The Intel 855GM/855GME chipset GMCH may be identified by the following component markings.

Component	Stepping	S-Spec	Top Marking	Notes
855GM	A2	SL6WW	RG82855GM	Production 82855GM GMCH
855GME	A2	SL72L	RG82855GME	Production 82855GME GMCH

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes that apply to the listed Intel® 855GM/855GME chipset GMCH steppings. Intel intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This item is either new or modified from the previous version of the document.

Note: Each Specification Update item is prefaced with a capital letter to distinguish the product. The key below details the letters that are used in this Specification Update.

A = Intel® 82855GM Graphics and Memory Controller Hub (GMCH)

B = Intel® 82855GME Graphics Memory Controller Hub (GMCH)

Errata

NO.	Stepping	PLANS	ERRATA
	A2		
A1, B1	x	No Fix	VGA Panning Test Issue
A2, B2	X	No Fix	VGA Timing issue
A3, B3	X	No Fix	Intermittent System hangs during power cycle test.
A4, B4	x	No Fix	Display may flicker when integrated graphics and ECC support are enabled
B5	x	No Fix	AGP PCI Write to system memory may be corrupted.
B6	x	No Fix	AGP write failure when ECC memory is enabled

Specification Changes

NO.	Stepping	PLANS	SPECIFICATION CHANGES
	A2		
			There are no Specification Changes.

Specification Clarifications

NO.	Stepping	PLANS	SPECIFICATION CLARIFICATIONS
	A2		
			There are no Specification Clarifications.

Documentation Changes

NO.	Stepping	PLANS	DOCUMENTATION CHANGES
	A2		
			There are no Documentation changes

Errata

1. A1,B1 - VGA Panning

Problem: VGA text mode diagnostic and stress test applications that use pixel panning can experience temporary visual anomalies under certain memory configurations. This issue was seen in two test configurations.

1. Test applications using a single VGA font table with a 32-kB font buffer range could fail. The failure can occur using 64-MB technology products that use 2 kB and 4 kB page sizes. This failure was seen in a diagnostic utility.

2. Test applications using multiple VGA font tables could fail if the first two fonts are from different tables. This failing condition can occur in any memory configuration. This failure was seen in a stress test utility.

Implication: Entire scan lines will appear to flicker in some VGA diagnostic and stress test applications. However, there are no known customer sightings of this erratum. No known end user applications fail for this erratum.

Workaround: No workaround exists.

Status: There are no plans to fix this erratum in silicon.

2. A2,B2 - VGA Timings

Problem: Some VGA applications, running in 40-column modes that use a non-black border color may experience color/visual issues on systems configured with certain monitors.

Implication: 40-column VGA modes may experience visual color anomalies on some CRT monitors. This was observed using VGA focused Intel test software. With certain monitors, colors in active areas may change as the border color changes. As observed while using the test software, visual color anomalies can range from a slight color change difference to a blank screen. Based on the lack of customer or end user reported issues related to this erratum, the number of VGA applications that run in 40-column modes and also use non-black border colors is low. Based on Intel's validation and compatibility testing, the number of CRT monitors that exhibit this color anomaly is also low.

Workaround: No workaround exists.

Status: There are no plans to fix this erratum in silicon.

3. A3,B3 - Intermittent System hangs during BIOS memory testing when Power Cycle testing

Problem: Systems may intermittently hang during BIOS memory testing as a result of the internal RCOMP state machine colliding with BIOS induced RCOMP cycle.

Implication: System hang may occur during boot-up or resume from S3. No other failures have been identified or reported. Issues are resolved with a BIOS workaround.

Workaround: Please refer to Intel 855GM Memory BIOS Specification and BIOS Spec Update for details.

Status: There are no plans to fix this erratum in silicon.

4. A4,B4 - Display may flicker when integrated graphics and ECC support are enabled

Problem: Display flicker and flashing may occur when integrated graphics and ECC support are enabled under certain graphics resolution modes.

Implication: A potentially undesirable amount of display flicker may occur.

Workaround: No workaround available.

Status: There are no plans to fix this erratum in silicon.

5. B5 - AGP PCI Write to system memory may be corrupted

Problem: Display corruption or a system hang may result if an upstream AGP FRAME#-based PCI write crosses a 32-byte aligned boundary. Note that upstream AGP FRAME#-based PCI writes which cross a 32-byte aligned boundary are expected to be rare.

Implication: The issue may cause display corruption or a system hang. With the workaround implemented, Intel has done extensive validation and expects less than 3% impact on system performance.

Workaround: A BIOS workaround is available which disconnects upstream AGP FRAME#-based PCI writes to system memory at 32-byte aligned boundaries. Please refer to your Intel representative for BIOS workaround details.

Status: There are no plans to fix this erratum in silicon.

6. B6 - AGP write failure when ECC memory is enabled.

Problem: Memory corruption or system hang may result if an AGP semantic write cycle targets a cache line in the AGP aperture window at the same time a PCI semantic write cycle from another PCI device is targeting the same cache line if ECC memory is enabled.

Implication: If ECC memory is enabled, data corruption or system hang may result.

Workaround: No workaround available. ECC memory will not be supported when using an AGP graphics device.

Status: There are no plans to fix this erratum in silicon

Specification Changes

There are no Specification Changes in this Specification Update.

Specification Clarifications

There are no Specification Clarifications in this Specification Update.

Documentation Changes

There are no Documenation Changes in this Specification Update.