Intel® 82443GX AGPset Specification Update

Specification Update

April, 2000

Notice: The Intel® 82443GX AGPset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Order Number: 290643-003

Contents

Revision History

Rev.	Draft/Changes	Date
-001	Initial Release	October 1998
-002	Added Specification Change 5, Modify Memory Buffer Strength Terminology in Register 69-6Eh.	November 1998
-003	Added Specification Change 6, Increase to the Supported Memory Configurations. Added Documentation Change 2, Correction to SERR# Pin Type. Added Specification Clarification 5, Multi-bit Memory Error	April 2000

Preface

This document is an update to the specifications contained in the Intel® 82443GX Intel® 440GX AGPset: 82443GX Host Bridge/Controller Datasheet, Rev -001. It is intended for hardware system manufacturers. It contains Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the Intel 82443GX AGPset, behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Identification via Programming Interface

The Intel 82443GX AGPset may be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
A-0	8086h	71A9/71A2h	00h

NOTES:
1. The Vendor ID corresponds to bits 15-0 of the Vendor ID Register located at offset 00-01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15-0 of the Device ID Register located at offset 02-03h in the PCI function 0 configuration space.
3. The Revision Number correspond to bits 7-0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Component Marking Information

The Intel® 82443GX AGPset may be identified by the following component markings:

Stepping	S-Spec	Top Marking	Notes
A-0		FW82443GX Q633ES	Engineering Sample, FM Test
A-0		FW82443GX Q634ES	Engineering Sample, T03 Test
A-0	SL2TF	FW82443GX SL2TF	443GX A-0 Production ASSY
A-0	SL2VJ	FW82443GX SL2VJ	443GX A-0 Production ASSY

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes which apply to the listed Intel® 82443GX AGPset steppings. Intel intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This item is either new or modified from the previous version of the document.

NO.	A0	PLANS	SPECIFICATION CHANGES
1	X	Doc	Modify Abort Disable Test Mode Configuration Bits in Register F4h [30:29]
2	X	Doc	Modify MD[63:0] [Control2] and MECC [7:0] [Control 1] bits in Register CA-CCh [20,17]
3	X	Doc	Non-Supported SDRAM Memory Configuration
4	X	Doc	Modify Input/Output Data Mask A/B-Side Data Buffer Strength Programming in Register CA-CCh [6:2]
5	X	Doc	Modify Memory Buffer Strength Terminology in Register 69-6Eh
6	X	Doc	Incease to the Supported Memory Configurations

NO.	A0	PLANS	ERRATA
1	X	No Fix	SDRAM Suspend Refresh

NO.	A0	PLANS	SPECIFICATION CLARIFICATIONS
1	X	Doc	CKE Function with Registered DMMs
2	X	Doc	Memory Initialization with ECC Enabled
3	X	Doc	Normal Refresh Enable
4	X	Doc	DCLKO State During POS/STR
5	X	Doc	Mulit-bit Memory Error Clarification

NO.	A0	PLANS	DOCUMENTATION CHANGES
1	X	Doc	Correction to the 82443GX Alphabetical BGA Pin List (Table 5-1)
2	X	Doc	Correction to SERR# Pin Type

Specification Changes

1. Modify Abort Disable Test Mode Configuration Bits in Register F4h [30:29]

Intel Reserved Register bits at offset F4h, bits 29 and 30 should be set to 1 for normal operation.

2. Modify MD[63:0] [Control2] and MECC [7:0] [Control 1] bits in Register CA-CCh [20,17]

Reserved programming of bits 20 and 17 of register CA-CCh are valid buffer programming options. These two bits can be programming to 0 for 100MHz A and 1 for 100MHz B, as shown below:

Bits	Description
20	**MD [63:0] [Control 2]** This bit enables 100Mhz buffers for **MD [63:0] [Control 2].** (Refer to the corresponding MBSC register for programming details). 0 100MHz A 1 100MHz B

Bits	Description
17	**MECC [7:0] [Control 1]** This bit enables either 100Mhz buffers for MECC [7:0] [Control 1] (Refer to the corresponding MBSC register for programming details). 0 100MHz A 1 100MHz B

3. Non-Supported SDRAM Memory Configuration

Any memory configuration using SDRAM memory of the type 128Mbit 32Mx4 with 13 rows and 10 columns is not supported by the Intel® 82443GX AGPset. This support has been removed because these SDRAM (13x10 128Mbit) devices are not planned for production by memory vendors.

4. Modify Input/Output Data Mask A/B-Side Data Buffer Strength Programming in Register CA-CCh [6:2]

Characterization of the Input/Output Data Mask A/B-Side Data buffers has shown that the actual buffers are stronger than the simulated buffer strengths. As a result, new buffer strength settings are recommended in order to improve system noise margin, as shown below:

Bits	Description
6	DQMA5. This bit enables 100MHz buffers for DQMA5. 0 100MHz A 1 100MHz B
5	DQMA1. This bit enables 100MHz buffers for DQMA1. 0 100MHz A 1 100MHz B
4	DQMB5. This bit enables 100MHz buffers for DQMB5. 0 100MHz A 1 100MHz B
3	DQMB1. This bit enables 100MHz buffers for DQMB1. 0 100MHz A 1 100MHz B
2	DQMA[7:6,4:2,0]. This bit enables 100MHz buffers for DQMA[7:6], DQMA[4:2], and DQMA[0]. 0 100MHz A 1 100MHz B

5. Modify Memory Buffer Strength Terminology in Register 69-6Eh.

Previous changes to Register CA-CCh (for example, Specification Changes 2 and 4 above) require similar changes to Register 69-6Eh. As a result, Register 69-6Eh bit changes are shown below. These bit changes match the “100MHz A” and “100MHz B” terminology found in Register CA-CCh.

35:34	MD [63:0] Buffer Strength Control 2 4 DIMM FET Configuration: This field sets the buffer strength for the MD[63:0] path that is connected to DIMM2 and DIMM3. The buffer strength is programmable based upon the SDRAM load in detected in DIMM slots 2&3. This path is enabled when FENA is asserted (High) by the Intel® 82443GX AGPset. 4 DIMM non-FET Configuration: This field should be programmed to the same value as MD[63:0] Buffer Strength Control 1. This buffer strength is programmable based upon the SDRAM load detected in all DIMM connectors.

	Value Buffer Strength 00 1X A and B 01 Reserved Invalid setting 10 2X A and B 11 3X B only
33:32	MD [63:0] Buffer Strength Control 1 4 DIMM FET Configuration: This field sets the buffer strength for the MD[63:0] path that is connected to DIMM0 and DIMM1. The buffer strength is programmable based upon the SDRAM load in detected in DIMM slots 0&1. This path is enabled when FENA is de-asserted (Low) by the Intel® 82443GX AGPset. 4 DIMM non-FET Configurations: The buffer strength is programmable based upon the SDRAM load detected in all DIMM connectors. Value Buffer Strength 00 1X A and B 01 Reserved Invalid setting 10 2X A and B 11 3X B only
31:30	MECC [7:0] Buffer Strength Control 2 4 DIMM FET Configuration: This field sets the buffer strength for the MECC[7:0] path that is connected to DIMM2 and DIMM3 The buffer strength is programmable based upon the SDRAM ECC load detected in DIMM slots 2&3. This path is enabled when FENA is asserted (High) by the Intel® 82443GX AGPset. 4 DIMM non-FET Configurations: This field should be programmed to the same value as MECC[7:0] Buffer Strength Control 1. This buffer strength is programmable based upon the SDRAM load detected in all DIMM connectors. Value Buffer Strength 00 1X A and B 01 Reserved Invalid setting 10 2X A and B 11 3X B only
29:28	MECC [7:0] Buffer Strength Control 1 4 DIMM FET Configuration: This field sets the buffer strength for the MECC[7:0] path that is connected to DIMM0 and DIMM1. The buffer strength is programmable based upon the SDRAM ECC load detected in DIMM slots 0&1. This path is enabled when FENA is de-asserted (Low) by the Intel® 82443GX AGPset. 4 DIMM non-FET Configuration: The buffer strength is programmable based upon the SDRAM ECC load detected in all DIMM slots.

	Value Buffer Strength 00 1X A and B 01 Reserved Invalid setting 10 2X A and B 11 3X B only
13:12	**DQMA5 Buffer Strength** This field sets the buffer strength for the DQMA5 pins. Value Buffer Strength 00 1X A and B 01 Reserved Invalid setting 10 2X A and B 11 3X A only
11:10	**DQMA1 Buffer Strength** This field sets the buffer strength for the DQMA1 pin. Value Buffer Strength 00 1X A and B 01 Reserved Invalid setting 10 2X A and B 11 3X A only
9:8	**DQMB5 Buffer Strength** This field sets the buffer strength for the DQMB5 pin. Value Buffer Strength 00 1X A and B 01 Reserved Invalid setting 10 2X A and B 11 3X A only
7:6	**DQMB1 Buffer Strength** This field sets the buffer strength for the DQMB1 pin. Value Buffer Strength 00 1X A and B 01 Reserved Invalid setting 10 2X A and B 11 3X A only

5:4	**DQMA[7:6,4:2,0] Buffer Strength** This field sets the buffer strength for the DQMA[7:6], DQMA[4:2], and the DQMA[0] pins. Value Buffer Strength 00 1X A and B 01 Reserved Invalid setting 10 2X A and B 11 3X A and B

6. Increase to the Supported Memory Configurations

Reference the Intel® 440GX AGPset: 82443GX Host Bridge/Controller Datasheet, Order Number 290638-001, pages 4-17 and 4-18. 128Mbit technology 16MX8 components organized as 32MX72 unbuffered DIMMs were tested in the Intel® 440GX AGPset validation platform and passed all tests. As a result, page 4-17 showing the "Option" and "SDRAM Component Type" for Option 4 is changed as follows:

OPTION SDRAM COMPONENT TYPE

4 (128 MB) 16MX16, 16MX8, or 16MX4

Also, Table 4-9, "Supported Memory Configurations", Technology 128Mb, 4 bank section on page 4-18 is changed as follows:

DRAM Attributes				DRAM DIMM		DRAM Addressing	DRAM Device			DRAM Size
Type	Tech	Depth	Width	SS x64	DS x64		Rows	Cols	Banks	Min (1 row)
SDRAM	16Mb	2M	8	2M	4M	Asymmetric	11	9	2	16 MB
		2M	8	2M	4M	Asymmetric	12	8	2	16 MB
		4M	4	4M	8M	Asymmetric	11	10	2	32 MB
		4M	4	4M	8M	Asymmetric	13	8	2	32 MB
SDRAM	64Mb 4 bank	4M	16	4M	8M	Asymmetric	12	8	4	32 MB
		8M	8	8M	16M	Asymmetric	12	9	4	64 MB
		16M	4	16M	32M	Asymmetric	12	10	4	128 MB
SDRAM	128Mb 4 bank	16M	8	16M	32M	Asymmetric	12	10	4	128 MB
		32M	4	32M	64M	Asymmetric	12	11	4	256 MB
SDRAM	256Mb2 4 bank	16M	16	16M	32M	Asymmetric	13	9	4	128MB
		32M	8	32M	64M	Asymmetric	13	10	4	256MB
		64M	4	64M	128M	Asymmetric	13	11	4	512MB

Errata

1. SDRAM Suspend Refresh

Problem: This erratum may occur in Intel® 440GX APGset chipset platforms that implement suspend or Stop Clock (C3) states. Platforms that are affected are 4 DIMM desktop platforms using GCKE.

This platform requires the Intel® 440GX APGset memory controller to stop the normal refresh and place the SDRAM in a self-refresh mode before the system transitions to one of these states. If the self-refresh trigger (SUSTAT1# signal asserted) occurs at the same time as an internally generated normal refresh request, the 440GX generates an incorrect GCKE and CSAx#CSBx# signal sequence to the SDRAM. The SDRAM is not placed in self-refresh mode and memory contents may be lost.

3 DIMM desktop platforms are not affected. 4 DIMM desktop platforms that do not use GCKE are also not affected.

Implication: The observed effect of the erratum is a system hang, although data loss or corruption is theoretically possible.

Workaround: APM BIOS workaround:

POS, POSCCL, POSCL, STR and C3 states

The workaround disables normal refresh prior to entering these states and before the Intel® 82443GX AGPset automatically generates the SDRAM self-refresh command. BIOS will re-enable normal refresh on exit from these states.

ACPI BIOS workaround (TBD):

Status: Implement BIOS workaround.

Specification Clarifications

1. CKE Function with Registered DIMMs

The stacking technology used for registered DIMMs prohibits the use of the CKE function. For registered DIMMs, components are stacked on top of one another. The stacked components are **physically** in the same row, but **logically** in separate rows. The stacked components connect all pins together, except for the CS# pin, in order to address components in different rows. Since the CKE pins for the components are connected together, and the components are **logically** in different rows, the CKE function is not supported.

2. Memory Initialization with ECC Enabled

For 82440GX ACPset systems using ECC memory, the memory must be initialized with ECC enabled (NBXCFG bits 31 through 24 and bits 7 and 8). Any ECC errors received during initialization should be ignored.

3. Normal Refresh Enable

When the user performs a soft reset, the PIIX4 will drive SUS_STAT1# to the Intel® 82443GX AGPset. This will force the Intel® 82443GX AGPset to switch to a suspend refresh state. When the BIOS attempts to execute cycles to DRAM, the Intel® 82443GX AGPset will not accept these cycles because it believes that it is in a suspend state

After coming out of reset the software must set the Normal refresh enable bit (bit 4, Power management control register Offset 7Ah) in the Intel® 82443GX AGPset before doing an access to memory.

4. DCLKO State During POS/STR

The state of DCLKO during POS/STR may be high or low. As a result, designs implementing POS/STR should move the CKBF component to the same VCC3 plane as the Intel® 82443GX AGPset component.

5. Multi-bit Memory Error Clarification

When a Intel® 440GX AGPset platform is configured for ECC support, if a multi-bit uncorrectable memory error is detected during a memory read by a system device, an SERR, SCI, or SMI will be generated. This typically results in an NMI, however bad data may still reach the intended target before the NMI can be generated or before NMI interrupt handler can service the problem. This may result in bad data being returned to the target and may be permanently stored, resulting in system data corruption. This chipset was not architected or designed to ensure that targets are protected from this corrupted data in these situations.

Documentation Changes

1. Correction to the 82443GX Alphabetical BGA Pin List (Table 5-1)

Table 5-1 has pin MAB14 incorrectly referenced as AE22. The correct pin location on the Intel® 82443GX AGPset is AE23.

2. Correction to SERR# Pin Type

Table 2-4, page 2-5, of the Intel® 440GX AGPset: 82443GX Host Bridge/Controller Datasheet, Order Number 290638-001, shows the SERR# pin type as I/O. This is not correct. The SERR# pin type is OD.

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