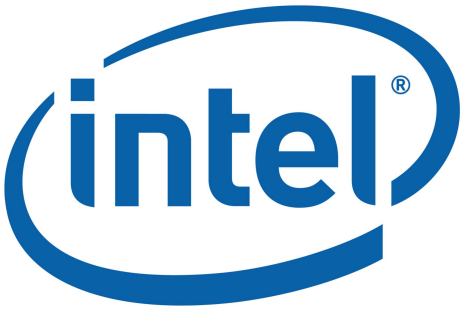


Intel® Ethernet Controller I211

Specification Update

Ethernet Networking Division (ND)

January 2020

Revision 1.8
333015-004

Revision History

Revision	Date	Comments
1.8	January 17, 2020	**Specification Clarifications added or updated:** • 6. PCIe Separate Reference Clock with Independent Spread (SRIS) Support (Added)
1.7	July 15, 2016	**Errata added or updated:** • 13. PCIe Throughput with Few Credits (Added)
1.6	June 15, 2016	**Errata added or updated:** • 12. PCIe Advanced Error Reporting: First Error Pointer (Added)
1.5	August 24, 2015	**Errata added or updated:** • 11. Certain Malformed IPv6 Extension Headers are Not Processed Correctly by the Device (Added)
1.4	February 10, 2015	**Specification Changes added or updated:** • 3. Revision ID of A2 Stepping (Added) **Errata added or updated:** • 10. Slow System Clock (Updated)
1.3	December 23, 2013	**Specification Clarifications added or updated:** • 4. No Match Firmware Proxying Configuration (Added) • 5. WUFC/PROXYFC NS Bits (Added) **Specification Changes added or updated:** • 1. PCIe Timing Parameter Update (Added) • 2. Multicast Listener Discovery (MLD) Protocol Offload is Not Supported (Added) **Errata added or updated:** • 7. Failure to Establish PCIe Link After Power Up (Added) • 8. Proxy: Neighbor Solicitation with Multicast Target Address is Not Dropped (Added) • 9. Proxy: Missing Target Link-Layer Address in Neighbor Advertisement (Added) • 10. Slow System Clock (Added)
1.2	July 8, 2013	**Documentation Updates added or updated** • 1. Port Identification LED Blinking (Word 0x04) (Added) **Errata added or updated:** • 5. DRV_LOAD is Not Cleared by PCIe Reset (Added) • 6. Proxy: Invalid Neighbor Advertisement Packet with VLAN Tag and SNAP Header (Added)
1.1	January 31, 2013	**Errata added or updated:** • 4. Protocol Offload: Incorrect Response to MLDv2 Queries (Added)
1.0	October 26, 2012	Initial release (Intel Public)

1. Introduction

This document applies to the Intel® Ethernet Controller I211.

This document is an update to a published specification, the *Intel® Ethernet Controller I211 Datasheet*. It is intended for use by system manufacturers and software developers. All product documents are subject to frequent revision, and new order numbers will apply. New documents may be added. Be sure you have the latest information before finalizing your design.

1.1 Product Code and Device Identification

Product Codes: WGI211AT (Commercial Temperature Range)

The following tables and component drawings describe the various identifying markings on the device package:

Table 1-1. Markings

Device	Stepping	Top Marking	Description
I211	A2	WGI211AT	Production (Commercial Copper)

Table 1-2. Device IDs

I211 Device ID Code	Vendor ID	Device ID	Revision ID[1]
WGI211AT (not programmed/factory default)	0x8086	0x1532	0x3
WGI211AT (programmed)	0x8086	0x1539	0x3

1. See Specification Change #3 for more details.

Table 1-3. MM Numbers

Product	MM Number	Spec	Media
WGI211AT - Production (Copper)	925144	SLJXY	Tape and Reel
	925145	SLJXZ	Tray

1.2 Marking Diagrams

Figure 1-1. I211 Production Top Marking Example

Notes:

- Line 1: With no spaces, “i”©YY
- Line 2: Fab Lot Trace Code 0123456.78 (10-char max)
- Line 3: S-Spec Code and Pb-free mark (e3 or e1)

1.3 Nomenclature Used in This Document

This document uses specific terms, codes, and abbreviations to describe changes, errata, sightings and/or clarifications that apply to silicon/steppings. See Table 1-4 for a description.

Table 1-4. Nomenclature

Name	Description
Specification Clarifications	Greater detail or further highlights concerning a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.
Specification Changes	Modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.
Errata	Design defects or errors. Errata may cause device behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.
Documentation Updates	Typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.
Doc	Document change or update that will be implemented.
Fixed	This erratum has been fixed.
Fix Planned	This erratum is intended to be fixed in a future stepping of the component.
NoFix	There are no plans to fix this erratum.
Fixed in NVM	This erratum has been fixed in NVM X.XX.
Fix Planned in NVM	This erratum is intended to be fixed in a future NVM version.
Eval	Plans to fix this erratum are under evaluation.
(No mark) or (Blank box)	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
DS	Datasheet
DG	Design Guide
SDM	Software Developer's Manual
EDS	External Data Specification
AP	Application Note

2. Hardware Clarifications, Changes, Updates and Errata

See Section 1.3 for an explanation of terms, codes, and abbreviations.

Table 2-1. Summary of Specification Clarifications

Specification Clarification	Status
1. PCIe Completion Timeout Mechanism Compliance	N/A
2. Padding on Transmitted SCTP Packets	N/A
3. Dynamic LED Modes Can Only be Used in an Active Low Configuration	N/A
4. No Match Firmware Proxying Configuration	N/A
5. WUFC/PROXYFC NS Bits	N/A
6. PCIe Separate Reference Clock with Independent Spread (SRIS) Support	N/A

Table 2-2. Summary of Specification Changes

Specification Change	Status
1. PCIe Timing Parameter Update	N/A
2. Multicast Listener Discovery (MLD) Protocol Offload is Not Supported	N/A
3. Revision ID of A2 Stepping	N/A

Table 2-3. Summary of Documentation Updates

Documentation Update	Status
1. Port Identification LED Blinking (Word 0x04)	N/A

Table 2-4. Summary of Errata; Errata Include Steppings

Erratum	Status
1. Device Off Deadlock	A2=Yes; NoFix
2. Marginal Low 10 Mb Amplitude	A2=Yes; NoFix
3. Non-Monotonic Integrated SVR Ramp	A2=Yes; NoFix
4. Protocol Offload: Incorrect Response to MLDv2 Queries	N/A
5. DRV_LOAD is Not Cleared by PCIe Reset	A2=Yes; NoFix
6. Proxy: Invalid Neighbor Advertisement Packet with VLAN Tag and SNAP Header	A2=Yes; NoFix
7. Failure to Establish PCIe Link After Power Up	A2=Yes; NoFix
8. Proxy: Neighbor Solicitation with Multicast Target Address is Not Dropped	A2=Yes; NoFix
9. Proxy: Missing Target Link-Layer Address in Neighbor Advertisement	A2=Yes; NoFix
10. Slow System Clock	A2=Yes; NoFix

Table 2-4. Summary of Errata; Errata Include Steppings (Continued)

Erratum	Status
11. Certain Malformed IPv6 Extension Headers are Not Processed Correctly by the Device	A2=Yes; NoFix
12. PCIe Advanced Error Reporting: First Error Pointer	A2=Yes; NoFix
13. PCIe Throughput with Few Credits	A2=Yes; NoFix

2.1 Specification Clarifications

1. PCIe Completion Timeout Mechanism Compliance

The I211 Completion Timeout Value[3:0] must be properly set by the system BIOS in the I211 PCIe Configuration Space Device Control 2 register (0xC8; W). Failure to do so can cause unexpected completion timeouts.

The I211 complies with the PCIe 2.0 specification for the completion timeout mechanism and programmable timeout values. The PCIe 2.0 specification provides programmable timeout ranges between 50 µs to 64 s with a default time range of 50 µs - 50 ms. The I211 defaults to a range of 16 ms - 32 ms.

Workaround:

The completion timeout value must be programmed correctly in PCIe configuration space (in Device Control 2 register); the value must be set above the expected maximum latency for completions in the system in which the I211 is installed. This ensures that the I211 receives the completions for the requests it sends out, avoiding a completion timeout scenario. Failure to properly set the completion timeout value can result in the device timing out prior to a completion returning.

The I211 can be programmed to resend a completion request after a completion timeout (the original completion request is assumed to be lost). But if the original completion arrives after a resend request, two completions may arrive for the same request; this can cause unpredictable behavior. Intel NVM images set the resend feature to off. Intel recommends that you do not change this setting.

2. Padding on Transmitted SCTP Packets

When using the I211 to offload the CRC calculation for transmitted SCTP packets, software should not add Ethernet padding bytes to short packets (less than 64 bytes). Instead, the TCTL.PSP bit should be set so that the I211 pads the packets after performing the CRC calculation.

3. Dynamic LED Modes Can Only be Used in an Active Low Configuration

In any of the dynamic LED modes (FILTER_ACTIVITY, LINK/ACTIVITY, COLLISION, ACTIVITY, PAUSED), LED blinking should only be enabled if the LED signal is configured as an active low output.

4. No Match Firmware Proxying Configuration

When the Set Firmware Proxying Configuration command is used and the No Match Data field is 0x01, any packet that passes the hardware proxy filters and cannot be processed by the firmware causes a wake up event. Care should be taken when using this setting to prevent the possibility of unintended wake-ups.

5. WUFC/PROXYFC NS Bits

The NS and NS Directed bits in both the WUFC and PROXYFC registers enable filters that pass Neighbor Solicitation packets. These filters do not check the ICMPv6 Type field, so they actually pass any ICMPv6 packet that meets all the other requirements. For example, ICMP Echo Request packets can pass these filters. Care should be exercised when setting these bits in WUFC to avoid unintentional system wake-ups.

6. PCIe Separate Reference Clock with Independent Spread (SRIS) Support

PCIe Separate Reference Clock with Independent Spread (SRIS) is NOT supported. The device requires a common PCIe reference clock and should be configured with "Common Clock: Mode in BIOS. SRIS mode causes PCI bus enumeration to fail.

2.2 Specification Changes

1. PCIe Timing Parameter Update

In Section 5.5.6 of the *Intel® Ethernet Controller I211 Datasheet*, the maximum value of timing parameter $t_{ppg\text{-}clkint}$ (PCIe* PE_RST de-assertion to internal PLL lock) has been updated to 5 ms.

2. Multicast Listener Discovery (MLD) Protocol Offload is Not Supported

IPv6 Multicast Listener Discovery (MLD) protocol offload is not supported.

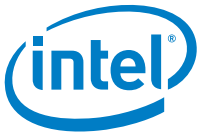
The Set Firmware Proxying Configuration host interface command must contain 0 in the Enable MLD field.

3. Revision ID of A2 Stepping

The Revision ID of the A2 stepping is either 0x02 or 0x03. The value of the least-significant bit is indeterminate.

This affects the following fields that can be read from the I211:

- Step Rev ID field in the Mirrored Revision ID (MREVID) CSR.
- Revision ID register in the PCIe configuration space.
- Version field read by the IDCODE and USERCODE JTAG instructions.



2.3 Documentation Updates

1. Port Identification LED Blinking (Word 0x04)

The default iNVM setting for this word can be left at 0xFFFF, which enables software to determine the proper mode of operation (Section 6.3.1 of the *Intel® Ethernet Controller I211 Datasheet*)

2.4 Errata

1. Device Off Deadlock

Problem:

If firmware resets (such as due to a parity error) after entering device off, the I211 does not detect the error and should enter device off but not shut the device down.

This happens only after a firmware reset.

Implication:

The chances of such an event happening while moving to device off are minimal.

Workaround:

None.

Status: A2=Yes; NoFix

2. Marginal Low 10 Mb Amplitude

Problem:

1. 10BASE-T amplitude.

   On some designs, the I211 might not meet the IEEE specification that states that the 10 Mb peak differential amplitude be between 2.2 V and 2.8 V for all data sequences.

2. 10BASE-T TP_IDLE mask failures.

   Some designs might have mask failures on the 10BASE-T TP_IDLE with TPM load.

3. 10 BASE-Te (802.3az section 14.10) amplitude.

   On some designs, the I211 might not meet the IEEE specification that states that when 10BASE-Te is enabled the 10 Mb peak differential amplitude be between 1.54 V and 1.96 V for all data sequences.

4. 10BASE-Te TP_IDLE and link test pulse waveform mask failures.

   Some designs might have mask failures on the 10BASE-Te TP_IDLE and link test pulse with and without TPM load.

Implication:

No implication on system level performance or interoperability, conformance test only impact.

Workaround:

None.

Status: A2=Yes; NoFix

3. Non-Monotonic Integrated SVR Ramp

Problem:

On some designs, both the 0.9 V and 1.5 V SVR show a non-monotonic start up.

Implication:

No functional impact for systems using an internal SVR, because the system is not vulnerable at the specific time that this non-monotonicity occurs.

Workaround:

None.

Status: A2=Yes; NoFix

4. Protocol Offload: Incorrect Response to MLDv2 Queries

Superseded by Specification Change #2.

5. DRV_LOAD is Not Cleared by PCIe Reset

Problem:

The CTRL_EXT.*DRV_LOAD* bit is not cleared by PCIe reset if Wake-on-LAN and Proxy offloads are disabled.

Implication:

Device is not visible in the Boot Manager Menu after rebooting the system.

Workaround:

Include a Word Auto-load Structure for word 0x24 in the iNVM.

This is implemented for all iNVM images starting with v0.6.

Status: A2=Yes; NoFix

6. Proxy: Invalid Neighbor Advertisement Packet with VLAN Tag and SNAP Header

Problem:

If a Neighbor Solicitation packet is received with a VLAN tag and a SNAP header, the Neighbor Advertisement (NA) response also contains a VLAN tag and a SNAP header. However, the length field in the SNAP header of the NA packet returned by the I211 contains an incorrect value.

Implication:

Neighbor Solicitation proxy offload failure.

Workaround:

Do not use both VLAN tag and SNAP header in a Neighbor Solicitation packet.

Status: A2=Yes; NoFix

7. Failure to Establish PCIe Link After Power Up

Problem:

If the first de-assertion of PE_RST_N following power-up lasts less than 5 ms, the PCIe PLL might be calibrated incorrectly. When this occurs, the PLL does not lock and the PCIe logic remains in reset until the next power cycle.

Implication:

Failure to establish PCIe link.

Workaround:

Ensure that the duration of the first de-assertion of PE_RST_N after power-up is at least 5 ms.

Status: A2=Yes; NoFix

8. Proxy: Neighbor Solicitation with Multicast Target Address is Not Dropped

Problem:

According to Section 7.1.1 of RFC 4861, a Neighbor Solicitation packet with a multicast Target Address field should be silently dropped. The I211 accepts and responds to such a packet if the Target Address corresponds to the Solicited Node address provided by the host.

Implication:

No implication when the network is functioning correctly since this is not a valid packet. Reduced immunity to invalid inputs.

Workaround:

None.

Status: A2=Yes; NoFix

9. Proxy: Missing Target Link-Layer Address in Neighbor Advertisement

Problem:

If a Neighbor Solicitation packet does not include a source link-layer address option, the Neighbor Advertisement packet sent by the I211 in response does not include a target link-layer address option.

Implication:

If the link partner is performing Duplicate Address Detection, the Neighbor Advertisement packet generated by the I211 is dropped by the receiver since the target link-layer address is missing. As a result, there could be undetected duplicate addresses on the network.

Workaround:

None.

Status: A2=Yes; NoFix

10. Slow System Clock

Problem:

On some devices, the internal PLL circuit occasionally provides the wrong clock frequency after power up. The probability of failure is typically less than one failure per 1000 power cycles. When the failure occurs, the internal clock frequency is in the range of 1/10 to 1/20 of the correct frequency.

The failure can be detected from software by either of the following:

- Read internal PHY register 14 from page 252 as detailed in Step 3 of the workaround. The failing state is indicated by a value of 0xFF in bits 7:0.
- Read the FRTIMER register twice at a known time interval and see if the difference in the two values matches the interval.

Implication:

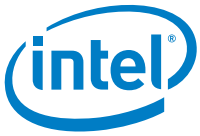
No link can be established until the next power cycle.

Workaround:

The following workaround can be performed in software.

Note: If a failure occurs, there is no link before the software runs, so APM WoL is not totally reliable in these applications.

1. Acquire the PHY semaphore.
2. Set MDICNFG.*Destination* to 0b.
3. Read PHY register 14 from page 252:
   a. Write 0xFC to PHY register 22 (dec) using MDIC.
   b. Wait at least 20 μs.
   c. Read from PHY register 14 (dec) using MDIC.
   d. Wait at least 20 μs.
   e. Write 0b to PHY register 22 (dec) using MDIC.



If bits 7:0 of the PHY register read in sub-step (c) != 0xFF, go to Step 15.

If the value is 0xFF after several (5) attempts to fix it (loops through Step 14), exit with a fatal error.

4. Set CTRL.*PHY_RST* to 1b.
5. Set both CTRL_EXT.*PHY_Power_Down_Enable* and CTRL_EXT.*SerDes_Low_Power_Enable* to 1b.
6. Clear WUC.
7. Determine the value of auto-load word 0x0A. If this word exists in the iNVM, use that value. Otherwise, use the hardware default value, 0x202F.
8. Perform a bitwise OR of 0x0010 with the value from the Step 6 and write it as an auto-load of 0x0A using EEARBC.
9. Set PCIe configuration space register PMCSR bits 1:0 to 11b. (D3 state).
10. Wait 1 ms.
11. Set PCIe configuration space register PMCSR bits 1:0 to 00b. (D0 state).
12. Write the value from Step 6 as an auto-load of 0x0A using EEARBC.
13. Restore WUC to its original value, if necessary.
14. Go to Step 2.
15. Restore MDICNFG.*Destination* to its original value, if necessary.
16. Release the PHY semaphore

This workaround has been implemented in Intel software device driver 19.1.

Status: A2=Yes; NoFix

11. Certain Malformed IPv6 Extension Headers are Not Processed Correctly by the Device

Problem:

Certain malformed IPv6 extension headers are not processed correctly by the device.

Implication:

If a packet containing such malformed IPv6 extension headers is received, the device might behave unpredictably.

Workaround:

Set bit 16 (*IPv6_ExDis*) in the RFCTL register to disable the processing of received IPv6 extension headers.

Note: With this bit set, checksum calculation and RSS are disabled for IPv6 packets containing extension headers.

This workaround has been implemented in Intel drivers starting from Release 20.2.

Status: A2=Yes; NoFix

12. PCIe Advanced Error Reporting: First Error Pointer

Problem:

The First Error Pointer in the Advanced Error Capabilities and Control Register (PCIe register 0x118 bits 4:0) is a field that identifies the bit position of the first error reported in the Uncorrectable Error Status register. In the I211 implementation, the following bits of the Uncorrectable Status Register are not covered by this field:

- Bit 4 -Data Link Protocol Error Status.
- Bit 13 - Flow Control Protocol Error Status.
- Bit 14 - Completion Timeout Status.

Implication:

PCIe specification compliance issue.

Workaround:

None.

Status: A2=Yes; NoFix

13. PCIe Throughput with Few Credits

Problem:

A received Update FC DLLP is not always processed immediately. It sometimes stalls in the I211 until the next TLP or DLLP is received.

Implication:

Reduced PCIe throughput when the number of credits provided by the PCIe port to which the I211 is connected is too small for continuous PCIe traffic.

Workaround:

Connect the I211 to a PCIe port that provides enough PCIe credits for continuous PCIe traffic.

Status: A2=Yes; NoFix

3. Software Clarifications

Table 3-1. Summary of Software Clarifications

Software Clarification	Status
1. While in TCP Segmentation Offload, Each Buffer is Limited to 64 KB	N/A
2. Serial Interfaces Programmed by Bit Banging	N/A

1. While in TCP Segmentation Offload, Each Buffer is Limited to 64 KB

The I211 supports 256 KB TCP packets. However, each buffer is limited to 64 KB since the data length field in the transmit descriptor is only 16 bits. This restriction increases driver implementation complexity if the operating system passes down a scatter/gather element greater than 64 KB in length. This can be avoided by limiting the offload size to 64 KB.

Investigation has concluded that the increase in data transfer size does not provide any noticeable improvements in LAN performance. As a result, Intel network software drivers limit the data transfer size in all drivers to 64 KB.

Please note that Linux operating systems only support 64 KB data transfers.

For further details about how Intel network software drivers address this issue, refer to Technical Advisory TA-191.

2. Serial Interfaces Programmed by Bit Banging

When bit-banging on a serial interface (such as SPI, I^2C, or MDIO), it is often necessary to perform consecutive register writes with a minimum delay between them. However, simply inserting a software delay between the writes can be unreliable due to hardware delays on the CPU and PCIe interfaces. The delay at the final hardware interface might be less than intended if the first write is delayed by hardware more than the second write. To prevent such problems, a register read should be inserted between the first register write and the software delay, i.e. “write”, “read”, “software delay”, “write”.

LEGAL