HT6535
SPP/EPP/ECP Controller

Features

- Multi-mode parallel port controller
  - Standard mode: IBM PC/XT, PC/AT and PS/2 compatible bidirectional parallel port
  - Enhanced parallel port (EPP) mode
  - Extended capabilities port (ECP) mode
- Support 6 base addresses
- 68-pin PLCC and 80-pin QFP package

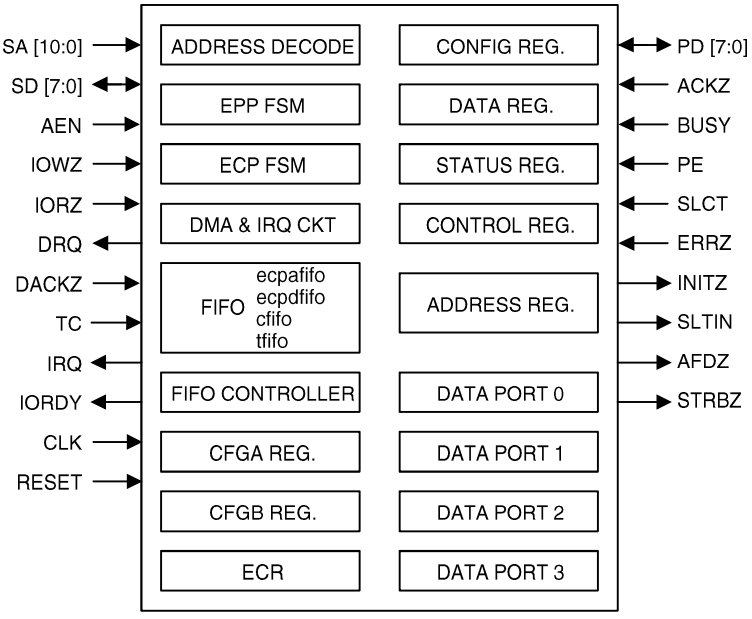
General Description

The Parallel Port Controller incorporates one IBM XT/AT compatible parallel port and support the PS/2 type bidirectional parallel port, the enhanced parallel port (EPP) and the extended capabilities port (ECP) modes. Refer to the Hardware/Software configuration description for information on changing the base address, selecting the mode of operation and setting the FIFO threshold that is used in ECP operation.

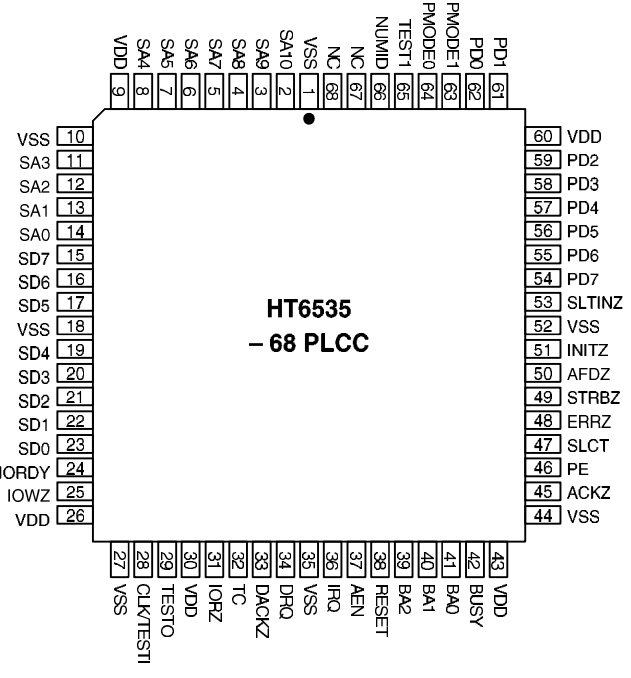
EPP retains complete backward compatibility with the existing XT/AT and PS/2 compatible functions and interface. EPP can provide high performance for bidirectional block mode data transfer. This is largely accomplished through hardware handshake.

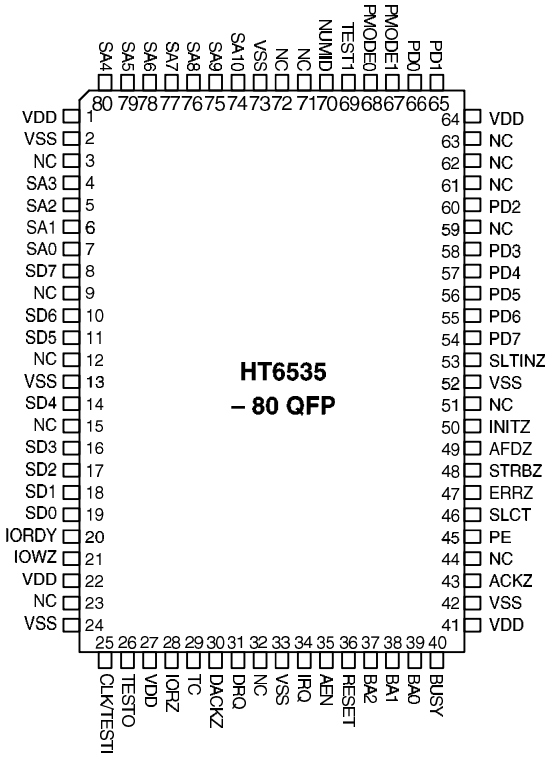
ECP is software and hardware-compatible with existing parallel ports. It provides an automatic high-burst bandwidth channel that supports DMA for ECP in both the forward and reverse directions. This chip supports 16-byte FIFO to smooth data flow and improves the bandwidth requirement. It also supports run-length encode (RLE) decompression in hardware.

Block Diagram



Pin Assignments





Pin Description

Pin Name	I/O	Description
SA [10:0]	I	These host address bits determine the I/O address to be accessed during IORZ and IOWZ cycles
SD [7:0]	I/O	The ISA data bus used by the host microprocessor to transmit data to or from this chip
IORDY	O	Normally, this pin is use as IORDY to extend the read/write command in EPP mode
IOWZ	I	This active low signal is issued by the host microprocessor to indicate a write operation
CLK/TESTI	I	14.318 MHz OSC input or 24MHz crystal input
TESTO	O	24 MHz crystal output
IORZ	I	This active low signal is issued by the host microprocessor to indicate a read operation
TC	I	This signal indicates to this chip that DMA operation data transfer is complete

Pin Name	I/O	Description
DACKZ	I	An active low input acknowledging the request for a DMA transfer of data
DRQ	O	This active high output is the DMA request for byte transfers of data to the host
IRQ	O	This pulse low output is the interrupt request signal. Note that this signal needs a connected external pull-up resistor
AEN	I	Active low address enable indicates microprocessor operations on the host data bus
RESET	I	Active high input signal that resets this chip
BA[2:0]	I	Parallel port base address select inputs for hardware initial setup
BUSY	I	This is a status input from the printer, high indicating that the printer is not ready to receive new data
ACKZ	I	A low active input from the printer indicating that it has received the data and is ready to accept new data
PE	I	A status input from the printer, high indicating that the printer is out of paper
SLCT	I	This high active output from the printer indicates that it has power on
ERRZ	I	A low on this input from the printer indicates that there is an error condition at the printer
STRBZ	O	A low active pulse on this output is used to strobe the printer data into the printer
AFDZ	O	This output goes low to cause the printer to automatically feed one line after each line is printed
INITZ	O	This is use to initiate the printer when low
SLTINZ	O	This active low output selects the printer
PD [7:0]	I/O	The bi-directional parallel data bus is used to transfer information between CPU and peripherals
PMODE[1:0]	I	Parallel port mode select inputs for hardware initial setup
TEST1	I	This input pin is for testing. It must be pulled low.
NUMID	I	This input pin decides the chip number ID. Refer to hardware configuration for use of this pin. It is pulled up internally.
NC	—	
VDD	—	Positive power supply inputs
VSS	—	Ground reference power supply inputs

Absolute Maximum Ratings

Supply Voltage ..... –1.3V to 5.5V
Input Voltage ..... V_{SS}–0.3V to V_{DD}+0.3V
Storage Temperature ..... –50°C to 125°C
Operating Temperature ..... 0°C to 70°C

D.C. Characteristics

(Ta=0° to 70°C, V_{DD}=5V±5%, V_{SS}=0V)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{IL}	Input Low Voltage	5V	—	–0.3	—	0.8	V
V_{IH}	Input High Voltage	5V	—	2.0	—	V_{DD}+0.3	V
I_{LIH}	Input High Leakage	5V	V_{IN}=V_{DD}	—	—	10	μA
I_{LIL}	Input Low Leakage	5V	V_{IN}=0V	—	—	–10	μA
V_{OL}	Output Low Voltage	5V	I_{sink}=6mA	—	—	0.4	V
V_{OH}	Output High Voltage	5V	I_{sour}=6mA	2.4	—	V_{DD}	V
C_{IN}	Input Capacitance	5V	—	—	—	5	PF
C_{OUT}	Output Capacitance	5V	—	—	—	10	PF
I_{STBY}	Standby Current	5V	—	—	—	10	μA
V_T	Threshold Voltage of CLK/TESTI Pin	5V	—	—	2.5	—	V
$I_{PULL-UP}$	Input with Internal Pull-High current	5V	V_{IN}=0	50	—	500	μA

Note 1: Standby current is measured with input gating, output unloading and CLK/TESTI=0.

Functional Description

Hardware Configuration

Hardware configuration are defined through the conditioning of PMODE [1:0] and BA [2:0] pins during power-on reset.

PMODE 1	PMODE 0	Parallel Port Mode
0	0	ISA Compatible
0	1	PS/2 Compatible
1	0	EPP
1	1	ECP

BA2	BA1	BA0	Base Address
0	0	0	378 H
0	0	1	278 H
0	1	0	3BCH
0	1	1	Disable
1	0	0	268H
1	0	1	26CH
1	1	0	27CH
1	1	1	Disable

- When the chip is disabled, the ISA-interface output pins will become tri-state.
- Two controller chips can be used simultaneously on a board by pulling up or NC the "NUMID" pin as controller #1 and pulling low the "NUMID" pin as controller #2. Refer to software configuration for use of this pin.

Software Configuration

After RESET the default values will be loaded into the configuration registers. The procedures for setting up the configuration registers are described as follows:

- To enter the configuration mode
  - Write 55H to 2FAH twice
  - Followed by writing AAH to 3FAH twice (if "NUMID"=1), or writing 55H to 3FAH twice (if "NUMID"=0)
- To program the configuration register
  - Write XXH to 3FAH, where XXH is the configuration register index
  - Followed by writing YYH to 2FAH, where YYH is the data for the configuration register XXH.
- To exit from the configuration mode
  Write 0FH to 3FAH, then write any value to 2FAH

The following describes the bit functions of each configuration register. Note that the configuration registers are all write only.

- Index 00: ECP FIFO threshold register (default value=00H)

3	2	1	0
0	0	0	0

- Index 01: Parallel port mode register

1	0	
PMODE1	PMODE0	
0	0	ISA Compatible
0	1	PS/2 Compatible
1	0	EPP
1	1	ECP

* SPP data register read and write modes

	CTR5	IORZ	IOWZ	Result
ISA Compatible	X	1	0	Data written to PD[0:7]
	X	0	1	Data read from the output latch
PS2 Compatible	0	1	0	Data written to PD[0:7]
	1	1	0	Data written is latched
	0	0	1	Data read from the output latch
	1	0	1	Data read from PD[0:7]

* EPP data register read and write modes

CTR5	IORZ	IOWZ	Result
X	1	0	Data written to PD[0:7]
X	0	1	Data read from PD[0:7]

• Index 02: Base address register

2	1	0	
BA2	BA1	BA0	
0	0	0	378H
0	0	1	278H
0	1	0	3BCH
0	1	1	Disable
1	0	0	268H
1	0	1	26CH
1	1	0	27CH
1	1	1	Disable

Note that the base address 3BCH, 26CH and 27CH cannot be selected for EPP mode.

Configuration example

The following is an example of configuration program in 80X86 assembly language:

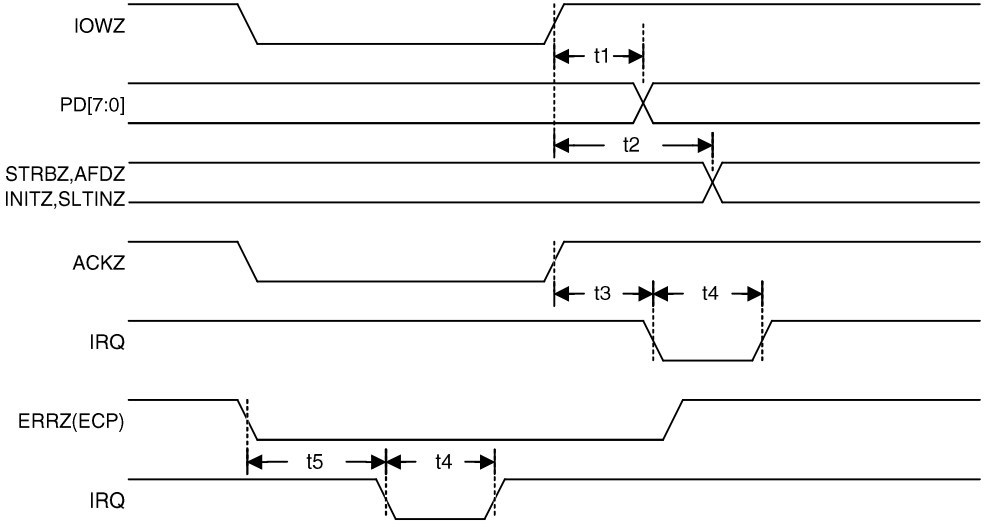
```
; ------------------------------------------------------
; Enter the configuration mode
; ------------------------------------------------------
        DX,
        AL,
        DX,
        DX,
MOV     DX,
MOV     AL,
OUT     DX,
OUT     D X ,
MOV     2FAH    ;       if
MOV     55H     NUM
OUT     AL      ID=1
OUT     AL
        3FAH
        AAH
        AL
        AL

; ------------------------------------------------------
; Program configuration registers
; ------------------------------------------------------
MOV     DX,     3FAH
MOV     AL,     00H
OUT     DX,     AL
MOV     DX,     2FAH
MOV     AL,     YYH
OUT     DX,     AL
MOV     DX,     3FAH
MOV     AL,     01H
OUT     DX,     AL
MOV     DX,     2FAH
MOV     AL,     YYH
OUT     DX,     AL
MOV     DX,     3FAH
MOV     AL,     02H
OUT     DX,     AL
MOV     DX,     2FAH
MOV     AL,     YYH
OUT     DX,     AL

; ------------------------------------------------------
; Exit configuration mode
; ------------------------------------------------------
MOV     DX,     3FAH
MOV     AL,     0FH
OUT     DX,     AL
MOV     DX,     2FAH
MOV     AL,     XXH
OUT     DX,     AL
```

Note that if two controllers are used, the configuration of controller #2 should begin after exiting the configuration mode of controller #1.

In EPP mode, if a time-out (10μs approximately) occurs, the current EPP cycle is aborted and the time-out condition is indicated in the Status register bit 0 as a logic "1". To clear this time-out bit, just write any value to the Status register.

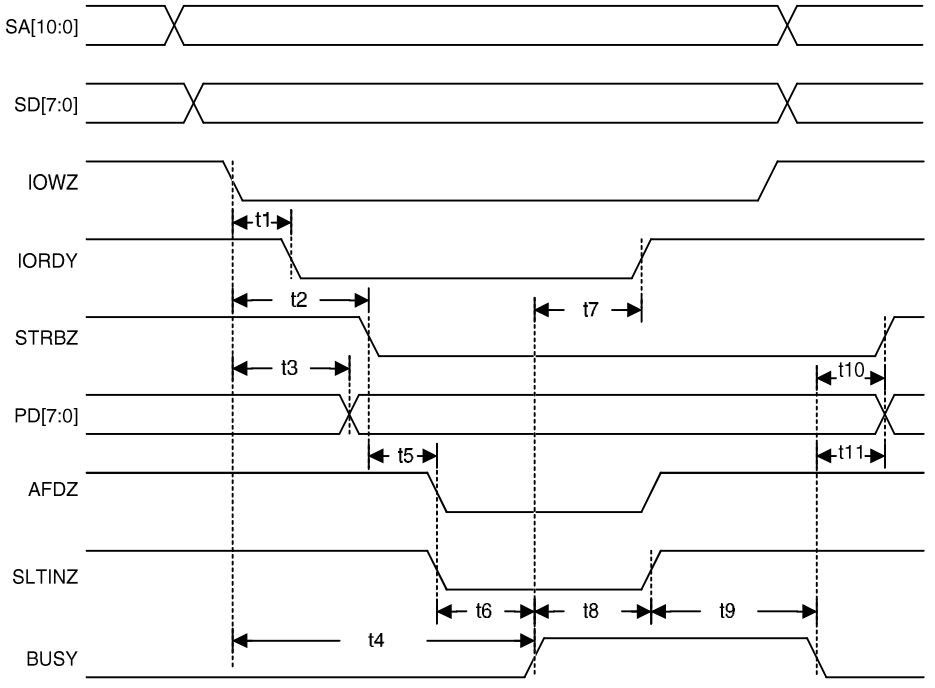
Timing Diagram

Parallel port timing



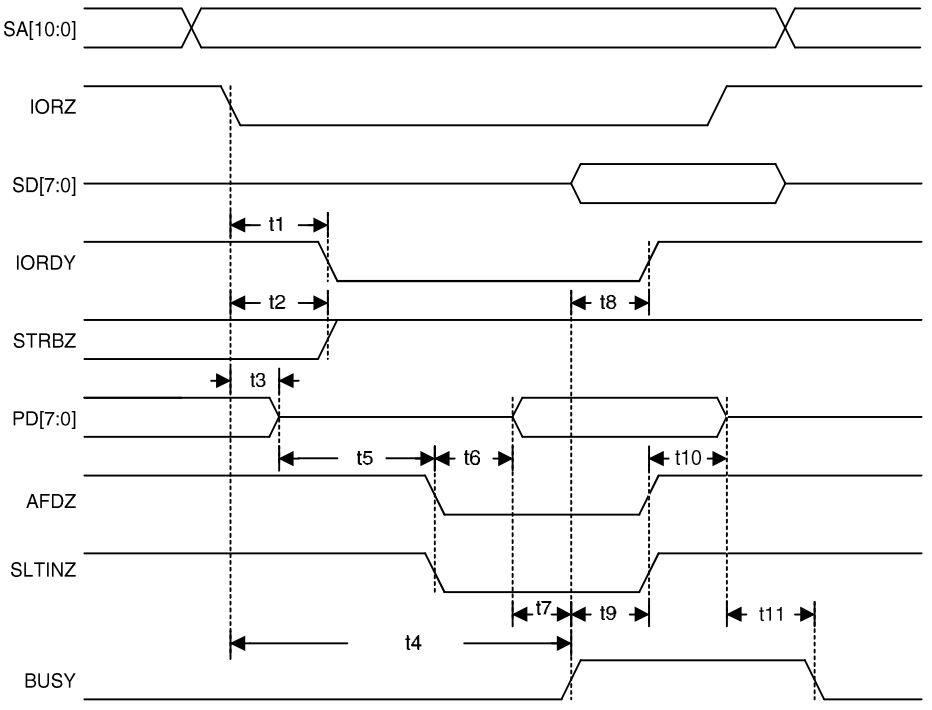
	Parameter	Min.	Max.	Units	Notes
t1	PD[7:0] delay from IOWZ inactive		60	ns	
t2	STRBZ, AFDZ, INITZ, SLTINZ delay from IOWZ inactive		100	ns	
t3	IRQ delay from ACKZ		70	ns	
t4	IRQ active low pulse width	800		ns	
t5	IRQ delay from ERRZ		180	ns	

EPP address or data WRITE cycle timing



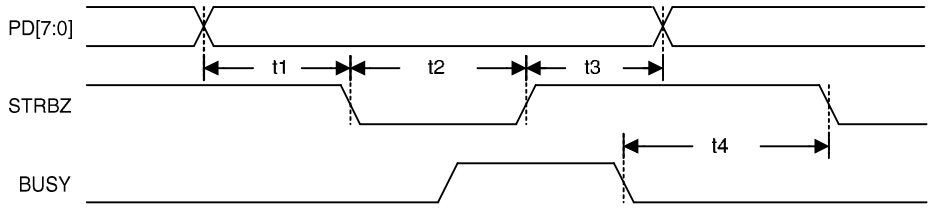
	Parameter	Min.	Max.	Units	Notes
t1	IOWZ asserted to IORDY asserted	10	80	ns	
t2	IOWZ asserted to STRBZ asserted	140	240	ns	
t3	IOWZ asserted to PD[7:0] valid		150	ns	
t4	time out	10	12	μs	
t5	STRBZ asserted to AFDZ, SLTINZ asserted	70	80	ns	
t6	AFDZ, SLTINZ asserted to BUSY asserted	0		ns	
t7	BUSY asserted to IORDY deasserted	70	140	ns	
t8	BUSY asserted to AFDZ, SLTINZ deasserted	70	140	ns	
t9	AFDZ, SLTINZ deasserted to BUSY deasserted	0			
t10	BUSY deasserted to STRBZ deasserted	70	140	ns	
t11	BUSY deasserted to PD[7:0] invalid		140	ns	

EPP address or data READ cycle timing



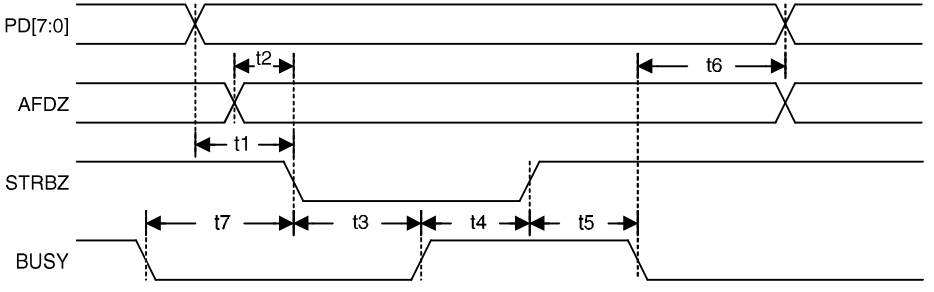
	Parameter	Min.	Max.	Units	Notes
t1	IORZ asserted to IORDY asserted	0	80	ns	
t2	IORZ asserted to STRBZ deasserted	0		ns	
t3	IORZ asserted to PD[7:0] Hi-Z	0	70	ns	
t4	time out	10	12	μs	
t5	PD[7:0] Hi-Z to AFDZ, SLTINZ asserted	140	210	ns	
t6	AFDZ, SLTINZ to PD[7:0] valid	0		ns	
t7	PD[7:0] valid to BUSY asserted	0		ns	
t8	BUSY asserted to IORDY deasserted	70	140	ns	
t9	BUSY asserted to AFDZ, SLTINZ deasserted	70	140	ns	
t10	AFDZ, SLTINZ deasserted to PD[7:0] Hi-Z	0		ns	
t11	PD[7:0] Hi-Z to BUSY deasserted	0		ns	

ECP parallel port FIFO mode timing



	Parameter	Min.	Max.	Units	Notes
t1	PD[7:0] valid to STRBZ active	500		ns	
t2	STRBZ active pulse width	500		ns	
t3	PD[7:0] hold from STRBZ inactive	500		ns	
t4	BUSY inactive to STRBZ active	900		ns	

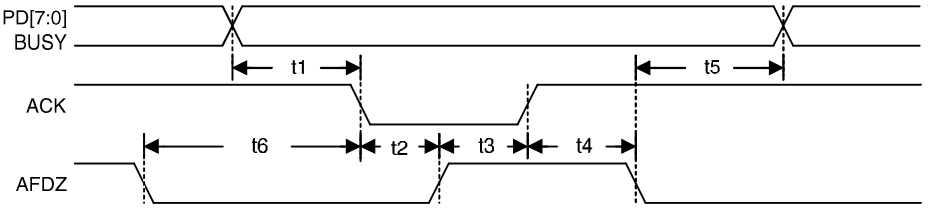
ECP parallel port forward timing



	Parameter	Min.	Max.	Units	Notes
t1	PD[7:0] valid to STRBZ asserted	0	180	ns	
t2	AFDZ valid to STRBZ asserted	0	70	ns	
t3	STRBZ asserted to BUSY asserted	0		ns	
t4	BUSY asserted to STRBZ deasserted	70	140	ns	
t5	STRBZ deasserted to BUSY deasserted	0		ns	
t6	BUSY deasserted to PD[7:0] changed	140	170	ns	
t7	BUSY deasserted to STRBZ asserted	560	850	ns	1

1. Maximum value only applies if there is data in the FIFO waiting to be written out.

ECP parallel port reverse timing



	Parameter	Min.	Max.	Units	Notes
t1	PD[7:0], BUSY valid to ACKZ asserted	0		ns	
t2	ACKZ asserted to AFDZ deasserted	140	210	ns	1
t3	AFDZ asserted to ACKZ deasserted	0		ns	
t4	ACKZ deasserted to AFDZ asserted	300	350	ns	
t5	AFDZ asserted to PD[7:0] changed	0		ns	
t6	AFDZ asserted to ACKZ asserted	0		ns	

1. Maximum value only applies if there is room in FIFO and a terminal count has not been received.

Application Circuit