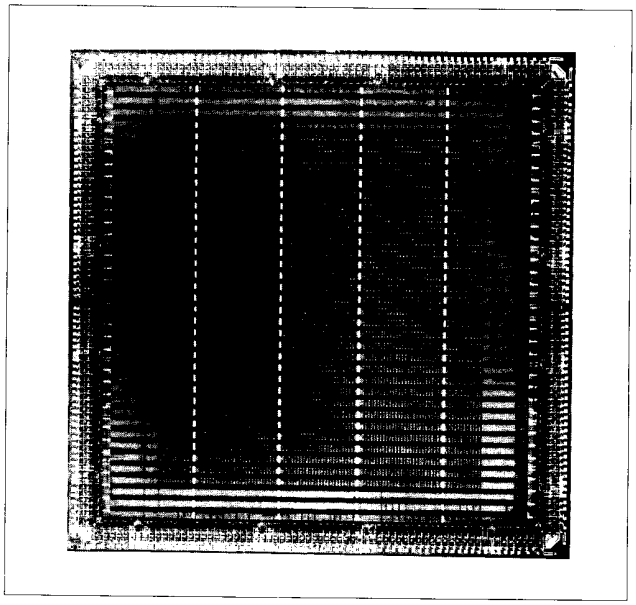
ADE-206-001C(H)
Feb.1990

HG62E SERIES
(Hitachi CMOS Gate Array)

HITACHI

The HG62E series is a master slice CMOS gate array of which the gate length is 1 μm and uses 2-layer metal interconnect technology. Auto-diagnosis is a typical feature of HG62E series. This series has twelve master chips with high gate count/pads from 770/68 to 24,020/272. These chips can replace not only CMOS logics but also TTL logics due to the high speed of 0.7 ns typ and compatibility of input and output buffers at TTL/CMOS level.

LSI design is fully automated by the DA (Design Automation) system and custom LSI are developed based on logic diagrams and test patterns from the customer in a short time and with reasonable cost. The engineering workstation method of interface is also available.



■ FEATURES

- **Auto-diagnosis**
  Our DA will generate test circuit and test pattern automatically.
- **Fast operation**
  Internal gate (2-input NAND, FO = 2, AI = 2 mm)
  . . . . . 0.7 ns typ
  Input buffer (FO = 2, AI = 2 mm) . . . . . 2.0 ns typ
  Output buffer (C_L = 50 pF) . . . . . 7.0 ns typ
- **Low power dissipation**
  At 10 MHz operation (internal gate) . . . 200 μW/gate typ
- **Flexible input and output configurations**
  Output can be CMOS/open drain/3-state
  Compatibility of input and output buffers at TTL/CMOS level.
  Oscillator, Schmitt input, pull-up/down resistors are available.
- **Wide operation temperature range**
  −20 to +75°C
- **Wide package selection**
  Especially plastic packages with high pin count
- **Powerful design support**
  Hierarchical design capability
  Test pattern evaluation with fault simulator
  Auto-generation of test pattern
  Designs support at local design center
  EWS support available
- **Quick turn around time and reasonable development cost**

■ LINE UP

		HG62E08	HG62E11	HG62E15	HG62E22	HG62E33
Gate count		770	1162	1515	2178	3297
Max. pad count		68	80	86	102	120
Package type and max. available Signal pin number	DILP-40	○38	○38	○38	○38	○38
	DILP-64S	⊙60	⊙60	○60	○60	○60
	QFP-64	○60	○60	○60	○60	○60
	QFP-80		○76	○76	○76	○76
	QFP-100			○82	○96	○96
	QFP3-64	○60	○60	○60	○60	○60
	QFP3-80		○76	○76	○76	○76
	QFP5-136					○112
	PLCC-44	○40				
	PLCC-68	⊙64	⊙64	⊙64	⊙64	⊙64
	PLCC-84			△	△	△

		HG62E43	HG62E58	HG62E75	HG62E101	HG62E130	HG62E182	HG62E240
Gate count		4309	5821	7488	10076	13015	18176	24020
Max. pad count		100	118	138	162	190	230	272
Package type and max.* available Signal pin number	DILP-40	○38	○38	○38				
	DILP-64S	○60	○60	○60	○60	○60		
	QFP-64	○60	○60	○60				
	QFP-80	○76	○76	○76	○76			
	QFP-100	○96	○96	○96	○96			
	QFP5-136		○110	○128	○128	○128		
	QFP5-168				○146	○152		
	QFP5-208						○188	
	PLCC-68	⊙64	○64	○64	○64	○64		
	PLCC-84	○80	○80	△	△			
	PGA-135			○127	○127			
	PGA-179				○146	○163		
	PGA-240						○198	○208

*Includes output dedicated pin (max. 8)

Notes QFP: QFP1420 (EIAJ)
QFP3: QFP1414 (EIAJ)
QFP5: QFP2828 (EIAJ)

△: Under development
⊙ : Applicable for wide-temperature range (Ta = −40 ~ +85℃)

■ ABSOLUTE MAXIMUM RATINGS

Item		Symbol	Rating	Unit
Supply Voltage		V_{CC}	−0.3 to +6.7	V
Terminal Voltage	Input	V_{TI}	−0.3 to +6.7	V
	Output	V_{TO}	−0.3 to V_{CC}+0.3	V
Output Current	per one output	I_O	−16 to +16	mA
	per one V_{CC}-GND	I_{OT}	−70 to +70	mA
Operating Temperature		T_{opr}	−20 to +75	°C
Storage Temperature	with Bias	T_{bias}	−20 to +85	°C
	without Bias	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±5%, T_a = −20 to +75°C)

Item		Symbol	Test Conditions	min.	typ.	max.	Unit
Input Voltage (TTL Level)		V_{IHT}		2.2	–	V_{CC}+0.3	V
		V_{ILT}		−0.3	–	0.8	V
Input Voltage (CMOS Level)		V_{IHC}		0.7×V_{CC}	–	V_{CC}+0.3	V
		V_{ILC}		−0.3	–	0.3×V_{CC}	V
Schmitt Trigger (TTL Level)		V_{TT}^+	V_{CC} = 5 V	1.5	–	2.5	V
		V_{TT}^-	V_{CC} = 5 V	0.5	–	1.5	V
		ΔV_{TT}	V_{CC} = 5 V	0.3	–	–	V
Schmitt Trigger (CMOS Level)		V_{TC}^+	V_{CC} = 5 V	2.8	–	4.0	V
		V_{TC}^-	V_{CC} = 5 V	1.2	–	2.4	V
		ΔV_{TC}	V_{CC} = 5 V	0.3	–	–	V
Output Voltage		V_{OH}	I_{OH}= −2 mA	3.5	–	–	V
		V_{OL}	I_{OL}= 8 mA	–	–	0.5	V
Input Leakage Current		I_{LI}		–	–	1	μA
Output Leakage Current		I_{LO}	at high impedance	–	–	1	μA
Pull-up Current		I_{PU}	V_{IN} = GND	80	220	550	μA
Pull-down Current		I_{PD}	V_{IN} = V_{CC}	80	220	550	μA
Gate Delay	Internal	t_{pd}	2 input NAND, FO = 2, Aℓ = 2 mm	–	0.7	–	ns
	Input Buffer	t_{pd}	FO = 2, Aℓ = 2mm	–	2.0	–	ns
	Output Buffer	t_{pd}	C_L = 50 pF	–	7.0	–	ns
Power Dissipation		I_{CC}	Internal 2 input NAND at 10 MHz	–	40	–	μA/Gate

■ TERMINAL CAPACITANCE (T_a = 25°C, f = 1 MHz)

Item	Symbol	Test Conditions	min.	typ.	max.	Unit
Terminal Capacitance	C_T	V_{in} = 0V	–	–	12.5	pF

* This parameter is sampled and not 100% tested.

■ DEVELOPMENT FLOW

Development flow of gate arrays is shown below. Logic design and test patterns development are done by users. These are fed to a computer which performs logic simulation. The machine drawn logic diagram is checked by the user. After the logic simulation and timing rule check, fault simulation is performed with test patterns designed by user to verify logic design. Auto-diagnosis detects the faults which fault simulation could not find. Then automatic layout and delay check of critical path are performed. After these design check, PG tape and test tape are generated. Sample production takes very short time because it needs only metal wiring on inventory wafers.

Finished wafers are probed with following two test patterns, of users design and auto-generation, then assembled, tested again and shipped.

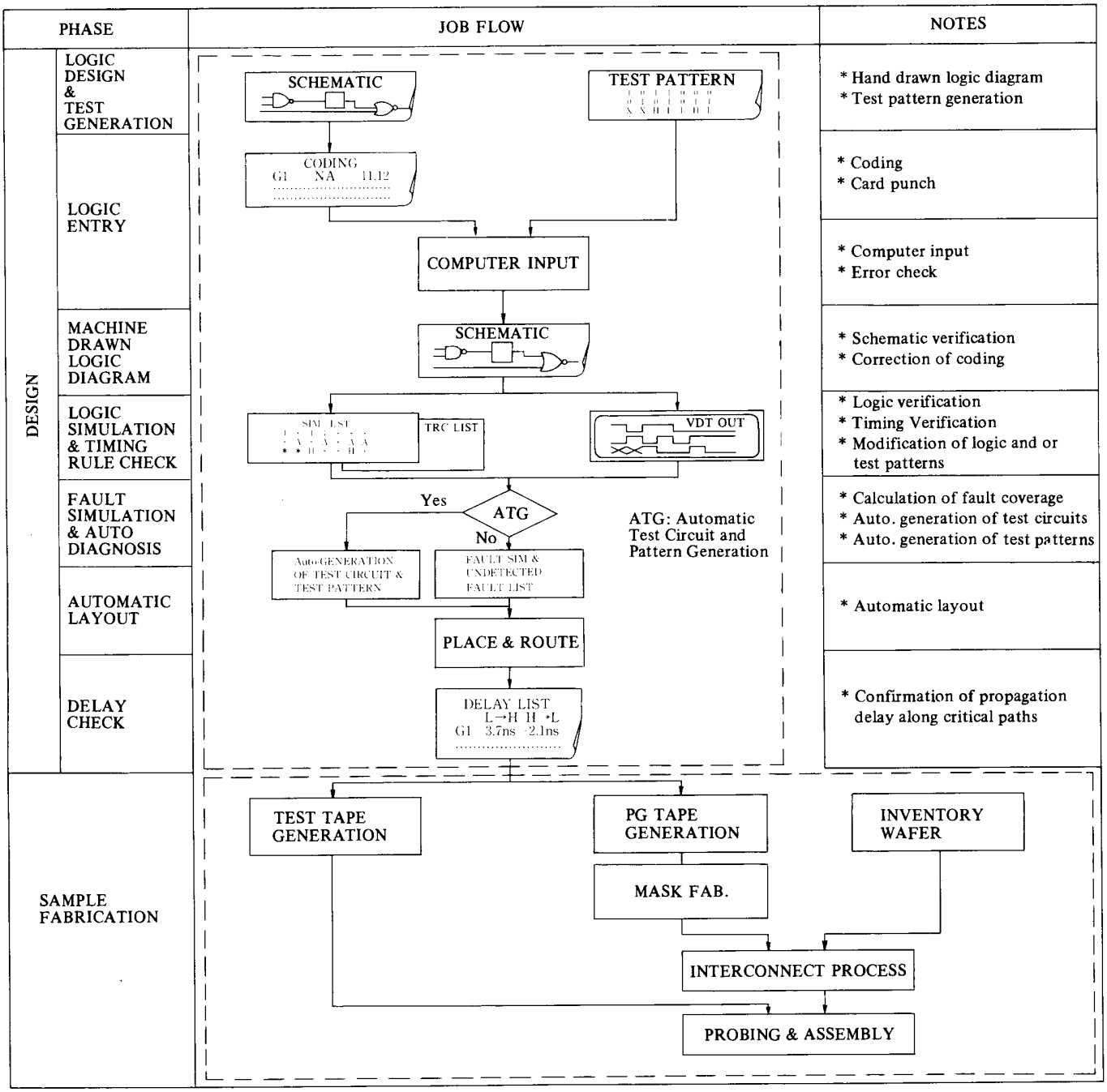
There are two standard interfaces between a user and Hitachi, Namely:

(1) Logic diagram interface

The user supplies logic diagram and test patterns to Hitachi. Further jobs are done by Hitachi except for same confirmation by the user.

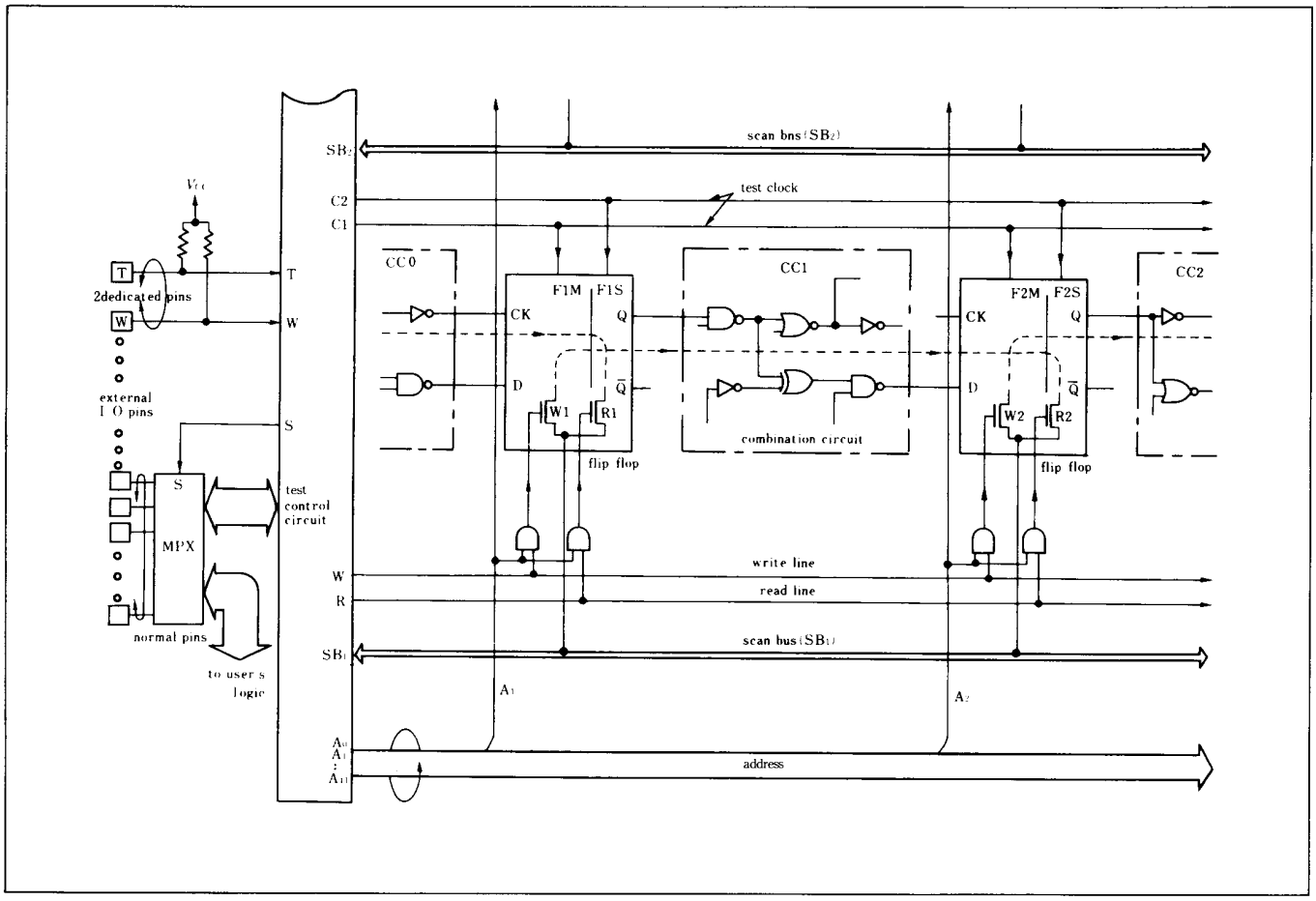
(2) Logic file interface

The user performs simulations by himself on his EWS, simulator or Hitachi's terminal for design. Then the user supplies Hitachi with complete logic file. Our engineers are willing to support the customer.



■ AUTO-DIAGNOSIS

Following is a schematic diagram of auto-diagnosis using scan bus. Auto-diagnosis requires such signals as address and scan bus assigned to flip-flop, read/write line, test clock etc. Diagnosis control circuit including address decoder controls these signals. Normal pin can be used as the pin of address and scan bus. Two test dedicated pins are required to control the test control circuit. Use flip-flops with scan (read/write) function, which consist of master part (performs normal functions) and slave part (latches data for a time). When you design logic, it is not necessary to take the circuits mentioned before into consideration.



The algorithm of combination circuit is not so complex, it is possible to generate high fault coverage of test patterns. But if the circuit includes flip-flops, it is difficult to get high fault coverage. Entire circuit is partitioned into combination circuits separated by flip-flops. Flip-flops are regarded as I/O terminals using scan bus. DA will generate the test patterns of every combination circuit separated by flip-flops.

- Procedure

(1) Auto-generation of test circuit

DA system will generate all test circuits; test control circuit, multiplexer, address, scan bus and clock after the logic verification by simulation.

(2) Auto-generation of test patterns

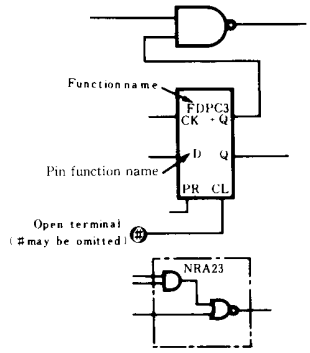
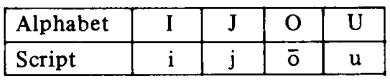
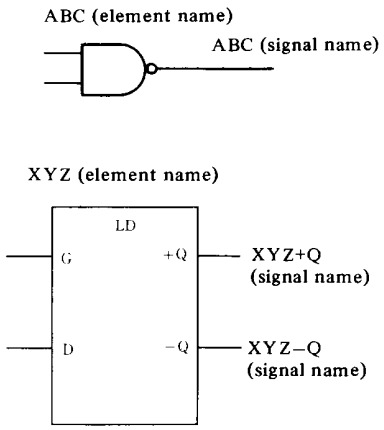
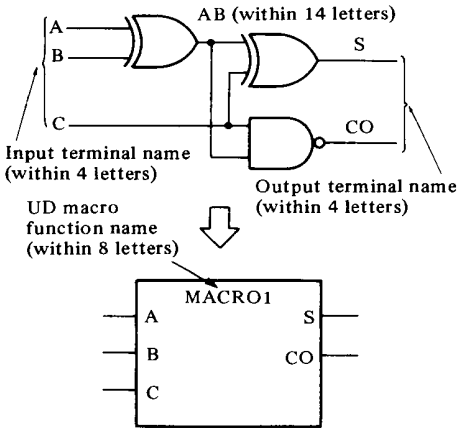
DA system will generate test patterns. The following is an example of testing combination circuit CC1 in the diagram.

① Scan in the data for CC1 testing at the slave side of flip-flop. Select address A1, then data is transmitted by the route of external I/O Pin → Scan bus (SB_1) → W_1 → F_1M → F_1S.

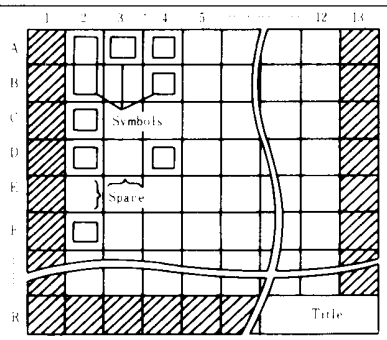
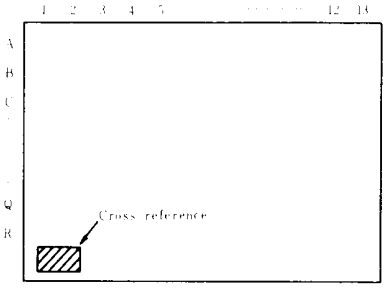
② The data passed CC1 is transmitted to flip-flop. The circuit becomes normal operation mode and the data is transmitted by the route of F_1S → CC1 → F_2M.

③ The data in flip-flop is scanned out on external I/O Pin. Select address A_2, then data is transmitted by the route of F_2M → F_2S → SB_1 → external I/O Pin.

Apply these procedure to generate high fault coverage of test patterns based on the fault detection algorithm of combination circuit.

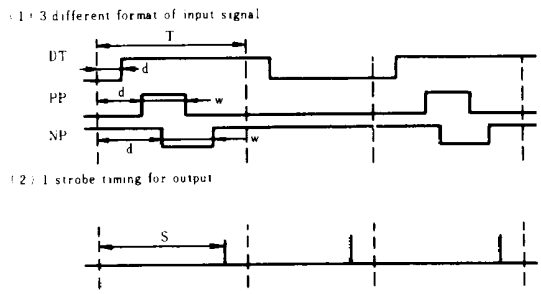
No.	Item	Rules	Examples
1.	Forms	Size A-3 forms supplied by Hitachi	
2.	Logic symbol	(1) Draw logic diagram with exactly the same symbols as shown in Macrocell Library including function name, terminal name and the size. (2) The internal symbol surrounded by dotted line can be omitted but macro function name must be described and the position of terminal can not be changed instead. (3) The template shall be provided. (4) 3-state gate will occupy 2 blocks in the drawing form.	
3.	Characters	(1) 2 to 3mm higher or larger alphabets, +, −, 0 to 9 in total 38 characters. (2) The letters shown in the table must be written as in the bottom column.	
4.	Signal/element name	(1) Give name all LSI pins within 8 letters. (2) Give name elements and internal signals within 14 letters. You can use different names for element and its output signal. For easy reference of signal name, (a) Use same name for a element and its output when it has only one output signal. (b) For the output signal names, use the combined names of element and its output terminals, when it has two or more output terminals. (c) It is easier to name a macrocell by using its location and page number of logic diagram.	
5.	Hierarchical design	The user can define his own macrocell as block (UD macro) and also can define blocks within the block. (1) Give name to the macrocells which composes UD macro within 14 letters. (2) Name input and output terminals of UD macro within 4 letters. (3) Give functional name to UD macro within 8 letters. Don't use letter '−' (minus) in the UD macro name. (4) For the symbol size of a UD macro, the width is the 'A' size of the template. Hight can be determined in proportion to the number of input or output terminals.	

(to be continued)

No.	Item	Rules	Examples
		Now, UD-macro can be used in a same way as macrocells in cell library. For users' convenience it is recommended to give element or signal names 8 letters or less. User has to deal with the longer names proportion to the depth of hierarchical level in the simulation.	
6.	Signal line	(1) LSI input/output signal must be shown by and LSI pin number in [ ]. (2) Up to three lines can be connected to one junction point	
7.	Symbol layout	(1) A signal should flow from left to right. (2) No symbol is allowed to be placed in the first, the 13th column and in the R row. (Shadow area) (3) Keep at least one spacing row every four adjacent occupied rows to keep area for wiring. (4) Keep at least one spacing column in every other column, to assure indication of signal names.	
8.	Cross reference	(1) When signal line extends to another sheet of machine drawing, following informations are indicated automatically. K...15, B-10 →logic location to be connected →page number of logic diagram to be connected →terminal specification of signal destination K . . . . . Sink S . . . . . Source Z . . . . . 3-state output N . . . . . 3-state control	

■ DESTINATION OF TEST PATTERNS

No.	Item	Rules	Examples
1.	Timing format		



Test Rate		300 ns		
	Timing No.	Format	d(ns)	w(ns)
Input	I_0	DT	–	–
	I_1	DT	20	–
	I_2	PP	50	150
	I_3	NP	70	100
	I_4			
	I_5			
	I_6			
Output	O_1	250 ns		

[Notes] 1. Number of input timing pulses: up to 7.
2. I_0 must be DT format with d = 0.

2. Test patterns

(1) Specify signal order.
iT = input (TTL Level)
iC = input (CMOS Level)
iTO = I/O (TTL Level)
iCO = I/O (CMOS Level)
OT = output
OZ = 3-state output
ODN = open drain output

(2) Describe test pattern with following expression. Horizontal axis shows time.

Input	DT format	0,1
	PP format	0,P
	NP format	1,N
Output		H, L, Z, X, M

(Note 1) P or N shows an active pulse in PP and NP format.

(Note 2) Z. . . . .high impedance
X. . . . .indefinite or masked
M . . . . masked

(Note 3) Black can be applied for no signal change.

(3) When the same patterns are repeated, describe the following at the beginning of signal block.

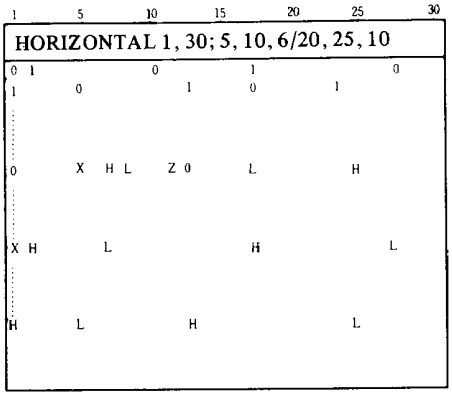
HORIZONTAL sc, ec; s_1 , e_1 , n_1 /s_2 , e_2 , n_2 /..

Signal block

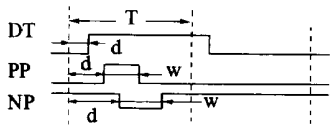
sc~ec: valid column range for test patterns
n_i : repeat number
s_i : start column of repeat
e_i : end column of repeat

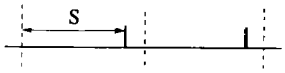
Signal name	I/O Format	Pin No.	Timing
INP–1	iT	15	I_1
INP–2	iC	7	I_3
:			
BUS–1	iTO	41	I_0
:			
OUT–1	OT	22	
:			

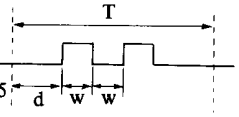
[Notes] 1. Signal name order may be free
2. BUS-1 input timing is I_0 and output strobe timing is O.

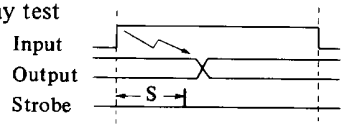


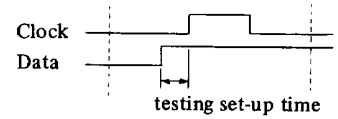
[Note] "HORIZONTAL" line shows the start column and end column of described patterns together with the conditions for repeating.

<table>
<tr><th>No.</th><th>Item</th><th>Rules</th><th>Examples</th></tr>
<tr><td>3</td><td>Fault coverage and auto-generation of test patterns</td><td>(1) Auto generated test patterns detects the faults which test patterns of user's design have not detected.
Two test patterns, of user's design and auto-generation, are available for final testing of products.
(2) Auto-generated test patterns is to increase the fault coverage. It disregards the real time function of user's hardware. Therefore, user has to design test patterns taking real time function into consideration.
When auto-diagnosis is not required, the final test of products is performed only with test patterns designed for logic verification.
Fault coverage of test patterns shall be as high as possible (final target ≧ 95%). Undetected faults by the test patterns is strongly suggested to be checked in the system test at the user's assembly line.</td><td></td></tr>
<tr><td>4</td><td>Contents of test patterns</td><td>It is requested to submit following two test patterns, functional test patterns and high speed test patterns which are generated under the timing restriction shown below respectively. In low speed application, it is allowed to omit high speed test patterns.
(1) Functional test
$T \geq 60, d \geq 5, w \geq 12.5$
$T - (d + w) \geq 5,\ 0 \leq S < T$
(2) High speed test
(a) Cycle test
To test real dynamic function.
(b) Delay test
To measure delay time along specified critical path of input to output.
(c) Skew test
To test set up time and hold time.
<table>
<tr><th></th><th>Cycle test</th><th>Delay test</th><th>Skew test</th></tr>
<tr><td>T</td><td>500</td><td>500</td><td>500</td></tr>
<tr><td>d</td><td>≥ 5</td><td>0</td><td>≥ 5</td></tr>
<tr><td>w</td><td>≥ 12.5</td><td>–</td><td>≥ 12.5</td></tr>
<tr><td>s</td><td>450</td><td>≥ 0</td><td>450</td></tr>
</table></td><td>(1) Functional test
 

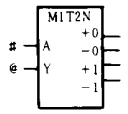
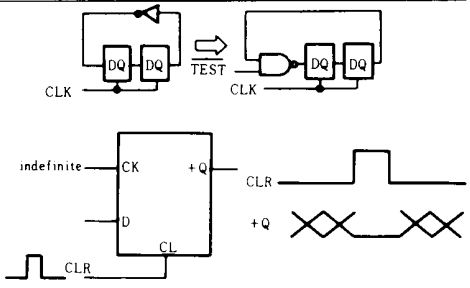


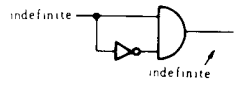
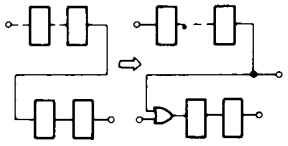
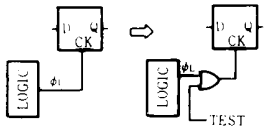
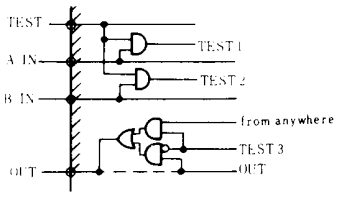
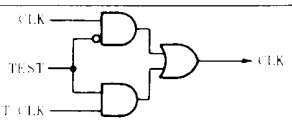
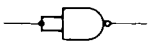
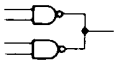
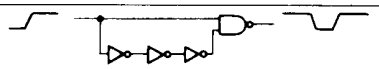
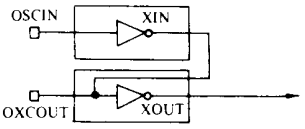
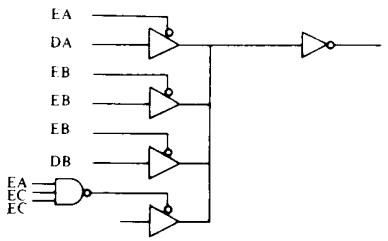
(2) High speed test
(a) Cycle test
Corresponding 40 MHz
When assuming w = 12.5


(b) Delay test


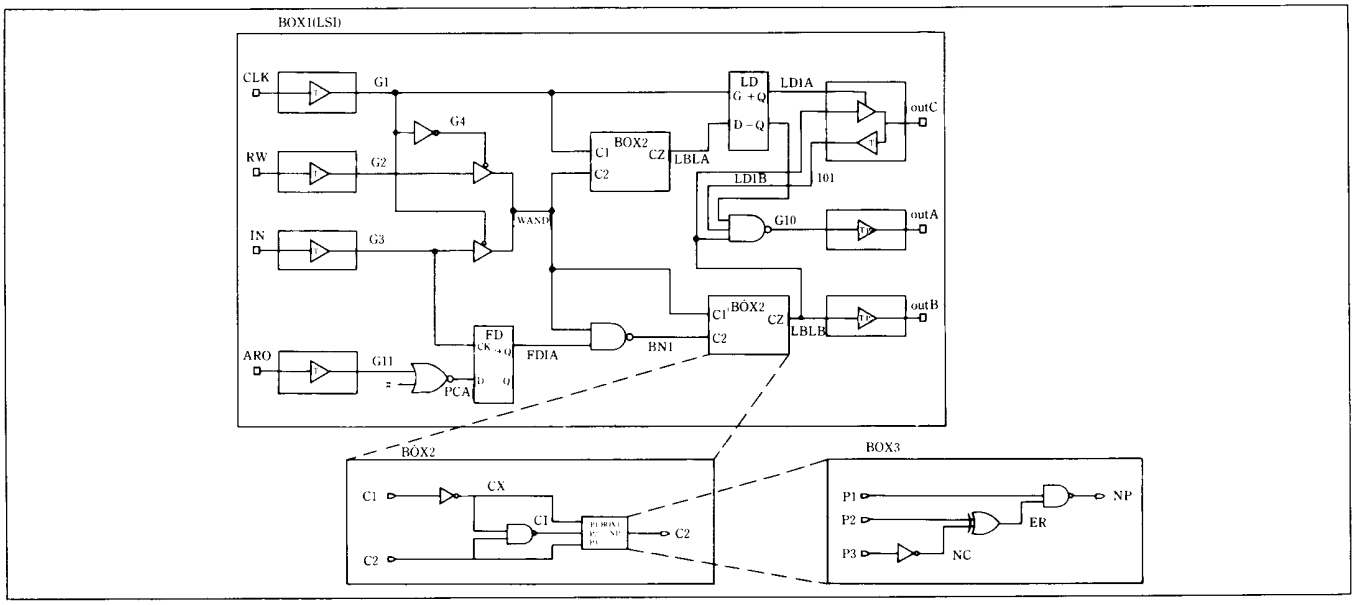
(c) Skew test

</td></tr>
<tr><td>5</td><td>Limitation of test patterns</td><td>(1) Up to 10 sets of test patterns.
(2) Up to 30000 test cycles after expanding the repeat in a set of test patterns.
(3) Total steps for all sets of test patterns.
(Repeat is counted as 1 time) is limited as shown in table on right.</td><td>
<table>
<tr><th></th><th>Functional test</th><th>High speed test</th></tr>
<tr><td>E08~E43</td><td>4000</td><td rowspan="3">4000</td></tr>
<tr><td>E58</td><td>6000</td></tr>
<tr><td>E75</td><td>8000</td></tr>
<tr><td>E101</td><td>11000</td><td rowspan="4">8000</td></tr>
<tr><td>E130</td><td>15000</td></tr>
<tr><td>E182</td><td>22000</td></tr>
<tr><td>E240</td><td>30000</td></tr>
</table></td></tr>
</table>

■ NOTES FOR LOGIC DESIGN

No.	Item	Notes	
1.	Utilization	Must be 90% or less in order to place and route successfully. When auto-diagnosis is used, must be 85% or less. Auto-diagnosis causes overhead. You have to take overhead into consideration when auto-diagnosis is required. The estimation of overhead depends on the numbers of latches, flip-flops and shift resistors (N_F). The right equation shows the calculation.	Maximum gate counts to be used actually. E08: 700 (660) E11: 1050 (990) E15: 1360 (1290) E22: 1960 (1850) E33: 2970 (2800) E43: 3880 (3660) E58: 5240 (4950) E75: 6740 (6360) E101: 9070 (8560) E130: 11710 (11060) E182: 16360 (15450) E240: 21620 (20420) ( ): When auto-diagnosis is used. [Maximum gate counts] ≧ (gate counts in user's logic) + 1.7 × N_F
2.	Auto-diagnosis	(1) Need two test dedicated pins. (2) Use latch, flip-flop and shift resistor with scan function.	
3.	Gate delay	Gate delay is obtained more accurately after place and route. However rough estimate should also be done using the equations shown right to prevent timing design errors in the earlier design phase. Effective Fan Out is calculated as sum of Normalized Loading Factor of the output node. These equation may contain the design margin a little bit.	$t_{PLH} = t_{OLH} + K_{LH} \cdot C_L$ $t_{PHL} = t_{OHL} + K_{HL} \cdot C_L$ Where, for internal gates $C_L = 0.4 \times EFO$ $EFO = \Sigma NLF$ Variational range: Min = 0.35 x typ Max = 1.8 x typ (Ta = –20 to +75°C, V_{CC} = 5V±5%)
4.	Maximum fanout	A clock driver, which drives CK inputs of FF's, has a restriction on the number of applicable fanouts, though the other signals have no limitation if lower speed is acceptable.	○ Max. Fanout of CK driver Power Inverter . . . 20/30/40 The others . . . . . 10 ○ The other signals 24
5.	Automatic Modification of unconnected inputs of macro	When an input of a macro is left unconnected, the automatic router connects it to either V_{CC} ("1" level) or GND ("0" level). The macrocell list shows which input of each macro will be connected to which level. An input of AND or NAND gates will be connected to V_{CC}, and that of OR or NOR gates to GND, even though these are not indicated in the list. "@" beside an input shows that the input will be connected to V_{CC}, and "#" to GND. It is not allowed to leave an input unconnected dropping "@" nor "#" except the cases of AND, NAND, OR or NOR.	 When inputs are left open, input A will be fixed to "0" input Y will be fixed to "1".
6.	Simultaneous Turn on/off of Output Buffers	The number of output buffers which simultaneously change their output levels must be equal to or less than the figures in the table respectively depending on the buffers.	Buffer: OT, $\overline{O}Z$, $\overline{O}DN$ — max. number: 8 Buffer: OTR, OZR, ODNR — max. number: 12
7.	Testing	(1) All the logic must be able to be initialized by external inputs. (2) Restriction due to the Simulator. (a) When one or more inputs associated with FF such as CK, CL and PR is indefinite the output is also indefinite. For example, output of FF will not be fixed when CK input is indefinite even if it is quite evident logically that CK input is stable either in high or low level.	

No.	Item	Notes	
		(b) For the given logical variables X, Y, suppose that there is the following relation between them $X = \overline{Y}$ When X or Y is indefinite, both X + Y and X·Y are also indefinite contrary to the theoretical result.	
		(3) It is preferable to split a multistage shift registers and/or counters to provide test signals in the proper positions in order to improve the efficiency of testing.	
		(4) It is preferable to provide test clock in addition to the original clock whose frequency is much lower than other clocks such as a system clock.	
		(5) The figure shows an example of additional test logic to generate several test signals from a single TEST pin, which is helpful when we suffer from the shortage of pins. Another example shown here is to share the output pin to monitor another internal signal.	
		(6) It is very important to do timing design of test logic as well. Is test logic speed OK? Won't unexpected events occur at the transition time from test to normal mode or contrary?	 Unexpected glitch will occur when TEST turns on/off.
8.	Others	(1) As far as a macro is concerned, one signal is prohibited to be employed to multi-input terminals.	
		(2) Output-to-output connection is not allowed except among 3-state buffers.	
		(3) A chopper circuit using gate delay is prohibited.	
		(4) Oscillator circuit should be built as shown. OSC IN and OSC OUT pins should be assigned next to the pins which never change their levels, such as V_{CC} and GND.	
		(5) Internal bus lines should be prevented from floating. Dummy 3-state buffer is recommended to be added.	

■ LOGIC DIAGRAM



■ EXAMPLE OF LOGIC DESCRIPTION

LSI profile

Device Type, master type, package type

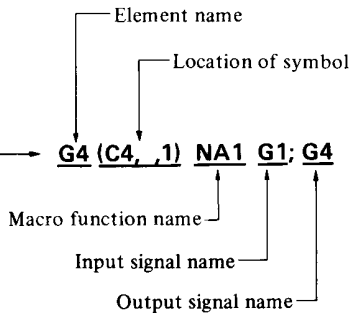
```
BEGIN PROFILE
  BEGIN PRODUCT BOX1
    IMPLEMENT GATEARRAY SERIES (HG62E43) ARRAY (HG62E)
    ROOTBLOCK BOX1
    ARRANGE DP40B0
    PACKAGE DP40
```

Pin assignment

```
  BIGIN PIN
    1  INPUT   RW
    2  INOUT   OUTC
    3  OUTPUT  OUTB
    4  OUTPUT  OUTA
   10  INPUT   IN
   11  INPUT   CLK
   14  INPUT   ARO
    END PIN
  END PRODUCT
END PROFILE
```

Schematic description

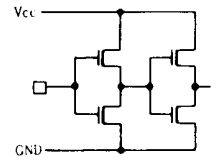
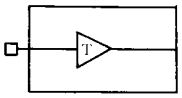
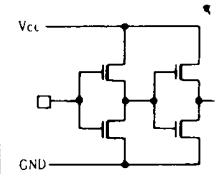
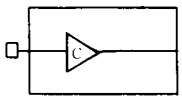
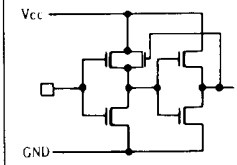
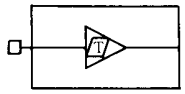
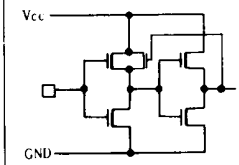
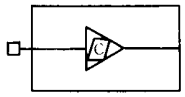
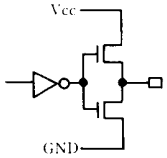
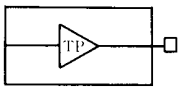
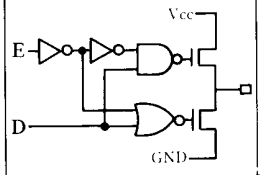
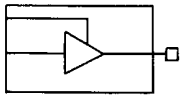
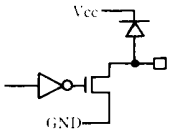
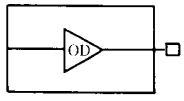
```
BIGIN LOGIC
  BEGIN BLOCK BOX1
    INTERFACE RW, IN, CLK, AR0; OUTB, OUTA; OUTC
    BEGIN NETLIST
      G11    (L3, ,1)    IT     ARO; G11
      G1     (B3, ,1)    IT     CLK; G1
      G2     (D3, ,1)    IT     RW; G2
      G3     (F3, ,1)    IT     IN; G3
      AR     (L4, ,1)    NR2    G11; PCA
      G4     (C4, 1)     NA1    G1; G4
      FD1    (J5, ,1)    FD     G3, PCA; FD1A
      G5     (D5, ,1)    ANZ    G4, G2; WAND
      G6     (F5, ,1)    ANZ    G1, G3; WAND
      BN1    (J6, ,1)    NA2    WAND, FD1A,; BN1
      LBL2   (G7, ,1)    BOX2   BN1, WAND; LBLB
      LBL1   (C7, ,1)    BOX2   WAND, G1; LBLA
      LD1    (B8, ,1)    LD     G1, LBLA; LD1A, LD1B
      G8     (E11, ,1)   OT     C10; OUTA
      G7     (G9, ,1)    OT     LBLB; OUTB
      G10    (E9, ,1)    NA3    IO1, LD1B, LBLB; G10
      G9     (C11, ,1)   ITO    LDIA, LBLB; IO1; OUTC
    END NETLIST
  END BLOCK
```

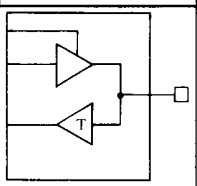
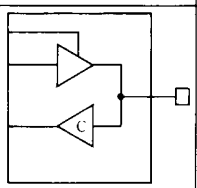
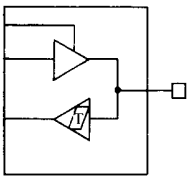
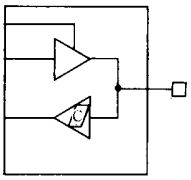
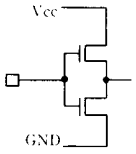
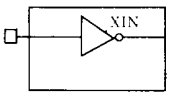
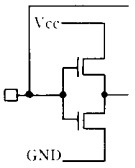
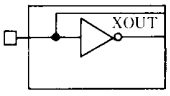
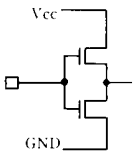
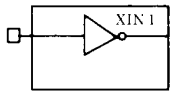
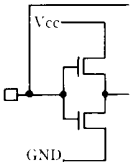
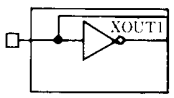


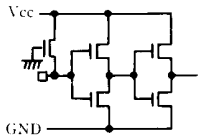
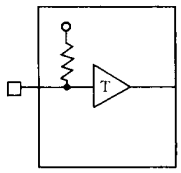
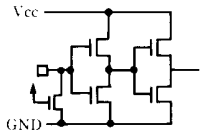
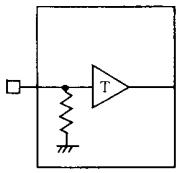
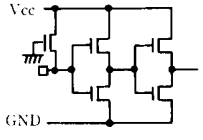
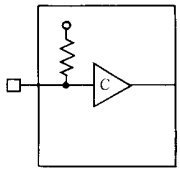
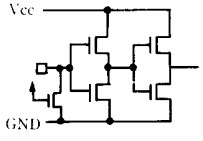
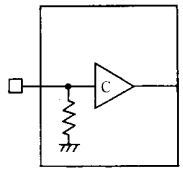
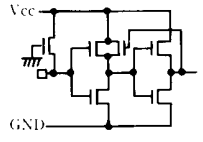
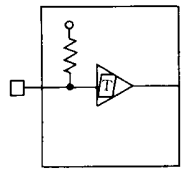
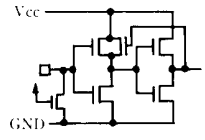
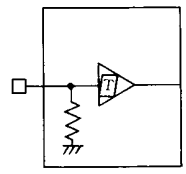
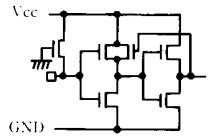
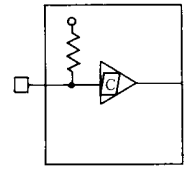
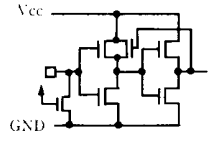
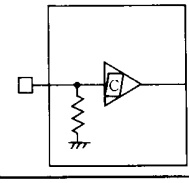
	BEGIN BLOCK BOX2 INTERFACE C2, C1; CZ SHAPE; J4, 2, A3 BEGIN NETLIST CX (D3, ,2) NA1 C1; CX CY (F5, ,2) NA2 CX, C2; CY PBK1 (F7, ,2) BOX3 C2, CY, CX; CZ END NETLIST END BLOCK	Description of BOX2 (User defined macro)
	BEGIN BLOCK BOX3 INTERFACE P3, P2, P1; NP SHAPE; J6, 1, A3 BEGIN NETLIST NG (E3, ,3) NA1 P3; NG ER (D4, ,3) EOR P2, NG; ER NP (B5, ,3) NAP2 P1, ER; NP END NETLIST END BLOCK END LOGIC	Description of BOX3 (User defined macro)
Test patterns	BEGIN TEST BEGIN PATTERN CASE1 BLOCKNAME BOX1 TIMING TRATE (150. 0N) STRB (120. 0N) BEGIN SIGNAL AR0 DT (20. 0N) CLK DT (0. 0N) IN PP (50. 0N, 100. 0N) OUTA OUTB OUTC DT (0. 0N) RW NP (50. 0N, 100. 0N) END SIGNAL	Definition of timing
	BEGIN VECTOR HORIZONTAL 1, 1010101 AR0 1100101 CLK P0P0P0P IN LLLLLLL OUTA LLLLLLL OUTB 111H1H1 OUTC N1N1111 RW END VECTOR END PATTERN END TEST	Description of test patterns In this case, the horizontal axis shows time, but there is another way of description that the vertical axis shows time.
Verification	BEGIN VERIFY BEGIN LOGSIM CASE1 TESTNAME CASE1 DELAY TYPICAL LOADC FANOUT DEFAULT STRB (120. 0N) BEGIN MONITOR MON1 BOX1. LBL1. CX STRB (140. 0N) BOX1. LBL2. CX STRB (140. 0N) END MONITOR COMPARE SRL SIGNAL (EXTERNAL' MONITOR (MON1)) SRF SIGNAL (EXTERNAL, MONITOR (MON1)) ERROR CONFLICT' TIME (10, 0N, 10. 0N) FAULT SEPARATE (1,999), ASSUME (1), DETECT (2), MODIFY STOP 7 END LOGSIM	Condition of logic simulation
	BEGIN TIMING TIM1 TESTNAME CASE1 DELAY TYPICAL LOADC ROUTING END TIMING END VERIFY	Specification of timing verification

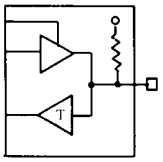
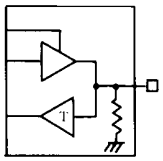
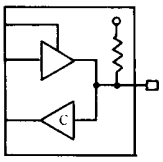
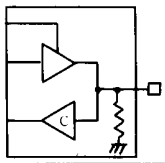
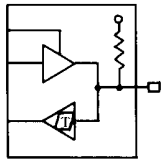
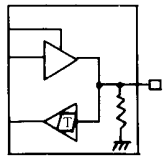
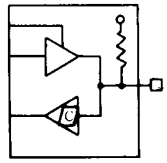
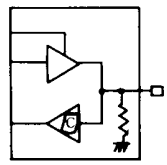
■ MACRO CELL LIBRARY

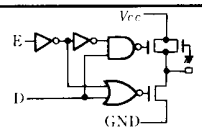
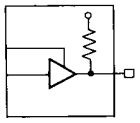
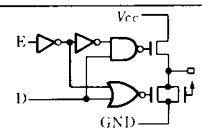
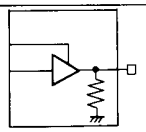
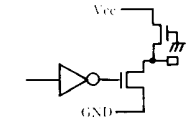
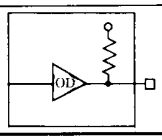
1. Input/Output Buffers

Macrocell: Function / Macro Function Name	Macrocell: Equivalent Circuit	Equivalent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Symbol No.	Delay: t_{PLH} (ns) t_{OLH}	Delay: t_{PLH} (ns) k_{LH}	Delay: t_{PHL} (ns) t_{OHL}	Delay: t_{PHL} (ns) k_{HL}
Input Buffer TTL Level IT		–	–			D1	1.5	0.4	2.0	0.9
Input Buffer CMOS Level IC		–	–			D1	2.0	0.4	2.0	0.8
SCHMITT TTL Level ITS		–	–			D1	2.5	1.3	9.2	2.0
SCHMITT CMOS Level ICS		–	–			D1	2.0	0.6	3.6	1.1
OUTPUT OT		–	1.2			D1	2.0	0.12	2.3	0.1
3-State OUTPUT OZ		–	1.2 1.4			(D) D1 (E)	2.2 — 2.6	0.12	2.3 — 2.5	0.1
Open Drain Output ODN		–	1.2			D1	–	–	2.3	0.1

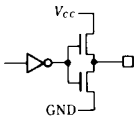
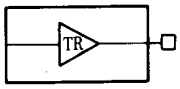
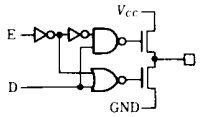
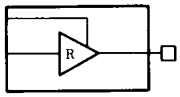
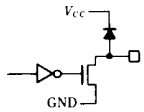
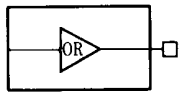
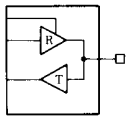
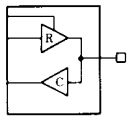
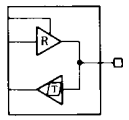
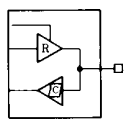
Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Symbol No.	Delay			
Function	Equivalent Circuit						t_{PLH} (ns)		t_{PHL} (ns)	
Macro Function Name							t_{OLH}	k_{LH}	t_{OHL}	k_{HL}
I/O Buffer TTL Level ITO	Output See "3-state" Input See "Input Buffer"	–	1.2 1.4			D2	Output See "3-state" Input See "Input Buffer"			
I/O Buffer CMOS Level ICO	Output See "3-state" Input See "Input Buffer"	–	1.2 1.4			D2	Output See "3-state" Input See "Input Buffer"			
I/O Buffer TTL SCHMITT Level ITSO	Output See "3-state" Input See "Input Buffer"	–	1.2 1.4			D2	Output See "3-state" Input See "Input Buffer"			
I/O Buffer CMOS SCHMITT Level ICSO	Output See "3-state" Input See "Input Buffer"	–	1.2 1.4			D2	Output See "3-state" Input See "Input Buffer"			
OSC In 2MHz to 20MHz XIN		–	–			D1	3.1	0.8	3.2	0.8
OSC Out 2MHz to 20MHz XOUT		–	–			D1	4.0	1.2	2.5	0.9
OSC In 32kHz to 400kHz XIN1		–	–			D1	3.1	40	3.2	40
OSC Out 32kHz to 400kHz XOUT1		–	–			D1	4.0	1.2	2.5	0.9

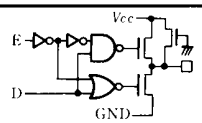
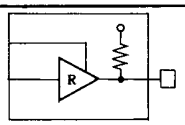
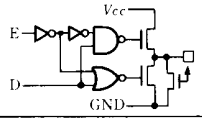
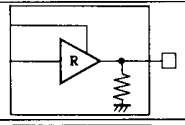
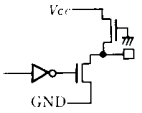
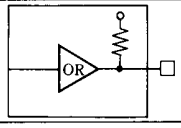
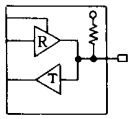
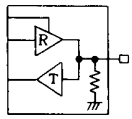
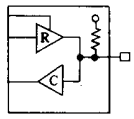
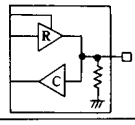
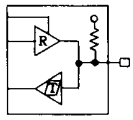
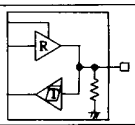
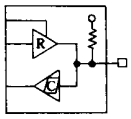
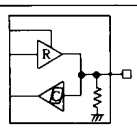
Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Symbol No.	Delay			
Function	Equivalent Circuit						t_{PLH} (ns)		t_{PHL} (ns)	
Macro Function Name							t_{OLH}	k_{LH}	t_{OHL}	k_{HL}
Input Buffer TTL Level with Pull-Up ITU		–	–			D2	1.5	0.4	2.0	0.9
Input Buffer TTL Level with Pull-Down ITD		–	–			D2	1.5	0.4	2.0	0.9
Input Buffer CMOS Level with Pull-Up ICU		–	–			D2	2.0	0.4	2.0	0.8
Input Buffer CMOS Level with Pull-Down ICD		–	–			D2	2.0	0.4	2.0	0.8
Schmitt TTL Level with Pull-Up ITSU		–	–			D2	2.5	1.3	9.2	2.0
Schmitt TTL Level with Pull-Down ITSD		–	–			D2	2.5	1.3	9.2	2.0
Schmitt CMOS Level with Pull-Up ICSU		–	–			D2	2.0	0.6	3.6	1.1
Schmitt CMOS Level with Pull-Down ICSD		–	–			D2	2.0	0.6	3.6	1.1

Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Symbol No.	Delay			
Function	Equivalent Circuit						t_{PLH} (ns)		t_{PHL} (ns)	
Macro Function Name							t_{OLH}	k_{LH}	t_{OHL}	k_{HL}
I/O Buffer TTL Level with Pull-Up ITOU	Output See "3-state"	–	1.2 1.4			D2	Output See "3-state"			
	Input See "Input Buffer"						Input See "Input Buffer"			
I/O Buffer TTL Level with Pull-Down ITOD	Output See "3-state"	–	1.2 1.4			D2	Output See "3-state"			
	Input See "Input Buffer"						Input See "Input Buffer"			
I/O Buffer CMOS Level with Pull-Up ICOU	Output See "3-state"	–	1.2 1.4			D2	Output See "3-state"			
	Input See "Input Buffer"						Input See "Input Buffer"			
I/O Buffer CMOS Level with Pull-Down ICOD	Output See "3-state"	–	1.2 1.4			D2	Output See "3-state"			
	Input See "Input Buffer"						Input See "Input Buffer"			
I/O Buffer TTL Schmitt Level with Pull-Up ITSOU	Output See "3-state"	–	1.2 1.4			D2	Output See "3-state"			
	Input See "Input Buffer"						Input See "Input Buffer"			
I/O Buffer TTL Schmitt Level with Pull-Down ITSOD	Output See "3-state"	–	1.2 1.4			D2	Output See "3-state"			
	Input See "Input Buffer"						Input See "Input Buffer"			
I/O Buffer CMOS Schmitt Level with Pull-Up ICSOU	Output See "3-state"	–	1.2 1.4			D2	Output See "3-state"			
	Input See "Input Buffer"						Input See "Input Buffer"			
I/O Buffer CMOS Schmitt Level with Pull-Down ICSOD	Output See "3-state"	–	1.2 1.4			D2	Output See "3-state"			
	Input See "Input Buffer"						Input See "Input Buffer"			

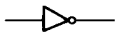
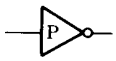
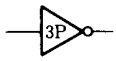
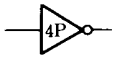
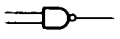
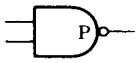
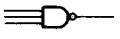
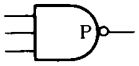
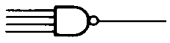
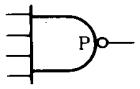
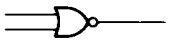
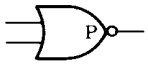
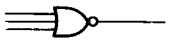
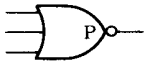
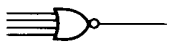
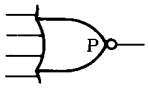
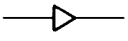
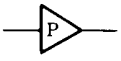
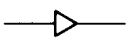
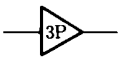
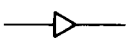
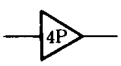
Macrocell: Function / Macro Function Name	Macrocell: Equivalent Circuit	Equivalent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Symbol No.	Delay: t_{PLH} (ns) t_{OLH}	Delay: t_{PLH} (ns) k_{LH}	Delay: t_{PHL} (ns) t_{OHL}	Delay: t_{PHL} (ns) k_{HL}
3-State Output with Pull-Up OZU		–	1.2 1.4			(D) D2 (D)	2.2 2.6	0.12	2.3 2.5	0.1
3-State Output with Pull-Down OZD		–	1.2 1.4			(D) D2 (E)	2.2 2.6	0.12	2.3 2.5	0.1
Open Drain Output with Pull-Up ODNU		–	1.2			D2	–	–	2.3	0.1

GND Noise Reduction Buffers

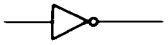
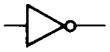
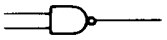
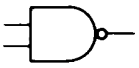
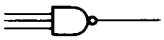
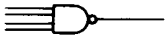
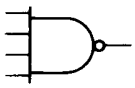
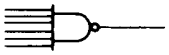
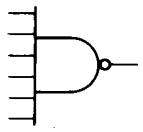
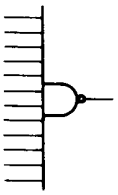
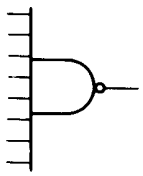
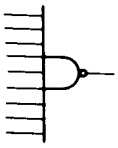
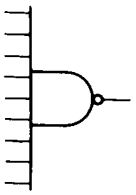
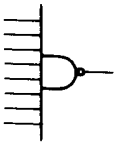
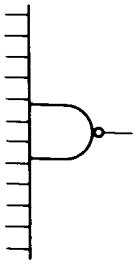
Macrocell: Function / Macro Function Name	Macrocell: Equivalent Circuit	Equivalent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Symbol No	Delay: t_{PLH}(ns) t_{OLH}	Delay: t_{PLH}(ns) k_{LH}	Delay: t_{PHL}(ns) t_{OHL}	Delay: t_{PHL}(ns) k_{HL}
Totem-pole output OTR		–	1.2			D1	3.7	0.12	12.6	0.12
3-state output OZR		–	1.2 1.4			(D) D1 (E)	3.2 3.6	0.12	6.2 6.4	0.1
Open-drain output ODNR		–	1.2			D1	–	–	6.2	0.1
I/O buffer TTL level ITOR	Output See "3-state" Input See "Input buffers"	–	1.2 1.4			D2	Output See "3-state" (OZR) Input See "Input buffers"			
I/O buffer CMOS level ICOR	Output See "3-state" Input See "Input buffers"	–	1.2 1.4			D2	Output See "3-state" (OZR) Input See "Input buffers"			
I/O buffer TTL Schmitt-trigger ITSOR	Output See "3-state" Input See "Input buffers"	–	1.2 1.4			D2	Output See "3-state" (OZR) Input See "Input buffers"			
I/O buffer CMOS Schmitt-trigger ICSOR	Output See "3-state" Input See "Input buffers"	–	1.2 1.4			D2	Output See "3-state" (OZR) Input See "Input buffers"			

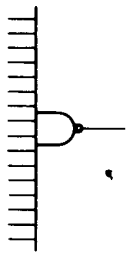
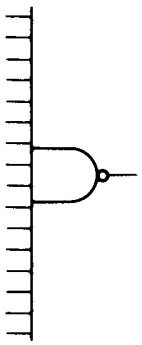
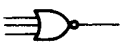
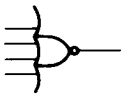
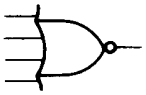
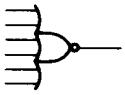
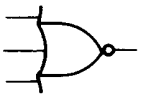
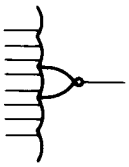
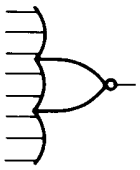
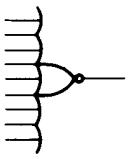
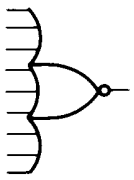
Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Symbol No.	Delay			
Function	Equivalent Circuit						t_{PLH}(ns)		t_{PHL}(ns)	
Macro Function Name							t_{OLH}	k_{LH}	t_{OHL}	k_{HL}
3-state output with Pull-Up OZRU		–	1.2 1.4			(D) D2 (E)	3.2 3.6	0.12	6.2 6.4	0.1
3-state output with Pull-Down OZRD		–	1.2 1.4			(D) D2 (E)	3.2 3.6	0.12	6.2 6.4	0.1
Open-drain output with Pull-Up ODNRU		–	1.2			D2	–	–	6.2	0.1
I/O buffer TTL level with Pull-Up ITORU	Output See "3-state"	–	1.2 1.4			D2	Output See "3-state" (OZR)			
	Input See "Input buffers"						Input See "Input buffers"			
I/O buffer TTL level with Pull-Down ITORD	Output See "3-state"	–	1.2 1.4			D2	Output See "3-state" (OZR)			
	Input See "Input buffers"						Input See "Input buffers"			
I/O buffer CMOS level with Pull-Up ICORU	Output See "3-state"	–	1.2 1.4			D2	Output See "3-state" (OZR)			
	Input See "Input buffers"						Input See "Input buffers"			
I/O buffer CMOS level with Pull-Down ICORD	Output See "3-state"	–	1.2 1.4			D2	Output See "3-state" (OZR)			
	Input See "Input buffers"						Input See "Input buffers"			
I/O buffer TTL Schmitt-trigger with Pull-Up ITSORU	Output See "3-state"	–	1.2 1.4			D2	Output See "3-state" (OZR)			
	Input See "Input buffers"						Input See "Input buffers"			
I/O buffer TTL Schmitt-trigger with Pull-Down ITSORD	Output See "3-state"	–	1.2 1.4			D2	Output See "3-state" (OZR)			
	Input See "Input buffers"						Input See "Input buffers"			
I/O buffer CMOS Schmitt-trigger with Pull-Up ICSORU	Output See "3-state"	–	1.2 1.4			D2	Output See "3-state" (OZR)			
	Input See "Input buffers"						Input See "Input buffers"			
I/O buffer CMOS Schmitt-trigger with Pull-Down ICSORD	Output See "3-state"	–	1.2 1.4			D2	Output See "3-state" (OZR)			
	Input See "Input buffers"						Input See "Input buffers"			

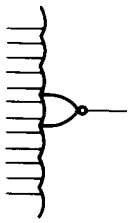
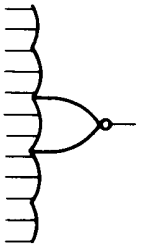
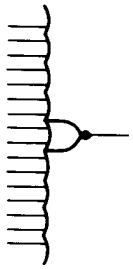
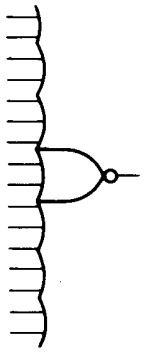
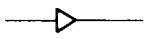
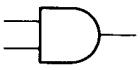
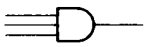
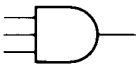
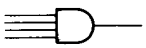
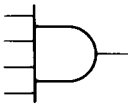
2. Power Gates

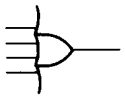
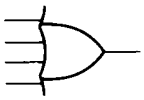
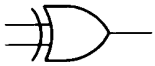
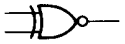
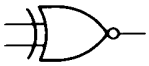
Macrocell: Function / Macro Function Name	Macrocell: Equivalent Circuit	Equivalent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Symbol No.	Delay: t_{PLH}(ns) t_{OLH}	Delay: t_{PLH}(ns) k_{LH}	Delay: t_{PHL}(ns) t_{OHL}	Delay: t_{PHL}(ns) k_{HL}
Power inverter NAP1		1	1.2	@		–	0.3	0.6	0.3	0.5
Power inverter NA3P		2	1.4	@		–	0.3	0.4	0.6	0.4
Power inverter NA4P		2	1.6	@		–	0.3	0.3	0.6	0.3
2-input power NAND NAP2		2	1.2	@		–	0.3	0.6	0.4	0.6
3-input power NAND NAP3		3	1.2	@		–	0.3	0.6	0.4	0.7
4-input power NOR NAP4		4	1.2	@		–	0.3	0.6	0.4	0.8
2-input power NOR NRP2		2	1.2	#		–	0.4	1.0	0.6	0.5
3-input power NOR NRP3		3	1.2	#		–	0.4	1.4	0.6	0.5
4-input power NOR NRP4		4	1.2	#		–	0.5	1.9	0.6	0.5
Power buffer ANP		2	1.0	@		–	0.8	0.6	0.6	0.5
Power buffer AN3P		3	1.2	@		–	0.7	0.4	0.5	0.4
Power buffer AN4P		3	1.2	@		–	0.8	0.3	0.6	0.3

3. GATES

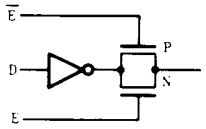
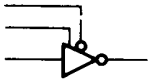
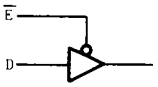
Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Symbol No.	Delay			
Function	Equivalent Circuit						t_{PLH} (ns)		t_{PHL} (ns)	
Macro Function Name							t_{OLH}	k_{LH}	t_{OHL}	k_{HL}
Inverter NA1		1	1	@		–	0.2	1.2	0.3	0.9
2-Input NAND NA2		1	1	@		–	0.2	1.2	0.3	1.2
3-Input NAND NA3		2	1	@		–	0.2	1.2	0.3	1.3
4-Input NAND NA4		2	1	@		–	0.3	1.2	0.3	1.5
6-Input NAND NA6		5	1	@		–	0.8	1.2	1.5	0.9
8-Input NAND NA8		6	1	@		–	0.9	1.2	1.6	0.9
9-Input NAND NA9		7	1	@		–	0.9	1.2	1.6	0.9
12-Input NAND NA12		8	1	@		–	0.9	1.2	1.9	0.9

Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Symbol No.	Delay			
Function	Equivalent Circuit						t_{PLH} (ns)		t_{PHL} (ns)	
Macro Function Name							t_{OLH}	k_{LH}	t_{OHL}	k_{HL}
16-Input NAND NA16		11	1	@		–	0.9	1.2	1.6	1.2
2-Input NOR NR2		1	1	#		–	0.3	2.0	0.7	0.9
3-Input NOR NR3		2	1	#		–	0.4	2.8	0.7	0.9
4-Input NOR NR4		2	1	#		–	0.4	3.7	0.7	0.9
6-Input NOR NR6		5	1	#		–	1.2	1.2	1.0	0.9
8-Input NOR NR8		6	1	#		–	1.3	1.2	1.0	0.9
9-Input NOR NR9		7	1	#		–	1.3	1.2	1.0	0.9

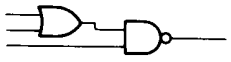
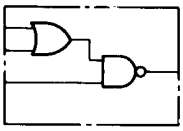
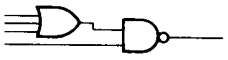
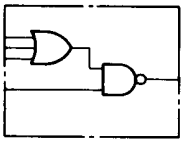
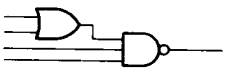
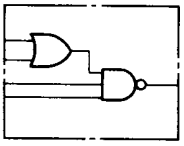
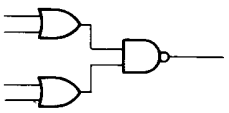
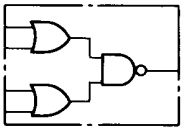
Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Symbol No.	Delay			
Function	Equivalent Circuit						t_{PLH} (ns)		t_{PHL} (ns)	
Macro Function Name							t_{OLH}	k_{LH}	t_{OHL}	k_{HL}
12-Input NOR NR12		8	1	#		–	1.4	1.2	1.0	0.9
16-Input NOR NR16		11	1	#		–	1.3	2.0	1.0	0.9
Buffer AN1		1	1	@		–	0.6	1.2	0.5	0.9
2-input AND AN2		2	1	@		–	0.7	1.2	0.5	0.9
3-input AND AN3		2	1	@		–	0.9	1.2	0.7	0.9
4-input AND AN4		3	1	@		–	1.0	1.2	0.8	0.9
2-input OR OR2		2	1	#		–	0.7	1.2	0.7	0.9

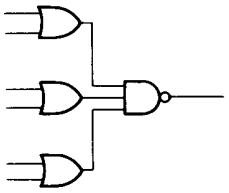
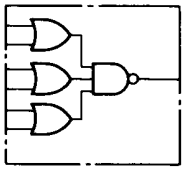
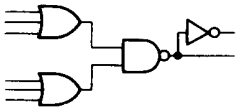
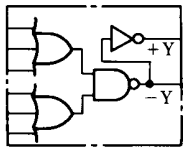
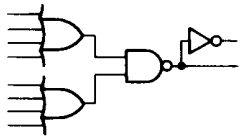
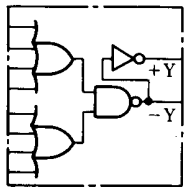
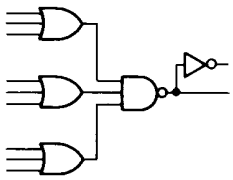
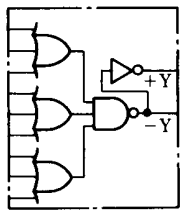
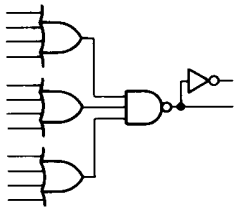
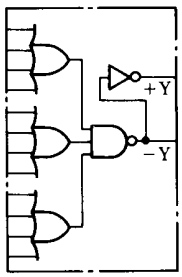
Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Symbol No.	Delay			
Function	Equivalent Circuit						t_{PLH}(ns)		t_{PHL}(ns)	
Macro Function Name							t_{OLH}	k_{LH}	t_{OHL}	k_{HL}
3-input OR OR3		2	1	#		–	0.7	1.2	0.9	0.9
4-input OR OR4		3	1	#		–	0.7	1.2	1.2	0.9
2-input EOR EOR		3	1.2	#		–	1.0	2.0	1.1	0.9
2-input ENOR ENR		3	1.2	#		–	0.9	1.2	1.0	1.2

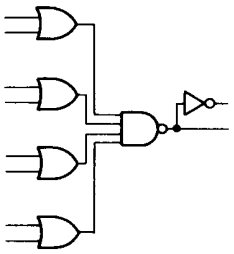
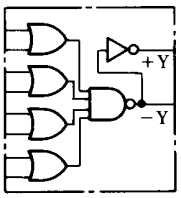
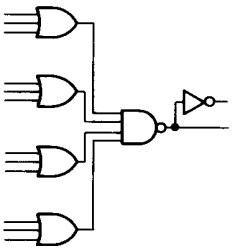
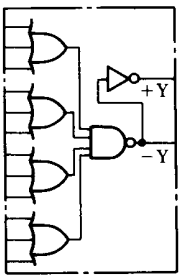
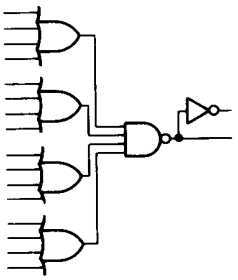
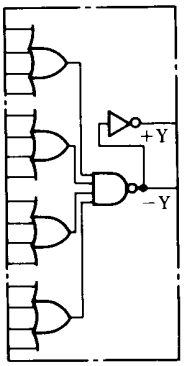
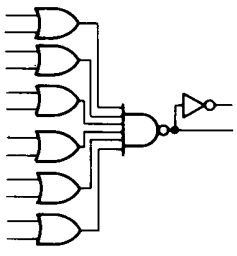
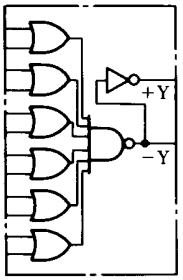
4. 3-STATE GATES

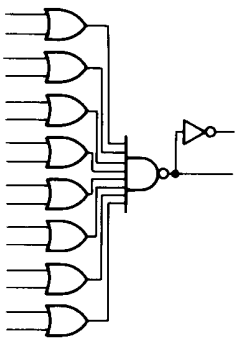
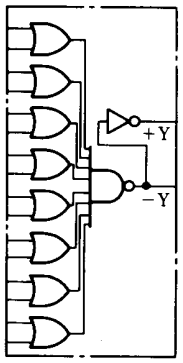
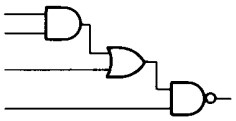
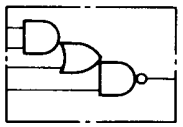
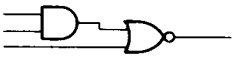
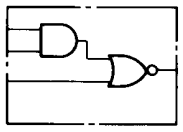
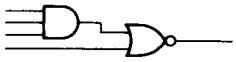
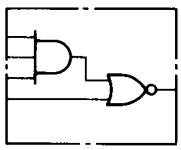
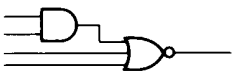
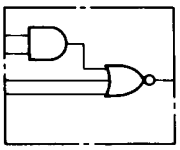
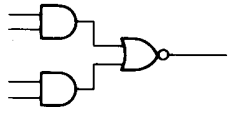
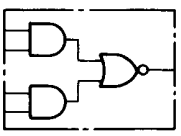
Macrocell: Function / Function Name	Macrocell: Equivalent Circuit	Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{PLH}(ns) t_{OLH}	Delay: t_{PLH}(ns) K_{LH}	Delay: t_{PHL}(ns) t_{OHL}	Delay: t_{PHL}(ns) K_{HL}
3-State Inverter (Internal) NAZ		1	1	@		–	D		0.4	2.0	0.8	1.2
							E/$\overline{E}$		0.2		0.3	
3-State Buffer (Internal) ANZ		3	1.2	# @		–	D		0.8	1.2	0.7	0.9
							E		1.0		1.0	

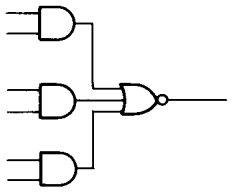
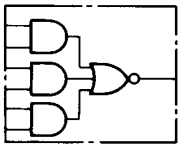
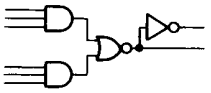
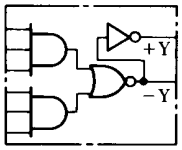
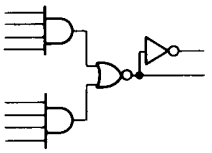
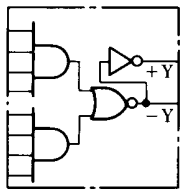
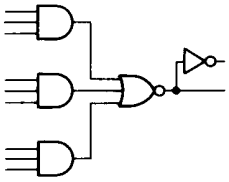
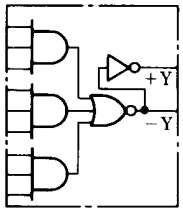
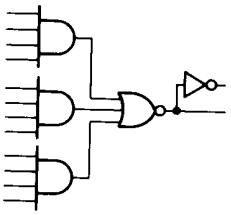
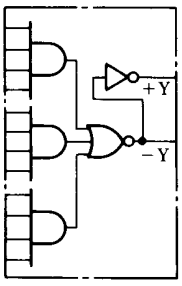
5. AND-NOR, OR-AND GATES

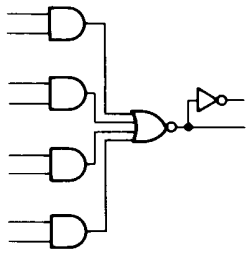
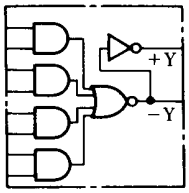
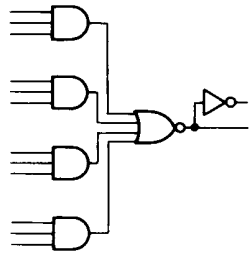
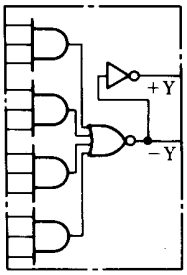
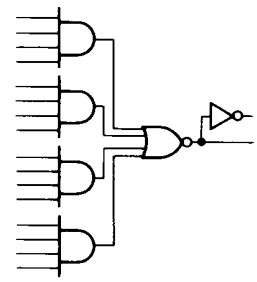
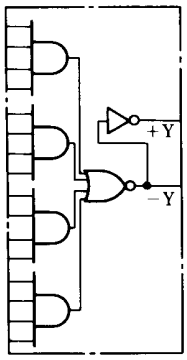
Macrocell: Function / Function Name	Macrocell: Equivalent circuit	Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{PLH}(ns) t_{OLH}	Delay: t_{PLH}(ns) K_{LH}	Delay: t_{PHL}(ns) t_{OHL}	Delay: t_{PHL}(ns) K_{HL}
2-OR-NAND NAR23		2	1	# # @		A1	OR input		0.4	2.0	0.8	1.2
							NAND input		0.3		0.8	
3-OR-NAND NAR34		2	1	# # # @		A2	OR input		0.5	2.8	0.8	1.2
							NAND input		0.4		0.8	
2-OR-3NAND NAR24		2	1	# # @ @		A2	OR input		0.4	2.0	0.9	1.3
							NAND input		0.4		0.8	
2-Wide 2-Input OR-NAND NA2R2		2	1	# # # #		A1			0.4	2.0	0.8	1.2

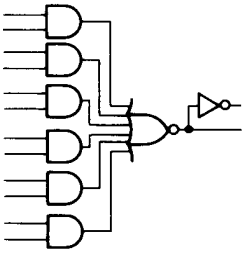
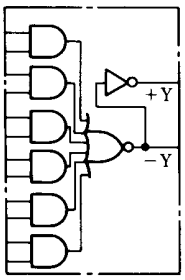
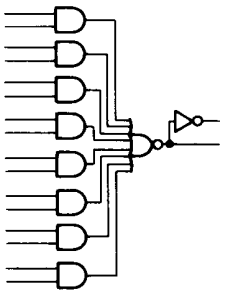
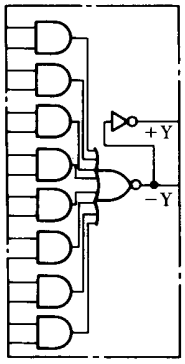
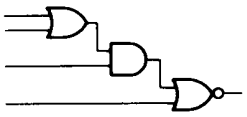
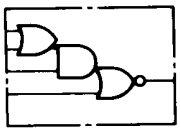
Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay				
Function / Function Name	Equivalent Circuit						Input Name	Output Name	t_{PLH}(ns)		t_{PHL}(ns)	
									t_{OLH}	K_{LH}	t_{OHL}	K_{HL}
3-Wide 3-Input OR-NAND NA3R2		3	1	# # # # #		A3			0.4	2.0	0.9	1.3
2-Wide 3-Input OR-NAND NA2R3N		4	1	# # # # # #		A2		NAND	0.8	2.8	1.0	1.2
								In-verter	1.2	1.2	1.1	0.9
2-Wide 4-Input OR-NAND NA2R4N		5	1	# # # # # # # # #		A4		NAND	1.1	3.7	1.0	1.2
								In-verter	1.2	1.2	1.4	0.9
3-Wide 3-Input OR-NAND NA3R3N		5	1	# # # # # # # # #				NAND	1.0	2.8	1.2	1.3
								In-verter	1.4	1.2	1.3	0.9
3-Wide 4-Input OR-NAND NA3R4N		7	1	# # # # # # # # # #				NAND	1.4	3.7	1.2	1.3
								In-verter	1.4	1.2	1.7	0.9

Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay					
Function / Function Name	Equivalent Circuit						Input Name	Output Name	t_{PLH}(ns)		t_{PHL}(ns)	
									t_{OLH}	K_{LH}	t_{OHL}	K_{HL}
4-Wide 2-Input OR-NAND		5	1	@ @ @ @ @ @ @ @		A4		NAND	0.7	2.0	1.3	1.5
								Inverter	1.5	1.2	1.0	0.9
NA4R2N												
4-Wide 3-Input OR-NAND		7	1	# # # # # # # # # # #				NAND	1.2	2.8	1.6	1.5
								Inverter	1.8	1.2	1.5	0.9
NA4R3N												
4-Wide 4-Input OR-NAND		9	1	# # # # # # # # # # # # #		A5		NAND	1.7	3.7	1.6	1.5
								Inverter	1.8	1.2	2.0	0.9
NA4R4N												
6-Wide 2-Input OR-NAND		8	1	@ @ @ @ @ @ @ @ @ @ @ @ @				NAND	1.4	1.2	1.6	0.9
								Inverter	1.3	2.0	1.2	0.9
NA6R2N												

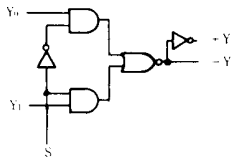
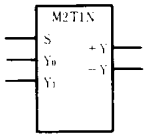
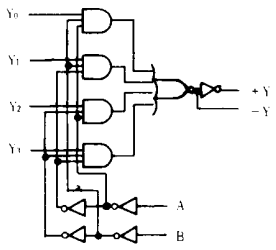
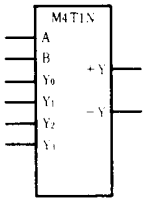
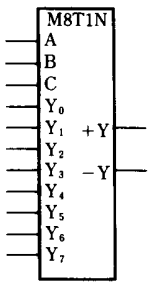
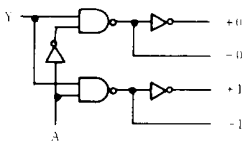
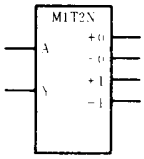
Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay					
Function / Function Name	Equivalent Circuit						Input Name	Output Name	t_{PLH}(ns)		t_{PHL}(ns)	
									t_{OLH}	K_{LH}	t_{OHL}	K_{HL}
8-Wide 2-Input OR-NAND NA8R2N		10	1	@ @ @ @ @ @ @ @ @ @ @ @ @ @ @ @		A5		NAND	1.5	1.2	1.6	0.9
								In-verter	1.4	2.8	1.2	0.9
2 AND OR-NAND NARA24		2	1	@ @ # @		A1	AND input		0.4	2.0	0.8	1.3
							OR input		0.4		0.8	
							NAND input		0.4		0.7	
2 AND-NOR NRA23		2	1	@ @ #		A1	AND input		0.4	2.0	0.8	1.2
							NOR input		0.3		0.7	
3 AND-NOR NRA34		2	1	@ @ @ #		A2	AND input		0.4	2.0	0.8	1.3
							NOR input		0.3		0.7	
2 AND-3 NOR NRA24		2	1	@ @ # #		A2	AND input		0.5	2.8	0.8	1.2
							NOR input		0.4		0.7	
2-Wide 2-Input AND-NOR NR2A2		2	1	@ @ @ @		A1			0.4	2.0	0.8	1.2

Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay					
Function	Equivalent Circuit						Input Name	Output Name	t_{PLH}(ns)		t_{PHL}(ns)	
Function Name									t_{OLH}	K_{LH}	t_{OHL}	K_{HL}
3-Wide 2-Input AND-NOR NR3A2		3	1	@ @ @ @ @ @		A3			0.6	2.8	0.8	1.2
2-Wide 3-Input AND-NOR NR2A3N		4	1	@ @ @ @ @ @		A2		NOR	0.6	2.0	1.0	1.3
								In-verter	1.2	1.2	0.9	0.9
2-Wide 4-Input AND-NOR NR2A4N		5	1	@ @ @ @ @ @ @ @		A4		NOR	0.6	2.0	1.1	1.5
								In-verter	1.3	1.2	0.9	0.9
3-Wide 3-Input AND-NOR NR3A3N		5	1	@ @ @ @ @ @ @ @ @ @				NOR	0.8	2.8	1.0	1.3
								In-verter	1.2	1.2	1.1	0.9
3-Wide 4-Input AND-NOR NR3A4N		7	1	@ @ @ @ @ @ @ @ @ @ @ @ @ @				NOR	1.3	2.8	1.3	1.5
								In-verter	1.5	1.2	1.6	0.9

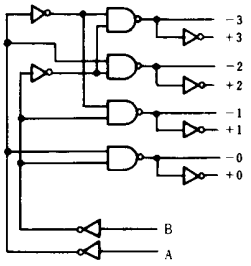
Macrocell: Function / Function Name	Macrocell: Equivalent Circuit	Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{PLH}(ns) t_{OLH}	Delay: t_{PLH}(ns) K_{LH}	Delay: t_{PHL}(ns) t_{OHL}	Delay: t_{PHL}(ns) K_{HL}
4-Wide 2-Input AND-NOR NR4A2N		5	1	# # # # # # # #		A4		NOR	1.0	3.7	1.1	1.2
								Inverter	1.3	1.2	1.3	0.9
4-Wide 3-Input AND-NOR NR4A3N		7	1	@ @ @ @ @ @ @ @ @ @ @ @				NOR	1.5	3.7	1.1	1.3
								Inverter	1.3	1.2	1.8	0.9
4-Wide 4-Input AND-NOR NR4A4N		9	1	@ @ @ @ @ @ @ @ @ @ @ @ @ @ @ @ @		A5		NOR	2.3	3.7	1.5	1.5
								Inverter	1.7	1.2	2.6	0.9

Macrocell: Function / Function Name	Macrocell: Equivalent Circuit	Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{PLH}(ns) t_{OLH}	Delay: t_{PLH}(ns) K_{LH}	Delay: t_{PHL}(ns) t_{OHL}	Delay: t_{PHL}(ns) K_{HL}
6-Wide 2-Input AND-NOR NR6A2N		8	1	# # # # # # # # # # # # #				NOR	1.6	1.2	1.3	0.9
								Inverter	1.0	1.2	1.4	1.2
8-Wide 2-Input AND-NOR NR8A2N		10	1	# # # # # # # # # # # # # # #		A5		NOR	1.3	1.2	1.4	0.9
								Inverter	1.6	1.2	1.6	0.9
2 AND-OR-NAND NRAR24		2	1	# # @ #		A1	OR input		0.5	2.8	1.2	1.2
							AND input		0.4		0.8	
							NOR input		0.3		0.7	

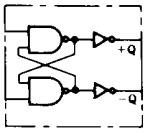
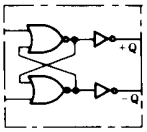
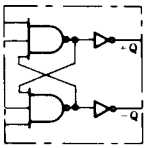
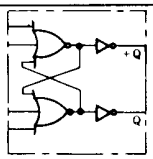
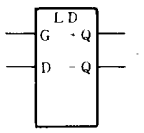
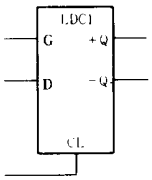
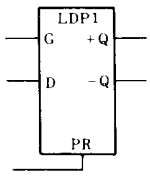
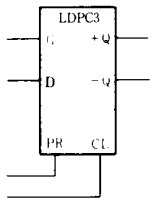
6. MULTIPLEXERS

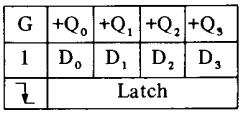
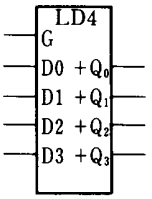
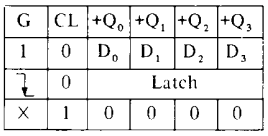
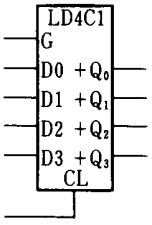
Macrocell: Function Name	Macrocell: Equivalent Circuit	Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{PLH}(ns) t_{OLH}	Delay: t_{PLH}(ns) K_{LH}	Delay: t_{PHL}(ns) t_{OHL}	Delay: t_{PHL}(ns) K_{HL}
2 to 1 Multiplexer M2T1N		3	1.2 1 1	# # #		B2	Y_0	+Y	1.1	1.2	0.8	0.9
							Y_1		1.1		0.8	
							S		1.3		1.2	
							Y_0	−Y	0.5	2.0	0.9	1.2
							Y_1		0.5		0.9	
							S		0.9		1.1	
4 to 1 Multiplexer M4T1N		9	1	# # # # # #		B4	Y_0	+Y	1.2	1.2	1.7	0.9
							Y_1		1.2		1.7	
							Y_2		1.2		1.7	
							Y_3		1.2		1.7	
							A		2.5		2.7	
							B		2.5		2.7	
							Y_0	−Y	1.4	3.7	1.0	1.3
							Y_1		1.4		1.0	
							Y_2		1.4		1.0	
							Y_3		1.4		1.0	
							A		2.4		2.3	
							B		2.4		2.3	
8 to 1 Multiplexer M8T1N		21	1	# # # # # # # # # #		B_6	Y_0 ≀ Y_7	+Y	1.7	1.2	2.0	1.3
							A, B, C		2.5		2.4	
							Y_0 ≀ Y_7	−Y	2.2	1.2	2.0	0.9
							A, B, C		2.6		2.8	
1 to 2 Demultiplexer M1T2N		4	1.2	# @		B3	Y	+0	1.2	1.2	0.8	0.9
							A		1.3		1.1	
							Y	+1	1.2	1.2	0.8	0.9
							A		1.2		0.8	
							Y	−0	0.5	1.2	1.0	1.2
							A		0.8		1.1	
							Y	−1	0.5	1.2	1.0	1.2
							A		0.5		1.0	

7. DECODERS

Macrocell: Function / Function Name	Macrocell: Equivalent Circuit	Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{PLH}(ns) t_{OLH}	Delay: t_{PLH}(ns) K_{LH}	Delay: t_{PHL}(ns) t_{OHL}	Delay: t_{PHL}(ns) K_{HL}
2-bit Decoder D2T4N		8	1	# # # #

8. LATCHES (with Scan Function)

Macrocell: Function / Function Name	Truth table	Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Input Name	Output Name	Delay: t_{PLH}(ns) t_{OLH}	K_{LH}	t_{PHL}(ns) t_{OHL}	K_{HL}
$\overline{RS}$-Latch LRS0	SN RN +Q −Q 0 0 0 0 0 1 1 0 1 0 0 1 1 1 Latch	8	1	@ @		A3	$\overline{S}$ $\overline{R}$ $\overline{S}$ $\overline{R}$	+Q +Q −Q −Q	2.7 2.5 2.5 2.7	1.0 1.0	– 2.6 2.6 –	0.6 0.6
RS-Latch LRS3	S R +Q −Q 0 0 Latch 0 1 0 1 1 0 1 0 1 1 1 1	8	1	# #		A3	S R S R	+Q +Q −Q −Q	2.4 – – 2.4	1.0 1.0	2.7 3.3 3.3 2.7	0.6 0.6
2-Input $\overline{RS}$ Latch LR2S20	SN RN +Q −Q 0 0 0 0 0 1 1 0 1 0 0 1 1 1 Latch	9	1	@ @ @ @		A4	$\overline{S}$ $\overline{R}$ $\overline{S}$ $\overline{R}$	+Q +Q −Q −Q	2.7 2.6 2.6 2.7	1.0 1.0	– 2.6 2.6 –	0.6 0.6
2-Input RS Latch LR2S23	S R +Q −Q 0 0 Latch 0 1 0 1 1 0 1 0 1 1 1 1	9	1	# # # #		A4	S R S R	+Q +Q −Q −Q	2.4 – – 2.4	1.0 1.0	3.1 3.7 3.7 3.1	0.6 0.6
D-Latch LD	G +Q −Q 1 D $\overline{D}$ ↓ Latch	5	1 1	@ @		C	G D G D	+Q +Q −Q −Q	3.2 3.2 2.6 2.6	1.2 1.2	2.9 2.9 2.9 2.9	0.9 0.9
D-Latch with CLR LDC1	G CL +Q −Q 1 0 D $\overline{D}$ ↓ 0 Latch X 1 0 1 X: Don't care	6	1 1 1	@ @ #		C	G CL D G CL D	+Q +Q +Q −Q −Q −Q	3.5 2.3 3.5 3.1 2.1 3.1	1.2 1.2	3.4 2.4 3.4 3.2 2.0 3.2	0.9 0.9
D-Latch with PRE LDP1	G PR +Q −Q 1 0 D $\overline{D}$ ↓ 0 Latch X 1 1 0 X: Don't care	6	1 1 1	@ @ #		C	G PR D G PR D	+Q +Q +Q −Q −Q −Q	3.3 2.4 3.3 2.9 2.2 2.9	1.2 1.2	3.2 2.5 3.2 3.0 2.1 3.0	0.9 0.9
D-Latch with PRE/CLR LDPC3	G PR CL +Q −Q 1 0 0 D $\overline{D}$ ↓ 0 0 Latch X 1 0 1 0 X 0 1 0 1 X 1 1 0 1 X: Don't care	7	1 1 1 1	@ @ # #		C	G PR CL D G PR CL D	+Q +Q +Q +Q −Q −Q −Q −Q	3.8 2.9 2.3 3.8 3.2 2.5 2.1 3.2	1.2 1.2	3.5 2.8 2.4 3.5 3.5 2.6 2.0 3.5	0.9 0.9

Macrocell: Function / Function Name	Macrocell: Truth table	Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{PLH}(ns) t_{OLH}	Delay: t_{PLH}(ns) k_{LH}	Delay: t_{PHL}(ns) t_{OHL}	Delay: t_{PHL}(ns) k_{HL}
4-Bit D-Latch LD4		20	1 1 1 1 1	@ @ @ @ @		B4	G D0 ~ D3	+Q0 ~ +Q3	3.5 3.2	1.2	3.2 2.9	0.9
4-Bit D-Latch with CLR LD4C1		26	1 1 1 1 1 1	@ @ @ @ @ #		B4	G D0 ~ D3 CL	Q0 ~ +Q3	3.6 3.3 3.0	1.2	3.2 2.9 2.7	0.9

9. FLIP-FLOPS (with Scan Function)

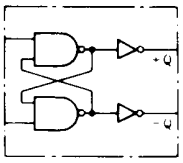
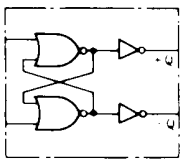
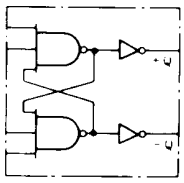
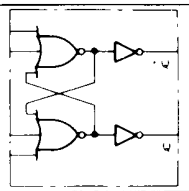
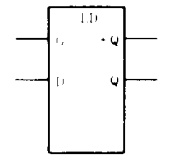
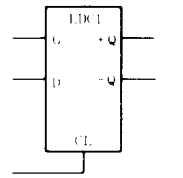
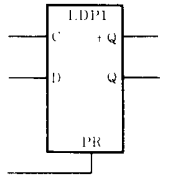
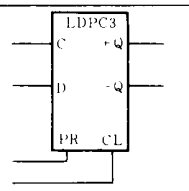
Macrocell: Function / Function Name	Macrocell: Truth table	Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{PLH}(ns) t_{OLH}	Delay: t_{PLH}(ns) K_{LH}	Delay: t_{PHL}(ns) t_{OHL}	Delay: t_{PHL}(ns) K_{HL}
DFF FD	CK | +Q | −Q ↑ | D | $\overline{D}$ ↓ | $+Q_0$ | $-Q_0$	7	1	@ @	FD CK +Q D −Q	C	CK	+Q	3.9	1.2	3.8	0.9
								−Q	3.5	1.2	3.6	0.9
DFF with Load FDL1	CK | L | +Q | −Q ↑ | 0 | D_C | $\overline{D_C}$ ↑ | 1 | D_L | $\overline{D_L}$ ↓ | X | $+Q_0$ | $-Q_0$ X:Don't care	9	1 1 1 1.2	@ @ @ #	FDL1 CK DC +Q DL −Q L	C	CK	+Q	3.9	1.2	3.8	0.9
								−Q	3.5	1.2	3.6	0.9
DFF with CLR FDC1	CK | CL | +Q | −Q ↑ | 0 | D | $\overline{D}$ ↓ | 0 | $+Q_0$ | $-Q_0$ X | 1 | 0 | 1 X:Don't care	8	1 1 1.2	@ @ #	FDC1 CK +Q D −Q CL	C	CK CL	+Q	4.0 –	1.2	4.1 2.1	0.9
							CK CL	−Q	3.8 1.8	1.2	3.7 –	0.9
DFF with PRE FDP1	CK | PR | +Q | −Q ↑ | 0 | D | $\overline{D}$ ↓ | 0 | $+Q_0$ | $-Q_0$ X | 1 | 1 | 0 X:Don't care	8	1 1 1.2	@ @ #	FDP1 CK +Q D −Q PR	C	CK RR	+Q	4.4 2.8	1.2	4.1 –	0.9
							CK PR	−Q	3.8 –	1.2	4.1 2.5	0.9
DFF with PRE/ CLR FDPC3	CK | PR | CL | +Q | −Q ↑ | 0 | 0 | D | $\overline{D}$ ↓ | 0 | 0 | $+Q_0$ | $-Q_0$ X | 1 | 0 | 1 | 0 X | 0 | 1 | 0 | 1 X | 1 | 1 | 0 | 1 X:Don't care	9	1 1 1.2 1.2	@ @ # #	FDPC3 CK +Q D −Q PR CL	C	CK CL PR	+Q	4.5 2.0 2.9	1.2	4.4 2.1 –	0.9
							CK CL PR	−Q	4.1 1.8 –	1.2	4.2 1.7 2.6	0.9
JKFF FJ	CK | J | K | +Q | −Q ↓ | 0 | 0 | 0 | 1 ↓ | 1 | 1 | 1 | 0 ↓ | 0 | 1 | $+Q_0$ | $-Q_0$ ↓ | 1 | 0 | $-Q_0$ | $+Q_0$ ↓ | X | X | $+Q_0$ | $-Q_0$ X:Don't care	10	1.2 1 1	@ @ #	FJ CK +Q J K −Q	C	CK	+Q	3.7	1.2	4.4	0.9
								−Q	3.6	1.2	4.4	0.9
JKFF with CLR FJC1	CK | J | K | CL | +Q | −Q ↓ | 0 | 0 | 0 | 0 | 1 ↓ | 1 | 1 | 0 | 1 | 0 ↓ | 0 | 1 | 0 | $+Q_0$ | $-Q_0$ ↓ | 1 | 0 | 0 | $-Q_0$ | $+Q_0$ ↓ | X | X | 0 | $+Q_0$ | $-Q_0$ X | X | X | 1 | 0 | 1 X:Don't care	13	1.2 1 1 1	@ @ # #	FJC1 CK +Q J K −Q CL	C	CK CL	+Q	4.3 –	1.2	4.6 4.8	0.9
							CK CL	−Q	4.0 3.5	1.2	4.9 –	0.9

Macrocell: Function / Function Name	Truth table	Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay: Input Name	Output Name	t_{PLH}(ns): t_{OLH}	k_{LH}	t_{PHL}(ns): t_{OHL}	k_{HL}
JKFF with PRE/CLR FJPC1	CK J K PR CL +Q −Q ↓ 0 0 1 0 0 1 ↓ 1 1 1 0 1 0 ↓ 0 1 1 0 $+Q_0$ Q_0 ↓ 1 0 1 0 $-Q_0$ $+Q_0$ ↑ X X 1 0 $+Q_0$ $-Q_0$ X X X 0 0 1 0 X X X 1 1 0 1 X X X 0 1 1 1 X:Don't care	14	1.2 1 1 1.2 1	@ @ # @ #	FJPC1 CK +Q J K −Q PR CL	C	CK $\overline{PR}$ CL CK $\overline{PR}$ CL	+Q −Q 	4.3 2.6 – 4.1 – 3.6	1.2 1.2 	4.6 2.6 4.8 4.9 4.6 2.6	0.9 0.9
TFF with CLR FTC1	CK CL +Q −Q ↓ 0 $-Q_0$ $+Q_0$ ↑ 0 $+Q_0$ $-Q_0$ X 1 0 1 X:Don't care	9	1 1.2	@ #	FTC1 CK +Q −Q CL	C	CK CL CK CL	+Q −Q 	4.0 – 3.8 1.8	1.2 1.2 	4.1 2.1 3.7 –	0.9 0.9
TFF with PRE FTP1	CK PR +Q −Q ↓ 0 $-Q_0$ $+Q_0$ ↑ 0 $+Q_0$ $-Q_0$ X 1 1 0 X:Don't care	9	1 1.2	@ #	FTP1 CK +Q −Q PR	C	CK PR CK PR	+Q −Q 	4.4 2.8 3.8 –	1.2 1.2 	4.1 – 4.1 2.5	0.9 0.9
TFF with PRE/CLR FTPC3	CK PR CL +Q −Q ↓ 0 0 $-Q_0$ $+Q_0$ ↑ 0 0 $+Q_0$ $-Q_0$ X 1 0 1 0 X 0 1 0 1 X 1 1 0 1 X:Don't care	10	1 1.2 1.2	@ # #	FTPC3 CK +Q −Q PR CL	C	CK PR CL CK PR CL	+Q −Q 	4.5 2.9 2.0 4.1 – 1.8	1.2 1.2 	4.4 – 2.1 4.2 2.6 1.7	0.9 0.9
4-Bit DFF FD4	CK $+Q_0$ $+Q_1$ $+Q_2$ $+Q_3$ ↓ D_0 D_1 D_2 D_3 ↑ $+Q_{00}$ $+Q_{10}$ $+Q_{20}$ $+Q_{30}$	28	1 1 1 1 1	@ @ @ @ @	FD4 CK D_0 $+Q_0$ D_1 $+Q_1$ D_2 $+Q_2$ D_3 $+Q_3$	B4	CK	$+Q_0$ ≀ $+Q_3$	4.1	1.2	4.0	0.9
4-Bit DFF with CLR FD4C1	CK CL $+Q_0$ $+Q_1$ $+Q_2$ $+Q_3$ ↓ 0 D_0 D_1 D_2 D_3 ↑ 0 $+Q_{00}$ $+Q_{10}$ $+Q_{20}$ $+Q_{30}$ X 1 0 0 0 0 X:Don't care	33	1 1 1 1 1 1	@ @ @ @ @ #	FD4C1 CK D_0 $+Q_0$ D_1 $+Q_1$ D_2 $+Q_2$ D_3 $+Q_3$ CL	B4	CK CL	$+Q_0$ ≀ $+Q_3$	4.4 –	1.2	4.3 3.3	0.9

10. SHIFT REGISTERS (with Scan Function)

Function / Function Name	Macrocell: Truth table	Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay: Input Name	Output Name	t_{PLH}(ns) t_{OLH}	t_{PLH}(ns) k_{LH}	t_{PHL}(ns) t_{OHL}	t_{PHL}(ns) k_{HL}
2-Bit SR ZSR	CK | +A | +B ↑ | D | $+A_0$ ↓ | $+A_0$ | $+B_0$	12	1 1	@ @	ZSR CK +A D +B	B1	CK	+A	4.1	1.2	4.0	0.9
								+B	4.1	1.2	4.0	0.9
2-Bit SR with CLR ZSRC1	CK | CLA | CLB | +A | +B ↑ | 0 | 0 | D | $+A_0$ ↓ | 0 | 0 | $+A_0$ | $+B_0$ X | 1 | X | 0 | X X | X | 1 | X | 0 X:Don't care	15	1 1 1.2 1.2	@ @ # #	ZSRC1 CK +A D CLA +B CLB	C	CK	+A	2.4	1.2	2.6	0.9
							CLA		–		2.5	
							CK	+B	2.4	1.2	2.6	0.9
							CLB		–		2.5	
2-Bit SR with CLR/PRE ZSRCP3	CK | CLA | CLB | PRA | PRB | +A | +B ↑ | 0 | 0 | 0 | 0 | D | $+A_0$ ↓ | 0 | 0 | 0 | 0 | $+A_0$ | $+B_0$ X | 1 | X | X | X | 0 | X X | X | 1 | X | X | X | 0 X | X | X | 1 | X | 1 | X X | X | X | X | 1 | X | 1 X | 1 | X | 1 | X | 0 | X X | X | 1 | X | 1 | X | 0 X:Don't care	17	1 1 1.2 1.2 1.2 1.2	@ @ # # # #	ZSRCP3 CK D +A CLA PRA CLB +B PRB	B4	CK	+A	4.7	1.2	4.6	0.9
							CLA		2.0		2.1	
							PRA		2.9		–	
							CK	+B	4.7	1.2	4.6	0.9
							CLB		2.0		2.1	
							PRB		2.9		–	
4-Bit SR ZSR4	CK | +A | +B | +C | +D ↑ | D | $+A_0$ | $+B_0$ | $+C_0$ ↓ | $+A_0$ | $+B_0$ | $+C_0$ | $+D_0$	28	1 1	@ @	ZSR4 CK +A D +B +C +D	C	CK	+A	4.2	1.2	4.1	0.9
								+B	4.2	1.2	4.1	0.9
								+C	4.2	1.2	4.1	0.9
								+D	4.2	1.2	4.1	0.9
4-Bit SR with CLR ZSR4C1	CK | CLA | CLB | CLC | CLD | +A | +B | +C | +D ↑ | 0 | 0 | 0 | 0 | D | $+A_0$ | $+B_0$ | $+C_0$ ↓ | 0 | 0 | 0 | 0 | $+A_0$ | $+B_0$ | $+C_0$ | $+D_0$ X | 1 | X | X | X | 0 | X | X | X X | X | 1 | X | X | X | 0 | X | X X | X | X | 1 | X | X | X | 0 | X X | X | X | X | 1 | X | X | X | 0 X:Don't care	36	1 1 1.2 1.2 1.2 1.2	@ @ # # # #	ZSR4C1 CK +A D +B CLA +C CLB +D CLC CLD	B4	CK	+A	4.5	1.2	4.4	0.9
							CLA		–		2.1	
							CK	+B	4.5	1.2	4.4	0.9
							CLB		–		2.1	
							CK	+C	4.5	1.2	4.4	0.9
							CLC		–		2.1	
							CK	+D	4.5	1.2	4.4	0.9
							CLD		–		2.1	

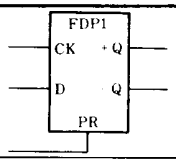
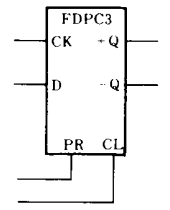
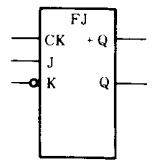
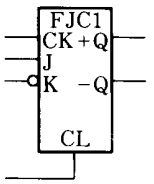
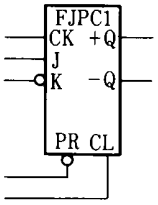
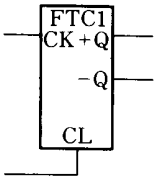
11. Latches (Normal Type)

Macrocell: Function / Function Name	Macrocell: Truth table	Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{PLH}(ns) t_{OLH}	Delay: t_{PLH}(ns) k_{LH}	Delay: t_{PHL}(ns) t_{OHL}	Delay: t_{PHL}(ns) k_{HL}
$\overline{RS}$ latch LRS0	SN RN +Q −Q 0 0 0 0 0 1 1 0 1 0 0 1 1 1 Latch	3	1	@ @		A3	$\overline{S}$ $\overline{R}$ $\overline{S}$ $\overline{R}$	+Q +Q −Q −Q	1.2 1.0 1.0 1.2	1.2 1.2	– 0.9 0.9 –	0.9 0.9
RS latch LRS3	S R +Q −Q 0 0 Latch 0 1 0 1 1 0 1 0 1 1 1 1	3	1	# #		A3	S R S R	+Q +Q −Q −Q	0.9 – – 0.9	1.2 1.2	1.0 1.6 1.6 1.0	0.9 0.9
2-Input $\overline{RS}$ latch LR2S20	SN RN +Q −Q 0 0 0 0 0 1 1 0 1 0 0 1 1 1 Latch	4	1	@ @ @ @		A4	$\overline{S}$ $\overline{R}$ $\overline{S}$ $\overline{R}$	+Q +Q −Q −Q	1.2 1.1 1.1 1.2	1.2 1.2	– 0.9 0.9 –	0.9 0.9
2-Input RS latch LR2S23	S R +Q −Q 0 0 Latch 0 1 0 1 1 0 1 0 1 1 1 1	4	1	# # # #		A4	S R S R	+Q +Q −Q −Q	0.9 – – 0.9	1.2 1.2	1.4 2.0 2.0 1.4	0.9 0.9
D latch LD	G +Q −Q 1 D $\overline{D}$ ⌝ Latch	4	1.2 1	@ @		C	G D G D	+Q +Q −Q −Q	1.5 1.5 1.6 1.6	1.2 1.2	1.5 1.5 1.8 1.8	0.9 0.9
D latch with CLR LDC1	G CL +Q −Q 1 0 D $\overline{D}$ ⌝ 0 Latch X 1 0 1 X: Don't care	5	1.2 1 1	@ @ #		C	G CL D G CL D	+Q +Q +Q −Q −Q −Q	2.8 1.6 2.8 2.1 1.1 2.1	1.2 1.2	2.4 1.4 2.4 2.8 1.6 2.8	0.9 0.9
D latch with PRE LDP1	G PR +Q −Q 1 0 D $\overline{D}$ ⌝ 0 Latch X 1 1 0 X: Don't care	5	1.2 1 1	@ @ #		C	G PR D G PR D	+Q +Q +Q −Q −Q −Q	1.6 0.7 1.6 1.9 1.2 1.9	1.2 1.2	1.8 1.1 1.8 1.9 1.0 1.9	0.9 0.9
D latch with PRE/CLR LDPC3	G PR CL +Q −Q 1 0 0 D $\overline{D}$ ⌝ 0 0 Latch X 1 0 1 0 X 0 1 0 1 X 1 1 0 1 X: Don't care	6	1.2 1 1 1	@ @ # #		C	G PR CL D G PR CL D	+Q +Q +Q +Q −Q −Q −Q −Q	3.1 2.2 1.6 3.1 2.2 1.5 1.1 2.2	1.2 1.2	2.5 1.8 1.4 2.5 2.9 2.0 1.4 2.9	0.9 0.9

Macrocell: Function Name	Macrocell: Truth table	Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{PLH}(ns) t_{OLH}	Delay: t_{PLH}(ns) k_{LH}	Delay: t_{PHL}(ns) t_{OHL}	Delay: t_{PHL}(ns) k_{HL}
4-Bit D latch LD4	G | $+Q_0$ | $+Q_1$ | $+Q_2$ | $+Q_3$ 1 | D_0 | D_1 | D_2 | D_3 ↓ | Latch	13	1 1 1 1 1	@ @ @ @ @	LD4 G D0 +Q_0 D1 +Q_1 D2 +Q_2 D3 +Q_3	B4	G D_0 ≀ D_3	$+Q_0$ ≀ $+Q_3$	1.8 1.5	1.2	1.8 1.5	0.9
4-Bit D latch with CLR LD4C1	G | CL | $+Q_0$ | $+Q_1$ | $+Q_2$ | $+Q_3$ 1 | 0 | D_0 | D_1 | D_2 | D_3 ↓ | 0 | Latch X | 1 | 0 | 0 | 0 | 0 X:Don't care	14	1 1 1 1 1 1	@ @ @ @ @ #	LD4C1 G D0 +Q_0 D1 +Q_1 D2 +Q_2 D3 +Q_3 CL	B4	G D_0 ≀ D_3 CL	$+Q_0$ ≀ $+Q_3$	1.9 1.6 1.3	1.2	1.8 1.5 1.3	0.9

12. FLIP-FLOPS (Normal Type)

Macrocell: Function Name	Macrocell: Truth table	Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{PLH}(ns) t_{OLH}	Delay: t_{PLH}(ns) k_{LH}	Delay: t_{PHL}(ns) t_{OHL}	Delay: t_{PHL}(ns) k_{HL}
DFF FD	CK | +Q | −Q ↑ | D | $\overline{D}$ ↓ | $+Q_0$ | $-Q_0$	6	1	@ @	FD CK +Q D Q	C	CK	+Q −Q	2.2 2.5	1.2 1.2	2.4 2.5	0.9 0.9
DFF with Load FDL1	CK | L | +Q | −Q ↑ | 0 | D_C | $\overline{D}_C$ ↑ | 1 | D_L | $\overline{D}_L$ ↓ | X | $+Q_0$ | $-Q_0$ X:Don't care	8	1 1 1 1.2	@ @ @ #	FDL1 CK DC +Q DL Q D	C	CK	+Q −Q	2.2 2.5	1.2 1.2	2.4 2.5	0.9 0.9
DFF with CLR FDC1	CK | CL | +Q | −Q ↑ | 0 | D | $\overline{D}$ ↓ | 0 | $+Q_0$ | $-Q_0$ X | 1 | 0 | 1 X:Don't care	7	1 1 1.2	@ @ #	FDC1 CK +Q D Q CL	C	CK CL CK CL	+Q −Q	2.2 — 2.9 0.9	1.2 1.2	2.4 2.5 2.6 —	0.9 0.9

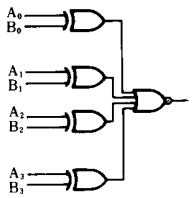
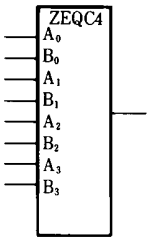
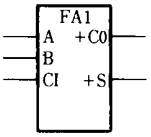
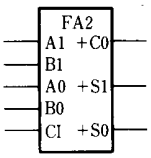
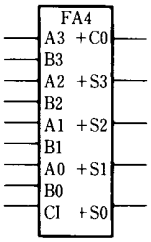
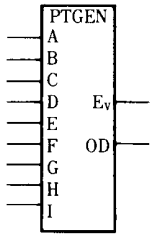
Macrocell: Function / Function Name	Macrocell: Truth table	Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{PLH}(ns) t_{OLH}	Delay: t_{PLH}(ns) K_{LH}	Delay: t_{PHL}(ns) t_{OHL}	Delay: t_{PHL}(ns) K_{HL}
DFF with PRE FDP1	CK PR +Q −Q ↓ 0 D $\bar{D}$ ↑ 0 $+Q_0$ $-Q_0$ × 1 1 0 X:Don't care	7	1 1 1.2	@ @ #		C	CK PR	+Q	2.6 1.0	1.2	2.8 –	0.9
							CK PR	−Q	2.8 –	1.2	3.0 1.4	0.9
DFF with PRE/CLR FDPC3	CK PR CL +Q −Q ↓ 0 0 D $\bar{D}$ ↑ 0 0 $+Q_0$ $-Q_0$ × 1 0 1 0 × 0 1 0 1 × 1 1 1 1 X:Don't care	8	1 1 1.2 1.2	@ @ # #		C	CK CL PR	+Q	2.6 – 1.0	1.2	2.8 2.9 1.2	0.9
							CK CL PR	−Q	3.2 0.9 –	1.2	3.1 0.6 1.5	0.9
JKFF FJ	CK J K +Q −Q ↓ 0 0 0 1 ↓ 1 1 1 0 ↓ 0 1 $+Q_0$ $-Q_0$ ↓ 1 0 $-Q_0$ $+Q_0$ ↑ × × $+Q_0$ $-Q_0$ X:Don't care	9	1.2 1 1	@ @ #		C	CK	+Q	2.7	1.2	2.1	0.9
								−Q	2.7	1.2	2.2	0.9
JKFF with CLR FJC1	CK J K CL +Q −Q ↓ 0 0 0 0 1 ↓ 1 1 0 1 0 ↓ 0 1 0 $+Q_0$ $-Q_0$ ↓ 1 0 0 $-Q_0$ $+Q_0$ ↑ × × 0 $+Q_0$ $-Q_0$ × × × 1 0 1 X:Don't care	12	1.2 1 1 1	@ @ # #		C	CK CL	+Q	3.2 –	1.2	2.6 2.1	0.9
							CK CL	−Q	2.8 3.0	1.2	2.8 –	0.9
JKFF with PRE/CLR FJPC1	CK J K PR CL +Q −Q ↓ 0 0 1 0 0 1 ↓ 1 1 1 0 1 0 ↓ 0 1 1 0 $+Q_0$ $-Q_0$ ↓ 1 0 1 0 $-Q_0$ $+Q_0$ ↑ × × 1 0 $+Q_0$ $-Q_0$ × × × 0 0 1 0 × × × 1 1 0 1 × × × 0 1 0 0 X:Don't care	13	1.2 1 1 1.2 1	@ @ # @ #		C	CK $\overline{PR}$ CL	+Q	3.2 2.9 0.9	1.2	2.6 – 2.1	0.9
							CK $\overline{PR}$ CL	−Q	2.9 0.9 3.1	1.2	2.8 1.1 –	0.9
TFF with CLR FTC1	CK CL +Q −Q ↓ 0 $-Q_0$ $+Q_0$ ↑ 0 $+Q_0$ $-Q_0$ × 1 0 1 X:Don't care	8	1 1.2	@ #		C	CK CL	+Q	2.2 –	1.2	2.4 2.5	0.9
							CK CL	−Q	2.9 0.9	1.2	2.6 –	0.9

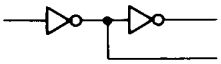
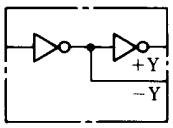
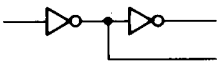
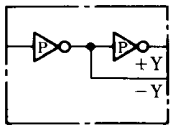
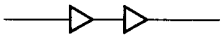
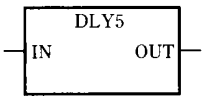
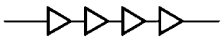
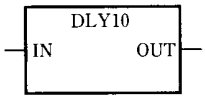
Macrocell: Function / Function Name	Macrocell: Truth table	Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{PLH}(ns) t_{OLH}	Delay: t_{PLH}(ns) K_{LH}	Delay: t_{PHL}(ns) t_{OHL}	Delay: t_{PHL}(ns) K_{HL}
TFF with PRE FTP1	CK | PR | +Q | −Q ↓ | 0 | $-Q_0$ | $+Q_0$ ↑ | 0 | $+Q_0$ | $-Q_0$ × | 1 | 1 | 0 X:Don't care	8	1 1.2	@ #	FTP1: CK +Q, −Q, PR	C	CK PR	+Q	2.6 1.0	1.2	2.8 –	0.9
							CK PR	−Q	2.8 –	1.2	3.0 1.4	0.9
TFF with PRE/CLR FTPC3	CK | PR | CL | +Q | −Q ↓ | 0 | 0 | $-Q_0$ | $+Q_0$ ↑ | 0 | 0 | $+Q_0$ | $-Q_0$ × | 1 | 0 | 1 | 0 × | 0 | 1 | 0 | 1 × | 1 | 1 | 1 | 1 X:Don't care	9	1 1.2 1.2	@ # #	FTPC3: CK +Q, −Q, PR CL	C	CK PR CL	+Q	2.6 1.0 –	1.2	2.8 1.2 2.9	0.9
							CK PR CL	−Q	3.2 – 0.9	1.2	3.1 1.5 0.6	0.9
4-Bit DFF FD4	CK | $+Q_0$ | $+Q_1$ | $+Q_2$ | $+Q_3$ ↓ | D_0 | D_1 | D_2 | D_3 ↑ | $+Q_{00}$ | $+Q_{10}$ | $+Q_{20}$ | $+Q_{30}$	21	1 1 1 1 1	@ @ @ @ @	FD4: CK, D_0 $+Q_0$, D_1 $+Q_1$, D_2 $+Q_2$, D_3 $+Q_3$	B4	CK	$+Q_0$ ≀ $+Q_3$	2.4	1.2	2.6	0.9
4-Bit DFF with CLR FD4C1	CK | CL | $+Q_0$ | $+Q_1$ | $+Q_2$ | $+Q_3$ ↓ | 0 | D_0 | D_1 | D_2 | D_3 ↑ | 0 | $+Q_{00}$ | $+Q_{10}$ | $+Q_{20}$ | $+Q_{30}$ × | 1 | 0 | 0 | 0 | 0 X:Don't care	25	1 1 1 1 1 1	@ @ @ @ @ #	FD4C1: CK, D_0 $+Q_0$, D_1 $+Q_1$, D_2 $+Q_2$, D_3 $+Q_3$, CL	B4	CK CL	$+Q_0$ ≀ $+Q_3$	2.6 –	1.2	2.6 1.6	0.9

13. SHIFT REGISTERS (Normal Type)

Macrocell: Function / Function Name	Macrocell: Truth table	Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{PLH}(ns) t_{OLH}	Delay: t_{PLH}(ns) K_{LH}	Delay: t_{PHL}(ns) t_{OHL}	Delay: t_{PHL}(ns) K_{HL}
2-Bit SR ZSR	CK | +A | +B ↑ | D | $+A_0$ ↓ | $+A_0$ | $+B_0$	10	1 1	@ @	ZSR: CK +A, D +B	B1	CK	+A	2.3	1.2	2.5	0.9
								+B	2.3	1.2	2.5	0.9
2-Bit SR with CLR ZSRC1	CK | CLA | CLB | +A | +B ↑ | 0 | 0 | D | $+A_0$ ↓ | 0 | 0 | $+A_0$ | $+B_0$ X | 1 | X | 0 | X X | X | 1 | X | 0 X:Don't care	12	1 1 1.2 1.2	@ @ # #	ZSRC1: CK +A, D, CLA +B, CLB	C	CK	+A	2.4	1.2	2.6	0.9
							CLA		–		2.5	
							CK	+B	2.4	1.2	2.6	0.9
							CLB		–		2.5	
2-Bit SR with CLR/PRE ZSRCP3	CK | CLA | CLB | PRA | PRB | +A | +B ↑ | 0 | 0 | 0 | 0 | D | $+A_0$ ↓ | 0 | 0 | 0 | 0 | $+A_0$ | $+B_0$ X | 1 | X | X | X | 0 | X X | X | 1 | X | X | X | 0 X | X | X | 1 | X | 1 | X X | X | X | X | 1 | X | 1 X | 1 | X | 1 | X | 1 | X X | X | 1 | X | 1 | X | 1 X:Don't care	14	1 1 1.2 1.2 1.2 1.2	@ @ # # # #	ZSRCP3: CK, D +A, CLA, PRA, CLB +B, PRB	B4	CK	+A	2.8	1.2	3.0	0.9
							CLA		–		2.9	
							PRA		1.0		1.2	
							CK	+B	2.8	1.2	3.0	0.9
							CLB		–		2.9	
							PRB		1.0		1.2	
4-Bit SR ZSR4	CK | +A | +B | +C | +D ↑ | D | $+A_0$ | $+B_0$ | $+C_0$ ↓ | $+A_0$ | $+B_0$ | $+C_0$ | $+D_0$	19	1 1	@ @	ZSR4: CK +A, D +B, +C, +D	C	CK	+A	2.4	1.2	2.6	0.9
								+B	2.4	1.2	2.6	0.9
								+C	2.4	1.2	2.6	0.9
								+D	2.4	1.2	2.6	0.9
4-Bit SR with CLR ZSR4C1	CK | CLA | CLB | CLC | CLD | +A | +B | +C | +D ↑ | 0 | 0 | 0 | 0 | D | $+A_0$ | $+B_0$ | $+C_0$ | $+D_0$ ↓ | 0 | 0 | 0 | 0 | $+A_0$ | $+B_0$ | $+C_0$ | $+D_0$ X | 1 | X | X | X | 0 | X | X | X X | X | 1 | X | X | X | 0 | X | X X | X | X | 1 | X | X | X | 0 | X X | X | X | X | 1 | X | X | X | 0 X:Don't care	23	1 1 1.2 1.2 1.2 1.2	@ @ # # # #	ZSR4C1: CK +A, D +B, CLA +C, CLB +D, CLC, CLD	B4	CK	+A	2.6	1.2	2.8	0.9
							CLA		–		2.5	
							CK	+B	2.6	1.2	2.8	0.9
							CLB		–		2.5	
							CK	+C	2.6	1.2	2.8	0.9
							CLC		–		2.5	
							CK	+D	2.6	1.2	2.8	0.9
							CLD		–		2.5	

14. OTHERS

Macrocell: Function / Function Name	Macrocell: Equivalent circuit	Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{PLH}(ns) t_{OLH}	Delay: t_{PLH}(ns) K_{LH}	Delay: t_{PHL}(ns) t_{OHL}	Delay: t_{PHL}(ns) K_{HL}
4-Bit comparator ZEQC4		12	1.2	# # # # # # # #		B5	A_0 A_1 A_2 A_3 B_0 B_1 B_2 B_3		1.4	3.7	1.6	0.9
1-Bit full-adder FA1		7	1.2 1.2 1.2	# # #		B2	A, B Ci	+Co	1.8 0.9	1.2	1.5 0.8	1.2
							A, B Ci	+S	1.6 0.9	1.2	2.2 1.3	0.9
2-Bit full-adder FA2		14	1.2 1.2 1.2 1.2 1.2	# # # # #		C	An, Bn Ci	+Co	2.7 1.8	1.2	2.6 1.6	1.2
							An,Bn Ci	+Sn	2.7 1.8	1.2	3.0 2.1	0.9
4-Bit full-adder FA4		43	1.2 1.2 1.2 1.2 1.2 1.2 1.2 1.2 1.6	# # # # # # # # #		B5	An, Bn Ci	+Co	2.2 2.0	1.2	1.9 1.7	0.9
							An,Bn Ci	+Sn	4.3 3.6	2.0	4.4 3.7	0.9
9-Bit parity generator/ checker PTGEN		37	1 1 1 1 1 1 1 1 1	# # # # # # # # #		B5	A ~ I	Ev	4.2	3.7	3.0	1.3
								OD	3.2	1.2	4.5	0.9

Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay					
Function / Function Name	Equivalent circuit						Input Name	Output Name	t_{PLH}(ns)		t_{PHL}(ns)	
									t_{OLH}	K_{LH}	t_{OHL}	K_{HL}
Buffer BUF		1	1	@		A1		+Y	0.6	1.2	0.6	0.9
								−Y	0.3	1.2	0.4	0.9
Power buffer BUFP		2	1.2	@		A1		+Y	0.7	0.6	0.7	0.5
								−Y	0.4	0.6	0.4	0.5
Delay cell DLY5		6	1	@			IN	OUT	5.0	1.2	5.2	0.9
Delay cell DLY10		13	1	@			IN	OUT	9.6	1.2	9.8	0.9

15. TTL 74 SERIES

Macro Function Name	Function	Gate count	with scan-function
HS00	QUADRUPLE 2-INPUT POSITIVE NAND GATES	4	
HS02	QUADRUPLE 2-INPUT POSITIVE NOR GATES	4	
HS04	HEX INVERTERS	6	
HS08	QUADRUPLE 2-INPUT POSITIVE AND GATES	8	
HS10	TRIPLE 3-INPUT POSITIVE NAND GATES	6	
HS11	TRIPLE 3-INPUT POSITIVE AND GATES	9	
HS20	DUAL 4-INPUT POSITIVE NAND GATES	4	
HS21	DUAL 4-INPUT POSITIVE AND GATES	6	
HS27	TRIPLE 3-INPUT POSITIVE NOR GATES	6	
HS30	8-INPUT POSITIVE NAND GATES	6	
HS32	QUADRUPLE 2-INPUT POSITIVE OR GATES	8	
HS42	BCD-TO-DECIMAL DECODER	28	
HS43	EXCESS 3-TO-DECIMAL DECODER	28	
HS44	EXCESS 3-GRAY-TO-DECIMAL DECODER	28	
HS51	2-WIDE 2-INPUT, 2-WIDE 3-INPUT AND-OR-INVERT GATES	6	
HS54	4-WIDE 2-INPUT, 3-INPUT AND-OR-INVERT GATE	9	
HS55	2-WIDE 4-INPUT AND-OR-INVERT GATE	5	
HS73	DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS (WITH CLEAR)	32	34
HS74	D-TYPE POSITIVE EDGE-TRIGGERED FLIP FLOPS	20	22
HS75	QUADRUPLE LATCHES	16	20
HS76	DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS (WITH PRESET AND CLEAR)	32	34
HS77	4-BIT BISTABLE LATCHES	16	20
HS78	DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS (WITH PRESET, COMMON CLEAR, AND COMMON CLOCK)	30	32
HS82	2-BIT BINARY FULL ADDER	29	
HS83	4-BIT BINARY FULL ADDER	63	
HS85	4-BIT MAGNITUDE COMPARATOR	78	
HS86	QUADRUPLE EXCLUSIVE-OR GATES	12	
HS90	DECADE COUNTER	41	45
HS91	8-BIT SHIFT REGISTER	50	58
HS92	DIVIDE-BY-TWELVE COUNTER	34	38
HS93	4-BIT BINARY COUNTER	32	36
HS94	4-BIT SHIFT REGISTER	44	48
HS95	4-BIT SHIFT REGISTER	40	44

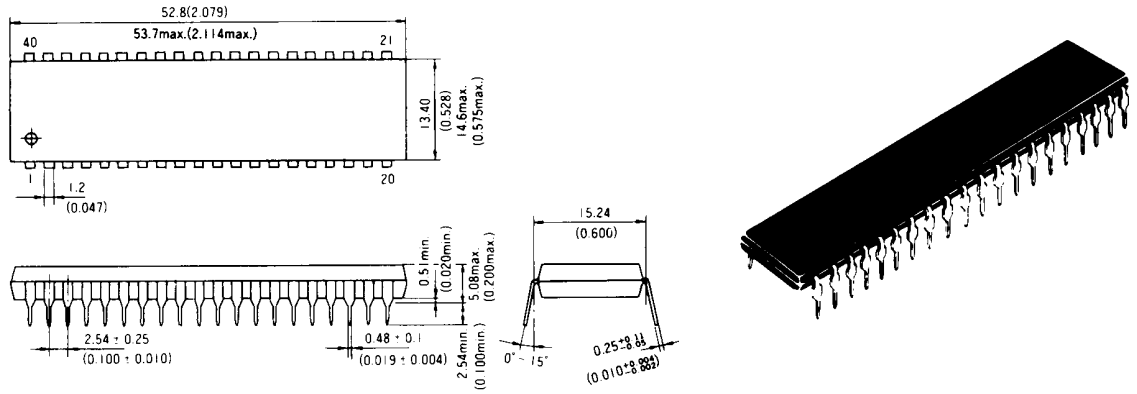
Macro Function Name	Function	Gate count	
			with scan-function
HS96	5-BIT SHIFT REGISTER (DUAL PARALLEL-IN, PARALLEL-OUT)	51	56
HS97	SYNCHRONOUS 6-BIT BINARY RATE MULTIPLEXER	144	150
HS98	4-BIT DATA SELECTOR/STORAGE REGISTER	35	39
HS99	4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTER	46	49
HS109	DUAL J-K POSITIVE EDGE-TRIGGERED FLIP FLOPS (WITH PRESET AND CLEAR)	28	30
HS113	DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS (WITH PRESET)	30	32
HS135	QUADRUPLE EXCLUSIVE-OR/NOR GATES	24	
HS137	3-LINE-TO-8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCHES	36	51
HS138	3-TO-8-LINE DECODER/DEMULTIPLEXER	25	
HS139	DUAL 2-TO-4-LINE DECODERS/DEMULTIPLEXERS	26	
HS147	10-LINE-TO-4-LINE PRIORITY ENCODER	46	
HS148	8-LINE-TO-3-LINE PRIORITY ENCODER	49	
HS150	16-BIT DATA SELECTOR/MULTIPLEXER	101	
HS151	1-OF-8-LINE DATA SELECTOR/MULTIPLEXER (WITH STROBE)	54	
HS152	1-OF-8-LINE DATA SELECTOR/MULTIPLEXER	29	
HS153	DUAL 4-OF-1-LINE DATA SELECTORS/MULTIPLEXERS	26	
HS154	4-OF-16-LINE DECODER/DEMULTIPLEXER	89	
HS155	DUAL 2-OF-4-LINE DECODERS/DEMULTIPLEXERS	23	
HS157	QUADRUPLE 2-OF-1-LINE DATA SELECTORS/MULTIPLEXERS (WITH NONINVERTED DATA OUTPUTS)	15	
HS158	QUADRUPLE 2-OF-1-LINE DATA SELECTORS/MULTIPLEXERS (WITH INVERTED DATA OUTPUTS)	11	
HS160	SYNCHRONOUS DECADE COUNTER	76	80
HS161	SYNCHRONOUS 4-BIT BINARY COUNTER	80	84
HS162	FULLY SYNCHRONOUS DECADE COUNTER	72	76
HS163	FULLY SYNCHRONOUS 4-BIT BINARY COUNTER	76	80
HS164	8-BIT PARALLEL-OUT SHIFT REGISTER	59	67
HS165	PARALLEL-LOAD 8-BIT SHIFT REGISTER	93	101
HS166	PARALLEL-LOAD 8-BIT SHIFT REGISTER	85	93
HS168	SYNCHRONOUS DECADE UP/DOWN COUNTER	94	98
HS169	SYNCHRONOUS BINARY UP/DOWN COUNTER	85	89
HS173	4-BIT D-TYPE REGISTER (WITH 3-STATE OUTPUTS)	51	55
HS174	HEX D-TYPE FLIP FLOPS (WITH CLEAR)	43	49
HS175	QUADRUPLE D-TYPE FLIP FLOPS (WITH CLEAR)	29	33
HS176	PRESETTABLE DECADE COUNTER	74	78

Macro Function Name	Function	Gate count	Gate count with scan-function
HS177	PRESETTABLE 4-BIT BINARY COUNTER	60	64
HS180	8-BIT ODD/EVEN PARITY GENERATOR/CHECKER	30	
HS181	ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR	119	
HS182	LOOK-AHEAD CARRY GENERATOR	41	
HS183	DUAL CARRY SAVE FULL ADDERS	40	
HS190	SYNCHRONOUS UP/DOWN DECADE COUNTER (SINGLE CLOCK LINE)	105	109
HS191	SYNCHRONOUS UP/DOWN 4-BIT BINARY COUNTER (SINGLE CLOCK LINE)	101	105
HS192	SYNCHRONOUS UP/DOWN DECADE COUNTER (DUAL CLOCK LINE)	91	95
HS193	SYNCHRONOUS UP/DOWN 4-BIT BINARY COUNTER (DUAL CLOCK LINE)	87	91
HS194	4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER	73	77
HS195	4-BIT PARALLEL ACCESS SHIFT REGISTER	47	51
HS198	8-BIT PARALLEL-IN, PARALLEL-OUT BIDIRECTIONAL SHIFT REGISTER	103	111
HS199	8-BIT PARALLEL-IN, PARALLEL-OUT SHIFT REGISTER (J-K INPUT FIRST STAGE)	89	97
HS251	1-OF-8-LINE DATA SELECTOR/MULTIPLEXER (WITH 3-STATE OUTPUTS)	34	
HS253	DUAL DATA SELECTORS/MULTIPLEXERS (WITH 3-STATE OUTPUTS)	32	
HS257	QUADRUPLE 2-TO-1-LINE DATA SELECTORS/MULTIPLEXERS (WITH NONINVERTED 3-STATE OUTPUTS)	19	
HS258	QUADRUPLE 2-TO-1-LINE DATA SELECTORS/MULTIPLEXERS (WITH 3-STATE OUTPUTS)	23	
HS259	8-BIT ADDRESSABLE LATCH	95	103
HS273	OCTAL D-TYPE POSITIVE-EDGE-TREGGERED FLIP FLOPS (WITH CLEAR)	57	65
HS279	QUADRUPLE S-R LATCHES	18	38
HS280	9-BIT ODD/EVEN PARITY GENERATOR/CHECKER	62	
HS283	4-BIT BINARY FULL ADDER (WITH FAST CARRY)	66	
HS290	DECADE COUNTER	40	44
HS293	4-BIT BINARY COUNTER	32	36
HS298	QUADRUPLE 2-INPUT MULTIPLEXERS (WITH STORAGE)	35	39
HS299	8-BIT UNIVERSAL SHIFT/STORAGE REGISTER (WITH 3-STATE OUTPUTS)	160	168
HS373	OCTAL D-TYPE TRANSPARENT LATCHES (WITH 3-STATE OUTPUTS)	49	57
HS374	OCTAL D-TYPE EDGE-TRIGGERED FLOP FLOPS (WITH 3-STATE OUTPUTS)	65	73
HS390	DUAL DECADE COUNTERS	66	74
HS393	DUAL 4-BIT BINARY COUNTERS	58	66
HS490	DUAL 4-BIT DECADE COUNTERS	78	86
HS668	SYNCHRONOUS DECADE UP/DOWN COUNTER	95	99
HS669	SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTER	80	84

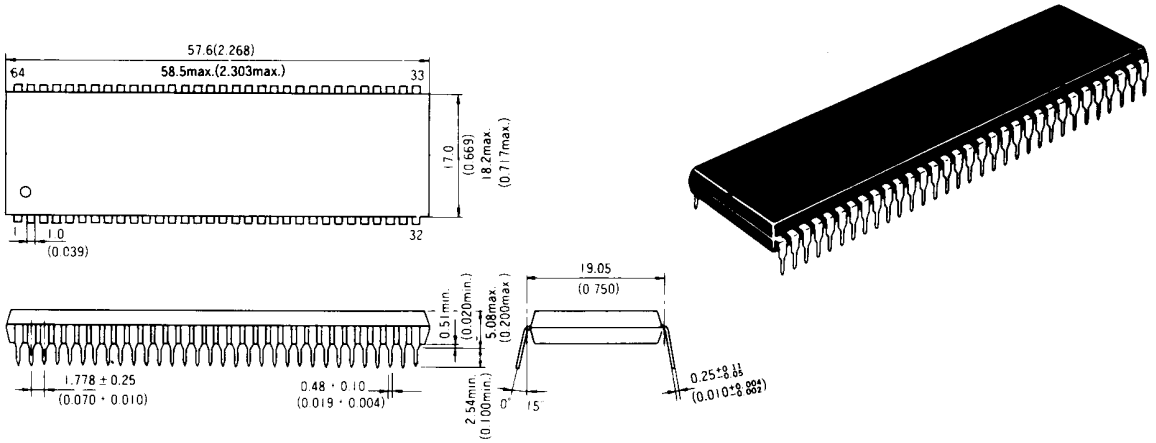
PACKAGE OUTLINE

Unit: mm (inch)

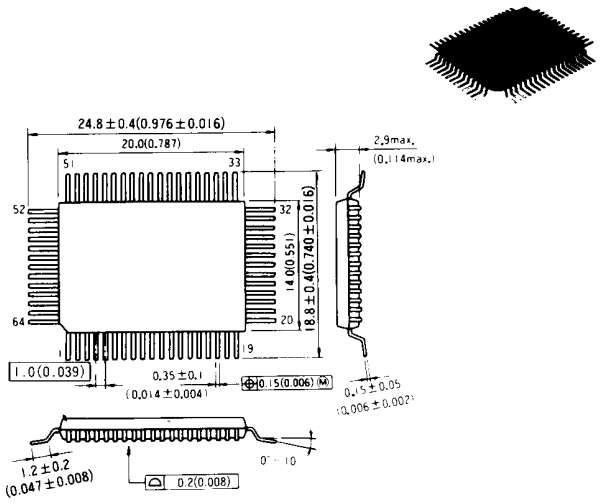
DILP-40



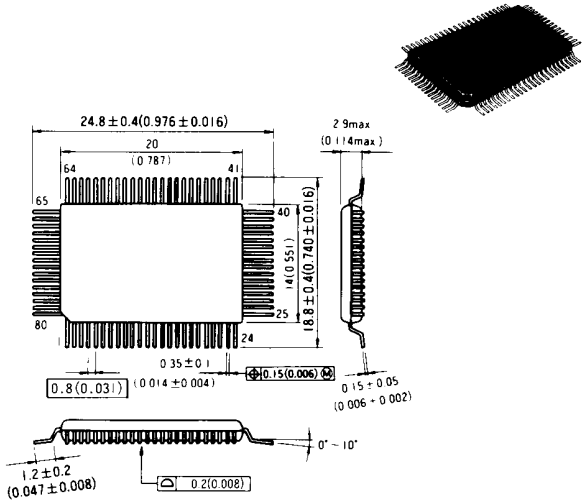
DILP-64S



QFP-64



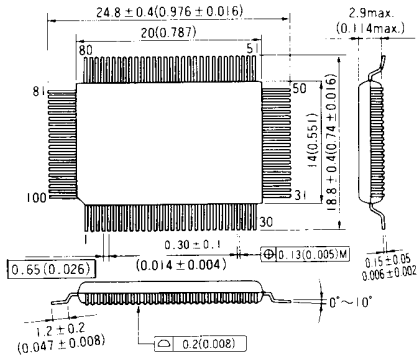
QFP-80

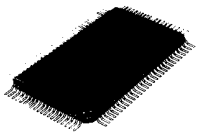


PACKAGE OUTLINE

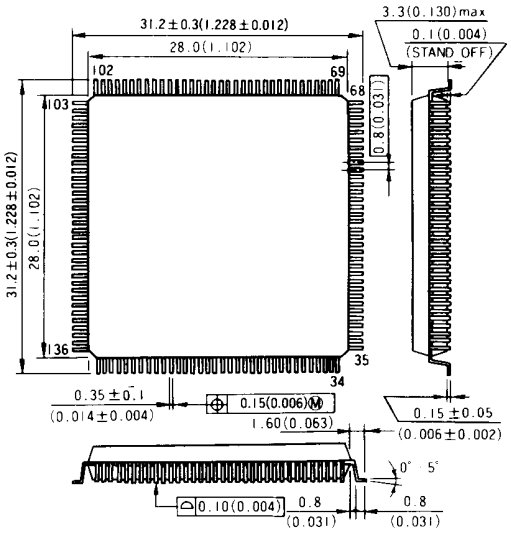
Unit: mm (inch)

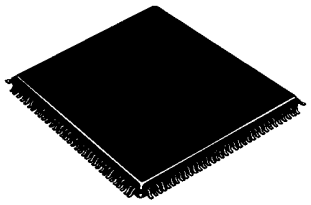
QFP-100



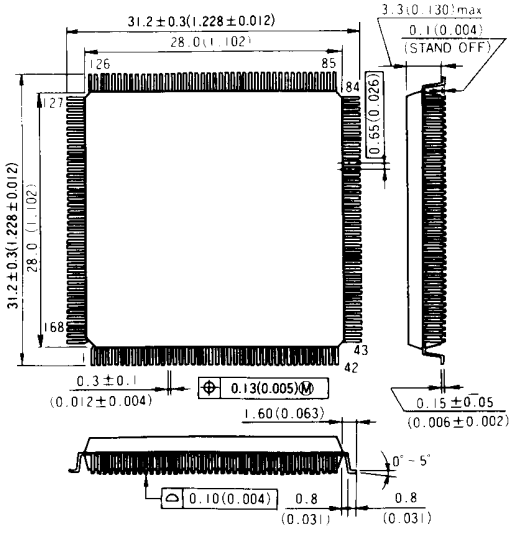


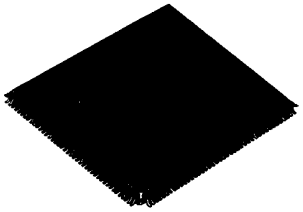
QFP5-136





QFP5-168

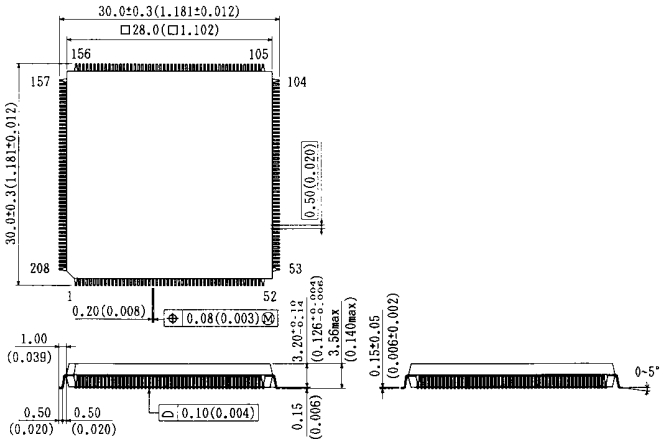


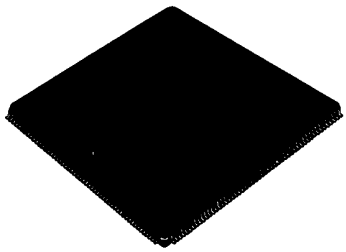


PACKAGE OUTLINE

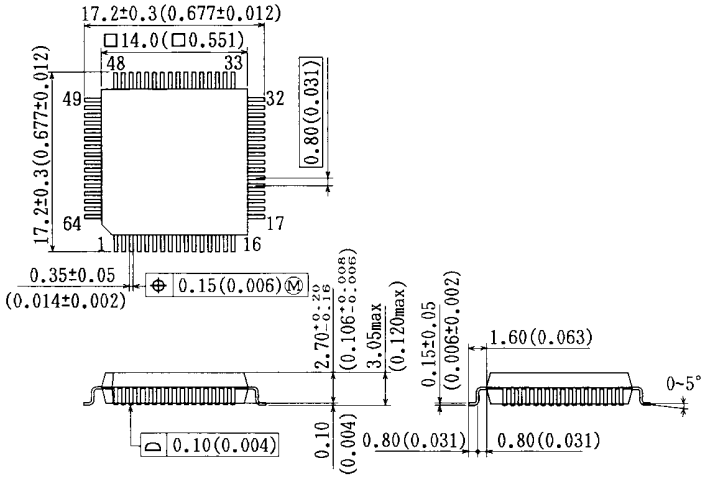
Unit: mm (inch)

QFP5-208

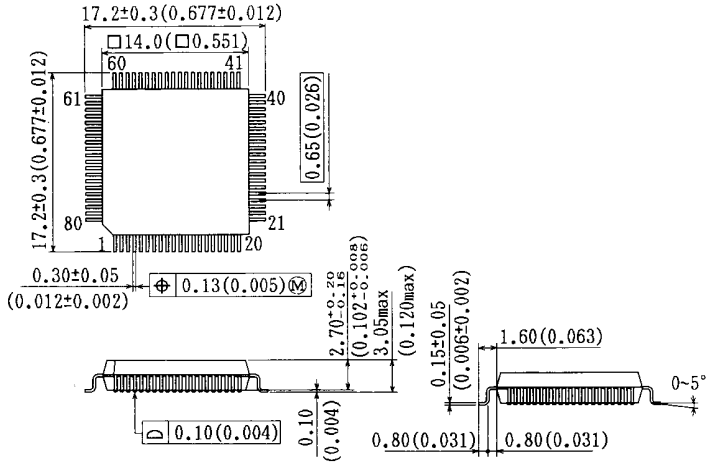


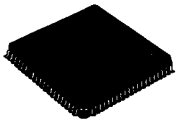


QFP3-64



QFP3-80

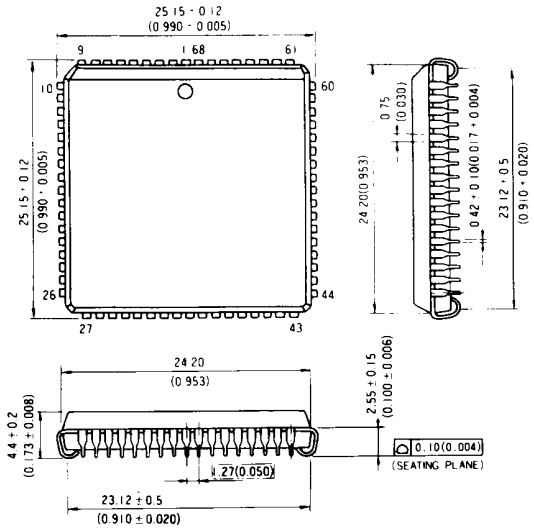


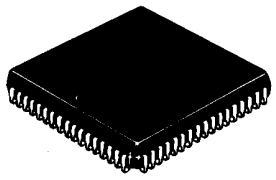


PACKAGE OUTLINE

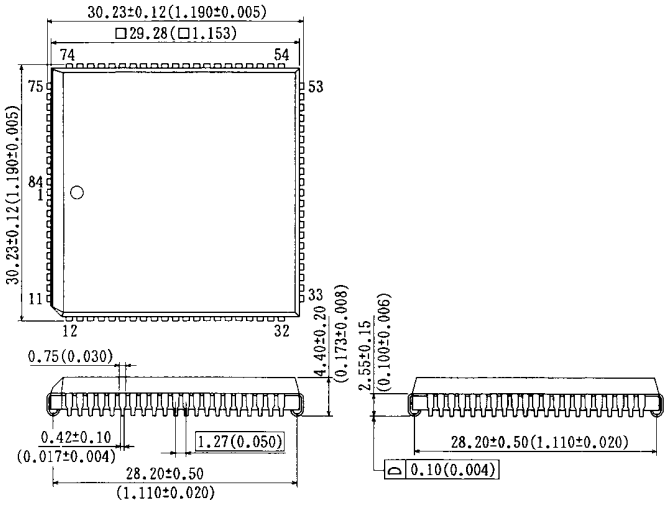
Unit: mm (inch)

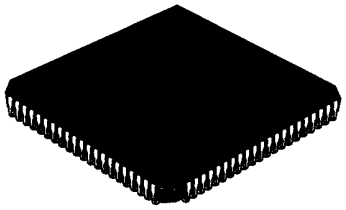
PLCC-68



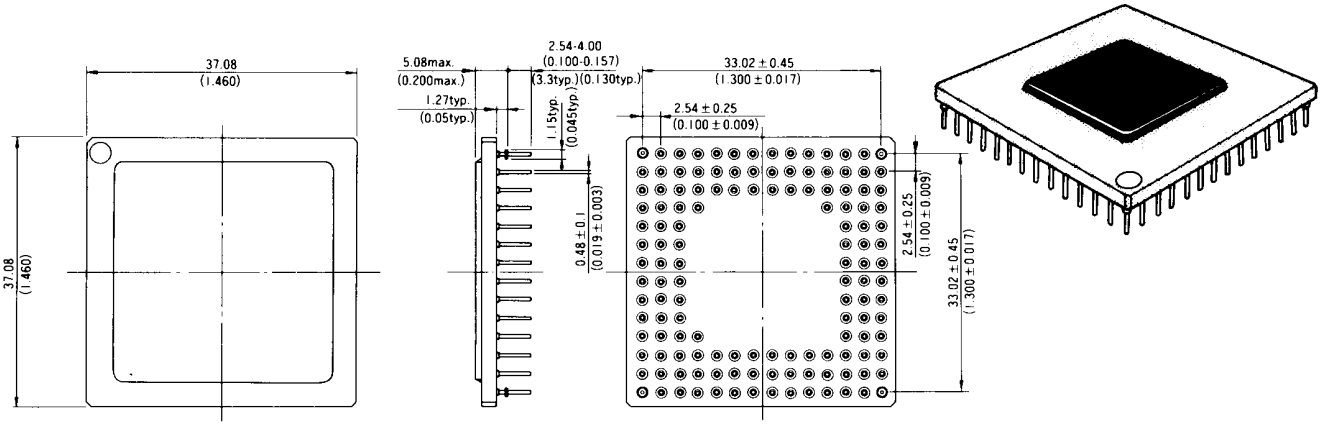


PLCC-84





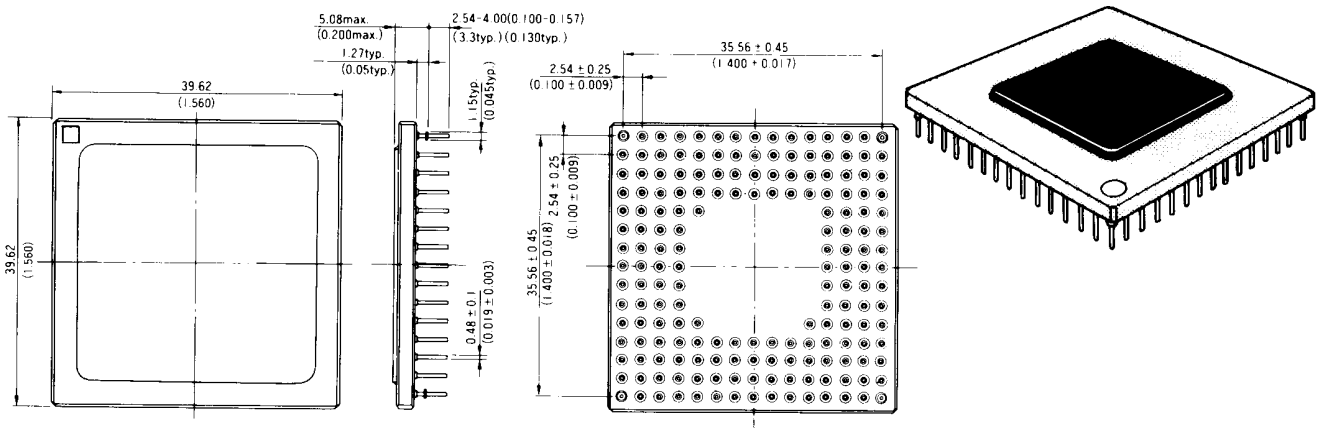
PGA-135



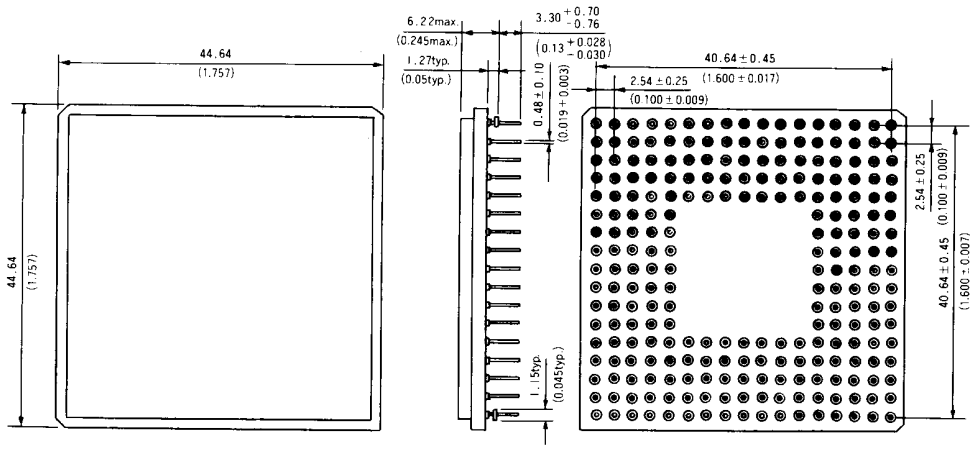
PACKAGE OUTLINE

Unit: mm (inch)

PGA-179



PGA-240



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