1. General Descriptions

LG Semicon's Mpact™ /3000 media processor (GM90C701Q) reaches a new level of multimedia integration for Windows 95 based PCs by leveraging architectural advances in VLIW, SIMD and vector processing and a high bandwidth Rambus memory system. The Mpact media processor is a high performance coprocessor for Windows95 based PCs. loaded with Mpact media modules, the media processor adds or enhances support for all seven multimedia functions ;

- Video compression and decompression,
- 2D graphics
- 3D graphics
- Audio
- FAX/modem
- Telephony
- Videoconferencing

The Mpact media processor uses an optimized real-time multitasking kernel to simultaneously execute these Mpact mediaware modules.

The kernel allows, for example, 2D and 3D graphics, music synthesis audio and modem communications to run concurrently. To adapt a Mpact media processor enabled system to changing market requirements, technology advances and new industry standards, upgrade the mediaware modules stored on the PC's hard disk via floppy disk, CD-ROM, or by using on-line services.

The Mpact media processor with its associated Rambus media memory resides on the PCI bus. A display interface supports popurlar RAMDACs for the RGB display monitor. A digital video interface and programmable I/O interface support a wide range of peripheral devices. This flexibility makes the Mpact media processor the ideal solution for designing integrated, low cost, multimedia PCs.

- ***Complete***
  - A total hardware solution for all multimedia ports ; display monitor, audio, telephone, video and joystick / MIDI
  - Integrated software for all for major multimedia functions on an x86 Windows 95 PC
- ***High Performance***
  - Very long Instruction Word (VLIW) processor sustaining 2 billion operations per second (BOPS)
  - 5 concurrent I/O and memory controllers
  - 132 MB/s PCI bus interface
  - Concurrent operation with MRK multitasking real-time kernel
  - Dynamically shared processing with x86 host for highest total system efficiency using the MRM resource manager
- ***Flexible***
  - Loadable mediaware modules provide the latest multimedia functionality using evolving APIs and operating system standards, while retaining the same hardware
  - Software programmable hardware interfaces support today's popular RAMDACs, video encoders and decoders, and audio and modem codecs, while allowing future I/O device requirements to be met
- ***Low cost***
  - High integration interfaces require minimal support circuitry
  - A single low cost 2-MByte Rambus DRAM needed for normal operation

2. Features

LG Semicon's Mpact™/3000 media processor (GM90C701Q) offers a complete multimedia solution for today's mainstream PC system, with the highest performance, integration and flexibility, and the lowest total cost.

- **Video** : MPEG-1 & , MPEG-1 encode
  DVD Playback (MPEG-2 decode)
- **2D graphics** : Full VGA, SVGA support, acceleration of video playback and GUI through GDI, DirectDraw
- **3D graphics** : Full 3D acceleration through Direct3D
- **Digital Audio** : Industry-standard Sound Card compatibility, 3D Audio (SRS) and 3D positional audio effects (DirectSound), Dolby AC-3 and MPEG-1 audio and MIDI, Wavetable and Waveguide synthesis
- **Fax/modem** : Data up to 33.6 kbps (V.34bis) ,Fax up to 14.4kbps (V.17) and DSVD (Digital Simultaneous Voice and Data)
- **Telephony** : Full-duplex speakerphone, Voicemail and callerID
- **Videophone** ; H.324 over POTS and H.320 over ISDN, H.323 over LAN

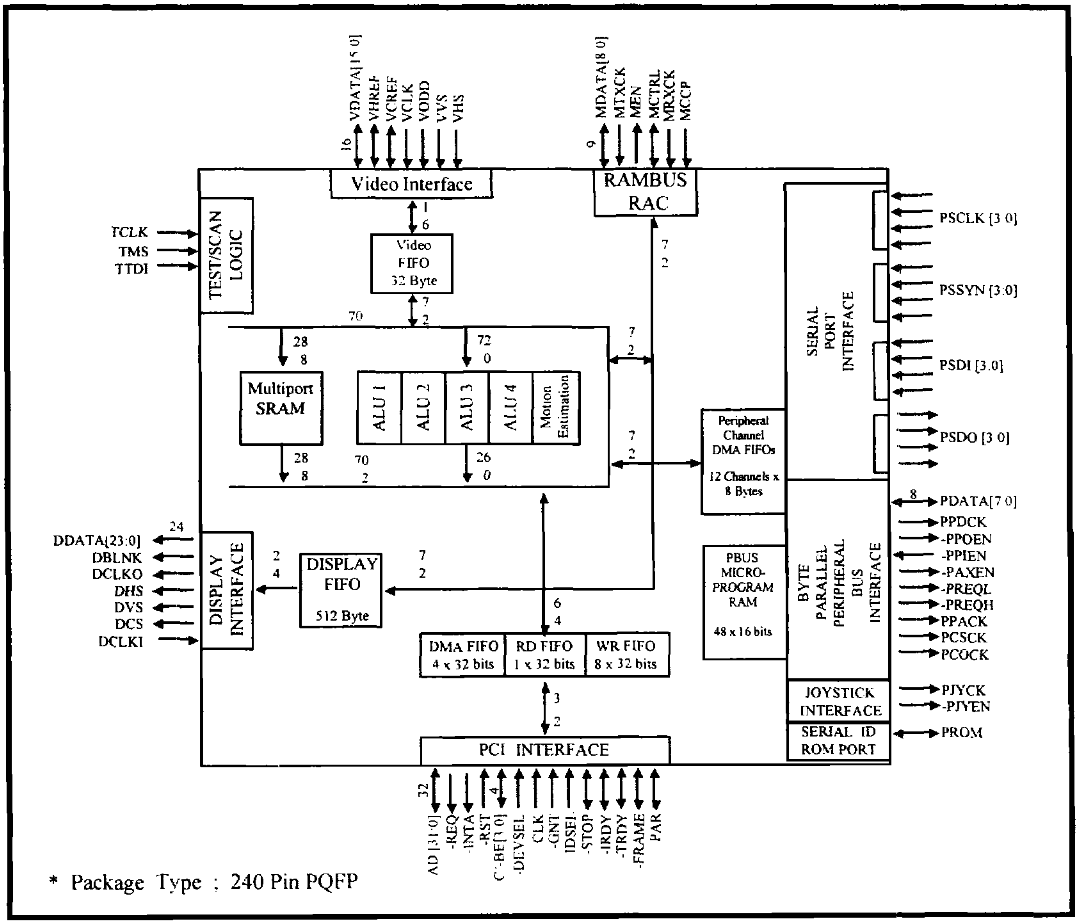
- Optimized real-time multitasking kernel executes multiple Mpact mediaware modules concurrently
- Small footprint 240-pin PQFP
- CMOS design with low power 3.3V operation

3. Block Diagram

The Mpact™/3000 media processor (GM90C701Q) 's high bandwidth Rambus memory system and its highly programmable interface to peripheral devices supports a wide range of integrated low cost multimedia systems.

The Mpact media processor implements a PCI interface, frame buffer controller, GUI accelerator and graphics controller, Rambus memory channel, digital video interface four serial channels, and a micro-programmable peripheral parallel interface.

FIGURE 3-1. Block Diagram with pin assignments



4. Pin Descriptions

4-1. PCI Bus Interface ; 48 Pins

Pin Number of Mpact	Symbol	# of Q`ty	Type	Function
2	-INTA	1	O	PCI bus interrupt a request
3	-RST	1	I	PCI bus reset.
4	CLK	1	I	PCI bus clock. All PCI inputs sampled on rising edge except reset (RST).
5	-GNT	1	I	PCI bus master Grant.
6	-REQ	1	O	PCI bus master Request
7, 9, 11-12, 14-17, 22-23, 25, 27-29, 32-33, 47-51, 53, 55-56, 58-59, 62, 64, 66, 68-70	AD[31:0]	32	I/O	PCI bus Address and data
19, 34, 46, 57	C/-BE[3:0]	4	I/O	PCI Bus command or Byte Enable during address transactions.
21	IDSEL	1	I	PCI bus Initialization Device select input
35	-FRAME	1	I/O	PCI bus Frame transaction
36	-IRDY	1	I/O	PCI bus Initiator Ready
38	-TRDY	1	I/O	PCI bus Target Ready
40	-DEVSEL	1	I/O	PCI bus Device Select. Target has decoded its address
42	-STOP	1	I/O	PCI bus stop transaction request by target
44	PAR	1	I/O	PCI bus Parity

4-2. Memory Interface - Rambus ; 15 Pins

Pin Number of Mpact	Symbol	# of Q`ty	Type	Function
76, 78, 80, 82, 88, 98, 100, 104, 106	MDATA [0:8]	9	I/O	Memory Data to/from the Rambus busdata signal.
86	MCTRL	1	I/O	Memory Control to/from the Rambus busctrl signal.
93	MTXCK	1	I	Memory Transmit clock from the Rambus TxClk signal. Transmit from memory.
95	MRXCK	1	I	Memory Receive clock from the Rambus RxClk signal. Receive into memory.
102	MEN	1	O	Memory Enable to the Rambus busenable signal.
108	MCCP	1	A	Memory Current Control Program (CCtlPgm), an analog input derived from Vterm
84	MVREF	1	A	Memory Voltage Reference, an analog input from the Rambus Vref

4-3. Video Interface ; 22 Pins

Pin Number of Mpact	Symbol	# of Q`ty	Type	Function
110	VVS	1	I	Video Vertical synchronization
74	VHS	1	I	Video Horizontal Synchronization
111	VODD	1	I	Video odd field indicator
112	VCREF	1	I/O	Video Pixel clock Reference.
113	VHREF	1	I/O	Video Horizontal reference.
114-117, 122-127, 129, 131, 133, 135-137	VDATA [0:15]	16	I/O	Video data, YUV
119	VCLK	1	I	Video clock. Twice the pixel rate

4-4. Display Interface ; 30 Pins

Pin Number of Mpact	Symbol	# of Q`ty	Type	Function
194-195, 197, 199, 201,203-204, 206,208-209, 212-220, 217, 219-220, 222, 224-227, 231-232	DDATA [23:0]	24	O	Display data, RGB
233	DBLNK	1	O	Display Blanking
234	DVS	1	O	Display Vertical sync.
236	DCS	1	O	Display Composite sync.
237	DHS	1	O	Display Horizontal sync.
239	DCLKI	1	I	Display clock Input. Pixel clock source.
229	DCLKO	1	O	Display clock Output. Pixel clock.

4-5. Peripheral I/O Interface - Parallel ; 19 Pins

Pin Number of Mpact	Symbol	# of Q`ty	Type	Function
139, 141, 143-145, 147, 149, 152	PDATA [7:0]	8	I/O	Peripheral parallel data
182	-PJYEN	1	O	Peripheral parallel joystick input enable. Enables joystick register onto PDATA.
177	-PAXEN	1	O	Peripheral auxiliary control input enable. Enables auxiliary control input onto PDATA.
190	-PPIEN	1	O	Peripheral Parallel data input enable. Enables I/O parallel bus onto PDATA.
192	-PPOEN	1	O	Peripheral Parallel data output enable. Enables DO register onto I/O parallel bus.
178	-PREQL	1	O	Peripheral Parallel Request Input Enable, Low Byte. Enables requests onto PDATA.
179	-PREQH	1	O	Peripheral Parallel Request Input Enable, High Bytes. Enables requests onto PDATA.

Pin Number of Mpact	Symbol	# of Q`ty	Type	Function
184	PPACK	1	O	Peripheral parallel address register clock. Clocks PDATA data into address registers.
185	PCSCK	1	O	Peripheral chip select register clock. Clocks PDATA data into chip select register.
189	PPDCK	1	O	Peripheral parallel data register clock. Clocks PDATA data into DO register.
183	PJYCK	1	O	Peripheral joystick register clock.Clocks joystick data into joystick input register.
186	PCOCK	1	O	Peripheral control output register clock. Clocks PDATA data into control out register.

4-6. Peripheral I/O Interface - Serial ; 16 Pins

Pin Number of Mpact	Symbol	# of Q`ty	Type	Function
174,169,164, 158	PSCLK [0 :3]	4	I	Peripheral Serial Clock Inputs, Channels 0-3
171,167,161, 156	PSSYN [0 :3]	4	I	Peripheral Serial Synchronization inputs, Channels 0-3
172,168,162, 157	PSDI [0 :3]	4	I	Peripheral Serial Data Inputs, Channels 0-3
176.170, 166 160	PSDO [0 :3]	4	O	Peripheral Serial Data Outputs, Channels 0-3

4-7. Peripheral I/O Interface - Special ; 5 Pins

Pin Number of Mpact	Symbol	# of Q'ty	Type	Function
155	PMSD	1	I/O	Peripheral Mpact Serial Bus Data
154	PMSC	1	I/O	Peripheral Mpact Serial Bus Clock
187	PB0	1	O	Peripheral Programmed output Bits 0
188	PB1	1	O	Peripheral Programmed output Bits 1
153	PROM	1	I/O	Peripheral System Identification ROM, Serial input/output

4-8. Test Interface ; 3 Pins

Pin Number of Mpact	Symbol	# of Q'ty	Type	Function
71	TDI	1	I	Test data Input. PSDO0 is also TDO, Test data output
72	TMS	1	I	Test mode select
73	TCLK	1	I	Test clock

* TDO/PSDO0 ; 176 Pin

4-9. Power ; 82 Pins

Pin Number of Mpact	Symbol	# of Q'ty	Type	Function
24,37,60,79,90 92,97,101,109, 128,150,163, 173,200,216, 240	V_{DD}	16	P	+3.3 volt power supply, core
13,41,63,118, 138,159	V_{5DD}	6	P	+5 volt power supply, I/O. Input clamping level. Should be 5.0 Volts in mixed 5/3.3-Volt supply voltage systems. maybe 3.3 Volts in 3.3-volt only supply voltage systems.

Pin Number of Mpact	Symbol	# of Q`ty	Type	Function
196,205,210 221,228,235	V_{DD1}	6	P	+3.3 volt power supply, display interface
8,18,30,43,52 65	V_{DD2}	6	P	+3.3 volt power supply, PCI bus interface
140,146,180,191	V_{DD3}	4	P	+3.3 volt power supply, peripheral interface
120,134	V_{DD4}	2	P	+3.3 volt power supply, video interface
96	V_{DDA}	1	A	+3.3 volt power supply, analog, memory interface
1,26,39,61,75, 77,81,85,87, 89,91,99,103, 105,107,130 151,165,175 202,218	V_{GND}	22	P	Power supply ground, core
198,207,211, 223,230,238	V_{GND1}	6	P	Power supply ground, display interface
10,20,31,45, 54,67	V_{GND2}	6	P	Power supply ground, PCI bus interface
142,148,181, 193	V_{GND3}	4	P	Power supply ground, peripheral interface
121,132	V_{GND4}	2	P	Power supply ground, video interface
94	V_{GNDA}	1	A	Power supply ground, analog, memory interface

* Subscription is optional in power supply names.

4-10. Signal Name By Pin Number

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	V GND	41	V5 DD	81	V GND	121	VGND4	161	PSSYN2	201	DDATA19
2	-INTA	42	-STOP	82	MDATA3	122	VDATA4	162	PSDI2	202	VGND
3	-RST	43	V DD 2	83	V GND	123	VDATA5	163	VDD	203	DDATA18
4	CLK	44	PAR	84	MVREF	124	VDATA6	164	PSCLK2	204	DDATA17
5	-GNT	45	V GND 2	85	V GND	125	VDATA7	165	VGND	205	VDD1
6	-REQ	46	C/-B1	86	MCTRL	126	VDATA8	166	PSDO2	206	DDATA16
7	AD31	47	AD15	87	V GND	127	VDATA9	167	PSSYN1	207	VGND1
8	V DD 2	48	AD14	88	MDATA4	128	VDD	168	PSDI1	208	DDATA15
9	AD30	49	AD13	89	V GND	129	VDATA10	169	PSCLK1	209	DDATA14
10	V GND 2	50	AD12	90	V DD	130	VGND	170	PSDO1	210	VDD1
11	AD29	51	AD11	91	VGND	131	VDATA11	171	PSSYN0	211	VGND1
12	AD28	52	V DD 2	92	VDD	132	VGND4	172	PSDI0	212	DDATA13
13	V5 DD	53	AD10	93	MTXCK	133	VDATA12	173	VDD	213	DDATA12
14	AD27	54	V GND 2	94	VGNDA	134	VDD4	174	PSCLK0	214	DDATA11
15	AD26	55	AD9	95	MRXCK	135	VDATA13	175	VGND	215	DDATA10
16	AD25	56	AD8	96	VDDA	136	VDATA14	176	PSDO0/TD0	216	VDD
17	AD24	57	C/-B0	97	VDD	137	VDATA15	177	-PAXEN	217	DDATA9
18	V DD 2	58	AD7	98	MDATA5	138	V5DD	178	-PREQL	218	VGND
19	C/-B3	59	AD6	99	VGND	139	PDATA7	179	-PREQH	219	DDATA8
20	V GND 2	60	V DD	100	MDATA6	140	VDD3	180	VDD3	220	DDATA7
21	IDSEL	61	V GND	101	VDD	141	PDATA6	181	VGND3	221	VDD1
22	AD23	62	AD5	102	MEN	142	VGND3	812	-PJYEN	222	DDATA6
23	AD22	63	V5 DD	103	VGND	143	PDATA5	183	PJYCK	223	VGND1
24	V DD	64	AD4	104	MDATA7	144	PDATA4	184	PPACK	224	DDATA5
25	AD21	65	V DD 2	105	VGND	145	PDATA3	185	PCSCK	225	DDATA4
26	V GND	66	AD3	106	MDATA8	146	VDD3	186	PCOCK	226	DDATA3
27	AD20	67	V GND 2	107	VGND	147	PDATA2	187	PB0	227	DDATA2
28	AD19	68	AD2	108	MCCP	148	VGND3	188	PB1	228	VDD1
29	AD18	69	AD1	109	VDD	149	PDATA1	189	PPDCK	229	DCLKO
30	V DD 2	70	AD0	110	VVS	150	VDD	190	-PPIEN	230	VGND1
31	V GND 2	71	TDI	111	VODD	151	VGND	191	VDD3	231	DDATA1
32	AD17	72	TMS	112	VCREF	152	PDATA0	192	-PPOEN	232	DDATA0
33	AD16	73	TCLK	113	VHREF	153	PROM	193	VGND3	233	DBLNK
34	C/-B2	74	VHS	114	VDATA0	154	PMSC	194	DDATA23	234	DVS
35	-FRAME	75	V GND	115	VDATA1	155	PMSD	195	DDATA22	235	VDD1
36	-IRDY	76	MDATA0	116	VDATA2	156	PSSYN3	196	VDD1	236	DCS
37	V DD	77	V GND	117	VDATA3	157	PSDI3	197	DDATA21	237	DHS
38	-TRDY	78	MDATA1	118	V5DD	158	PSCLK3	198	VGND1	238	VGND1
39	V GND	79	V DD	119	VCLK	159	V5DD	199	DDATA20	239	DCLK1
40	-DEVSEL	80	MDATA2	120	VDD4	160	PSDO3	200	VDD	240	VDD

5. Functional Descriptions

5-1. System Configuration Overview

The functionality and performance of the x86 PC has steadily increased to meet the demands of multimedia. This has been through higher host x86 performance and a variety of peripheral processors and accelerator boards designed for specific media related functions. Commercial success has brought some generally accepted standard functions, hardware interfaces and, importantly with Windows95, the DirectX family of uniform Application Programming Interfaces (APIs).

The high functional density and speed of submicron integrated circuit technology now allows all of the special multimedia processing to be combined in one programmable processor. Also, Rambus technology now provides low cost, but high bandwidth dynamic memories to support graphics and video buffer needs.

The Mpact media processor system architecture is an innovative mixture of the host CPU and its memory structure, the Mpact chip (including what amounts to an on-chip cache), the Mpact main memory, and various channel hardware to support the video, audio, and peripheral device. The Mpact media processor is on the host PCI bus for a tightly coupled sharing of the multimedia tasks being executed.

The arithmetic and display buffer intensive portions of the tasks are done in a Very Long Instruction Word (VLIW) Central Processing Unit (CPU) that operates out of a shared eight port SRAM. The CPU has five execution units operating in parallel from a single 72-bit instruction word. The software is split among an x86 host-based resource manager, an Mpact-based real time kernel, and various drivers for the individual devices.

The 4KB SRAM is organized into 512 words of 72 bits each. Software partitions this memory into instruction and data areas, with the instruction area configurable to 256, 512, or 1K bytes. The instruction side is a direct-mapped cache with a 128-bytes line size. The data side is self-managed, looking more like scratch-pad memory with no real line size. Data is moved in 72-bit in the RDRAM for data instead of parity.

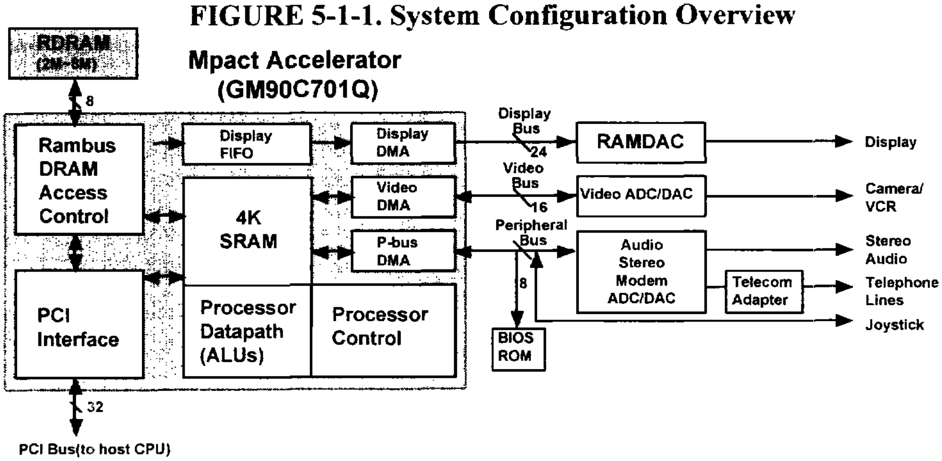
Prefetching is done only by explicit instruction direction, and it is done in address order.

Mpact mediaware's programs are written carefully to avoid any prefetching delays. The SRAM has simultaneously in a single cycle. One write port is typically dedicated to the RDRAM interface and one to a DMA channel ; the other two are general-purpose.

- ***Display***

• For high resolution 24-bit RGB color RAMDACs and PC monitors.

FIGURE 5-1-1. System Configuration Overview



- *Video*
  - For YUV digital video from analog or digital sources and to analog or digital displays.
- *Peripheral I/O*
  - For serial and peripheral digital audio and telephony codecs, digital interfaces to joysticks and MIDI, and the BIOS and plug and play ROMs, Microprogrammable for flexibility.
- *Memory*
  - For 9-bit-wide modules of 500 MB/s Rambus media memory. Normal configuration uses one 2 MB RDRAM.
- *PCI Bus*
  - A 132 MB/s burst connection to the x86 host system.

5-1-1. Dual Instruction Execution

Mpact media processor has a straightforward instruction model with a few advanced features. The very long instruction word is an eight-byte instruction pair. They instructions may be three, four, or five bytes in length, with pairing done by hand or using Mpact mediaware's compiler. Resource conflicts may cause the instructions to be executed sequentially, but even so, packing two instructions together helps with code density.

An instruction typically consists of one byte of opcode, two source bytes, and one destination byte. these 9 bit source and destination addresses can access any 72-bit word in the on-chip SRAM. Other instruction forms include a three-byte format for two-operand instructions and a five-byte format that allows four-operand calculations such as multiply-add.

An instruction count register creates a repeated vector that can improve code density and speed inner loops. The vector operations are coded only in eight-byte instruction pairs and have a maximum iterations count of 127.

Vector loads transfer data from the RDRAM to the SRAM at 500 Mbyte/sec. A vector operation can move as many as 256 bytes. Branches are simple two-byte immediate, allowing a maximum code size of 1M in the Mpact RDRAM.

Two forms of each conditional-branch instruction--branch likely and branch unlikely--allow static prediction set by the programmer or compiler. Conditionals are only on the sign of a result ; there are no other condition codes.

The 9-bit bytes lend themselves nicely to 16-bit audio applications, providing two bits of extra precision for intermediate results. This structure avoids the need to go to 24 bit data, which would use more space and time.

5-1-2. Hundreds of Adders

The five function units that call ALU groups. Each group consists of essentially an eight-byte (72-bit) arithmetic unit that can operate on one, two, four, or eight bytes at a time. Thus, they can be configured to do eight 9-bit ALU operations in one cycle, giving very good performance at the lower precision required by many multimedia algorithms.

Generally, only one ALU group is active per instruction (two for an instruction pair). Multiplies and special inner loop instructions can activate more than one group. To achieve the rated 2.0 BOPS, all four standard ALU groups must be processing eight bytes per cycle at the 62.5 MHz clock speed.

Each group has a specialization. Group 1 is a shift/align unit, while Group 2 is a standard ALU. Multiplication uses Group 3 and 4. The multiplier can be configured to produce eight 9 x 9 18-bit multiplies, four 18 x 18 36-bit multiplies, or two 24 x 24 36-bit multiplies. Alternatively, Group 3 can be used as a dual three-input adder.

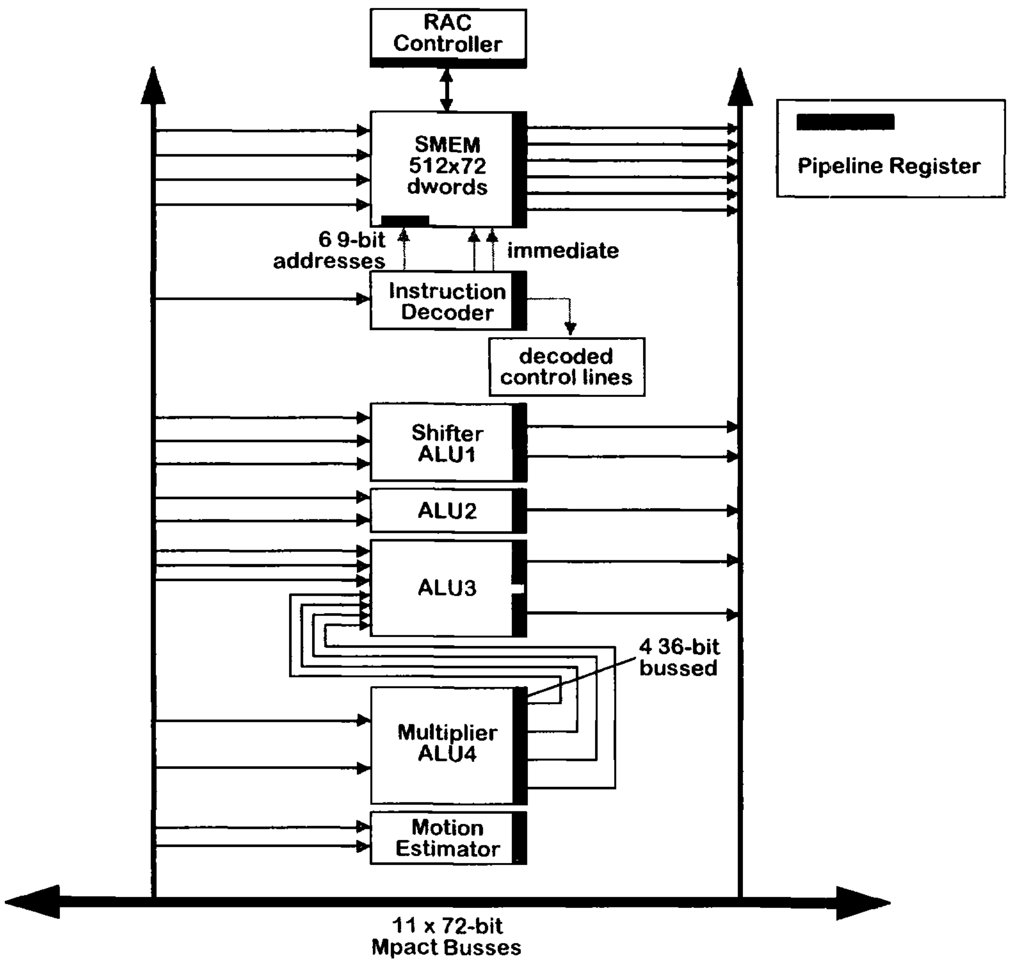
Finally, Group 5 is a specialized motion-estimation unit with some 400 ALUs, most consisting of a few bits.

All these units are connected by a crossbar bus that can place any result into any input for the next cycle. This requires a massive 792-bit unidirectional bus with a single source (11 results of 72 bits each) and 19 taps.

The pipeline has just four stages ; fetch, decode, execute, and writeback.

The leisurely clock rate allows SRAM data to be read and used in the same cycle (no load-use penalty). Splitting multiplication between two ALU groups allows it to be fully pipelined with one-cycle throughput and two-cycle latency. Correctly predicted branches have no penalties, whereas writeback stages up to 127 times before moving on.

FIGURE 5-1-2. Data Path Structure



5-1-3. Internal Block Diagram

The Mpact media processor is implemented in 0.5 μm three-layer-metal CMOS and consumes 1.5 million transistors.

The 62.5 MHz Mpact media processor operates at 3.3 V but tolerates 5 V input. The package is a 240-pin heat slugged PQFP.

The Mpact media processor is on the host PCI bus for tightly coupled sharing of the multimedia tasks being executed.

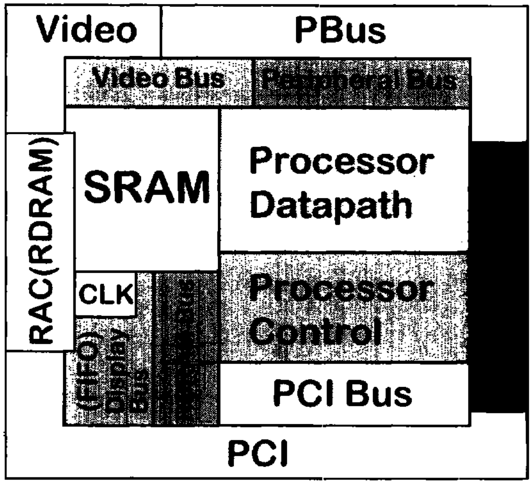
The arithmetic and display buffer intensive portions of the tasks are done in a very long instruction word (VLIW) central processing unit (CPU) that operates out of a shared eight port SRAM.

The CPU has five execution units operating in parallel from a single 72-bit instruction word. Five controllers share the SRAM with the CPU to concurrently support the wide variety of multimedia peripherals shown in FIGURE 5-1-3.

An Mpact media processor is composed of the interconnected functional hardware units shown in the block diagram of FIGURE 5-1-4. The five interface controllers with their associated memory or FIFOs share the 4 Kbyte multiport SRAM with the central processing unit (CPU). The basic bus width is that of a double word of eight 9-bit bytes for a total of 72-bits. Wider buses are shown with multiples of this basic width in parenthesis. Most interconnection is by crossbar connection to a 792-bit bus that allows multiple data sinks for an aggregate bandwidth of 9.0 GB/s.

Transfers are controlled by the instructions executed by the CPU in combination with the interface controllers whose operation is setup by the CPU. The FIFOs on the non-memory interfaces ensure steady I/O flows and a direct link to the display interface from the RDRAM media memory maintains the display.

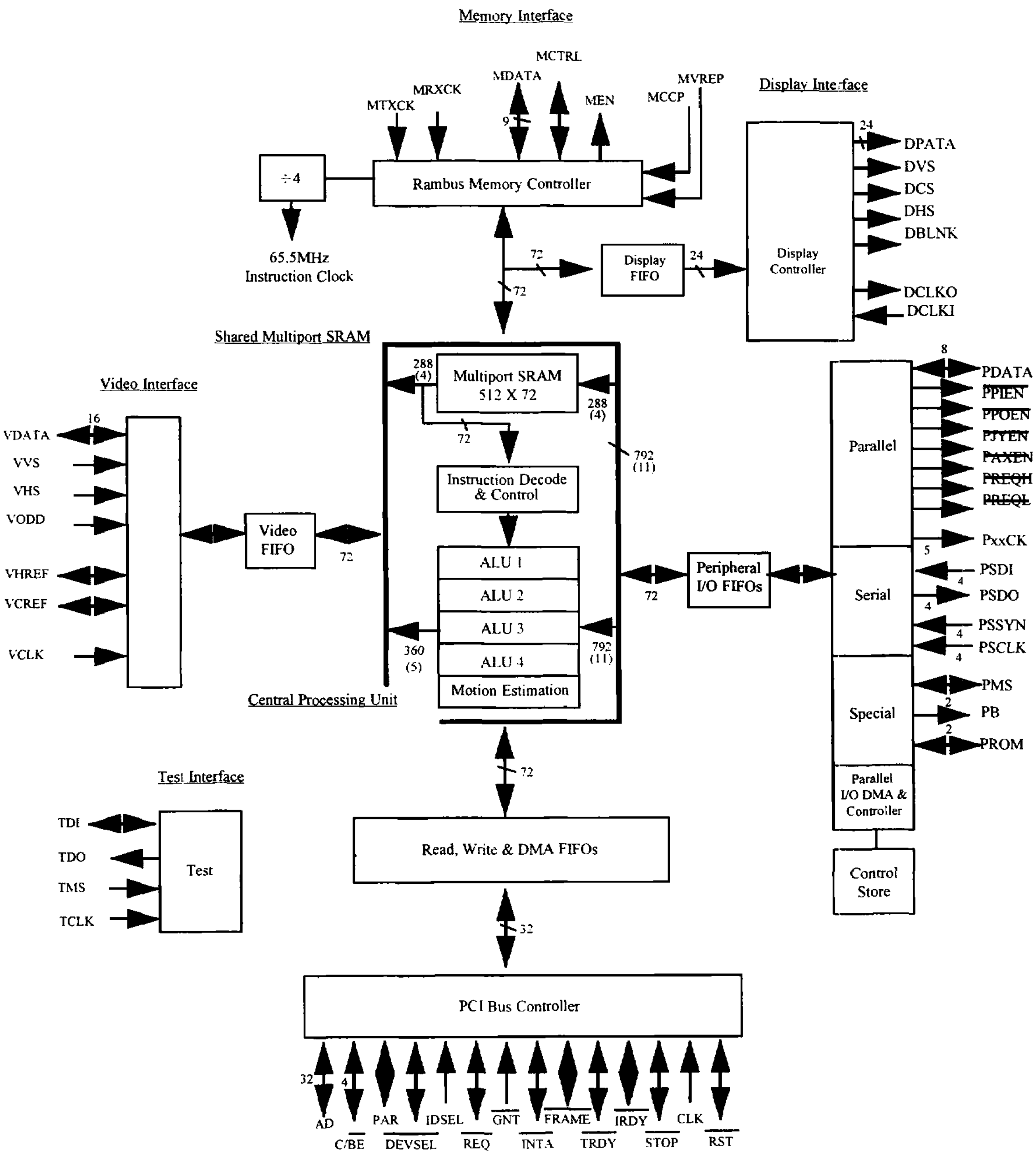
FIGURE 5-1-4. Mpact Floor Design



5-1-3-1. Instruction Execution

The central processing unit consists of four arithmetic/logic unit (ALU) groups, a motion estimation unit and the instruction decode and control. The Mpact media processor is a very long instruction word (VLIW) processor where each instruction word is 72 bits. Each word is composed of two instructions that are 3 to 5 bytes in length each. Instructions cause multiple operations within a group and even multiple operations in multiple groups. A single instruction word can cause 8 single-byte operations to be executed on each of the four ALU groups for sustained rates of 2 billion operation per second (2 BOPS). Peak rates can reach 3 BOPS. Instruc-tion memory efficiency is high because of vector and block repeat instructions.

FIGURE 5-1-3. The GM90C701Q Internal Block Diagram



5-1-3-2. Shared Multiport SRAM

All CPU instructions are fetched out of the shared multiport SRAM and most data operations are on data stored there. The simultaneous four read and four write ports provide a steady flow of instructions and data to the CPU, allow I/O buffers to be maintained in the SRAM and execute load and store instructions with the RDRAM media memory. The 4 Kbytes SRAM is organized as 512 double words of 8 bytes each. The CPU maintains the cache of data and instructions in the SRAM from the RDRAM media memory.

5-1-3-3. ALU 1

Each ALU group operates on double words of 8 bytes which can be 1, 2, 4 or 8 operands. ALU 1 is a shift and align group which uses three inputs for extensive crossbar operations to produce two results.

5-1-3-4. ALU 2

ALU 2 is a general purpose ALU prop with two inputs and a single output result except for special FFT butterfly instructions which produce a sum and difference result.

5-1-3-5. ALU 3 & 4

ALU 3 is a general purpose ALU group without the butterfly operational but it is augmented with three inputs for ternary operations that produce two results. ALU 4 uses Booth encoders in a structure to produce various precisions of multiply and multiply-add operations in combination with ALU 3 which outputs the results.

5-1-3-6. Motion Estimation Unit

The motion estimation unit consists of some 400 arithmetic elements which produce an additional 20 BOPS performance for MPEG motion estimation. Five controllers share the SRAM with the CPU to concurrently support the wide variety of multimedia peripherals shown in Figure 5-1-5.

These peripherals, the media buffer memory and PCI bus connect through five distinct interfaces whose signals are summarized in 4. Pin Descriptions.

The Mpact media processor connects to a 32-bit host CPU through a PCI bus.

The Mpact media processor connects to a 32-bit host CPU through a PCI bus. The Mpact media processor includes bus interfaces for speedy processing of multimedia data, outlined as follows ;

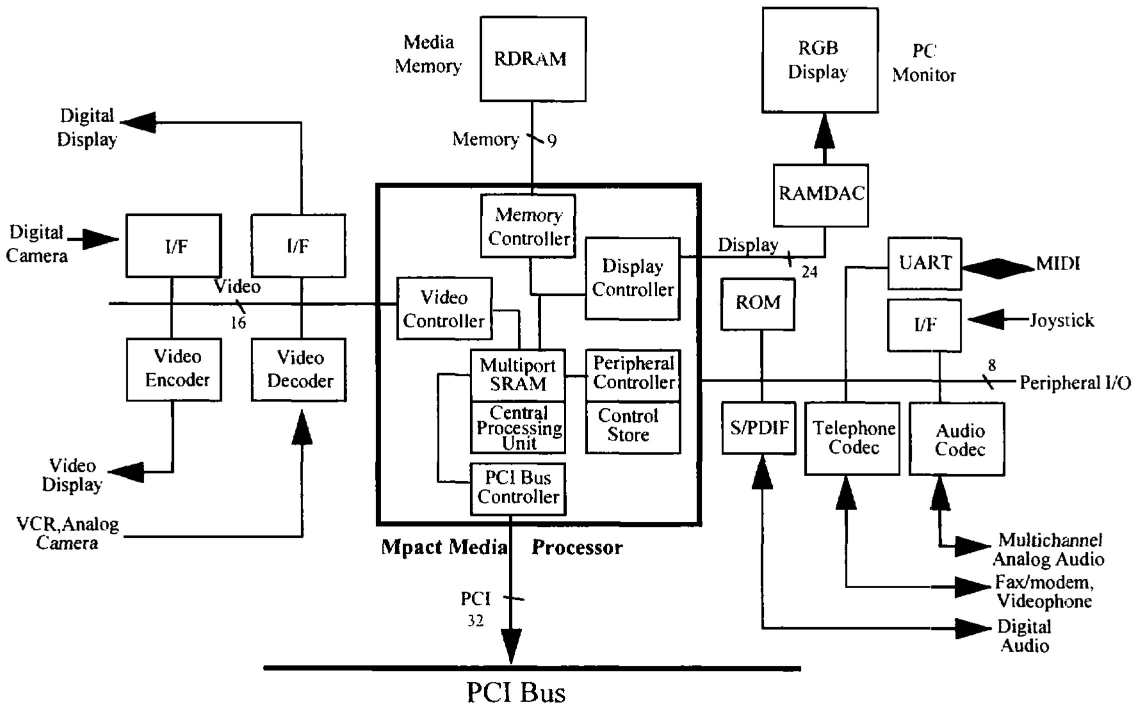
* Host Bus — 32-bit PCI bus with master interfaces, Supports Plug and Play conventions
* Memory Bus — Rambus DRAM through the Rambus Access Controller (RAC)
* Display Bus — RAMDAC video out, 24-bit maximum
* Peripheral Bus — 8-bit peripheral bus supports the following ;
  Digital audio
  - Sound Blaster, Sound Blaster Pro, and
  - Sound Blaster 16
  - Audio compression and decompression
  Joystick
  FAX / Modem
* Digital Video Bus — 9-bit video interface supports MPEG video decoder and encoder Video in

The Mpact media processor has a 72-bit architecture.

All accelerations and other operations are programmed as integer processes. In addition to the Mpact media processor and its controller, the Mpact chip contains the following controllers ;

- Bus controller
- RAC controller
- Display controller
- Video Bus controller
- Peripheral Bus controller

FIGURE 5-1-5. A CPU and Five I/O Controllers Operating Out of a Multiport SRAM Concurrently Service the elements of a multimedia



5-2. Comprehensive System Design

Applications, when running, invoke various functions through their API or hardware view. These become single or multiple individual tasks related to the I/O port that is involved ; Video tasks use the Video port, 2D and 3D graphics use the display port, digital audio tasks use the Audio port, Fax/modem, Telephony and Videoconferencing use the Telephone port and the joystick, MIDI and ancillary functions use the general Port. A port is a logical distinction which may combine more than one electrical interface and is I/O device specific for the system.The host accesses the Mpact media processor through the PCI bus interface controller. The bus controller is connected to the core of the chip through a queue.

The queue head receives requests from the host and decides which part of the chip should handle them. The queue head either writes data into the appropriate controller registers or into the internal 4 kbytes of on-chip static memory (SMEM). Optionally, the queue head notifies the RAC controller to forward a copy into RDRAM.

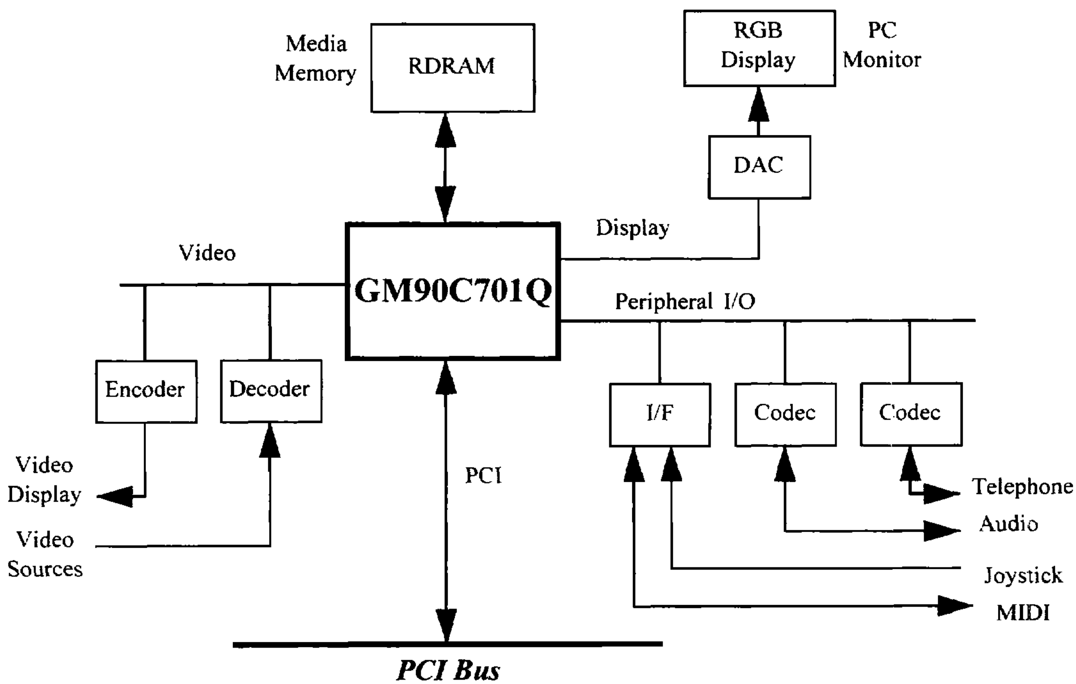
The timing generator can be programmed to generate timing both for computer monitors and for NTSC and PAL video. The Mpact media processor architecture provides several advantages for high-speed processing of multimedia functions.

The Mpact media processor fetches and decodes 72-bit instructions from SMEM.

All Mpact media processor operations are performed on data stored in SMEM. The Mpact media processor reads and writes internal registers and requests the RAC controller to copy data to and from RDRAM.

The RAC controller fetches streams of video data from RDRAM and passes the data to the display FIFO. The display front-end monitors the display FIFO and requests the RAC controller to fill it when it is becoming empty. The display backend empties the display FIFO as allowed by the display timing generator.

FIGURE 5-2-1. Comprehensive System Design Overview



5-2-1. SIMD

The Mpact media processor has a single instruction multiple data (SIMD) architecture. In order to achieve high performance, a single Mpact media processor instruction operates on packed groups of data elements.

5-2-2. VLIW

The Mpact media processor also is classified as having very long instruction word (VLIW) architecture. It can issue instructions and data to more than one instruction unit per clock cycle. Unlike superscalar designs, the VLIW architecture places the burden of dependency checking on the compiler rather than the hardware.

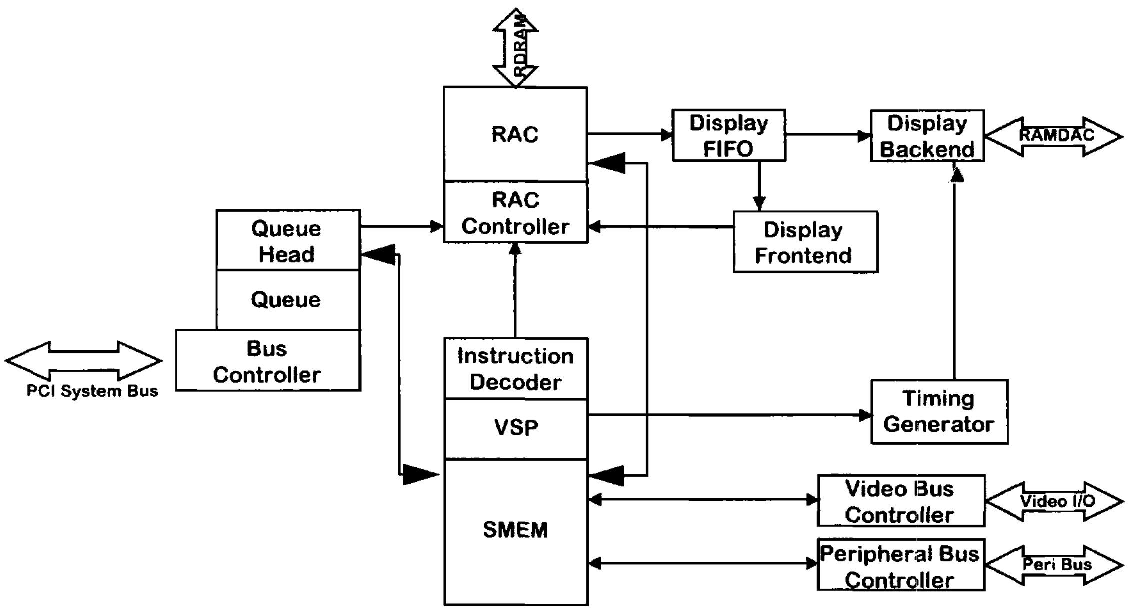
5-2-3. Memory Management

The Mpact media processor data at high rates between RDRAM and SMEM. The Mpact media processor uses direct mapped memory registers to transfer data to and from the various busses. The queue head controls accesses to the host and view into RDRAM. Although RDRAM contains 16 megabytes, many of the views map only into 2 megabytes of the 16.

The all-memory views map into all 16 megabytes of RDRAM. The views take up much the Mpact media processors 128 megabytes of address space.

The process status register and 3-bit control register contain 21 bits for mapping Mpact media processor instruction code from SMEM directly into 2 megabytes of RDRAM.

FIGURE 5-2-2. VLIW (Very Long Instruction Word) Structure



5-2-4. RDRAM

The bulk of Mpact media processor's memory is kept off chip in a special type of DRAM known as RDRAM (Rambus DRAM).

RDRAM uses the RAMBUS protocol to transfer bursts of data a narrow channel. A Mpact media processor system uses 2 or 16 MB of RDRAM. The RDRAM holds the frame buffer that generates the video display, and those Mpact media processor programs and data not resident on-chip. Each byte of RDRAM contains 9 bits.

The RDRAMs provides a fast memory that transfers display data at 500 MB per second. The Mpact media processor drivers use memory tiling to accommodate a variety of display formats. The tiling algorithm optimizes the RDRAMs 2 K cache line burst reads and writes to speed access of display data.

The RAC controller transfers blocks of memory between SMEM and RDRAM. The functional units of the MPACT media engine cannot access RDRAM directly. Although there is variable latency from the request of a transfer and start of the actual transfer, once the transfer is initiated it proceeds at a rate of one double every clock cycle.

Read and write requests between SMEM and RDRAM are queued. The queue can hold up to two pending requests. Programmers must manage the queue during task switching.

RDRAM is generally addressed indirectly, since an SMEM register specifies a byte of RDRAM. In contrast, SMEM addresses are specified directly. For instance, even though the indices of an array increment automatically during a vector operation, the vector instruction uses the same registers the next time it executes.

5-2-5. SMEM

SMEM, the Mpact media processor's on-chip static RAM, provides 4 KB of memory for Mpact media processor programmers. Although the Mpact media processor does not depend heavily on registers, programmers can think of SMEM as a general purpose register file of up to 4 KB.

In addition to holding temporary buffers for data. SMEM is arranged as 512 double words of 72 bits each. Since there is no way to read or write fewer than 72 bits, one of the functional units must perform a read / modify / write operation to update part of an SMEM double.

SMEM contains both data and instructions. since the Mpact media processor does not provide a protected mode, its programmers must manage the SMEM allocation for each type of information.

Read and write requests between SMEM and RDRAM are queued. The queue can hold up to two pending requests. Programmers must manage the queue during task switching.

Although instructions may use any of the 512 doubles contained in SMEM, TABLE 5-2-1 describes the double words reserved by the kernel for temporary values, FIFO buffers and other purposes.

SMEM reserves the kernel area at all times.

The currently running ISR owns the ISR data portion of SMEM. ISRs should be small enough for interrupts to be off as they process. So, by convention, if an ISR requires more than 3 us to process, including called kernel services, it should use the task data portion of SRAM and enable other interrupts.

FIGURE 5-2-3. SMEM Read and Write Ports

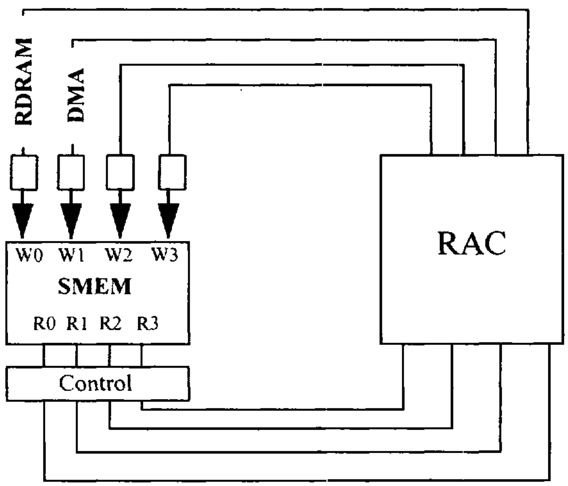


TABLE 5-2-1. SMEM kernel Allocation

SMEM Range		Purpose	Size
0 - 127	0x000 - 0x07F	Instruction Cache	128
128 - 415	0x080 - 0x19F	Task data	288
416 - 427	0x1A0 - 0x1AB	kernel	12
428 - 447	0x1AC - 0x1BF	Interrupt Service Routine (ISR)	20
Hardware-Specific			
448 - 459	0x1C0 - 0x1CB	Peripheral bus DMA buffers	12
460 - 463	0x1CC - 0x1CF	Extra kernel registers	4
464 - 495	0x1D0 - 0x1DF	PCI FIFO	16
480 - 495	0x1E0 - 0x1EF	ISA Emulation FIFO	16
496 - 511	0x1F0 - 0x1FF	Video FIFO	16

5-2-6. Instruction Set / Format

The Mpact media processor packs two instruction words into one 72-bit double word. The instruction words vary in length, requiring three, four, or five bytes.

Since the program counter points to an aligned double word, instruction doubles can never cross double word boundaries. The arguments represent 9-bit immediate or pointer to one of 512 doubles in SMEM. The Mpact media processor supports instruction pairing. The following diagram illustrates how two 4-byte instructions are partitioned into two instruction words ;

opcode1	opcode0	argA1	argA0	argB1	argB0	argC1	argC0

This section has the formats of the Mpact media processor instructions.

- Primary format
- Secondary format
- Instruction modes
- Generic instruction syntax
- Addressing modes

The Mpact media processor have several formats. The two main formats are as follows ;

- Primary format opcodes are contained in a single bytes
- Secondary format opcodes use an escape sequence that continues the opcode in argB of the instruction word.

5-2-7. Mpact Resource Manager-MRM

Operational tasks are executed on the x86 host, the media processor or both as determined by the MRM resource manager operating on the host. MRM performs dynamic real-time task linking and loading based on the resources available as well as providing a backoff or graceful degradation strategy when either is over subscribed.

5-2-8. Mpact Real-time Kernel-MRK

The MRK dynamically schedules and dispatches tasks based on nearest deadlines. It is Mpact media processor resident and can be pre-emotive to meet the nearest deadline requirements.

5-2-9. Mpact Audio Processing Manager - MAPM

Real-time audio related tasks are controlled by a sub-task processing manager to ensure that synchronous audio operations are maintained without interruption. The human ear is more sensitive to time lapses than the eye is to the lapse's visual effects.

5-2-10. Memory Resources

FIGURE 5-2-4 shows the five memories managed by the Mpact Resource manager. All media processor operations, including the MRK control, are from instructions resident in its multiported SRAM. Task instructions and corresponding SRAM data buffers are kept current from the media memory. The media memory also contains graphic and video display and audio buffers which are maintained directly by the processor and controllers.

The Peripheral I/O controller microcode executes out of its control store RAM.

Normally all I/O routines can be resident, with only error handling needing to be downloaded from the media memory on a demand basis. Boot initialization routines for the media processor and extended BIOS reside in the ROM on the Peripheral I/O interface.

All other operational software is resident on the x86 host memory system and managed by the MRM. The Mediaware modules are easily updated for new functionality using diskettes, CD-ROMs or by using on-line services.

5-2-11. Register Overview

The Mpact media processor supports instruction pairing. The following diagram illustrates how two 4-byte instructions are partitioned into two instruction words ;

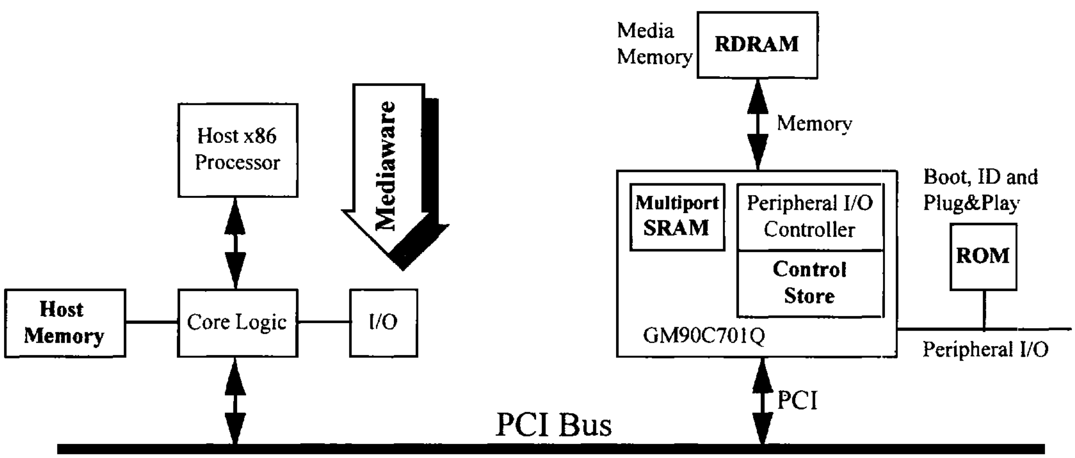
This section has the formats of the Mpact media processor instructions.

- Primary format
- Secondary format
- Instruction modes
- Generic instruction syntax
- Addressing modes

TABLE 5-2-2. Register Sets

Register Sets	function
Mpact Registers	controls the operation of the Mpact media processor's on-chip processor
Queue head registers	control data transfer to end from the host over the PCI bus
Peripheral bus registers	controls data and instruction transfer to and from the devices on the peri-pheral bus
RAC contro-ller registers	set up timing and tiling options for controlling access to RDRAM
Display controller registers	control the display options and the display timing registers control display timing

FIGURE 5-2-4. Real-Time Multimedia Operation Utilizes Mpact mediaware modules resident in Five Memories.



Register Set	function
Display timing control RAM registers	-
Video bus registers	control data and instruction transfer to and from the devices on the video bus
Lock bit registers	provide test-and-set and test-and-clear semaphores for controlling task swi-tching
Result registers	forward results of one ALU to another and provide pointers
Process status registers	-

5-3. System Interface

5-3-1. Input/Output Interface and Port

Of the five interface on the media processor, three are used for system input/output devices : the Display, the Video and the Peripheral I/O interfaces. A typical I/O device uses signals from more than one interface. The combination of signals from various interface to support a particular class of I/O device and its associated mediaware is called a port. There are five classes of ports for display, video, digital audio, telephone and general digital devices. Table 5-3-1 lists available ports and the interfaces signals that are used in each. Each port supports different functions and specific commercial devices for that function. Example ports and devices are illustrated in FIGURE 5-3-1.

5-3-1-1. Video Port

The video port is used for direct digital video input or output in the 4:2:2 YUV format of CCIR 601. The video interface signals can be used directly for most digital video cameras, solid-state digital display or the Zoom Video interface.

Analog video is input through decoders and output through encoders. Data is transferred on the video interface with Mpact Serial and/or the Peripheral I/O parallel interface used for control functions.

5-3-1-2. Display Port

The display port is used for the PC monitor`s RGB color display or with an encoder for an RGB video color display. Data is transferred on the display interface with the Mpact Serial and /or the Peripheral I/O parallel interface used for control functions.

5-3-1-3. Digital Audio Port

The digital audio port is used for both analog codecs and digital S/PDIF devices for input and output. Data is transferred on the Peripheral I/O interface along with control.

5-3-1-4. Telephone Port

The telephone port uses the Peripheral I/O interface for supporting telephony, fax/modem and videoconferencing cedecs.

5-3-1-5. General Port

The General port uses the Peripheral I/O interface for transfers with other digital support devices that are in the typical multimedia system. These include game joysticks, MIDI and the various system ROMs.

5-3-1-6. Memory and PCI Bus Interfaces

These interfaces are used for standard Rambus media memory and the industry standard 32-bit PCI bus.

5-3-1-7. Peripheral I/O Parallel Bus

The peripheral I/O Parallel Bus is formed from Peripheral I/O interface signals using discrete external buffers or an inclusive ASIC.

TABLE 5-3-1. Mpact Input/Output Ports & Interfaces

(This list of reference only)

I/O Function	Interface*	I/O Device	Remark
Video Port - YUV			
Analog output encoder ;			
NTSC/PAL	V, PP, PMS	AD7176	
		SAA7187	
Analog input Decoder ;			
NTSC/PAL/SECAM	V, PP, PMS	KS0122	
NTSC/PAL	V, PP, PMS	SAA7110	
Digital I/O :			
CCIR 601 4:2:2 YUV	V		
Display Port - RGB			
RGB 24-bit RAMDAC			
1280x1024 @ 75 Hz. 8 , 16, 18 b/p	D, PP, PMS	ATT 1178AB	
		Bt473, ADV473KP	
Digital Audio Port			
Parallel Codec			
16 bit, 48 KHz, Stereo	PP, PB	CS4231A	
		AD1845, 1848	
Serial Codec			
16 bit, 48 KHz, Stereo	PS, PB	CS4216	
S/PDIF			
Output	PP, PS, PB	CS8401	
Telephone Port			
Fax/Modem/Telephony/H.324 Videoconferencing			
V.34	PP, PS	CSP1027	
Fax/Modem/Telephony			
V.32bis	PP, PS	T7525	
Videoconferencing			
H.320 for ISDN			

* V= Video, D= Display, PP= Peripheral I/O Parallel, PS= Peripheral I/O Serial, PMS= Peripheral Mpact Serial, PB= Peripheral Programmed Bits.

(This list of reference only)

I/O Function	Interface*	I/O Device	Remark
General Port			
Joystick	PP	Ind. Std.	
System ID ROM	PROM	DS2430A	
Boot and P&P Flash EPROM	PP	AM29F010	
Boot ROM	PP	Ind. Std.	
Plug&Play Serial EEPROM	PP, PB	X84041	
Memory Interface	Memory	Rambus	
PCI Bus Interface	PCI Bus	Ind. Std.	
Peripheral I/O Parallel Bus			
Discrete Components	PP		
Glueart	PP	GM90C553TQ#	

* V= Video, D= Display, PP= Peripheral I/O Parallel, PS= Peripheral I/O Serial, PMS= Peripheral Mpact Serial, PB= Peripheral Programmed Bits.

Glueart including General UART GM16C550 and Logic Buffers)

5-3-2. PCI Bus Controller and Interface

The PCI bus controller and its three FIFOs manage access between the Mpact media processor and host x86. The interface is fully compliant with PCI Local Bus Specification, Revision 2,0 with richer 3.3 or 5-Volt signaling. Peak transfer rates are 132 MB/s on the 32-bit bus. The Mpact media processor acts as a target or a bus master with transfers being fully concurrent with the host or memory subsystem at a synchronous 33 MHz rate. Three separate FIFOs provide for variable length read and write burst operation as a target and DMA operation as a master. The DMA FIFO is eight words and the read only a single word buffer.

As determined in the PCI configuration space, the Mpact media processor appears in address space in three forms ; as 128 MB of memory, as 128 KB of extension ROM and as specific device compatibility addresses is supported. Correct 5 volt PCI bus signaling operation is assured by connecting the six V5DD power pins +5 Volts rather than +3.3 Volts.

The PCI bus controller manages X86 access to the Mpact media processor and controls the Mpact media processor registers for VGA support through the X86 interface. The PCI bus controller contains a queue head that manages both x86 access to the Mpact media processor and on-chip data transfer. XOS, the Mpact media processor's kernel, uses the queue head to control SMEM write and read access registers for VGA emulation for the x86 interface.

The Mpact media processor bus controller receives 32-bit addresses from the system bus. The bus interface qualifies the address data as read or write for I/O space or memory space. It accepts write request packets that consist of 32-bit packets of data, 4-bit byte enable signal, a 1-bit address tag, and 1-bit flag to indicate whether the packet is the last word in a burst.

Following the PCI frame signal specification, the address starting a new packet follows the last word in a burst. If the x86 data is an address, only the address and last word flags are included. After the last word in a burst, the next packet sent contains the address for starting the next packet. Its read packet consists of an address since the bus interface is stalled synchronously waiting for the chip core to return data.

The Mpact media processor responds to the following address spaces ;

• Memory space determined by the PCI memory space configuration register

5-3-2-1. Functional Description

The Mpact PCI Bus Interface is the media processor's link to the host x86 system. Its 48 signals and operation are fully com-pliant with the industry standard PCI Local Bus Specification, Revision 2.0 for either 3.3- or 5-Volt signaling for planar devic-es. The PCI bus controller and its three FIFOs manage access between the Mpact media processor and the host x86 with peak transfer rates up to 132 MB/second on the 32-bit bus. The PCI bus controller and its three FIFOs manage access between the Mpact media processor and the host x86 with peak transfer rates up to 132 MB/second on the 32-bit bus.

FIGURE 5-3-1. The Mpact media processor PCI Bus Interface to Host CPU

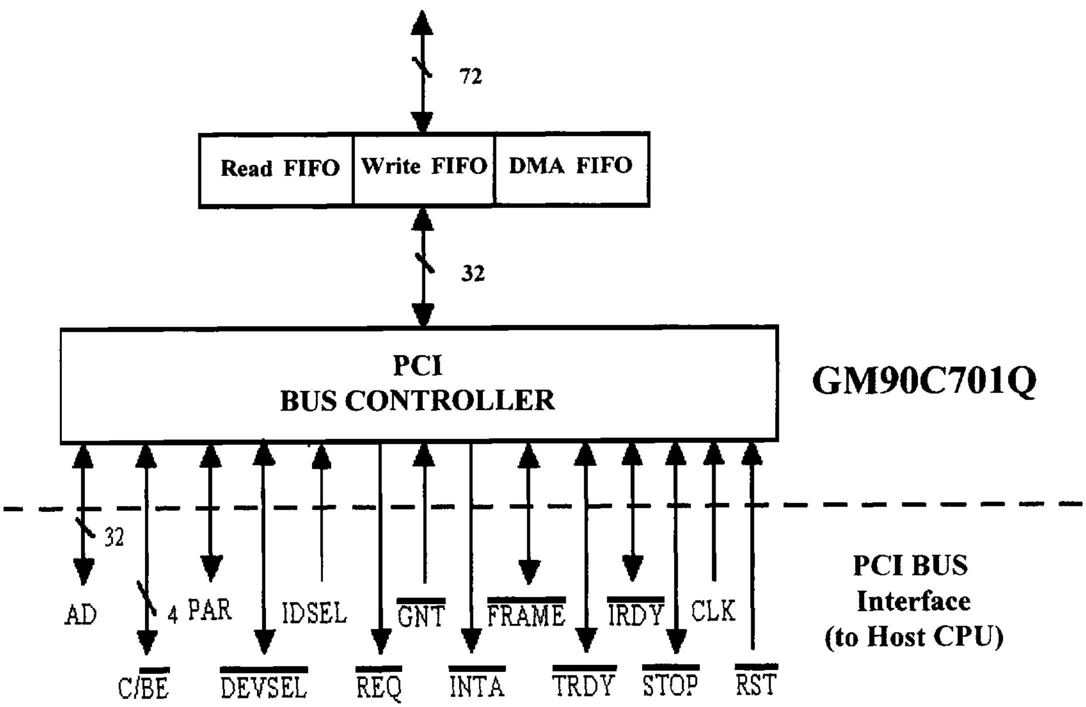
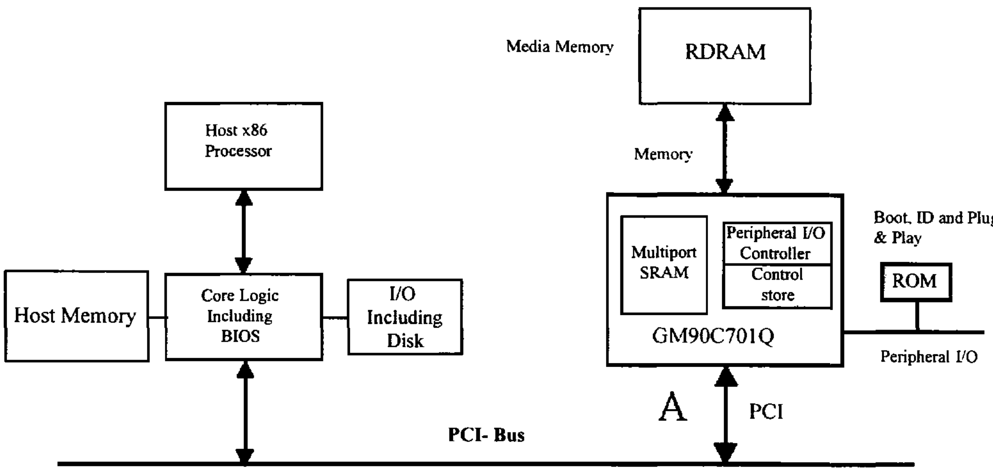


FIGURE 5-3-2. The five Different Memory Space (Shaded Blocks) In a Typical Mpact System



A : Mpact in system Address Space

The Mpact media processor acts as a target or a bus master with transfers being fully concurrent with the host and memory sys-tem at a synchronous 33-MHz clock rate.

This appendix describes the PCI Bus Interface and its operation and helps understanding Mpact reference designs including the one for the Mpact PCI Evaluation Board.

The PCI Bus Controller and FIFOs (read, write and DMA) shown in Figure 5-3-1 manage transactions with the host pro-cessor. The media processor acts as a target or bus master with transfers concurrent with the host operations with the system memory when configured in a typical system as shown in Figure 5-3-2.

As a target, it accepts memory, I/O and PCI configuration writes and reads. As a master, it initiates memory-writes. The FIFOs provide for variable length target memory-write burst operation and master DMA transactions.

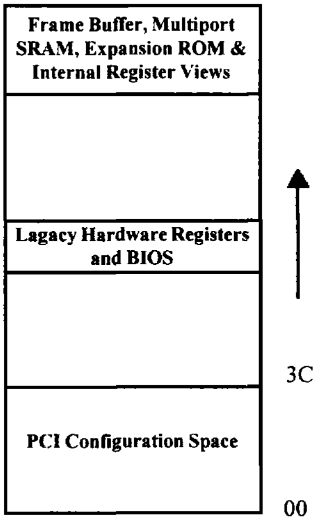
On-chip data trans-fers, access to external ROM (via the Peripheral I/O Bus) and access to registers for VGA and sound card emulation are also managed by the PCI Bus Controller. Legacy PC I/O devices re-side at predefined I/O or memory addresses that predate the PCI configuration mechanism.

5-3-2-2. Address Spaces

The Mpact media processor responds in three separate groups of locations in the system address spaces looking in at point A in Figure 5-3-2. These three groups of locations are shown in Figure 5-3-3. The PCI Configuration Space is shown expanded in Figure 5-3-4. The VGA BIOS ROM along with specific de-vice hardware registers exists at the fixed memory addresses shown in Figure 5-3-5 on the PCI bus. In high memory at an ad-dress determined in the PCI configuration space is 128 MB of memory for the media processor frame buffer, expansion ROM, multiport SRAM and internal register views.

FIGURE 5-3-3. The Mpact media Processor In The x86 System Address Spaces

A: Mpact in system Address Space



5-3-2-3. Design Considerations

There are many design considerations, both electrical and me-chanical, involved in meeting the specifications for the PCI Lo-cal Bus. The PCI Local Bus Specification, Revision 2.0 should be consulted for these. The provisions for the 33-MHz, 32-bit configuration with either 3.3- or 5.0-Volt signaling apply.

Figure 5-3-6 shows the connection of the Mpact media proces-sor with the PCI bus used in the PCI Evaluation Board. Note the following :

ⓐ Series termination resistors are used in most but not all connections between the media processor and the bus.

ⓑ The connection of TDI to TDO to keep the scan path intact.

ⓒ The grounding of pin 9B PRSNT1 on the PCI bus to indi-cate power requirements and the physical presence of the board.

ⓓ Correct 5 Volt PCI bus signaling operation is assured by connecting the six V5 DD power pins to the +5 Volt supply rather than +3.3 Volt.

ⓔ The six V GND ground pins of the media processor are connected physically close to the eighteen Ground pins of the bus.

The media processor PCI Bus Interface signal descriptions and pin numbers are given in Tables 5-3-2 and 5-3-3.

FIGURE 5-3-4. PCI Configuration Space Address Map

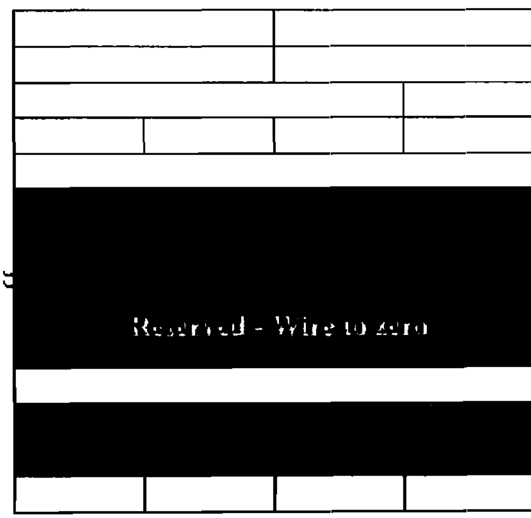


FIGURE 5-3-5. I/O Register and Memory Emulation Addresses

Emulation Description	I/O Address
COM4-1 serial port	2E8 - 2EF
	or 2F8 - 2FF
	or 3E8 - 3EF
	or 3F8 - 3FF
Industry standard sound card 2.0	220 - 22F
	or 240 - 24F
Industry standard sound card FM (OPL-3) I/O	220 - 22F
VGA Memory	Varies
VGA I/O	03Bx, 03Cx,03Dx,46E8
VGA BIOS ROM (for 32K)	C0000
MIDI (MPU-401) I/O	330 - 331
Game port, joystick I/O	201

FIGURE 5-3-6. The PCI Bus Connection to the Mpact PCI Interface on the Mpact PCI EvaluationBoard

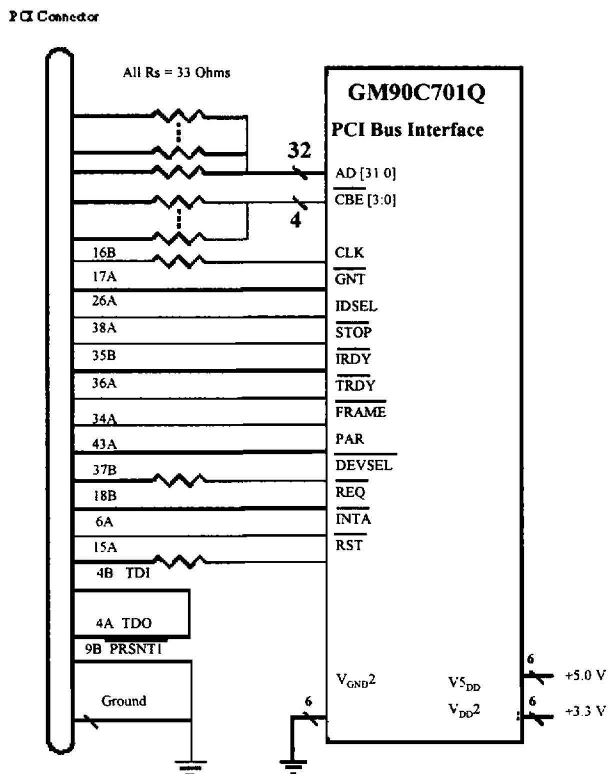


TABLE 5-3-2. Media Processor PCI Bus Interface Signals

NAME	NUMBER	TYPE	DESCRIPTION
			PCI Bus Interface (48)
AD[31:0]	32	I/O	PCI bus Address and Data
C/$\overline{\text{BE}}$[3:0]	4	I/O	PCI bus Command or Byte Enable during address transactions
PAR	1	I/O	PCI bus Parity
$\overline{\text{DEVSEL}}$	1	I/O	PCI bus Device Select. Target has decoded its address.
IDSEL	1	I	PCI bus Initialization Device Select input
$\overline{\text{REQ}}$	1	O	PCI bus master Request
$\overline{\text{GNT}}$	1	I	PCI bus master Grant
$\overline{\text{INTA}}$	1	O	PCI bus Interrupt A request
$\overline{\text{FRAME}}$	1	I/O	PCI bus Frame transaction
$\overline{\text{IRDY}}$	1	I/O	PCI bus Initiator Ready
$\overline{\text{TRDY}}$	1	I/O	PCI bus Target Ready
$\overline{\text{STOP}}$	1	I/O	PCI bus Stop transaction request by target
CLK	1	I	PCI bus Clock
$\overline{\text{RST}}$	1	I	PCI bus Reset
			PCI Bus Power (18)
$V_{DD}2$	6	P	+3.3 Volt power supply, PCI bus interface
$V5_{DD}$	6	P	+5 Volt power supply, I/O. Input clamping level. Should be 5.0 Volts in mixed 5/3.3-Volt Supply voltage systems. May be 3.3 Volts in 3.3-Volt only supply voltage systems.
$V_{GND}2$	6	P	Power supply ground, PCI bus interface

TABLE 5-3-3. Media Processor PCI Bus Interface Pin Numbers

Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number
			PCI Bus Interface (48)				
AD31	7	AD19	28	AD7	58	PAR	44
AD30	9	AD18	29	AD6	59	$\overline{\text{DEVSEL}}$	40
AD29	11	AD17	32	AD5	62	IDSEL	21
AD28	12	AD16	33	AD4	64	$\overline{\text{REQ}}$	6
AD27	14	AD15	47	AD3	66	GNT	5
AD26	15	AD14	48	AD2	68	INTA	2
AD25	16	AD13	49	AD1	69	$\overline{\text{FRAME}}$	35
AD24	17	AD12	50	AD0	70	$\overline{\text{IRDY}}$	36
AD23	22	AD11	51	C/$\overline{\text{B}}$3	19	TRDY	38
AD22	23	AD10	53	C/$\overline{\text{B}}$2	34	STOP	42
AD21	25	AD9	55	C/$\overline{\text{B}}$1	46	CLK	4
AD20	27	AD8	56	C/$\overline{\text{B}}$0	57	RST	3

PCI Bus Power (18)

Pin Name	Number of Pins	Pin Numbers
$V5_{DD}$	6	13, 41, 63, 118, 138, 159
$V_{DD}2$	6	8, 18, 30, 43, 52, 65
$V_{GND}2$	6	10, 20, 31, 45, 54, 67

• ROM space determined by the PCI ROM space configuration register

• A broad class of fixed address spaces not configured or enabled by normal PCI mechanisms, called compatibility addresses"

Aperture registers enable x86 access to all Mpact media processor registers under 1 MB in DOS real mode.

The Mpact media processor supports both 5 V and 3.3 V signaling environments of the PCI bus signals, so it can switch between the two environments. Although this section provides some information about the PCI bus Ver.2.0 and 2.1.

This Mpact media processor shows the pins to support the PCI bus for the configuration, ROM, and compatibility spaces, the aperture registers and the queue head. It decribes the registers and the memory map for the host and queue head.

The PCI bus controller manages x86 access to the Mpact media processor and controls the Mpact media processor registers for VGA support through the x86 interface.

The Mpact media processor's PCI interface supports the following features ;

- 3.3 V and 5 V signaling environment, fully PCI V2.0 and V2.1compliant
- 32-bit datapath with 132 MB/s peak bandwidth
- Drives bus as master or acts as slave to host processor
  - Provides full concurrency with processor or with memory subsystems
  - Supports variable length read and write bursts in slave mode
  - Synchronizes bus operation up to 33 MHz
- Direct memory access (DMA) support
- Provides full auto configuration for add-in cards and components

The Mpact media processor also provides support for COM ports and SoundBlaster. Other independent register sets provide flexible support for changing or emerging technologies.

The Mpact media processor uses the PCI configuration space to configure the following address spaces ;

- 128 MB of memory space
- ROM space for expansion ROM base addresses

TABLE 5-3-4. PCI Signal for Mpact

Signal[a]	Type[b]	Description
Address and Data		
AD[31:0]	B	Address and data
C/-BE[3:0]	B	Bus command(during address) and Byte enable(during data); multiplexed
PAR	B	Parity, even cver AD and C/BE#
Interface Control		
FRAME#	B	Driven by master for duration of access
TRDY#		Target ready to accept and complete data phase
IRDY#	B	Initiator ready to complete current data phase
STOP#	B	Target requests master to stop current transaction
DEVSEL#	B	Driven when device has decoded itself to be target of current transaction
IDSEL	I	Device select during initialization (config read and write)
Error Reporting		
PERR#	B	Data parity error detected
System		
CLK	I	PCI clock. All inputs sampled on rising edge except RST# and IRQ [ABCD]#
RST#	I	Reset PCI-specific state
Interrupt		
INTA#	O:od	Interrupt request,daisy-chained
Arbitration		
REQ#	O	Requesting bus ownership. Point-to-point between device and controller
GNT#	I	Bus ownership granted by controller. Point-to-point.

a A trilling # indicates active low
b Signal type coded.B, I,and O are the obvious logical types
O types may be totem pole (tp), or open drain 'od

5-3-3. Rambus Memory Controller and Interface

The Mpact media processor has a single off-chip volatile memory system for data and program storage. It is com-posed of Rambus DRAMs (RDRAMs) connected to its memory interface. This appendix explains the design and operation of this media memory system. Major design considerations are:

Supplying the special reference and termination volt-ages, drive current input and the Rambus clock which is also the main processor system clock,

- Accommodating the choice of the memory size, which can vary between 2 MB and 8 MB,
- Recognizing the special printed circuit board require-ments due to the high-bandwidth transmission line nature of the Rambus channel.

This helps understanding Mpact reference designs including the one for the Mpact PCI Evaluation Board.

The memory controller supports external Rambus DRAM media memory connected to the memory interface. Media memory is used for both data and instruction storage for transfer to the processor multiported SRAM as well as video and display data buffers.

The controller has direct access to the multiported SRAM and the display FIFO for rapid transfers with the RDRAM. All addresses are translated in the controller to provide tiling for greater transfer rates on large video and display buffers. In addition, the controller provides memory refresh and facilitates internal RDRAM register initialization.

The minimum media memory is 2 Mbytes of 9-bit (18 Mbits) RDRAM. Increments of 1 or 2 Mbytes can be added up to a maximum of 8 Mbytes. The interface utilizes the Rambus Signaling Logic (RSL) for transfers on each clock edge at a 500 Mbyte/s peak rate. The minimum amount of media memory required is function of the maximum display resolution and associated pixel depth as is shown in TABLE 5-3-5.

The interconnection of the RDRAM media memory on the Rambus channel is shown in FIGURE 5-3-7. Note that the external 250 MHz Rambus clock is the main processor system clock.

The MCCP analog current input determines drive capability of the memory interfaces as specified by RSL.

The Mpact media processor design supports from 2 to 8 MB of 9-bit wide Rambus DRAM memory.

RDRAM provides many system advantages :

- 500 MB/s burst the bandwidth on a single 9-bit wide channel
- 3 to 5 times the bandwidth of standard VRAMs
- 5 to 15 times the bandwidth of standard DRAMs
- Better scalability for greatest design flexibility
- Reduced board space requirements, only 9 in^2 instead of the 32 in for conventional memory systems
- Pin-for-pin compatibility across RDRAM generations ensures easy upgrades
- Reduced pin count of only 28 pins

TABLE 5-3-5. Media Memory Requirements

Display Resolution	Pixel Depth in Bits	MINIMUM RDRAM Size
1600 x 1200	8	4 MB
1360 x 1024	8	4 MB
1280 x 1024	18	4 MB
1280 x 1024	8	2 MB
1152 x 870	18	4 MB
1152 x 870	8	2 MB
1024 x 768	24	4 MB
1024 x 768	8 , 18	2 MB
800 x 600	8 , 18 , 24	2 MB
800 x 480	8 , 18 , 24	2 MB

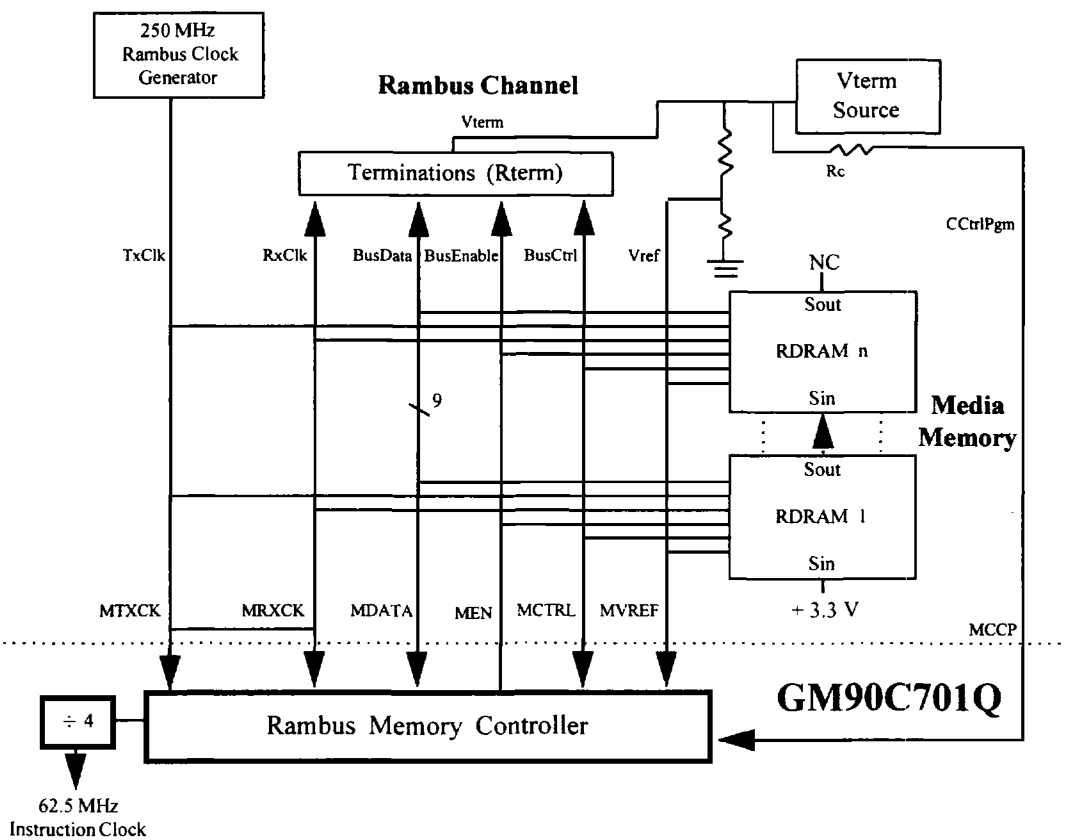
5-3-3-1. Functional Description

The major elements of the media memory system are shown in Figure 5-3-7. The 18-Mbit RDRAMs (2M x 9) are arrayed along the Rambus channel which physically and electrically extends from the memory controller within the Mpact media processor to the Rterm termination resistors connected to Vterm.

The Rambus clock generator is physically located at the termination end of the channel. When reading, transfers are made by the TxClk (transmit from memory) clock which propagates with the data from memory to the con-troller. When writing, transfers are made by RxClk (re-ceived into memory) which is a continuation of TxClk that propagates with data from the controller to memory.

A uniform threshold reference voltage Vref is distributed to all memory and the controller. The controller output drive levels on the Rambus channel are determined by the MCCP input which tracks changes in Vterm and is a function of the number of RDRAMs as determined by Rc.

FIGURE 5-3-7. RDRAM Media Memory on the Mpact Memory Interface



5-3-3-2. Media Memory Sizes

The minimum media memory for Mpact media processor operation is 2 Mbytes (2M x 9 bits) or one 18-Mbit RDRAM. This is adequate for a full set of multimedia fea-tures but a larger memory supports higher display resolu-tions and color pixel depths. Up to 8 Mbytes of media memory can be used for this higher performance. If the choice of the amount of memory can be made at the board assembly time, then the board should be laid out for the maximum number of RDRAMs expected and then populated with RDRAMs soldered in as desired. The Fig-ure 5-3-8 reference design is an example where the max-imum is 4 MB but RDRAM 2 can be left off at assembly time to create a 2 MB system.

If it is desired to make the amount of media memory up-gradable in the field, then the configuration in the refer-ence design in Figure 5-3-8 should be used. This so-called Y-channel splits the Rambus channel with one leg going to the required 2 MB RDRAM1 mounted on the board and the other leg going to the optional 2 to 6 MB added in on an RModule plugged into the RSocket. Each leg of the Y-channel is terminated separately.

Note than in addition to sharing Vterm and Vref, the RSocket also has a CCtlPgm signal and a BusClk source from the clock generator. The CCtlPgm signal adjusts the controller output drive for different amounts of RDRAM on the RModule and the BusClk provide another TxClk source at that termination end. In the Y-channel design Rterm is 47 Ohms, Vterm is 2.48 Volts and Vref is 2.09 Volts. Rc is now 50% of Rterm.

The initialization daisy chain with SIn and SOut signals still begins with RDRAM1 and continues on to the RModule.

5-3-3-3. Design Considerations

The system design engineer should be thoroughly famil-iar with the current Rambus reference manuals listed at the end of this appendix when designing the RDRAM me-dia memory for the Mpact media processor.

This appen-dix only highlights design considerations that are important because the Mpact media processor is the Rambus memory controller.

Figure 5-3-8 is a simplification of a 4 MB Mpact reference design available from Chromatic which illustrates a work-ing example circuit.

Note the generation, physical distribution, interconnec-tion and final termination to Vterm of the 250 MHz Ram-bus clock. Rterm is 41.2 Ohms. Vterm is 2.41 Volts and derived from the +5 Volt supply. All terminations should be bypassed physically close to the resistors as shown. Vref, which is 1.93 Volts and tracks changes in Vterm, can be derived from Vterm with a simple resistive divider and is distributed to all memory and the controller on the Rambus channel. Note also the connection of the media processor's analog power supply signals V GND A and V DD A to their respective printed circuit board voltage planes.

The current control program (CCtlPgm) signal in Rambus designs is an analog current that is sampled periodically to adjust the drive capability of the memory controller out-puts. The media processor's Rambus memory controller samples the MCCP signal for this function. For proper op-eration, MCCP should be tied to Vterm by a resistor with 40% of the resistance of Rterm.

Multiple RDRAMs are daisy chained through their SIn and SOut signals as shown for proper initialization after reset.

5-3-3-4. Circuit Board Design

Proper physical layout of the Rambus channel on a print-ed circuit board is critical. Designers must comply with the Rambus Signaling Logic (RSL) design constraints de-tailed in the Rambus Channel Design Guide, Rambus Inc. The Chromatic reference designs show by example how these constrains apply to a working Mpact media processor design.

FIGURE 5-3-8. Mpact Memory Interface with 4 MB of Board-mounted RDRAM Media Memory

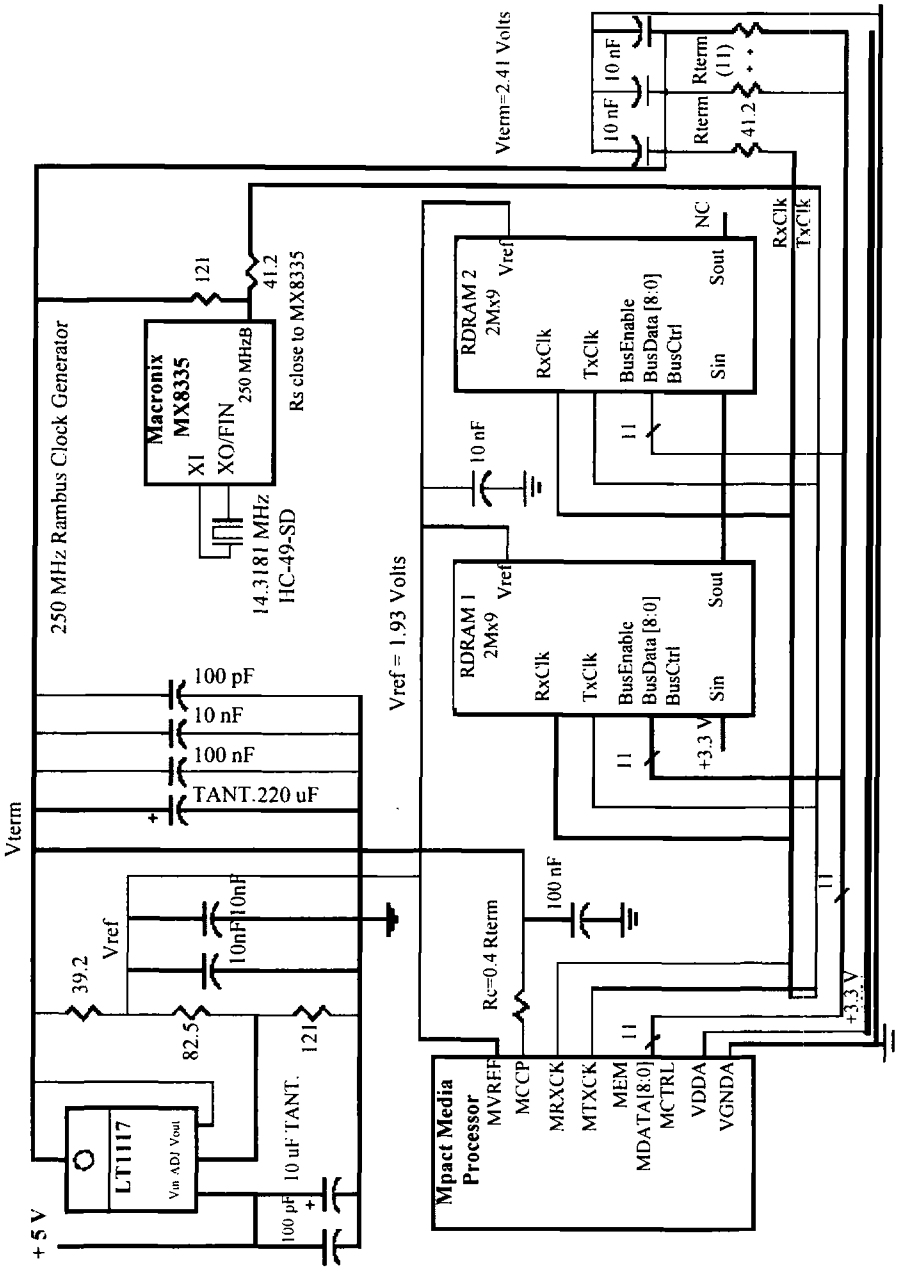
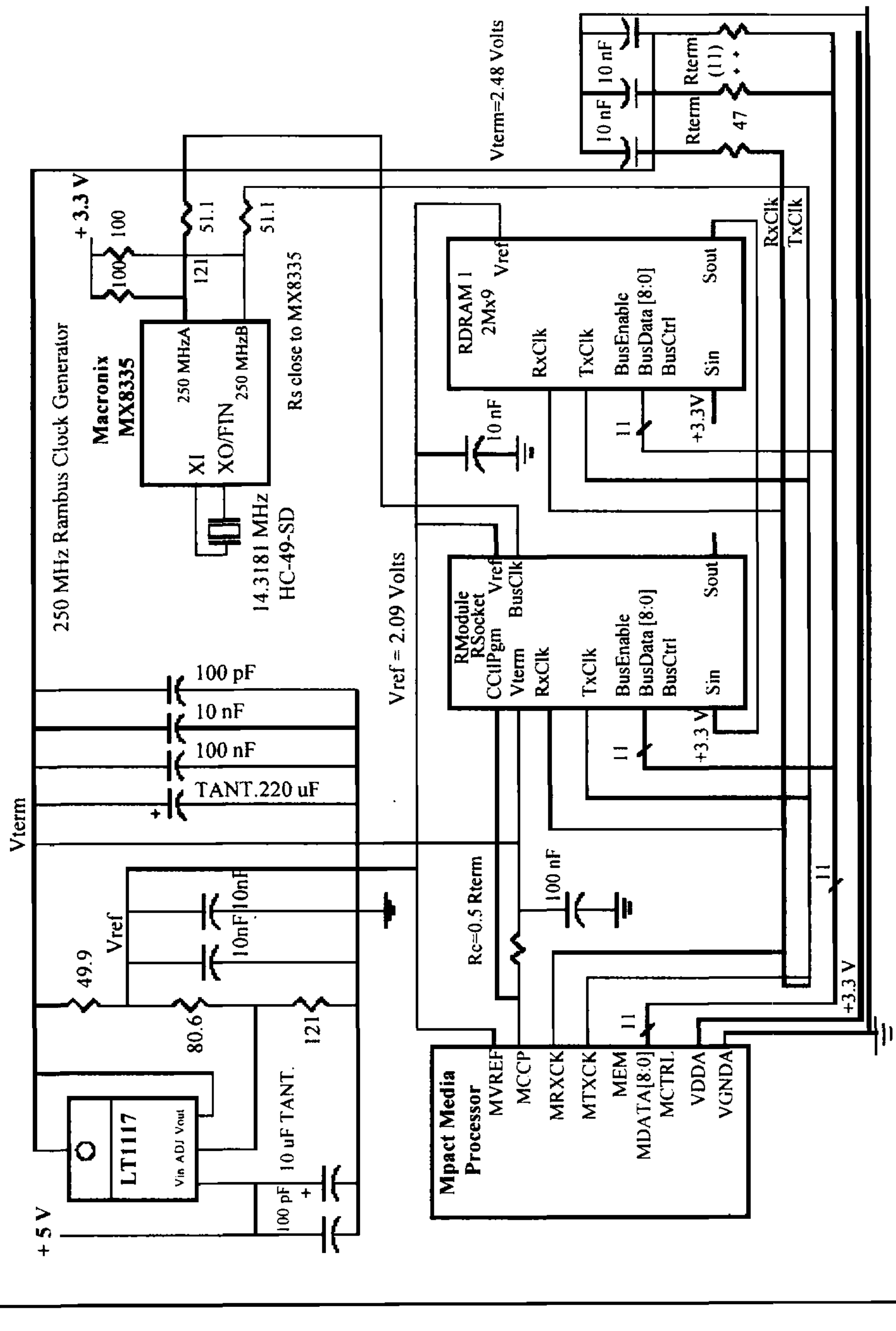


FIGURE 5-3-9. Mpact Memory Interface with 2 MB of Board-mounted RDRAM and Extension Socket



5-3-3-5. RDRAM Controller

Memory transmit and receive clocks TxClk and RxClk provide the fundamental timing and operating frequency for the Rambus Memory Controller within the Mpact me-dia processor. Memory input and output data timing is with respect to these clocks. The internal 62.5 MHz pro-cessor instruction clock is also derived from these clocks.

Data is moved on the Rambus channel on both clock edg-es to achieve 500 MB/s transfers as shown in Figure 5-3-10. Skewing between clock and data signals must be min-imized to achieve this high-speed data transfer. To this end TxClk, RxClk and BusData circuit paths must be arranged in parallel so that they have the nearly equal prop-agation times. The two clock inputs on the media processor, MTXCK and MRXCK, eliminate the effects of even the short physical distance between these two pins. The clock duty cycles are not critical as shown in Figure 5-3-11 with a maximum of a 45-55% duty ratio accepted. Two consecutive falling edges define one bus cycle. The clock signal level is referenced to Vref, with a logic-one being a low-level voltage and a logic-zero being a high-level voltage.

The propagation time on the Rambus channel typically results in a delay time t TR at the memory between the transmit and receive clocks as shown.

FIGURE 5-3-10. The Basic Rambus Transfer Cycle Timing

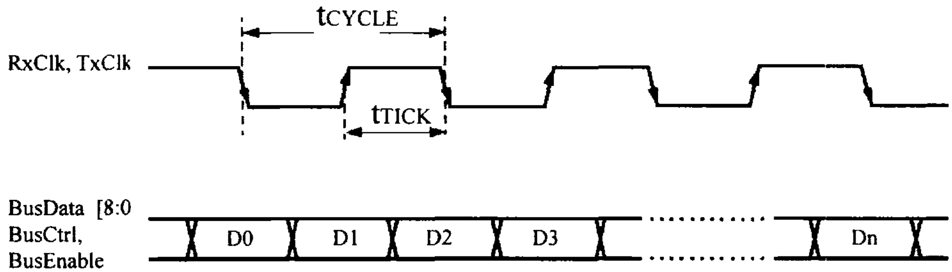
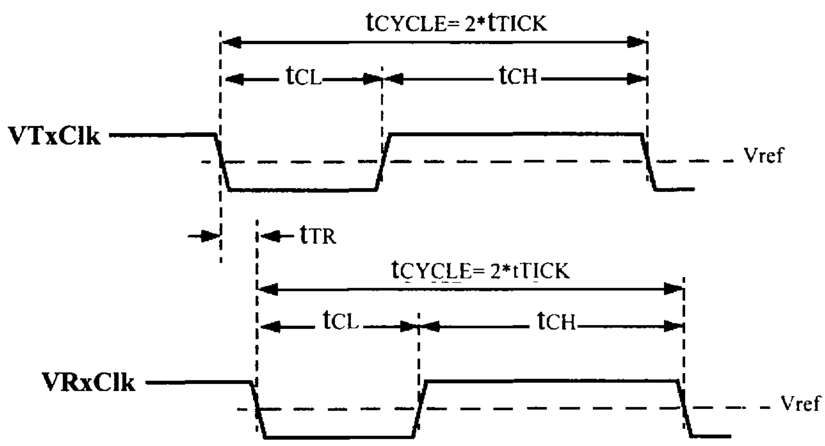


FIGURE 5-3-11. The Basic Rambus Transfer Cycle Timing



The Mpact media processor Rambus interface transfers data between RDRAM and the following interfaces ;

- Display and cursor interface
- Video bus interface
- Peripheral bus interface
- PCI interface

The Rambus interface refreshes RDRAM and provides a mechanism for initializing the RDRAM's internal registers.

The Mpact media processor Rambus interface controller performs address translation on all requests made to it. This process, called tiling, increases RDRAM cache hits for graphics and video applications, substantially improving overall system performance.

The frame buffer views provides speedy translation of graphics and other data from the 9-bit RDRAM format to a RAMDAC format.

A single 16-Mbit RDRAM provides 2MB of memory , standard system size. The Rambus transfers one byte every 2ns, or one 72-bit word every 16ns, giving rise to Mpact's 62.5 MHz core clock rate. Two RDRAMs are needed for MPEG-1 encoding or MPEG-2 decoding.

There is no virtual memory-management hardware, since all programs run in real memory out of the RDRAM. Even the SRAM is controlled completely by software with little hardware support.

TABLE 5-3-6. Memory address for Emulation

Address Range	Function	Feature Emulated	Size
A0000-AFFFF	VGA	VGA mode D,E,F 12,13	64 KB
B8000-BBFFF	VGA	VGA mode 0,1	16 KB
B8000-BFFFF	VGA	VGA mode 2,3,7	32 KB
C0000-C3FFF	VGA BIOS	VGA BIOS ROM	16 KB

5-3-4. Peripheral Input/Output Controller and Interface

The Peripheral I/O controller and its associated FIFOs provide the interface to lower bandwidth peripheral components of the multimedia system. This is done with eight generic unidirectional bit-serial data buses, a single generic bi-directional 8-bit parallel data bus and three special buses. The aggregate data rate can be as high as 5 MB/s. These generic buses become device and function specific ports with the loading of the 96-byte controller microcode RAM and the use of the various mediaware modules.

A total of fourteen different transaction ports may be operational at on time, with twelve of them using separate DMAs and 8-byte each FIFOs. FIGURE 5-3-12 shows the interface connections to ten example I/O devices that are supported by mediaware. Signals labeled and shown visibly passing through the block are connected in that block. These serve to illustrate typical interfaces to I/O peripherals.

The Peripheral Input/Output Interface divides naturally into three sections for parallel data, serial data and special transfers. Since the Mpact media processor's parallel channels are highly programmable, it supports not only a wide variety of current Codecs or other peripherals, but through software upgrades, should support future devices as well. For DMA operations, an external signal triggers a micro-program that transfers data to or from an external device. The most common transactions are kept resident in the microprogram control store memory to maximize I/O throughput and to minimize service latency. Unusual transactions, such as those for error handing, are stored in RDRAM and are loaded on demand into control store memory, optimizing the use of on-chip hardware resources.

The serial channels support a programmable protocol that tells the channel when to transfer data based on clock and synchronization signals supplied by an external device, such as an audio Codec. Channel C is dedicated to ROM. Its microprogram is hardwired to output a 24-bit address to the ROM, pause for the ROM access time, then read the data into a register. Channel D is a general-purpose, internally requested channel that writes control registers and reads status in external devices.

The Mpact Peripheral I/O Parallel Bus is 80 data, address and control signals derived from the 8-bit parallel portion of the Mpact media processor's Peripheral I/O interface. It provides one of the moderate bandwidth digital interfac-es to a variety of multimedia I/O devices. When the Mpact media processor is loaded with peripheral I/O interface controller microcode and appropriate mediaware mod-ules, the bus supports function specific ports and devices. The implementation discussed in this appendix supports the ports required for display, video, digital audio, tele-phone and the general port for game devices and the sys-tem ROMs. Because its timing and functions are programmable it can easily adapt to the data, address and sequence formats of new devices in the future.

This appendix explains the design and operation of the digital interface circuitry that generates the Peripheral I/O Parallel Bus from the Mpact's Peripheral I/O Interface. Designs using the Mpact System Integration ASIC (MSIA) and discrete components are covered.

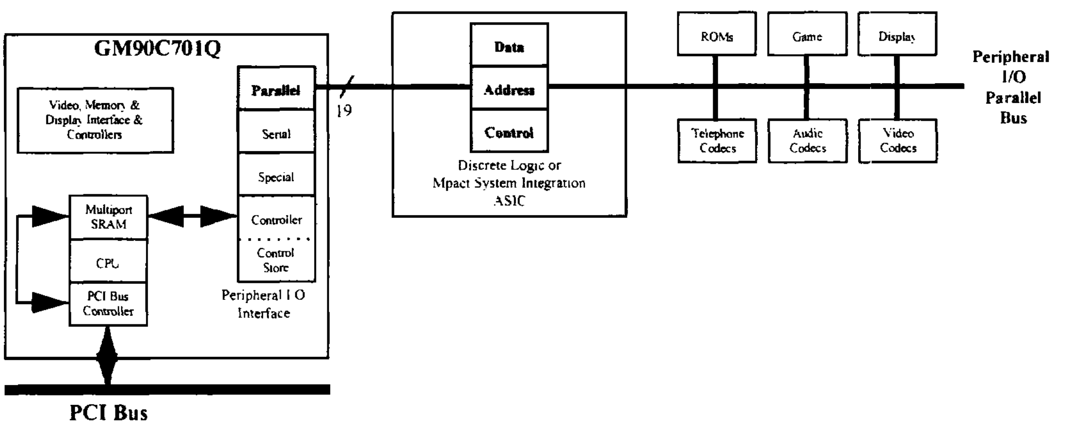
This appendix helps understanding Mpact reference de-signs including the one for the Mpact PCI Evaluation Board.

As shown in Figure 5-3-12, the Peripheral I/O Parallel Bus is an 80 signal expansion of the 19 signal parallel portion of the Peripheral I/O Parallel Interface. Using the multi-plexer and register functions in Figure 5-3-14, the 8-bit data signals of the interface become 24 bits of address, 24 in-put control signals and 16 output control signals in addi-tion to the 8-bit data input/output. Eight of the output control signals are designated as chip selects and eight for general purpose control. Twelve of the input control signals are for real-time operations as they produce an internal processor interrupt. The other twelve input control signals are DMA requests for high-speed data transfers. A joystick data input is provided and is read periodically for this General Port function. The Peripheral I/O Parallel Bus signals are summarized in Table 5-3-9.

The Peripheral I/O Parallel Bus generally serves two functions. It provides moderate rate data transfers for de-vices with a parallel interface (e.g., audio codec, tele-phone codec and MIDI UART.) It also provides control to configure devices connected to the Mpact Video, Display or serial portion of the Peripheral I/O Interfaces.

There is no general protocol or timing standard used for the bus, but rather it is determined by the mediaware for the spe-cific port and devices in use.

FIGURE 5-3-12. The Mpact media processor peripheral I/O parallel Bus



5-3-4-1. Design Considerations

The register and multiplexing logic functions shown in the left-hand side of Figure 5-3-14 can be implemented directly in discrete logic as shown in the figure or by using the Mpact System Integration ASIC (MSIA).

5-3-4-2. Discrete Logic

Using discrete logic has the possible benefit of using 3.3 Volt logic for lower power consumption than the 5.0 Volt MSIA or to meet other special requirements. Also the log-ic may be included in a custom ASIC which supports dif-ferent peripheral devices than the MSIA and includes other glue logic required by the particular system.

5-3-4-3. Mpact System Integration ASIC (MSIA)

The 144-pin Mpact System Integration ASIC provides a small footprint way to generate the Peripheral I/O Parallel Bus along with important peripheral device glue logic for the configuration used on the Mpact PCI Evaluation Board. It minimizes the devices needed for the game, S/PDIF digital audio and modem functions and for general system functions like resetting. Figure 5-3-13 shows on the left-hand side the signal inter-connection of the MSIA to the parallel portion of the Mpact Peripheral I/O Interface. The right-hand side shows the connection of the Peripheral I/O Parallel Bus from the MSIA to a typical (non-joystick) peripheral de-vice.

Table 5-3-7 summarizes all of the signals of the MSIA. Note that only a 23 bit address space is supported on the bus generated by the MSIA. The Joystick Data In is divid-ed into four bits of button data and four bits of timer data.

Table 5-3-8 is a complete signal description including the miscellaneous signals used for specific peripheral devic-es or general functions. Their use is described in the cor-responding Appendix.

FIGURE 5-3-13. Connection of the Mpact system integration ASIC (MSIA) to the media processor and a typical peripheral device on the peripheral I/O parallel Bus

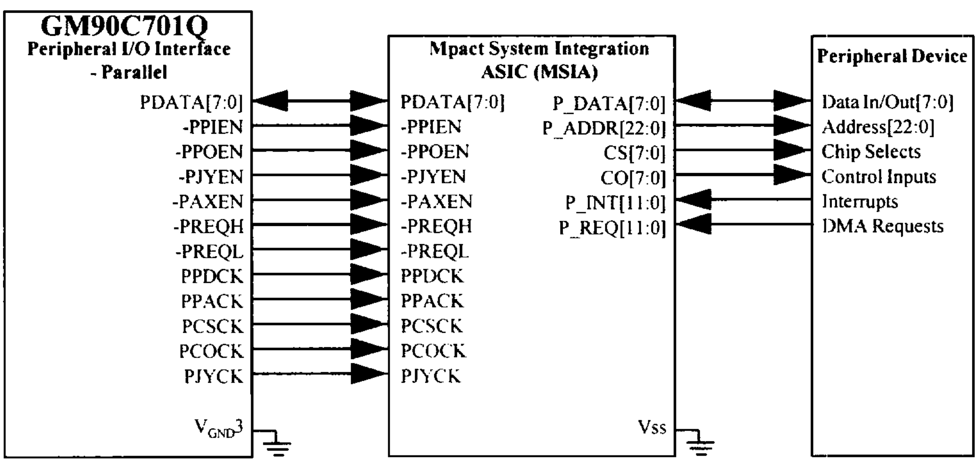


TABLE 5-3-7. Mpact system integration ASIC (MSIA) signal summary

Name	Number	Type	Description
Peripheral I/O Interface - Parallel	**19**		
PDATA[7:0]	8	I/O	Peripheral Parallel Data to/from media processor
-PPIEN, -PPOEN	2	I	Peripheral Parallel Data input and output enables from media processor
-PJYEN, -PAXEN	2	I	Peripheral Parallel Joystick and auxiliary control input enables from media processor
-PREQH. -PREQL	2	I	Peripheral Parallel Request input enables for high and low bytes from media processor
PPDCK, PPACK, PCSCK, PCOCK, PJYCK	5	I	Peripheral Parallel Data, Parallel Address, Chip Select, Control and Joystick register clocks from media processor
Peripheral I/O Parallel Bus	**79**		
P_DATA[7:0]	8	I/O	Peripheral I/O Parallel Bus Data to/from peripherals
P_ADDR[22:0]	23	O	Peripheral I/O Parallel Bus Address to peripherals
CS [7:0]	8	O	Chip select output to peripherals
CO[7:0]	8	O	Control outputs to peripherals
P_INT[11:0]	12	I	Interrupt inputs from peripherals
P_REQ[11:0]	12	I	DMA Request inputs from peripherals
BUTTON_IN[B2:A1]	4	I	Joystick Button data input
TIM_OUT[D:A]	4	I	Joystick Timer data input
Miscellaneous	**22**		
P_-RESET, VSP_-RESET, MRESET, -MRESET. -POR, PROM	6	I&O	Reset related
PB1, PB0	2	I	Control related
EDGE_INT, EDGE_INT_-CLR, CS8401_MCK, 16.9344_MHz, 24.576_MHz	5	I&O	S/PDIF related
3V25VIN[1:0]. 3V25V_OUT[1:0]	4	I&O	Modem related
MIDI_TXD, -MIDI_EN. SEL0/ UART_CK, SEL1/MIDI_RXD	4	I&O	MIDI related
NC	1	-	No Connection
Power	**24**		
VDD[10:1]	10	P	+5.0 Volt power supply
VDD[14:1]	14	P	Power supply ground
Total	**144**		

TABLE 5-3-8. Mpact system integration ASIC (MSIA) signal Description

Name	Number	Type	Description
PDATA[7:0]	58-55, 53-50	I/O	Peripheral Parallel Data to/from media processor
-PPOEN	24	I	Peripheral Parallel Data output enable from media processor
-PPIEN	25	I	Peripheral Parallel Data in enable from media processor
-PJYEN	33	I	Peripheral Joystick input enable from media processor
-PAXEN	44	I	Peripheral Auxiliary control input enable from media processor
-PREQH	42	I	Peripheral Request input enable. high byte from media processor
-PREQL	43	I	Peripheral Request input enable. low byte from media processor
PPDCK	26	I	Peripheral Parallel data output clock from media processor
PCOCK	29	I	Peripheral control output clock from media processor
PCSCK	30	I	Peripheral chip select clock from media processor
PPACK	31	I	Peripheral Parallel address clock from media processor
PJYCK	32	I	Peripheral Joystick register clock from media processor
P_DATA[7:0]	128-131, 133-136	I/O	Peripheral Joystick register clock from media processor
P_ADDR[22:0]	103-98,89,88,90,92,86, 96,97,94,93,85-78	O	Peripheral I/O Parallel Address to peripherals. Lower order 23 bits.
P_REQ[11:0]	106,34,68,104,76,11, 74,141,69,138,4,10	I	DMA Requests level inputs from peripherals
P_INT[11:0]	108,36,71,105,77,12, 75,142,49,137,6,9	I	Interrupt Requests level inputs from peripherals
CS[7:0]	119-126	O	Chip select outputs to peripherals
CO[7:0]	13,15-17,19-21,23	O	Control outputs to peripherals
BUTTONB[2:1]_IN	59,60	I	Paddleboard Button B Inputs
BUTTONA[2:1]_IN	61,62	I	Paddleboard Button A Inputs
TIM_OUT[D:A]	67-64	I	Joystick Timer data Outputs.
P_-RESET	40	I	PCI Bus reset
VSP_-RESET	41	O	Reset to media processor
POR	39	I	Power On Reset analog input
MRESET	7	O	Master Reset to peripherals
-MRESET	8	O	Master Reset to peripherals
PROM	48	I	System ID ROM, input used for reset logic in MSIA
PB1, PB0	27,28	I	Peripheral program output Bits 1 and 0 from media processor
CS8401_MCK	112	O	S/PDIF Master Clock output
EDGE_INT	116	I	S/PDIF Interrupt
EDGE_INT_-CLR	117	I	S/PDIF Interrupt Clear
16.9344_MHz	3	I	S/PDIF clock input
24.576_MHz	5	I	S/PDIF clock input
3V25V_IN[1:0]	46,47	I	Modem related interface voltage level conversion inputs
3V25V_OUT[1:0]	140,139	O	Modem related interface voltage level conversion inputs
MIDI_TXD	111	O	MIDI UART Transmit Data
-MIDI_EN	113	I	MIDI UART Enable
SEL0/UART_CK	114	I	MDI UART Clock Selected
SEL1/MIDI_RXD	115	I	MDI Receive Data Selected
NC	144	-	No connection
VSS[14:1]	143,127,110,107,95,87, 73,70,54,38,35,22,14,2	Power	Power supply ground
VDD[10:1]	136,118,109,91,72,63, 45,37,18,1	Power	+5 Volt power supply

5-3-4-4. Parallel Interface

The 8-bit bi-directional PDATA [7:0] bus transfers not only data in and out, but also has specific clocking and control signals to support 24-bit addressing, 8 chip-select outputs, 8 general control signal outputs, 12 interrupt requests and 12 DMA requests. Also, it provides the periodic clock timing for a joystick input. FIGURE 5-3-10 shows the clocking and output enables for the seven 8-bit registers and four input multiplexers. TABLE 5-3-10 summarizes the Peripheral I/O Parallel Bus signals that result.

This configuration can support most popular I/O peripherals with a parallel data interface today, but because its timing and function is programmable it can easily adapt to the data, address and sequence formats of future devices.

The Peripheral bus (PBus) has 14 virtual access channels for communicating with peripherals and controlled by external devices and are used for DMA. These channels are micro-programmable and are capable of a total bandwidth of 25 MB/s operation. Channels C and D are controlled by register accesses from the PCI or Mpact media processor.

In addition to being micro-programmable, eight of the DMA channels may be configured using either a parallel or a serial interface. The remaining four channels use only a parallel interface. The following table illustrates the configuration options for each programmable channel ;

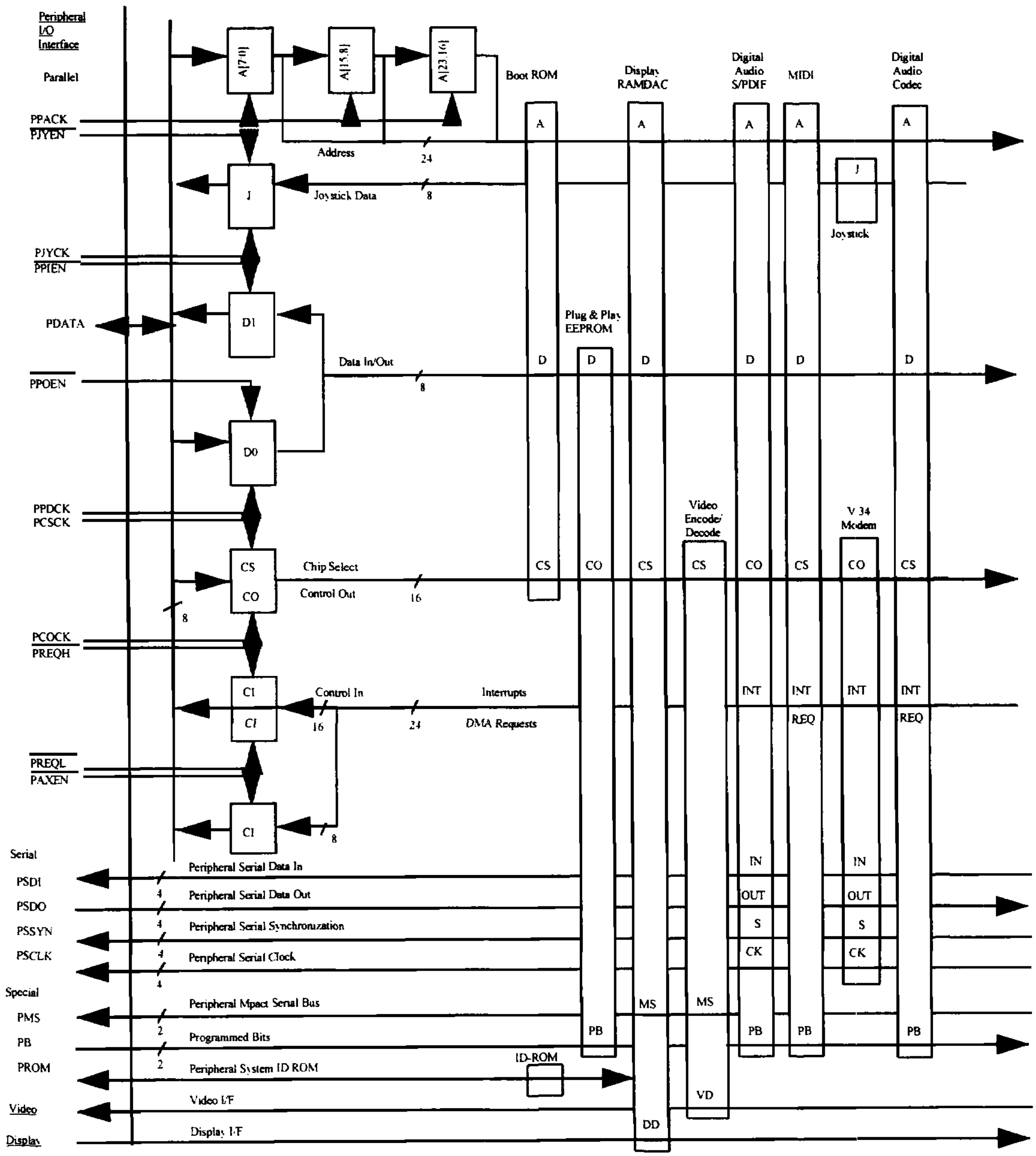
TABLE 5-3-9. Peripheral I/O Parallel Bus Signals

Signal	Number	Type
Data In/Out [7:0]	8	I/O
Address [23:0]	24	O
Chip Select [7:0]	8	O
Control Out [7:0]	8	O
Interrupt In [11:0]	12	I
DMA Request In [11:0]	12	I
Joystick Data In [7:0]	8	I

5-3-4-5. Serial Interface

The bit serial interface has four input channels 0-3 and four output channels 0-3. Like numbered input and output channels, PSD [3:0] and PSDO [3:0], share common data clocks PSCLK [3:0] and frame synchronization signals PSSYN [3:0]. These can support the wide variety of slave mode serial data formats used in audio and telephony cedecs as well as the serial control ports of many microprocessor peripherals.

FIGURE 5-3-14. External Logic functions needed to generate the Peripheral I/O parallel Bus on the Peripheral I/O interface and The Bus signals used in the vari- I/O ports.



5-3-4-6. Special Interface

• ***Mpact serial Bus***

Many microprocessor peripherals, including display and video products, use a two-wire bi-directional bus for multi-master control. The peripheral Mpact Serial Bus, PMSD and PMSC, is an enhanced version of the industry standard for support of these devices.

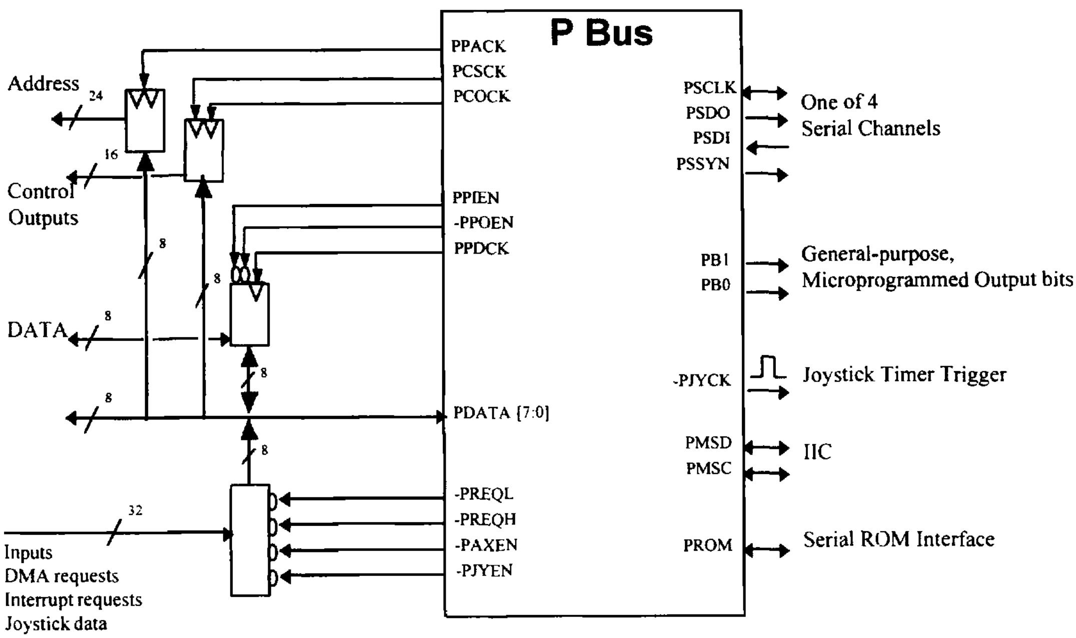
• ***Programmed Bits***

The PB [1:0] signals are two outputs without external registering that can be used for peripheral communication without regard to other transfers on the parallel or serial interfaces. They are set and cleared directly by the peripheral I/O controller's microcode.

• ***System Identification ROM***

Each Mpact media processor has a unique system indentification number read from a one-time-programmable ROM. The bidirectional PROM signal provides a single pin connection to a DS2430A or a similar device for this purpose.

FIGURE 5-3-15. PBus Interface



5-3-5. Display Controller and Interface

The display controller in combination with the 512-byte display FIFO provides continuous RGB display data to the display interface from buffers in the RDRAM media memory. The display controller generates all data, synchronization and clock signals to the display RAMDAC (digital-to-analog converter) or display encoder from a single video clock generator input DCLKI. Both 8-bit indexed-color and 24-bit true-color RAMDACs can be supported as well as NTSC and PAL RGB encoders. Possible display resolutions and the pixel clock frequency DCLKO are shown in FIGURE 5-3-12. The maximum refresh rate may not be possible with the maximum pixel depth.

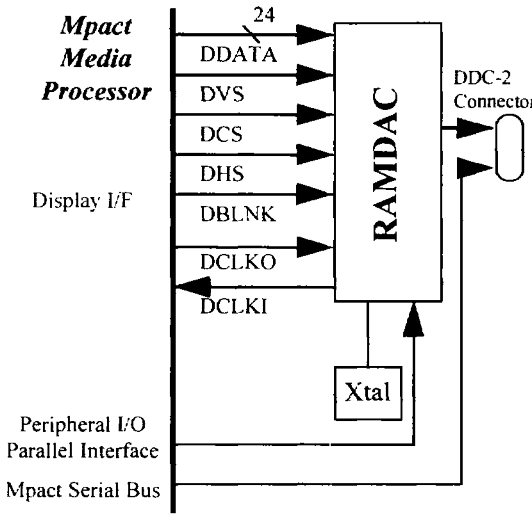
Control of the display RAMDAC or encoder is through the use of the Mpact Serial bus and /or the peripheral bus in the Peripheral I/O interface.

Display data is stored in the media memory in one-, two-, or three-byte formats to support 8, 15, 16, 18 and 24 bits per pixel. The special 18 bits per pixel data Chro-color format provides a 32-bit buffer view yet takes only two bytes in the media memory. The conversion from media memory format to RAMDAC format takes place in the display controller. Supported devices in the Mpact mediaware modules display port are the ATT 1178AB, Bt473 and ADV473KP.

TABLE 5-3-10. Display Resolutions

Display Resolution	Pixel Clock Frequency (MHz)	Maximum Refresh Rate (Hz)	Maximum Pixel Depth
1600 x 1200	220	75	8
1360 x 1024	135	75	8
1280 x 1024	125	75	18
1152 x 870	100	85	18
1024 x 768	80	85	18
800 x 600	50	85	24
640 x 480	32	85	24
NTSC:720x480	12.27	30	24
PAL;720x576	14.75	25	24

FIGURE 5-3-16. RAMDAC Interface



The display controller coordinates the transfer of information between RDRAM and the display RAMDAC. The display controller translates 9-bit data from RDRAM into 24-bit data for the RAMDAC. The display is refreshed through the DMA from RDRAM. Figure 4 shows a functional block diagram of the Mpact media processor's components for display control.

The Mpact media processor presents the following frame buffer views to the PCI host interface ;

- 8 bpp
- 18 bpp
  - 16 bpp (5:5:5)
  - 16 bpp (5:6:5)
  - presents a 24 bpp software programming model
- 24 bpp

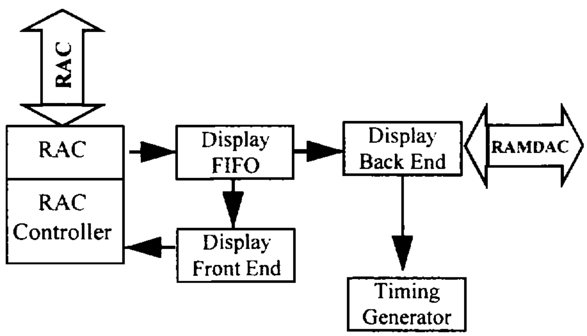
The Mpact media processor provides the PCI views by using the three native frame buffer views in the following RDRAM formats ;

- 8 bpp (one Rambus byte)
- 18 bpp (two Rambus bytes for 15 bpp, 16 bpp and 32 bpp views)
- 24 bpp (three Rambus bytes)

The Mpact media processor's special *chro-color* format, the 32 bpp mode, packs 24 bpp into 18 bits and provides color depth performance between the 16 bpp hi-color mode and the 24-bit true-color mode. Using 18 bpp provides color quality near 24 bpp at substantially less memory cost than 24 bpp.

The display controller is comprised of the following components, as shown in the following block diagram.

FIGURE 5-3-17. Display Block Diagram



The Mpact media processor supports full indexed color for 8 bpp RAMDACs. In addition to industry-standard 8-bit RAMDACs, the Mpact media engine's 135 MHz display interface supports the following true-color RAMDACs ;

- ATT21C499
- Bt473
- ADV473KP

- **Display FIFO** moves data from the RDRAM frame buffers into the display back end.
- **Display front end** specifies to the RAC controller the location of the frame buffer and the cursor image and provides information about the size of the scan-line
- **Display back end** presents RGB information to the RAMDAC and provides zoom control.
- **Timing Generator** provides sync information for the scan-line and pixels.

Data flows left to right from RDRAM to the display FIFO to the display back end and out on the RAMDAC. Data requests and control signals flow from right to left.

The display clock and timing generator generate clocks that clock pixel data out of the chip. The data moves from the display FIFO to the display back end, which requests data from RDRAM. The Mpact media processor supports the following display resolutions and modes in Table 5-3-11. Resolutions, Memory Requirements and Refresh Rates

FIGURE 5-3-18. Display Interface Block Diagram

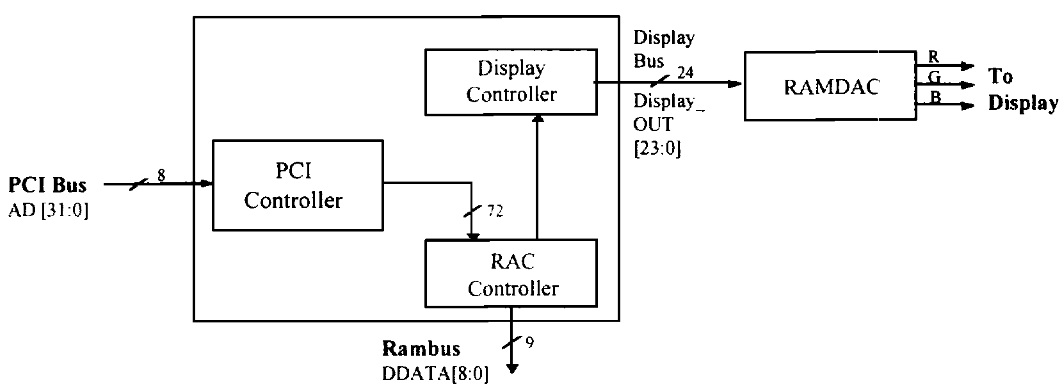


Table 5-3-11. Resolutions, Memory Requirements and Refresh Rates

Max Refresh	Resolution	Dot Clock Frequency (Approx.)	RDRAM required for pixel depths		
			8 bpp	18 bpp	24 bpp
75 Hz	1600 x 1200	220 MHz	4 MB	n/a	n/a
75 Hz	1280 x 1024	135 MHz	2 MB	4 MB	n/a
75 Hz	1024 x 768	79 MHz	2 MB	2 MB	4 MB
75 Hz	800 x 600	50 MHz	2 MB	2 MB	2 MB
75 Hz	640 x 480	32 MHz	2 MB	2 MB	2 MB
NTSC		12.27 MHz	2 MB	2 MB	2 MB
PAL		14.75 MHz	2 MB	2 MB	2 MB

TABLE 5-3-12. PCI Frame Buffer Views to RDRAM

Description	Indexed	R	G	B
8 bpp frame buffer	P_AD [7:0]			
15 bpp (5:5:5) hi-color		AD [14:10] rrrrr*	AD [9:5] gggggg*	AD [4:0] bbbbbb*
16 bpp (5:6:5) hi-color		AD [15:11] rrrrr*	AD [10:5] gggggg	AD [4:0] bbbbbb*
32 bpp chro-color		AD [23:18] rrrrr	AD [15:10] gggggg	AD [7:2] bbbbbb
24 bpp true-color		AD [23:16] rrrrrrrr	AD [15:8] gggggggg	AD [7:0] bbbbbbbb

*. The most significant bit is copied to the least significant bit to preserve all black or all white fields.

TABLE 5-3-13. RDRAM to RAMDAC Pixel Formats

Description	R [7:0]	R [7:0]		B [7:0]
8 bpp indexed BUS_DATA [7:0]				
18 bpp (15 bpp, 16 bpp, and 32 bpp PCI views)	DDATA [8:3] rrrrr rr*	DDATA [2:0] ggg	DDATA [8:6] ggg gg*	DDATA [5:0] bbbbbb bb*
24 bpp	DDATA [7:0] rrrrrrrr	DDATA [7:0] gggggggg		DDATA [7:0] bbbbbbbb

*. The most significant bit is copied to the least significant bit to preserve all black or all white fields.

5-3-6. Video Controller and Interface

The video controller, in combination with the 32-byte video FIFO, inputs or outputs YUV video data on the 16-bit video interface. This programmable interface is bidirectional but transfers are half-duplex. The three input synchronization signals, two bidirectional reference clock signals and an external video clock input can support a wide variety of 16-bit input video sources and output devices in either 8- or 16-bit formats. Industry standard NTSC or PAL encoders and decoders can be used at full scan rates for analog composite or S-video signals. Digital interfaces can be used for Zoom Video or CCIR 601 YUV 4:2:2 digital cameras or displays. Formats can be interlaced or progressive scan. The video controller is capable of horizontal decimation on input or output.

Among the supported devices in the Mpact mediaware modules video port are the SAA7187 and AD7176 encoders and the SAA7110 and KS0122 decoders. Control of the interlaced device is with the Peripheral Mpact Serial bus (the PMSD and PMSC signals) with possible device selection from the Peripheral I/O parallel interface.

The video bus (VBus) is a highly programmable interface that offers a great deal of flexibility in sending and receiving 16-bit YUV video data. It provides support for pixel scaling, color space conversion, and dithering.

The video bus and peripheral bus share an interface with RDRAM in which the video bus has priority over the peripheral bus.

Unlikely the peripheral bus that transfers only 1 dword at a time, the video bus transfers 8 dword FIFO. Video bus logic uses its sync signals to determine when the FIFO has data to read or write.

The video bus is bidirectional but half-duplex. It provides 1 horizontal sync **(v_sync)** and 1 vertical sync **(v_vsync)**. Video bus logic uses sync signals to determine when to read or with on-chip video FIFO. FIGURE 5-3-15 provides the signal waveforms.

The video bus hardware provides decimation functions for pixel data. When defining the size for RDRAM access from the video bus, the most used tile sizes and number od lines are as follows ;

- 64-byte tiles with 32 lines
- 128-byte tiles with 32 lines

The video bus supposes the following signals (TABLE 5-3-14)

The VCLK runs at 2 times the pixel rate. VCREF controls the clock on which data and control signals transfer. The VHREF signal runs continuously, even on lines with no pixels.

Errors are detected by testing the VODD, VHREF and VCREF signals. The video logic computes a pixel qualifier by adding the number of active lines, the number of active pixels and the valid clock cycles. This qualifier tests for valid pixels. The video logic supports two ways to indicate a field. The VODD signal indicates the current field.

In decimation of YUV, The video bus supports YUV video, including various compression algorithm. Normally, YUV 4:2:2 data is encoded as follows where Y defines luminance and UV define color.

To select the decimation mode, set bits [1:0] of the control register using the following values ;

00 No decimation. Pass through all data

01 Pass through the following values

$Y_0U_0V_0Y_2$

10 Drop every other byte, keeping all luminance values and discarding all color information

TABLE 5-3-14. Video signal

Signal	Direction	Description
VCLK	I	2 times the pixel rate
VDATA	I/O	Pixel rate
VVS	I	Vertical scan
VHS	I	Horizontal scan
VODD	I	Field indicator
VHREF	I/O	Horizontal or composite blank
VCREF	I	Clock per pixel qualifier

FIGURE 5-3-19. Video Encoder/Decoder Interface

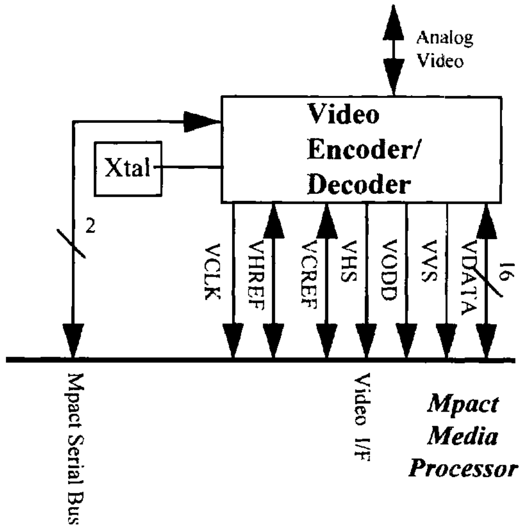


FIGURE 5-3-20. VBus Flow

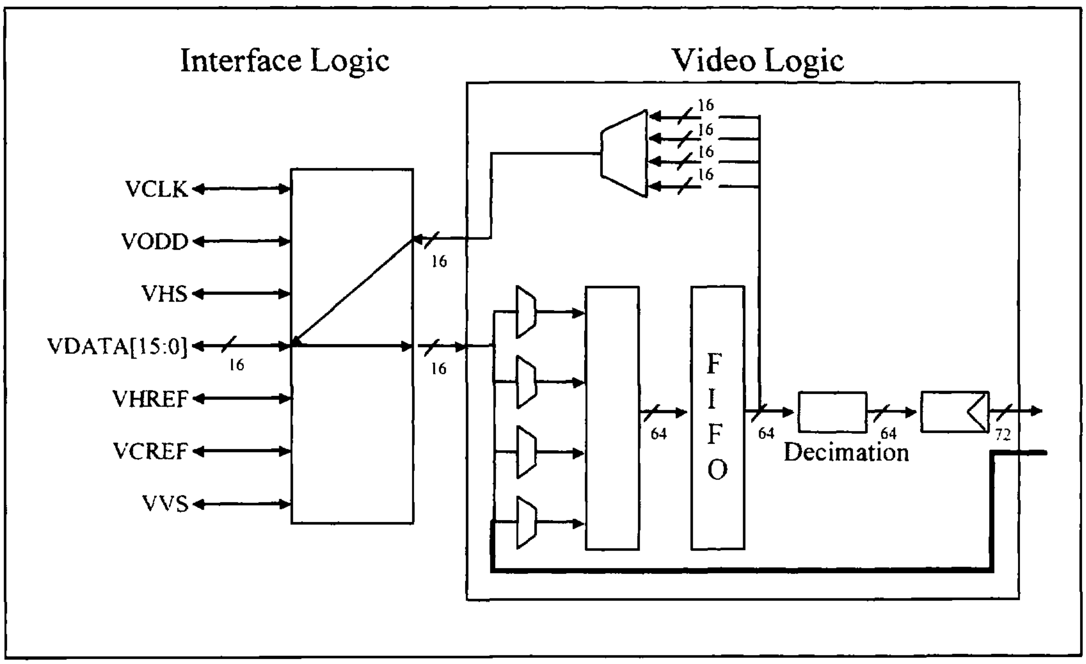
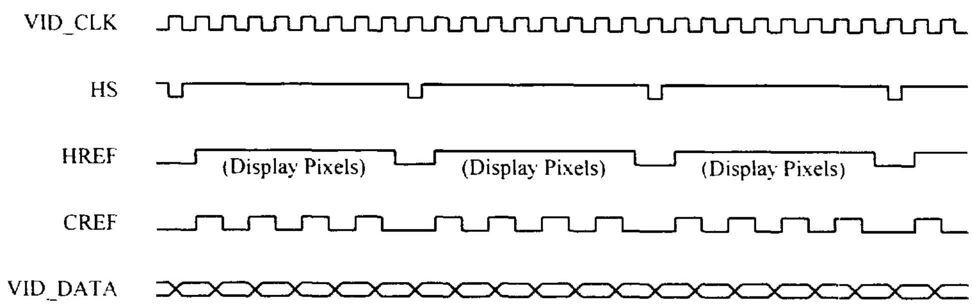


FIGURE 5-3-21. Video Signal Waveforms



5-3-7. Test Interface

The Mpact media processor can be tested using the four signals in the test interface.

When the test mode is selected by asserting TMS, then serial test data is clocked into TDI with the TCLK clock and out of PSDO0 which becomes TDO.

5-4. Mpact Mediaware Modules

Mpact mediaware by Chromatic Research is the software that enables access to the high-performance Mpact media processor on an x86 system. Through support for the latest DirectX APIs, in addition to alternative and earlier component APIs and legacy hardware views, the mediaware provides Mpact's power to DOS and Windows applications running on Windows95. The system software component parts are shown schematically in a highly simplified form in Figure 5-4-1.

A mediaware module can be thought of as a narrow vertical slice extending from the top to the bottom of FIGURE 5-4-1. Each mediaware module adds a multimedia function generally defined by its primary task. These functions are summarized in TABLE 5-4-1 with their primary attributes for eight functional groups. Of equal importance are the supported APIs at the bottom that are supported by an I/O port. TABLE 5-4-2 summarizes the supported APIs and TABLE 5-4-3 in the Input/Output Interface section summarizes the supported devices.

TABLE 5-4-3 shows by major API the functions that are enabled.

Applications, when running, invoke various functions through their API or hardware view.

These become single or multiple individual tasks related to the I/O port that is involved ; Video tasks use the Video port, 2D and 3D graphics use the display port, digital audio tasks use the audio port, Fax/Modem, telephony and videoconferencing use the telephone port and the joystick, MIDI and ancillary functions use the general port. These five classes of port are an important logical logical distinction. A port may use more than one electrical interface and is I/O device specific for the system.

Creating a low cost, high power multimedia PC is as easy as loading software when you combine the Mpact media processor-enabled PC with the mediaware configuration modules. To add additional features or new levels of technology to a multimedia PC, simply upgrade the appropriate mediaware module.

Each mediaware module includes a microprogram for the Mpact media processor, x86 drivers for the PC operating system such as Windows95 (or other operating systems where applicable), and the appropriate control panel and setup applications. The features of the Mpact mediaware modules are described in the following sections.

FIGURE 5-4-1. Distribution Of Operating Between The Mpact Media Processor And a Windows95` PC Host.

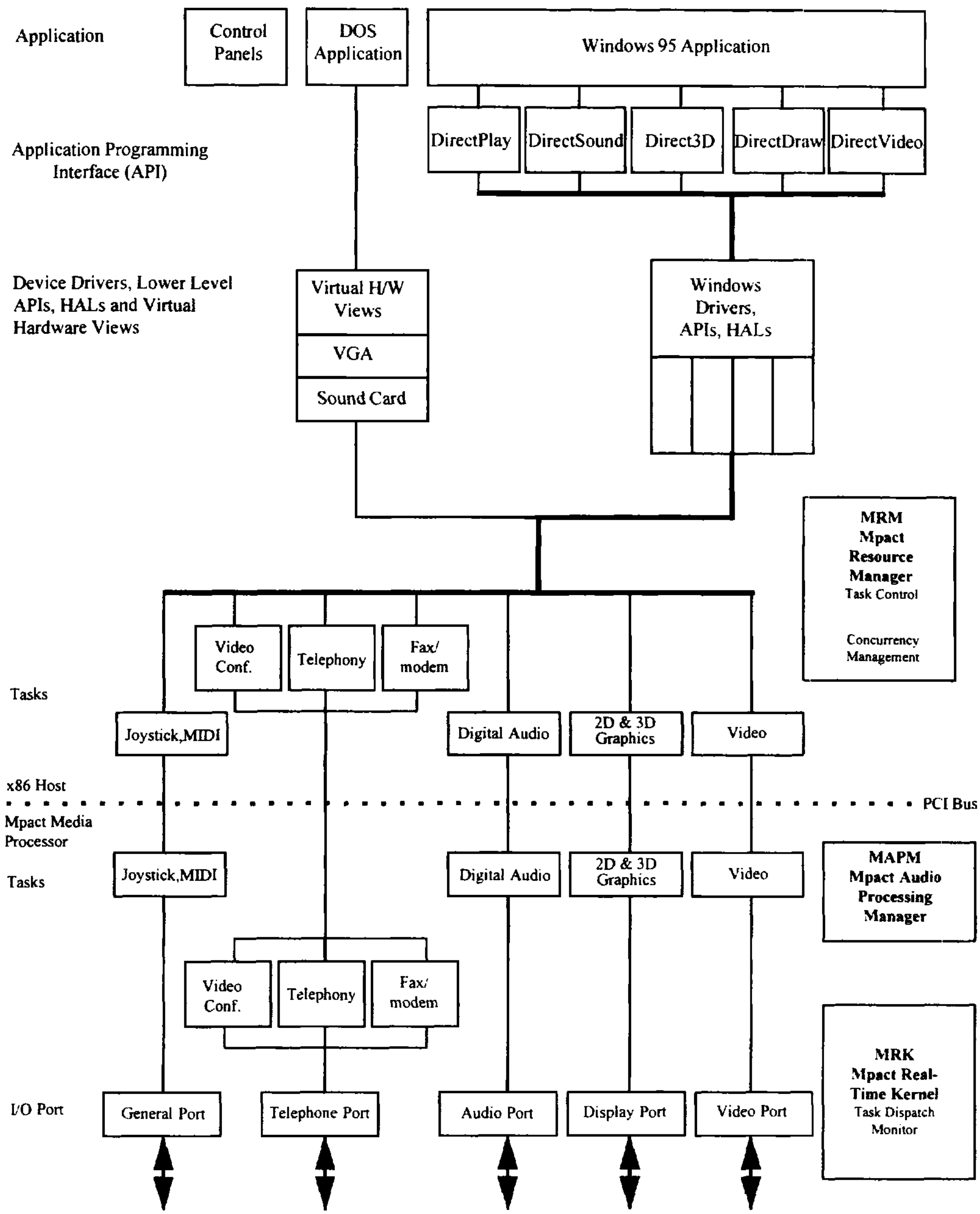


TABLE 5-4-1. Mpact Mediaware API Summary by function

FUNCTION	APIs
Video	
MPEG Decode ;	DirectVideo, MCI, ActiveMovie
MPEG Encode ;	ActiveMovie
Graphics - 2D	
Graphics Card ;	VGA, SVGA Compatible
GUI Acceleration ;	DirectDraw, GDI
Graphics - 3D	
3D Acceleration ;	Direct3D, OpenGL, Reality Lab
Digital Audio	
Sound Card ;	Industry Standard with FM
Output ;	DirectSound, MCI
Music ;	MCI, MIDI our/in, WAVEout/in
Effects ;	DirectSound 3D Audio
Fax/Modem	
Fax/Data modem	TAPI, TSPI, VCOMM, DirectPlay
Telephony	
Speakerphone, DSVD, Voicemail	TAPI, TSPI, VCOMM, DirectPlay
Videoconferencing	
	ActiveMovie, Independent Software Vendor's (ISV's)
General	
Joystick / MIDI	Industry Standard Sound Card

TABLE 5-4-2. Mpact Mediaware API support Summary

API	FUNCTIONS
DOS	
VGA Compatible	All
SVGA Compatible	All VESA Extention 2.0
Sound Card	All
WINDOWS95	
DirectVideo	
ActiveMovie	MPEG encode and decode, videoconferencing
DirectDraw	
Direct3D	
DirectSound	
DirectPlay	

TABLE 5-4-3. Mpact Mediaware Functions summary

FUNCTION	APIs
Video	
Encode & Decode ;	MPEG-1 Decoder, SIF 352 x 240, 30 f/s
	MPEG-2 Decoder, Main Level, Main Profile, NTSC 720 X 480, 30 f/s or PAL 720 X 576 25 f/s
	MPEG-1 Real-Time encode, SIF I frame 30 f/s, 10 Mb/s
	MPEG-1 Non-Real-Time encode, IBP frames
Graphics - 2D	
Graphics Card ;	VGA, All mode, 640 x 480 x 4 b/p @ 85 Hz
	SVGA, 1280 x 1024 x 18 b/p @ 75 Hz or 1024 x 768 x 24 b/p @ 85 Hz
GUI Acceleration ;	Full 256 Ternary ROPs, BitBLT, Font Acceleration, Line draw, Polygon engine, YUV color conversion, H/W cursor
Graphics - 3D	
3D Acceleration ;	Full rendering with lighting, shading, texturing, anti-aliasing support for rectangle fills, 3D spans and geometric primitives such as lines, triangles and quadrilaterals.
Digital Audio	
Sound Card ;	Industry Standard with FM synthesis
Encode & Decode ;	MPEG-1, Layer 1 & 2
	MPEG-2 AC-3 decode
	Dolby AC-3, 5.1 channel decode
	Dolby Prologic, 4 channel and stereo decode
	IMA ADPCM for Windows
Music ;	FM Synthesis
	Wavetable Synthesis(32 voices,32 multitrimbality parts), Synclavier® sample library
	Waveguide Synthesis
	General MIDI, 128 Instruments +>50 percussion, 64 voices
Effects ;	Surround and 3D sound (SRS),3D Positional Audio Effects(DirectSound), reverb, chorus, noise cancellation
Fax/Modem	
Data Rates ;	Up to V.34bis @ 33.6 Kb/s
Fax Rates ;	Up to V.17 @ 14.4 Kb/s
Data Protocols ;	V.42, V.42bis, MNP 2-4 error correction, compression
	AT Command set

FUNCTION	APIs
Fax Protocols ;	Class 1 (TIA-578), 2, 2.0 (TIA-592)
Telephony	
	Full-duplex speakerphone, Caller ID and answering machine using the IS-101A (AT+V Command set)
	IMA ADPCM encoding and decoding
	Digital Simultaneous Voice and Data (DSVD)
Videoconferencing	
	H.320 over ISDN
	H.324 over POTS
General	
Joystick	Industry standard connector including MIDI
MIDI ;	Industry standard GM16C550 UART I/O

5-4-1. Video Compression and Decompression

The mediaware video modules support international standards for decompression, including MPEG-1 and MPEG-2 video, audio and system decoding through the DirectVideo, MCI and ActiveMovie APIs. The media processor's patented hardware motion estimation function enables high quality real-time MPEG-1 video, audio and system encoding as well as videoconferencing.

For high quality video playback display, the processor can concurrently perform image processing algorithms such as picture resizing, noise reduction, scanline convolution, line-doubling, edge enhancement and motion-adaptive filtering.

Special features include ;

- MPEG-1 decode: SIF, 30 frames/s
- MPEG-2 decode: main profile, main level, 30 frames/s
- Real-time MPEG-1 encode: SIF, IBP frames, 30 frames/s

5-4-2. 2D Graphics-VGA and GUI Acceleration

The mediaware graphics module provides full VGA compatibility for legacy applications and full SVGA as defined in VESA BIOS extension 2.0.

Internal buffers support 8-,15-,16-,24- and 32-bits per pixel views. The special 18-bit Chro-color format provides color depth performance between the 16-bit and 24-bit true-color with greater memory efficiency.

- 640 x 480 for 256 colors
- 800 x 600 for 16 colors

GUI acceleration is optimized for Windows95 performance with a hardware cursor through the GDI and DirectDraw APIs. Acceleration is provided for solid and pattern fill, font and polygon generation, line draw, scaling and clipping, and color space conversion.

- BitBLT, Stretch BLTs, transparent BLTs
- Font acceleration, line draw, polygon engine
- YUV color space conversion
- 256 ternary (3-operand) ROPs
- Hardware cursor, Windows compatible

5-4-3. 3D Graphics

The mediaware 3D module is optimized to fully accelerate 3D rendering for game play through the Direct3D API.

- Rectangle fills, 3D spans and 3D geometric primitives such as lines, triangles and quadrilaterals
- Z-buffering and double buffered rendering
- Texture heaps, allocating and mipmapped textures, texture memory status, and textured primitives

5-4-4. Digital Audio

The mediaware digital audio modules can utilize full 36-bit processing at 48 KHz, even for compute-intensive functions like Dolby AC-3 and Waveguide physical modeling music synthesis. Automatic resampling is used so that all processing is at a uniform 48-KHz rate on up to 8 simultaneous stereo record/playback channels..

The mediaware audio modules perform the following audio signal processing, music synthesis, compression and decompression, and mixing functions :

- Industry-standard sound card compatible, with FM synthesis
- MIDI
- Wavetable audio synthesis
- Waveguide physical modeling audio synthesis
- Audio effects such as 3D sound
- ADPCM for Windows
- MPEG audio (Layers 1 and 2) compression and decompression
- Dolby AC-3 audio

APIs supported include WAVE in/out, MIDI in/out and Windows95 DirectSound.

5-4-5. FAX/Modem

The mediaware FAX/Modem modules support the latest current data and fax modem standards. For data modulation to 33,600 bps there is V.34bis, V.32bis, V.22bis, V.21, Bell 212A and Bell 103. For Fax modulation to 14,400 bps there is V.17, V.29, V.27ter, and V.21.

5-4-6. Telephony

The mediaware telephony modules combine the AT+V command set with various functions like echo-canceling, DTMF, ADPCM coding and DSVD processing to permit a full range of telephony operations like speakerphone, voicemail, answering machine or voice response.

The following telecommunications standards and interfaces :

- Windows95 TSPI
- Windows95 DirectPlay
- True Speech®
- Simultaneous voice and data
- Speakerphone with adaptive echo cancellation
- Voice mail and answering machine capabilities through support for AT+V

5-4-7. Videoconferencing

The mediaware videoconferencing modules support international standards over ISDN and standard telephone lines to interface with various ISV's videophone applications.

The following international videoconferencing standards ;

- H.320 for videoconferencing over ISDN connections
- H.324 for videoconferencing over POTS connections
- H.323 for videoconferencing over LAN connections

5-4-8. General

For games and entertainment, the industry standard sound board interfaces to a joystick with buttons and MIDI, the Musical Instrument Digital Interface, are supported in mediaware modules.

LG Semicon offers the Media Processor and Mediaware Software modules.

~ Media Processor processing a high bandwidth RAMBUS Memory modules.

~ Mediaware software modules to support all seven multimedia functions.

LG Semicon's part offers system manufacturers 5 features that makes it the best choice for a mother board solution ;

1. Modem and Telephony
2. Sound Blaster
3. Graphics Acceleration
4. MPEG support
5. 3-D Acceleration

5-5. Mpact Mediaware Environment

The hardware technology is the enabler, but the software must be comprehensive and scanless and can make or break the solution.

Mpact media processor's mediaware architecture is clean and lends itself nicely to upgrades as standards evolve. The soft approach sets Mpact apart from fixed-function solutions. Every new PC standard, such as Wave-table or Sound Blaster audio, needs to be supported by Mpact mediaware. The good news is that standard APIs are taking hold in the PC industry.

It can be decomposed into three levels ; the application, the driver, and the virtual devices. Additionally, there is a resource manager (not to be confused with Microsoft's RMI) running in the x86 processor and the Mpact real time kernel (MRK) running in the Mpact chip itself.

The device drivers (on the x86 side) are the compatibility software, or front end, to the entire Mpact media processor solution. The hardware technology is the enabler, but the software must be comprehensive and scanless and can make or break the solution.

Mpact media processor's mediaware architecture is clean and lends itself nicely to upgrades as standards evolve. The soft approach sets Mpact apart from fixed-function solutions. Every new PC standard, such as Wave-table or Sound Blaster audio, needs to be supported by Mpact mediaware. The good news is that standard APIs are taking hold in the PC industry.

It can be decomposed into three levels ; the application, the driver, and the virtual devices. Additionally, there is a resource manager (not to be confused with Microsoft's RMI) running in the x86 processor and the Mpact real time kernel (MRK) running in the Mpact chip itself.

The device drivers (on the x86 side) are the compatibility software, or front end, to the entire Mpact media processor solution.

These drivers must strictly adhere to the API, communicating to the virtual devices through MRK and, periodically, to the resource manager. The resource manager manages the RDRAM memory and other resources, maintains priorities, and sets up block and direct-communication transfers. This allocation changes as tasks are created and completed.

The resource manager talks to MRK, a multitasking kernel that juggles interrupts and requests from both the drivers and the hardware nodes operating the physical devices.

This kernel allocates the Mpact internal SRAM and performs task switching and task synchronization. MRK makes all devices appear independent to the drives and maintains real-time response by giving priority to the nearest deadline event. It is also quite clever in its handling of the instruction side of the SRAM cache, overlaying device tasks dynamically.

Finally, the virtual-device tasks that control the actual hardware are quite simple in most cases. The one exception is the audio section, which is complex enough to merit another mini-kernel that handles several processes at once. The software architecture allows to enhance the capabilities of the device over time, matching market developments and providing incremental performance enhancements.

This section has its own queuing, priority, and task-switching capability. Audio deserves this special attention due to the sensitivity of human hearing, which readily detects dropped bits that create clicks or discontinuities in the sound stream.

The software works together to balance the road between the host CPU and the Mpact media engine. Normally, as much processing as possible is shifted to Mpact, freeing the host CPU. If an extensive combination of applications -- for example, a high-resolution graphics stream, a 28.8 Kbps modem, and a demanding audio task-- are launched at once, the Mpact media processor could become overwhelmed. In this case, the resource manager shifts complex graphics operations - such as text acceleration, font caching, and solid fills - to the GDI driver on the host CPU, maintaining the performance of the most critical operations.

5-6. High Performance , Flexibility's

Mpact media processor consumes only 25-50 % of the host x86 processor with all devices running simultaneously. For instance, an 800 x 600 x 18-bit display running MPEG-1 audio and video decode and a simultaneous 14.4 Kbps modem uses 47 % of a 100 MHz Pentium. This performance reduction is certainly noticeable by a user running other application, but it greatly outperforms most other solution available today.

But a 2M system begins to slow thing with a 1,024x768x18 display and other multimedia applications running. For these higher-definition displays, or systems with MPEG encode or MPEG-2 decode capabilities, a second RDRAM is recommended.

6. Electrical Characteristics

6-1. Absolute Maximum Ratings

- **Supply Voltage (Vdd)** -------------------------------- **- 0.5 ~ 6 V**
- **Operating Temperature** -------------------------------- **0 ~ 70 ℃**
- **Storage Temperature** -------------------------------- **- 65 ~ + 175**
- **All Input and Output Voltages to Vss** ---------------------- **- 0.5 ~ Vcc + 0.5**
- **Power Dissipation(P_D)** -------------------------------- **2 W**

(When operating Concurret in Diplsay Mode, audio/video, fax/modem and so on. It is variable.)

This is a measured the power consumption of Mpact boards by looking at voltage drops across the series resistors on a PCI extender card.
The +3.3V and -12V currents were minimal, as might be expected.
Here are results for the other 2 rails, in the order +5V ; +12V ;

	First Test	Second Test
Windows, after boot-up..	1.53A ; 0.267A	----- ; ------
Windows, various multimedia apps..	1.69A ; 0.265A	----- ; ------
dbg2, after boot..	1.53A ; 0.207A	1.39A ; 0.051A
dbg2, after hwinit..	1.21A ; 0.400A	1.51A ; 0.105A
dbg2, after &vid..	1.31A ; 0.440A	1.58A ; 0.149A

The results show that around 300 mA of 12V current was transferred to the +5V rail on Second Test.
In windows, the highest +5V current drain was obtained with the "tunnel" 3D demo.
The variation with application was only 100mA or so.
The variation in +12V current with application was small.
It seems reasonable to predict all out currents from these figures, for windows with MPEG audio, 3D graphics, and video capture. This would be:

First Test : 1.7A ; 0.44A and Second Test : 2.0A ; 0.15A.

Some parts of the board, e.g. the video encoder and modem, remain unexercised.
The nominal power burned by M1S/M1LG + 2 RDRAMs + Rambus Termination when just refreshing a 1024x768x16 display with nothing else going on.
They fed 3.3V directly from the power supply to the Mpact and RDRAMs (so 3.3V regulator power was not measured), and 5V power was applied to the Vterm/Vref regulator:

GM90C701Q => 3.45W @ 3.3V + 275mW @ 5V = ~3.75W

When two audio streams + MPEG I were run, the power increased by ~250mW to:

GM90C701Q => 3.7W @ 3.3V + 330mW @ 5V = ~4W

6-2. DC Electrical Characteristics

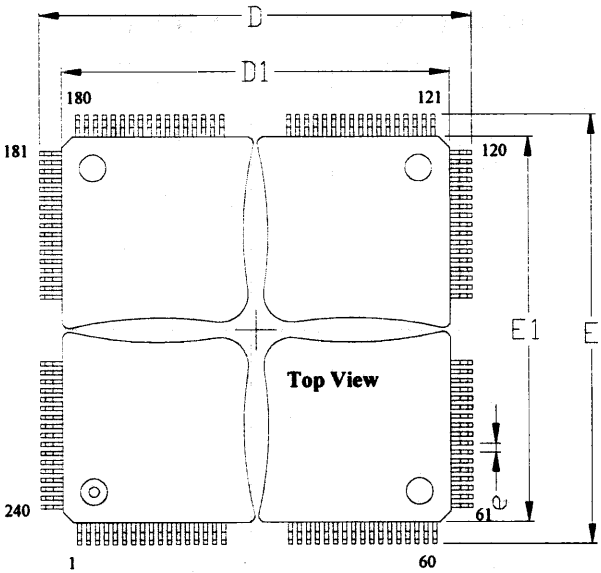
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{il}	Input Low Voltage	Vdd = 3.0 V , PCI , TTL		0.9 0.8	V
V_{ih}	Input High Voltage	Vdd = 3.6 V , PCI , TTL	1.8 2		V
V_{ol}	Output Low Voltage	Vdd = 3.0 V , PCI (Iol ; 1.5mA) , Video (Iol ; 4 mA) , PBUS (Iol ; 6 mA) , RAMDAC (Iol ; 4 mA)		0.3 0.4 0.4 0.4	V
V_{oh}	Output High Voltage	Vdd = 3.0 V , PCI (Ioh ; 0.5mA) , Video (Ioh ; 2 mA) , PBUS (Ioh ; 2 mA) , RAMDAC (Ioh ; 2 mA)	2.7 2.4 2.4 2.4		V
I_{ol}	Output Low Current	Vdd = 3.0 V , PCI (Vol ; 0.54mA) . Video (Vol ; 0.4 mA) , PBUS (Vol ; 0.4 mA) , RAMDAC (Vol ; 0.4 mA)	14.4 4 6 4	136.8	mA

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
Ioh	Output High Current	Vdd = 3.0 V , PCI (Voh ; 2.1mA) , Video (Voh ; 2.4 mA) , PBUS (Voh ; 2.4 mA) , RAMDAC (Voh ; 2.4 mA)	15.4 2 2 2	115.2	mA
Iil / Iih	Input Leakage	Vdd = 3.3 V	-10	10	uA

6-3. AC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
Tsu	Input Data Setup	Vdd = 3.0 V , PCI , Video , PBUS	7 4 7		uS
Thd	Input Data Hold	Vdd = 3.6 V , PCI , Video , PBUS	1 5 10		uS
Tpd	Output Pro Delay	Vdd = 3.0 V , PCI , Video , PBUS , RAMDAC	2 1.7	11 15 20	uS
Tdh	Output Data Hold	Vdd = 3.0 V , PCI , Video , PBUS , RAMDAC		 15 15 5.7	uS

7. Package Dimensions



UNIT : MM

	MIN.	TYP.	MAX.
A	3.55	3.78	4.20
A_1	0.25	0.38	—
A_2	3.30	3.40	3.50
D	34.40	34.60	34.80
D_1	31.90	32.00	32.10
E	34.40	34.60	34.80
E_1	31.90	32.00	32.10
L	0.50	0.60	0.70
L_1	1.30 REF		
e	0.50 BSC.		
b	0.16	—	0.28
C	0.09	—	0.20