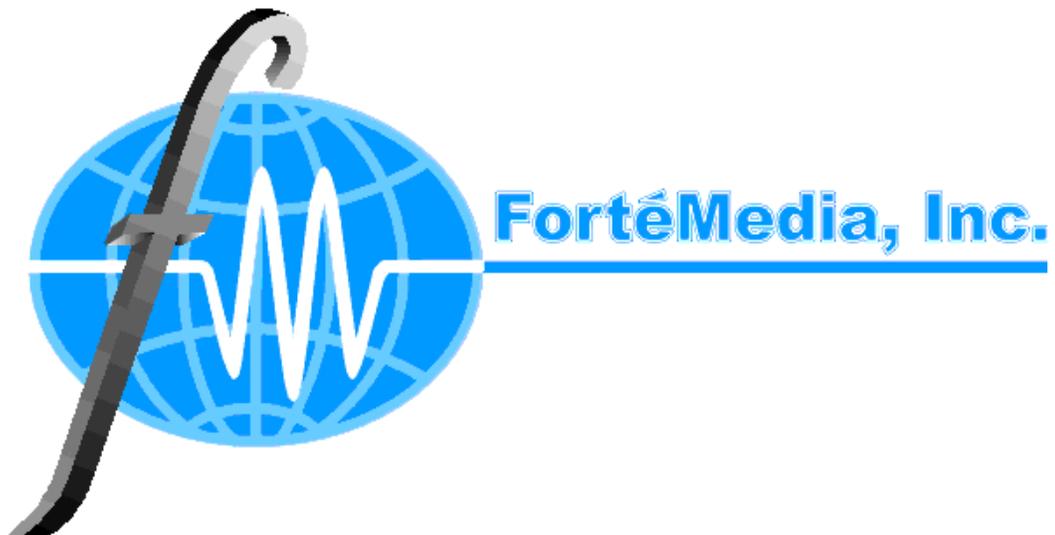# Fundamental PCI Audio Solution

FM801 - Hardware Design Specification

Revision 2.2

Written by

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1   INTRODUCTION

This document is describing the hardware design specification for *FM801*. It is intended as the design documentation for engineering team.

This document will cover the architecture of *FM801*, the detailed definition of *FM801* control registers, design interface protocol as well as functional blocks.

1.1   Terminology

SB   : Sound Blaster

SB Pro   : Sound Blaster Pro

SBE   : Sound Blaster Engine in *FM801*

AC'97   : Audio Codec 97.

FM synthesizer : FM music synthesizer

SRC   : Hw Sample Rate Converter

Digital Mixing   : Include Volume and Panning Control

DFC   : Data Flow Controller

2 OVERVIEW

FM801 is a single-chip PCI based highly-integrated digital audio controller. *FM801* supports all the legacy audio standard, including SB Pro, WSS, Game Port, MPU-401 and FM music synthesis while also supports the state-of-the-art audio standard DirectSound and Direct3D Sound from Microsoft with PCI interface. Combining with high-performance AC97 Codec, it provides the most cost-effective yet high quality audio experience to the PC end users.

2.1 Features

- PCI v.2.1 compliance with bus master and scatter-and-gather capability

- 100% Sound Blaster Pro legacy audio compatible on PCI (Legacy, DDMA, PC/PCI, Serial IRQ)

- H/W OPL3-compatible FM Synthesizer

- H/W high performance Sample Rate Converter and Digital Mixer

- Integrated MIDI UART with FIFO for MPU-401 Port

- Analog/Digital Joystick Interface (DirectInput Support)

- I^{2}S/ZV Port Support

- S/PDIF Digital Output Port Support

- 2/4/6 output channels support for surround sound and AC-3 application

- Power management supports Advanced Power Management (APM) v1.2, PCI Power Management Interface (PPMI) v1.0, Advanced Configuration and Power Interface (ACPI) v1.0 and PCI CLKRUN protocols

- H/W Master Volume Control (Up/Down/Mute)

- Support AC97 AC-link/AC-link 2.1

- Support secondary AC97 v.2.0 for docking station application

- Windows 95/WDM/Windows NT driver support

- Single-chip 100-pin package

2.2 Architecture Overview

FM801 is an PCI Audio device which supports Microsoft DirectSound and AC'98 standard, it also maintains Sound Blaster Pro, MIDI and MPU-401 compatibility, thus provides the most advanced audio standard supports and the backward compatibility to the legacy standard.
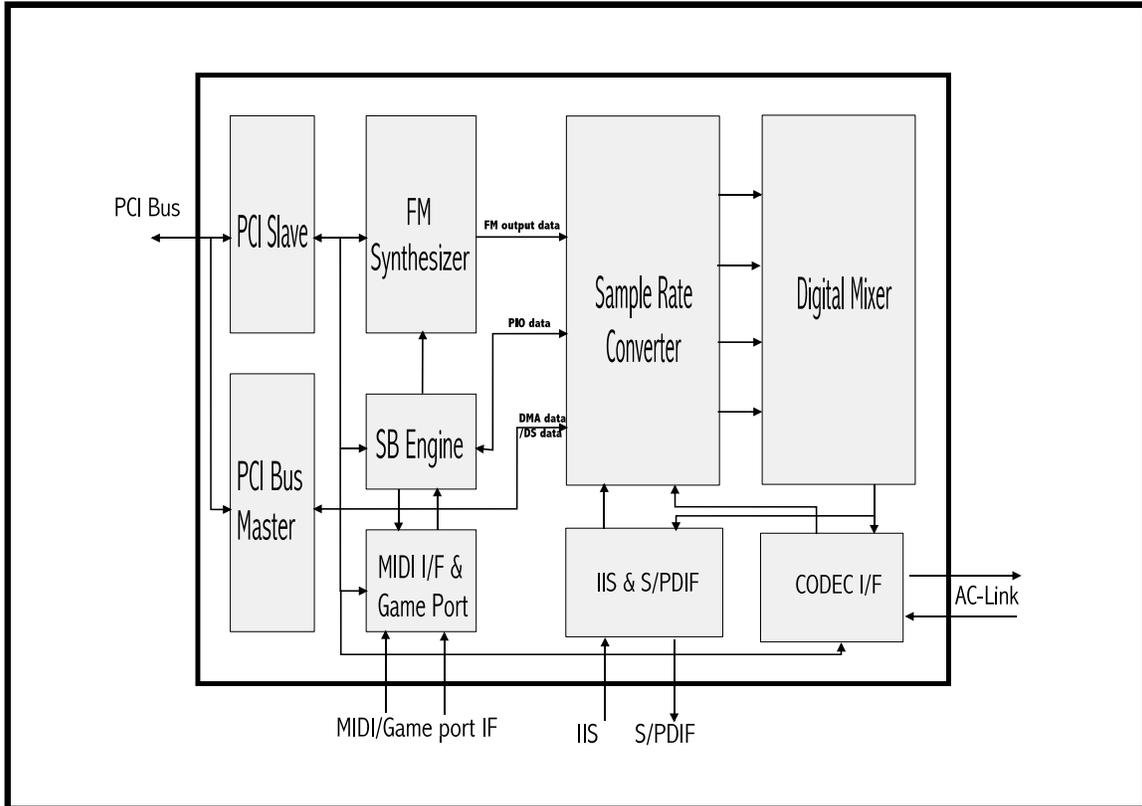
Block Diagram of ROME

Figure 1 Functional Block Diagram of FM801

FM801 can be partitioned into 5 major functional blocks: PCI Interface, FM Synthesizer, SB Engine(including MIDI Port and Game Port), Streaming engine and Peripheral Interface (including Codec IF, I²S IF and SPDIF).

PCI Interface provides the interface to the 33MHz, 32-bit PCI bus with the ability to support PCI configuration (PCI Plug & Play), PCI slave I/O cycles and PCI bus master memory read/write cycles. It also interfaces to all the internal blocks, serving as the gate to the system. This block can be further partitioned into 3 sub-blocks, DMA Controller, PCI slave IF and PCI master IF. PCI slave IF handles the PCI configuration and also translates the PCI I/O cycles to internal I/O cycles. Moreover, this sub-block is also the center of power controlling to the whole chip. PCI master IF mainly interfaces to the Streaming Engine and internal DMAC, providing the scheme of system memory access or DMA emulation to the SB Engine. It contains 2 sets of Ping-Pong buffer(16bytesX2) for playback and capture. DMA Controller will provide the functionality of ISA DMA Controller, thus resolving the legacy Audio issues on PCI bus. It also provides the address when PCI bus master is activated.

FM Synthesizer is the engine of 20-voice music synthesis. This block interfaces to the PCI slave IF, allowing the host system to control the synthesis parameters via I/O access. The output of the synthesizer will be sampled at 48KHz and stored in the 2-level FIFOs, allowing the Streaming Engine to do digital mixing with minimum effort.

SB Engine includes 3 sub-blocks: SB-Pro compatible state machine, MPU-401/MIDI port and Game port. It interfaces to the PCI IF and DMAC for SB legacy IO port access and ISA bus DMA emulation. It supports DDMA and Compaq backed 'Serial-IRQ' for ISA DMA and Interrupt issues.

Streaming Engine includes 3 main sub-blocks: Data Flow Controller, Sample Rate Converter and Digital Mixer. Sample Rate Converter will read the data from each sound source (FM, PCM Data, I2S) and converted it to 48khz data streams. Digital Mixer will then mix these sound sources into one output stream @48Khz and send it to Codec IF and SPDIF. For Capture, SRC will read the recording data either from Codec IF, FM or I2S. After converting the data stream from 48Khz to the designate sample rate, SRC will write the recording data into PCI Capture FIFO. PCI master will then execute bus master to write the data back to the system memory when one of the Ping-Pong FIFO is filled. Data Flow Controller will convert and pack the data into the desired format. For playback, it will throw away the junk and data and convert the non-16 bit PCM data into one uniform format: 16-bit stereo signed data for SRC to process. For capture, DFC will convert the 16-bit signed data into the desired format(8-bit/16-bit, Mono/Stereo) and pack into right alignment.

Peripheral Interface includes all the miscellaneous input/output interfaces: Codec IF, I²S, Volume Control and S/PDIF interface. I²S and S/PDIF IF will be accessed by Streaming Engine based on the fixed-rate interrupt (@48Khz).

3   IO PINS DESCRIPTIONS

FM801 is available in 100-pin PQFP and TQFP packages. The IO pins descriptions are tabled as following:

Table 1. PCI IF IO Pins (Total=53)

Pin Name	Pin #	IO Type	IO PAD Type	Description
PPCICLK		I		PCI Clock (33MHz)
PRST_		I		PCI System reset
PAD[31:0]		B		PCI address/data bus
PCBE[3:0]		B		PCI command/byte enable
PIRDYN_		B		PCI initiator ready
PTRDYN_		B		PCI target ready
PDEVSEL_		B		PCI device select
PFRAME_		B		PCI Frame
PIDSEL		I		PCI ID select
PPAR		B		PCI parity
PSTOP_		B		PCI stop
PINTA_		O		PCI interrupt A (For SB, DS, MIDI)
PINTB_ / PSERIRQ_		B		PCI interrupt B (For Game Port) / Serial IRQ
PREQ_		O		PCI bus request
PGNT_		I		PCI bus grant
PCREQ_		O		PC-PCI Request
PPERR_		B		Parity Error
PCGNT_		I		PC-PCI Grant
PME_		O		Power Management Enable

Table 2. Codec IF IO Pins (Total=7)

Pin Name	Pin #	IO Type	IO PAD Type	Description
PSP1MCLK		O		Serial Port I main clock
PSP1RST_		O		Serial Port I Codec reset
PSCLK1		I		Serial Port I Codec serial clock
PSDI1		I		Serial Port I Codec serial data in
PSDO1/ EPROMOB_*		O/I		Serial Port I Codec serial data out/ EPROM on board
PFS1/ I2CSEL**		O I		Serial Port I Codec frame sync I2C 2/4 wire select
PSDI2		I		Serial Port II Codec serial data in

Table 3. MIDI/Game Port IO Pins (Total=10)

Pin Name	Pin #	IO Type	IO PAD Type	Description
PTXD/TSTD[0]		O		MIDI transmitting data/Test Data Out [0]
PRXD/TSTD[1]		I/O		MIDI receiving data/Test Data Out [1]
P1PBUTA/TSTD[2]		I/O		Game Port 1 button A/Test Data Out [2]
P1PBUTB/TSTD[3]		I/O		Game Port 1 button B/Test Data Out [3]
P2PBUTA/TSTD[4]		I/O		Game Port 2 button A/Test Data Out [4]
P2PBUTB/TSTD[5]		I/O		Game Port 2 button B/Test Data Out [5]
P1PJOYX/TSTD[6]		B		Game Port 1 joystick X-axis/Test Data Out [6]
P1PJOYY/TSTD[7]		B		Game Port 1 joystick Y-axis/Test Data Out [7]
P2PJOYX/TSTD[8]		B		Game Port 2 joystick X-axis/Test Data Out [8]
P2PJOYY/TSTD[9]		B		Game Port 2 joystick Y-axis/Test Data Out [9]

*Note: * Jumper input. 0:EEPROM on board, 1: No EEPROM.*

Table 4. I²S and S/PDIF IF (Total=4)

Pin Name	Pin #	IO Type	IO PAD Type	Description
PBCLK/TSTD[10]		I/O		I2S Bit clock/Test Data Out [10]
PI2SD/TSTD[11]		I/O		I2S serial data/Test Data Out [11]
PLRCK/TSTD[12]		I/O		I2S left/right clock/Test Data Out [12]
SPDIFD/GPIO0 /INTB_EN*		I/O		S/PDIF Data / GPIO[0]/INTB Enable

*Note : *Jumper Input. 1=PCI INTB is required, 0=Not required.*

Table 5. Miscellaneous IO Pins (Total=6+ VDD/VSS)

Pin Name	Pin #	IO Type	IO PAD Type	Description
PXTAL0IN		I		FM801 Main clock (24.576mhz) Crystal in
PXTAL0OUT		O		FM801 Main clock (24.576mhz) Crystal out
PVOLUP/TSTD[13] /GPIO1/EPRMCK		I/O		Volume Up/Test Data Out [13]/ GPIO[1]/EEPROM Serial Clock
PVOLDN/TSTD[14] /GPIO2/EPRMDI		I/O		Volume Down/Test Data Out [14]/ GPIO[2]/EEPROM(93c57) Data In/ EEPROM(24c00) Data In & Out
PVMUTE/TSTD[15] /GPIO3/EPRMDO		I/O		Volume Mute/Test Data Out [15]/ GPIO[3]/EEPROM(93c57) Data Out
CLKRUN/EPRMCS**1**		B		PCI Clock Run/EEPROM(93c57) Chip select/ EEPROM(24c00) Serial Clock
VDD/VSS		I		Power ground pins

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1 External EEPROM will load 6-words of EPROM data into Subsystem Vendor ID, Subsystem ID (func0), Subsystem ID (func1), Vendor ID, Device ID (func0), Device ID (func1) in this order.

3.1 Strap Selected Option

Pin Name	Pin #	Condition	Description
EPROMOB_	90	Low/High	0=E2PROM on board, 1=No E2PROM.
I2CSEL	86	Low/High	0=93C57(Microchip.Atmel…), 1=24C00/24C01(Microchip)
INTB_EN	75	Low/High	0=No PCI INTB, 1=PCI INTB is required.

4   LEGACY AUDIO CONTROL REGISTERS

This section describes all the legacy audio control registers supported by *FM801*.

- SB base: 0x220, 0x240

- OPL-3 base: 0x388

- Game base: 0x200

- MPU base: 0x330, 0x300, 0x320, 0x340

4.1   OPL-3

Host Offset	R/W	Width	Description
SB base + 0	R	8	Status read
SB base + 0	W	8	Address bank0 write
SB base + 2	W	8	Address bank1 write
SB base + 1	R/W	8	Data write/Data read
SB base + 3	W		Data write
SB base + 8	R	8	Status read
SB base + 8	W	8	Address bank0 write
SB base + 9	W	8	Data write
OPL base + 0	R	8	Status read
OPL base + 0	W	8	Address bank0 write
OPL base + 2	W	8	Address bank1 write
OPL base + 1	R/W	8	Data write/Data read
OPL base + 3	W		Data write

4.2   SB Pro I/O

Host Offset	R/W	Width	Description
SB base + 6	W	8	SB DSP reset
SB base + A	R	8	SB DSP read data port
SB base + C	W	8	SB DSP write data port
SB base + C	R	8	SB DSP write buffer status
SB base + E	R	8	SB DSP read buffer status

4.3 SB Pro Mixer

Host Offset	R/W	Width	Description
SB base + 4	W	8	SB mixer address port
SB base + 5	R/W	8	SB mixer data port

4.4 Game Port

Host Offset	R/W	Width	Description
Game base + 0	W	8	Conventional game port
Game base + 1	R/W	8	Conventional game port

4.5 MPU-401

Host Offset	R/W	Width	Description
MPU base + 0	R/W	8	Data port
MPU base + 1	R	8	Status port
MPU base + 1	W	8	Command port

5   FM801 PCI CONFIGURATION REGISTERS

This section describes the summary and detailed description of *FM801* Configuration registers. *FM801* is a PCI multi-functions device (2 functions), Audio device(Function-0) and Game port device(Function-1). Therefore, there are 2 devices' configuration space defined in *FM801*.

5.1   FM801 PCI Audio Device Configuration Registers Summary Table

Table 6 PCI Audio Device (Function-0) Configuration Register Summary

Host Config Address	Host R/W	Power-on Value	Description
0x00~01	R	0x1319	Vendor ID
0x02~03	R	0x0801	Device ID
0x04~05	R/W	0x0000	PCI Command Register
0x06~07	R/W	0x0290	PCI Status Register
0x08	R	0xB1	Revision ID Register
0x09~0B	R	0x040100	Class Code (multimedia audio device)
0x0C	R	0x00	Cache Line Size Register (not implemented)
0x0D	R/W	0x00	Latency Timer
0x0E	R	0x80	Header Type
0x0F	R	0x00	BIST (not implemented)
0x10~13	R/W	0x00000001	I/O Base Register (offset=0x00~0x7F)
0x2C~2D	R	0x1319	Subsystem Vendor ID
0x2E~2F	R	0x1319	Subsystem ID
0x34	R	0xDC	Capabilities Pointer
0x3C	R/W	0x00	Interrupt Line Register
0x3D	R	0x01	Interrupt Pin Register (INTA#)
0x3E	R	0x04	Min Grant PCI Burst period
0x3F	R	0x28	Max Latency PCI grant period
0x40~41	R/W	0x907F	Legacy Audio Control
0xA0	R/W	0x00	DFC Reset Control
0xDC	R	0x01	Capability ID
0xDD	R	0x00	Next Item Pointer
0xDE~DF	R	0x0421	Power Management Capabilities
0xE0~E1	R/W	0x0000	Power Management Control/Status

5.2 FM801 PCI Audio Device Config. Registers Detailed Description

5.2.1 Vendor ID Register (R)

- Host Configuration Address: 0x00 – 0x01

- Power-on value: 0x1319

- Description: ForteMedia Vendor ID.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	1	0	0	0	1	1	0	0	1

5.2.2 Device ID Register (R)

- Host Configuration Address: 0x02 – 0x03

- Power-on value: 0x0801

- Description: FM801 part number - 801.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1

5.2.3 PCI Command Register (R/W)

- Host Configuration Address: 0x04 – 0x05

- Power-on value: 0x0000

- Description: Device capability on PCI operations.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						0	0	0	0	0	0	0	0	0	0

B0: Response to PCI I/O access - A value of 0 disables FM801's response to I/O access. A value of 1 enables FM801's response to I/O access.

B1: Response to PCI Memory access - A value of 0 disables FM801's response to memory access. A value of 1 enables FM801's response to memory access.

B2: Bus Master Capability - A value of 0 disables FM801 from generating PCI accesses. A value of 1 allows FM801 to behave as a bus master.

B3: Response to Special cycle - Zero always. Read only.

B4: Memory Write and Invalidate Command Generation - Zero always. Read only.

B5: VGA Palette Snoop - Zero always. Read only.

B6: PERR# Generation - If zero, FM801 ignore parity error it detects. If one FM801 will assert PERR# if parity error occurs.

B7: Address/Data stepping - Zero always. Read only.

B8: SERR# Generation - A value of 0 disables FM801 to generate SERR#. A value of 1 enables FM801 to generate SERR#.

B9: Fast Back-to-Back - Zero always. Read only.

B15~B10: Reserved.

5.2.4   PCI Status Register (R /W)

- Host Configuration Address: 0x06 – 0x07

- Power-on value: 0x0290

- Description: Status information for PCI bus related events.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	1	0	0	1				

B3~B0: Reserved

B4: PCI Power Management features appear in the standard configuration space header. Read Only.

B5: 66 MHz Capable- Zero always. Read only.

B6: UDF(User Definable Features) Support – Zero always

B7: Fast Back-to-Back - One always. Read only.

B8: PERR# active as Master - This bit is set when FM801, as a master, asserts PERR# or detects the assertion of PERR# by other agent. This bit is cleared by writing an one to it.

B10~9: DEVSEL# Timing (Read only) -

    0 0 = Fast

    0 1 = Medium (Always)

    1 0 = Slow

    1 1 = reserved

B11: Signaled Target Abort - 0 = No, 1 = Yes. Write one to clear.

B12: Received Target Abort - 0 = No, 1 = Yes. Write one to clear.

B13: Received Master Abort - 0 = No, 1 = Yes. Write one to clear.

B14: Signaled System Error - 0 = No, 1 = Yes. Write one to clear.

B15: Detected Parity Error - 0 = No, 1 = Yes. Write one to clear.

5.2.5   Revision ID Register (R)

- Host Configuration Address: 0x08

- Power-on value: 0xB1

- Description: B1h for 3rd revision.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								1	0	1	1	0	0	0	1

5.2.6   *Programming Interface Register of Class Code (R)*

- Host Configuration Address: 0x09

- Power-on value: 0x00

- Description: Specific register-level programming interface

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0								

5.2.7   *Sub-class code Register of Class Code (R)*

- Host Configuration Address: 0x0A

- Power-on value: 0x01(Func-0)

- Description: Sub-Class Code, Audio device

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0	0	0	0	0	0	0	1

5.2.8   *Base-class Code Register of Class Code (R)*

- Host Configuration Address: 0x0B

- Power-on value: 0x04(Func-0)

- Description: Base Class Code, Multimedia device

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0								

5.2.9   *Cache Line Size Register (R)*

- Host Configuration Address: 0x0C

- Description: Not implemented.

5.2.10 *Latency Timer Register (R/W)*

- Host Configuration Address: 0x0D

- Power-on value: 0x00

- Description: Specifies the maximum number of PCI clocks that FM801, as a bus master, will stay on the bus.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0								

5.2.11 Header Type Register (R)

- Host Configuration Address: 0x0E

- Power-on value: 0x80

- Description: Header type

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								1	0	0	0	0	0	0	0

B7: Set to one to indicate multifunctional device.

B6~B0: Specify layout type of bytes 10h~3Fh; type "0" for bytes 10~3Fh, as defined in the PCI spec.

5.2.12 BIST Register (R)

- Host Configuration Address: 0x0F

- Power-on value: 0x00

- Description: Not implemented.

5.2.13 Base Address Register (R/W)

- Host Configuration Address: 0x10 – 0x13

- Power-on value: 0x00000001

- Description: Starting address of FM801 control register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

B0: I/O Indicator - One always. Read only.

B1: reserved. Zero always. Read only.

B6~B2: Hardwired to zero. Read only.

B31~B7: Base Address - This address determines the starting address of 128 byte FM801 I/O registers mapped into PCI I/O space.

5.2.14 Subsystem Vendor ID (R)

- Host Configuration Address : 0x2C – 0x2D

- Power-on value : 0x1319

- Description : Subsystem Vendor ID. Can be written by external EEPROM. This register is shared between 2 functions.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	1	0	0	0	1	1	0	0	1

5.2.15 Subsystem ID (R)

- Host Configuration Address : 0x2E – 0x2F

- Power-on value : 0x1319

- Description : Subsystem ID. Can be written by external EEPROM

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	1	0	0	0	1	1	0	0	1

5.2.16 Capabilities Pointer (R)

- Host Configuration Address: 0x34

- Power-on value: 0xDC

- Description: This register is indicated where the PCI Power Management features appear in the standard configuration space header.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								1	1	0	1	1	1	0	0

5.2.17 Interrupt Line Register (R/W)

- Host Configuration Address: 0x3C

- Power-on value: 0x00

- Description: This register is used to communicate the interrupt line routing information.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0	0	0	0	0	0	0	0

5.2.18 Interrupt Pin Register (R)

- Host Configuration Address: 0x3D

- Power-on value: 0x01(Func-0)

- Description: This register of Func-0 is hardwired to 0x01, which indicates that FM801 uses INTA# as interrupt pin.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1								

5.2.19 Min Grant Period for PCI burst (R)

- Host Configuration Address: 0x3E

- Power-on value: 0x04 (1 us)

- Description: This register is used to specify how long of a burst period the device needs(in ¼ microsecond unit). FM801 will use 1 us burst period.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0	0	0	0	0	1	0	0

5.2.20 Max Latency for PCI Grant(R)

- Host Configuration Address: 0x3F

- Power-on value: 0x28 (10 us)

- Description: This register is used to specify how often the device needs(in ¼ microsecond unit) to gain access to the PCI bus. FM801 needs the PCI bus grant every 10 us.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	1	0	0	0								

5.2.21 Legacy Audio Control Register (R/W)

- Host Configuration Address: 0x40 – 0x41

- Power-on value: 0x907F

- Description: This register provides control for independent enable/disable for each of the legacy audio subfunctions. This register can only be accessed through Func0.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	1	0	0	0	0	0	1	1	1	1	1	1	1

B0: Sound Blaster Enable. 1=Enable SB I/O positive decoding, 0=Disable.

B1: FM Synthesis Enable. 1=Enable FM Synthesis register positive decoding, 0=Disable.

B2: Game Port Enable. 1=Enable Game Port register positive decoding, 0=Disable.

B3: MPU-401 I/O Enable. 1=Enable MPU-401 register positive decoding, 0=Disable.

B4: MPU-401 IRQ Enable. 1=Enable IRQ specified in B13-B11, 0=Disable.

B5: I/O Address Alias Control. 1=10-bit address decoding, 0=16-bit address decoding.

B7~B6: SB DMA Channel Select. 00=DMA CH0, 01=DMA CH1, 10=Reserved, 11=DMA CH3.

B10~B8: SB IRQ Select. 000=IRQ5, 001=IRQ7, 010=IRQ9, 011=IRQ10, 100=IRQ11, others=Reserved.

B13~B11: MIDI I/O IRQ Select. 000=IRQ5, 001=IRQ7, 010=IRQ9, 011=IRQ10, 100=IRQ11, others=Reserved.

B14: Serial IRQ. 1=Serial IRQ enable, 0=Disbale.

B15: Global Legacy Audio Disable, supersede B4~B0. 1=Disable legacy audio, 0=Enable.

5.2.22 DFC Reset Control (R/W)

- Host Configuration Address: 0xA0

- Power-on value: 0x00

- Description: DFC reset control.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
													0	0	0

B0 : Reset DFC pointer when reciveing PLAYBACK START command.

B1 : Reset DFC pointer when reciveing PLAYBACK STOP command.

B2 : DC Test (NAND Tree) Enable.

5.2.23 Capabilities ID (R)

- Host Configuration Address: 0xDC

- Power-on value: 0x01

- Description: "01" indicates that the linked list item as being the PCI Power Management Registers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0	0	0	0	0	0	0	1

5.2.24 Next Item Pointer (R)

- Host Configuration Address: 0xDD

- Power-on value: 0x00

- Description: "00" indicates that there are no additional items in the Capabilities list.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0								

5.2.25 Power Management Capabilities (R)

- Host Configuration Address: 0xDE – 0xDF

- Power-on value: 0x0421(Func-0)

- Description:Describes information on the capabilities of the function related to power management.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1

B2~B0: Version number.

B3: PME Clock. '0' indicates that no PCI clock is required to generated PME#.

B4: Reserved.

B5: Device Specific Initialization. '1' indicates that the function requires that a device specific initialization sequence following transition to the D0 uninitialized state.

B8~B6: Reserved.

B9(read only): D1 Support. 1=Yes, 0=No.

B10(read only): D2 Support. 1=Yes(Shutdown 24Mhz clock, I2S & AC97 DAC, ADC, Mixer), 0=No.

B15~B11: PME Support. For Func-0 device, power-on value is "00000", there's no PME support. For Func-1, it's "01000" which indicates that PME# can be asserted from D3hot or D0.

5.2.26 Power Management Control/Status (R/W)

- Host Configuration Address: 0xE0 – 0xE1

- Power-on value: 0x0000

- Description: This register is used to manage the PCI function's power management state as well as to enable/monitor power management events.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0							0	0

B1~B0: Power state.

B7~B2: Reserved.

B8: PME Enable.

B12~B9: Data select. (Read only)

B14~B13: Data scale. (Read only)

B15: PME Status. Writing '1' to this bit will clear it and cause the function to stop asserting a PME. This bit defaults to '0' indicates the function does not support PME# generation from D3cold.

5.3 FM801 PCI GamePort Device Config. Registers Summary Table

Table 7 PCI GamePort Device (Function-1) Configuration Register Summary

Host Config Address	Host R/W	Power-on Value	Description
0x00~01	R	0x1319	Vendor ID
0x02~03	R	0x0802	Device ID
0x04~05	R/W	0x0000	PCI Command Register
0x06~07	R/W	0x0290	PCI Status Register
0x08	R	0xB1	Revision ID Register
0x09~0B	R	0x090410	Class Code (Gameport controller)
0x0C	R	0x00	Cache Line Size Register (not implemented)
0x0D	R/W	0x00	Latency Timer
0x0E	R	0x80	Header Type
0x0F	R	0x00	BIST (not implemented)
0x10~13	R/W	0x00000001	I/O Base Register (offset=0x00~0x0F)
0x2C~2D	R	0x1319	Subsystem Vendor ID
0x2E~2F	R	0x1319	Subsystem ID
0x34	R	0xDC	Capabilities Pointer
0x3C	R/W	0x00	Interrupt Line Register
0x3D	R	0x02	Interrupt Pin Register (INTB#)
0x3E	R	0x04	Min Grant PCI Burst period
0x3F	R	0x28	Max Latency PCI grant period
0x40~41	R	0x907F	Legacy Audio Control (only bit-2 is writeable)
0xDC	R	0x01	Capability ID
0xDD	R	0x00	Next Item Pointer
0xDE~DF	R	0x5221	Power Management Capabilities
0xE0~E1	R/W	0x0000	Power Management Control/Status

5.4   FM801 PCI Game Device Config. Registers Detailed Description

5.4.1   Vendor ID Register (R)

- Host Configuration Address: 0x00 – 0x01

- Power-on value: 0x1319

- Description: ForteMedia Vendor ID.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	1	0	0	0	1	1	0	0	1

5.4.2   Device ID Register (R)

- Host Configuration Address: 0x02 – 0x03

- Power-on value: 0x0802

- Description: FM801 Gameport device ID – 802.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0

5.4.3   PCI Command Register (R/W)

- Host Configuration Address: 0x04 – 0x05

- Power-on value: 0x0000

- Description: Device capability on PCI operations.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
▨	▨	▨	▨	▨	▨	0	0	0	0	0	0	0	0	0	0

B0: Response to PCI I/O access - A value of 0 disables FM801's response to I/O access. A value of 1 enables FM801's response to I/O access.

B1: Response to PCI Memory access - A value of 0 disables FM801's response to memory access. A value of 1 enables FM801's response to memory access.

B2: Bus Master Capability - A value of 0 disables FM801 from generating PCI accesses. A value of 1 allows FM801 to behave as a bus master.

B3: Response to Special cycle - Zero always. Read only.

B4: Memory Write and Invalidate Command Generation - Zero always. Read only.

B5: VGA Palette Snoop - Zero always. Read only.

B6: PERR# Generation - If zero, FM801 ignore parity error it detects. If one FM801 will assert PERR# if parity error occurs.

B7: Address/Data stepping - Zero always. Read only.

B8: SERR# Generation - A value of 0 disables FM801 to generate SERR#. A value of 1 enables FM801 to generate SERR#.

B9: Fast Back-to-Back - Zero always. Read only.

B15~B10: Reserved.

5.4.4   PCI Status Register (R /W)

- Host Configuration Address: 0x06 – 0x07

- Power-on value: 0x0290

- Description: Status information for PCI bus related events.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	1	0	0	1				

B3~B0: Reserved

B4: PCI Power Management features appear in the standard configuration space header. Read Only.

B5: 66 MHz Capable- Zero always. Read only.

B6: UDF(User Definable Features) Support – Zero always

B7: Fast Back-to-Back - One always. Read only.

B8: PERR# active as Master - This bit is set when FM801, as a master, asserts PERR# or detects the assertion of PERR# by other agent. This bit is cleared by writing an one to it.

B10~9: DEVSEL# Timing (Read only) -

> 0 0 = Fast

> 0 1 = Medium (Always)

> 1 0 = Slow

> 1 1 = reserved

B11: Signaled Target Abort - 0 = No, 1 = Yes. Write one to clear.

B12: Received Target Abort - 0 = No, 1 = Yes. Write one to clear.

B13: Received Master Abort - 0 = No, 1 = Yes. Write one to clear.

B14: Signaled System Error - 0 = No, 1 = Yes. Write one to clear.

B15: Detected Parity Error - 0 = No, 1 = Yes. Write one to clear.

5.4.5   Revision ID Register (R)

- Host Configuration Address: 0x08

- Power-on value: 0xB1

- Description: B1h for 3rd revision.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								1	0	1	1	0	0	0	1

5.4.6   Programming Interface Register of Class Code (R)

- Host Configuration Address: 0x09

- Power-on value: 0x10

- Description: Specific register-level programming interface

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	0								

5.4.7   Sub-class code Register of Class Code (R)

- Host Configuration Address: 0x0A

- Power-on value: 0x04(Func-1)

- Description: Sub-Class Code, Gameport controller

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0	0	0	0	0	1	0	0

5.4.8   Base-class Code Register of Class Code (R)

- Host Configuration Address: 0x0B

- Power-on value: 0x09(Func-1)

- Description: Base Class Code, Input device

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	1								

5.4.9   Cache Line Size Register (R)

- Host Configuration Address: 0x0C

- Description: Not implemented.

5.4.10 Latency Timer Register (R/W)

- Host Configuration Address: 0x0D

- Power-on value: 0x00

- Description: Specifies the maximum number of PCI clocks that FM801, as a bus master, will stay on the bus.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0								

5.4.11 Header Type Register (R)

- Host Configuration Address: 0x0E

- Power-on value: 0x80

- Description: Header type

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								1	0	0	0	0	0	0	0

B7: Set to one to indicate multifunctional device.

B6~B0: Specify layout type of bytes 10h~3Fh; type "0" for bytes 10~3Fh, as defined in the PCI spec.

5.4.12 BIST Register (R)

- Host Configuration Address: 0x0F

- Power-on value: 0x00

- Description: Not implemented.

5.4.13 Base Address Register (R/W)

- Host Configuration Address: 0x10 – 0x13

- Power-on value: 0x00000001

- Description: Starting address of FM801 control register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

B0: I/O Indicator - One always. Read only.

B1: reserved. Zero always. Read only.

B3~B2: Hardwired to zero. Read only.

B31~B4: Base Address - This address determines the starting address of 16 byte FM801 I/O registers mapped into PCI I/O space for Gameport.

5.4.14 Subsystem Vendor ID (R)

- Host Configuration Address : 0x2C – 0x2D

- Power-on value : 0x1319

- Description : Subsystem Vendor ID. Can be written by external EEPROM. This register is shared between 2 functions.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	1	0	0	0	1	1	0	0	1

5.4.15 Subsystem ID (R)

- Host Configuration Address : 0x2E – 0x2F

- Power-on value : 0x1319

- Description : Subsystem Vendor ID. Can be written by external EEPROM.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	1	0	0	0	1	1	0	0	1

5.4.16 Capabilities Pointer (R)

- Host Configuration Address: 0x34

- Power-on value: 0xDC

- Description: This register is indicated where the PCI Power Management features appear in the standard configuration space header.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								1	1	0	1	1	1	0	0

5.4.17 Interrupt Line Register (R/W)

- Host Configuration Address: 0x3C

- Power-on value: 0x00

- Description: This register is used to communicate the interrupt line routing information.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0	0	0	0	0	0	0	0

5.4.18 Interrupt Pin Register (R)

- Host Configuration Address: 0x3D

- Power-on value: 0x02(Func-1)

- Description: The register of Func-1 is hardwired to 0x02, which indicates that FM801 Func1 uses INTB# as interrupt pin.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0								

5.4.19 Min Grant Period for PCI burst (R)

- Host Configuration Address: 0x3E

- Power-on value: 0x04 (1 us)

- Description: This register is used to specify how long of a burst period the device needs(in ¼ microsecond unit). FM801 will use 1 us burst period.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0	0	0	0	0	1	0	0

5.4.20 Max Latency for PCI Grant(R)

- Host Configuration Address: 0x3F

- Power-on value: 0x28 (10 us)

- Description: This register is used to specify how often the device needs(in ¼ microsecond unit) to gain access to the PCI bus. FM801 needs the PCI bus grant every 10 us.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	1	0	0	0								

5.4.21 Legacy Audio Control Register (R)

- Host Configuration Address: 0x40 – 0x41

- Power-on value: 0x907F

- Description: This register provides control for independent enable/disable for each of the legacy audio subfunctions. This register can only be accessed through Func0.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	1	0	0	0	0	0	1	1	1	1	1	1	1

B0: Sound Blaster Enable. 1=Enable SB I/O positive decoding, 0=Disable.

B1: FM Synthesis Enable. 1=Enable FM Synthesis register positive decoding, 0=Disable.

B2 (R/W): Game Port Enable. 1=Enable Game Port register positive decoding, 0=Disable.

B3: MPU-401 I/O Enable. 1=Enable MPU-401 register positive decoding, 0=Disable.

B4: MPU-401 IRQ Enable. 1=Enable IRQ specified in B13-B11, 0=Disable.

B5: I/O Address Alias Control. 1=10-bit address decoding, 0=16-bit address decoding.

B7~B6: SB DMA Channel Select. 00=DMA CH0, 01=DMA CH1, 10=Reserved, 11=DMA CH3.

B10~B8: SB IRQ Select. 000=IRQ5, 001=IRQ7, 010=IRQ9, 011=IRQ10, 100=IRQ11, others=Reserved.

B13~B11: MIDI I/O IRQ Select. 000=IRQ5, 001=IRQ7, 010=IRQ9, 011=IRQ10, 100=IRQ11, others=Reserved.

B14: Serial IRQ. 1=Serial IRQ enable, 0=Disbale.

B15: Global Legacy Audio Disable, supersede B4~B0. 1=Disable legacy audio, 0=Enable.

5.4.22 Capabilities ID (R)

- Host Configuration Address: 0xDC

- Power-on value: 0x01

- Description: "01" indicates that the linked list item as being the PCI Power Management Registers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0	0	0	0	0	0	0	1

5.4.23 Next Item Pointer (R)

- Host Configuration Address: 0xDD

- Power-on value: 0x00

- Description: "00" indicates that there are no additional items in the Capabilities list.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0								

5.4.24 Power Management Capabilities (R)

- Host Configuration Address: 0xDE – 0xDF

- Power-on value: 0x5221(Func-1)

- Description:Describes information on the capabilities of the function related to power management.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	0	0	1	0	0	0	1	0	0	0	0	1

B2~B0: Version number.

B3: PME Clock. '0' indicates that no PCI clock is required to generated PME#.

B4: Reserved.

B5: Device Specific Initialization. '1' indicates that the function requires that a device specific initialization sequence following transition to the D0 uninitialized state.

B8~B6: Reserved.

B9(read only): D1 Support. 1=Yes(Gameport power saving mode), 0=No.

B10(read only): D2 Support. 1=Yes, 0=No.

B15~B11: PME Support. For Func-0 device, power-on value is "00000", there's no PME support. For Func-1, it's "01010" which indicates that PME# can be asserted from D3hot, D1 or D0.

5.4.25 Power Management Control/Status (R/W)

- Host Configuration Address: 0xE0 – 0xE1

- Power-on value: 0x0000

- Description: This register is used to manage the PCI function's power management state as well as to enable/monitor power management events.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	▨	▨	▨	▨	▨	▨	0	0

B1~B0: Power state.

B7~B2: Reserved.

B8: PME Enable.

B12~B9: Data select. (Read only)

B14~B13: Data scale. (Read only)

B15: PME Status. Writing '1' to this bit will clear it and cause the function to stop asserting a PME. This bit defaults to '0' indicates the function does not support PME# generation from D3cold.

6   FM801 PCI CONTROL REGISTERS

This section describes the summary and detailed description of *FM801* I/O Control registers.

6.1   FM801 Audio Device Control Registers Summary Table

This section describes the summary and details of FM801 Audio Device Control Registers.

Table 8 FM801 Audio Device Control Registers Summary Table

Host Offset	Host R/W	Power-on Value	Description
0x00~01	R/W	0x8808	PCM Out Volume
0x02~03	R/W	0x8808	FM Out Volume
0x04~05	R/W	0x8808	I2S Volume
0x06	R/W	0x00	Digital Recording Source Select
0x08~09	R/W	0xCA00	Playback Channel Control
0x0A~0B	R/W	-	Playback Channel Data Length
0x0C~0F	R/W	-	Playback Channel Buffer I System Starting Address
0x10~13	R/W	-	Playback Channel Buffer II System Starting Address
0x14~15	R/W	0xCA00	Capture Channel Control
0x16~17	R/W	-	Capture Channel Data Length
0x18~1B	R/W	-	Capture Channel Buffer I System Starting Address
0x1C~1F	R/W	-	Capture Channel Buffer II System Starting Address
0x22~23	R/W	0x0000	Codec Control
0x24~25	R/W	0x0003	I^{2}S Mode Control
0x26	R	0xXX	Volume Up/Dn/Mute Status
0x29	R/W	0x00	I2C Control
0x2A~2B	R/W	0x00	Codec Index Register Command Port
0x2C~2D	R/W	-	Codec Index Register Data Port
0x30	R/W	-	MPU401 Data port
0x31	R/W	0x80	MPU401 Command/Status port
0x52~53	R/W	0x0E00	General Purpose I/O Control
0x54~55	R/W	0x280C	General Control
0x56~57	R/W	0x00DF	Interrupt Mask Control
0x5B	R/W	0x00	Interrupt Status/Clear
0x68	R/W	-	OPL-3 status read/address bank0 write (0x388)

Host Offset	Host R/W	Power-on Value	Description
0x69	R/W	-	OPL-3 data write (0x389)
0x6A	W	-	OPL-3 address bank1 write (0x38A)
0x6B	W	-	OPL-3 data write (0x38B)
0x70~71	R/W	0x0000	FM801 Blocks Power down control

6.2 FM801 Audio Device Control Registers Detailed Description

6.2.1 PCM Out Volume

- Host Offset Address: 0x00 - 0x01

- Power-on value: 0x8808

- Description: PCM Out Volume

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	▨	▨	0	1	0	0	0	▨	▨	▨	0	1	0	0	0

B15: PCM Out Mute.

B14~B13: Reserved.

B12~B8: PCM Right Channel Gain. 00000=+12db gain, 01000=0db gain, 11111=-34.5db gain.
(each step corresponds to approximately 1.5db)

B7~B5: Reserved.

B4~B0: PCM Left Channel Gain. 00000=+12db gain, 01000=0db gain, 11111=-34.5db gain.
(each step corresponds to approximately 1.5db)

* B15, B12~B8, B4~B0: read/write by host.

6.2.2 FM Out Volume

- Host Offset Address: 0x02 - 0x03

- Power-on value: 0x8808

- Description: FM Out Volume

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	▨	▨	0	1	0	0	0	▨	▨	▨	0	1	0	0	0

B15: FM Out Mute.

B14~B13: Reserved.

B12~B8: FM Right Channel Gain. 00000=+12db gain, 01000=0db gain, 11111=-34.5db gain.
(each step corresponds to approximately 1.5db)

B7~B5: Reserved.

B4~B0: FM Left Channel Gain. 00000=+12db gain, 01000=0db gain, 11111=-34.5db gain. (each
step corresponds to approximately 1.5db)

* B15, B12~B8, B4~B0: read/write by host.

6.2.3   I2S Volume

- Host Offset Address: 0x04 - 0x05

- Power-on value: 0x8808

- Description: I2S Volume

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1			0	1	0	0	0				0	1	0	0	0

B15: I2S Out Mute.

B14~B13: Reserved.

B12~B8: I2S Right Channel Gain. 00000=+12db gain, 01000=0db gain, 11111=-34.5db gain. (each step corresponds to approximately 1.5db)

B7~B5: Reserved.

B4~B0: I2S Left Channel Gain. 00000=+12db gain, 01000=0db gain, 11111=-34.5db gain. (each step corresponds to approximately 1.5db)

* B15, B12~B8, B4~B0: read/write by host.

6.2.4   Digital Recording Source Select

- Host Offset Address: 0x06

- Power-on value: 0x00

- Description: Digital Recording Source Select.

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
													0	0	0

B2~B0: Digital Recording Source Select. 000=Recording Data from ADC of AC97 primary codec, 001=FM, 010=I2S, 011=PCM, 100=Recording Data from ADC of AC97 secondary codec.

B7~B3: Reserved.

* B2~B0: read/write by host.

6.2.5 Playback Channel Control

- Host Offset Address: 0x08 – 0x09

- Power-on value: 0xCA00

- Description: Direct Sound Playback Channel Control.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	1	0	1	0	0	0	0	▨	▨	0	0	0

B0: DFC/PFIFO data empty. 1=Empty, 0=Not empty.

B1: Current buffer I transfer is the last transfer. 0=No, 1=Yes.

B2: Current buffer II transfer is the last transfer. 0=No, 1=Yes.

B4~B3: Reserved.

B5: Channel Action. 0=Stop Transfer, 1=Start Transfer.

B6: Channel Pause. 0=Normal, 1=Transfer Pause. (To pause, bit-5 has to remain '1')

B7: Channel Stop Point. 0=At the end of current buffer, 1=Immediately stop when receiving Stop command.

B11~B8: Sampling Rate. 0000=5.5Khz, 0001=8Khz, 0010=9.6Khz, 0011=11.025Khz, 0100=16Khz, 0101=19.2Khz, 0110=22.05Khz, 0111=32Khz, 1000=38.4Khz, 1001=44.1Khz, 1010=48Khz.

B13~B12: Reserved.

B14: Data Format. 0=8-bit unsigned, 1=16-bit signed.

B15: Stereo/Mono. 0=Mono, 1=Stereo.

* B15~B5, B2~B1: read/write by host. B0:read only.

6.2.6 Playback Channel Data Length/Current Count

- Host Offset Address: 0x0A - 0x0B

- Power-on value: 0xXXXX

- Description: Direct Sound Playback Channel Data Length & Current Count.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

B15~B0(write): DS Channel Data Length for buffer I and II (Have to be the same size for both buffers). **The actual transfer count will be this register value plus 1**.

B15~B0(read): DS Channel Data Current Remaining Count.(not available until playback starts)

* B15~B0: read/write by host.

6.2.7 *Playback Channel Buffer I System Starting Address*

- Host Offset Address: 0x0C - 0x0F

- Power-on value: 0xXXXX

- Description: Direct Sound Playback Channel Buffer I System Starting Address.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

B31~B0(write): DS Playback Channel Buffer I System Starting Address.

B31~B0(read): DS Playback Channel Buffer current address.

* B31~B0: read/write by host.

6.2.8 *Playback Channel Buffer II System Starting Address*

- Host Offset Address: 0x10 - 0x13

- Power-on value: 0xXXXX

- Description: Direct Sound Playback Channel Buffer II System Starting Address.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

B31~B0(write): DS Playback Channel Buffer II System Starting Address.

B31~B0(read): DS Playback Channel Buffer current address.

* B31~B0: read/write by host.

6.2.9 *Capture Channel Control*

- Host Offset Address: 0x14 – 0x15

- Power-on value: 0xCA00

- Description: Direct Sound Capture Channel Control.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	▨	▨	1	0	1	0	0	0	0	▨	▨	0	0	▨

B0: Reserved.

B1: Current buffer I transfer is the last transfer. 0=No, 1=Yes.

B2: Current buffer II transfer is the last transfer. 0=No, 1=Yes.

B4~B3: Reserved.

B5: Channel Action. 0=Stop Transfer, 1=Start Transfer.

B6: Channel Pause. 0=Normal, 1=Transfer Pause. (To pause, bit-5 has to remain '1')

B7: Channel Stop Point. 0=At the end of current buffer, 1=Immediately stop when receiving Stop command.

B11~B8: Sampling Rate. 0000=5.5Khz, 0001=8Khz, 0010=9.6Khz, 0011=11.025Khz, 0100=16Khz, 0101=19.2Khz, 0110=22.05Khz, 0111=32Khz, 1000=38.4Khz, 1001=44.1Khz, 1010=48Khz.

B13~B12: Reserved.

B14: Data Format. 0=8-bit unsigned, 1=16-bit signed.

B15: Stereo/Mono. 0=Mono, 1=Stereo.

* B15~B14, B11~B5, B2~B0: read/write by host.

6.2.10 *Capture Channel Data Length/Current Count*

- Host Offset Address: 0x16 - 0x17

- Power-on value: 0xXXXX

- Description: Capture Channel Data Length & Current Count.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

B15~B0(write): Capture Channel Data Length for buffer I and II (Have to be the same size for both buffers). **The actual transfer count will be this register value plus 1**.

B15~B0(read): DS Channel Data Current Remaining Count.(not available until capture starts)

* B15~B0: read/write by host.

6.2.11 Capture Channel Buffer I System Starting Address

- Host Offset Address: 0x18 - 0x1B

- Power-on value: 0xXXXX

- Description: Capture Channel Buffer I System Starting Address.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

B31~B0(write): Capture Channel Buffer I System Starting Address.

B31~B0(read): Capture Channel Buffer current address.

* B31~B0: read/write by host.

6.2.12 Capture Channel Buffer II System Starting Address

- Host Offset Address: 0x1C - 0x1F

- Power-on value: 0xXXXX

- Description: Direct Sound Playback Channel Buffer II System Starting Address.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

B31~B0(write): Capture Channel Buffer II System Starting Address.

B31~B0(read): Capture Channel Buffer current address.

* B31~B0: read/write by host.

6.2.13 Codec Control

- Host Offset Address: 0x22 - 0x23

- Power-on value: 0x0000

- Description: Audio Codec Control.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						0	0		0	0					

B4~B0: Reserved.

B5: Codec Cold Reset. 1=Cold Reset, 0=Normal.

B6: AC'97 Warm Reset. 1=Warm Reset, 0=Normal.

B8: AC'97 ATE Test Mode. 1=ATE Test Mode On, 0=Normal.

B9: AC'97 GPIO Mode is enable. 1=Enable, 0=Disable.

B15~B10, B7: Reserved.

* B9~B8, B6~B5: read/write by Host.

6.2.14 I²S Mode Control

- Host Offset Address: 0x24 – 0x25

- Power-on value: 0x0003

- Description: I²S Serial Port Data Format Mode Control.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0	0	0				1	1

B1~B0: I2S Format. 00, 01=DAC, Digital Format. 10=ADC, DSP Serial Port, 11=I2S Mode.

B4~B2: Reserved.

B5: I2S Sample Rate Source Select. 1=Sw Control, 0=Hw Logic Detect.

B7~B6: I2S Sampling Rate. 00=48Khz, 01=44.1Khz, 10=32Khz.

B15~B8: Reserved.

* B7~B5, B1~B0: read/write by Host.

6.2.15 *Volume Up/Dn/Mute Status & Volume Counter Enable*

- Host Offset Address: 0x26

- Power-on value: 0xXX

- Description: Volume Up/Dn/Mute Status(Read) & Volume Counter Enable(Write).

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
													0	0	0

B0: Volume Up button is pushed. 1=Pushed, 0=No activity.

B1: Volume Down button is pushed. 1=Pushed, 0=No activity.

B2: Volume Mute button is pushed. 1=Pushed, 0=No activity.

B7~B3: Reserved.

* B2~B0: read only by host.

** When write to this register will enable the volume control counter to start counting.

** When both volume up and down are pushed at the same time, it will mute the volume.

6.2.16 *I2C Control*

7   Host Offset Address : 0x29

8   DSP I/O Address : N/A

9   Power-on value : 0x00

10 Description : I2C Control.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0	0	0	0	0	0	0	0

B0: I2C Clock output.

B1: I2C Data output.

B2: I2C Chip select. 1=Enable, 0=Disable.

B3: I2C Port Enable. 1=Enable, 0=Disable.

B4: I2C read. 1=Read from EPROM, 0=Disable.

B5: I2C read from beginning of EPROM.

B6: I2C 4 bytes data are ready. 1=Ready, 0=Not ready.

B7: I2C Data Input. 1=Enable, 0=Disable.

* B7~B6: read only by host. B3~B0: read/write by host.

10.1.1 Codec Index Register Command Port

- Host Offset Address: 0x2A – 0x2B

- Power-on value: 0x0000

- Description: Audio Codec Index Register Command Port.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				0	0	0	0	0	-	-	-	-	-	-	-

B6~B0: Codec Index Address.

B7: Read/Write Command. 0=Write, 1=Read.

B8: Data Port Valid Flag. 0=Invalid, 1=Valid.

B9: Command Port Status. 0=Ready, 1=Busy.

B11~B10: Codec ID been programmed.

* B9~B8: read only. B11~B10, B7~B0: read/write by host.

10.1.2 Codec Index Register Data Port

- Host Offset Address: 0x2C - 0x2D

- Power-on value: 0xXXXX

- Description: Audio Codec Index Register Data port

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

B15~B0: Codec Register data port.

* B15~B0: read/write by host.

10.1.3 MPU401 Data Port

- Host Offset Address: 0x30

- Power-on value: N/A

- Description: MPU401 Data Port.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								-	-	-	-	-	-	-	-

B7~B0: MPU401 Data [7:0]

* B7~B0: read/write by Host.

10.1.4 MPU401 Command/Status Port

- Host Offset Address: 0x31

- Power-on value: 0x80

- Description: MPU401 Command/Status Port.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	0	0	0	0								

B15~B8(Write): MPU401 Command [7:0]

* B15~B8: Write by Host.

B15(Read): MIDI Data Valid. 1=Not Valid, 0=Valid.

B14(Read): MIDI Cmd/Data Port Status. 1=Busy, 0=Not Busy.

B13~B10(Read): MIDI Valid Data Count.

B9~B8(Read): Reserved.

* B13~B10: read by Host.

10.1.5 General Purpose I/O Control

- Host Offset Address: 0x52 – 0x53

- Power-on value: 0x0E00

- Description: General Purpose I/O Pins Control.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0

B3~B0: General Purpose I/O [3:0] (Go through FM801)

B7~B4: General Purpose I/O [7:4] (Go though AC'97)

B11~B8: General Purpose I/O [3:0] Configuration. 1=Input, 0=Output.

B15~B12: General Purpose Output Pins Select [3:0]. 1=GPIO select, 0=Other functions.

* B15~B0: read/write by Host.

10.1.6 General Control

- Host Offset Address: 0x54 - 0x55

- Power-on value: 0x280C

- Description: General Control of the *FM801* Hardware.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	1	0	0	0	0	0	0	0	1	1	0	0

B0: Software Warm Reset. 1=Software Warm Reset, 0=Normal.

B1: PC/PCI Enable. 1=Enable, 0=Disable(Using other Legacy/DDMA mode)

B2: SPDIF Output Enable. 1=Enable, 0=Disable.

B3: Check system retry cycle before starting write-back. 1=Enable, 0=Disable.

B4: SB short write-back enable. 1=Enable, 0=Disable.

B5: DMAC Byte-counter interrupt control select. 0=DMAC update speed, 1=Byte consuming table (according to SB sampling rate)

B7~B6: Volume division control. 00=No division, 01=All Sources Divided by 2, 10=Divided by 4.

B9~B8: PC/PCI data access speed. 00=1 byte, 01=2 bytes, 10=4 bytes, 11=N/A.

B14~B10: Legacy 2 mode back-to-back cycle retry counter.

B15: Write-back retry counter enable. 1=Enable, 0=Disable.

* B15~B0: read/write by Host.

10.1.7 Interrupt Mask Control

- Host Offset Address: 0x56 - 0x57

- Power-on value: 0x00DF

- Description: Interrupt Mask Control of the *FM801* Hardware. If it is set, it will mask the interrupt to the host.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								1	1	0	1	1	1	1	1

B0: Playback Channel Interrupt Mask. 1=Mask, 0=Non-Mask.

B1: Capture Channel Interrupt Mask. 1=Mask, 0=Non-Mask.

B5~B2: Reserved. (Do not change the initial value)

B6: Volume Control Interrupt Mask. 1=Mask(Polling mode), 0=Non-Mask. (only set when Sw routing mode is selected, bit15 of PCI cfg.0x97=0)

B7: MPU401 Interrupt Mask(shadowed by bit-4 of configuration register(0x40~41)). 1=Mask(MPU401 enhancement mode), 0=Non-Mask.

B15~B8: Reserved.

* B6~B0: read/write by host. B7: read only by host.

10.1.8 Interrupt Status/Clear

- Host Offset Address: 0x5B

- Power-on value: 0x00

- Description: P/C Channel, Hw Timer, Modem DAA or MPU-401 interrupt will set this register corresponding bits. Write '1' will clear the interrupt, write '0' will have no effect.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0								

B8: Playback Channel Interrupt.

B9: Capture Channel Interrupt.

B13~B10: Reserved.

B14: Volume Control Interrupt.

B15: MPU-401 Interrupt.

* B15, B9~B8: read/write by Host and DSP. B13: read only by host.

10.1.9 OPL-3 status read/address bank0 write

- Host Offset Address: 0x68 (equivalent to ISA 0x388)

- Power-on value: N/A

- Description: OPL-3 status read/address bank0 write.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								-	-	-	-	-	-	-	-

B7~B0: OPL-3 status/address bank0.

*B7~B0: read/write by host.

10.1.10   OPL-3 data write/data read

- Host Offset Address: 0x69 (equivalent to ISA 0x389)

- Power-on value: N/A

- Description: OPL-3 data write/data read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-								

B15~B8: OPL-3 data write/data read.

*B15~B8: read/write by host.

10.1.11   OPL-3 address bank1 write

- Host Offset Address: 0x6A (equivalent to ISA 0x38A)

- Power-on value: N/A

- Description: OPL-3 address bank1 write.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								-	-	-	-	-	-	-	-

B7~B0: OPL-3 address bank1 write.

*B7~B0: write only by host.

10.1.12   OPL-3 data write

- Host Offset Address: 0x6B (equivalent to ISA 0x38B)

- Power-on value: N/A

- Description: OPL-3 data write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-								

B15~B8: OPL-3 data write.

*B15~B8: write only by host.

10.1.13   FM801 Blocks Power Down Control

- Host Offset Address: 0x70 - 0x71

- DSP I/O Address: N/A

- Power-on value: 0x0000

- Description: This register will power down the Hw blocks in FM801.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							0								

B15: Shutdown 24.576Mhz clock internally. 1=Shutdown, 0=Normal.

B14~B9: Reserved.

B8: PCI Clock can be turn off. 1=Ready, 0=Not ready to power down.

* B15, B8: read/write by host

10.2 FM801 GamePort Device Control Registers Summary Table

This section describes the summary and details of FM801 GamePort Control Registers.

Table 9 FM801 GamePort Device Control Registers Summary Table

Host Offset	Host R/W	Power-on Value	Description
0x00~01	R/W	-	Conventional Game Port
0x02~03	R	-	Game Port J1-X Counter
0x04~05	R	-	Game Port J1-Y Counter
0x06~07	R	-	Game Port J2-X Counter
0x08~09	R	-	Game Port J2-Y Counter
0x0D	R/W	0x68	Game Port Control
0x0E	R/W	0xDD	Interrupt Mask Control
0x0F	R/W	0x00	Interrupt Status/Clear

10.3 FM801 GamePort Device Control Registers Detailed Description

10.3.1 Conventional Game Port

- GamePort Host Offset Address: 0x00 – 0x01

- Power-on value: N/A

- Description: Game Port. Write any value to this port will reset the register value. This register is an alias of the legacy gameport register at 0x200~0x201.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

B8, B0: Joystick 1P X-axis.

B9, B1: Joystick 1P Y-axis.

B10, B2: Joystick 2P X-axis.

B11, B3: Joystick 2P Y-axis.

B12, B4: Joystick 1P Button A.

B13, B5: Joystick 1P Button B.

B14, B6: Joystick 2P Button A.

B15, B7: Joystick 2P Button B.

* B15~B8, B7~B0: read/write by Host

10.3.2 Game Port J1-X Counter

- GamePort Host Offset Address: 0x02 - 0x03

- Power-on value: N/A

- Description: Game Port Joystick 1P X-counter. Write any value to "Conventional game port"(0x00) will reset the register value.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	▨	-	-	-	-	-	-	-	-	-	-	-	-	-

B12~B0: Game Port Joystick 1P X-axis counter value.

B13: Reserved.

B14: Joystick 1P Button A.

B15: Joystick 1P Button B.

* B15~B14, B12~B0: read only by Host.

10.3.3 Game Port J1-Y Counter

- GamePort Host Offset Address: 0x04 - 0x05

- Power-on value: N/A

- Description: Game Port Joystick 1P Y-counter. Write any value to "Conventional game port"(0x00) will reset the register value.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
▨	▨	▨	-	-	-	-	-	-	-	-	-	-	-	-	-

B12~B0: Game Port Joystick 1P Y-axis counter value.

B15~B13: Reserved.

* B12~B0: read only by Host.

10.3.4 Game Port J2-X Counter

- GamePort Host Offset Address: 0x06 - 0x07

- Power-on value: N/A

- Description: Game Port Joystick 2P X-counter. Write any value to "Conventional game port"(0x00) will reset the register value.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	▨	-	-	-	-	-	-	-	-	-	-	-	-	-

B12~B0: Game Port Joystick 2P X-axis counter value.

B13: Reserved.

B14: Joystick 1P Button A.

B15: Joystick 1P Button B.

* B15~B14, B12~B0: read only by Host.

10.3.5 Game Port J2-Y Counter

- GamePort Host Offset Address: 0x08 - 0x09

- Power-on value: N/A

- Description: Game Port Joystick 2P Y-counter. Write any value to "Conventional game port"(0x00) will reset the register value.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
▨	▨	▨	-	-	-	-	-	-	-	-	-	-	-	-	-

B12~B0: Game Port Joystick 2P Y-axis counter value.

B15~B13: Reserved.

* B12~B0: read only by Host.

10.3.6 *Game Port Control*

- GamePort Host Offset Address: 0x0D

- Power-on value: 0x68

- Description: Game Port Control.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0	1	1	0	1	0	0	0

B1~B0: Game Port Movement Resolution. 00=9-bit, 01=8-bit, 10=7-bit, 11=6-bit.

B2: Intelligent Game Port Mode Enable. 1=On(Motion/push button auto detect), 0=Off.

B3: Game Port trigger PME Enable. 1=Enable, 0=Disable.

B4: Game Port Power Saving Mode. 1=On(No discharge after charging to 1), 0=Off.

B5: Game port Joystick 1 enable/disable. 1=Enable, 0=Disable.

B6: Game port Joystick 2 enable/disable. 1=Enable, 0=Disable.

B7: Game Port Sw reset. 1=Reset, 0=Normal.

*B7~B0: read/write by host.

10.3.7 *Interrupt Mask Control*

- Host Offset Address: 0x0E

- Power-on value: 0xDD

- Description: Interrupt Mask Control of the *FM801* Hardware. If it is set, it will mask the interrupt to the host.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								1	1		1	1	1		1

B0: Game port Interrupt Mask. 1= Mask(game port interrupt is disabled), 0=Non-Mask..

B7~B1: Reserved. (Initial value can not be changed)

* B6,B4~B2,B0: read/write by host. B7:read only by host.

10.3.8 Interrupt Status/Clear

- Host Offset Address: 0x0F

- Power-on value: 0x00

- Description: Interrupt will set this register corresponding bits. Write '1' will clear the interrupt, write '0' will have no effect.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	▨	0	0	0	▨	0								

B8: Game Port Interrupt.

B15~B9: Reserved.

* B15~B14, B12~B10, B8: read/write by Host.

11 PROTOCOL AND DATAFLOW

11.1 Codec(AC'972) access

11.1.1 Codec DAC and ADC data access

1. Codec IF will read the DAC data (left and right channels) from digital mixer @48Khz. If underrun happens, the same DAC data has to remain in the buffer of mixer for Codec IF to access.

2. Codec IF will write the ADC data (left and right channels) to the SRC @48Khz. When overrun occurs, new data will overwrite the old data.

11.1.2 Codec control register access

1. Host can access the Codec index registers through FM801 control register (0x2A~2D). For register write, Host has to poll bit-9 of Codec Command Port (0x2A~2B) first until it's ready. After making sure that Hw is ready to access Codec registers, host can program the data port (0x2C~2D) first, then it should issue 'write command' and the index address to register 0x2A to trigger the Hw to start programming Codec.

2. For register read from Codec, Host has to poll bit-9 of Codec Command Port (0x2A~2B) first until it's ready. Host is then allowed to issue the 'read command' and the address to register 0x2A . To read the data, Host starts polling bit-8 of it until it is set, then it can read the data from data port at 0x2C~2D.

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2 Please refer to Intel AC97 ver2.1 spec for details of the codec index registers map.

11.2 DirectSound Playback

1. Program Playback Buffer Length (Func-0 Ctrl Register, 0x0A~0x0B) and Playback Buffer Address 1 & 2 (Func-0 Ctrl Register, 0x0C~0x13) with proper value.

2. Set playback WAVE format by setting Stereo or Mono, 8-bit or 16-bit and the sampling rate at Playback Channel Control (Func-0 Ctrl Register, 0x08~09).

3. Fill buffer 1 and buffer 2 with playback data. Set bit-5 of Playback Channel Control (Func-0 Ctrl Register, 0x08~09) to '1' to start the PCI bus-master transfer for playback.

4. Playback current address can be read from Playback Channel Buffer Address (0x0C~0x0F or 0x10~0x13). Playback current remaining count can be read from Playback Channel Current Count Register(0x0A~0x0B) to determine where the Hw pointer is. Interrupt status will be generated when the current count reaches zero.

5. When the current count reaches zero, Hw will switch to buffer 2 starting address to transfer the data (ping-pong buffers scheme) and the current count will be re-loaded and start from data length again. In the meantime, driver has to start filling the data in the buffer 1.

6. To pause the playback, set bit-7 and bit-6 of Playback Channel Control (Func-0 Ctrl Register, 0x08~09) to '1'. To resume, just restore '0' to both of these 2 registers.

7. To stop/finish playback, set bit-7 of Playback Channel Control (Func-0 Ctrl Register, 0x08~09) to '1' and bit-5 to '0'.

11.3 DirectSound Recording

1. Program Capture Buffer Length (Func-0 Ctrl Register, 0x16~0x17) and Capture Buffer Address 1 & 2 (Func-0 Ctrl Register, 0x18~0x1F) with proper value.

2. Set Recording WAVE format by setting Stereo or Mono, 8-bit or 16-bit and the sampling rate at Capture Channel Control (Func-0 Ctrl Register, 0x14~15).

3. Set bit-5 of Capture Channel Control (Func-0 Ctrl Register, 0x14~15) to '1' to start the PCI bus-master transfer for Recording.

4. Capture current address can be read from Capture Channel Buffer Address (0x18~0x1B or 0x1C~0x1F). Capture current remaining count can be read from Capture Channel Current Count Register(0x16~0x17) to determine where the Hw pointer is. Interrupt status will be generated when the current count reaches zero.

5. When the current count reaches zero, Hw will switch to buffer 2 starting address to transfer the data (ping-pong buffers scheme) and the current count will be re-loaded and start from data length again. In the meantime, driver has to move the data in the buffer 1 to the system.

6. To pause the recording, set bit-7 and bit-6 of Capture Channel Control (Func-0 Ctrl Register, 0x14~15) to '1'. To resume, just restore '0' to both of these 2 registers.

7. To stop/finish Recording, set bit-7 of Capture Channel Control (Func-0 Ctrl Register, 0x14~15) to '1' and bit-5 to '0'.