HiNT
HB1-SE
PCI-PCI Bridge

Preliminary Specification
Rev 0.96
October 4, 2000

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Tel: (510)-623-0932 Fax: (510)-623-1803
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HB1-SE PCI-PCI Bridge

HiNT HB1-SE is a family of three 32-bit PCI-PCI bridges: HB1-SE33, HB1-SE33P and HB1-SE66. HB1-SE66 is capable of running at 66MHz PCI Bus and HB1-SE33 and HB1-SE33P runs at 33MHz. All parts are specially designed for applications that require high performance 32-bit PCI bus expansion. Add-in card designers can use HB1-SE to expand PCI connection capacity beyond the limitation of a single PCI device. Designers can use HB1-SE to build multi-device PCI cards such as RAID controllers and other multimedia applications.

Part numbers and Description:

Part Number	Description	Package Type
HB1-SE33	33Mhz, 32-bit PCI interface	160-pin Tiny BGA
HB1-SE33P	33Mhz, 32-bit PCI interface	160-pin PQFP
HB1-SE66	66Mhz, 32-bit PCI interface (AGP 2x port compatible)	160-pin Tiny BGA

- PCI Local Bus Specification Rev. 2.2 with VPD support
- HB1-SE66 is 66Mhz capable and HB1-SE33 runs at 33Mhz
- Synchronous primary and secondary PCI bus operation
- Compact PCI Hot Swap Friendly support with Ejector connection
- High performance, no retry penalty flow with uninterrupted 0 wait state burst up to 1K bytes
- Provides 4 Dwords buffering for posted write transactions and 4 Dwords for prefetchable read transactions each direction
- PCI Mobile Design Guide Rev. 1.1
- PC99 Power Management D3 Cold Wakeup capable
- Concurrent primary and secondary port operation supports traffic isolation
- Provides programmable arbitration support for 4 bus masters on secondary interface
- 5 Buffered secondary PCI clock outputs
- 4 GPIO pins
- Enhanced address decoding
  - Support 32-bit I/O address range
  - Support 64-bit memory- address range
  - ISA aware mode for legacy support in the first 64KB of I/O address range
  - VGA addressing and VGA palette snooping support
- Supports 3.3V PCI with 5V tolerant I/O

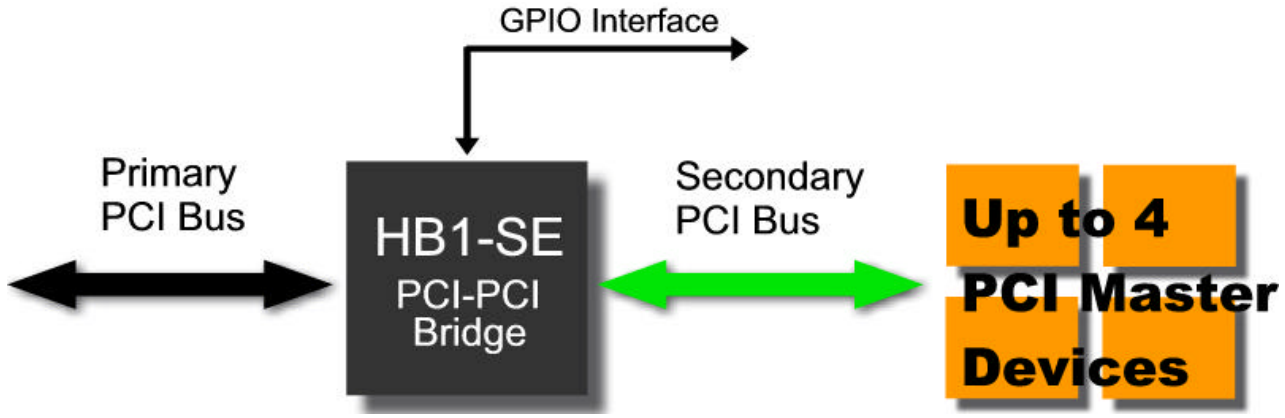

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Table of Contents

1 REGISTER INDEX 6

2 INTRODUCTION 7

3 ORDERING INFORMATION 7

4 PIN DIAGRAM 8

5 SIGNAL DEFINITION 9

5.1 PRIMARY BUS INTERFACE SIGNALS 9
5.2 SECONDARY BUS INTERFACE SIGNALS 11
5.3 CLOCK SIGNALS 12
5.4 RESET SIGNALS 12
5.5 HOT SWAP SIGNALS 13
5.6 MISCELLANEOUS SIGNALS 13
5.7 POWER SIGNALS 15

6 PIN ASSIGNMENT 16

6.1 HB1-SE PINOUT TABLES 17
6.1.1 Pin Assignment Sorted By Location 17
6.1.2 Pin Assignment Sorted by Signal Name 19

7 CONFIGURATION REGISTERS 21

7.1 CONFIGURATION SPACE MAP – TRANSPARENT MODE 21
7.2 CONFIGURATION REGISTER DESCRIPTION 22

8 PCI BUS OPERATION 42

8.1 TYPES OF TRANSACTIONS 42
8.2 ADDRESS PHASE 43
8.3 DEVICE SELECT (LDEV#) GENERATION 43
8.4 DATA PHASE 43
8.5 WRITE TRANSACTIONS 44
8.6 READ TRANSACTIONS 44
8.7 CONFIGURATION TRANSACTIONS 45
8.7.1 Type 0 Access to HB1-SE 45
8.7.2 Type 1 to Type 0 Translation 46
8.7.3 Type 1 to Type 1 Forwarding 48
8.7.4 Special Cycles 49
8.8 TRANSACTION TERMINATION 50
8.8.1 Master Termination Initiated by HB1-SE 50
8.8.2 Master Abort Received by HB1-SE 51
8.8.3 Target Termination Received by HB1-SE 51
8.8.4 Target Termination Initiated by HB1-SE 54

9 ADDRESS DECODING 56

9.1 ADDRESS RANGES 56

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9.2 I/O ADDRESS DECODING 56
9.2.1 I/O Base and Limit Address Registers 57
9.2.2 ISA Mode 58
9.3 MEMORY ADDRESS DECODING 58
9.3.1 Memory-Mapped I/O Base and Limit Address Registers 59

10 PCI BUS ARBITRATION 60

10.1 PRIMARY PCI BUS ARBITRATION 60
10.2 SECONDARY PCI BUS ARBITRATION 60

11 TRANSACTION DELAY 61

12 ERROR HANDLING 62

12.1 ADDRESS PARITY ERRORS 62
12.2 DATA PARITY ERRORS 63
12.2.1 Configuration Write Transactions to Configuration Space 63
12.2.2 Read Transactions 63
12.3 DATA PARITY ERROR REPORTING SUMMARY 64
12.4 SYSTEM ERROR (SERR#) REPORTING 67

13 RESET 68

13.1 PRIMARY INTERFACE RESET 68
13.2 SECONDARY INTERFACE RESET 68

14 BRIDGE BEHAVIOR 69

14.1 ABNORMAL TERMINATION (INITIATED BY BRIDGE MASTER) 70
14.1.1 Master Abort 70
14.1.2 PCI Master on Primary Bus 70
14.2 CONFIGURATION TYPE #1 TO TYPE #0 CONVERSION 70
14.3 CONFIGURATION TYPE #1 TO TYPE #1 BY-PASSING 71
14.4 TYPE-0 CONFIGURATION CYCLE FILTER MODE 71
14.5 DECODING 71
14.6 SECONDARY MASTER 72
14.7 PCI CLOCK RUN FEATURE 72

15 CLOCKS 73

15.1 PRIMARY AND SECONDARY CLOCK INPUTS 73
15.2 SECONDARY CLOCK OUTPUTS 73

16 66-MHZ OPERATION 74

17 MISCELLANEOUS OPTIONS 75

17.1 EEPROM INTERFACE 75
17.1.1 Auto mode EEPROM access 75
17.1.2 EEPROM mode at Reset: 75
17.1.3 EEPROM data structure: 75
17.1.4 EEPROM address and Corresponding HB1-SE Register 76
17.2 GENERAL PURPOSE I/O INTERFACE 77
17.3 VITAL PRODUCT DATA 77

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18 PCI POWER MANAGEMENT 78

19 HOT SWAP 79

19.1 HOTSWAP INSERTION 79
19.2 HOTSWAP EXTRACTION 79

20 PACKAGE SPECIFICATIONS 80

20.1 160-PIN TINY BGA 80
20.2 160-PIN STANDARD PQFP 82

21 ELECTRICAL SPECIFICATIONS 84

21.1 MAXIMUM RATINGS 84
21.2 FUNCTIONAL OPERATING RANGE 84
21.3 DC ELECTRICAL CHARACTERISTICS 85
21.4 PCI CLOCK SIGNAL AC PARAMETER MEASUREMENTS 86
21.4.1 33MHz PCI Clock Signal AC parameters 86
21.4.2 66MHz PCI Clock Signal AC parameters 87
21.5 PCI SIGNAL TIMING SPECIFICATION 87
21.5.1 33MHz PCI Signal Timing 88
21.5.2 66MHz PCI Signal Timing 88

APPENDIX A: HB1-SE33P PART DESCRIPTION 89

HB1-SE33P 160 PIN PINOUT 90
Pin Assignment Sorted by Location 90
Pin Assignment Sorted by Signal Name 93
HB1-SE33P/21152 PINOUT COMPARISON 95

APPENDIX B : SAMPLE SCHEMATICS 96

APPENDIX C: APPLICATION NOTES 102

HB1-SE66 APPLICATION NOTE 1: CONNECTING HB1-SE66 TO THE AGP INTERFACE 102
INTRODUCTION 102
TYPICAL APPLICATIONS 102
DESIGN CONSIDERATION 102

APPENDIX D: TIMING DIAGRAMS 103

FIGURE 1 : PRIMARY TO SECONDARY TYPE 1 TO TYPE 0 CONFIGURATION CYCLE CONVERSION. 103
FIGURE 2 : PRIMARY TO SECONDARY TYPE 1 TO TYPE 1 CONFIGURATION CYCLE PASSING. 104
FIGURE 3 : SECONDARY TO PRIMARY MEMORY READ LINE TRANSACTION. 105
FIGURE 4 : PRIMARY TO SECONDARY MEMORY READ TRANSACTION. 106
FIGURE 5 : SECONDARY TO PRIMARY MEMORY READ TRANSACTION. 107
FIGURE 6 : PRIMARY TO SECONDARY MEMORY WRITE TRANSACTION FOLLOWED BY SECONDARY TO PRIMARY MEMORY WRITE TRANSACTION. 108
FIGURE 7 : SECONDARY TO PRIMARY MEMORY WRITE TRANSACTION. 109

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1 Register Index

Arbiter Control Register 30
Bridge Control Register 28
Cache Line Size Register 24
Capability Identifier 32, 33, 34
Chip Control Register 29
Class Code Register 24
Clkrun Register 31
Data Register 33
Device ID Register 21
ECP Pointer 26
EEPROM Address 39
EEPROM Control 39
EEPROM Data 39
GPIO Control Register 38
HB1-SE Test Register 40
Header Type Register 24
Hot Swap Register 34
Hot Swap Switch 34
I/O Base Address Upper 16 Bits Register 26
I/O Base Register 24
I/O Limit Address Upper 16 Bits Register 26
I/O Limit Register 24
Internal Arbiter Control Register 37
Interrupt Pin Register 28
Memory Base Register 26
Memory Limit Register 26
Miscellaneous Control Register 36, 37
Next Item Pointer 32, 33, 34
PMCSR Bridge Support 33
Power Management Capabilities 32
Power Management Control/ Status 33
Prefetchable Memory Base Register 26
Prefetchable Memory Base Register Upper 32 Bits 26
Prefetchable Memory Limit Register 26
Prefetchable Memory Limit Register Upper 32 Bits 26
Primary Bus Number Register 24
Primary Command Register 21
Primary Latency Timer Register 24
Primary Status Register 23
Revision ID Register 24
Secondary Bus Number Register 24
Secondary Clock Control Register 30
Secondary Latency Timer 24
Secondary Status Register 25
Subordinate Bus Number Register 24
Subsystem ID 40
Subsystem Vendor ID 40
Vendor ID Register 21
VPD Data Register 35
VPD Register 35

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2 Introduction

This document describes the implementation and functionality of HiNT's 32-bit, 66/33MHz HB1-SE PCI-to-PCI Bridge chip. The specification includes required function and limitations.

HB1-SE has the following features:

- PCI Local Bus Specification Revision 2.2 features including VPD
- Support delayed transactions for PCI configuration, I/O and memory read commands
- Provides memory write data buffering in both directions
- Provides concurrent primary and secondary bus operation to isolate traffic
- Provides separate arbitration support for individual secondary port
  - Programmable 2-level arbiter
- Enhanced address decoding
  - 32-bit I/O and memory address decoding
- Supports PCI transaction forwarding for
  - Type 1 to Type 0 downstream only configuration commands
  - Type 1 to Type 1 configuration commands
  - Type 1 configuration write to special cycle
- Tristating of I/O during powerup and powerdown
- Supports 3.3V, 5V tolerant signaling

3 Ordering Information

The following parts are available:

Part Number	Description	Package Type
HB1-SE33	33Mhz, 32-bit PCI interface	160-pin Tiny BGA
HB1-SE33P *	33Mhz, 32-bit PCI interface	160-pin PQFP
HB1-SE66	66Mhz, 32-bit PCI interface (AGP 2x port compatible)	160-pin Tiny BGA

Mechanical specifications for each package type can be found in the appendix.
* Refer to Appendix A for detailed information about this part.

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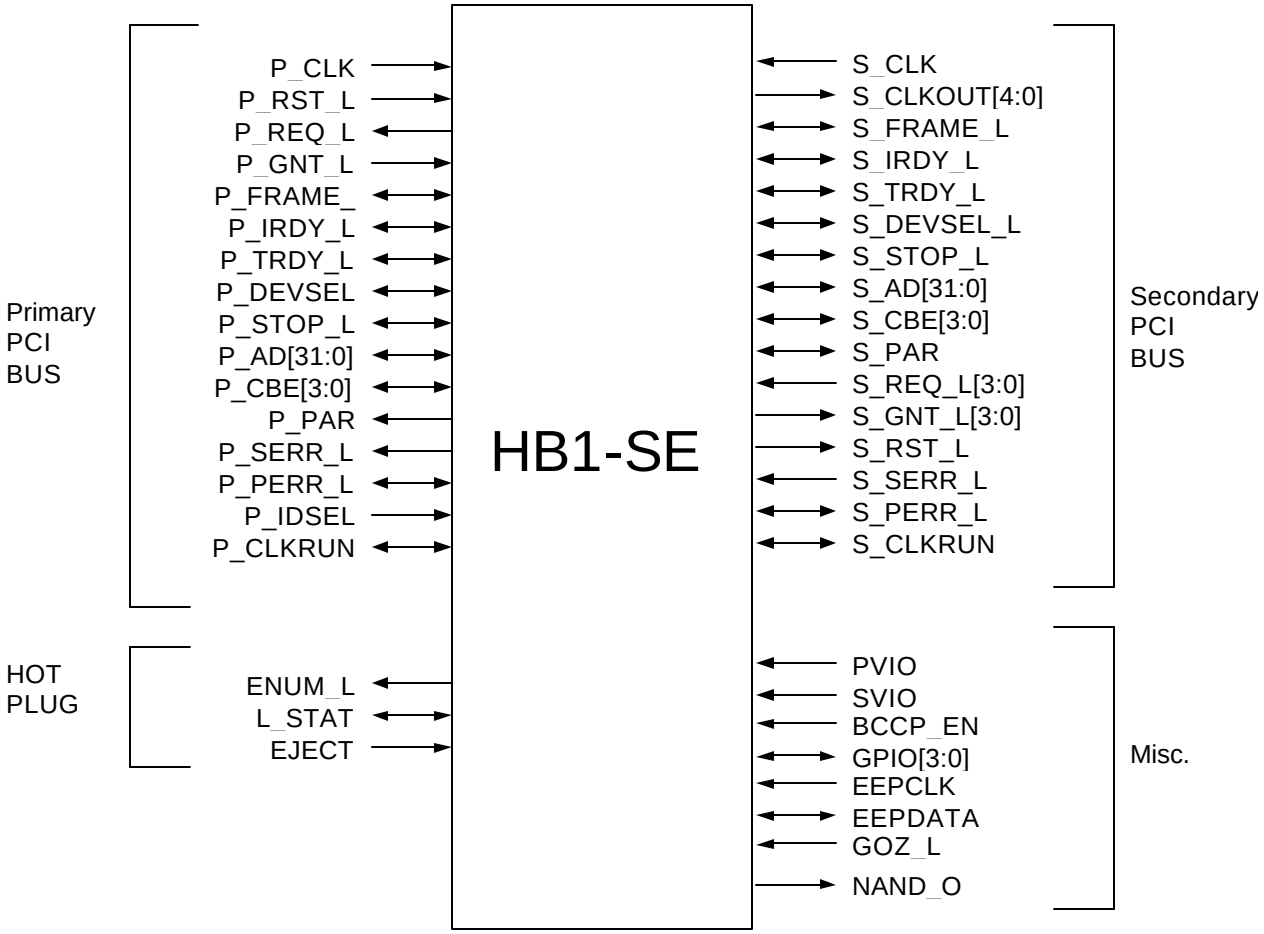
4 Pin Diagram



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5 Signal Definition

Signal Types

PI	PCI Input (5V tolerant, I/O VDD=3.3V)
PTS	PCI Tri-state bidirectional(5V tolerant, I/O VDD=3.3V)
PO	PCI Output
PSTS	PCI Sustained tristate Output. (Active LOW signal which must be driven inactive for one cycle before being tristated to ensure HIGH performance on a shared signal line)
OD	Output which either drives LOW (active state) or is tri-stated
I	CMOS Input
O	CMOS Output
IO	CMOS Bidirect

5.1 Primary Bus Interface Signals

Name	Type	Description
P_AD[31:0]	PTS	**Primary address/data:** Multiplexed address and data bus. Address is indicated by P_FRAME_L assertion. Write data is stable and valid when P_IRDY_L is asserted and read data is stable and valid when P_TRDY_L is asserted. Data is transferred on rising clock edges when both P_IRDY_L and P_TRDY_L are asserted. During bus idle, HB1-SE drives P_AD to a valid logic level when P_GNT_L is asserted.
P_CBE[3:0]	PTS	**Primary command/byte enables:** Multiplexed command field and byte enable field. During address phase, the initiator drives the transaction type on these pins. After that the initiator drives the byte enables during data phases. During bus idle, HB1-SE drives P_CBE[3:0] to a valid logic level when P_GNT_L is asserted.
P_PAR	PTS	**Primary Parity:** Parity is even across P_AD[31:0], P_CBE[3:0], and P_PAR (i.e. an even number of '1's). P_PAR is an input and is valid and stable one cycle after the address phase (indicated by assertion of P_FRAME_L) for address parity. For write data phases, P_PAR is an input and is valid one clock after P_IRDY_L is asserted. For read data phase, P_PAR is an output and is valid one clock after P_TRDY_L is asserted. Signal P_PAR is tristated one cycle after the PAD lines are tristated. During bus idle, HB1-SE drives PPAR to a valid logic level when P_GNT_L is asserted.
P_FRAME_L	PSTS	**Primary FRAME:** Driven by the initiator of a transaction to indicate the beginning and duration of an access. The deassertion of P_FRAME_L indicates the final data phase requested by the initiator. Before being tristated, it is driven to a deasserted state for one cycle.

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P_IRDY_L	PSTS	**Primary IRDY:** Driven by the initiator of a transaction to indicate its ability to complete the current data phase on the primary side. Once asserted in a data phase, it is not deasserted until end of the data phase. Before being tristated, it is driven to a deasserted state for one cycle.
P_TRDY_L	PSTS	**Primary TRDY:** Driven by the target of a transaction to indicate its ability to complete the current data phase on the primary side. Once asserted in a data phase, it is not deasserted until end of the data phase. Before being tristated, it is driven to a deasserted state for one cycle.
P_DEVSEL_L	PSTS	**Primary Device Select:** Asserted by the target indicating that the device is accepting the transaction. As a master, HB1-SE waits for the assertion of this signal within 5 cycles of P_FRAME_L assertion; otherwise, terminate with master abort. Before being tristated, it is driven to a deasserted state for one cycle.
P_STOP_L	PSTS	**Primary STOP:** Asserted by the target indicating that the target is requesting the initiator to stop the current transaction. Before being tristated, it is driven to a deasserted state for one cycle.
P_IDSEL	PI	**Primary ID Select.** Used as chip select line for Type 0 configuration access to HB1-SE configuration space.
P_PERR_L	PSTS	**Primary Parity Error:** Asserted when a data parity error is detected for data received on the primary interface. Before being tristated, it is driven to a deasserted state for one cycle.
P_SERR_L	OD	**Primary System Error:** Can be driven LOW by any device to indicate a system error condition, HB1-SE drives this pin on • Address parity error • Posted write data parity error on target bus • Secondary bus S_SERR_L asserted • Master abort during posted write transaction • Target abort during posted write transaction • Posted write transaction discarded • Delayed write request discarded • Delayed read request discarded • Delayed transaction master timeout This signal is pulled up through an external resistor.
P_REQ_L	PTS	**Primary Request:** This is asserted by HB1-SE to indicate that it wants to start a transaction on the primary bus. HB1-SE deasserts this pin for at least 2 PCI clock cycles before asserting it again.
P_GNT_L	PI	**Primary Grant:** When asserted, HB1-SE can access the primary bus. During idle and P_GNT_L asserted, HB1-SE will drive P_AD, P_CBE and P_PAR to valid logic level.

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5.2 Secondary Bus Interface Signals

Name	Type	Description
S_AD[31:0]	PTS	**Secondary Address/Data:** Multiplexed address and data bus. Address is indicated by S_FRAME_L assertion. Write data is stable and valid when S_IRDY_L is asserted and read data is stable and valid when S_TRDY_L is asserted. Data is transferred on rising clock edges when both S_IRDY_L and S_TRDY_L are asserted. During bus idle, HB1-SE drives S_AD to a valid logic level when the S_GNT_L is asserted
S_CBE[3:0]	PTS	**Secondary Command/Byte Enables:** Multiplexed command field and byte enable field. During the address phase, the initiator drives the transaction type on these pins. After that the initiator drives the byte enables during data phases. During bus idle, HB1-SE drives S_CBE[3:0] to a valid logic level when the internal grant is asserted.
S_PAR	PTS	**Secondary Parity:** Parity is even across S_AD[31:0], S_CBE[3:0], and S_PAR (i.e. an even number of '1's). S_PAR is an input and is valid and stable one cycle after the address phase (indicated by assertion of S_FRAME_L) for address parity. For write data phases, S_PAR is an input and is valid one clock after S_IRDY_L is asserted. For read data phase, S_PAR is an output and is valid one clock after S_TRDY_L is asserted. Signal S_PAR is tristated one cycle after the S_AD lines are tristated. During bus idle, HB1-SE drives S_PAR to a valid logic level when the internal grant is asserted.
S_FRAME_L	PSTS	**Secondary FRAME:** Driven by the initiator of a transaction to indicate the beginning and duration of an access. The deassertion of S_FRAME_L indicates the final data phase requested by the initiator. Before being tristated, it is driven to a deasserted state for one cycle
S_IRDY_L	PSTS	**Secondary IRDY:** Driven by the initiator of a transaction to indicate its ability to complete the current data phase on the primary side. Once asserted in a data phase, it is not deasserted until end of the data phase. Before being tristated, it is driven to a deasserted state for one cycle.
S_TRDY_L	PSTS	**Secondary TRDY:** Driven by the target of a transaction to indicate its ability to complete the current data phase on the primary side. Once asserted in a data phase, it is not deasserted until end of the data phase. Before being tristated, it is driven to a deasserted state for one cycle.
S_DEVSEL_L	PSTS	**Secondary Device Select:** Asserted by the target indicating that the device is accepting the transaction. As a master, HB1-SE waits for the assertion of this signal within 5 cycles of S_FRAME_L assertion; otherwise, terminate with master abort. Before being tristated, it is driven to a deasserted state for one cycle.
S_STOP_L	PSTS	**Secondary STOP:** Asserted by the target indicating that the target is requesting the initiator to stop the current transaction. Before being tristated, it is driven to a deasserted state for one cycle.

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S_PERR_L	PSTS	**Secondary Parity Error:** Asserted when a data parity error is detected for data received on the primary interface. Before being tristated, it is driven to a deasserted state for one cycle.
S_SERR_L	PI	**Secondary System Error:** Can be driven LOW by any device to indicate a system error condition.
S_REQ_L[3:0]	PI	**Secondary Requests:** This is asserted by external device to indicate that it wants to start a transaction on the Secondary bus. They are external pulled up through resistors to VDD.
S_GNT_L[3:0]	PO	**Secondary Grant:** HB1-SE asserts this pin to access the secondary bus. HB1-SE deasserts this pin for at least 2 PCI clock cycles before asserting it again. During idle and S_GNT_L asserted, HB1-SE will drive S_AD, S_CBE and S_PAR to valid logic levels.

5.3 Clock Signals

Name	Type	Description
P_CLK	I	**Primary CLK input:** Provides timing for all transaction on primary interface.
S_CLK	I	**Secondary CLK input:** Provides timing for all transaction on secondary interface.
S_CLKOUT[4:0]	O	**Secondary CLK output:** Provides secondary clocks phase synchronous with the P_CLK.

5.4 Reset Signals

Name	Type	Description
P_RST_L	I	**Primary Reset:** When P_RST_L is active, outputs and should be asynchronously tri-stated and P_SERR_L and P_GNT_L floated.
S_RST_L	PO	**Secondary Reset:** Asserted when any of the following conditions is met: 1. Signal P_RST_L is asserted. 2. The secondary reset bit in the bridge control register in configuration space is set. When asserted, all control signals are tri-stated and zeros are driven on S_AD, S_CBE and S_PAR.

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5.5 Hot Swap Signals

Name	Type	Description
ENUM_L	O	**Hot Swap Interrupt:** An open drain bussed signal to signal a change in status for the chip. Leave floating if not used.
EJECT	I	**Hot Swap Eject:** Indicates the status of software connection process. If pin is used to detect the insertion of hotswap devices. Pin should be tied to ground if not used.
L_STAT	IO	**Hot Swap LED:** Indicates the status of software connection process. Signal should be pulled down to ground if not used.

5.6 Miscellaneous Signals

Name	Type	Description
P_CLKRUN_L	I/OD	**Primary CLKRUN:** Used by the central resource to stop the PCI clock or to slow it down. If not used, this pin should be connected to ground to signify that PCLK is always running.
S_CLKRUN_L	I/O	**Secondary CLKRUN:** Drive high to stop or slow down secondary PCI clock, driven by secondary PCI device to keep clock running. If secondary PCI devices do not support CLKRUN#, this pin needs to be pulled low by a 300ohm resistor.
BPCC_EN	I	**Bus/power clock control management pin.** When signal is tied high and the HB1-SE is placed in the D3hot power state, the HB1-SE places the secondary bus in the B2 power state. The HB1-SE disables the secondary clocks and drives them to 0. When tied low, placing the HB1-SE in the D3hot power state has no effect on the secondary bus clocks.
GPIO[3:0]	PTS	**General Purpose Input Output pins.** These 4 general purpose signals are programmable as either input-only or bi-directional signals by writing the GPIO output enable control register
EEPCLK	O	**EEPROM Clock.** This pin is the clock signal to the EEPROM interface used during autoload and for VPD functions.
EEPDATA	I/O	**EEPROM Serial Data.** This pin is serial data interface to the EEPROM.
PVIO	I	**Primary Interface I/O Voltage** This signal must be tied to either 3.3V or 5V, depending on the signaling voltage of the primary interface.
SVIO	I	**Secondary Interface I/O Voltage** This signal must be tied to either 3.3V or 5V, depending on the signaling voltage of the secondray interface.
GOZ_L	I	**Diagnostic tristate control.** This signal, when asserted, tristates all bidirectional and tristatable output pins.
NAND_O	O	**Nand tree diagnostic output**. This signal is dedicated to the diagnostic Nand tree. The GOZ_L signal should be asserted when the Nand tree mechanism is used.

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5.7 Power Signals

Name	Type	Description
VDD		+3.3V
VSS		Ground

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6 Pin Assignment

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	BPCCE	SCBE1_L	SAD15	SAD13	SAD10	SCBE0_L	SAD5	SAD4	SAD1	PAD1	PAD3	PAD6	CBE0_L	PCLKRUN_L
B	SPAR	VSS	SCLKRUN_L	ENUM_L	SAD11	SAD8	SAD6	SAD3	SAD0	L_STAT	PAD4	PAD7	VSS	PAD8
C	SPERR_L	SSERR_L	VSS	SAD14	SAD12	SAD9	SAD7	SAD2	PAD0	PAD2	PAD5	VSS	PAD9	EJECT
D	STRDY_L	SLDEV_L	SSTOP_L	VSS	VSS	VDD	VDD	VDD	VDD	VSS	VSS	PAD10	PAD11	PAD12
E	EEPD	SFRAME_L	SIRDY_L	VSS							VSS	PAD13	PAD14	PAD15
F	SAD17	SAD16	SCBE2_L	VDD							VDD	PCBE1_L	PPAR	PSERR_L
G	SAD20	SAD19	SAD18	VDD							VDD	PPERR_L	EEPCLK	PSTOP_L
H	SAD21	SAD22	SAD23	VDD							VDD	PIRDY_L	PTRDY_L	PLDEV_L
J	SCBE3_L	SAD24	SAD25	VDD							VDD	PAD16	CBE2_L	PFRAME_L
K	SAD26	GPIO0	SAD27	VSS							VSS	PAD19	PAD18	PAD17
L	SAD28	SAD29	SAD30	VSS	VSS	VDD	VDD	VDD	VDD	VSS	VSS	PAD22	PAD21	PAD20
M	SAD31	SREQ0_L	VSS	SGNT2_L	SCLK	SCLK1	SCLK4	PCLK	PREQ_L	PAD29	PAD26	VSS	GPIO3	PAD23
N	SREQ1_L	VSS	SGNT0_L	SGNT3_L	SVIO	SCLK2	NAND_O	GPIO1	PGNT_L	PAD30	PAD27	PAD24	VSS	PIDSEL
P	SREQ2_L	SREQ3_L	SGNT1_L	SRST_L	SCLK0	SCLK3	GOZ_L	RST_L	PVIO	PAD31	PAD28	PAD25	GPIO2	CBE3_L

HB1-SE Top View

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6.1 HB1-SE pinout tables

6.1.1 Pin Assignment Sorted By Location

Location	Pin Name	Type
A01	BPCCE	I
A02	S_CBE_L[1]	TS
A03	S_AD[15]	TS
A04	S_AD[13]	TS
A05	S_AD[10]	TS
A06	S_CBE_L[0]	TS
A07	S_AD[05]	TS
A08	S_AD[04]	TS
A09	S_AD[01]	TS
A10	P_AD[01]	TS
A11	P_AD[03]	TS
A12	P_AD[06]	TS
A13	P_CBE_L[0]	TS
A14	P_CLKRUN_L	TS
B01	S_PAR	TS
B02	VSS	P
B03	S_CLKRUN_L	TS
B04	ENUM_L	TS
B05	S_AD[11]	TS
B06	S_AD[08]	TS
B07	S_AD[06]	TS
B08	S_AD[03]	TS
B09	S_AD[00]	TS
B10	L_STAT	TS
B11	P_AD[04]	TS
B12	P_AD[07]	TS
B13	VSS	P
B14	P_AD[08]	TS
C01	S_PERR_L	TS
C02	S_SERR_L	I
C03	VSS	P
C04	S_AD[14]	TS
C05	S_AD[12]	TS
C06	S_AD[09]	TS
C07	S_AD[07]	TS
C08	S_AD[02]	TS
C09	P_AD[00]	TS
C10	P_AD[02]	TS
C11	P_AD[05]	TS
C12	VSS	P
C13	P_AD[09]	TS
C14	EJECT	I
D01	S_TRDY_L	STS
D02	S_DEVSEL_L	STS
D03	S_STOP_L	STS
D04	VSS	P
D05	VSS	P
D06	VDD	P
D07	VDD	P
D08	VDD	P
D09	VDD	P
D10	VSS	P
D11	VSS	P
D12	P_AD[10]	TS
D13	P_AD[11]	TS
D14	P_AD[12]	TS
E01	EEPD	I/O
E02	S_FRAME_L	STS
E03	S_IRDY_L	STS
E04	VSS	P
E11	VSS	P
E12	P_AD[13]	TS
E13	P_AD[14]	TS
E14	P_AD[15]	TS
F01	S_AD[17]	TS
F02	S_AD[16]	TS
F03	S_CBE_L[2]	TS
F04	VDD	P
F11	VDD	P
F12	P_CBE_L[1]	TS
F13	P_PAR	TS
F14	P_SERR_L	OD
G01	S_AD[20]	TS
G02	S_AD[19]	TS
G03	S_AD[18]	TS
G04	VDD	P
G11	VDD	P
G12	P_PERR_L	STS
G13	EEPCLK	O
G14	P_STOP_L	STS
H01	S_AD[21]	TS

47923A Warm Springs Blvd., Fremont, CA 94539
Tel: (510)-623-0932 Fax: (510)-623-1803

H02	S_AD[22]	TS
H03	S_AD[23]	TS
H04	VDD	P
H11	VDD	P
H12	P_IRDY_L	STS
H13	P_TRDY_L	STS
H14	P_DEVSEL_L	STS
J01	S_CBE_L[3]	TS
J02	S_AD[24]	TS
J03	S_AD[25]	TS
J04	VDD	P
J11	VDD	P
J12	P_AD[16]	TS
J13	P_CBE_L[2]	STS
J14	P_FRAME_L	STS
K01	S_AD[26]	TS
K02	GPIO[0]	TS
K03	S_AD[27]	TS
K04	VSS	P
K11	VSS	P
K12	P_AD[19]	TS
K13	P_AD[18]	TS
K14	P_AD[17]	TS
L01	S_AD[28]	TS
L02	S_AD[29]	TS
L03	S_AD[30]	TS
L04	VSS	P
L05	VSS	P
L06	VDD	P
L07	VDD	P
L08	VDD	P
L09	VDD	P
L10	VSS	P
L11	VSS	P
L12	P_AD[22]	TS
L13	P_AD[21]	TS
L14	P_AD[20]	TS
M01	S_AD[31]	TS
M02	S_REQ_L[0]	I
M03	VSS	P

M04	S_GNT_L[2]	O
M05	S_CLK	I
M06	S_CLK_O[1]	O
M07	S_CLK_O[4]	O
M08	P_CLK	I
M09	P_REQ_L	O
M10	P_AD[29]	TS
M11	P_AD[26]	TS
M12	VSS	P
M13	GPIO[3]	I/O
M14	P_AD[23]	TS
N01	S_REQ_L[1]	I
N02	VSS	P
N03	S_GNT_L[0]	O
N04	S_GNT_L[3]	O
N05	S_VIO	I
N06	S_CLK_O[2]	O
N07	NAND_OUT	O
N08	GPIO[1]	I/O
N09	P_GNT_L	I
N10	P_AD[30]	TS
N11	P_AD[27]	TS
N12	P_AD[24]	TS
N13	VSS	P
N14	P_IDSEL	I
P01	S_REQ_L[2]	I
P02	S_REQ_L[3]	I
P03	S_GNT_L[1]	O
P04	S_RST_L	O
P05	S_CLK_O[0]	O
P06	S_CLK_O[3]	O
P07	GOZ_L	I
P08	RST_L	I
P09	P_VIO	I
P10	P_AD[31]	TS
P11	P_AD[28]	TS
P12	P_AD[25]	TS
P13	GPIO[2]	I/O
P14	P_CBE_L[3]	TS

47923A Warm Springs Blvd., Fremont, CA 94539
Tel: (510)-623-0932 Fax: (510)-623-1803

6.1.2 Pin Assignment Sorted by Signal Name

Location	Pin Name	Type
A01	BPCCE	I
G13	EEPCLK	O
E01	EEPD	I/O
C14	EJECT	I
B04	ENUM_L	TS
P07	GOZ_L	I
K02	GPIO[0]	TS
N08	GPIO[1]	I/O
P13	GPIO[2]	I/O
M13	GPIO[3]	I/O
B10	L_STAT	TS
N07	NAND_OUT	O
C09	P_AD[00]	TS
A10	P_AD[01]	TS
C10	P_AD[02]	TS
A11	P_AD[03]	TS
B11	P_AD[04]	TS
C11	P_AD[05]	TS
A12	P_AD[06]	TS
B12	P_AD[07]	TS
B14	P_AD[08]	TS
C13	P_AD[09]	TS
D12	P_AD[10]	TS
D13	P_AD[11]	TS
D14	P_AD[12]	TS
E12	P_AD[13]	TS
E13	P_AD[14]	TS
E14	P_AD[15]	TS
J12	P_AD[16]	TS
K14	P_AD[17]	TS
K13	P_AD[18]	TS
K12	P_AD[19]	TS
L14	P_AD[20]	TS
L13	P_AD[21]	TS
L12	P_AD[22]	TS
M14	P_AD[23]	TS
N12	P_AD[24]	TS
P12	P_AD[25]	TS
M11	P_AD[26]	TS
N11	P_AD[27]	TS
P11	P_AD[28]	TS
M10	P_AD[29]	TS
N10	P_AD[30]	TS
P10	P_AD[31]	TS
A13	P_CBE_L[0]	TS
F12	P_CBE_L[1]	TS
J13	P_CBE_L[2]	STS
P14	P_CBE_L[3]	TS
M08	P_CLK	I
A14	P_CLKRUN_L	TS
H14	P_DEVSEL_L	STS
J14	P_FRAME_L	STS
N09	P_GNT_L	I
N14	P_IDSEL	I
H12	P_IRDY_L	STS
F13	P_PAR	TS
G12	P_PERR_L	STS
M09	P_REQ_L	O
F14	P_SERR_L	OD
G14	P_STOP_L	STS
H13	P_TRDY_L	STS
P09	P_VIO	I
P08	RST_L	I
B09	S_AD[00]	TS
A09	S_AD[01]	TS
C08	S_AD[02]	TS
B08	S_AD[03]	TS
A08	S_AD[04]	TS
A07	S_AD[05]	TS
B07	S_AD[06]	TS
C07	S_AD[07]	TS
B06	S_AD[08]	TS
C06	S_AD[09]	TS
A05	S_AD[10]	TS
B05	S_AD[11]	TS
C05	S_AD[12]	TS
A04	S_AD[13]	TS
C04	S_AD[14]	TS
A03	S_AD[15]	TS
F02	S_AD[16]	TS
F01	S_AD[17]	TS
G03	S_AD[18]	TS
G02	S_AD[19]	TS
G01	S_AD[20]	TS
H01	S_AD[21]	TS
H02	S_AD[22]	TS
H03	S_AD[23]	TS
J02	S_AD[24]	TS
J03	S_AD[25]	TS
K01	S_AD[26]	TS
K03	S_AD[27]	TS

47923A Warm Springs Blvd., Fremont, CA 94539
Tel: (510)-623-0932 Fax: (510)-623-1803

L01	S_AD[28]	TS
L02	S_AD[29]	TS
L03	S_AD[30]	TS
M01	S_AD[31]	TS
A06	S_CBE_L[0]	TS
A02	S_CBE_L[1]	TS
F03	S_CBE_L[2]	TS
J01	S_CBE_L[3]	TS
M05	S_CLK	I
P05	S_CLK_O[0]	O
M06	S_CLK_O[1]	O
N06	S_CLK_O[2]	O
P06	S_CLK_O[3]	O
M07	S_CLK_O[4]	O
B03	S_CLKRUN_L	TS
D02	S_DEVSEL_L	STS
E02	S_FRAME_L	STS
N03	S_GNT_L[0]	O
P03	S_GNT_L[1]	O
M04	S_GNT_L[2]	O
N04	S_GNT_L[3]	O
E03	S_IRDY_L	STS
B01	S_PAR	TS
C01	S_PERR_L	TS
M02	S_REQ_L[0]	I
N01	S_REQ_L[1]	I
P01	S_REQ_L[2]	I
P02	S_REQ_L[3]	I
P04	S_RST_L	O
C02	S_SERR_L	I
D03	S_STOP_L	STS
D01	S_TRDY_L	STS
N05	S_VIO	I
D06	VDD	P
D07	VDD	P
D08	VDD	P
D09	VDD	P
F04	VDD	P
F11	VDD	P
G04	VDD	P
G11	VDD	P
H04	VDD	P
H11	VDD	P
J04	VDD	P
J11	VDD	P
L06	VDD	P
L07	VDD	P
L08	VDD	P
L09	VDD	P
B02	VSS	P
B13	VSS	P
C03	VSS	P
C12	VSS	P
D04	VSS	P
D05	VSS	P
D10	VSS	P
D11	VSS	P
E04	VSS	P
E11	VSS	P
K04	VSS	P
K11	VSS	P
L04	VSS	P
L05	VSS	P
L10	VSS	P
L11	VSS	P
M03	VSS	P
M12	VSS	P
N02	VSS	P
N13	VSS	P

47923A Warm Springs Blvd., Fremont, CA 94539
Tel: (510)-623-0932 Fax: (510)-623-1803

7 Configuration Registers

7.1 Configuration Space Map – Transparent Mode

31-24	23-16	15-8	7-0	Address
Device ID		**Vendor ID**		00h
Primary Status		**Primary Command**		04h
Class Code			**Revision ID**	08h
Reserved	**Header Type**	**Primary Latency Timer**	**Cache Line Size**	0Ch
Reserved				10h – 17h
Secondary Latency Timer	**Subordinate Bus Number**	**Secondary Bus Number**	**Primary Bus Number**	18h
Secondary Status		**I/O Limit**	**I/O Base**	1Ch
Memory Limit		**Memory Base**		20h
Prefetchable Memory Limit		**Prefetchable Memory Base**		24h
Prefetchable Memory Base Upper 32 Bits				28h
Prefetchable Memory Limit Upper 32 Bits				2Ch
I/O Limit Upper 16 Bits		**I/O Base Upper 16 Bits**		30h
Reserved			**ECP Pointer**	34h
Reserved				38h
Bridge Control		**Interrupt Pin**	**Interrupt Line**	3Ch
Arbiter Control		**Chip Control**		40h
Reserved				44h-67h
Reserved		**Secondary Clock Control**		68h
Clkrun	Reserved			
Reserved				
Power Management Capabilities		**Next Item Ptr = 90**	**Capability ID = 01**	80h
Data	**PMCSR Bridge Support**	**Power Management CSR**		84h
Reserved				88-8Fh
Reserved	**HSCSR = 00**	**Next Item Ptr = A0**	**Capability ID = 06**	90h
Reserved			**Hotswap switch**	94hh
Reserved				98h-9Fh

47923A Warm Springs Blvd., Fremont, CA 94539
Tel: (510)-623-0932 Fax: (510)-623-1803

VPD Register = 0000		**Next Item Ptr = 00**	**Capability ID = 03**	A0h
VPD Data Register = 0000_0000				A4h
Reserved				A8h-BFh
Arbiter Control	Reserved	**Miscellaneous Control**	Reserved	C0h
Reserved	**GPIO Control**		**Miscellaneous Control**	C4h
EEPROM Data		**EEPROM Address**	**EEPROM control**	C8h
Test Register			Reserved	CCh
Reserved				D0h-EFh
Subsystem ID		**Subsystem Vendor ID**		F0h
Reserved				F4h-FFh

7.2 Configuration Register Description

Vendor ID Register (Read Only) - Offset 0h

Defaults to 3388(h).

Device ID Register (Read Only) - Offset 2h

Defaults to 0021(h).

(Note: R/W - Read/Write, R/O - Read Only, R/WC - Read/ Write 1 to clear)

Primary Command Register (Read/Write) - Offset 4h

Bit	Function	Type	Description
0	I/O Space Enable	R/W	Controls the bridge's response to I/O accesses on the primary interface. **0=ignore I/O transaction** 1=enable response to I/O transaction Reset to 0.
1	Memory Space Enable	R/W	Controls the bridge's response to memory accesses on the primary interface. **0=ignore all memory transaction** 1=enable response to memory transaction Reset to 0.

47923A Warm Springs Blvd., Fremont, CA 94539
Tel: (510)-623-0932 Fax: (510)-623-1803

2	Bus Master Enable	R/W	Controls the bridge's ability to operate as a master on the primary interface. **0=do not initiate transaction on the primary interface and disable response to memory or I/O transactions on secondary interface** 1=enable the bridge to operate as a master on the primary interface Reset to 0.
3	Special Cycle Enable	R/O	No special cycle implementation (**set to '0'**).
4	Memory Write and Invalidate Enable	R/O	Memory write and invalidate not supported (**set to '0'**).
5	VGA Palette Snoop Enable	R/W	Controls the bridge's response to VGA compatible palette accesses. **0=ignore VGA palette accesses on the primary interface** 1=enable response to VGA palette writes on the primary interface (I/O address AD[9:0]=3C6h, 3C8h and 3C9h) Reset to 0.
6	Parity Error Enable	R/W	Controls the bridge's response to parity errors. **0=ignore any parity errors** 1=normal parity checking performed Reset to 0.
7	Wait Cycle Control	R/O	HB1-SE performs address / data stepping (**set to '1'**).
8	P_SERR_L Enable	R/W	Controls the enable for the P_SERR_L pin. **0=disable the P_SERR_L driver** 1=enable the P_SERR_L driver Reset to 0.
9	Fast Back to Back Enable	R/W	Controls the bridge's ability to generate fast back-to-back transactions to **different** devices on the primary interface. **0=no fast back to back transaction** 1=enable fast back to back transaction Reset to 0.
10-15	Reserved	R/O	Reserved. Reset to 0.

47923A Warm Springs Blvd., Fremont, CA 94539
Tel: (510)-623-0932 Fax: (510)-623-1803

Primary Status Register(Read/Write) – Offset 6h

Bit	Function	Type	Description
0-3	Reserved	R/O	Reserved (**set to '0's**).
4	ECP	R/O	Enhanced Capabilities port. Reads as 1 to indicate HB1-SE supports an enhanced capabilities list.
5	66MHz	R/O	66Mhz Capable : Indicates if primary interface can run at 66Mhz This bit is set to '0' for HB1-SE33 and set to '1' for HB1-SE66.
6	UDF	R/O	No User-Definable Features (**set to '0'**).
7	Fast Back to Back Capable	R/O	Fast back-to-back write capable on primary side (**set to '1'**).
8	Data Parity Error Detected	R/WC	It is set when the following conditions are met: 1. P_PERR_L is asserted 2. Bit 6 of Command Register is set Reset to 0.
9-10	DEVSEL timing	R/O	DEVSEL_L timing (**default to '01')** to indicate medium timing .
11	Signaled Target Abort	R/WC	Should be set (by a target device) whenever a Target Abort cycle occurs. Reset to 0.
12	Received Target Abort	R/WC	Set to '1' (by a master device) when transactions are terminated with Target Abort. Reset to 0.
13	Received Master Abort	R/WC	Set to '1' (by a master) when transactions are terminated with Master Abort. Reset to 0.
14	Signaled System Error	R/WC	Should be set whenever P_SERR_L is asserted. Reset to 0.
15	Detected Parity Error	R/WC	Should be set whenever a parity error is detected regardless of the state of the bit 6 of command register. Reset to 0.

47923A Warm Springs Blvd., Fremont, CA 94539
Tel: (510)-623-0932 Fax: (510)-623-1803

Revision ID Register (Read Only) – Offset 8h
Defaults to 12h.

Class Code Register (Read Only) – Offset 9h
Defaults to 060400h.

Cache Line Size Register (Read/Write) – Offset 0Ch
This register is used when terminating memory write and invalidate transactions and when prefetching.

Only cache line sizes (in units of 32-bits words) which are power of two are valid (only one bit can be set in this register). Reset to 0.

Primary Latency Timer Register (Read/Write) – Offset 0Dh
This register sets the value for Master Latency Timer which starts counting when the master asserts FRAME_L. Reset to 0.

Header Type Register (Read Only) – Offset 0Eh
Hardwired to 01h.

Primary Bus Number Register (Read/Write) – Offset 18h
Programmed with the number of the PCI bus to which the primary bridge interface is connected. This value is set with configuration software. Reset to 0.

Secondary Bus Number Register (Read/Write) – Offset 19h
Programmed with the number of the PCI bus to which the secondary bridge interface is connected. This value is set with configuration software. Reset to 0.

Subordinate Bus Number Register (Read/Write) –Offset 1Ah
Programmed with the number of the PCI bus with the highest number that is subordinate to the bridge. This value is set with configuration software. Reset to 0.

Secondary Latency Timer (Read/Write) – Offset 1Bh
This register is programmed in units of PCI bus clocks. Reset to 0. The latency timer checks for master accesses on the secondary side that remain unclaimed by any target.

I/O Base Register (Read/Write) – Offset 1Ch
This register defines the bottom address of the I/O address range for the bridge. The upper four bits define the bottom address range used by the chip to determine when to forward I/O transactions from one interface to the other. These 4 bits correspond to address bits <15:12> and are writeable. The upper 16 bits corresponding to address bits <31:16> are defined in the I/O base address upper 16 bits register. The address bits <11:0> are assumed to be 000h. The lower four bits (3:0) of this register set to '0001' (read-only) to indicate 32-bit I/O addressing. Reset to 0.

I/O Limit Register (Read/Write) – Offset 1Dh
This register defines the top address of the I/O address range for the bridge. The upper four bits define the top address range used by the chip to determine when to forward I/O transactions from one interface to the other. These 4 bits correspond to address bits <15:12> and are writeable. The upper 16 bits corresponding to address bits <31:16> are defined in the I/O limit address upper 16 bits register. The address bits <11:0> are assumed to be FFFh. The lower four bits (3:0) of this register set to '0001' (read-only) to indicate 32-bit I/O addressing. Reset to 0.

47923A Warm Springs Blvd., Fremont, CA 94539
Tel: (510)-623-0932 Fax: (510)-623-1803

Secondary Status Register (Read/Write) – Offset 1Eh

Bit	Function	Type	Description
0-4	reserved	R/O	Reserved (**set to '0's**).
5	66MHz	R/O	66Mhz Capable : Indicates if primary interface can run at 66Mhz This bit is set to '0' for HB1-SE33 and set to '1' for HB1-SE66.
6	UDF	R/O	No User-Definable Features (**set to '0'**).
7	Fast Back to Back Capable	R/O	Fast back-to-back write capable on secondary port (**set to '1'**).
8	Data Parity Error Detected	R/WC	It is set when the following conditions are met: 1. SPERR_L is asserted 2. Bit 6 of Command Register is set Reset to 0.
9-10	DEVSEL timing	R/O	Medium DEVSEL_L timing (**set to '01'**)
11	Signaled Target Abort	R/WC	Should be set (by a target device) whenever a Target Abort cycle occurs. Should be '0' after reset. Reset to 0.
12	Received Target Abort	R/WC	Set to '1' (by a master device) when transactions are terminated with Target Abort. Reset to 0.
13	Received Master Abort	R/WC	Set to '1' (by a master) when transactions are terminated with Master Abort. Reset to 0.
14	Received System Error	R/WC	Should be set whenever SSERR_L is detected. Should be a '0 after reset. Reset to 0.
15	Detected Parity Error	R/WC	Should be set whenever a parity error is detected regardless of the state of the bit 6 of command register. Reset to 0.

47923A Warm Springs Blvd., Fremont, CA 94539
Tel: (510)-623-0932 Fax: (510)-623-1803

Memory Base Register (Read/Write) – Offset 20h

This register defines the base address of the memory-mapped address range for forwarding the cycle through the bridge. The upper twelve bits corresponding to address bits <31:20> are writeable. The lower 20 address bits (19:0) are assumed to be 00000h. The 12 bits are reset to 0. The lower 4 bits are read only and set to 0.

Memory Limit Register (Read/Write) – Offset 22h

This register defines the upper limit address of the memory-mapped address range for forwarding the cycle through the bridge. The upper twelve bits corresponding to address bits <31:20> are writeable. The 12 bits are reset to 0. The lower 4 bits are read only and are set to 0. The lower 20 address bits (19:0) are assumed to be FFFFFh. Reset to 0.

Prefetchable Memory Base Register (Read/Write) - Offset 24h

This register defines the base address of the prefetchable memory-mapped address range for forwarding the cycle through the bridge. The upper twelve bits corresponding to address bits <31:20> are writeable. The 12 bits are reset to 0. The lower 4 bits are read only and are set to 0. The lower 20 address bits (19:0) are assumed to be 00000h. Reset to 0.

Prefetchable Memory Limit Register (Read/Write) – Offset 26h

This register defines the upper limit address of the memory-mapped address range for forwarding the cycle through the bridge. The upper twelve bits correspond to address bits <31:20> are writeable. The 12 bits are reset to 0. The lower 4 bits are read only and are set to 0. The lower 20 address bits (19:0) are assumed to be FFFFFh. Reset to 0.

Prefetchable Memory Base Register Upper 32 Bits (Read/Write) – Offset 28h

This register defines the base address of the prefetchable memory-mapped address range for forwarding the cycle through the bridge. The upper twelve bits corresponding to address bits <31:20> are writeable. The 12 bits are reset to 0. The lower 4 bits are read only and are set to 0. The lower 20 address bits (19:0) are assumed to be 00000h. Reset to 0.

Prefetchable Memory Limit Register Upper 32 Bits (Read/Write) – Offset 2Ch

This register defines the upper limit address of the memory-mapped address range for forwarding the cycle through the bridge. The upper twelve bits correspond to address bits <31:20> are writeable. The 12 bits are reset to 0. The lower 4 bits are read only and are set to 0. The lower 20 address bits (19:0) are assumed to be FFFFFh. Reset to 0.

I/O Base Address Upper 16 Bits Register (Read/Write) – Offset 30h

This register defines the upper 16 bits of a 32-bit base I/O address range used for forwarding the cycle through the bridge. Reset to 0.

I/O Limit Address Upper 16 Bits Register (Read/Write) – Offset 32h

This register defines the upper 16 bits of a 32-bit limit I/O address range used for forwarding the cycle through the bridge. Reset to 0.

ECP Pointer (Read/Only) – Offset 34h

Bit	Function	Type	Description
7-0	ECP Pointer	R/O	Enhanced capabilities port offset pointer. This register reads as 80h to indicate the offset of the power management registers.

47923A Warm Springs Blvd., Fremont, CA 94539
Tel: (510)-623-0932 Fax: (510)-623-1803

Interrupt Pin Register (Read Only) – Offset 3Dh

Reads as 0 to indicate that HB1-SE does not use any interrupt pin.

Bridge Control Register (Read/Write) – Offset 3Eh

Bit	Function	Type	Description
0	Parity Error Response Enable	R/W	Controls the bridge's response to parity errors on the secondary interface. **0=ignore address and data parity errors on the secondary interface** 1=enable parity error reporting and detection on the secondary interface Reset to 0.
1	S_SERR_L Enable	R/W	Controls the forwarding of S_SERR_L to the primary interface. **0=disable the forwarding S_SERR_L to primary** 1=enable the forwarding of S_SERR_L to primary Reset to 0.
2	ISA Enable	R/W	Controls the bridge's response to ISA I/O addresses, which is limited to the first 64K. **0=forward all I/O addresses in the range defined by the I/O Base and I/O Limit registers** 1=block forwarding of ISA I/O addresses in the range defined by the I/O Base and I/O Limit registers that are in the first 64K of I/O space that address the last 768 bytes in each 1Kbytes block. Secondary I/O transactions are forwarded upstream if the address falls within the last 768 bytes in each 1Kbytes block Reset to 0.
3	VGA Enable	R/W	Controls the bridge's response to VGA compatible addresses. **0=do not forward VGA compatible memory and I/O addresses from primary to secondary** 1=forward VGA compatible memory and I/O address from primary to secondary regardless of other settings Reset to 0.
4	reserved	R/O	Reserved (**set to 0**).

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5	Master Abort Mode	R/W	Controls the bridge behavior in responding to master aborts on secondary interface **0=do not report master aborts (return ffff_ffffh on reads and discards data on writes)** 1=report master aborts by signaling target abort if possible by the assertion of P_SERR_L if enabled Reset to 0. Note: During lock cycles, HB1-SE ignores this bit, and always completes the cycle as a target abort.
6	Secondary Interface Reset	R/W	Forces the assertion of SRST_L signal pin on the secondary interface. **0=do not force the assertion of SRST_L pin** 1=force the assertion of SRST_L pin Reset to 0.
7	Fast Back to Back Enable	R/W	Controls the bridge's ability to generate fast back-to-back transactions to **different** devices on the secondary interface. **0=no fast back to back transaction** 1=enable fast back to back transaction Reset to 0.
8-11	Reserved	R/W	Can be used as a software register
15-12	reserved	R/O	Reserved (**set to '0's**).

Chip Control Register (Read/Write) – Offset 40h

Bit	Function	Type	Description
3-0	Reserved	R/O	Reserved**(Set to 0)**
4	Secondary bus prefetch disable	R/W	Controls HB1-SE's ability to prefetch during upstream memory read transactions. When 0 the chip prefetches and does not forward byte enable bits during memory read transactions. When 1, HB1-SE requests only one Dword from the target during memory read transactions and forwards read enable bits. HB1-SE returns a target disconnect to the requesting master on the first data transfer. Memory read line and memory read multiple transactions are still prefetchable. Reset to 0.
7-6	Reserved	R/O	Reserved

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Arbiter Control Register (Read/Write) – Offset 42h

Bit	Function	Type	Description
3-0	Arbiter Control	R/W	Each bit controls whether a secondary bus master is assigned to the high priority group or the low priority group. Bits [3:0] correspond to request inputs S_REQ_L[3:0], respectively. Reset value is 0.
6-4	Reserved	R/O	Reserved
8-7	Reserved	R/W	Can be used as software register
9	HB1-SE priority	R/W	Defines whether the secondary port of HB1-SE is in high priority group or the low priority group 0=low priority group **1=high priority group.** Reset to 1.
15:10	Reserved	R/O	Reserved **(set to '0's)**

Secondary Clock Control Register (Read/Write) – Offset 68h

Bit	Function	Type	Description
1:0	Clock 0 Disable	R/W	If either bit is 0, S_CLKOUT[0] is enabled. When both bits are 1, S_CLKOUT[0] is disabled.
3:2	Clock 1 Disable	R/W	If either bit is 0, S_CLKO[1] is enabled. When both bits are 1, S_CLKO[1] is disabled.
5:4	Clock 2 Disable	R/W	If either bit is 0, S_CLKO[2] is enabled. When both bits are 1, S_CLKO[2] is disabled.
7:6	Clock 3 Disable	R/W	If either bit is 0, S_CLKO[3] is enabled. When both bits are 1, S_CLKO[3] is disabled.
8	Clock 4 Disable	R/W	If 0, S_CLKO[3] is enabled. Otherwise, it is disabled.
15:9	Reserved	R/O	Reserved

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Clkrun Register (Read/Write) – Offset 6Fh

Bit	Function	Type	Description
0	Secondary Clock Stop Status	R/O	Secondary clock stop status 0 = Secondary clock not stopped 1 = Secondary clock stopped Defaults to 0
1	Secondary Clkrun Enable	R/W	Secondary clkrun protocol enable 0 = disable 1 = enable Defaults to 0
2	Primary Clock Stop	R/W	Primary clock stop 0 = allow primary clock to stop if secondary clock is stopped 1 = always keep primary clock running Defaults to 0
3	Primary Clkrun Enable	R/W	Primary clkrun protocol enable 0 = disable 1 = enable Defaults to 0
4	Clkrun Mode	R/W	Clkrun mode 0 = Stop the secondary clock only on request from the primary bus 1 = Stop the secondary clock whenever the secondary bus is idle and there are no requests from the primary bus. Defaults to 0

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Hot Swap and Power Management Registers

Capability Identifier (R/O) - Offset 80h

This register is set to 01h to indicate power management interface registers.

Next Item Pointer (R/O) – Offset 81h

Set to 90h. This field provides an offset into the function's PCI Configuration Space pointing to the location of next item in the function's capability list. In HB1-SE, this points to the hot swap registers.

Power Management Capabilities(R/O) – Offset 82h

Bit	Function	Type	Description
0-2	Version	R/O	This register is set to 001b, indicating that this function complies with Rev 1.0 of the PCI Power Management Interface Specification
3	PME Clock	R/O	This bit is a '0', indicating that HB1-SE does not support PME# signaling.
4	Auxiliary Power Source	R/O	This bit is set to ‘0’ since HB1-SE does not support PME# signaling
5	DSI	R/O	Device Specific Initialization . Returns ‘0’ indicating that HB1-SE does not need special initialization
6-8	Reserved	R/O	Reserved
9	D1 Support	R/O	Returns ‘1’ indicating that HB1-SE supports the D1 device power state
10	D2 Support	R/O	Returns ‘1’ indicating that HB1-SE supports the D2 device power state
11-15	PME Support	R/O	Set to ‘00000b’ indicating that PME# is not supported

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Power Management Control/ Status(R/W) – Offset 84h

Bit	Function	Type	Description
0-1	Power State	R/W	This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. The definition of the field values is given below. 00b - D0 01b - D1 : valid only if D1 capable bit is 1 10b - D2 : valid only if D2 capable bit is 1 11b - D3hot : if BCPPE is 1, SCLK output will be stopped
2-7	Reserved	R/O	Reserved
8	PME Enable	R/O	This bit is set to '0' since HB1-SE does not support PME# signaling
9-12	Data Select	R/W	This 4-bit field is used to select which data is to be reported through the Data registers and Data Scale field
13-14	Data Scale	R/O	This 2-bit field indicates the scaling factor to be used when interpreting the value of the Data register. The value and meaning of this field will vary depending on which data value has been selected by the Data Select field
15	PME Status	R/O	This bit is set to '0' since HB1-SE does not support PME# signaling

PMCSR Bridge Support(R/W) – Offset 86h

Bit	Function	Type	Description
0-5	Reserved	R/O	Reserved
6	B2/B3 Support for D3hot	R/O	This bit returns a '1' when read indicating that when HB1-SE is programmed to D3hot state the secondary bus's clock is stopped.
7	Bus Power Control Enable	R/O	Returns '1' indicating that the power management state of the secondary bus follows that of HB1-SE with one exception , D3hot state.

Data Register (R/W) – Offset 87h

Bit	Function	Type	Description
0-7	Data Register	R/O	This register is used to report the state dependent data requested by the Data Select field. The value of this register is scaled by the value reported by the Data Scale field. This register is EEPROM loadable

Capability Identifier (R/O) - Offset 90h

This register is set to 06h to indicate Hotswap interface registers.

Next Item Pointer (R/O) - Offset 91h

Set to A0h. This field provides an offset into the function's PCI Configuration Space pointing to the location of next item in the function's capability list. In HB1-SE, this points to the Vital Product Data (VPD) registers.

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Hot Swap Register(R/W) – Offset 92h

Bit	Function	Type	Description
0	Reserved	R/O	Reserved
1	ENUM# Mask Status	R/W	Enables or disables ENUM# assertion 0 = enable ENUM# signal 1 = mask off ENUM# signal
2	Reserved	R/O	Reserved
3	LED status	R/W	Indicates if LED is on or off. Writing a '1' to this bit drives the LSTAT signal high. Writing a '0' drives the pin low. 0 = LED is off 1 = LED is on
4-5	Reserved	R/O	Reserved
6	Extraction State	W1TC	Indicates assertion of ENUM# due to the device being extracted. Writing a '1' to this bit clears the status. 0 = ENUM# is set to '1' 1 = ENUM# is asserted low
7	Insertion State	W1TC	Indicates assertion of ENUM# due to the device being inserted. Writing a '1' to thisbit clears the status 0 = ENUM# is set to '1' 1 = ENUM# is asserted low

Hot Swap Switch (R/W) – Offset 94h

Bit	Function	Type	Description
0	**Hotswap extraction switch**	R/O	**Hotswap extraction switch :** Software switch used to signal extraction of board. If set, board is in inserted state. Writing a '0' to this bit will signal the pending extraction of the board.
1-7	**Reserved**	R/O	**Reserved**

Capability Identifier (R/O) - Offset A0h

This register is set to 03h to indicate VPD registers.

Next Item Pointer (R/O) - Offset A1h

Set to 00h. End of Capability list.

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VPD Register (R/W) – Offset A2h

Bit	Function	Type	Description
1-0	**Reserved**	R/O	**Reserved**
7-2	**VPD Address**	R/W	**VPD Address: Contains Dword address that will be used when generating a read or write cycle to the VPD table.**
14-8	**Reserved**	R/O	**Reserved**
15	**VPD Operation**	R/W	**VPD operation:** Writing a '0' to this bit generates a read cycle from the EEPROM at the VPD address specified in bits 7-2 of this register. This bit will remain at a logic '0' value until EEPROM cycle is finished, then it be set to '1'. Data for reads is available at register 9ch Writing a '1' to this bit generates a write cycle to the EEPROM at the VPD address specified in bits 7-2 of this register. This bit will remain at a logic '1' value until EEPROM cycle is finished, then it be cleared to '0'.

VPD Data Register (R/W) – Offset A4h

Bit	Function	Type	Description
31-0	**VPD Data**	R/W	**VPD Data** (EEPROM data[addr + 0x40]) - The least significant byte of this register corresponds to the byte of VPD at the address specified by the VPD Address register. The data read from or written to this register uses the normal PCI byte transfer capabilities. Reads to this register will return the last data read from or written to the EEPROM.

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Miscellaneous Control Register (R/W) – Offset C1h

Bit	Function	Type	Description
0	ISA IO	R/W	This bit enables several I/O addresses to be located behind HB1-SE. If set, the following I/O addresses belong to the secondary bus. • 0207h – 0200h : Game port • 038bh – 0388h : FM • 0233h – 0220h: Audio • 0331h – 0330h: MIDI
1	Memory Read Line control	R/W	If 1, HB1-SE will always stop prefetch on cacheline boundaries on memory read line transactions.
2	Read BE control	R/W	If 1, HB1-SE will force all byte enables to be active during read burst cycles.
3	Reserved	R/O	Reserved
4	Low priority group fixed arbitration	R/W	If 1, the low priority group uses the fixed priority arbitration scheme, otherwise a rotating priority arbitration scheme is used
5	Low priority group arbitration order	R/W	This bit is only valid when the low priority arbitration group is set to a fixed arbitration scheme. If 1, priority decreases in ascending numbers of the master, for example master #4 will have higher priority than master #3. If 0, the reverse is true. This order is relative to the master with the highest priority for this group, as specified in bits 7-4 of this register.
6	High priority group fixed arbitration	R/W	If 1, the high priority group uses the fixed priority arbitration scheme, otherwise a rotating priority arbitration scheme is used
7	High priority group arbitration order	R/W	This bit is only valid when the high priority arbitration group is set to a fixed arbitration scheme. If 1, priority decreases in ascending numbers of the master, for example master #4 will have higher priority than master #3. If 0, the reverse is true. This order is relative to the master with the highest priority for this group, as specified in bits 11-8 of this register.

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Internal Arbiter Control Register - Offset C3h

Bit	Function	Type	Description
0-3	Highest priority master in low priority group	R/W	Controls which master in the low priority group has the highest priority. It is valid only if the group uses the fixed arbitration scheme. 0000 : master#0 has highest priority 0001 : … 1001 : HB1-SE has highest priority 1010-1111 : Reserved
4-7	Highest priority master in high priority group	R/W	Controls which master in the high priority group has the highest priority. It is valid only if the group uses the fixed arbitration scheme. 0000 : master#0 has highest priority 0001 : … 1001 : HB1-SE has highest priority 1010-1111 : Reserved

Miscellaneous Control Register (R/W) – Offset C4h

Bit	Function	Type	Description
0-2	Reserved	R/O	Reserved
3	SGNT_L deassertion	R/W	If 1, HB1-SE will deassert SGNT_L 1 clock after PGNT_L is deasserted, else, SGNT_L is deasserted at the same time as PGNT_L. This bit defaults to 1
4	Secondary to Primary transaction delay	R/W	Specify delay for transactions going from secondary to primary PCI interface 0 = delay Secondary bus to Primary bus transfer by 1 PCLK 1 = delay Secondary bus to Primary bus transfer by 2 PCLKs
5	Primary to Secondary transaction delay	R/W	Specify delay for transactions going from primary to secondary PCI interface 0 = delay Primary bus to Secondary bus transfer by 1 PCLK 1 = delay Primary bus to Secondary bus transfer by 2 PCLKs
6	Retry Secondary Master	R/W	If 0, and if HB1-SE has been granted access to the primary bus, and a secondary master initiates a cycle to access the primary bus while it is still busy, HB1-SE will wait for the primary bus to be idle instead of immediately retrying the secondary master. If 1, HB1-SE will immediately retry the secondary master if granted access to the primary bus while the primary bus is busy.
7	Back to Back Cycle Enable	R/W	This bit enables back to back cycles on the primary interface, if bit 9 of the primary command register is also enabled.

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GPIO Control Register (R/W) – Offset C5h

Bit	Function	Type	Description
0	GPIO0 Input	R/O	Contains the state of the GPIO0 pin
1	GPIO0 Output Enable	R/W	If 1, GPIO0 is configured as output. If 0, GPIO0 is an input pin
2	GPIO0 Output Register	R/W	Value written here will be output to GPIO0 pin if configured as output
3	Reserved	R/O	Reserved
4	GPIO1 Input	R/O	Contains the state of the GPIO1 pin
5	GPIO1 Output Enable	R/W	If 1, GPIO1 is configured as output. If 0, GPIO1 is an input pin
6	GPIO1 Output Register	R/W	Value written here will be output to GPIO1 pin if configured as output
7	Reserved	R/O	Reserved
8	GPIO2 Input	R/O	Contains the state of the GPIO2 pin
9	GPIO2 Output Enable	R/W	If 1, GPIO2 is configured as output. If 0, GPIO2 is an input pin
10	GPIO2 Output Register	R/W	Value written here will be output to GPIO2 pin if configured as output
11	Reserved	R/O	Reserved
12	GPIO3 Input	R/O	Contains the state of the GPIO3 pin
13	GPIO3 Output Enable	R/W	If 1, GPIO3 is configured as output. If 0, GPIO3 is an input pin
14	GPIO3 Output Register	R/W	Value written here will be output to GPIO3 pin if configured as output
15	Reserved	R/O	Reserved

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EEPROM Control - Offset C8

Bit	Function	Type	Description
0	Start	R/W	Starts the EEPROM read or write cycle.
1	EEPROM command	R/W	Controls the command sent to the EEPROM 1 : write 0 : read
2	EEPROM Error	R/O	This bit is set to 1 if EEPROM ack was not received during EEPROM cycle.
3	EEPROM autoload successful	R/O	This bit is set to 1 if EEPROM autoload occurred succesfully after reset, and some configuration registers were loaded with values programmed in the EEPROM. If zero, EEPROM autoload was unsuccessful or was disabled.
5-4	Reserved	R/O	Reserved. Returns '0' when read.
7-6	EEPROM clock rate	R/W	Controls frequency of EEPROM clock. EEPROM clock is derived from the primary PCI clock. 00 = Reserved 01 = PCLK/256 (Used for 33Mhz PCI) 10 = PCLK/128 11 = PCLK (test mode) defaults to 01

EEPROM Address - Offset C9h

Bit	Function	Type	Description
0	Reserved	R/O	Reserved
7-1	EEPROM address	R/W	Word address for EEPROM cycle.

EEPROM Data - Offset CAh

Bit	Function	Type	Description
15-0	EEPROM Data	R/W	Contains data to be written to the EEPROM. During reads, this register contains data received from the EEPROM after a read cycle has completed.

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HB1-SE Test Register - Offset CDh

Bit	Function	Type	Description
3-7	Reserved	R/O	Reserved

HB1-SE Test Register - Offset CEh

Bit	Function	Type	Description
3-7	Reserved	R/O	Reserved

HB1-SE Test Register - Offset CFh

Bit	Function	Type	Description
0	EEPROM Autoload control	R/W	If 1, disables EEPROM autoload
1	Fast EEPROM Autoload	R/W	If 1, speeds up EEPROM autoload
2	EEPROM autoload status	R/O	Status of EEPROM autoload
3-7	Reserved	R/O	Reserved

Subsystem Vendor ID - Offset F0h
(Read Only)

This register is a nonstandard implementation of the Subsystem Vendor ID register. It is EEPROM loadable. Defaults to 3388h

Subsystem ID - Offset F2h
(Read Only)

This register is a nonstandard implementation of the Subsystem ID register. It is EEPROM loadable. Defaults to 0021h

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8 PCI Bus Operation

This chapter presents detailed information about PCI transactions HB1-SE responds to and transactions initiated by the HB1-SE.

HB1-SE provides a simple, but complete PCI-PCI bridge capability, allowing PCI master and slave on its either side. It passes control and data between primary and secondary bus to guarantee complete visibility from either side. HB1-SE is designed to behave like an intelligent buffer.

HB1-SE achieves its zero wait state bridging function by controlling the direction of control and data. It divides control and data into 3 signal groups; the FRAME#/IRDY#/CBE#, LDEV#/TRDY#/STOP#, and AD signal groups.

Direction of FRAME#/IRDY#/CBE# is determined by P_GNT#. If P_GNT# is asserted at the time FRAME# is active, direction of LDEV#/TRDY#/STOP# is determined by address decode, as described in the address decode section. Direction of AD[31:0] is determined by the combination of address decode and location of slave.

8.1 Types of Transactions

This section provides a summary of PCI transactions performed by HB1-SE. Table 4–1 lists the command code and name of each PCI transaction. The Master and Target columns indicate support for each transaction when HB1-SE initiates transactions as a master, on the primary bus and on the secondary bus, and when HB1-SE responds to transactions as a target, on the primary bus and on the secondary bus.

Table 7–1 PCI Transactions

Type of transaction		Initiates as Master		Responds as Target	
		Primary	Secondary	Primary	Secondary
0000	Interrupt acknowledge	N	N	N	N
0001	Special cycle	Y	Y	N	N
0010	I/O read	Y	Y	Y	Y
0011	I/O write	Y	Y	Y	Y
0100	Reserved	N	N	N	N
0101	Reserved	N	N	N	N
0110	Memory read	Y	Y	Y	Y
0111	Memory write	Y	Y	Y	Y
1000	Reserved	N	N	N	N
1001	Reserved	N	N	N	N
1010	Configuration read	N	Y	Y	N
1011	Configuration write	Type 1	Y	Y	Type 1
1100	Memory read multiple	Y	Y	Y	Y
1101	Dual address cycle	N	N	N	N
1110	Memory read line	Y	Y	Y	Y
1111	Memory write and invalidate	Y	Y	Y	Y

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As indicated in Table 7–1, the following PCI commands are not supported by HB1-SE :

- HB1-SE never initiates a PCI transaction with a reserved command code and, as a target, HB1-SE ignores reserved command codes.
- HB1-SE never initiates an interrupt acknowledge transaction and, as a target, HB1-SE ignores interrupt acknowledge transactions. Interrupt acknowledge transactions are expected to reside entirely on the primary PCI bus closest to the host bridge.
- HB1-SE does not respond to special cycle transactions. To generate special cycle transactions on other PCI buses, either upstream or downstream, a Type 1 configuration command must be used.
- HB1-SE does not generate Type 0 configuration transactions on the primary interface, nor does it respond to Type 0 configuration transactions on the secondary PCI interface. The PCI-to-PCI Bridge Architecture Specification does not support configuration from the secondary bus.
- HB1-SE does not respond to nor initiate DAC cycle transactions.

8.2 Address Phase

A 32-bit address uses a single address phase. This address is driven on AD<31:0>, and the bus command is driven on P_CBE[3:0]

8.3 Device Select (LDEV#) Generation

HB1-SE always performs positive address decoding when accepting transactions on either the primary or secondary buses. HB1-SE never subtractively decodes. Medium LDEV# timing is used on both interfaces.

8.4 Data Phase

The address phase or phases of a PCI transaction are followed by one or more data phases. A data phase is completed when IRDY# and either TRDY# or STOP# are asserted. A transfer of data occurs only when both IRDY# and TRDY# are asserted during the same PCI clock cycle. The last data phase of a transaction is indicated when FRAME# is de-asserted and both TRDY# and IRDY# are asserted, or when IRDY# and STOP# are asserted.

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8.5 Write Transactions

Acting as PCI bus extender, HB1-SE responds differently according to the address and initiator.

Case 1: Primary master access device on primary bus
HB1-SE will forward all PCI signals from primary to secondary so that any device there can track the PCI bus.

Case 2: Primary master access device on secondary bus
HB1-SE will forward address, command, data, byte enable, P_IRDY# to secondary while forwarding S_LDEV#, S_TRDY# and S_STOP# to primary bus.

Case 3: Secondary master access device on secondary bus
HB1-SE will forward all PCI signals from secondary to primary so that any device there can track the PCI bus.

Case 4: Secondary master access device on primary bus
HB1-SE will forward address, command, data, byte enable, S_IRDY# to primary while forwarding P_LDEV#, P_TRDY# and P_STOP# to secondary.

There is no buffer inside HB1-SE for write.

8.6 Read Transactions

HB1-SE responds according to the address and initiator of the read command.

Case 1: Primary master access device on primary bus

HB1-SE will forward all PCI signals from primary to secondary so that any device there can track the PCI bus.

Case 2: Primary master access device on secondary bus
HB1-SE will forward address, command, byte enable, P_IRDY# to secondary while forwarding data, S_LDEV#, S_TRDY# and S_STOP# to primary bus.

Case 3: Secondary master access device on secondary bus
HB1-SE will forward all PCI signals from secondary to primary so that any device there can track the PCI bus.

Case 4: Secondary master access device on primary bus
HB1-SE will forward address, command, byte enable, S_IRDY# to primary while forwarding data, P_LDEV#, P_TRDY# and P_STOP# to secondary.

There is no buffer inside HB1-SE for read.

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8.7 Configuration Transactions

Configuration transactions are used to initialize a PCI system. Every PCI device has a configuration space that is accessed by configuration commands. All registers are accessible in configuration space only.

In addition to accepting configuration transactions for initialization of its own configuration space, HB1-SE also forwards configuration transactions for device initialization in hierarchical PCI systems, as well as for special cycle generation.

To support hierarchical PCI bus systems, two types of configuration transactions are specified: Type 0 and Type 1.

Type 0 configuration transactions are issued when the intended target resides on the same PCI bus as the initiator. A Type 0 configuration transaction is identified by the configuration command and the Lowest 2 bits of the address set to 00b.

Type 1 configuration transactions are issued when the intended target resides on another PCI bus, or when a special cycle is to be generated on another PCI bus. A Type 1 configuration command is identified by the configuration command and the Lowest 2 address bits set to 01b.

The register number is found in both Type 0 and Type 1 formats and gives the Dword address of the configuration register to be accessed. The function number is also included in both Type 0 and Type 1 formats and indicates which function of a multifunction device is to be accessed. For single-function devices, this value is not decoded. Type 1 configuration transaction addresses also include a 5-bit field designating the device number that identifies the device on the target PCI bus that is to be accessed. In addition, the bus number in Type 1 transactions specifies the PCI bus to which the transaction is targeted.

8.7.1 Type 0 Access to HB1-SE

The configuration space is accessed by a Type 0 configuration transaction on the primary interface. The configuration space cannot be accessed from the secondary bus. HB1-SE responds to a Type 0 configuration transaction by asserting P_LDEV# when the following conditions are met during the address phase:

- The bus command is a configuration read or configuration write transaction.
- low 2 address bits P_AD<1:0> must be 00b.
- Signal P_IDSEL must be asserted.
- The function code is 0.

HB1-SE limits all configuration accesses to a single Dword data transfer and returns a target disconnect with the first data transfer if additional data phases are requested. Because read transactions to configuration space do not have side effects, all bytes in the requested Dword are returned, regardless of the value of the byte enable bits.

Type 0 configuration write and read transactions do not use data buffers; that is, these transactions are completed immediately.

HB1-SE ignores all Type 0 transactions initiated on the secondary interface.

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8.7.2 Type 1 to Type 0 Translation

Type 1 configuration transactions are used specifically for device configuration in a hierarchical PCI bus system. A PCI-to-PCI bridge is the only type of device that should respond to a Type 1 configuration command. Type 1 configuration commands are used when the configuration access is intended for a PCI device that resides on a PCI bus other than the one where the Type 1 transaction is generated.

HB1-SE performs a Type 1 to Type 0 translation when the Type 1 transaction is generated on the primary bus and is intended for a device attached directly to the secondary bus. HB1-SE must convert the configuration command to a Type 0 format so that the secondary bus device can respond to it. Type 1 to Type 0 translations are performed only in the downstream direction; that is, HB1-SE generates a Type 0 transaction only on the secondary bus, and never on the primary bus.

HB1-SE responds to a Type 1 configuration transaction and translates it into a Type 0 transaction on the secondary bus when the following conditions are met during the address phase:

- The low 2 address bits on P_AD<1:0> are 01b.
- The bus number in address field P_AD<23:16> is equal to the value in the secondary bus number register in configuration space.
- The bus command on P_CBE<3:0> is a configuration read or configuration write transaction.

When HB1-SE translates the Type 1 transaction to a Type 0 transaction on the secondary interface, it performs the following translations to the address:

- Sets the low 2 address bits on S_AD<1:0> to 00b.
- Decodes the device number and drives the bit pattern specified in Table 4–6 on S_AD<31:16> for the purpose of asserting the device's IDSEL signal.
- Sets S_AD<15:11> to 0.
- Leaves unchanged the function number and register number fields.

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HB1-SE asserts a unique address line based on the device number. These address lines may be used as secondary bus IDSEL signals. The mapping of the address lines depends on the device number in the Type 1 address bits P_AD<15:11>. Table 7–2 presents the mapping that HB1-SE uses.

Table 7–2 Device Number to IDSEL S_AD Pin Mapping

Device Number	P_AD<15:11>	Secondary IDSEL S_AD<31:16>	S_AD Bit
0h	00000	0000 0000 0000 0001	16
1h	00001	0000 0000 0000 0010	17
2h	00010	0000 0000 0000 0100	18
3h	00011	0000 0000 0000 1000	19
4h	00100	0000 0000 0001 0000	20
5h	00101	0000 0000 0010 0000	21
6h	0110	0000 0000 0100 0000	22
7h	00111	0000 0000 1000 0000	23
8h	01000	0000 0001 0000 0000	24
9h	01001	0000 0010 0000 0000	25
Ah	01010	0000 0100 0000 0000	26
Bh	01011	0000 1000 0000 0000	27
Ch	01100	0001 0000 0000 0000	28
Dh	01101	0010 0000 0000 0000	29
Eh	01110	0100 0000 0000 0000	30
Fh	01111	1000 0000 0000 0000	31
1Fh	11111	Generate special cycle (P_AD<7:2> = 00h) 0000 0000 0000 0000 (P_AD<7:2> != 00h)	-

HB1-SE can assert up to 16 unique address lines to be used as IDSEL signals for up to 16 devices on the secondary bus, for device numbers ranging from 0 through 15. Because of electrical loading constraints of the PCI bus, more than 16 IDSEL signals should not be necessary. However, if device numbers greater than 15 are desired, some external method of generating IDSEL lines must be used, and no upper address bits are then asserted. The configuration transaction is still translated and passed from the primary bus to the secondary bus. If no IDSEL pin is asserted to a secondary device, the transaction ends in a master abort.

HB1-SE forwards Type 1 to Type 0 configuration read or write transactions as delayed transactions. Type 1 to Type 0 configuration read or write transactions are limited to a single 32-bit data transfer.

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8.7.3 Type 1 to Type 1 Forwarding

Type 1 to Type 1 transaction forwarding provides a hierarchical configuration mechanism when two or more levels of PCI-to-PCI bridges are used.

When HB1-SE detects a Type 1 configuration transaction intended for a PCI bus downstream from the secondary bus, HB1-SE forwards the transaction unchanged to the secondary bus. Ultimately, this transaction is translated to a Type 0 configuration command or to a special cycle transaction by a downstream PCI-to-PCI bridge. Downstream Type 1 to Type 1 forwarding occurs when the following conditions are met during the address phase:

- The low 2 address bits are equal to 01b.
- The bus number falls in the range defined by the lower limit (exclusive) in the secondary bus number register and the upper limit (inclusive) in the subordinate bus number register.
- The bus command is a configuration read or write transaction.

HB1-SE also supports Type 1 to Type 1 forwarding of configuration write transactions upstream to support upstream special cycle generation. A Type 1 configuration command is forwarded upstream when the following conditions are met:

- The low 2 address bits are equal to 01b.
- The bus number falls outside the range defined by the lower limit (inclusive) in the secondary bus number register and the upper limit (inclusive) in the subordinate bus number register.
- The device number in address bits AD<15:11> is equal to 11111b.
- The function number in address bits AD<10:8> is equal to 111b.
- The bus command is a configuration write transaction.

HB1-SE forwards Type 1 to Type 1 configuration write transactions as delayed transactions. Type 1 to Type 1 configuration write transactions are limited to a single data transfer.

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8.7.4 Special Cycles

The Type 1 configuration mechanism is used to generate special cycle transactions in hierarchical PCI systems. Special cycle transactions are ignored by acting as a target and are not forwarded across the bridge. Special cycle transactions can be generated from Type 1 configuration write transactions in either the upstream or the downstream direction.

HB1-SE initiates a special cycle on the target bus when a Type 1 configuration write transaction is

detected on the initiating bus and the following conditions are met during the address phase:

- The low 2 address bits on AD<1:0> are equal to 01b.
- The device number in address bits AD<15:11> is equal to 11111b.
- The function number in address bits AD<10:8> is equal to 111b.
- The register number in address bits AD<7:2> is equal to 000000b.
- The bus number is equal to the value in the secondary bus number register in configuration space for downstream forwarding or equal to the value in the primary bus number register in configuration space for upstream forwarding.
- The bus command on P_CBE# is a configuration write command.

When HB1-SE initiates the transaction on the target interface, the bus command is changed from configuration write to special cycle. The address and data are forwarded unchanged. Devices that use special cycles ignore the address and decode only the bus command. The data phase contains the special cycle message. The transaction is forwarded as a delayed transaction, but in this case the target response is not forwarded back (because special cycles result in a master abort). Once the transaction is completed on the target bus, through detection of the master abort condition, HB1-SE responds with TRDY# to the next attempt of the configuration transaction from the initiator.

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8.8 Transaction Termination

This section describes how HB1-SE returns transaction termination conditions back to the initiator.

The initiator can terminate transactions with one of the following types of termination:

- Normal termination
- Normal termination occurs when the initiator de-asserts FRAME# at the beginning of the last data phase, and de-asserts IRDY# at the end of the last data phase in conjunction with either TRDY# or STOP# assertion from the target.
- Master abort
- A master abort occurs when no target response is detected. When the initiator does not detect a LDEV# from the target within five clock cycles after asserting FRAME#, the initiator terminates the transaction with a master abort. If FRAME# is still asserted, the initiator de-asserts FRAME# on the next cycle, and then de-asserts IRDY# on the following cycle. IRDY# must be asserted in the same cycle in which FRAME# de-asserts. If FRAME# is already de-asserted, IRDY# can be de-asserted on the next clock cycle following detection of the master abort condition.
- The target can terminate transactions with one of the following types of termination:
- Normal termination—TRDY# and LDEV# asserted in conjunction with FRAME# de-asserted and IRDY# asserted.
- Target retry—STOP# and LDEV# asserted without TRDY# during the first data phase. No data transfers occur during the transaction. This transaction must be repeated.
- Target disconnect with data transfer—STOP# and LDEV# asserted with TRDY#. Signals that this is the last data transfer of the transaction.
- Target disconnect without data transfer—STOP# and LDEV# asserted without TRDY# after previous data transfers have been made. Indicates that no more data transfers will be made during this transaction.
- Target abort—STOP# asserted without LDEV# and without TRDY#.
- Indicates that the target will never be able to complete this transaction. LDEV# must be asserted for at least one cycle during the transaction before the target abort is signaled.

8.8.1 Master Termination Initiated by HB1-SE

HB1-SE, as an initiator, uses normal termination if LDEV# is returned by the target within five clock cycles of HB1-SE's assertion of FRAME# on the target bus. HB1-SE terminates a transaction when the target terminates the transaction with last data transfer, retry, disconnect, or target abort.

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8.8.2 Master Abort Received by HB1-SE

If the initiator initiates a transaction on the target bus and does not detect LDEV# returned by the target within five clock cycles of HB1-SE's assertion of FRAME#, HB1-SE terminates the transaction with a master abort. This sets the received master abort bit in the status register corresponding to the target bus.

For delayed read and write transactions, HB1-SE is able to reflect the master abort condition back to the initiator. When HB1-SE detects a master abort in response to a delayed transaction, and when the initiator repeats the transaction, HB1-SE does not respond to the transaction with LDEV#. This passes the master abort condition back to the initiator.

Note

When HB1-SE performs a Type 1 to special cycle translation, a master abort is the expected termination for the special cycle on the target bus. In this case, the master abort received bit is not set, and the Type 1 configuration transaction is disconnected after the first data phase.

8.8.3 Target Termination Received by HB1-SE

When HB1-SE initiates a transaction on the target bus and the target responds with LDEV#, the target can end the transaction with one of the following types of termination:

- Normal termination (upon de-assertion of FRAME#)
- Target retry
- Target disconnect
- Target abort

HB1-SE handles these terminations in different ways, depending on the type of transaction being performed.

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8.8.3.1 Delayed Write Target Termination Response

When HB1-SE initiates a delayed write transaction, the type of target termination received from the target can be passed back to the initiator. Table 7–3 shows the response to each type of target termination that occurs during a delayed write transaction.

- HB1-SE repeats a delayed write transaction until one of the following conditions is met:
- HB1-SE completes at least one data transfer.
- HB1-SE receives a master abort.
- HB1-SE receives a target abort.

HB1-SE makes 2^{24} write attempts resulting in a response of target retry.

Table 7-3 Response to Delayed Write Target Termination

Target Termination	Response
Normal	Return disconnect to initiator with first data transfer only if multiple data phases requested.
Target retry	Return target retry to initiator. Continue write attempts to target.
Target disconnect	Return disconnect to initiator with first data transfer only if multiple data phases requested.
Target abort	Return target abort to initiator. Set received target abort bit in target interface status register. Set signaled target abort bit in initiator interface status register.

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8.8.3.2 Delayed Read Target Termination Response

When HB1-SE initiates a delayed read transaction, the abnormal target responses can be passed back to the initiator. Other target responses depend on how much data the initiator requests. Table 7-4 shows the response to each type of target termination that occurs during a delayed read transaction.

Table 7-4 Response to Delayed Read Target Termination

Target termination	Response
Normal	If prefetchable, target disconnect only if initiator requests more data than read from target. If nonprefetchable, target disconnect on first data phase.
Target retry	Reinitiate read transaction to target
Target disconnect	If initiator requests more data than read from target, return target disconnect to initiator
Target abort	Return target abort to initiator. Set received target abort bit in the target interface status register. Set signaled target abort bit in the initiator interface status register.

HB1-SE repeats a delayed read transaction until one of the following conditions is met:

- HB1-SE completes at least one data transfer.
- HB1-SE receives a master abort.
- HB1-SE receives a target abort.

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8.8.4 Target Termination Initiated by HB1-SE

HB1-SE can return a target retry, target disconnect, or target abort to an initiator for reasons other than detection of that condition at the target interface.

8.8.4.1 Target Retry

HB1-SE returns a target retry to the initiator when it cannot accept write data or return read data as a result of internal conditions. HB1-SE returns a target retry to an initiator when any of the following conditions is met:

- For delayed write transactions:
  - The transaction is being entered into the delayed transaction queue.
  - The transaction has already been entered into the delayed transaction queue, but target response has not yet been received.
  - The delayed transaction queue is full, and the transaction cannot be queued.
  - A transaction with the same address and command has been queued.
  - Uses more than 16 clocks to accept this transaction.

- For delayed read transactions:
  - The transaction is being entered into the delayed transaction queue.
  - The read request has already been queued, but read data is not yet available.
  - The delayed transaction queue is full, and the transaction cannot be queued.
  - A delayed read request with the same address and bus command has already been queued.
  - Uses more than 16 clocks to accept this transaction.

When a target retry is returned to the initiator of a delayed transaction, the initiator must repeat the transaction with the same address and bus command as well as the data if this is a write transaction, within the time frame specified by the master timeout value; otherwise, the transaction is discarded from the buffer.

8.8.4.2 Target Disconnect

HB1-SE returns a target disconnect to an initiator when the target returns target disconnect.

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8.8.4.3 Target Abort

HB1-SE returns a target abort to an initiator when one of the following conditions is met:

- HB1-SE is returning a target abort from the intended target.
- HB1-SE is unable to obtain delayed read data from the target or to deliver delayed write data to the target after 2 attempts.

When HB1-SE returns a target abort to the initiator, it sets the signaled target abort bit in the status register corresponding to the initiator interface.

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9 Address Decoding

HB1-SE uses three address ranges that control I/O and memory transaction forwarding. These address ranges are defined by base and limit address registers in the configuration space. This chapter describes these address ranges, as well as ISA-mode and VGA-addressing support.

9.1 Address Ranges

HB1-SE uses the following address ranges to determine which I/O and memory transactions are forwarded from the primary PCI bus to the secondary PCI bus, and from the secondary bus to the primary bus:

- Two 32-bit I/O address ranges

Transactions falling within these ranges are forwarded downstream from the primary PCI bus to the two secondary PCI buses. Transactions falling outside these ranges are forwarded upstream from the two secondary PCI buses to the primary PCI bus.

HB1-SE uses a flat address space; that is, it does not perform any address translations. The address space has no ‘‘gaps’’—addresses that are not marked for downstream forwarding are always forwarded upstream.

9.2 I/O Address Decoding

HB1-SE uses the following mechanisms that are defined in the configuration space to specify the I/O address space for downstream and upstream forwarding:

- I/O base and limit address registers
- The ISA enable bit
- The VGA mode bit
- The VGA snoop bit

This section provides information on the I/O address registers and ISA mode.

To enable downstream forwarding of I/O transactions, the I/O enable bit must be set in the command register in configuration space. If the I/O enable bit is not set, all I/O transactions initiated on the primary bus are ignored. To enable upstream forwarding of I/O transactions, the master enable bit must be set in the command register. If the master enable bit is not set, HB1-SE ignores all I/O and memory transactions initiated on the secondary bus. Setting the master enable bit also Allows upstream forwarding of memory transactions.

Caution

If any configuration state affecting I/O transaction forwarding is changed by a configuration write operation on the primary bus at the same time that I/O transactions are ongoing on the secondary bus, the

HB1-SE response to the secondary bus I/O transactions is not predictable. Configure the I/O base and limit address registers, ISA enable bit, VGA mode bit, and VGA snoop bit before setting the I/O enable and master enable bits, and change them subsequently only when the primary and secondary PCI buses are idle.

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9.2.1 I/O Base and Limit Address Registers

HB1-SE implements one set of I/O base and limit address registers in configuration space that define an I/O address range per port downstream forwarding. HB1-SE supports 32-bit I/O addressing, which Allows I/O addresses downstream of HB1-SE to be mapped anywhere in a 4GB I/O address space.

I/O transactions with addresses that fall inside the range defined by the I/O base and limit registers are forwarded downstream from the primary PCI bus to the secondary PCI bus. I/O transactions with addresses that fall outside this range are forwarded upstream from the secondary PCI bus to the primary PCI bus.

The I/O range can be turned off by setting the I/O base address to a value greater than that of the I/O limit address. When the I/O range is turned off, all I/O transactions are forwarded upstream, and no I/O transactions are forwarded downstream.

The I/O range has a minimum granularity of 4KB and is aligned on a 4KB boundary. The maximum I/O range is 4GB in size.

The I/O base register consists of an 8-bit field at configuration address 1Ch, and a 16-bit field at address 30h. The top 4 bits of the 8-bit field define bits <15:12> of the I/O base address. The bottom 4 bits read only as 1h to indicate that HB1-SE supports 32-bit I/O addressing. Bits <11:0> of the base address are assumed to be 0, which naturally aligns the base address to a 4KB boundary. The 16 bits contained in the I/O base upper 16 bits register at configuration offset 30h define AD<31:16> of the I/O base address. All 16 bits are read/write. After primary bus reset or chip reset, the value of the I/O base address is initialized to 0000 0000h.

The I/O limit register consists of an 8-bit field at configuration offset 1Dh and a 16-bit field at offset 32h. The top 4 bits of the 8-bit field define bits <15:12> of the I/O limit address. The bottom 4 bits read only as 1h to indicate that 32-bit I/O addressing is supported. Bits <11:0> of the limit address are assumed to be FFFh, which naturally aligns the limit address to the top of a 4KB I/O address block. The 16 bits contained in the I/O limit upper 16 bits register at configuration offset 32h define AD<31:16> of the I/O limit address. All 16 bits are read/write. After primary bus reset or chip reset, the value of the I/O limit address is reset to 0000 0FFFh.

Note

The initial states of the I/O base and I/O limit address registers define an I/O range of 0000 0000h to 0000 0FFFh, which is the bottom 4KB of I/O space. Write these registers with their appropriate values before setting either the I/O enable bit or the master enable bit in the command register in configuration space.

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9.2.2 ISA Mode

HB1-SE supports ISA mode by providing an ISA enable bit in the bridge control register in configuration space. ISA mode modifies the response of HB1-SE inside the I/O address range in order to support mapping of I/O space in the presence of an ISA bus in the system. This bit only affects the response of HB1-SE when the transaction falls inside the address range defined by the I/O base and limit address registers, and only when this address also falls inside the first 64KB of I/O space (address bits <31:16> are 0000h).

When the ISA enable bit is set, HB1-SE does not forward downstream any I/O transactions addressing the top 768 bytes of each aligned 1KB block. Only those transactions addressing the bottom 256 bytes of an aligned 1KB block inside the base and limit I/O address range are forwarded downstream. Transactions above the 64KB I/O address boundary are forwarded as defined by the address range defined by the I/O base and limit registers.

Accordingly, if the ISA enable bit is set, HB1-SE forwards upstream those I/O transactions addressing the top 768 bytes of each aligned 1KB block within the first 64KB of I/O space. The master enable bit in the command configuration register must also be set to enable upstream forwarding. All other I/O transactions initiated on the secondary bus are forwarded upstream only if they fall outside the I/O address range.

When the ISA enable bit is set, devices downstream of HB1-SE can have I/O space mapped into the first 256 bytes of each 1KB chunk below the 64KB boundary, or anywhere in I/O space above the 64KB boundary.

9.3 Memory Address Decoding

HB1-SE has three mechanisms for defining memory address ranges for forwarding of memory transactions:

- Memory-mapped I/O base and limit address registers
- Prefetchable memory base and limit address registers
- VGA mode

This section describes the first two mechanisms.

To enable downstream forwarding of memory transactions, the memory enable bit must be set in the command register in configuration space. To enable upstream forwarding of memory transactions, the master enable bit must be set in the command register. Setting the master enable bit also Allows upstream forwarding of I/O transactions.

Caution

If any configuration state affecting memory transaction forwarding is changed by a configuration write operation on the primary bus at the same time that memory transactions are ongoing on the secondary bus, response to the secondary bus memory transactions is not predictable. Configure the memory-mapped I/O base and limit address registers, prefetchable memory base and limit address registers, and VGA mode bit before setting the memory enable and master enable bits, and change them subsequently only when the primary and secondary PCI buses are idle.

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9.3.1 Memory-Mapped I/O Base and Limit Address Registers

Memory-mapped I/O is also referred to as nonprefetchable memory. Memory addresses that cannot automatically be prefetched but that can conditionally prefetch based on command type should be mapped into this space. Read transactions to nonprefetchable space may exhibit side effects; this space may have non-memory-like behavior. HB1-SE prefetches in this space only if the memory read line or memory read multiple commands are used; transactions using the memory read command are limited to a single data transfer.

The memory-mapped I/O base address and memory-mapped I/O limit address registers define an address range that HB1-SE uses to determine when to forward memory commands. HB1-SE forwards a memory transaction from the primary to the secondary interface if the transaction address falls within the memory-mapped I/O address range. HB1-SE ignores memory transactions initiated on the secondary interface that fall into this address range. Any transactions that fall outside this address range are ignored on the primary interface and are forwarded upstream from the secondary interface (provided that they do not fall into the prefetchable memory range or are not forwarded downstream by the VGA mechanism).

The memory-mapped I/O range supports 32-bit addressing only. The PCI-to-PCI Bridge Architecture Specification does not provide for 64-bit addressing in the memory-mapped I/O space. The memory-mapped I/O address range has a granularity and alignment of 1MB. The maximum memory-mapped I/O address range is 4GB.

The memory-mapped I/O address range is defined by a 16-bit memory-mapped I/O base address register at configuration offset 20h and by a 16-bit memory-mapped I/O limit address register at offset 22h. The top 12 bits of each of these registers correspond to bits <31:20> of the memory address. The low 4 bits are hardwired to 0. The low 20 bits of the memory-mapped I/O base address are assumed to be 0 0000h, which results in a natural alignment to a 1MB boundary. The low 20 bits of the memory-mapped I/O limit address are assumed to be F FFFFh, which results in an alignment to the top of a 1MB block.

Note

The initial state of the memory-mapped I/O base address register is 0000 0000h. The initial state of the memory-mapped I/O limit address register is 000F FFFFh. Note that the initial states of these registers define a memory-mapped I/O range at the bottom 1MB block of memory. Write these registers with their appropriate values before setting either the memory enable bit or the master enable bit in the command register in configuration space.

To turn off the memory-mapped I/O address range, write the memory-mapped I/O base address register with a value greater than that of the memory-mapped I/O limit address register.

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10 PCI Bus Arbitration

HB1-SE must arbitrate for use of the primary bus when forwarding upstream transactions, and for use of the secondary bus when forwarding downstream transactions. The arbiter for the primary bus resides external to the typically on the motherboard. For the secondary PCI bus, HB1-SE implements an internal arbiter.

10.1 Primary PCI Bus Arbitration

HB1-SE implements a request output pin, P_REQ#, and a grant input pin, P_GNT#, for primary PCI bus arbitration. HB1-SE asserts P_REQ# when forwarding transactions upstream; that is, it acts as initiator on the primary PCI bus. However, if a target retry, target disconnect, or a target abort is received in response to a transaction initiated by HB1-SE on the primary PCI bus, HB1-SE de-asserts P_REQ# for two PCI clock cycles.

When P_GNT# is asserted LOW by the primary bus arbiter after HB1-SE has asserted P_REQ#, HB1-SE initiates a transaction on the primary bus on behalf of master on secondary. When P_GNT# is asserted to HB1-SE when P_REQ# is not asserted, HB1-SE parks P_AD, P_CBE, and P_PAR by driving them to valid logic levels. When the primary bus is parked at HB1-SE and HB1-SE then has a transaction to initiate on the primary bus, HB1-SE starts the transaction if P_GNT# was asserted during the previous cycle.

10.2 Secondary PCI Bus Arbitration

HB1-SE implements an internal secondary PCI bus arbiter. This arbiter supports 4 external masters in addition to HB1-SE.

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11 Transaction Delay

HB1-SE transaction delay from one interface to the other can be controlled through register C4h, bits 4 and 5. Primary to secondary transaction delay and secondary to primary transaction delay can be configured separately at 1 or 2 clocks delay.

HB1-SE supports 1 clock latency mode in order to minimize the delay. In this mode, there is strictly 1 clock delay between the originating FRAME and the bridge FRAME. HB1-SE passes all memory and I/O cycles, regardless of the address. On the 2nd clock of the cycle, HB1-SE checks which side the cycle belongs to. If it is determined to be the wrong side, HB1-SE will self terminate its own cycle by asserting STOP_L.

This mode can be independently enabled for the Primary to Secondary transfer, and for the Secondary to Primary transfer. It is used primarily to minimize the delay between the assertion of the PGNT_L on the Primary side and the assertion of PFRAME_L due to the transaction initiated on the secondary side. HB1-SE is designed to restrict SGNT_L based on the assertion of PGNT_L.

The control flow is as follows:

1. Primary asserts PGNT_L in response to the PREQ_L asserted by HB1-SE
2. Secondary asserts SGNT_L in response to PGNT_L
3. Secondary master asserts SFRAME_L in response to SGNT_L
4. HB1-SE passes through the SFRAME_L to PFRAME_L.

There could be up to 4 clocks delay from step 1 to 4. This mode will decrease the delay to 3 clocks.

If 2 clock latency mode is enabled, which is the default, then the delay for step 4 above is 2 clocks instead of 1, with everything else the same.

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12 Error Handling

HB1-SE checks, forwards, and generates parity on both the primary and secondary interfaces. To maintain transparency, HB1-SE always tries to forward the existing parity condition on one bus to the other bus, along with address and data.

To support error reporting on the PCI bus, HB1-SE implements the following:

- S_SERR# signal on the secondary interface
- Primary status and secondary status registers

This chapter provides detailed information about how HB1-SE handles errors. It also describes error status reporting and error operation disabling.

12.1 Address Parity Errors

HB1-SE checks address parity for all transactions on both buses, for all address and all bus commands.

When HB1-SE detects an address parity error on the primary interface, the following events occur:

- If the parity error response bit is set in the command register, HB1-SE does not claim the transaction with P_LDEV#; this may allow the transaction to terminate in a master abort.

  If the parity error response bit is not set, HB1-SE proceeds normally and accepts the transaction if it is directed to or across the HB1-SE.

- HB1-SE sets the detected parity error bit in the status register.
- HB1-SE asserts P_SERR# and sets the signaled system error bit in the status register, if both of the following conditions are met:
    - The SERR# enable bit is set in the command register.
    - The parity error response bit is set in the command register.

When HB1-SE detects an address parity error on the secondary interface, the following events occur:

- If the parity error response bit is set in the bridge control register, HB1-SE does not claim the transaction with S_LDEV#; this may allow the transaction to terminate in a master abort.

If the parity error response bit is not set, HB1-SE proceeds normally and accepts the transaction if it is directed to or across the HB1-SE.

- HB1-SE sets the detected parity error bit in the secondary status register.
- HB1-SE asserts S_SERR# and sets the signaled system error bit in the status register, if both of the following conditions are met:
    - The SERR# enable bit is set in the command register.
    - The parity error response bit is set in the bridge control register.

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12.2 Data Parity Errors

When forwarding transactions, HB1-SE attempts to pass the data parity condition from one interface to the other unchanged, whenever possible, to allow the master and target devices to handle the error condition.

The following sections describe, for each type of transaction, the sequence of events that occurs when a parity error is detected and the way in which the parity condition is forwarded across HB1-SE.

12.2.1 Configuration Write Transactions to Configuration Space

When HB1-SE detects a data parity error during a Type 0 configuration write transaction to configuration space, the following events occur:

- If the parity error response bit is set in the command register, HB1-SE asserts P_TRDY# and writes the data to the configuration register. HB1-SE also asserts S_SERR#.
- If the parity error response bit is not set, HB1-SE does not assert P_SERR#.

HB1-SE sets the detected parity error bit in the status register, regardless of the state of the parity error response bit.

12.2.2 Read Transactions

When HB1-SE detects a parity error during a read transaction, the target drives data and data parity, and the initiator checks parity and conditionally asserts SERR#.

For downstream transactions, when HB1-SE detects a read data parity error on the secondary bus, the following events occur:

- HB1-SE asserts P_SERR# two cycles following the data transfer, if the secondary interface parity error response bit is set in the bridge control register.
- HB1-SE sets the detected parity error bit in the secondary status register.
- HB1-SE sets the data parity detected bit in the secondary status register, if the secondary interface parity error response bit is set in the bridge control register.
- HB1-SE forwards the bad parity with the data back to the initiator on the primary bus.
- HB1-SE completes the transaction normally.

For upstream transactions, when HB1-SE detects a read data parity error on the primary bus, the following events occur:

- HB1-SE asserts P_SERR# two cycles following the data transfer, if the primary interface parity error response bit is set in the command register.
- HB1-SE sets the detected parity error bit in the primary status register.
- HB1-SE sets the data parity detected bit in the primary status register, if the primary interface parity error response bit is set in the command register.
- HB1-SE forwards the bad parity with the data back to the initiator on the secondary bus.
- HB1-SE completes the transaction normally.

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HB1-SE returns to the initiator the data and parity that was received from the target. When the initiator detects a parity error on this read data and is enabled to report it, the initiator asserts PERR# two cycles after the data transfer occurs. It is assumed that the initiator takes responsibility for handling a parity error condition.

12.3 Data Parity Error Reporting Summary

In the previous sections, the HB1-SE's responses to data parity errors are presented according to the type of transaction in progress. This section organizes the HB1-SE's responses to data parity errors according to the status bits that the HB1-SE sets and the signals that it asserts.

Table 11-1 shows setting the detected parity error bit in the status register, corresponding to the primary interface. This bit is set when HB1-SE detects a parity error on the primary interface.

Table 11–1 Setting the Primary Interface Detected Parity Error Bit

Primary detected parity error bit	Transaction type	Direction	Bus where error was detected	Primary/secondary parity error response bits
0	Read	Downstream	Primary	x/x[1]
0	Read	Downstream	Secondary	x/x
1	Read	Upstream	Primary	x/x
0	Read	Upstream	Secondary	x/x
1	Delayed write	Downstream	Primary	x/x
0	Delayed write	Downstream	Secondary	x/x
0	Delayed write	Upstream	Primary	x/x
0	Delayed write	Upstream	Secondary	x/x

[1]x =don't care

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Table 11–2 shows setting the detected parity error bit in the secondary status register, corresponding to the secondary interface. This bit is set when HB1-SE detects a parity error on the secondary interface.

Table 11–2 Setting the Secondary Interface Detected Parity Error Bit

Secondary detected parity error bit	Transaction type	Direction	Bus where error was detected	Primary/secondary parity error response bits
0	Read	Downstream	Primary	x/x[1]
1	Read	Downstream	Secondary	x/x
0	Read	Upstream	Primary	x/x
0	Read	Upstream	Secondary	x/x
0	Delayed write	Downstream	Primary	x/x
0	Delayed write	Downstream	Secondary	x/x
0	Delayed write	Upstream	Primary	x/x
1	Delayed write	Upstream	Secondary	x/x

[1]x =don't care

Table 11-3 shows setting the data parity detected bit in the status register, corresponding to the primary interface. This bit is set under the following conditions:

- HB1-SE must be a master on the primary bus.
- The parity error response bit in the command register, corresponding to the primary interface, must be set.

Table 11-3 Setting the Primary Interface Data Parity Detected Bit

Primary data parity detected bit	Transaction type	Direction	Bus where error was detected	Primary/secondary parity error response bits
0	Read	Downstream	Primary	x/x[1]
0	Read	Downstream	Secondary	x/x
1	Read	Upstream	Primary	1/x
0	Read	Upstream	Secondary	x/x
0	Delayed write	Downstream	Primary	x/x
0	Delayed write	Downstream	Secondary	x/x
1	Delayed write	Upstream	Primary	1/x
0	Delayed write	Upstream	Secondary	x/x

[1]x =don't care

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Table 11–4 shows setting the data parity detected bit in the secondary status register, corresponding to the secondary interface. This bit is set under the following conditions:

- The HB1-SE must be a master on the secondary bus.
- The parity error response bit in the bridge control register, corresponding to the secondary interface, must be set.

Table 11–4 Setting the Secondary Interface Data Parity Detected Bit

Secondary data parity detected bit	Transaction type	Direction	Bus where error was detected	Primary/secondary parity error response bits
0	Read	Downstream	Primary	x/x[1]
1	Read	Downstream	Secondary	x/1
0	Read	Upstream	Primary	x/x
0	Read	Upstream	Secondary	x/x
0	Delayed write	Downstream	Primary	x/x
1	Delayed write	Downstream	Secondary	x/1
0	Delayed write	Upstream	Primary	x/x
0	Delayed write	Upstream	Secondary	x/x

[1]x =dont care

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Table 11-5 shows assertion of S_SERR#. This signal is set under the following conditions:

- The parity error response bit on the command register and the parity error response bit on the bridge control register must both be set.
- The SERR# enable bit must be set in the command register.

Table 11-5 Assertion of S_SERR# for Data Parity Errors

Transaction type	Direction	Bus where error was detected	Primary/secondary parity error response bits
Read	Downstream	Primary	x/x[1]
Read	Downstream	Secondary	x/x
Read	Upstream	Primary	x/x
Read	Upstream	Secondary	x/x
Delayed write	Downstream	Primary	x/x
Delayed write	Downstream	Secondary	x/x
Delayed write	Upstream	Primary	x/x
Delayed write	Upstream	Secondary	x/x

[1]x =don't care

[2]The parity error was detected on the target (secondary) bus but not on the initiator (primary) bus.

[3]The parity error was detected on the target (primary) bus but not on the initiator (secondary) bus.

12.4 System Error (SERR#) Reporting

HB1-SE uses the P_SERR# signal to report conditionally a number of system error conditions in addition to the special case parity error conditions.

Whenever the assertion of P_SERR# is discussed in this document, it is assumed that the following conditions apply:

- For HB1-SE to assert P_SERR# for any reason, the SERR# enable bit must be set in the command register.
- Whenever HB1-SE asserts P_SERR#, HB1-SE must also set the signaled system error bit in the status register.

When S_SERR# is asserted by secondary device, HB1-SE sets the received system error bit in the secondary status register.

The HB1-SE also conditionally asserts P_SERR# when parity error reported on target bus during write transaction.

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13 Reset

This chapter describes the primary interface, secondary interface, and chip reset mechanisms.

13.1 Primary Interface Reset

HB1-SE has one reset input, P_RST#. When P_RST# is asserted, the following events occur:

- HB1-SE immediately tristates all primary and secondary PCI interface signals.
- HB1-SE performs a chip reset.
- Registers that have default values are reset.

The P_RST# asserting and de-asserting edges can be asynchronous to P_CLK and S_CLK.

13.2 Secondary Interface Reset

HB1-SE is responsible for driving the secondary bus reset signal, S_RST#.

HB1-SE asserts S_RST# when any of the following conditions is met:

- Signal P_RST# is asserted.
- Signal S_RST# remains asserted as long as P_RST# is asserted and does not de-assert until P_RST# is de-asserted and the secondary clock serial disable mask has been shifted in (23 clock cycles after P_RST# de-assertion).
- The secondary reset bit in the bridge control register is set.
- Signal S_RST# remains asserted until a configuration write operation clears the secondary reset bit and the secondary clock serial mask has been shifted in.
- The chip reset bit in the diagnostic control register is set.
- Signal S_RST# remains asserted until a configuration write operation clears the secondary reset bit and the secondary clock serial mask has been shifted in.

When S_RST# is asserted, all secondary PCI interface control signals, including the secondary grant outputs, are immediately tristated. Signals S_AD, S_CBE#, and S_PAR are driven LOW for the duration of S_RST# assertion. All posted write and delayed transaction data buffers are reset; therefore, any transactions residing in buffers at the time of secondary reset are discarded.

When S_RST# is asserted by means of the secondary reset bit, HB1-SE remains accessible during secondary interface reset and continues to respond to accesses to its configuration space from the primary interface.

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14 Bridge Behavior

A PCI cycle is initiated by asserting the FRAME# signal. In a bridge, there are a number of possibilities. These are summarized in the table below.

Bridge Actions for Various Cycle Types

Initiator	Target	Response
Master on primary	Target on Primary	HB1-SE forward all signals to secondary. It detects this situation by decoding the address as well as monitoring the P_LDEV# for other fast and medium devices on the primary port.
Master on primary	Target on secondary	HB1-SE asserts P_LDEV#, then passes the cycle to the secondary. When cycle is complete on the target port, it will wait for the initiator to end with normal termination.
Master on primary	Target not on primary nor secondary port	HB1-SE does not respond and the cycle will terminate as master abort.
Master on secondary	Target on the secondary port	HB1-SE forward all signals to primary. It detects this situation by decoding the address as well as monitoring the S_LDEV# for other fast and medium devices on the secondary port.
Master on secondary	Target on primary port	HB1-SE asserts S_LDEV#, then passes the cycle to the appropriate port. When cycle is complete on the target port, it will wait for the initiator to end with normal termination.
Master on secondary	Target not on primary nor the other secondary	HB1-SE does not respond.

A target then has up to three cycles to respond before subtractive decoding is initiated. If the target detects an address hit, it should assert its LDEV# signal in the cycle corresponding to the values of bits 9 and 10 in the Configuration Status Register.

Termination of a PCI cycle can occur in a number of ways. Normal termination begins by the initiator (master) de-asserting FRAME# with IRDY# being asserted (or remaining asserted) on the same cycle. The cycle completes when TRDY# and IRDY# are both asserted simultaneously. The target should de-assert TRDY# for one cycle following final assertion (sustained tri-state signal).

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14.1 Abnormal Termination (Initiated by Bridge Master)

14.1.1 Master Abort

Master abort indicates that HB1-SE acting as a master receives no response (i.e., no target asserts P_LDEV# or S_LDEV#) from a target., the bridge de-asserts FRAME# and then de-asserts IRDY#.

14.1.2 PCI Master on Primary Bus

The table illustrates the direction of the PCI control/data path when a PCI transaction is initiated by a PCI master residing on the primary bus. It guarantees the integrity of the cycle, viewed from the primary and the secondary side.

Slave location	Command	FRAME/CBE IRDY	LDEV/TRDY STOP	AD
Primary bus	read	S->P	P->S	P->S
Primary bus	write	S->P	P->S	P<-S
Secondary bus	read	S->P	P<-S	---
Secondary bus	write	S->P	P<-S	---

HB1-SE is designed to pass almost all the primary cycles to the secondary side, except configuration cycle in the 1 clock delay case, as described below. HB1-SE performs configuration type #1 to type #0 conversion, on the cycle with a matched bus-number. It will pass the type #1 configuration cycle that locates on the secondary side of the bridge.

14.2 Configuration type #1 to type #0 conversion

When a type #1 configuration cycle appears on the primary side with a bus-number equaling to HB1-SE bridge bus-number, HB1-SE performs the type #1 to type #0 conversion cycle, as follows.

First, it will retry all the subsequent all the primary cycles, until its completion. And it will de-grant the secondary bus to block the secondary master. The conversion cycle will appear on the secondary bus only, without being reflected to the primary side.

Then, it issues the converted type #0 configuration cycle on the secondary side. The termination of the cycle can be either normal, master abort or slave abort. In the case of read, HB1-SE will latch the data, and wait for the same type #1 configuration cycle on the primary side.

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14.3 Configuration type #1 to type #1 by-passing

When a type #1 configuration cycle appears on the primary side with a bus-number greater than HB1-SE bridge bus-number, but smaller than the secondary sub-ordinate bus-number, the same type #1 configuration cycle will appear on the secondary side. Otherwise, the bypassing process is very similar to the type #1 to type #0 conversion process. HB1-SE's internal state machine will generate the secondary cycle, retry all the primary cycle, and block any secondary master.

14.4 Type-0 Configuration cycle filter mode

In this Type-0 configuration cycle filter mode, HB1-SE will filter out all the primary Type-0 configuration cycle by delaying passing of primary P_FRAME# by one PCI clock. In case of Type-1 configuration cycle through the bridge, it will return retry and relies on the internal state machine to do the conversion cycle to generate Type-0 or Type-1 on the secondary side.

14.5 Decoding

HB1-SE uses decoding circuit to determine the slave device location.

During the memory cycle, HB1-SE uses Memory Base/Limit and PrefetchBase/Limit. Slave is on the secondary side if one of the following is true:

- MemoryBase[31:16] <= Address <= MemoryLimit[31:16]
- PrefetchBase[31:16] <= Address <= PrefetchLimit[31:16]
- when VGA is enabled, 0xa0000 <= Address <= 0xbffff

During the I/O cycle, HB1-SE uses I/O Base/Limit register. Slave device is on the secondary side if one of the following is true:

- I/O Base[15:4] <= Address <= IoLimit[15:4], see Note 1.
- when VGA is enabled, 0x3b0 <= Address <= 0x3bb
- when VGA is enabled, 0x3c0 <= Address <= 0x3df

Note1: when ISA is enabled, the I/O space between address 0-256 are always reserved at every 1K boundary.

During the Type-1 configuration cycle, HB1-SE uses the device bus-number and the sub-ordinate bus-number. Slave device is on the secondary side if:

BusNumber[7:0] <= Address <= SubordinateBusNumber[7:0]

All the type #0 configuration cycle, interrupt acknowledge cycle and the special cycle appearing on the primary side is considered to have slave on the primary side. Likewise, all the similar cycle appearing on the secondary side is considered to have slave on the secondary side.

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14.6 Secondary master

The secondary master issues S_REQ#[3:0] to request the bus. HB1-SE will generate P_REQ# on the primary side. When P_GNT# is active, HB1-SE will use the round-robin algorithm to grant one secondary master using S_GNT#[3:0].

The control/data path is illustrated below. HB1-SE will pass all the cycle from the secondary side to the primary.

Slave location	read/ Write	FRAME/CBE IRDY	LDEV/TRDY STOP	AD
primary	read	S->P	P->S	P->S
primary	write	S->P	P->S	P<-S
slave	read	S->P	P<-S	---
slave	write	S->P	P<-S	---

14.7 PCI clock run feature

HB1-SE supports PCI clock run protocol defined in the PCI Mobile Design Guide 1.0. P_CLKRUN# is set high when the system's central resource wants to stop P_CLK, and then HB1-SE will either signal that it allows PCI clock to be stopped by letting P_CLKRUN# remain high, or it will signal to the system to keep P_CLK running by driving P_CLKRUN# low for 2 clocks then release by then the system's central resource will keep P_CLKRUN# low. There are three situations that HB1-SE will keep primary clock running. First is bit 2 of clock run control register is set, second there is a pending cycle on going through the chip, third is on behalf of secondary PCI device.

Secondary clock run is enabled by bit 1 of the clock run control register, by default the initiation of stopping/slowing down secondary comes from primary, however if bit 4 of clock run control register is set, secondary clock will be stopped when the bus is idle and there is no cycle from primary bus.

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15 Clocks

This chapter provides information about the clocks.

15.1 Primary and Secondary Clock Inputs

HB1-SE implements a separate clock input for each PCI interface. The primary interface is synchronized to the primary clock input, P_CLK, and the secondary interface is synchronized to the secondary clock input, S_CLK.

15.2 Secondary Clock Outputs

HB1-SE has 5 secondary clock outputs that can be used as clock inputs for up to 4 external secondary bus devices with one feedback to S_CLK.

The rules for using secondary clocks are:

- Each secondary clock output is limited to no more than 2 loads.
- One of the secondary clock outputs must be used for the HB1-SE S_CLK input
- Using an equivalent amount of etch on the board for all secondary clocks is recommended, to minimize skew between them, and a maximum delay of the etch of 2ns.
- Terminating or disabling unused secondary clock outputs is recommended to reduse power dissipation and noise in the system

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16 66-Mhz Operation

HB1-SE66 supports a maximum frequency of 66-Mhz. There are no special procedures necessary to configure HB1-SE66 as a 66Mhz device. Bit 5 of the PCI status register is supported, and shows HB1-SE66 as a 66Mhz capable device to the system. HB1-SE66 does not have an M66EN pin. It is up to the system designer to implement the M66EN connection when using the HB1-SE66.

HB1-SE is a synchronous design, and supports only 1:1 frequency ratio on the primary and secondary bus interfaces.

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17 Miscellaneous Options

17.1 EEPROM Interface

HB1-SE has an interface to EEPROM device. The interface can control an ISSI IS24C02 or compatible part, which is organized as 256X8 bits. The EEPROM is used to initialize the registers. After PRST_L is deasserted, HB1-SE will automatically load data from the EEPROM. The data structure is defined in the following section. The EEPROM interface is organized on 16 bit base in little endian format, and HB1-SE supplies a 7-bit EEPROM word address.

The following pins are used for the EEPROM interface:

- EEPCLK: EEPROM clock output
- EEPDATA: EEPROM bi-directional serial data pin

The HB1-SE does not control the EEPROM address inputs, it can only access EEPROM with address inputs set to 0.

17.1.1 Auto mode EEPROM access

Using auto mode, the HB1-SE can access the EEPROM on a word basis via hardware sequencer. User need only to access word data via HB1-SE configuration registers for EEPROM START control, address, read/write command. Before each access, software should check the Auto Mode Cycle in Progress status before issuing the next START.

17.1.2 EEPROM mode at Reset:

During RESET, the HB1-SE will autoload input for EEPROM automatic load condition. The first offset in the EEPROM contains a signature. If the signature is recognized, register auto-load will commence right after RESET. During the auto-load, HB1-SE will read sequential words from the EEPROM and write to the appropriate registers. Before the HB1-SE registers can be accessed through host, user should check the auto-load condition by reading the EEPAUTO bit. Host access is allowed only after EEPAUTO status becomes '0' which means that the auto load initialization sequence is complete.

17.1.3 EEPROM data structure:

Following the reset, if the condition above is met, HB1-SE will auto-load the register with data from EEPROM. The following table describes the data structure used in EEPROM.

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17.1.4 EEPROM address and Corresponding HB1-SE Register

EEPROM Byte Address	PCI Configuration Offset	Description
00-01h		**EEPROM signature:** Autoload will only proceed if it reads a value of 1516h on the first word loaded. 0x1516=valid signature, otherwise disable autoloading
02h		**Region Enable:** Enables or disables certain regions of the PCI configuration space from being loaded from the EEPROM. Valid combinations are: Bit 0: Reserved Bits 4-1: 0000 = stop autoload at offset 02h 0001 = stop autoload at offset 04h 0011 = stop autoload at offset 07h 0111 = stop autoload at offset 11h 1111 = autoload all EEPROM loadable registers. Other combinations are undefined. Bits7-5: reserved
03h		**Secondary Clock Enable :** Bit0: 1=disable SCLKO[0] output Bit1: 1=disable SCLKO[1] output Bit2: 1=disable SCLKO[2] output Bit3: 1=disable SCLKO[3] output Bit4: 1=disable SCLKO[4] output Bit7-5: Reserved
04h-05h	F0-F1h	**Subsystem Vendor ID**
06h-07h	F2-F3h	**Subsysem ID**
08h-09h	C0-C4	**Miscellaneous** Bit0:register C0h, bit 0 Bits7-1: register C4h, bits 7:1 Bits15-8: register C1h
0Ah-0Bh	00h-01h	**Vendor ID**
0Ch-ODh	02h-03h	**Device ID**
0Eh-0Fh	C3h, 42h	**Miscellaneous** Bits7-0: register 42h Bits15-8: register C3h
10h-11h	82h	**PMC register**
12h-13h	87h	**PMC register** Bits7-0: reserved Bits15-8: register 87h
14h-15h	CDh	**Test Register CDh** Bits7-0: reserved Bits15-8:register CDh

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15h-16h	CEh, CFh	**Test Register CE/CFh** Bits7-0: register CEh Bits11-8: reserved Bits15-8: register CFh, bits 7-4

17.2 General Purpose I/O Interface

The HB1-SE implements a 4-pin general-purpose I/O GPIO interface. Each pin can be configured as input or output through the GPIO control register at offset C5h.

17.3 Vital Product Data

HB1-SE contains the VPD registers as specified in the PCI Local Bus Specification Revision 2.2. The VPD information is stored in the EEPROM device along with the autoload information. HB1-SE provides for storage of 224 bytes of VPD data in the EEPROM device. VPD related registers are located starting at offset A0h of the PCI configuration space. VPD also uses the enhanced capabilities port address mechanism

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18 PCI Power Management

HB1-SE incorporates functionality that meets the requirements of the PCI Power Management Specification, Revision 1.0. These features include:

- PCI power management registers using the enhanced capabilities port (ECP) address mechanism
- Support for D0, $D3_{hot}$ and $D3_{cold}$ power management states
- Support for D0, D1, D2, $D3_{hot}$ and $D3_{cold}$ power management states for devices behind the bridge
- Support of the B2 secondary bus power state when in the $D3_{hot}$ power management state

The table below shows the states and related actions that the HB1-SE performs during power management transitions. (no other transactions are permitted.)

Current State	Next State	Action
D0	$D3_{cold}$	Power has been removed from the HB1-SE. A power-up reset must be performed to bring the HB1-SE to D0.
D0	$D3_{hot}$	If enabled to do so by the BPCCE pin, the HB1-SE will disable the secondary clocks and drive them low.
D0	D2	Unimplemented power state. The HB1-SE will ignore the write to the power state bits (power state remains at D0).
D0	D1	Unimplemented power state. The HB1-SE will ignore the write to the power state bits (power state remains at D0).
$D3_{hot}$	D0	The HB1-SE enables secondary clock outputs and performs an internal chip reset. Signal S_RST_L will not be asserted. All registers will be returned to the reset values and buffers will be cleared.
$D3_{hot}$	$D3_{cold}$	Power has been removed from the HB1-SE. A power-up reset must be performed to bring the HB1-SE to D0.
$D3_{cold}$	D0	Power-up reset. The HB1-SE performs the standard power-up reset functions.

PME# signals are routed from downstream devices around PCI-to PCI bridges. PME# signals do not pass through PCI-PCI bridges.

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19 Hot Swap

HB1-SE incorporates functionality that meets the requirements of the CompactPCI Specification, Rev2.1. HB1-SE is a hotswap friendly device, it contains support for Software Connection Control. The CompactPCI Hot Swap register block is located at PCI configuration offset E4h. The Hot Swap specification allows active insertion and extraction by controlling ENUM_L and LED signals.

HB1-SE has the following hotswap related pins:

- ENUM_L: Signal to notify system of insertion/extraction of hotswap cards.
- LED: Hotswap status light
- EJECT: Indicates HB1-SE of insertion/extraction of hotswap card, should be connected to switch of hotswap card.

19.1 Hotswap Insertion

After reset, HB1-SE will wait for the EJECT pin to be asserted to indicate successful insertion. It will signal the host by asserting ENUM_L. The host reads register 92h, to determine if ENUM_L was asserted as a result of a card insertion. The host will then set bit[7] of the hot swap register to acknowledge the insertion. Software drivers will then perform initialization and deassert ENUM_L after which the HB1-SE will enter normal operation.

19.2 Hotswap Extraction

During the extraction phase, user first has to deassert EJECT by toggling the switch on the hotswap card. HB1-SE will signal the host by asserting ENUM_L. The host will set bit[6] of the configuration register 92h to acknowledge the extraction. HB1-SE deasserts ENUM_L, and waits for the extraction. During the extraction phase, user can optionally cancel the extraction by setting asserting EJECT again.

Note that hot-swap is an independent section of HB1-SE. Its function has no impact on the rest of the chip. If hot-swap feature is not needed, simply leave ENUM_L unconnected.

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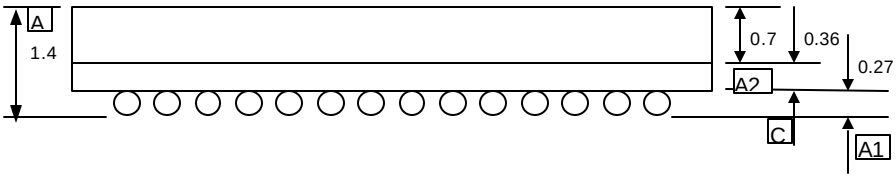
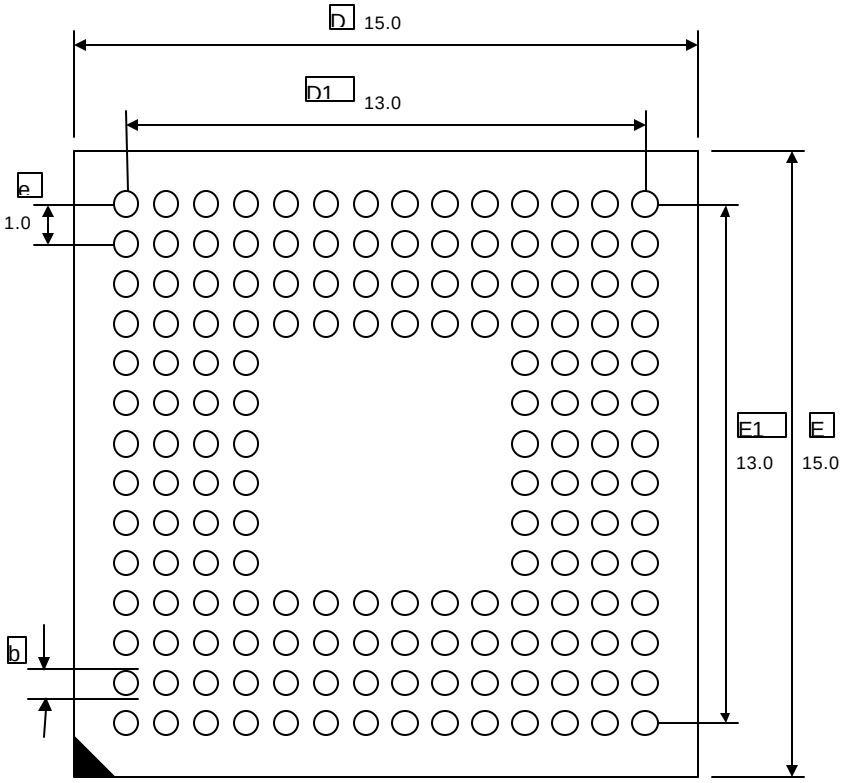
20 Package Specifications

20.1 160-pin Tiny BGA

This specification outlines the mechanical dimensions for 160 pin Tiny BGA package as shown below. All dimensions are in millimeters (mm).



SIDE VIEW



BOTTOM VIEW

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The following table lists the package dimensions in millimeters.

Symbol	Dimension	Minimum	Nominal	Maximum
e	Ball pitch		1.00	
A	Overall package height			1.40
A1	Package standoff height		0.27	
A2	Encapsulation thickness		0.70	
b	Ball diameter	0.35	0.40	0.45
C	Substrate thickness		0.36	
D	Overall package width		15.00	
D1	Overall Encapsulation width		13.00	
E	Overall package width		15.00	
E1	Overall Encapsulation width		13.00	

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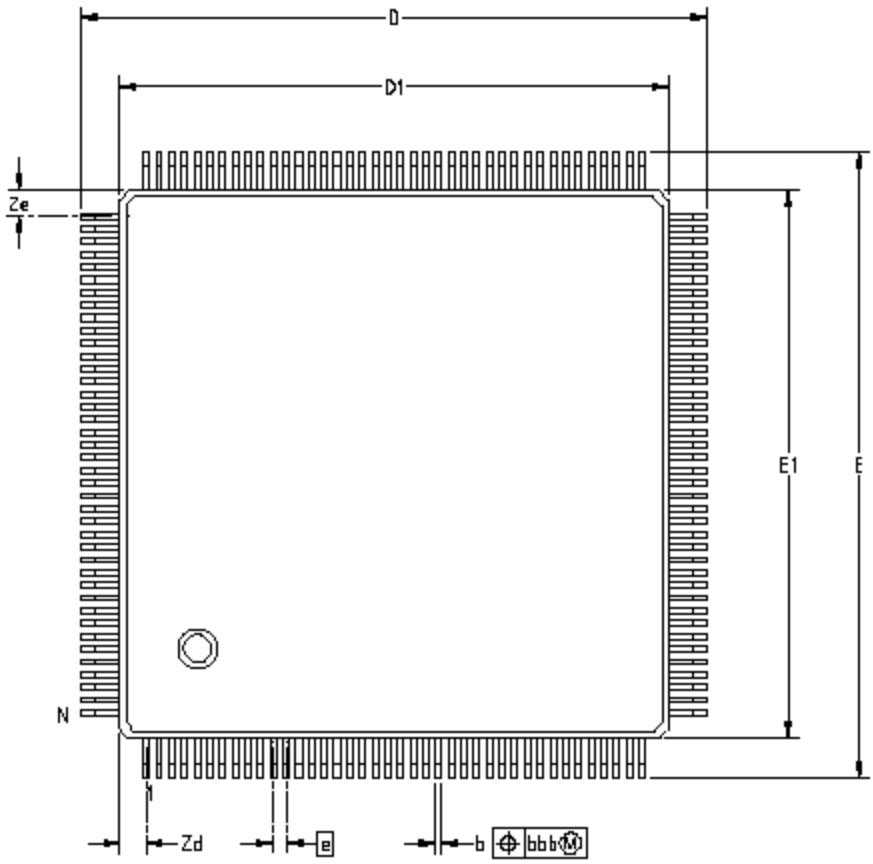
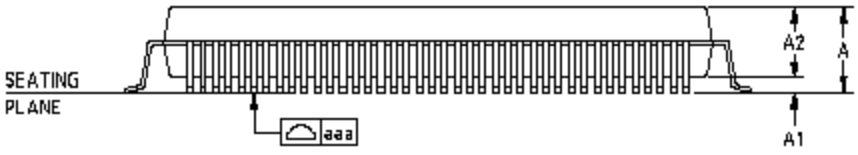
20.2 160-pin Standard PQFP

This specification outlines the mechanical dimensions for 160 pin standard PQFP (plastic quad flat pack) package as shown below. All dimensions are in millimeters (mm).





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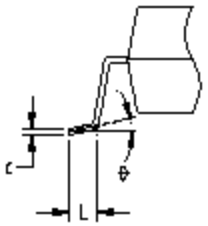

160-pin PQFP package dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	-	-	4.45
A1	0.35	0.45	0.65
A2	3.4	3.6	3.8
b	0.2	0.3	0.4
c	0.10	0.15	0.25
D	31.6	32.0	32.4
D1	27.8	28.0	28.2
E	31.6	32.0	32.4
E1	27.8	28.0	28.2
e	0.65 BSC		
L	0.6	0.8	1.0
Zd	1.325 TYP		
Ze	1.325 TYP		
θ	0°	-	10°
aaa	0.1		
bbb	0.13		
N	160		

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21 Electrical Specifications

21.1 Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested).

Parameter	Minimum	Maximum
Storage Temperature Range	-55 °C	125 °C
Junction Temperature		125 °C
Supply Voltage, V_{DD}		3.9V
Maximum Voltage to signal pins		5.5V
Maximum Power		300mW

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

21.2 Functional Operating Range

Parameter	Minimum	Maximum
Supply Voltage	3.0 V	3.6 V
Operating ambient temperature	0 °C	70 °C

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21.3 DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Max	Unit	Notes
V_{DD}	Supply Voltage		3.0	3.6	V	
V_{IO}	**PVIO, SVIO** pin Interface I/O Voltage		3.0	5.5	V	
V_{ih}	Input HIGH Voltage		0.5 V_{DD}	V_{IO}	V	
V_{il}	Input LOW Voltage		-0.5	0.3 V_{DD}	V	
V_{ol}	Output LOW Voltage	I_{iout} = 1500 μA		0.1 V_{DD}	V	
V_{ol5V}	5V Signalling Output LOW Voltage	I_{iout} = 6 mA		0.1 V_{DD}	V	
V_{oh}	Output HIGH Voltage	I_{iout} = -500 μA	0.9 V_{DD}		V	
V_{oh5V}	5V Signalling Output HIGH Voltage	I_{iout} = -2 mA	2.7		V	
I_{il}	Input Leakage Current	$0 < V_{in} < V_{DD}$		$\pm$10	μA	
C_{in}	Input Pin Capacitance			10.0	pF	
C_{clk}	**CLK** Pin Capacitance		5.0	12.0	pF	
C_{IDSEL}	**IDSEL** Pin Capacitance			8.0	pF	

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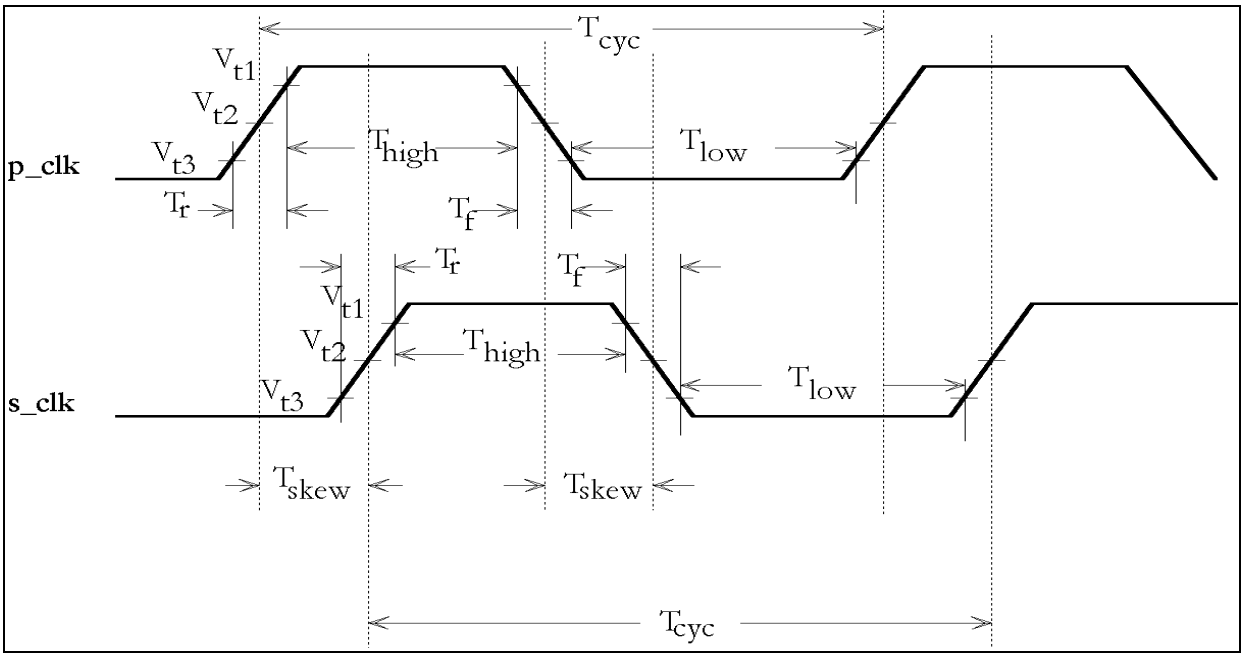
21.4 PCI Clock Signal AC Parameter Measurements



NOTE: V_{t1} - 2.0V for 5V clocks; 0.5VCC for 3.3V clocks
V_{t2} - 1.5V for 5V clocks; 0.4VCC for 3.3V clocks
V_{t3} – 0.8V for 5V clocks; 0.3VCC for 3.3V clocks

21.4.1 33MHz PCI Clock Signal AC parameters

Symbol	Parameter	Minimum	Maximum	Unit
T_{cyc}	PCLK, SCLK cycle time	30		ns
T_{high}	PCLK, SCLK high time	11	-	ns
T_{low}	PCLK, SCLK low time	11	-	ns
	PCLK, SCLK slew rate	1	4	V/ns
T_{sclk}	Delay from PCLK to SCLK	0	7	ns
T_{sclkr}	PCLK rising to SCLKO rising	0	5	ns
T_{sclkf}	PCLK falling to SCLKO falling	0	5	
T_{skew}	SCLKO[x] to SCLKO[y]	-	0.500	ns

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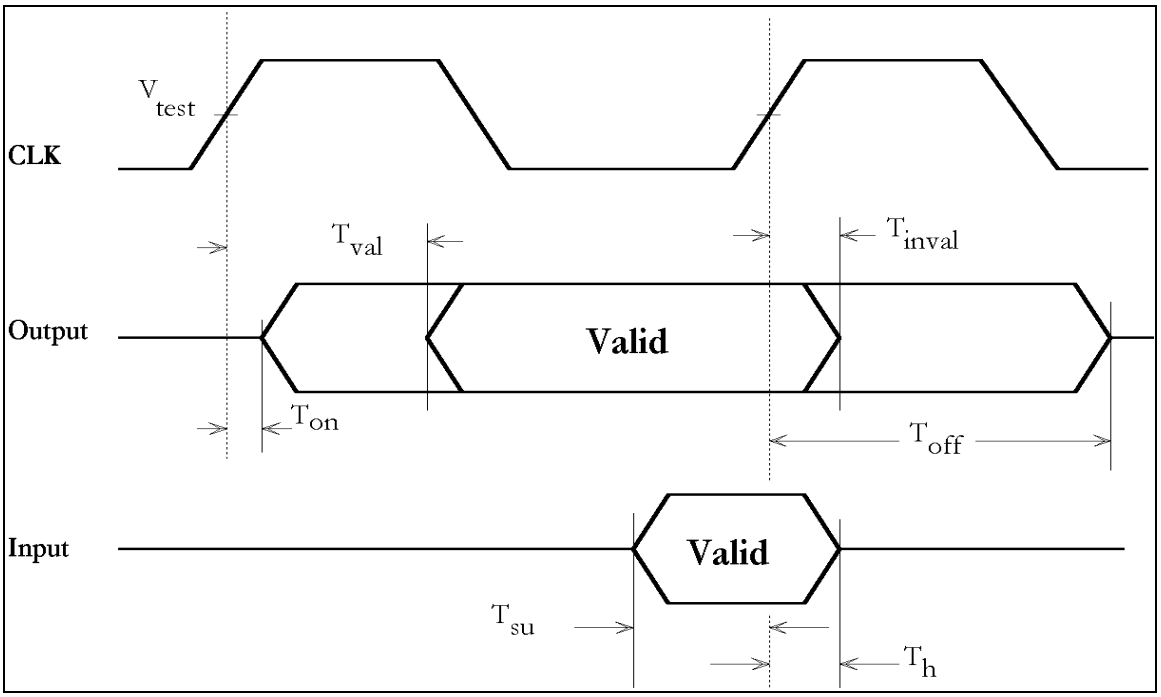
21.4.2 66MHz PCI Clock Signal AC parameters

Symbol	Parameter	Minimum	Maximum	Unit
T_{cyc}	PCLK, SCLK cycle time	15	30	ns
T_{high}	PCLK, SCLK high time	6	-	ns
T_{low}	PCLK, SCLK low time	6	-	ns
	PCLK, SCLK slew rate	1.5	4	V/ns
T_{sclk}	Delay from PCLK to SCLK	0	5	ns
T_{sclkr}	PCLK rising to SCLKO rising	0	5	ns
T_{sclkf}	PCLK falling to SCLKO falling	0	5	
T_{skew}	SCLKO[x] to SCLKO[y]	-	0.500	ns

21.5 PCI Signal Timing Specification



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21.5.1 33MHz PCI Signal Timing

Symbol	Parameter	Minimum	Maximum	Unit
T_{val}	CLK to signal valid delay - bused signals	2	11	ns
$T_{val(ptp)}$	CLK to signal valid delay – point to point	2	12	ns
T_{on}	Float to active delay	2	-	ns
T_{off}	Active to float delay	-	28	ns
T_{su}	Input setup time to CLK – bused signals	7	-	ns
$T_{su(ptp)}$	Input setup time to CLK – point to point	10,12	-	
T_{h}	Input signal hold time from CLK	0	-	ns

21.5.2 66MHz PCI Signal Timing

Symbol	Parameter	Minimum	Maximum	Unit
T_{val}	CLK to signal valid delay - bused signals	2	6	ns
$T_{val(ptp)}$	CLK to signal valid delay – point to point	2	6	ns
T_{on}	Float to active delay	2	-	ns
T_{off}	Active to float delay	-	14	ns
T_{su}	Input setup time to CLK – bused signals	3	-	ns
$T_{su(ptp)}$	Input setup time to CLK – point to point	5	-	
T_{h}	Input signal hold time from CLK	0	-	ns

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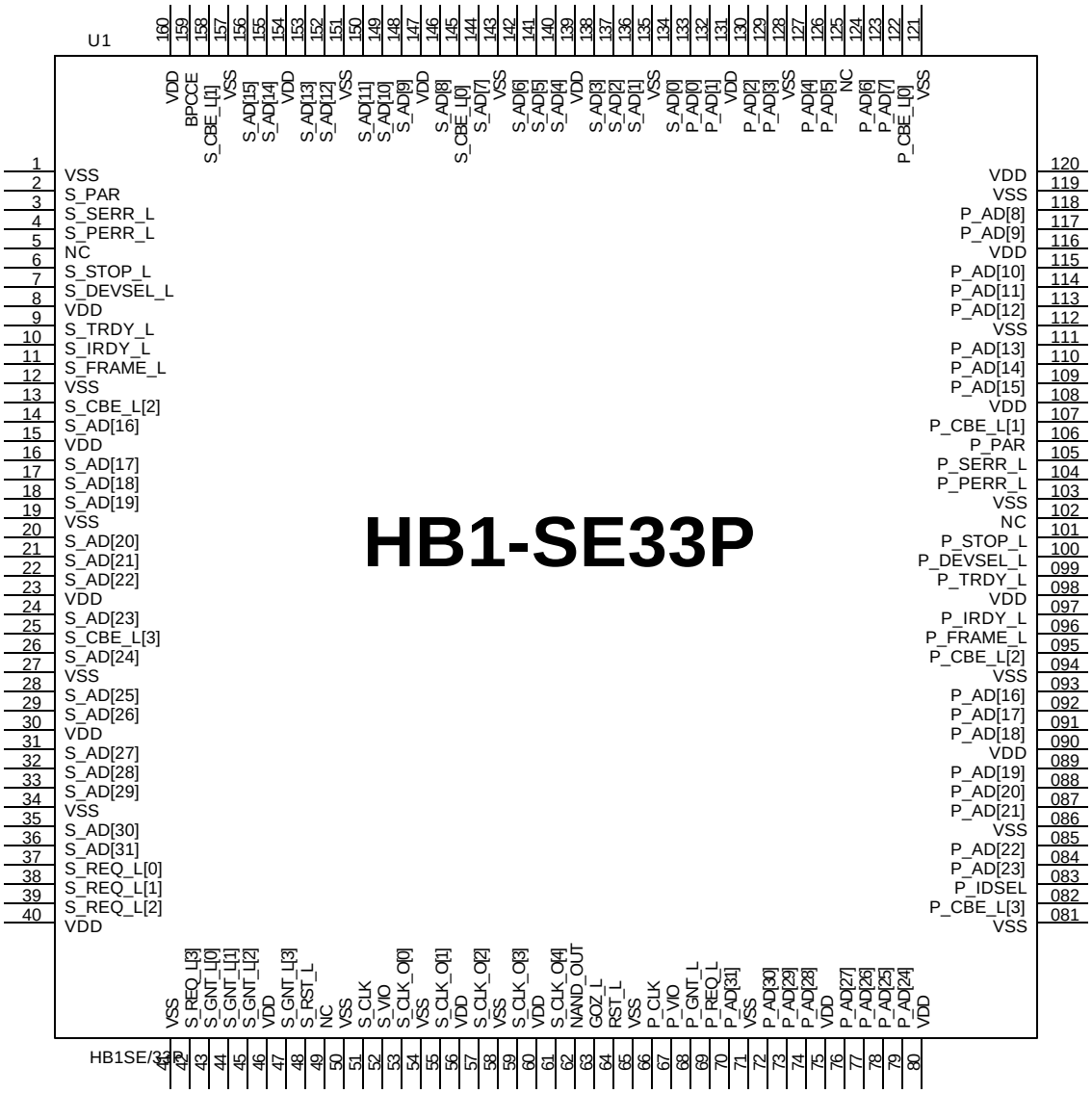
Appendix A: HB1-SE33P Part Description

Part number HB1-SE33P is a 160 pin PQFP, designed to be a replacement part for Intel 21152 Bridge. It is in a separate section, because even though it is HB1-SE33 internally, some pins, and therefore some HB1-SE functions are not available in this configuration. This section will highlight these features.



Pin Diagram, Top View

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HB1-SE33P 160 pin pinout

HB1-SE33P does not support the following pins:

ENUM_L
L_STAT
EEPD
EEPCLK
GPIO[0]
GPIO[1]
GPIO[2]
GPIO[3]
P_CLKRUN_L
S_CLKRUN_L
EJECT

Thus, all functions associated with this pins, such as hotswap, power management, EEPROM, VPD, and GPIO are not supported in this configuration.

Pin Assignment Sorted by Location

Location	Pin Name	Type
001	VSS	P
002	S_PAR	TS
003	S_SERR_L	I
004	S_PERR_L	TS
005	NC	
006	S_STOP_L	STS
007	S_DEVSEL_L	STS
008	VDD	P
009	S_TRDY_L	STS
010	S_IRDY_L	STS
011	S_FRAME_L	STS
012	VSS	P
013	S_CBE_L[2]	TS
014	S_AD[16]	TS
015	VDD	P
016	S_AD[17]	TS
017	S_AD[18]	TS
018	S_AD[19]	TS
019	VSS	TS
020	S_AD[20]	TS
021	S_AD[21]	TS
022	S_AD[22]	TS
023	VDD	P
024	S_AD[23]	TS
025	S_CBE_L[3]	TS
026	S_AD[24]	TS
027	VSS	P
028	S_AD[25]	TS
029	S_AD[26]	TS
030	VDD	P
031	S_AD[27]	TS
032	S_AD[28]	TS
033	S_AD[29]	TS
034	VSS	P
035	S_AD[30]	TS
036	S_AD[31]	TS
037	S_REQ_L[0]	I
038	S_REQ_L[1]	I
039	S_REQ_L[2]	I
040	VDD	P
041	VSS	P
042	S_REQ_L[3]	I
043	S_GNT_L[0]	I
044	S_GNT_L[1]	O
045	S_GNT_L[2]	O
046	VDD	P
047	S_GNT_L[3]	I
048	S_RST_L	O
049	NC	
050	VSS	P
051	S_CLK	I
052	S_VIO	I
053	S_CLK_O[0]	O
054	VSS	P
055	S_CLK_O[1]	O

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056	VDD	P
057	S_CLK_O[2]	O
058	VSS	P
059	S_CLK_O[3]	O
060	VDD	P
061	S_CLK_O[4]	O
062	NAND_OUT	O
063	GOZ_L	I
064	RST_L	I
065	VSS	P
066	P_CLK	I
067	P_VIO	I
068	P_GNT_L	I
069	P_REQ_L	O
070	P_AD[31]	TS
071	VSS	P
072	P_AD[30]	TS
073	P_AD[29]	TS
074	P_AD[28]	TS
075	VDD	P
076	P_AD[27]	TS
077	P_AD[26]	TS
078	P_AD[25]	TS
079	P_AD[24]	TS
080	VDD	P
081	VSS	P
082	P_CBE_L[3]	TS
083	P_IDSEL	I
084	P_AD[23]	TS
085	P_AD[22]	TS
086	VSS	P
087	P_AD[21]	TS
088	P_AD[20]	TS
089	P_AD[19]	TS
090	VDD	P
091	P_AD[18]	TS
092	P_AD[17]	TS
093	P_AD[16]	TS
094	VSS	P
095	P_CBE_L[2]	STS
096	P_FRAME_L	STS
097	P_IRDY_L	STS
098	VDD	P
099	P_TRDY_L	STS
100	P_DEVSEL_L	STS
101	P_STOP_L	STS
102	NC	

103	VSS	P
104	P_PERR_L	STS
105	P_SERR_L	OD
106	P_PAR	TS
107	P_CBE_L[1]	TS
108	VDD	P
109	P_AD[15]	TS
110	P_AD[14]	TS
111	P_AD[13]	TS
112	VSS	P
113	P_AD[12]	TS
114	P_AD[11]	TS
115	P_AD[10]	TS
116	VDD	P
117	P_AD[09]	TS
118	P_AD[08]	TS
119	VSS	P
120	VDD	P
121	VSS	P
122	P_CBE_L[0]	TS
123	P_AD[07]	TS
124	P_AD[06]	TS
125	NC	
126	P_AD[05]	TS
127	P_AD[04]	TS
128	VSS	P
129	P_AD[03]	TS
130	P_AD[02]	TS
131	VDD	P
132	P_AD[01]	TS
133	P_AD[00]	TS
134	S_AD[00]	TS
135	VSS	P
136	S_AD[01]	TS
137	S_AD[02]	TS
138	S_AD[03]	TS
139	VDD	P
140	S_AD[04]	TS
141	S_AD[05]	TS
142	S_AD[06]	TS
143	VSS	P
144	S_AD[07]	TS
145	S_CBE_L[0]	TS
146	S_AD[08]	TS
147	VDD	P
148	S_AD[09]	TS
149	S_AD[10]	TS

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150	S_AD[11]	TS
151	VSS	P
152	S_AD[12]	TS
153	S_AD[13]	TS
154	VDD	P
155	S_AD[14]	TS

156	S_AD[15]	TS
157	VSS	P
158	S_CBE_L[1]	TS
159	BPCCE	I
160	VDD	P

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Pin Assignment Sorted by Signal Name

Location	Pin Name	Type
159	BPCCE	I
063	GOZ_L	I
062	NAND_OUT	O
005	NC	
049	NC	
102	NC	
125	NC	
133	P_AD[00]	TS
132	P_AD[01]	TS
130	P_AD[02]	TS
129	P_AD[03]	TS
127	P_AD[04]	TS
126	P_AD[05]	TS
124	P_AD[06]	TS
123	P_AD[07]	TS
118	P_AD[08]	TS
117	P_AD[09]	TS
115	P_AD[10]	TS
114	P_AD[11]	TS
113	P_AD[12]	TS
111	P_AD[13]	TS
110	P_AD[14]	TS
109	P_AD[15]	TS
093	P_AD[16]	TS
092	P_AD[17]	TS
091	P_AD[18]	TS
089	P_AD[19]	TS
088	P_AD[20]	TS
087	P_AD[21]	TS
085	P_AD[22]	TS
084	P_AD[23]	TS
079	P_AD[24]	TS
078	P_AD[25]	TS
077	P_AD[26]	TS
076	P_AD[27]	TS
074	P_AD[28]	TS
073	P_AD[29]	TS
072	P_AD[30]	TS
070	P_AD[31]	TS
122	P_CBE_L[0]	TS
107	P_CBE_L[1]	TS
095	P_CBE_L[2]	STS
082	P_CBE_L[3]	TS
066	P_CLK	I
100	P_DEVSEL_L	STS
096	P_FRAME_L	STS
068	P_GNT_L	I
083	P_IDSEL	I
097	P_IRDY_L	STS
106	P_PAR	TS
104	P_PERR_L	STS
069	P_REQ_L	O
105	P_SERR_L	OD
101	P_STOP_L	STS
099	P_TRDY_L	STS
067	P_VIO	I
064	RST_L	I
134	S_AD[00]	TS
136	S_AD[01]	TS
137	S_AD[02]	TS
138	S_AD[03]	TS
140	S_AD[04]	TS
141	S_AD[05]	TS
142	S_AD[06]	TS
144	S_AD[07]	TS
146	S_AD[08]	TS
148	S_AD[09]	TS
149	S_AD[10]	TS
150	S_AD[11]	TS
152	S_AD[12]	TS
153	S_AD[13]	TS
155	S_AD[14]	TS
156	S_AD[15]	TS
014	S_AD[16]	TS
016	S_AD[17]	TS
017	S_AD[18]	TS
018	S_AD[19]	TS
020	S_AD[20]	TS
021	S_AD[21]	TS
022	S_AD[22]	TS
024	S_AD[23]	TS
026	S_AD[24]	TS
028	S_AD[25]	TS
029	S_AD[26]	TS
031	S_AD[27]	TS
032	S_AD[28]	TS
033	S_AD[29]	TS
035	S_AD[30]	TS
036	S_AD[31]	TS
145	S_CBE_L[0]	TS
158	S_CBE_L[1]	TS

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013	S_CBE_L[2]	TS
025	S_CBE_L[3]	TS
051	S_CLK	I
053	S_CLK_O[0]	O
055	S_CLK_O[1]	O
057	S_CLK_O[2]	O
059	S_CLK_O[3]	O
061	S_CLK_O[4]	O
007	S_DEVSEL_L	STS
011	S_FRAME_L	STS
043	S_GNT_L[0]	I
044	S_GNT_L[1]	O
045	S_GNT_L[2]	O
047	S_GNT_L[3]	I
010	S_IRDY_L	STS
002	S_PAR	TS
004	S_PERR_L	TS
037	S_REQ_L[0]	I
038	S_REQ_L[1]	I
039	S_REQ_L[2]	I
042	S_REQ_L[3]	I
048	S_RST_L	O
003	S_SERR_L	I
006	S_STOP_L	STS
009	S_TRDY_L	STS
052	S_VIO	I
116	VDD	P
008	VDD	P
015	VDD	P
023	VDD	P
030	VDD	P
040	VDD	P
046	VDD	P
056	VDD	P
060	VDD	P

075	VDD	P
080	VDD	P
090	VDD	P
098	VDD	P
108	VDD	P
120	VDD	P
131	VDD	P
139	VDD	P
147	VDD	P
154	VDD	P
160	VDD	P
119	VSS	P
157	VSS	P
001	VSS	P
012	VSS	P
019	VSS	TS
027	VSS	P
034	VSS	P
041	VSS	P
050	VSS	P
054	VSS	P
058	VSS	P
065	VSS	P
071	VSS	P
081	VSS	P
086	VSS	P
094	VSS	P
103	VSS	P
112	VSS	P
121	VSS	P
128	VSS	P
135	VSS	P
143	VSS	P
151	VSS	P

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HB1-SE33P/21152 pinout comparison

This section describes pinout differences between the Intel 21152 and HB1-SE33P and some the design considerations for using the HB1-SE33P.

Pin No.	Intel 21152	HiNT HB1-SE33P	Notes
5	s_lock_l	N/C[1]	The HB1-SE33P does not support the PCI lock mechanism on its secondary interface. [2]
49	s_cfn_l	N/C	The s_cfn_l pin specifies whether 21152 uses internal or external arbitration. HB1-SE33P only supports internal arbitration, so will only function correctly in designs that do not use an external arbiter.
102	p_lock_l	N/C	The HB1-SE33P does not support the PCI lock mechanism on its primary interface. [3]
125	vdd	N/C	This is a power pin, and has no effect on operation.

[1] N/C: No Connect.
[2,3] In most cases, this will not present a problem, as very few devices implement lock functionality.

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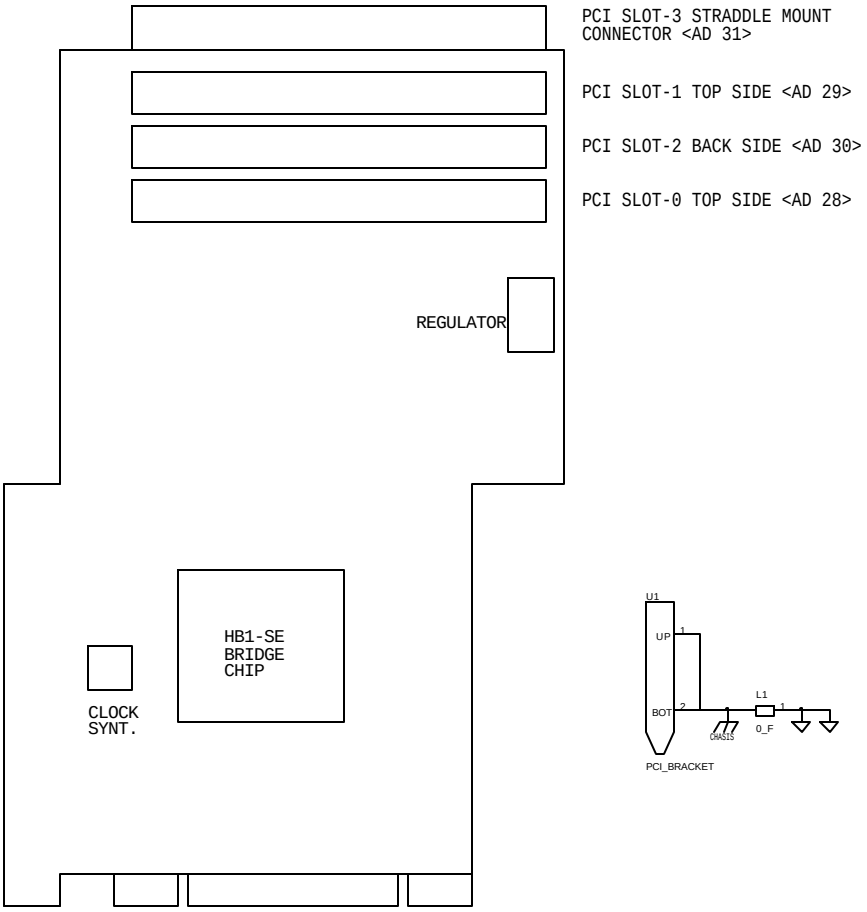
Appendix B : Sample Schematics

HiNT HB1-SE PCI-PCI BRIDGE DEMO BOARD

PAGE	FUNCTIONAL DESCRIPTION
1.	COVER
2.	HB1-SE PCI-PCI BRIDGE
3.	PCI BUS GOLD FINGER
4.	PCI SLOT 0 and 1
5.	PCI SLOT 2 and 3
6.	PCI SLOT 4
7.	POWER

REVISION HISTORY:
REV. B 3/22/00.

FEATURES:
- 4 PCI SLOTs



ORCAD Capture for Windows - Ver. 9.00.1153

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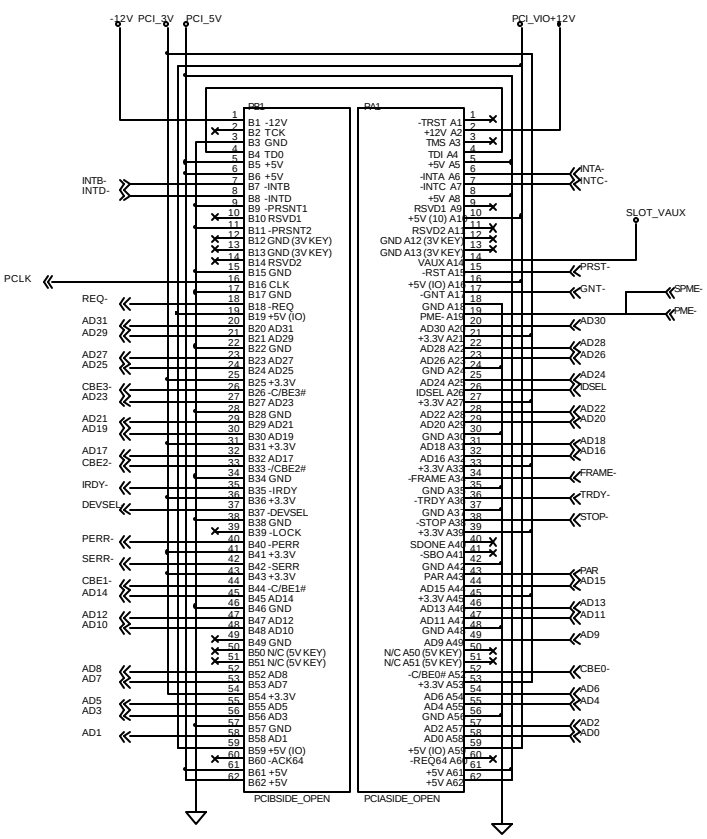
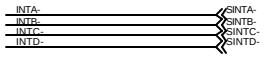


GOLD FINGER



THIS IS AN UNVERIFIED EXAMPLE
PLEASE CHECK FOR POSSIBLE MISTAKES
HINT DOES NOT ASSUME ANY RESPONSIBILIT
OR LIABILITY OUT OF THIS APPLICATION

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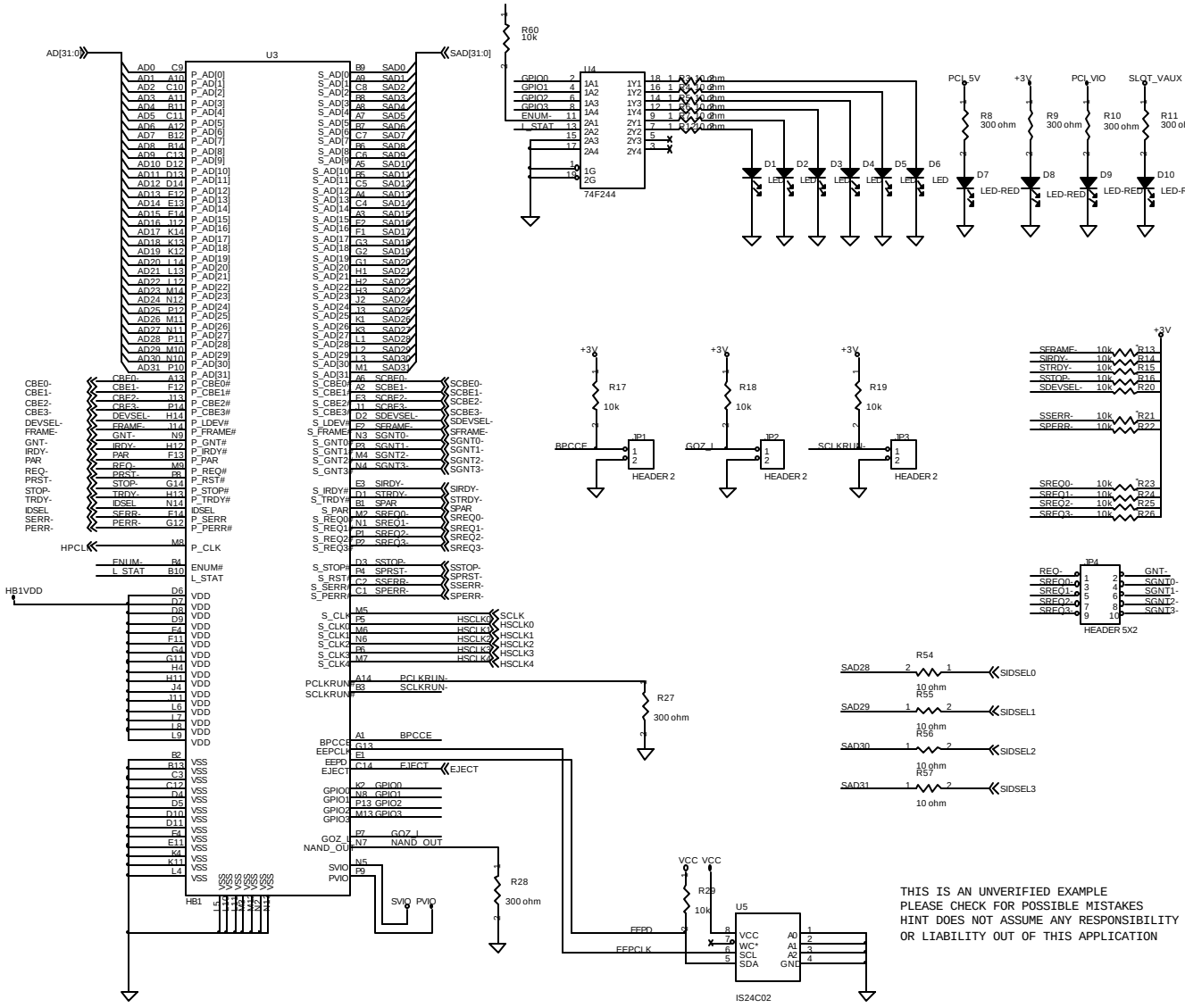

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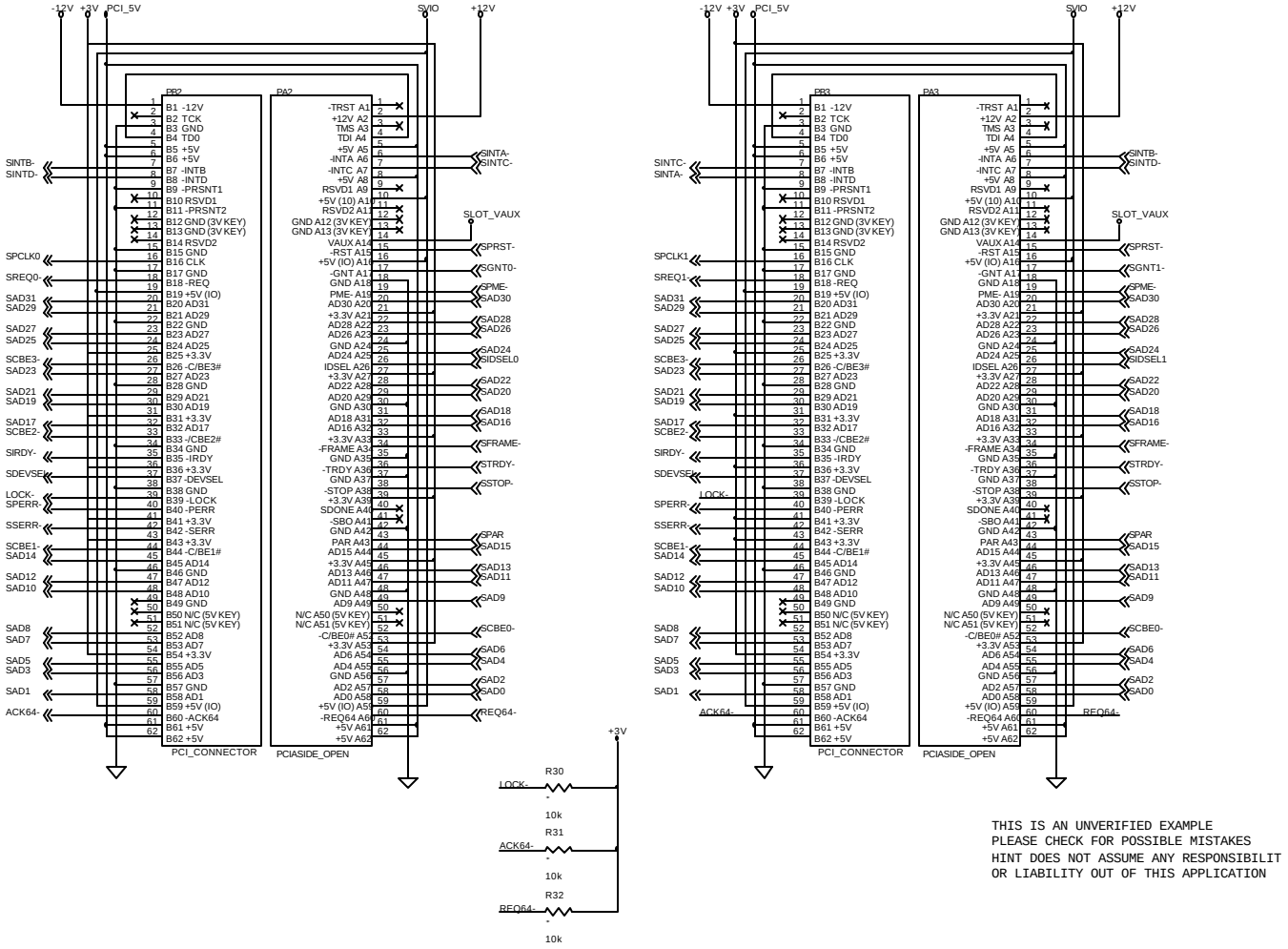
PCI SLOT 0

PCI SLOT 1



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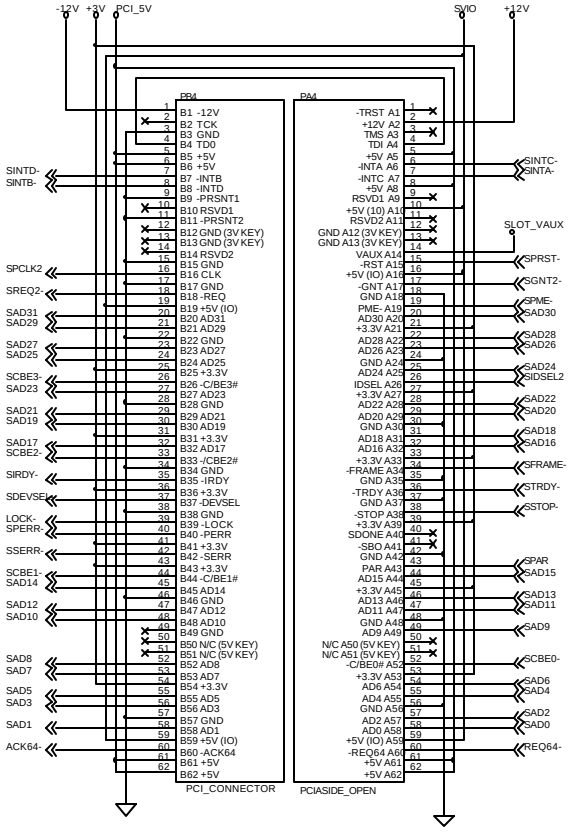
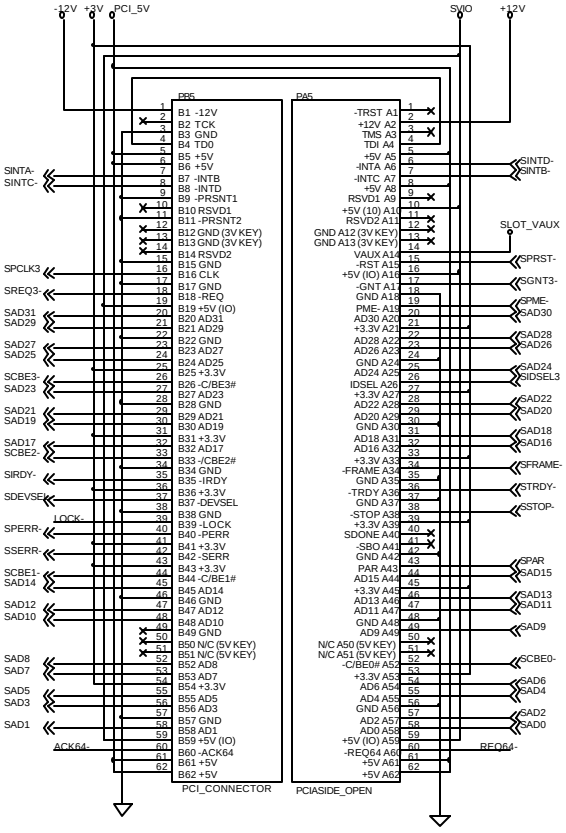
PCI SLOT 2



PCI SLOT 3



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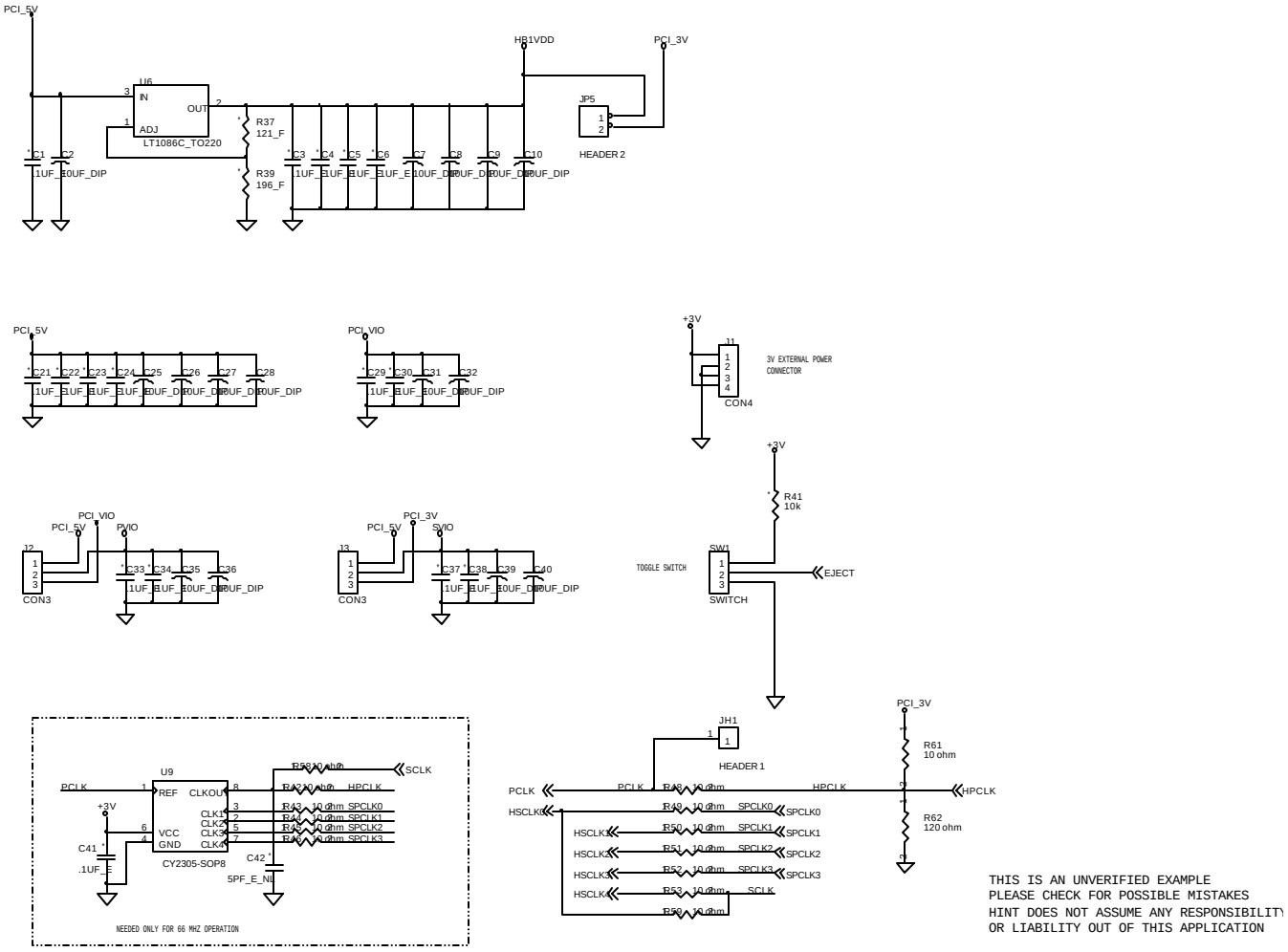

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Appendix C: Application Notes

HB1-SE66 Application Note 1: Connecting HB1-SE66 to the AGP interface

Introduction

HB1-SE66 is a 32-bit 66MHz PCI to PCI bridge for high performance designs. This application note describes how to utilize the existing AGP interface a 66MHz PCI slot and implement a 66MHz PCI add-in card design with multiple PCI devices. HB1-SE66 can be used behind the AGP interface to bridge the PCI devices.

The AGP interface specification uses the 66MHz PCI specification as an operational baseline, and provides extensions to it. As such, it is possible to connect a purely PCI device behind the AGP connector, as all PCI signals are supported by the interface. However, AGP interface is optimized for a point to point topology, so only 1 device can be connected to the interface.

HB1-SE66 can provide the electrical isolation and arbitration necessary to connect more than one 66MHz PCI device to the AGP interface.

Typical Applications

One application would be for a graphics adapter with multiple monitor support, using multiple AGP devices (running as PCI). Most computers do not have 66MHz PCI slots, so this is the simplest way to implement existing AGP chips in multiple configurations.

Applications are not limited to graphics chips or AGP devices. Other PCI devices can also be connected in this way.

Design Consideration

Since AGP was designed for a single device only, there is no IDSEL pin for configuration. For most systems, it is assumed that the AGP device uses AD[16]. When connecting the HB1-SE66, its primary IDSEL pin should therefore be connected to AD[16] of the AGP interface. On the secondary side, this presents the same problem when connecting more than one AGP device. The solution to this issue is implementation specific, and is left to the system designer.

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Appendix D: Timing Diagrams

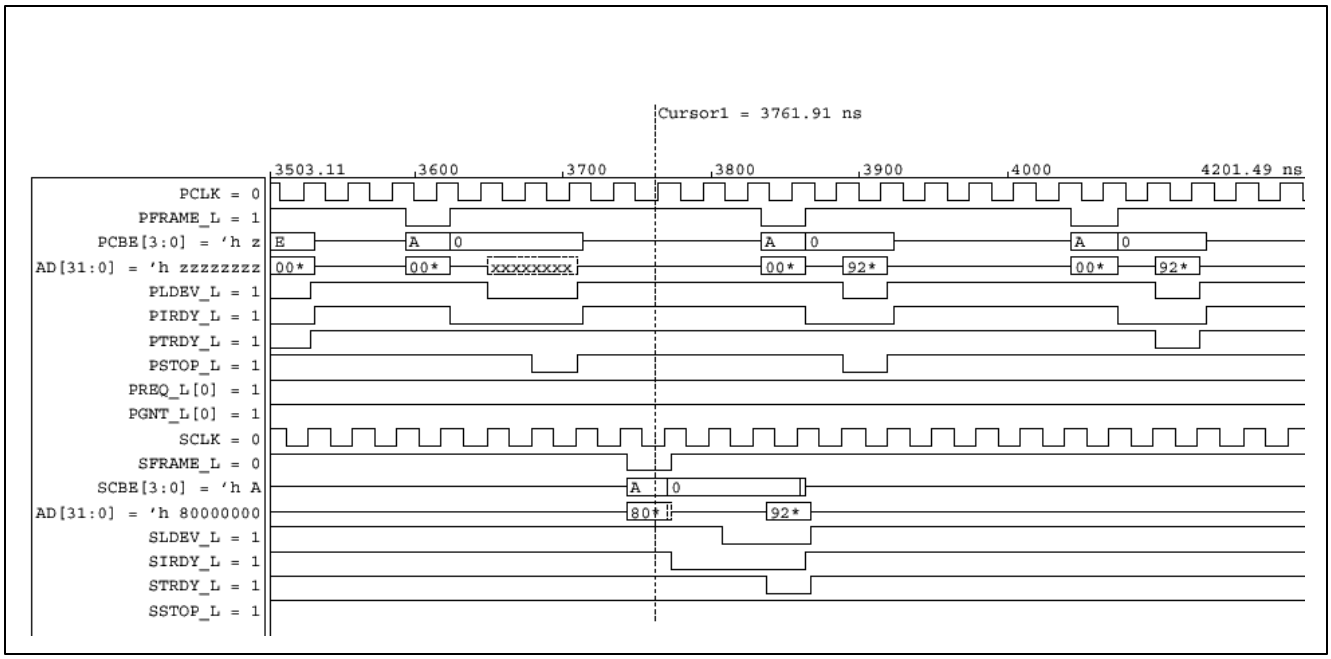

Figure 1 : Primary to Secondary Type 1 to Type 0 Configuration Cycle conversion.

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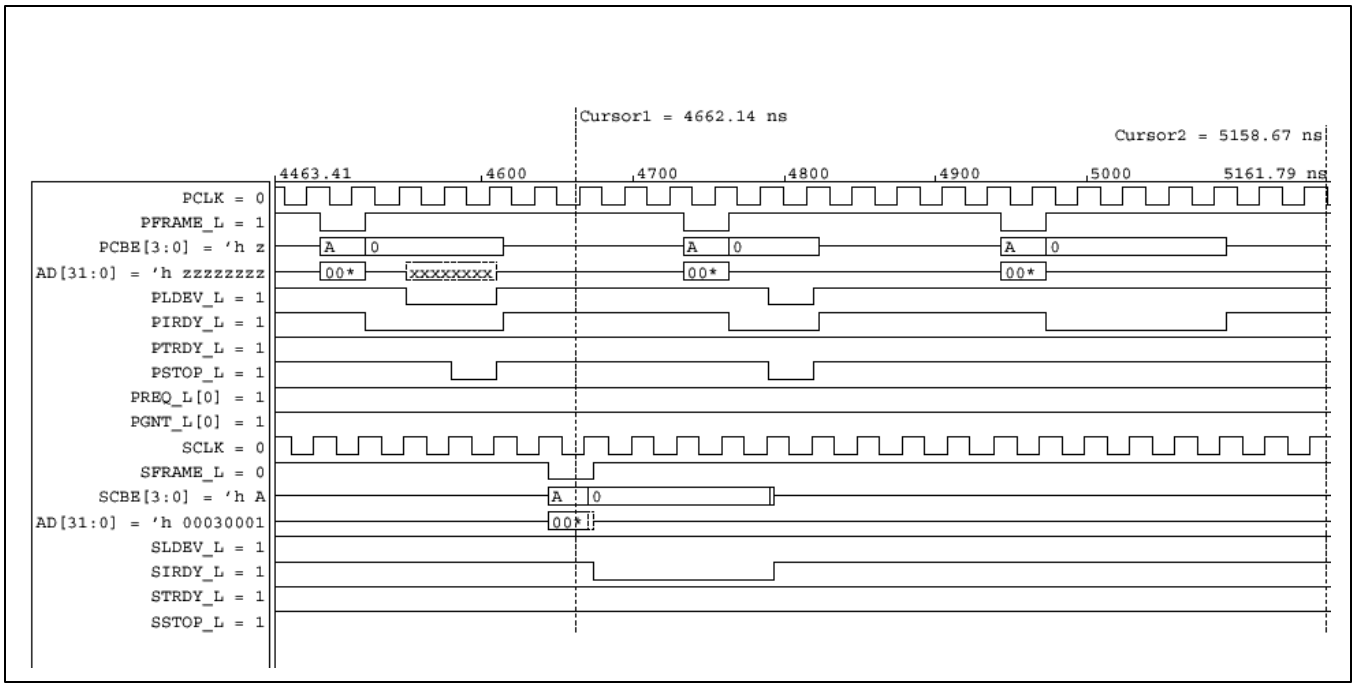

Figure 2 : Primary to Secondary Type 1 to Type 1 Configuration Cycle passing.

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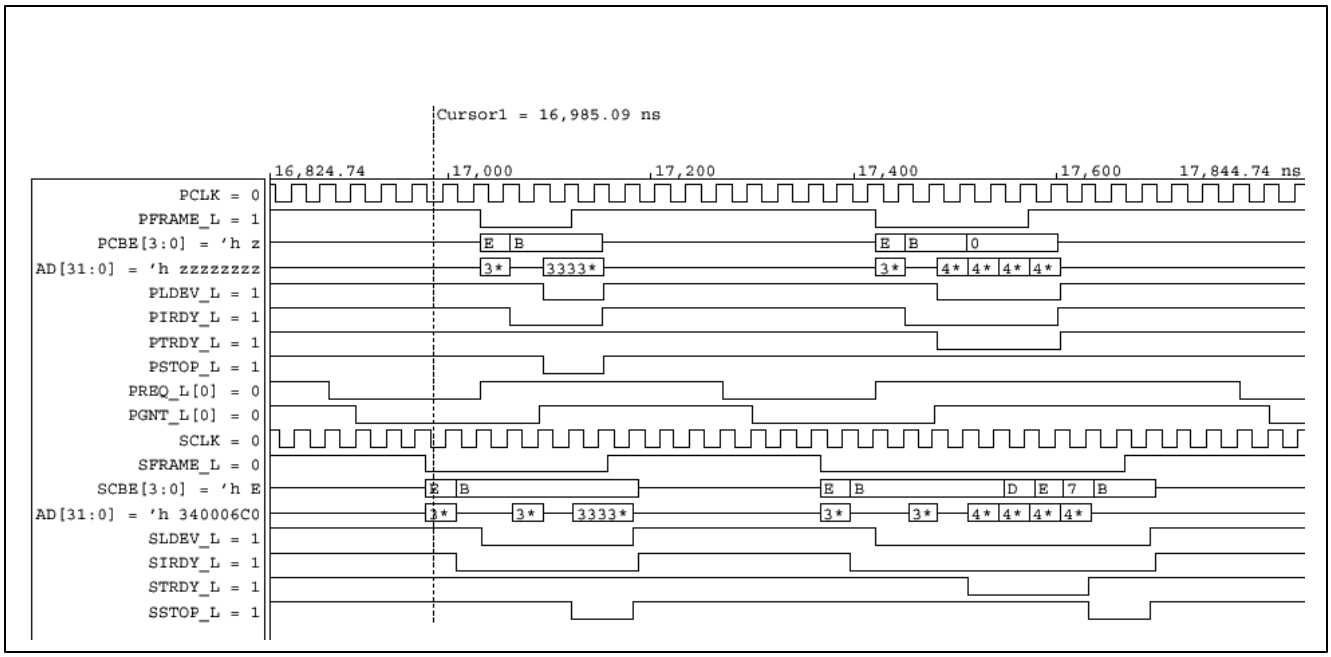

Figure 3 : Secondary to Primary Memory Read Line transaction.

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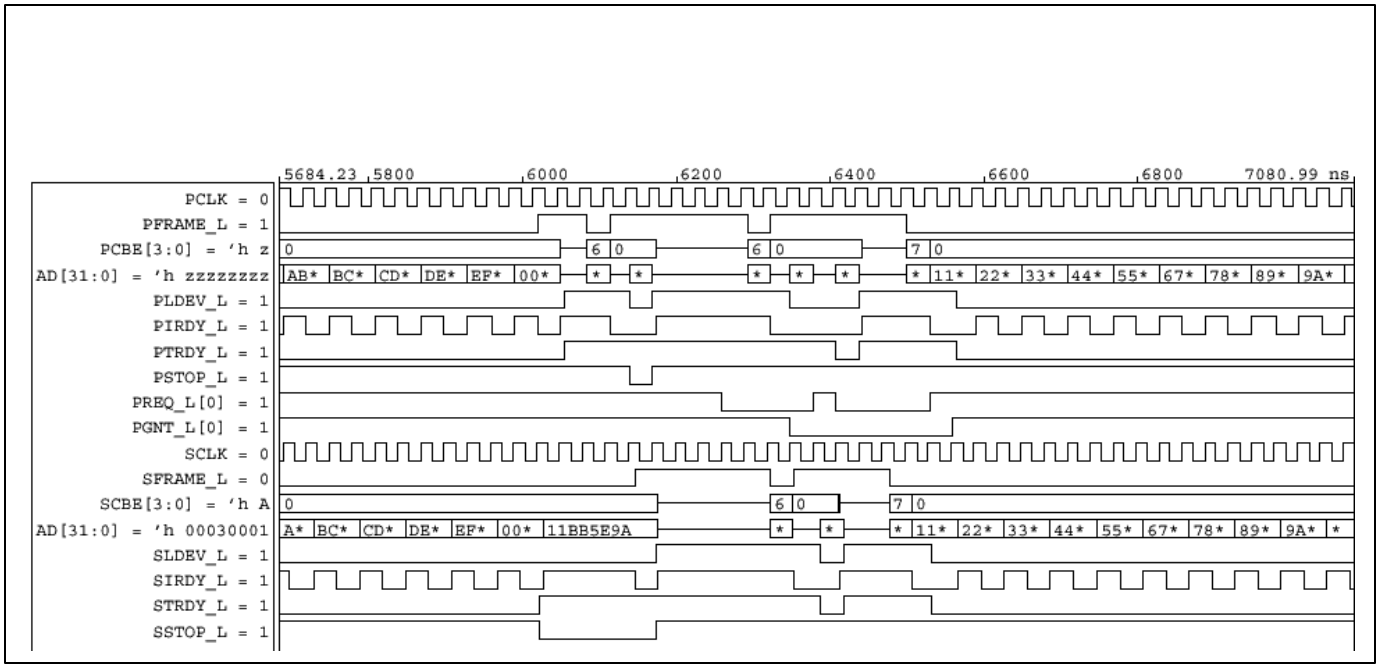

Figure 4 : Primary to Secondary Memory Read transaction.

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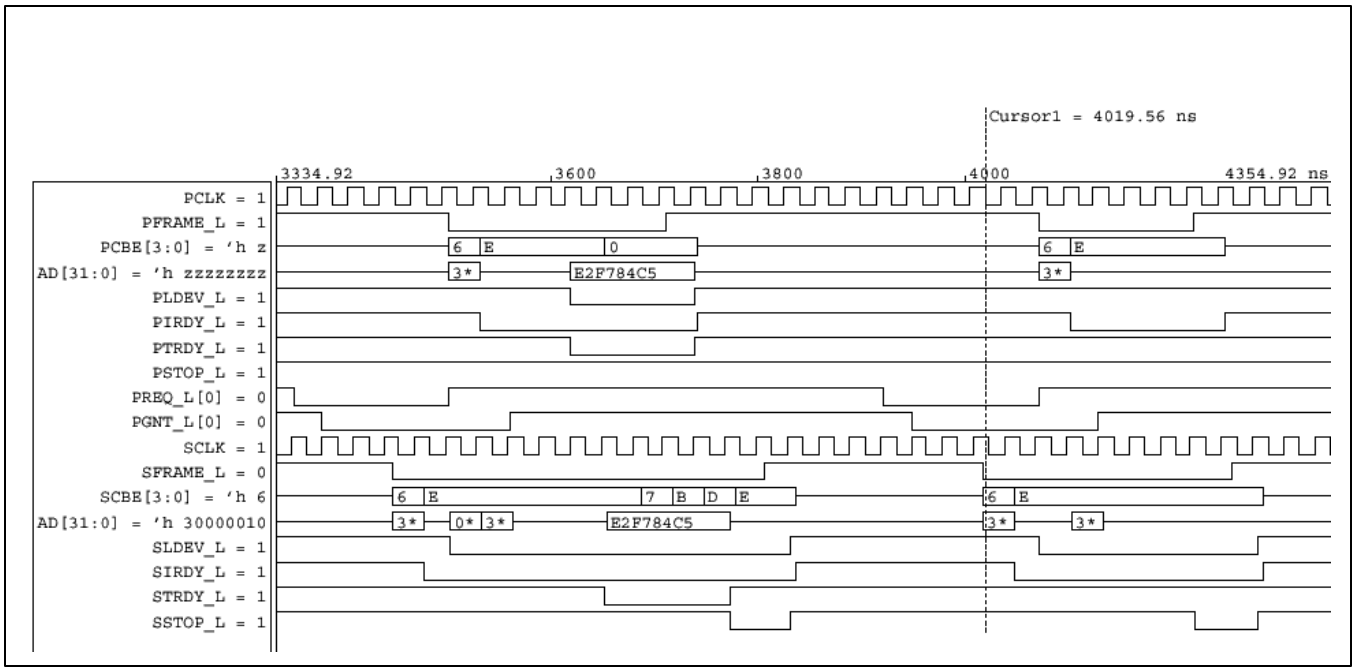

Figure 5 : Secondary to Primary Memory Read transaction.

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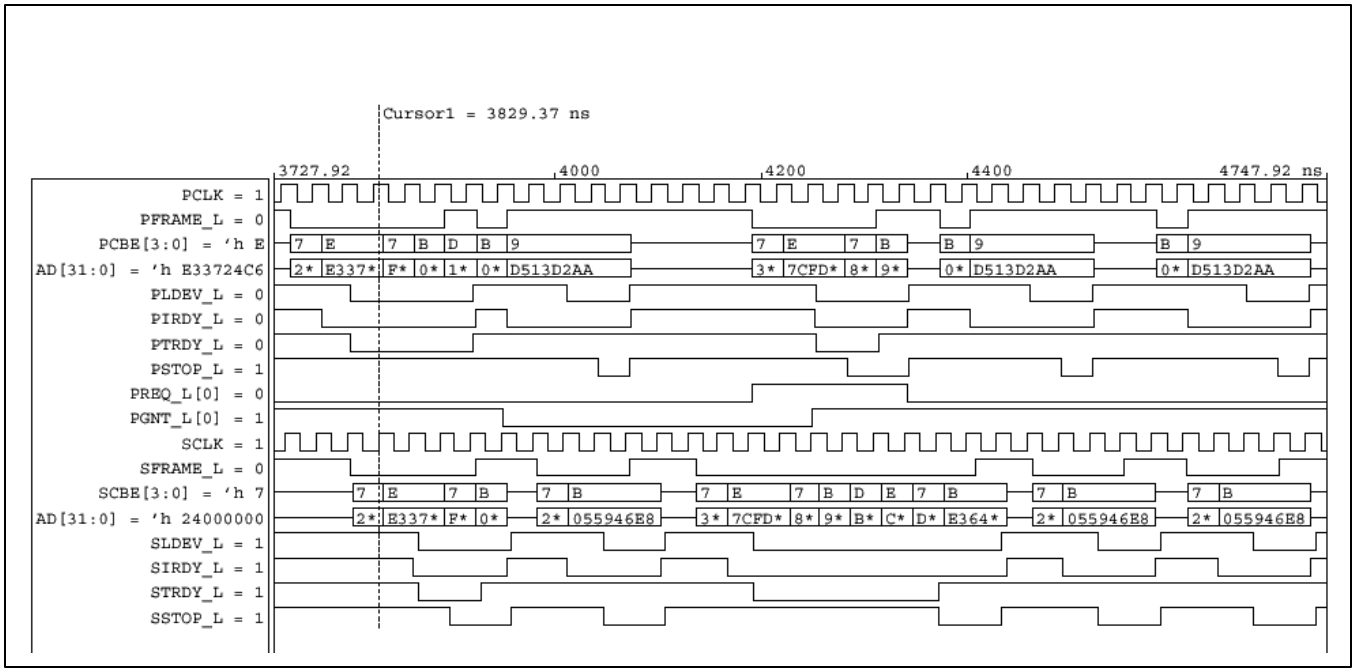

Figure 6 : Primary to Secondary Memory Write transaction followed by Secondary to Primary Memory Write transaction.

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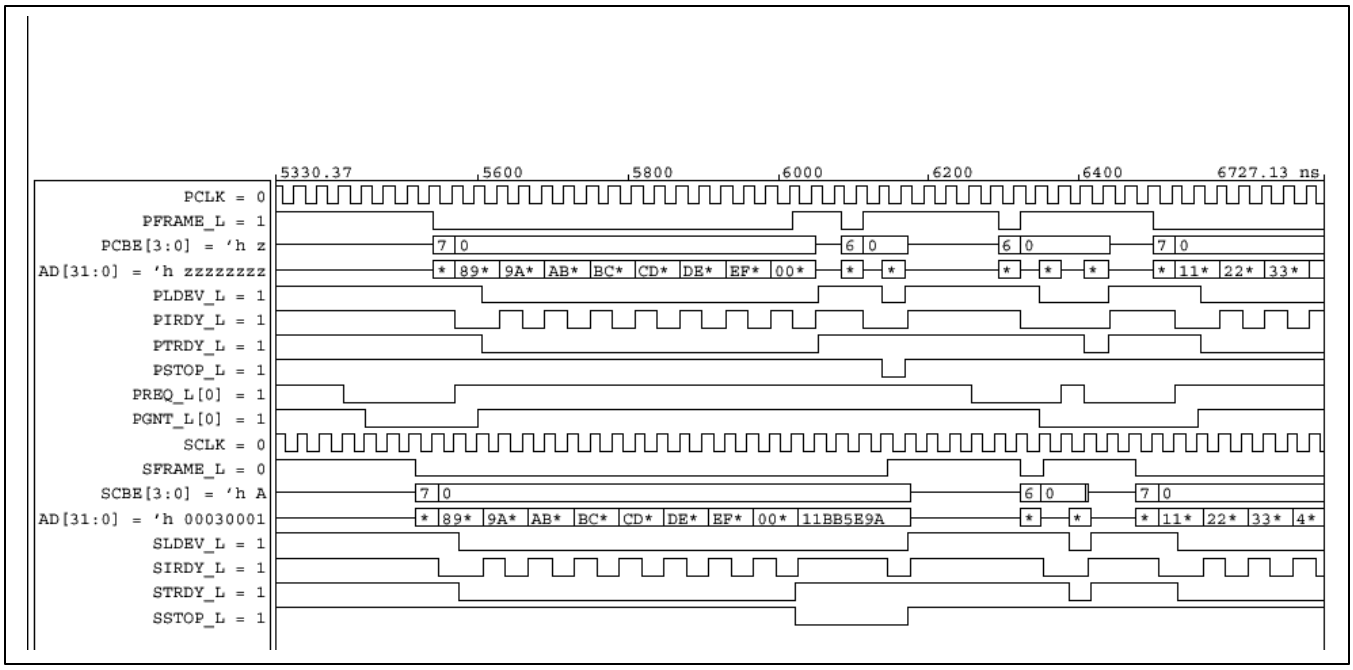

Figure 7 : Secondary to Primary Memory Write transaction.

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