FW533

PCI Express® 1394a PHY/Link Open Host Controller Interface

Product Brief

Introduction

The Agere Systems FW533 is specifically designed for PCI Express. It combines an OHCI (open host controller interface) with Agere's *TrueFIRE*™ technology and a high-performance, standards-compliant *PCI Exress* 1.0a host system interface in a small footprint and with low power dissipation.

Multiple VCs (virtual channels) on the *PCI Express* link provide native support for QoS (quality of service) transmission for real-time and multimedia applications in a standards-based framework, ensuring compatibility with current and future operating systems. Active-state power management allows dynamic power management during periods of reduced network activity.

The FW533 is composed of the following major functional sections:

- *PCI Express* subsystem, consisting of PHY, link, and transport layers.
- OHCI core with isochronous and asynchronous DMA engines.
- 1394a link core.
- 1394a PHY core with three bilingual 1394a ports.

Features

Core

- Single-chip link and PHY enables smaller, simpler, more efficient motherboard, and add-in card designs, thereby lowering overall system cost.
- Leverages proven 1394a-2002 PHY core design.
- Compatibility with current *Microsoft*® *Windows*®, *MacOS*®, *Linux*® drivers, and common applications.
- Interoperability with existing, as well as older, 1394 consumer electronics and peripherals products.
- Supports low-power system designs with 525 mW typical power dissipation and extensive power management features.
- Single external 24.576 MHz crystal (or crystal oscillator for *TI*® compatibility) for 1394 clock generation.
- Two-port and one-port options available.
- Low-power mode when a 1394 cable is not attached. PME interrupt is generated when a cable is attached.
- 127-ball VTFSBGA package.
- Optional register configuration through a serial EEPROM interface or back-door BIOS access. Default configuration does not require external EEPROM.
- Fabricated in cost-effective 0.13 µm technology with single 3.3 V power supply.
- Scan, BIST, and NAND tree based design for testability (DFT) support.

PCI Express

- Fully compliant with revision 1.0a base specification.
- Multiple virtual channel (VC0, VC1) support for differentiating 1394 isochronous traffic.
- Supports eight user-programmable traffic classes.
- Interrupt coalescing from different parts of the device.
- 64-bit and 32-bit platform support.
- Supports 1394 packet address alignment.
- Interrupts via legacy INTx interface or message signaled interrupt (MSI).
- Supports *PCI Express* clock power management via CLKREQN signal for form factors that support this protocol.
- Supports all link power management states (L0, L0s, L1, and L2/L3) and active state power management (ASPM).
- Integrated 2.5 Gbits/s SerDes for full-duplex serial data transfer.

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OHCI (Open Host Controller Interface)

- Enhanced with the OHCI 1.2 draft specification for 1394a-2000 PHY full operational compliance.
- OHCI 1.0 backwards-compatible. Configurable via EEPROM to operate in either OHCI 1.0 or OHCI 1.1 mode.
- 8 Kbyte isochronous transmit FIFO.
- 4 Kbyte asynchronous transmit FIFO.
- 8 Kbyte isochronous receive FIFO.
- 8 Kbyte asynchronous receive FIFO.
- Dedicated asynchronous and isochronous descriptor-based DMA engines.
- Eight isochronous transmit contexts.
- Eight isochronous receive contexts.
- Supports parallel processing of incoming physical read and write requests.
- Supports up to 48-bit addressing per OHCI specification for the physical DMA transfers.

1394a-2000 Link

- Cycle master and isochronous resource manager capable.
- Supports 1394a-2000 acceleration features.

1394a-2000 PHY

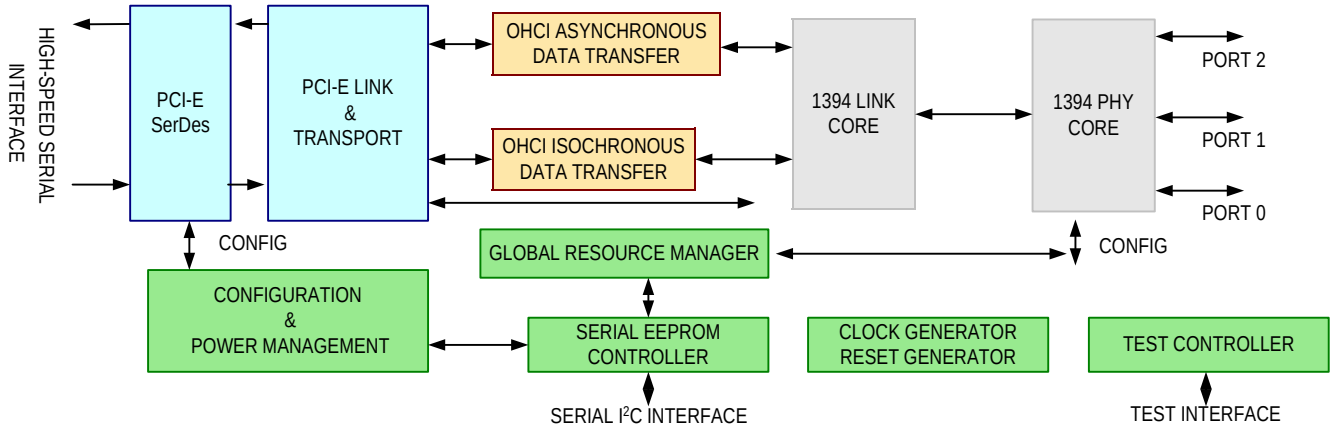
- Provides three *IEEE*® 1394a-2000 compliant ports supporting speeds of 100 Mbits/s, 200 Mbits/s, and 400 Mbits/s over 4.5 m copper.
- Fully supports provisions of *IEEE* 1394a-2000 and 1394-1995 standards for high-performance serial bus.
- Link is not required for hub operation.
- Supports extended BIAS_HANDSHAKE time for enhanced interoperability with camcorders.
- Does not require external filter capacitor for PLL.
- Supports arbitrated short bus reset to improve utilization of the bus.
- Supports ack-accelerated arbitration and fly-by concatenation.
- Supports PHY pinging and remote PHY access packets.
- Fully supports suspend/resume.
- Reports cable power fail interrupt when voltage at CPSball falls below 7.5 V.

Ordering Information

Device Code	Comcode
L-FW533-DB*	7110099250

* Lead-free: No intentional addition of lead, and less than 1000 ppm. Agere Systems lead-free devices are fully compliant with the Restriction of Hazardous Substances (RoHS) directive that restricts the content of six hazardous substances in electronic equipment in the European Union. Beginning July 1, 2006, electronic equipment sold in the European Union must be manufactured in accordance with the standards set by the RoHS directive.

Functional Block Diagram



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