# FW321 07 NV129

## 1394a PCI PHY/Link Open Host Controller Interface

**agere** systems

## Features

- 129-ball VTFSBGA lead-free package.
- 1394a-2000 OHCI link and PHY core function in a single device:
  - Single-chip link and PHY enable smaller, simpler, more efficient motherboard and add-in card designs.
  - Compatibility with current *Microsoft Windows®* drivers and common applications.
  - Interoperability with existing, as well as older, 1394 consumer electronics and peripherals products.
  - Support low-power system designs (CMOS implementation and power management features).
  - LPS, LKON, and CNA outputs to support legacy power management implementations.

- OHCI:
  - Complies with the *1394 OHCI 1.1 Specification*.
  - OHCI 1.0 backwards compatible: configurable via PCI bus commands to operate in either OHCI 1.0 or OHCI 1.1 mode.
  - Listed on *Windows* hardware compatibility list http://testedproducts.windowsmarketplace.com.
  - Compatible with *Microsoft Windows* and *MacOS®* operating systems.
  - 4 Kbyte isochronous transmit FIFO.
  - 2 Kbyte asynchronous transmit FIFO.
  - 4 Kbyte isochronous receive FIFO.
  - 2 Kbyte asynchronous receive FIFO.
  - Dedicated asynchronous and isochronous descriptor-based DMA engines.
  - Eight isochronous transmit/receive contexts.
  - Prefetches isochronous transmit data.
  - Supports posted write transactions.
  - Supports parallel processing of incoming physical read and write requests.
  - May be used without an EEPROM when the system BIOS is programmed with the EEPROM contents.

- 1394a-2000 PHY core:
  - Compliant with *IEEE® 1394a-2000, Standard for a High Performance Serial Bus*.
  - Provides one fully compliant cable port, supporting 400 Mbits/s, 200 Mbits/s, and 100 Mbits/s traffic.
  - Does not require external filter capacitor for PLL.
  - Supports link-on as a part of the internal PHY core-link interface.
  - Supports arbitrated short bus reset to improve utilization of the bus.

  - Supports multispeed packet concatenation.
  - Supports PHY pinging and remote PHY access packets.
  - Reports cable power fail interrupt when voltage at CPS pin falls below 7.5 V.

- PCI:
  - Revision 2.3 compliant.
  - 33 MHz/32-bit operation.
  - Programmable burst size thresholds for PCI data transfer.
  - Supports optimized memory read line, memory read multiple, and memory write invalidate burst commands.
  - Supports *PCI Bus Power Management Interface Specification* v.1.1.
  - Supports CLKRUN# protocol per PCI Mobile Design Guide.
  - Supports *Mini PCI Specification* v1.0, including *Mini PCI®* power requirements.
  - CardBus support per PC card standard release 8.0, including 128 bytes of on-chip tuple memory.

## Other Features

- CMOS process.
- 3.3 V operation, 5 V tolerant inputs.
- $I^2C$ serial ROM interface.

## Block Diagram
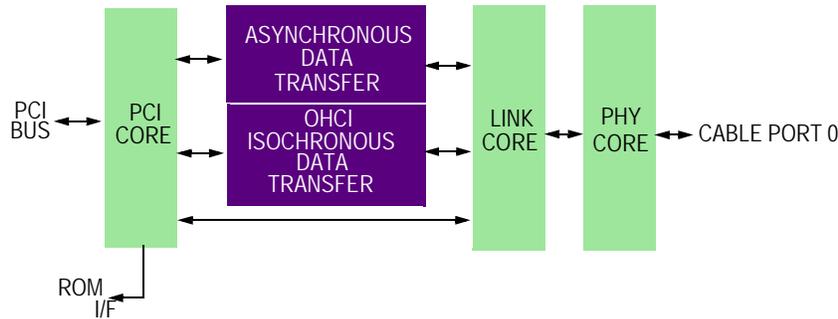


## Ordering Information

| Device Code | Package | Comcode |
|---|---|---|
| L-FW321-076-NV129-DB*† | 129-Ball VTFSBGAC | 711009132 |

\* Lead-free: No intentional addition of lead, and less than 1000 ppm.

† Agere Systems lead-free devices are fully compliant with the Restriction of Hazardous Substances (RoHS) directive that restricts the content of six hazardous substances in electronic equipment in the European Union. Beginning July 1, 2006, electronic equipment sold in the European Union must be manufactured in accordance with the standards set by the RoHS directive.

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