ALC262-GR
ALC262-VB Series
(ALC262-VB0-GR, ALC262SRS-GR, ALC262H-GR)
ALC262-VC Series (ALC262-VC1-GR, ALC262-VC2-GR)
ALC262-VD Series (ALC262-VD2-GR, ALC262W-VD2-GR)

4-CHANNEL DAC AND 6-CHANNEL ADC HIGH DEFINITION AUDIO CODEC

DATASHEET

Rev. 1.9
15 April 2008
Track ID: JATR-1076-21

Realtek Semiconductor Corp.
No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com.tw

COPYRIGHT

DISCLAIMER

Realtek provides this document "as is", without warranty of any kind, neither expressed nor implied, including, but not limited to, the particular purpose. Realtek may make improvements and/or changes in this document or in the product described in this document at any time. This document could include technical inaccuracies or typographical errors.

TRADEMARKS

Realtek is a trademark of Realtek Semiconductor Corporation. Other names mentioned in this document are trademarks/registered trademarks of their respective owners.

USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek ALC262 Series Audio Codecs.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2005/05/02	First release.
1.1	2005/06/09	Update section 12 Ordering Information, page 78. Revise analog output port information in section 1 General Description, page 1.
1.2	2005/08/25	Add ordering information note (see section 12 Ordering Information, page 78).
1.3	2005/10/17	Revise Figure 2, page 7. Revise Table 84, page 72. Update section 122 Ordering Information, page 78.
1.4	2005/11/25	Update section 12 Ordering Information, page 78.
1.5	2006/06/22	Release for ALC262 'C' version. Revise section 4 Block Diagram, page 6 Improve DAC/ADC filter characteristics, Table 79, page 68. Support low voltage (1.5V~3.3V) IO for HAD link. Add digital microphone input support (pins 2 and 46), see Figure 5, page 10. Add digital microphone application note (section 10.4 Digital Microphone Implementation, page 74). Update section 12 Ordering Information, page 78.
1.6	2007/01/15	Update section 12 Ordering Information, page 78.
1.7	2007/01/22	Cosmetic changes to Figure 5, page 10.
1.8	2007/07/04	Release for ALC262 'D' version. This release was never checked/reviewed/approved Supports 2nd SPDIF output: Update section 8.2 Verb – Get Connection Select Control (Verb ID=F01h), page 40. Update section 8.3 Verb – Set Connection Select (Verb ID=701h), page 41. Meets Intel low power ECR compliant and power status control for all analog converter and pin widgets. See section 7.5 Power Management, page 28.
1.9	2008/04/15	Added information for all ALC262 series (version A/B/C/D). Added part number ALC262W-VD2-GR in section 12 Ordering Information, page 78.

Table of Contents

List of Tables

List of Figures

1. General Description

The ALC262 series are 4-Channel DAC and 6-Channel ADC High Definition Audio Codecs with UAA (Universal Audio Architecture). Featuring two 24-bit stereo DACs and three 24-bit stereo ADCs (the ALC262, ALC262-VB and ALC262-VC support 20-bit ADC format, the ALC262-VD supports 24-bit ADC format), they are designed for high-performance multimedia desktop and laptop systems. The ALC262 series incorporates proprietary converter technology to achieve over 100dB Signal-to-Noise ratio playback quality.

The ALC series meets the current WLP3.10 (Windows® Logo Program) requirements, and the ALC262-VD (D version) meets future WLP requirements that become effective from 01 June 2008, bringing PC sound quality closer to consumer electronic devices.

The ALC262 series provide 4 channels of DAC, supporting stereo sound playback on the rear panel and independent stereo sound output on the front panel simultaneously (multiple streaming), along with flexible mixing, mute, and fine gain control functions to provide a complete integrated audio solution.

The ALC262 series also integrates three stereo ADCs that can support a microphone array with Acoustic Echo Cancellation (AEC), Beam Forming (BF), and Noise Suppression (NS) technology simultaneously, significantly improving sound quality for PC VoIP applications. With this unique feature (3 stereo ADCs), the ALC262 can provide high-quality audio using S/PDIF to output analog data, or for multiple-source recording applications.

All analog IO are input and output capable and can be re-tasked according to user's definitions. Headphone amplifiers are also integrated at analog output ports A, B, C, D, E, and F. The ALC262 series supports 16/20/24 S/PDIF input and output to offer easy connection of PCs to high quality consumer electronic products such as digital decoders and speakers.

The ALC262 series supports host/soft audio from the Intel ICH chipset, and also from any other HDA compatible audio controller. With EAX/Direct Sound 3D/I3DL2/A3D compatibility, and excellent software utilities like Karaoke mode, environment emulation, software equalizer, HRTF 3D positional audio, and optional Dolby®, SRS®, Fortemedia® and Waves® audio technology the ALC262 provides an excellent entertainment package and game experience for PC users.

Two functions are added in the ALC262 C version:

- Addition of a digital microphone interface. The ALC262 C version supports most digital microphones currently available. With digital microphone implementation, a notebook computer can achieve better voice input quality without noise interference caused by geometric PCB layout and radio frequency devices
- The ALC262 C supports scalable I/O voltage (1.5V to 3.3V) on an HDA link, which will be a requirement in future chipsets designed for low voltage operation.

The ALC262 D supports a secondary S/PDIF output converter and a dedicated output pin (S/PDIF-OUT2) to a HDMI transmitter, and all ADCs support up to192K sample rate and 24-bit PCM format. The ALC262 D version conforms to Intel's Audio Codec low power state white paper and is ECR compliant, with improved frequency response at a 44.1kHz sampling rate, and THD+N measured at -1dB full scale in compliance with future WLP requirements that become effective from 01 June 2008.

Note: ALC262 version differences are listed in section 12 Ordering Information, page 78.

2. Features

2.1. Hardware Features

- High-performance DACs with 100dB SNR
- ADCs with 90dB SNR (A-weighting)
- Meets WLP (Windows Logo Program) 3.10 and future WLP requirements that become effective from 01 June 2008
- Two stereo DACs support 16/20/24-bit PCM for stereo audio playback on the rear panel, plus 2 channels of independent stereo sound output (multiple streaming) through the Front-Out-Left and Front-Out-Right channels
- Three stereo ADCs support 16/20-bit PCM for multiple input streaming (ALC262A/B/C versions)
- Three stereo ADCs support 16/20/24-bit PCM for multiple input streaming (ALC262D version)
- All DACs supports 44.1/48/96/192kHz sample rate
- All ADCs support 44.1/48/96kHz sample rate (ALC262 A/B/C version)
- All ADCs support 44.1/48/96/192kHz sample rate (ALC262 D version)
- 16/20/24-bit S/PDIF-OUT supports 44.1/48/96/192kHz sample rate
- 16/20/24-bit S/PDIF-IN supports 44.1/48/96/192kHz sample rate
- Up to four channels of microphone input are supported for AEC/BF applications
- Supports MONO line output with independent volume control
- High-quality analog differential CD input
- Supports external PCBEEP input and built-in digital BEEP generator
- Software selectable 2.5V/3.75V VREFOUT
- Two jack detection pins each designed to detect up to 4 jacks
- Wide range (–80dB ~ +42dB) volume control with 1.5dB resolution of analog to analog mixer gain
- All analog jacks are stereo input and output re-tasking for analog plug & play
- Built-in headphone amplifiers for port-A/D/E/F

- Supports both analog DC volume control and GPI digital volume control (requires driver support)
- 4 GPIOs (General Purpose Input/Output) for customized applications
- Optional EAPD (External Amplifier Power Down) is supported
- Power support: Digital: 3.3V; Analog: 3.3V/5.0V
- Power management and enhanced power saving features
- 48-pin LQFP 'Green' package; pin compatible with the ALC260
- Supports low voltage (1.5V~3.3V) IO for HDA link (ALC262 C/D version)
- Supports stereo digital microphone input (ALC262 C/D version)
- Supports 2nd S/PDIF output. (ALC262 D version)
- Intel low power ECR compliant and power status control for all widgets (ALC262 D version)

2.2. Software Features

- Meets Microsoft Windows Logo Program requirements
- EAX™ 1.0 & 2.0 compatible
- Direct Sound 3D™ compatible
- A3D™ compatible
- I3DL2 compatible
- HRTF 3D Positional Audio (Windows XP only)
- Emulation of 26 sound environments to enhance gaming experience
- Multi-band software equalizer and tools
- Voice Cancellation and Key Shifting in Karaoke mode
- Dynamic range control (expander, compressor and limiter) with adjustable parameters
- Intuitive Configuration Panel (Realtek Audio Manager) to enhance user experience
- Provides 10-foot GUI for Windows Media Center

- Microphone Acoustic Echo Cancellation (AEC), Noise Suppression (NS), and Beam Forming (BF) technology for voice application
- Smart multiple streaming operation
- HDMI audio driver for AMD platform
- Dolby® PCEE program™ (optional software feature)
- SRS® TrueSurround HD (optional software feature)
- Fortemedia® SAM™ technology for voice processing (Beam Forming and Acoustic Echo Cancellation) (optional software feature)
- MaxxAudio technologies from Waves (optional software feature, ALC262-VD2 only)

3. System Applications

- Multimedia desktop and laptop PCs
- Information appliances (IA)

4. Block Diagram

4.1. ALC262 A/B Version

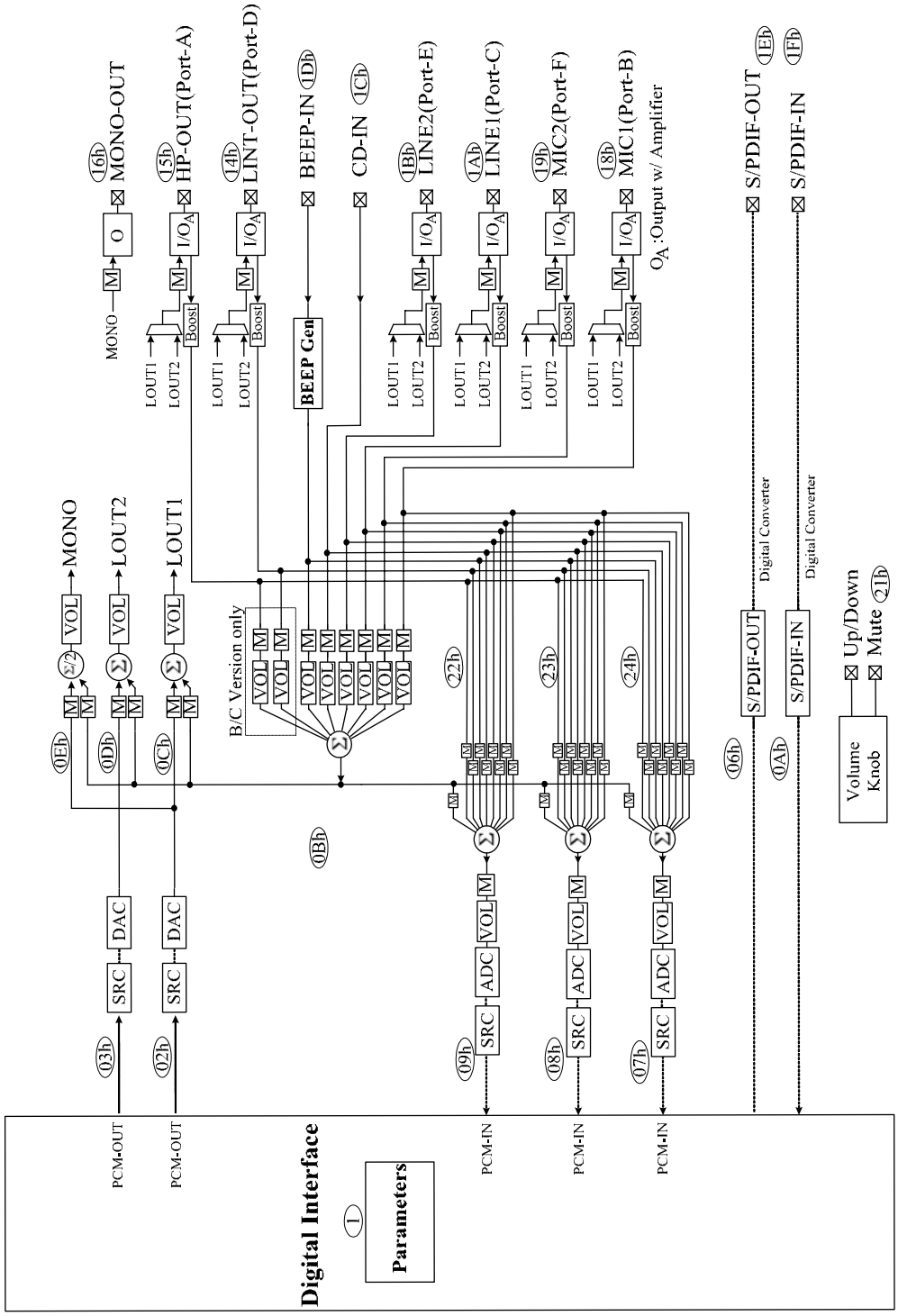


Figure 1. Block Diagram – ALC262 A/B Version

4.2. ALC262 C Version

Note: The ALC262 C Version supports digital MIC (DMIC-CLK, DMIC-DATA).

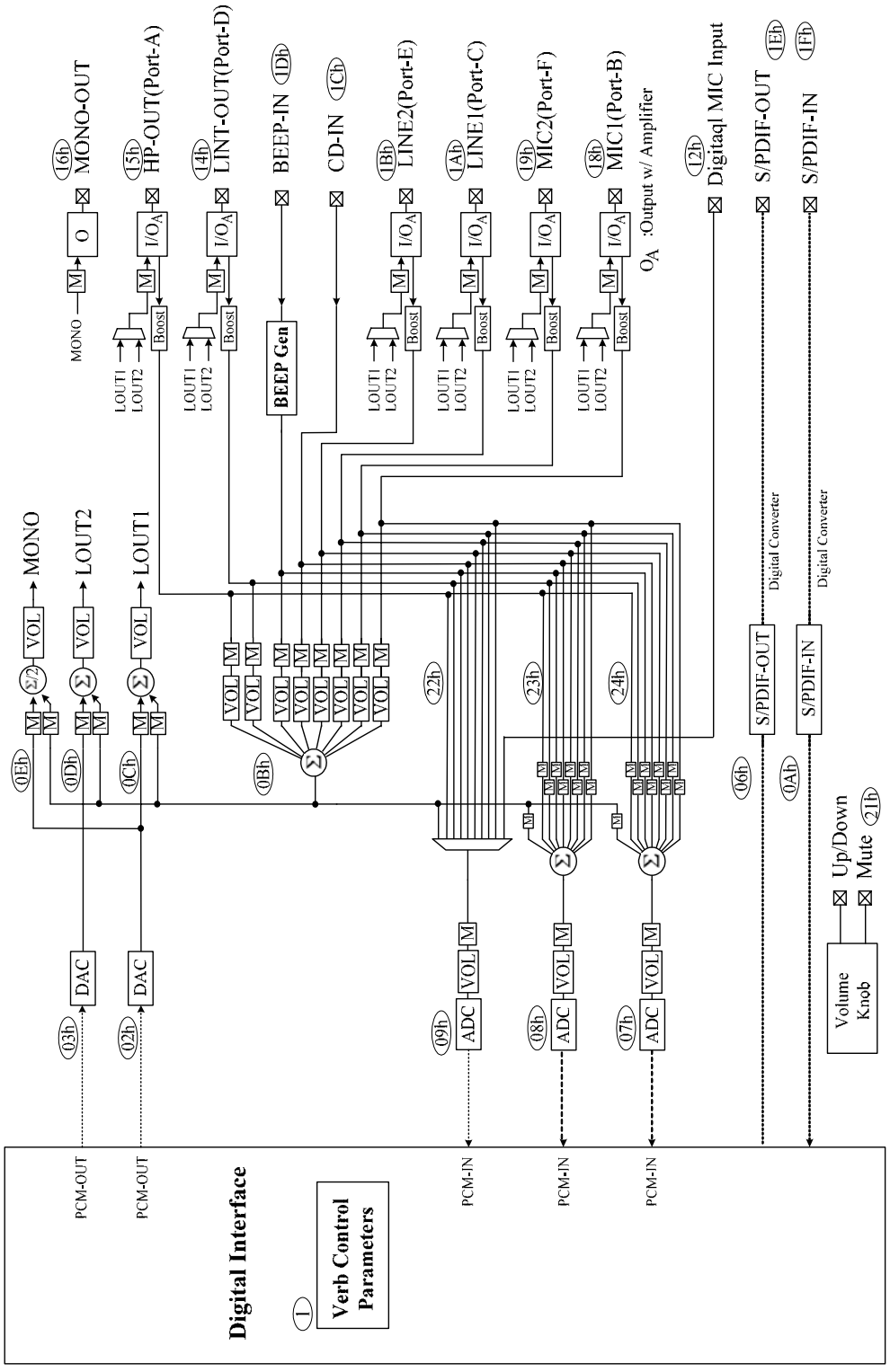


Figure 2. Block Diagram – ALC262 C Version

4.3. ALC262 D Version

Note: The ALC262 D Version supports digital MIC (DMIC-CLK, DMIC-DATA) and S/DPIF-OUT2.

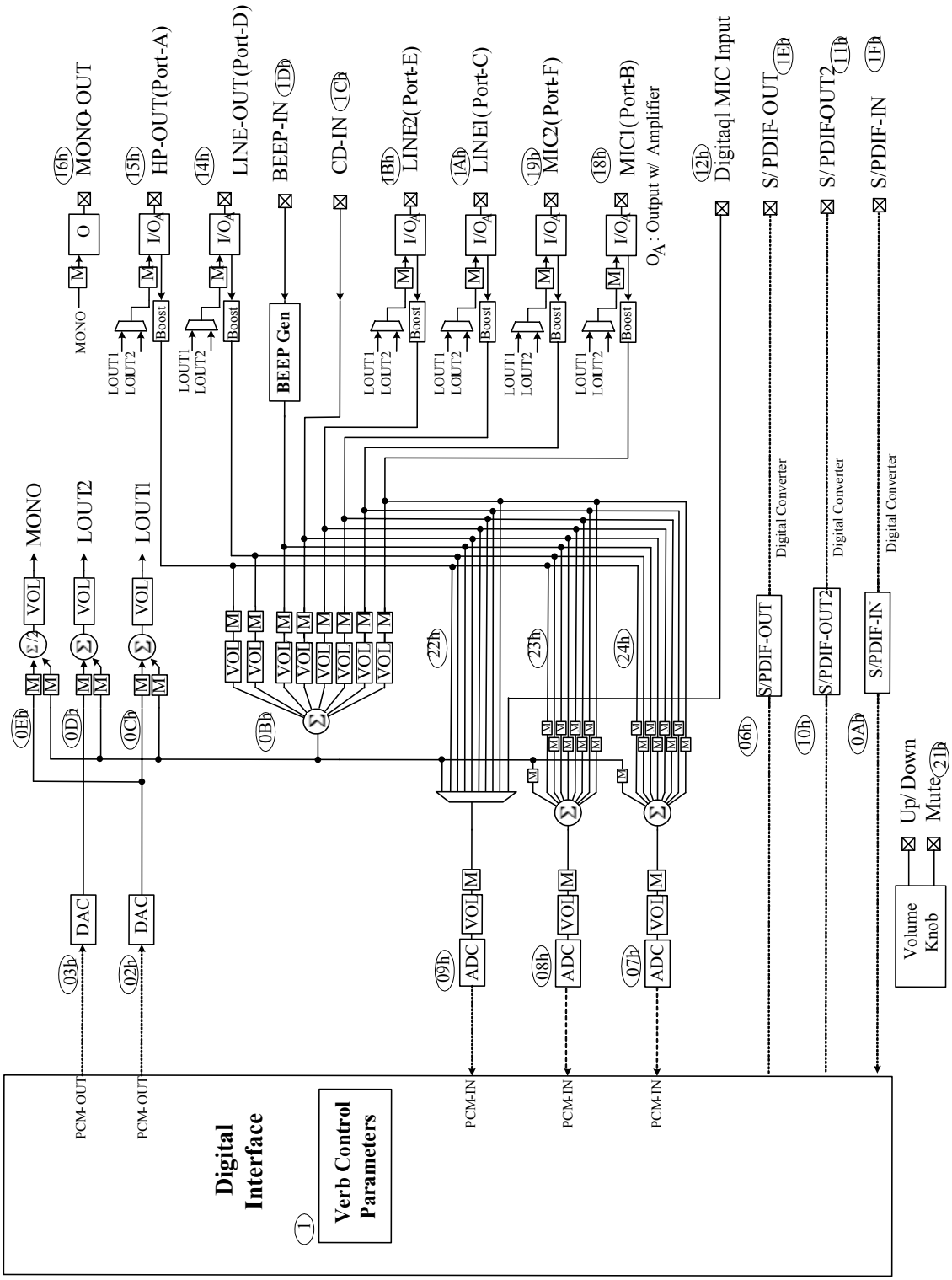


Figure 3. Block Diagram – ALC262 D Version

4.4. Analog Input/Output Unit

Pin Complex widgets NID=14h~16h, 18h~1Bh are re-tasking IO.

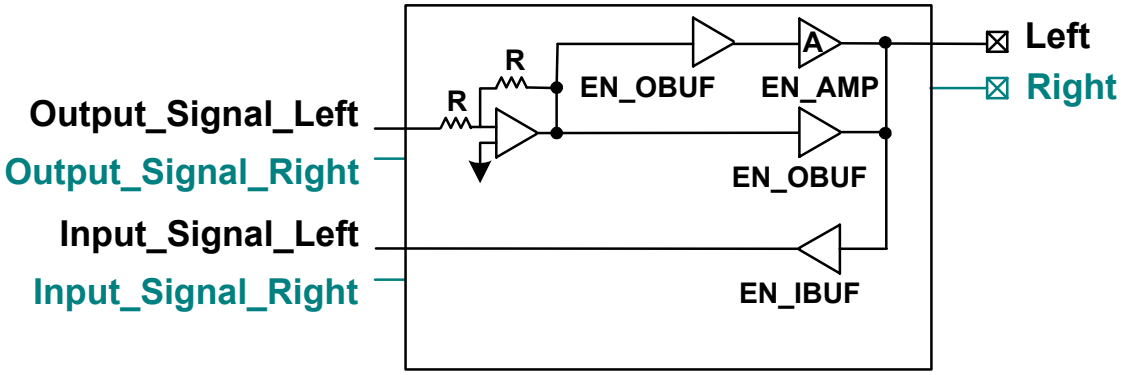


Figure 4. Analog Input/Output Unit

5. Pin Assignments

5.1. ALC262 A/B Version

Note: C and D versions (Figure 6, page 11, and Figure 7, page 12) support digital MIC (pin 2, 46) and Scalable I/O Power (pin 9).

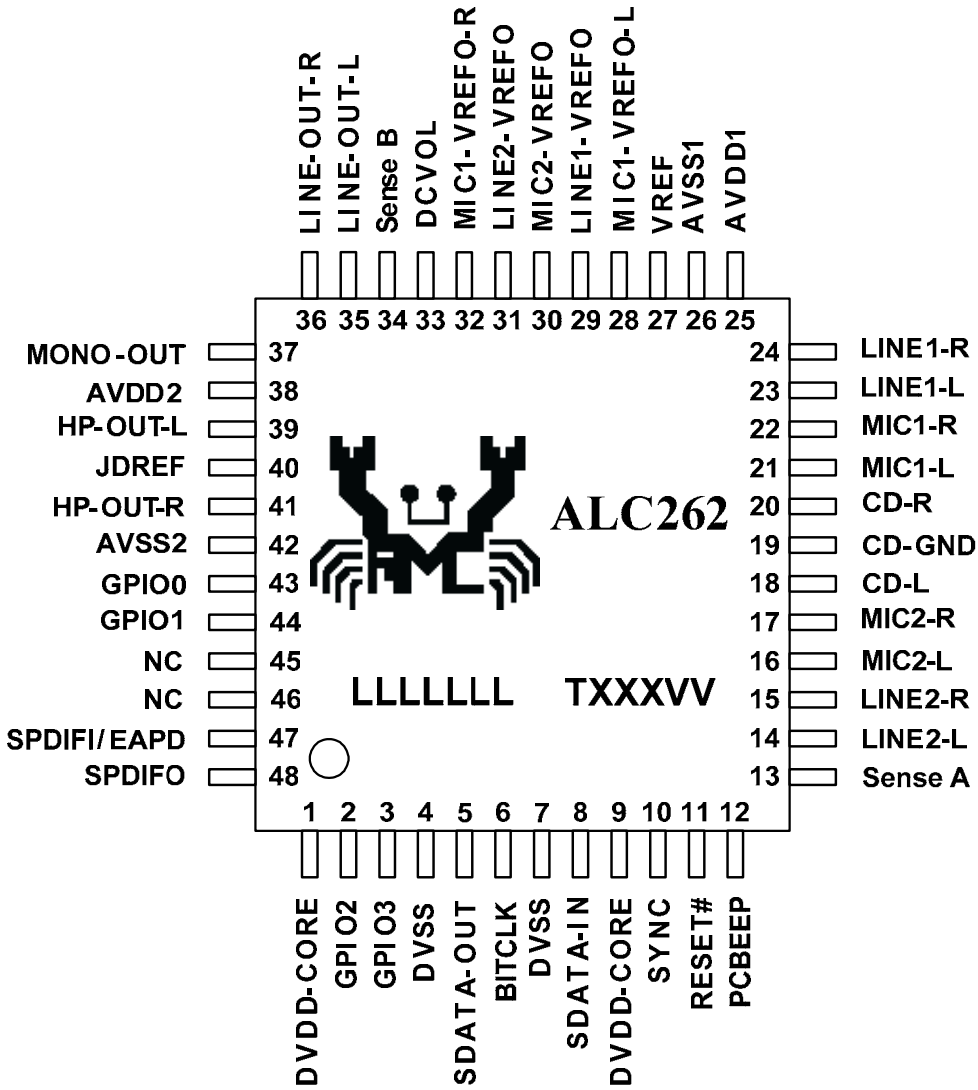


Figure 5. ALC262 A/B Version Pin Assignments

5.2. Green Package and Version Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 5. The version number is shown in the location marked 'VV'. For example, 'VV=B0' indicates silicon version 'B' and stepping version '0', which is the first stepping of the ALC262 version B.

5.3. ALC262 C Version

The C version supports digital MIC (pin 2, 46) and Scalable I/O Power (pin 9).

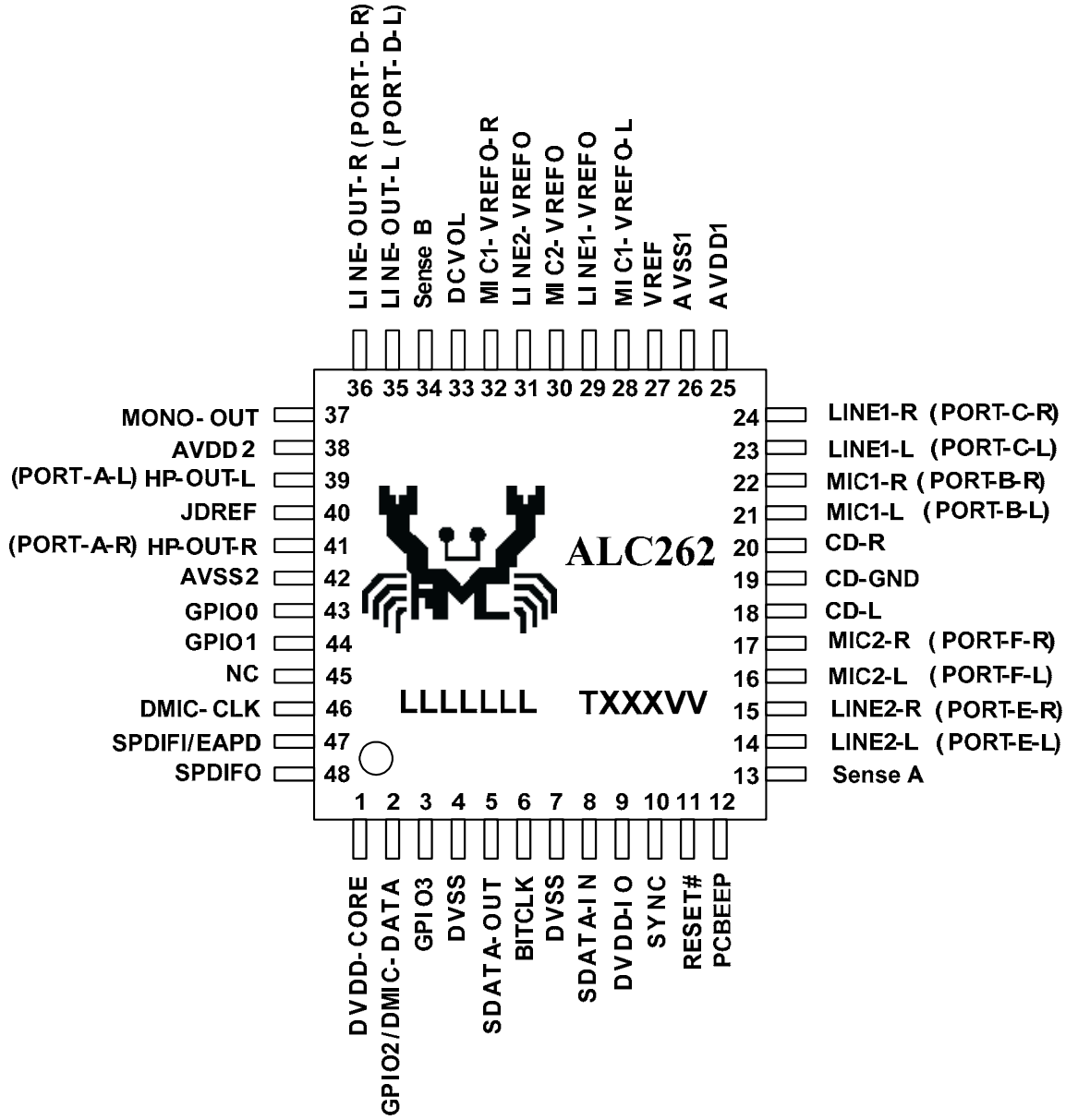


Figure 6. ALC262 C Version Pin Assignments

5.4. Green Package and Version Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 6. The version number is shown in the location marked 'VV'. For example, 'VV=C0' indicates silicon version 'C' and stepping version '0', which is the first stepping of the ALC262-VC.

5.5. ALC262 D Version

The D version supports digital MIC (pin 2, 46), Scalable I/O Power (pin 9), and S/PDIFO2 (pin45).

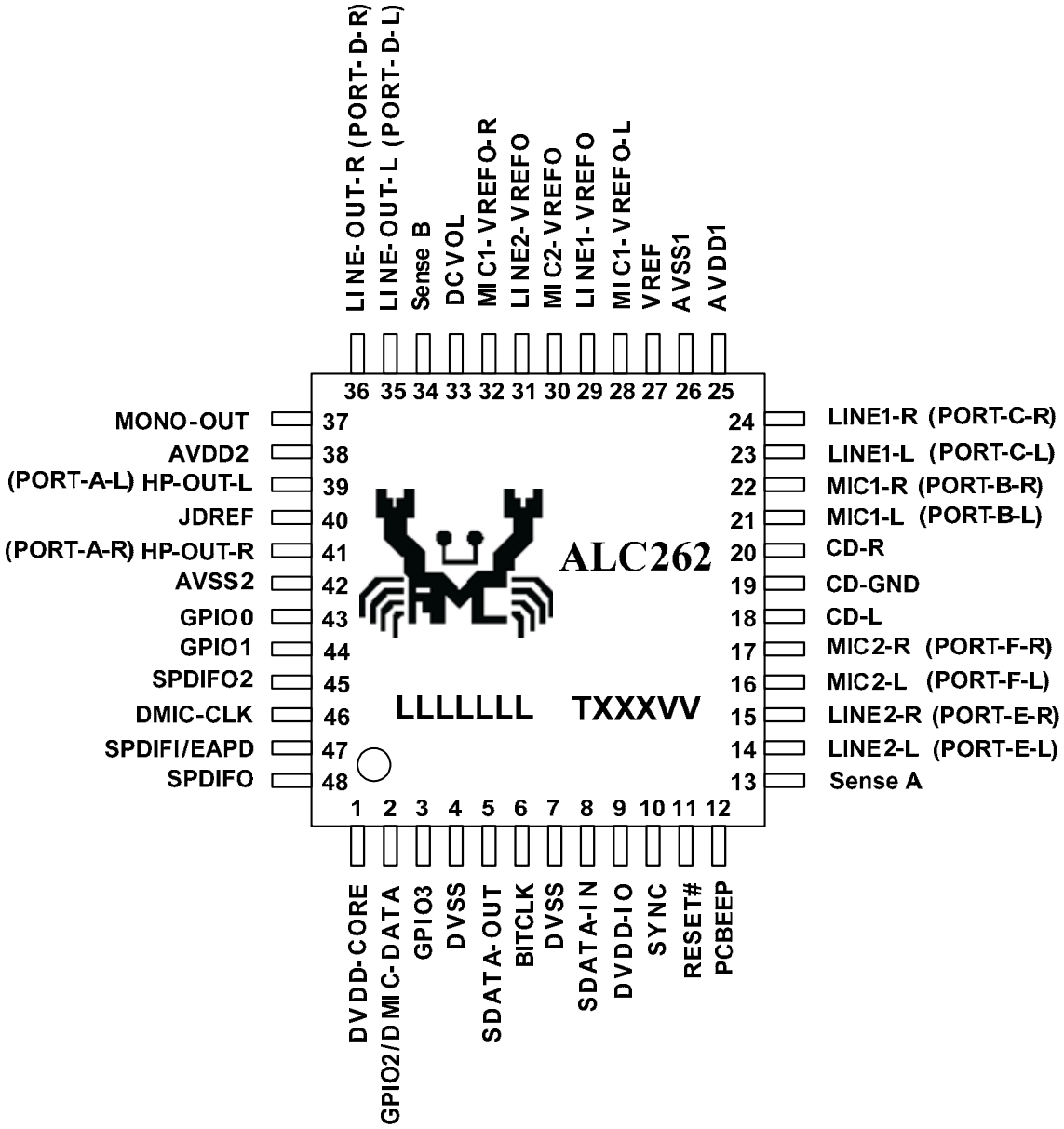


Figure 7. ALC262 D Version Pin Assignments

5.6. Green Package and Version Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 7. The version number is shown in the location marked 'VV'. For example, 'VV=D0' indicates silicon version 'D' and stepping version '0', which is the first stepping of the ALC262-VD.

6. Pin Descriptions

6.1. Digital I/O Pins

Table 1. Digital I/O Pins

Name	Type	Pin No.	Description	Characteristic Definition
RESET#	I	11	H/W Reset Control	V_t=0.5*DVDD
SYNC	I	10	Sample Sync (48kHz)	Schmitt trigger input, V_{IL}=1.0V, V_{IH}=2.0V
BITCLK	I	6	24MHz Bit Clock Input	Schmitt trigger input, V_{IL}=1.0V, V_{IH}=2.0V
SDATA-OUT	I	5	Serial TDM Data Input	V_t=0.5*DVDD
SDATA-IN	O	8	Serial TDM Data Output	V_{OH}=0.9*DVDD, V_{OL}=0.1*DVDD
SPDIFI / EAPD	IO	47	S/PDIF Input / Signal to Power Down Ext. Amp	Self bias to V_t=1.5V / Output V_{OH}=0.9*DVDD, V_{OL}=0.1*DVDD
SPDIFO	O	48	S/PDIF Output	Output has 12mA@75Ω driving capability.
SPDIFO2	O	45[1]	S/PDIF Output	Output has 12mA@75Ω driving capability.
GPIO0	IO	43	General Purpose Input/Output 0	Input Vt=(2/3)*DVDD, output V_{OH}=0.9*DVDD, V_{OL}=0.1*DVDD, internal pulled up by 50KΩ
GPIO1	IO	44	General Purpose Input/Output 1	Input Vt=(2/3)*DVDD, output V_{OH}=0.9*DVDD, V_{OL}=0.1*DVDD, internal pulled up by 50KΩ
GPIO2 / DMIC-DATA	IO	2[2]	General Purpose Input/Output 2. Data Input from Digital MIC	Input Vt=(2/3)*DVDD, output V_{OH}=0.9*DVDD, V_{OL}=0.1*DVDD, internal pulled up by 50KΩ
GPIO3	IO	3	General Purpose Input/Output 3	Input Vt=(2/3)*DVDD, output V_{OH}=0.9*DVDD, V_{OL}=0.1*DVDD, internal pulled up by 50KΩ
DMIC-CLK	O	46[2]	Clock Output for Digital MIC	Default 2.048MHz clock output
				Total: 13 Pins

Note 1: Only the D version supports SPDIFO2.

Note 2: Only the C version and D version support DMIC-DATA and DMIC-CLK.

6.2. Analog I/O Pins

Table 2. Analog I/O Pins

Name	Type	Pin No.	Description	Characteristic Definition
LINE2-L	IO	14	2nd Line Input Left Channel	Analog input/output, default is input (PORT-E)
LINE2-R	IO	15	2nd Line Input Right Channel	Analog input/output, default is input (PORT-E)
MIC2-L	IO	16	2nd Stereo Microphone Input Left Channel	Analog input/output, default is input (PORT-F)
MIC2-R	IO	17	2nd Stereo Microphone Input Right Channel	Analog input/output, default is input (PORT-F)
CD-L	I	18	CD Input Left Channel	Analog input, 1.6Vrms of full scale input
CD-GND	I	19	CD Input Reference Ground	Analog input, 1.6Vrms of full scale input
CD-R	I	20	CD Input Right Channel	Analog input, 1.6Vrms of full scale input
MIC1-L	IO	21	1st Stereo Microphone Input Left Channel	Analog input/output, default is input (PORT-B)

Name	Type	Pin No.	Description	Characteristic Definition
MIC1-R	IO	22	1st Stereo Microphone Input Right Channel	Analog input/output, default is input (PORT-B)
LINE1-L	IO	23	1st Line Input Left Channel	Analog input/output, default is input (PORT-C)
LINE1-R	IO	24	1st Line Input Right Channel	Analog input/output, default is input (PORT-C)
PCBEEP	I	12	External PCBEEP Input	Analog input, 1.6Vrms of full scale input
LINE-OUT-L	IO	35	Line Output Left Channel	Analog output (PORT-D)
LINE-OUT-R	IO	36	Line Output Right Channel	Analog output (PORT-D)
HP-OUT-L	IO	39	Headphone Out Left Channel	Analog output (PORT-A)
HP-OUT-R	IO	41	Headphone Out Right Channel	Analog output (PORT-A)
MONO-OUT	O	37	MONO Output	Analog mono output is summation of (L+R)/2
Sense A	I	13	Jack Detect Pin 1	Jack resistor network input 1
Sense B	I	34	Jack Detect Pin 2	Jack resistor network input 2
DCVOL	I	33	DC Sense for Volume Control	Analog DC input for external volume control
				Total: 20 Pins

6.3. Filter/Reference

Table 3. Filter/Reference

Name	Type	Pin No.	Description	Characteristic Definition
VREF	-	27	2.5V Reference Voltage	1µF capacitor to analog ground
MIC1-VREFO-L	O	28	Bias Voltage for MIC1 Jack	2.5V/3.75Vreference voltage
LINE1-VREFO	O	29	Bias Voltage for LINE1 Jack	2.5V/3.75Vreference voltage
MIC2-VREFO	O	30	Bias Voltage for MIC2 Jack	2.5V/3.75Vreference voltage
LINE2-VREFO	O	31	Bias Voltage for LINE2 Jack	2.5V/3.75Vreference voltage
MIC1-VREFO-R	O	32	Bias Voltage for MIC1 Jack	2.5V/3.75Vreference voltage
JDREF	-	40	Ref. Resistor for Jack Detect	20K, 1% resistor to analog ground
NC	-	45, 46	Not Connected	-
				Total: 7 Pins

6.4. Power/Ground

Table 4. Power/Ground

Name	Type	Pin No	Description	Characteristic Definition
AVDD1	I	25	Analog VDD (5V or 3.3V)	Analog power for mixer and amplifier
AVSS1	I	26	Analog GND	Analog ground for mixer and amplifier
AVDD2	I	38	Analog VDD (5V or 3.3V)	Analog power for DACs and ADCs
AVSS2	I	42	Analog GND	Analog ground for DACs and ADCs
DVDD-CORE	I	1	Digital VDD (3.3V)	Digital power
DVSS	I	4	Digital GND	Digital ground
DVDD-CORE DVDD-IO	I	9	Digital VDD (3.3V) Digital VDD (1.5V~3.3V)	A/B version: Digital power for core and HDA link. C/D version: Scalable digital power for HDA link.
DVSS	I	7	Digital GND	Digital ground
				Total: 8 Pins

7. High Definition Audio Link Protocol

7.1. Link Signals

The High Definition Audio (HDA) Link is the digital serial interface that connects the HDA codecs to the HDA Controller. The HDA link protocol is controller synchronous, based on a 24.0MHz BIT-CLK sent by the HDA controller. The input and output streams, including command and PCM data, are isochronous with a 48kHz frame rate. Figure 8 shows the basic concept of the HDA link protocol.

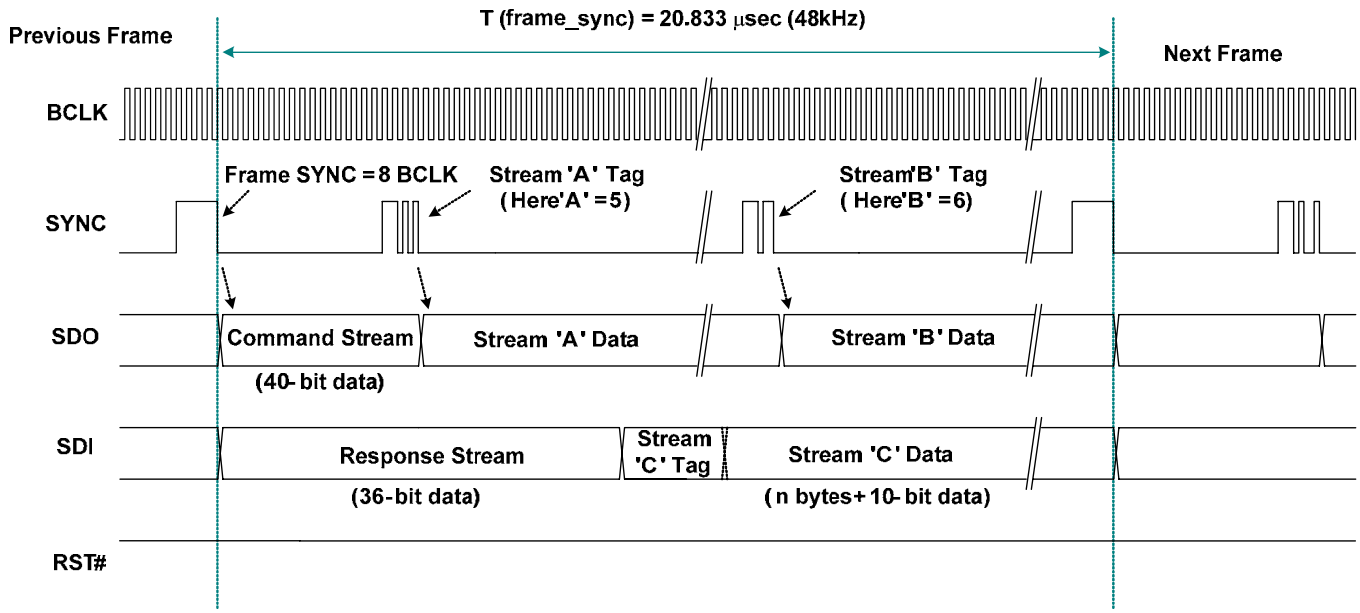


Figure 8. HDA Link Protocol

7.1.1. Signal Definitions

Table 5. Link Signal Definitions

Item	Description
BCLK	24.0MHz of bit clock sourced from the HDA controller and connecting to all codecs.
SYNC	48kHz of signal is used to synchronize input and output streams on the link. It is sourced from the HDA controller and connects to all codecs.
SDO	Serial data output signal driven by the HDA controller to all codecs. Commands and data streams are carried on SDO. The data rate is double pumped; the controller drives data onto the SDO, the codec samples data present on SDO with respect to each edge of BCLK. The HDA controller must support at least one SDO. To extend outbound bandwidth, multiple SDOs may be supported.
SDI	Serial data input signal driven by the codec. It is point-to-point serial data from the codec to the HDA controller. The controller must support at least one SDI, and up to a maximum of 15 SDI's can be supported. SDI is driven by the codec at each rising edge of BCLK, and sampled by the controller at each rising edge of BCLK. SDI can be driven by the controller to initialize the codec's ID.
RST#	Active low reset signal. Asserted to reset the codec to default power on state. RST# is sourced from the HDA controller and connects to all codecs.

Table 6. HDA Signal Definitions

Signal Name	Source	Controller Type	Description
BCLK	Controller	Output	Global 24.0MHz Bit Clock.
SYNC	Controller	Output	Global 48kHz Frame Sync and Outbound Tag Signal.
SDO	Controller	Output	Serial Data Output from Controller.
SDI	Codec/Controller	Input/Output	Serial Data Input from Codec. Weakly pulled down by the controller.
RST#	Controller	Output	Global Active Low Reset Signal.

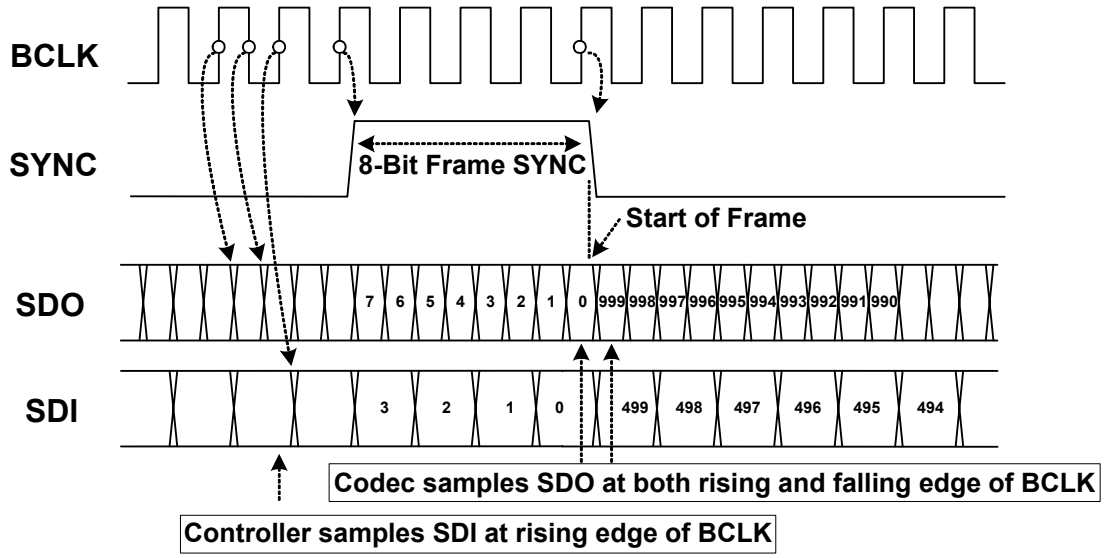


Figure 9. Bit Timing

7.1.2. Signaling Topology

The HDA controller supports two SDOs for the outbound stream, up to 15 SDIs for the inbound stream. RST#, BCLK, SYNC, SDO0, and SDO1 are driven by controller to codecs. Each codec drives its own point-to-point SDI signal(s) to the controller.

Figure 10 shows the possible connections between the HDA controller and codecs:

- Codec 0 is a basic connection. There is one single SDO and one single SDI for normal transmission
- Codec 1 has two SDOs for doubled outbound rate, a single SDI for normal inbound rate
- Codec 3 supports a single SDO for normal outbound rate, and two SDIs for doubled inbound rate
- Codec N has two SDOs and multiple SDIs

The multiple SDOs and multiple SDIs are used to expand the transmission rate between controller and codecs. Section 7.2 Frame Composition, page 18, describes the detailed outbound and inbound stream compositions for single and multiple SDOs/SDIs.

The connections shown in Figure 10 can be implemented concurrently in an HDA system. The ALC262 is designed to receive a single SDO stream.

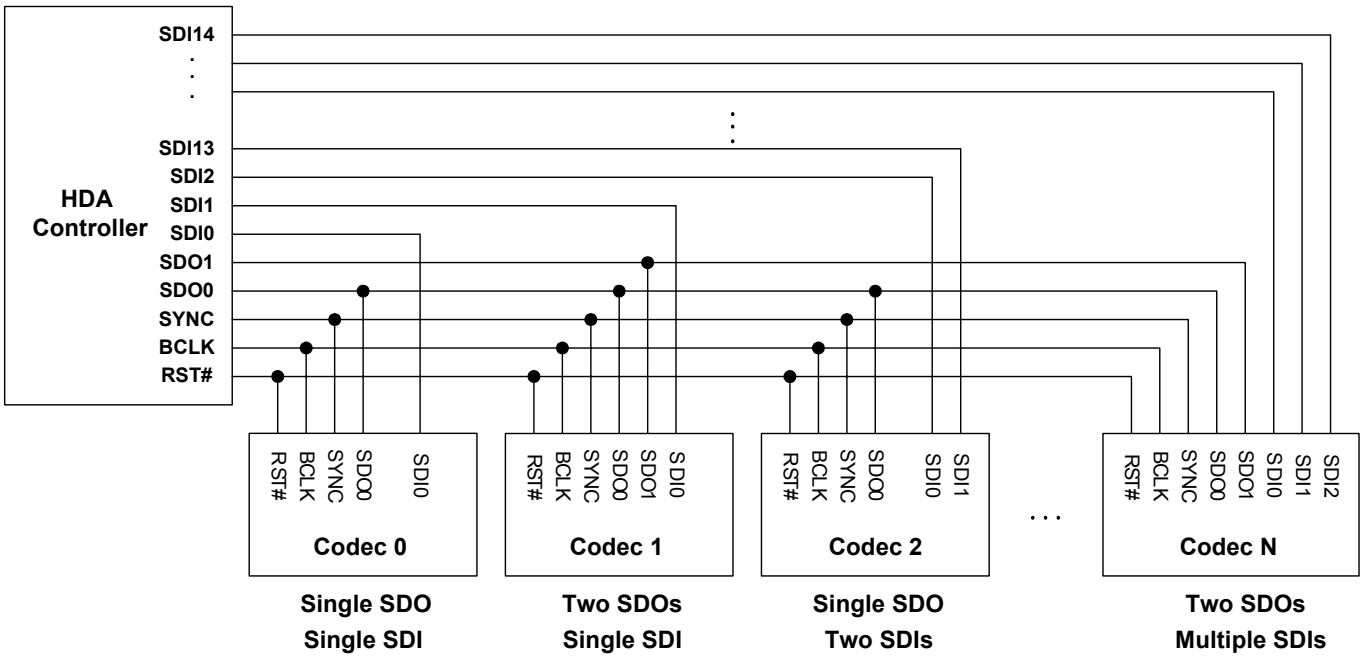


Figure 10. Signaling Topology

7.2. Frame Composition

7.2.1. Outbound Frame – Single SDO

An outbound frame is composed of one 32-bit command stream and multiple data streams. There are one or multiple sample blocks in a data stream. Only one sample block exists in a stream if the HDA controller delivers a 48kHz rate of samples to the codec. Multiple sample blocks in a stream means the sample rate is a multiple of 48kHz. This means there should be 2 blocks in the same stream to carry 96kHz samples (Figure 11).

For outbound frames, the stream tag is not in SDO, but in the SYNC signal. A new data stream is started at the end of the stream tag. The stream tag includes a 4-bit preamble and 4-bit stream ID (Figure 12).

To keep the cadence of converters bound to the same stream, samples for these converters must be placed in the same block.

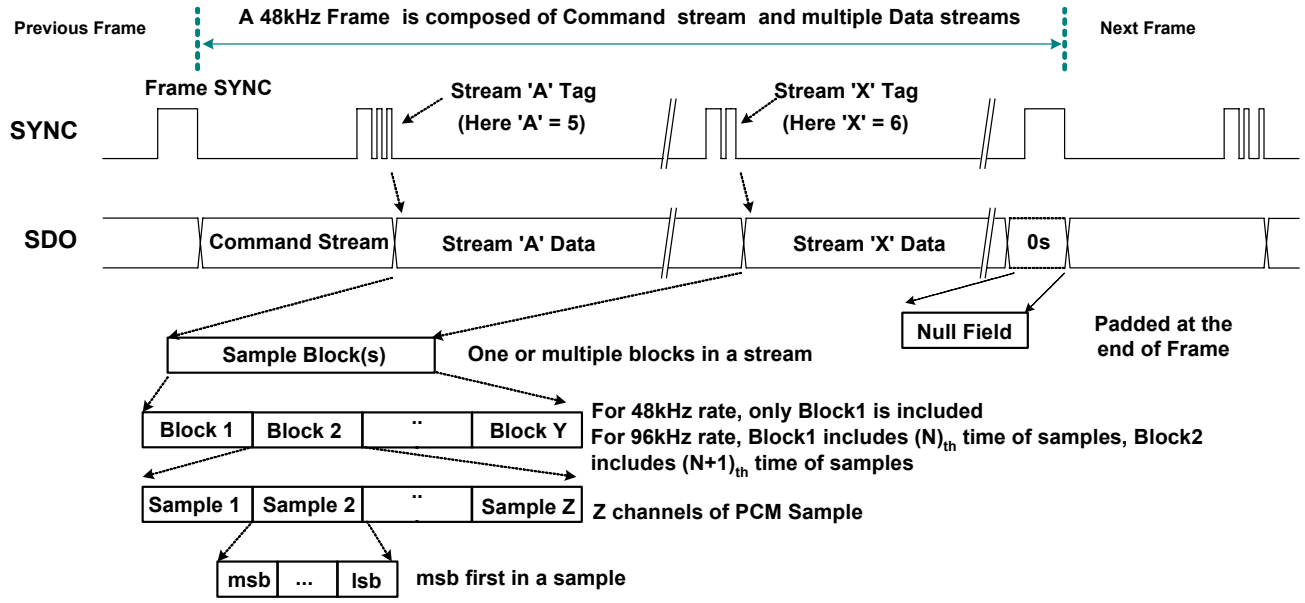


Figure 11. SDO Outbound Frame

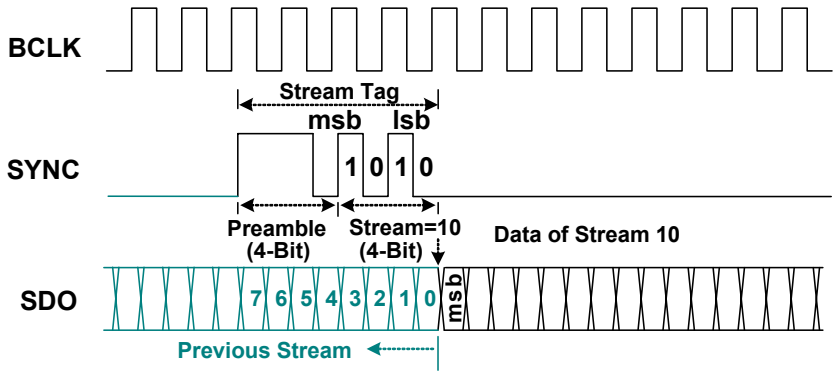


Figure 12. SDO Stream Tag is Indicated in SYNC

7.2.2. Outbound Frame – Multiple SDO

The HDA controller allows two SDO signals to be used to stripe outbound data, completing transmission in less time to get more bandwidth. If software determines the target codec supports multiple SDO capability, it enables the 'Stripe Control' bit in the controller's Output Stream Control Register to initiate a specific stream (Stream 'A' in Figure 13) to be transmitted on multiple SDOs. In this case, the MSB of stream data is always carried on SDO0, the second bit on SDO1 and so forth.

SDO1 is for transmitting a striped stream. The codec does not support multiple SDOs connected to SDO0.

To guarantee all codecs can determine their corresponding stream, the command stream is not striped. It is always transmitted on SDO0, and copied on SDO1.

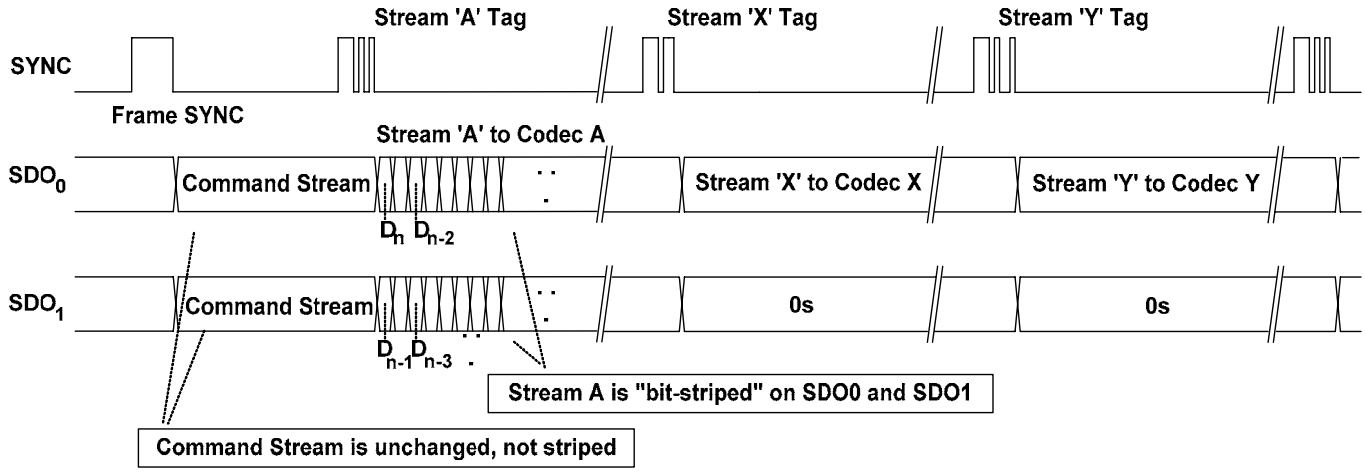


Figure 13. Striped Stream on Multiple SDOs

7.2.3. Inbound Frame – Single SDI

An Inbound Frame – A single SDI is composed of one 36-bit response stream and multiple data streams. Except for the initialization sequence (turnaround and address frame), SDI is driven by the codec at each rising edge of BCLK. The controller also samples data at the rising edge of BCLK (Figure 14).

The SDI stream tag is not carried by SYNC, but included in the SDI. A complete SDI data stream includes one 4-bit stream tag, one 6-bit data length, and n-bit sample blocks. Zeros will be padded if the total length of the contiguous sample blocks within a given stream is not of integral byte length (Figure 15).

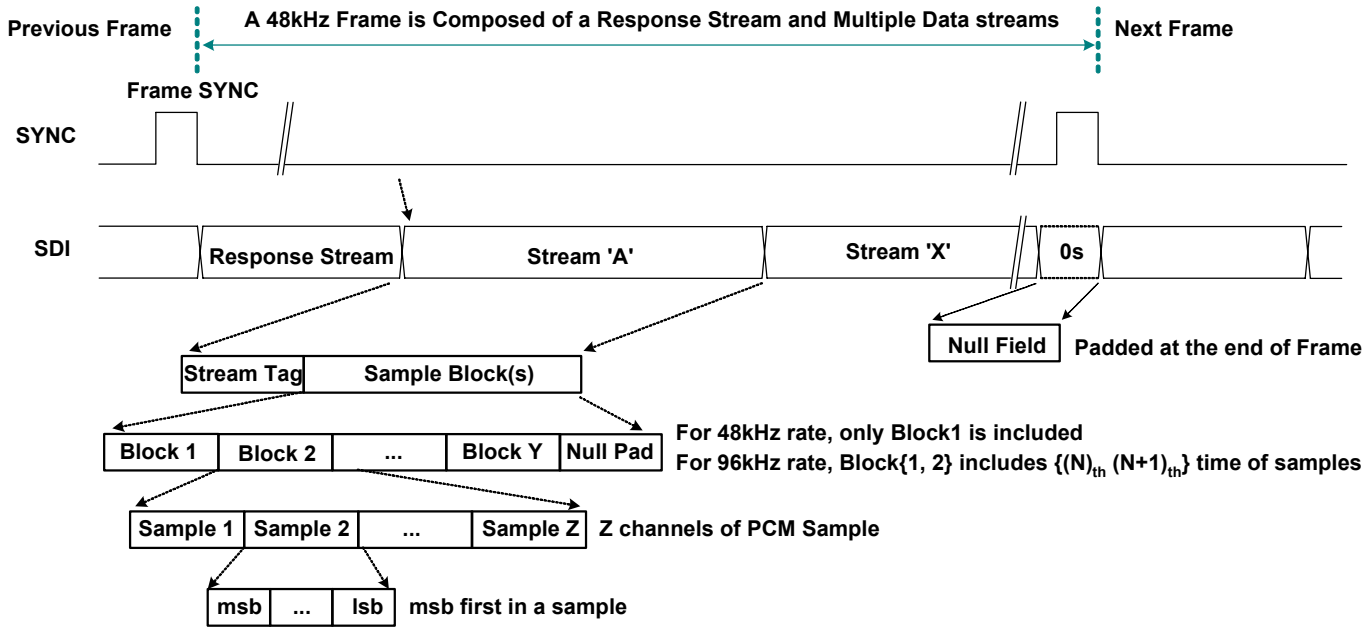


Figure 14. SDI Inbound Stream

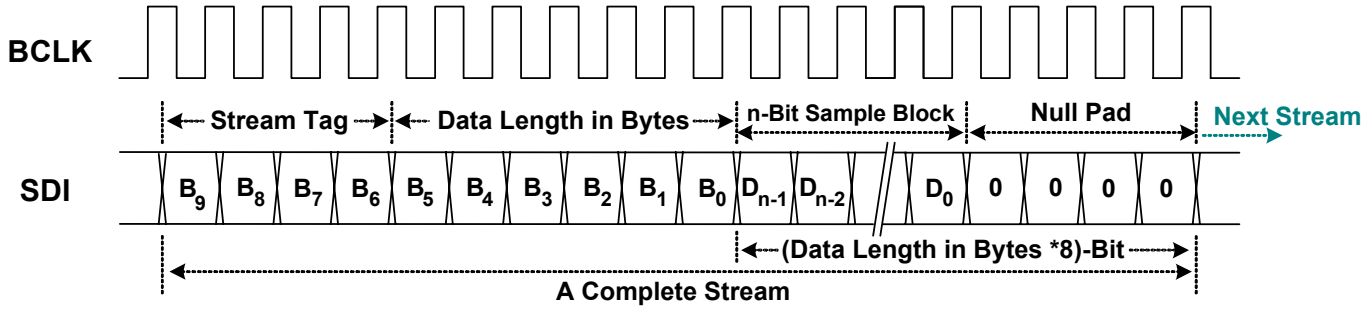


Figure 15. SDI Stream Tag and Data

7.2.4. Inbound Frame – Multiple SDI

A codec can deliver data to the controller on multiple SDIs to achieve higher bandwidth. If an inbound stream exceeds the data transfer limits of a single SDI, the codec can divide the data onto separate SDI signals, each of which operate independently, with different stream numbers at the same frame time. This is similar to having multiple codecs connected to the controller. The controller samples the divided stream into separate memory with multiple DMA descriptors, then software re-combines the divided data into a meaningful stream.

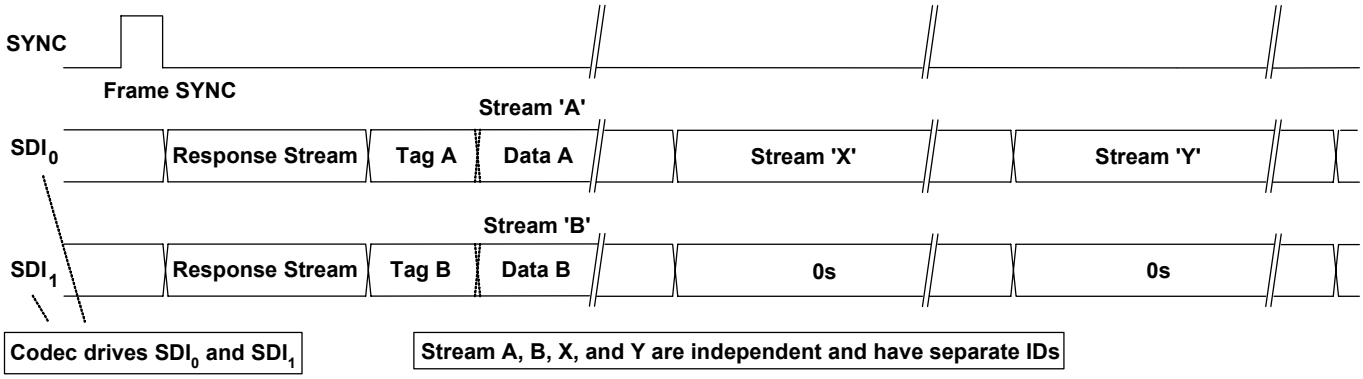


Figure 16. Codec Transmits Data Over Multiple SDIs

7.2.5. Variable Sample Rates

The HDA link is designed for sample rates of 48kHz. Variable rates of sample are delivered in multiple or sub-multiple rates of 48kHz. Two sample blocks per frame result in a 96kHz delivery rate, one sample block over two frames results in a 24kHz delivery rate. The HDA specification states that the sample rate of the outbound stream be synchronized by the controller, not by the codec. Each stream has its own sample rate, independent of any other stream.

The HDA controller supports 48kHz and 44.1kHz base rates. Table 7, page 22, shows the recommended sample rates based on multiples or sub-multiples of one of the two base rates.

Rates in sub-multiples (1/n) of 48kHz are interleaving n frames containing no sample blocks. Rates in multiples (n) of 48kHz contain n sample blocks in a frame. Table 8, page 22, shows the delivery cadence of variable rates based on 48kHz.

The HDA link is defined to operate at a fixed 48kHz frame rate. To deliver samples in (sub) multiple rates of 44.1kHz, an appropriate ratio between 44.1kHz and 48kHz must be maintained to avoid frequency drift. The appropriate ratio between 44.1kHz and 48kHz is 147/160. Meaning 147 sample blocks are transmitted every 160 frames.

The cadence '12-11-11-12-11-11-12-11-11-12-11-11-11- (repeat)' interleaves 13 frames containing no sample blocks in every 160 frames. It provides a low long-term frequency drift for 44.1kHz of delivery rate. Rates in sub-multiples (1/n) of 44.1kHz also follow this cadence and interleave n empty frames. Rates in multiples (n) of 44.1kHz applying this cadence contain n sample blocks in the non-empty frame and interleave an empty frame between non-empty frames (Table 9, page 23).

Table 7. Defined Sample Rate and Transmission Rate

(Sub) Multiple	48kHz Base	44.1kHz Base
1/6	8kHz (1 sample block every 6 frames)	-
1/4	12kHz (1 sample block every 4 frames)	11.025kHz (1 sample block every 4 frames)
1/3	16kHz (1 sample block every 3 frames)	-
1/2	-	22.05kHz (1 sample block every 2 frames)
2/3	32kHz (2 sample blocks every 3 frames)	-
1	48kHz (1 sample block per frame)	44.1kHz (1 sample block per frame)
2	96kHz (2 sample blocks per frame)	88.2kHz (2 sample blocks per frame)
4	192kHz (4 sample blocks per frame)	176.4kHz (4 sample blocks per frame)

Table 8. 48kHz Variable Rate of Delivery Timing

Rate	Delivery Cadence	Description
8kHz	YNNNNN (repeat)	One sample block is transmitted in every 6 frames
12kHz	YNNN (repeat)	One sample block is transmitted in every 4 frames
16kHz	YNN (repeat)	One sample block is transmitted in every 3 frames
32kHz	Y^2NN (repeat)	One sample block is transmitted in every 6 frames
48kHz	Y (repeat)	One sample block is transmitted in every 6 frames
96kHz	Y^2 (repeat)	Two sample blocks are transmitted in each frame
192kHz	Y^4 (repeat)	Four sample blocks are transmitted in each frame

N: No sample block in a frame.
Y: One sample block in a frame.
Y^x: X sample blocks in a frame.

Table 9. 44.1kHz Variable Rate of Delivery Timing

Rate	Delivery Cadence
11.025kHz	{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{11}{-} (repeat)
22.05kHz	{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{11}{-} (repeat)
44.1kHz	12-11-11-12-11-11-12-11-11-12-11-11-11- (repeat)
88.2kHz	12^2-11^2-11^2-12^2-11^2-11^2-12^2-11^2-11^2-12^2-11^2-11^2-11^2- (repeat)
174.4kHz	12^4-11^4-11^4-12^4-11^4-11^4-12^4-11^4-11^4-12^4-11^4-11^4-11^4- (repeat)

11.025kHz: {12}=YNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNN

{11}=YNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNN

{ - }=NNNN

22.050kHz: {12}=YNYNYNYNYNYNYNYNYNYNYNYN

{11}=YNYNYNYNYNYNYNYNYNYNYN

{ - }=NN

44.1kHz 12- =Contiguous 12 frames containing 1 sample blocks each, followed by one frame with no sample block.

88.2kHz 122- =Contiguous 12 frames containing 2 sample blocks each, followed by one frame with no sample block.

174.4kHz 124- =Contiguous 12 frames containing 4 sample blocks each, followed by one frame with no sample block.

7.3. Reset and Initialization

There are two types of reset within an HDA link:

- Link Reset. Generated by assertion of the RST# signal, all codecs return to their power on state
- Codec Reset. Generated by software directing a command to reset a specific codec back to its default state

An initialization sequence is requested after any of the following three events:

1. Link Reset

2. Codec Reset

3. Codec changes its power state (For example, hot docking a codec to an HDA system)

7.3.1. Link Reset

A link reset may be caused by 3 events:

1. The HDA controller asserts RST# for any reason (power up, or PCI reset)

2. Software initiates a link reset via the 'CRST' bit in the Global Control Register (GCR) of the HDA controller

3. Software initiates power management sequences. Figure 17, page 25, shows the 'Link Reset' timing including the 'Enter' sequence (❶~❺) and 'Exit' sequence (❻~❾)

Enter 'Link Reset':

❶ Software writes a 0 to the 'CRST' bit in the Global Control Register of the HDA controller to initiate a link reset

❷ As the controller completes the current frame, it does not signal the normal 8-bit frame SYNC at the end of the frame

❸ The controller drives SYNC and all SDOs to low. Codecs also drive SDIs to low

❹ The controller asserts the RST# signal to low, and enters the 'Link Reset' state

❺ All link signals driven by controller and codecs should be tri-state by internal pull low resistors

Exit from ‘Link Reset’:

❻ If BCLK is re-started for any reason (codec wake-up event, power management, etc.)

❼ Software is responsible for de-asserting RST# after a minimum of 100µsec BCLK running time (the 100µsec provides time for the codec PLL to stabilize)

❽ Minimum of 4 BCLK after RST# is de-asserted, the controller starts to signal normal frame SYNC

❾ When the codec drives its SDI to request an initialization sequence (when the SDI is driven high at the last bit of frame SYNC, it means the codec requests an initialization sequence)

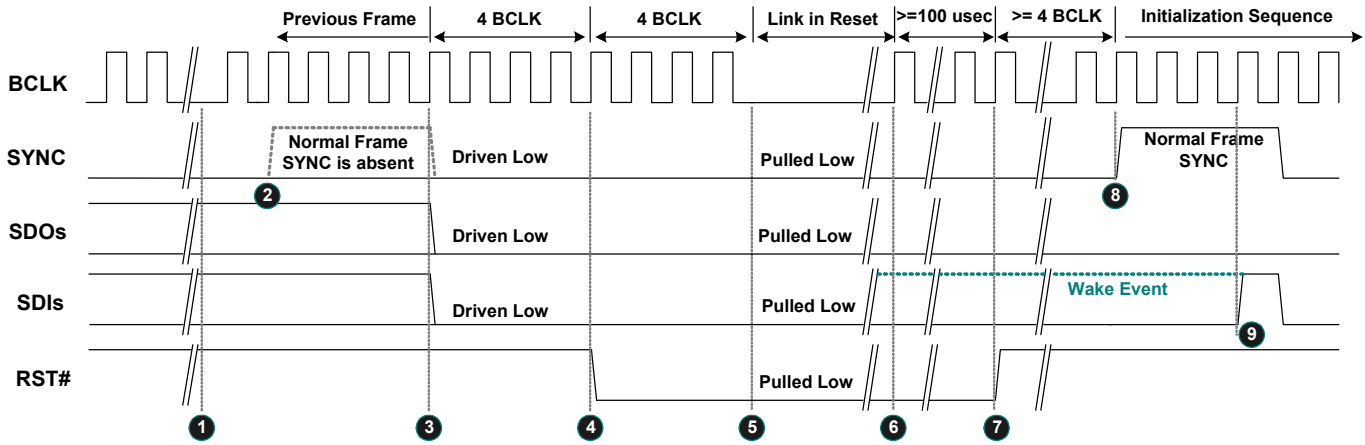


Figure 17. Link Reset Timing

7.3.2. Codec Reset

A ‘Codec Reset’ is initiated via the Codec RESET command verb. It results in the target codec being reset to the default state. After the target codec completes its reset operation, an initialization sequence is requested.

In ALC262 D version, the extend power state of conforming to Intel low power ECR the function reset could not initialize the register setting. Host SW needs to send ‘two’ function reset consecutively to reset all settings.

7.3.3. Codec Initialization Sequence

❶ The codec drives SDI high at the last bit of SYNC to request a Codec Address (CAD) from the controller.

❷ The codec will stop driving the SDI during this turnaround period.

❸❹❺❻ The controller drives SDI to assign a CAD to the codec.

❼ The controller releases the SDI after the CAD has been assigned.

❽ Normal operation state

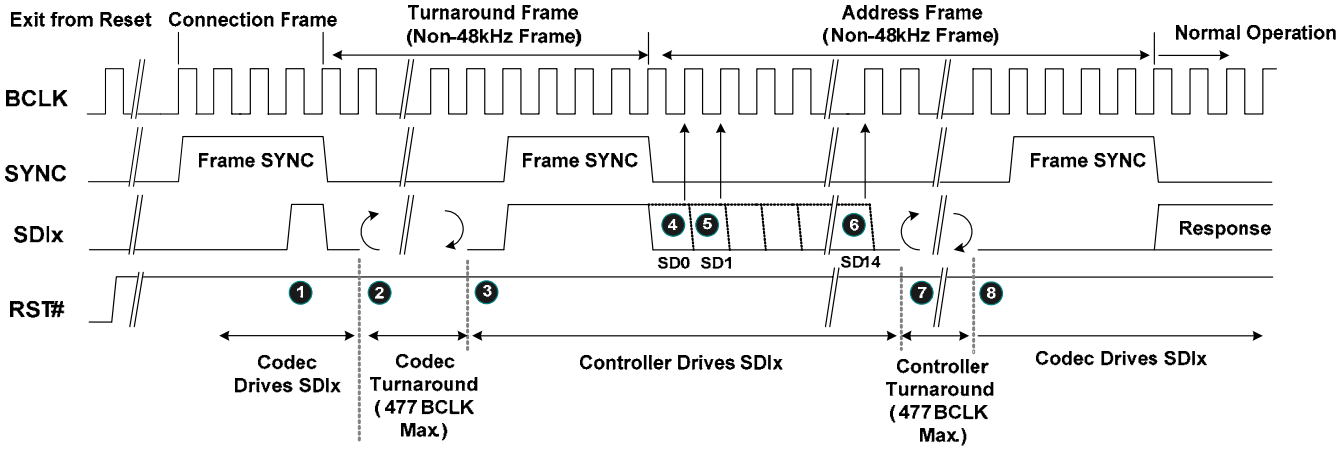


Figure 18. Codec Initialization Sequence

7.4. Verb and Response Format

7.4.1. Command Verb Format

There are two types of verbs: one with 4-bit identifiers (4-bit verbs) and 16-bits of data, the other with 12-bit identifiers (12-bit verbs) and 8-bits of data. Table 10 shows the 4-bit verb structure of a command stream sent from the controller to operate the codec. Table 11 is the 12-bit verb structure that gets and controls parameters in the codec.

Table 10. 40-bit Commands in 4-bit Verb Format

Bit [39:32]	Bit [31:28]	Bit [27:20]	Bit [19:16]	Bit [15:0]
Reserved	Codec Address	Node ID	Verb ID	Payload

Table 11. 40-bit Commands in 12-bit Verb Format

Bit [39:32]	Bit [31:28]	Bit [27:20]	Bit [19:8]	Bit [7:0]
Reserved	Codec Address	Node ID	Verb ID	Payload

7.4.2. Response Format

There are two types of response from the codec to the controller. Solicited Responses are returned by the codec in response to a current command verb. The codec will send Solicited Response data in the next frame, without regard to the Set (Write) or Get (Read) command. The 32-bit Response is interpreted by software, opaque to the controller.

Unsolicited Responses are sent by the codec independently of software requests. Jack Detection or GPI status information can be actively delivered to the controller and interpreted by software. The 'Tag' in Bit[31:28] is used to identify unsolicited events. This tag is undefined in the HDA specifications.

Table 12. Solicited Response Format

Bit [35]	Bit [34]	Bit [33:32]	Bit [31:0]
Valid	Unsol=0	Reserved	Response

Table 13. Unsolicited Response Format

Bit [35]	Bit [34]	Bit [33:32]	Bit [31:28]	Bit [27:0]
Valid	Unsol=1	Reserved	Tag	Response

Note: The response stream in the link protocol is 36-bits wide. The response is placed in the lower 32-bit field. Bit-35 is a 'Valid' bit to indicate the response is 'Ready'. Bit-34 is set to indicate that an unsolicited response was sent.

7.5. Power Management

7.5.1. ALC262 A/B/C Versions

The ALC262 does not support Wake-Up events when in low power mode. All power management state changes in widgets are driven by software. Table 14 shows the System Power State Definitions.

In the ALC262, all the widgets include output/input converters support power control. Software may have various power states depending on system configuration. Table 15 indicates those nodes that support power management. To simplify power control, software can configure whole codec power states through the audio function (NID=01h). Output converters (DACs) and input converters (ADCs) have *no* individual power control to supply fine-grained power control.

7.5.1.1 System Power State Definitions

Table 14. System Power State Definitions

Power States	Definitions
D0	All Power On. Individual DACs and ADCs can be powered up or down as required.
D1	All amplifiers and converters (DACs and ADCs) are powered down. State maintained, analog reference stays up.
D2	All amplifiers and converters (DACs and ADCs) are powered down. State maintained, but analog reference off (D1 + analog reference off).
D3 (Hot)	Power Still Supplied. The codec stops the internal clock. State is maintained.
D3 (Cold)	All Power Removed. State lost.

7.5.1.2 Power Controls in NID is 01h, 02h~05h, 07h~09h

Table 15. Power Controls in NID is 01h, 02h~05h, 07h~09h

	Description	D0	D1	D2	D3 (Hot/Cold)	Link Reset
Audio Function (NID=01h)	LINK Response	Normal	Normal	Normal	PD	PD
	DAC	Normal	PD	PD	PD	PD
	LINE ADC	Normal	PD	PD	PD	PD
	MIX ADC	Normal	PD	PD	PD	PD
	All Headphone Drivers	Normal	Normal	PD	PD	Normal
	All Mixers	Normal	Normal	PD	PD	Normal
	All Reference	Normal	Normal	PD	PD	Normal

Note: PD=Powered Down.

7.5.1.3 ALC262 Version A/B/C Powered Down Conditions

Table 16. ALC262 Version A/B/C Powered Down Conditions

Condition	Description
LINK Response powered down	Internal clock is stopped. SDATA-IN and S/PDIF-OUT are floated with pulled low 47K resistors internally. Detection of 'Link Reset Entry' and 'Link Reset Exit' sequences are supported. All states are maintained if DVDD is supplied.
LOUT DAC powered down	Analog block and digital filter are powered down.
LINE ADC powered down	Analog block and digital filter are powered down. The data on SDATA-IN is quiet.
MIX ADC powered down	Analog block and digital filter are powered down. The data on SDATA-IN is quiet.
Headphone Driver powered down	All headphone drivers are powered down.
Mixers powered down	All internal mixer widgets are powered down. The DC reference and VREFOUTx at individual pin complex are still alive.
Reference power down	All internal references, DC reference, and VREFOUTx at individual pin complexes are off.

7.5.2. ALC262 D Version

The ALC262 version D is designed to meet Intel's low-power-state white paper and is ECR HDA-015B compliant. It meets the five attributes discussed in the white paper:

1. D3 state power < 30mW.

2. Exit latency (D3 to D0 transfer) < 10ms.

3. Audio pop/click suppression during D3 and D0 transition < -65dBV.

4. Supports Jack detection in D3 state.

5. D3 functions with or without the BITCLK

The ALC262-VD minimizes D3 state idle mode power consumption and increases overall battery life in mobile systems.

In D3 mode, only a power on reset or a 'double function reset' resets all ALC262-VD settings, cutting software configuration time spent entering/leaving D3 state, and reducing latency time for D3 to D0 transitions.

The ALC262-VD supports Wake-Up events in D3 mode, including jack detection and GPIO status changes. If the HDA-Link was alive (with BCLK), the ALC262-VD Wake-Up response is as normal. If no BITCLK is present, the ALC262-VD drives the SDI high in order to wake up the system.

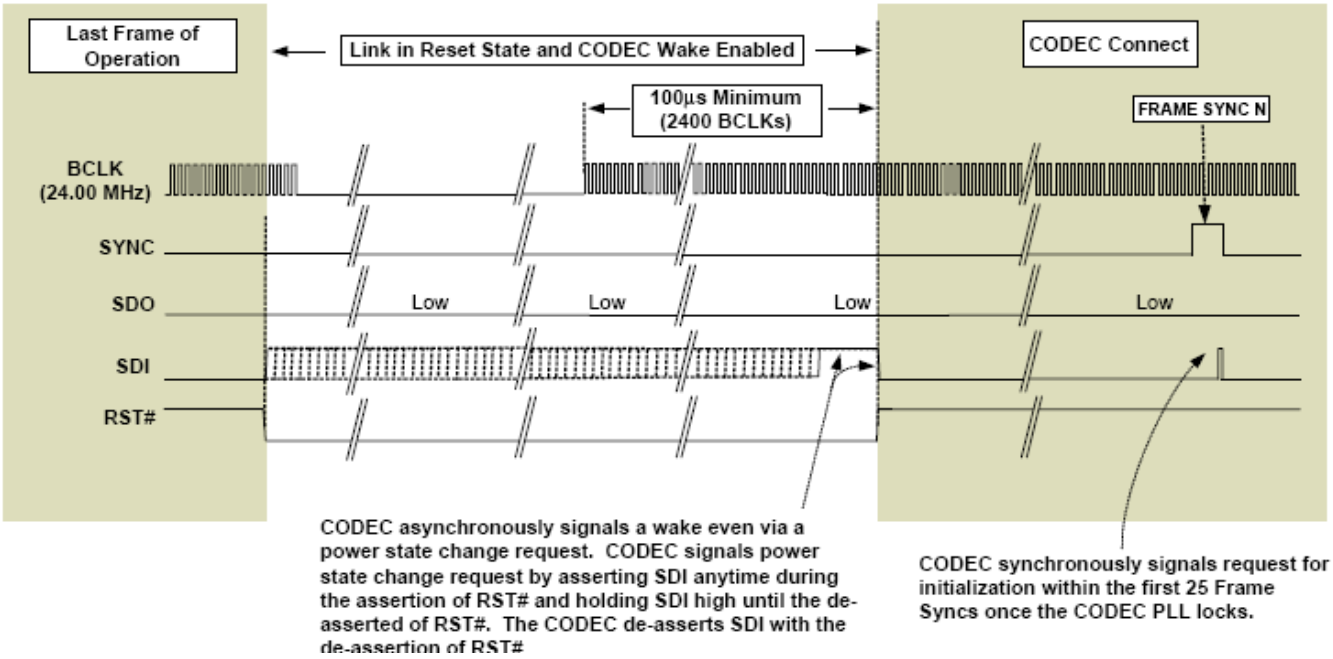


Figure 19. Codec Initialization Sequence

All power management state changes in widgets are driven by software. Table 17 indicates the definitions of power states.

In the ALC262-VD, the Audio Function (NID=01h), input converter, output converter, and each pin widget supports power control. Software may have various power states dependent on system configuration. Table 17 indicates those Nodes that support power management. To simplify power control, software can configure whole codec power states using only the Audio Function (NID=01h). Output converters (DACs) and input converters (ADCs) have no individual power control to supply fine-Grained power control.

7.5.2.1 ALC262-VD Supports Power Controls in NID 01h, 02h~03h, 06h, 07h~0Ah, 10h~12h, 14h~1Fh

Table 17. ALC262-VD Supports Power Controls in NID 01h, 02h~03h, 06h, 07h~0Ah, 10h~12h, 14h~1Fh

	Description	D0	D1	D2	D3	D3 (No BCLK)	Link Reset
Audio Function (NID=01h)	LINK Response	Normal	Normal	Normal	PD	PD	PD
	DAC	Normal	PD	PD	PD	PD	PD
	LINE ADC	Normal	PD	PD	PD	PD	PD
	MIX ADC	Normal	PD	PD	PD	PD	PD
	All Headphone Drivers	Normal	Normal	PD	PD	PD	Normal
	All Mixers	Normal	Normal	PD	PD	PD	Normal
	All Reference	Normal	Normal	PD	PD	PD	Normal

7.5.2.2 ALC262 Version D Powered Down Conditions

Table 18. ALC262 Version D Powered Down Conditions

Condition	Description
LINK Response powered down	Internal clock is stopped. SDATA-IN and S/PDIF-OUT are floated with pulled low 47K resistors internally. Detection of 'Link Reset Entry' and 'Link Reset Exit' sequences are supported. All states are maintained if DVDD is supplied.
LOUT DAC powered down	Analog block and digital filter are powered down.
LINE ADC powered down	Analog block and digital filter are powered down. The data on SDATA-IN is quiet.
MIX ADC powered down	Analog block and digital filter are powered down. The data on SDATA-IN is quiet.
Headphone Driver powered down	All headphone drivers are powered down.
Mixers powered down	All internal mixer widgets are powered down. The DC reference and VREFOUTx at individual pin complexes are still alive.
Reference power down	All internal references, DC reference, and VREFOUTx at individual pin complexes are off.

8. Supported Verbs and Parameters

This section describes the Verbs and Parameters supported by various widgets in the ALC262. If a verb is not supported by the addressed widget, it will respond with 32 bits of '0'.

8.1. Verb – Get Parameters (Verb ID=F00h)

The 'Get Parameters' verb is used to get system information and the function capabilities of the HDA codec. All the parameters are read-only. Refer to section 7.4.1 Command Verb Format, page 27, to get detailed information about supported parameters.

Table 19. Verb – Get Parameters (Verb ID=F00h)

Get Parameter Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=00h	Verb ID=F00h	Parameter ID[7:0]

Codec Response Format

Response [31:0]
32-bit Response

Note: If the parameter ID is not supported, the returned response is 32 bits of '0'.

8.1.1. Parameter – Vendor ID (Verb ID=F00h, Parameter ID=00h)

Table 20. Parameter – Vendor ID (Verb ID=F00h, Parameter ID=00h)

Codec Response Format

Bit	Description
31:16	Vendor ID=10ECh (Realtek's PCI vendor ID).
15:0	Device ID=0262h.

Note: The Root Node (NID=00h) supports this parameter.

8.1.2. Parameter – Revision ID (Verb ID=F00h, Parameter ID=02h)

Table 21. Parameter – Revision ID (Verb ID=F00h, Parameter ID=02h)

Codec Response Format

Bit	Description
31:24	Reserved. Read as 0's.
23:20	MajRev. The major version number (in decimal) of the HDA Spec to which the ALC262 is fully compliant.
19:16	MinRev. The minor version number (in decimal) of the HDA Spec to which the ALC262 is fully compliant.
15:8	Revision ID. The vendor's revision number. 00h is for the first silicon version, 01h is for the second version, etc.
7:0	Stepping ID. The vendor's stepping number within the given Revision ID.

Note: The Root Node (NID=00h in the ALC262) supports this parameter.

8.1.3. Parameter – Subordinate Node Count (Verb ID=F00h, Parameter ID=04h)

For the root node, the Subordinate Node Count provides information about audio function group nodes associated with the root node.

For function group nodes, it provides the total number of widgets associated with this function node.

Table 22. Parameter – Subordinate Node Count (Verb ID=F00h, Parameter ID=04h)

Codec Response Format

Bit	Description
31:24	Reserved. Read as 0's.
23:16	Starting Node Number. The starting node number in the sequential widgets.
15:8	Reserved. Read as 0's.
7:0	Total Number of Nodes. For a root node, the total number of function groups in the root node. For a function group, the total number of widget nodes in the function group.

8.1.4. Parameter – Function Group Type (Verb ID=F00h, Parameter ID=05h)

Table 23. Parameter – Function Group Type (Verb ID=F00h, Parameter ID=05h)

Codec Response Format

Bit	Description
31:8	Reserved. Read as 0's.
7:0	Function Group Type. 00h: Reserved 01h: Audio Function 02h: Modem Function 03h~7Fh: Reserved 80h~FFh: Vendor Defined Function.

Note: The Audio Function Group (NID=01h) supports this parameter.

8.1.5. Parameter – Audio Function Capabilities (Verb ID=F00h, Parameter ID=08h)

Table 24. Parameter – Audio Function Capabilities (Verb ID=F00h, Parameter ID=08h)

Codec Response Format

Bit	Description
31:17	Reserved. Read as 0's.
16	Beep Generator. A '1' indicates the presence of an integrated Beep generator within the Audio Function Group.
15:12	Reserved. Read as 0's.
11:8	Input Delay.
7:4	Reserved. Read as 0's.
3:0	Output Delay.

Note: The Audio Function Group (NID=01h) supports this parameter.

8.1.6. Parameter – Audio Widget Capabilities (Verb ID=F00h, Parameter ID=09h)

Table 25. Parameter – Audio Widget Capabilities (Verb ID=F00h, Parameter ID=09h)

Codec Response Format

Bit	Description
31:24	Reserved. Read as 0's.
23:20	Widget Type. 0h: Audio Output 1h: Audio Input 2h: Mixer 3h: Selector 4h: Pin Complex 5h: Power Widget 6h: Volume Knob Widget 7h~Eh: Reserved Fh: Vendor defined audio widget
19:16	Delay. Samples delayed between the HDA link and widgets.
15:11	Reserved. Read as 0's.
10	Power Control. 0: Power state control is not supported on this widget 1: Power state is supported on this widget
9	Digital. 0: An analog input or output converter 1: A widget translating digital data between the HDA link and digital I/O (S/PDIF, I2S, etc.)
8	ConnList. Connection List. 0: Connected to HDA link. No Connection List Entry should be queried 1: Connection List Entry must be queried
7	UnsolCap. Unsolicited Capable. 0: Unsolicited response is not supported 1: Unsolicited response is supported
6	ProcWidget. Processing Widget. 0: No processing control 1: Processing control is supported
5	Reserved. Read as 0.
4	Format Override.
3	AmpParOvr, AMP Param Override.
2	OutAmpPre, Out AMP Present.
1	InAmpPre, In AMP Present.
0	Stereo. 0: Mono Widget 1: Stereo Widget

8.1.7. Parameter – Supported PCM Size, Rates (Verb ID=F00h, Parameter ID=0Ah)

Parameter in audio function provides default information about formats. Individual converters have their own parameters to provide supported formats if their 'Format Override' bit is set.

Table 26. Parameter – Supported PCM Size, Rates (Verb ID=F00h, Parameter ID=0Ah)

Codec Response Format

Bit	Description
31:21	Reserved. Read as 0's.
20	B32: Indicates whether 32-bit audio format is supported. 0: Not supported 1: Supported
19	B24: Indicates whether 24-bit audio format is supported. 0: Not supported 1: Supported
18	B20: Indicates whether 20-bit audio format is supported. 0: Not supported 1: Supported
17	B16: Indicates whether 16-bit audio format is supported. 0: Not supported 1: Supported
16	B8: Indicates whether 8-bit audio format is supported. 0: Not supported 1: Supported
15:12	Reserved. Read as 0's.
11	R12: Indicates whether 384kHz (=8*48kHz) rate is supported. 0: Not supported 1: Supported
10	R11: Indicates whether 192kHz (=4*48kHz) rate is supported. 0: Not supported 1: Supported
9	R10: Indicates whether 176.4kHz (=4*44.1kHz) rate is supported. 0: Not supported 1: Supported
8	R9: Indicates whether 96kHz (=2*48kHz) rate is supported. 0: Not supported 1: Supported
7	R8: Indicates whether 88.2kHz (=2*44.1kHz) rate is supported. 0: Not supported 1: Supported
6	R7: Indicates whether 48kHz rate is supported. 0: Not supported 1: Supported
5	R6: Indicates whether 44.1kHz rate is supported. 0: Not supported 1: Supported
4	R5: Indicates whether 32kHz (=2/3*48kHz) rate is supported. 0: Not supported 1: Supported
3	R4: Indicates whether 22.05kHz (=1/2*44.1kHz) rate is supported. 0: Not supported 1: Supported
2	R3: Indicates whether 16kHz (=1/3*48kHz) rate is supported. 0: Not supported 1: Supported
1	R2: Indicates whether 11.025kHz (=1/4*44.1kHz) rate is supported. 0: Not supported 1: Supported
0	R1: Indicates whether 8kHz (=1/6*48kHz) rate is supported. 0: Not supported 1: Supported

8.1.8. Parameter – Supported Stream Formats (Verb ID=F00h, Parameter ID=0Bh)

Parameters in this node only provide default information for audio function groups. Individual converters have their own parameters to provide supported formats if the 'Format Override' bit is set.

Table 27. Parameter – Supported Stream Formats (Verb ID=F00h, Parameter ID=0Bh)

Codec Response Format

Bit	Description
31:3	Reserved. Read as 0's.
2	AC3. 0: Not supported 1: Supported
1	Float32. 0: Not supported 1: Supported
0	PCM. 0: Not supported 1: Supported

Note: Input converters and output converters support this parameter.

8.1.9. Parameter – Pin Capabilities (Verb ID=F00h, Parameter ID=0Ch)

The Pin Capabilities parameter returns a bit field describing the capabilities of the Pin Complex widget.

Table 28. Parameter – Pin Capabilities (Verb ID=F00h, Parameter ID=0Ch)

Codec Response Format

Bit	Description
31:16	Reserved. Read as 0's.
15:8	VREF Control Capability. '1' in corresponding bit field indicates signal levels of associated Vrefout are specified as a percentage of AVDD.

7:6	5	4	3	2	1	0
Reserved	100%	80%	Reserved	Ground	50%	Hi-Z

Bit	Description
7	L-R Swap. Indicates the capability of swapping the left and rights.
6	Balanced I/O Pin. '1' indicates this pin complex has balanced pins.
5	Input Capable. '1' indicates this pin complex supports input.
4	Output Capable. '1' indicates this pin complex supports output.
3	Headphone Drive Capable. '1' indicates this pin complex has an amplifier to drive a headphone.
2	Presence Detect Capable. '1' indicates this pin complex can detect whether there is anything plugged in.
1	Trigger Required. '1' indicates whether a software trigger is required for an impedance measurement.
0	Impedance Sense Capable. '1' indicates this pin complex can perform analog sense on the attached device to determine its type.

Note: Only Pin Complex widgets support this parameter.

8.1.10. Parameter – Amplifier Capabilities (Verb ID=F00h, Input Amplifier Parameter ID=0Dh)

Parameters in this node provide audio function group default information. Individual converters have their own parameters to provide amplifier capabilities if the 'AMP Param Override' bit is set.

Table 29. Parameter – Amplifier Capabilities (Verb ID=F00h, Input Amplifier Parameter ID=0Dh)

Codec Response Format

Bit	Description
31	(Input) Mute Capable.
30:23	Reserved. Read as 0.
22:16	Step Size. Indicates the size of each step in the gain range. Each step may be 0~32dB, specified in 0.25dB steps. '0' indicates a step of 0.25dB. '127' indicates a step of 32dB.
15	Reserved. Read as 0.
14:8	Number of Steps. Indicates the number of steps in the gain range. '0' means the gain is fixed.
7	Reserved. Read as 0.
6:0	Offset. Indicates which step is 0dB.

8.1.11. Parameter – Amplifier Capabilities (Verb ID=F00h, Output Amplifier Parameter ID=12h)

Parameters in this node provide audio function group default information. Individual converters have their own parameters to provide amplifier capabilities if the 'AMP Param Override' bit is set.

Table 30. Parameter – Amplifier Capabilities (Verb ID=F00h, Output Amplifier Parameter ID=12h)

Codec Response Format

Bit	Description
31	(Output) Mute Capable.
30:23	Reserved. Read as 0.
22:16	Step Size. Indicates the size of each step in the gain range. Each step may be 0~32dB, specified in 0.25dB steps. '0' indicates a step of 0.25dB. '127' indicates a step of 32dB.
15	Reserved. Read as 0.
14:8	Number of Steps. Indicates the number of steps in the gain range. '0' means the gain is fixed.
7	Reserved. Read as 0.
6:0	Offset. Indicates which step is 0dB.

8.1.12. Parameter – Connect List Length (Verb ID=F00h, Parameter ID=0Eh)

Parameters in this node provide audio function widget connection information.

Table 31. Parameter – Connect List Length (Verb ID=F00h, Parameter ID=0Eh)

Codec Response Format

Bit	Description
31:8	Reserved. Read as 0.
7	Short Form. 0: Short Form 1: Long Form
6:0	Connect List Length. Indicates the number of inputs connected to a widget. If the Connect List Length is 1, there is only one input, and there is no Connection Select Control (Not a MUX widget).

8.1.13. Parameter – Supported Power States (Verb ID=F00h, Parameter ID=0Fh) (ALC262 A/B/C Version)

Table 32. Parameter – Supported Power States (Verb ID=F00h, Parameter ID=0Fh) (ALC262 A/B/C Version)

Bit	Description
31:4	Reserved. Read as 0's.
3	D3Sup. 1: Power state D3 is supported.
2	D2Sup. 1: Power state D2 is supported.
1	D1Sup. 1: Power state D1 is supported.
0	D0Sup 1: Power state D0 is supported.

8.1.14. Parameter – Supported Power States (Verb ID=F00h, Parameter ID=0Fh) (ALC262 D Version)

The ALC262 version D is designed to meet Intel's low-power-state white paper and is ECR HDA-015B compliant.

Table 33. Parameter – Supported Power States (Verb ID=F00h, Parameter ID=0Fh) (ALC262 D Version)

Codec Response Format

Bit	Description
31	Extended Power States Supported (EPSS) 1: Extended power state EPSS is supported.
30	CLKSTOP 1: D3 mode operates even when no BITCLK presents on the link.
29:4	Reserved, read as 0s.
3	D3Sup. 1: Power state D3 is supported.
2	D2Sup. 1: Power state D2 is supported.
1	D1Sup. 1: Power state D1 is supported.
0	D0Sup 1: Power state D0 is supported.

8.1.15. Parameter – Processing Capabilities (Verb ID=F00h, Parameter ID=10h)

Table 34. Parameter – Processing Capabilities (Verb ID=F00h, Parameter ID=10h)

Codec Response Format

Bit	Description
31:16	Reserved. Read as 0's.
15:8	NumCoeff. Number of Coefficient
7:1	Reserved. Read as 0's.
0	Benign. 0: Processing unit is not linear, nor is it time variant 1: Processing unit is linear and is time invariant

8.1.16. Parameter – GPIO Capabilities (Verb ID=F00h, Parameter ID=11h)

Table 35. Parameter – GPIO Capabilities (Verb ID=F00h, Parameter ID=11h)

Codec Response Format

Bit	Description
31	GPIWake=0. The ALC262 does not support GPIO wake up function.
30	GPIUnsol=1. The ALC262 supports GPIO unsolicited response.
29:24	Reserved. Read as 0's.
23:16	NumGPIs=00h. No GPI pin is supported.
15:8	NumGPOs=00h. No GPO pin is supported.
7:0	NumGPIOs=04h. Two GPIO pins are supported.

8.1.17. Parameter – Volume Knob Capabilities (Verb ID=F00h, Parameter ID=13h)

Table 36. Parameter – Volume Knob Capabilities (Verb ID=F00h, Parameter ID=13h)

Codec Response Format for NID=21h (Volume Control Knob)

Bit	Description
31:8	Reserved. Read as 0's.
7	Delta. 0: Software cannot modify the Volume Control Knob volume 1: Software can write a base volume to the Volume Control Knob
6:0	NumSteps. The number of steps in the range of the Volume Control Knob

8.2. Verb – Get Connection Select Control (Verb ID=F01h)

Table 37. Verb – Get Connection Select Control (Verb ID=F01h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F01h	0's

Codec Response Format

Response [31:0]
Bit[7:0] are Connection Index

Codec Response for Analog Port-A/B/C/D/E/F

Bit	Description
31:8	0's.
7:0	Connection Index Currently Set (Default value is 00h). 00h: Sum Widget NID=0Ch 01h: Sum Widget NID=0Dh Other: Reserved

Codec Response for Digital Pin S/PDIF-OUT

Bit	Description
31:8	0's.
7:0	Connection Index Currently Set (Default value is 00h). 00h: Digital Converter (S/PDIF-OUT) Other: Reserved

Codec Response for Digital Pin S/PDIF-OUT2 (ALC262 D version only)

Bit	Description
31:8	0's.
7:0	Connection Index Currently Set (Default value is 00h). 00h: Digital Converter (S/PDIF-OUT) Other: Reserved

Codec Response for NID=22hh (Mixer) (ALC262 C version only)

Bit	Description
31:8	0's.
7:0	Connection Index Currently Set (Default value is 00h). 00h: Pin Complex – MIC1 NID=18h 01h: Pin Complex – MIC2 NID=19h 02h: Pin Complex – LINE1 NID=1Ah 03h: Pin Complex – LINE2 NID=1Bh 04h: Pin Complex – CD_IN NID=1Ch 05h: Pin Complex – PCBEEP NID=1Dh 06h: Pin Complex – LINE_OUT NID=14h 07h: Pin Complex – HP_OUT NID=15h 08h: Pin Complex – Sum Widget NID=0Bh 09h: Pin Complex – DMIC NID=12h Other: Reserved

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.3. Verb – Set Connection Select (Verb ID=701h)

Table 38. Verb – Set Connection Select (Verb ID=701h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=701h	Select Index [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

8.4. Verb – Get Connection List Entry (Verb ID=F02h)

Table 39. Verb – Get Connection List Entry (Verb ID=F02h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F02h	Offset Index - N[7:0]

Codec Response Format

Response [31:0]
32-bit Response

Codec Response for NID=07h (MIC ADC)

Bit	Description
31:8	Connection List Entry (N+3), (N+2) and (N+1). Returns 000000h.
7:0	Connection List Entry (N). Returns 24h (Sum Widget) for N=0~3. Returns 00h for N>3.

Codec Response for NID=08h (LINE ADC)

Bit	Description
31:8	Connection List Entry (N+3), (N+2) and (N+1). Returns 000000h.
7:0	Connection List Entry (N). Returns 23h (Sum Widget) for N=0~3. Returns 00h for N>3.

Codec Response for NID=09h (MIX ADC)

Bit	Description
15:8	Connection List Entry (N+3), (N+2) and (N+1). Returns 000000h.
7:0	Connection List Entry (N). Returns 22h (Sum Widget) for N=0~3. Returns 00h for N>3.

Codec Response for NID=0Ah (S/PDIF-IN Converter)

Bit	Description
31:8	Connection List Entry (N+3), (N+2) and (N+1). Returns 000000h.
7:0	Connection List Entry (N). Returns 1Fh (S/PDIF-IN Pin Widget) for N=0~3. Returns 00h for N>3.

Codec Response for NID=0Bh (Mixer)

Bit	Description
31:24	Connection List Entry (N+3). Returns 1Bh (Pin Complex - LINE2) for N=0~3. Returns 00h for N>3.
23:16	Connection List Entry (N+2). Returns 1Ah (Pin Complex - LINE1) for N=0~3. Returns 00h for N>3.
15:8	Connection List Entry (N+1). Returns 19h (Pin Complex - MIC2) for N=0~3. Returns 1Dh (Pin Complex - BEEP) for N=4~7. Returns 00h for N>7.
7:0	Connection List Entry (N). Returns 18h (Pin Complex - MIC1) for N=0~3. Returns 1Ch (Pin Complex - CD) for N=4~7. Returns 00h for N>7.

Codec Response for NID=0Ch

Bit	Description
31:24	Connection List Entry (N). Returns 00h.
23:16	Connection List Entry (N+2). Returns 00h.
15:8	Connection List Entry (N+1). Returns 0Bh (Mixer) for N=0~3. Returns 00h for N>3.
7:0	Connection List Entry (N). Returns 02h (LOUT DAC) for N=0~3. Returns 00h for N>3.

Codec Response for NID=0Dh

Bit	Description
31:24	Connection List Entry (N). Returns 00h.
23:16	Connection List Entry (N+2). Returns 00h.
15:8	Connection List Entry (N+1). Returns 0Bh (Mixer) for N=0~3. Returns 00h for N>3.
7:0	Connection List Entry (N). Returns 03h (HP-OUT DAC) for N=0~3. Returns 00h for N>3.

Codec Response for NID=0Eh)

Bit	Description
31:24	Connection List Entry (N). Returns 00h.
23:16	Connection List Entry (N+2). Returns 00h.
15:8	Connection List Entry (N+1). Returns 0Bh (Mixer) for N=0~3. Returns 00h for N>3.
7:0	Connection List Entry (N). Returns 02h (LINE-OUT DAC) for N=0~3. Returns 00h for N>3.

Codec Response for NID =14h~15h, 18h~1Bh (PORT-A ~ PORT-F)

Bit	Description
31:24	Connection List Entry (N+3). Returns 00h.
23:16	Connection List Entry (N+2). Returns 00h.
15:8	Connection List Entry (N+1). Returns 0Dh (Sum Widget NID=0Dh) for N=0~3. Returns 00h for N>7.
7:0	Connection List Entry (N). Returns 0Ch (Sum Widget NID=0Ch) for N=0~3. Returns 00h for N>7.

Codec Response for NID=16h (Pin Widget: MONO-OUT)

Bit	Description
31:8	Connection List Entry (N+3), (N+2) and (N+1). Returns 000000h.
7:0	Connection List Entry (N). Returns 0Eh for N=0~3. Returns 00h for N>3.

Codec Response for NID=1Eh (Pin Widget: S/PDIF-OUT)

Bit	Description
31:16	Connection List Entry (N+3) and (N+2). Returns 0000h.
15:8	Connection List Entry (N+1). Returns 00h for N>3.
7:0	Connection List Entry (N). Returns 06h (S/PDIF-OUT converter) for N=0~3. Returns 00h for N>3.

Codec Response for NID=11h (Pin Widget: S/PDIF-OUT2 for ALC262 D Version)

Bit	Description
31:16	Connection List Entry (N+3) and (N+2). Returns 0000h.
15:8	Connection List Entry (N+1). Returns 00h for N>3.
7:0	Connection List Entry (N). Returns 06h (S/PDIF-OUT converter) for N=0~3. Returns 00h for N>3.

Codec Response for NID=22h/23h/24h (Sum Widget before MIX/LINE/MIC ADCs)

Bit	Description
31:24	Connection List Entry (N+3). Returns 1Bh (Pin Complex - LINE2) for N=0~3. Returns 15h (Pin Complex-SURR) for N=4~7. Returns 00h for N>7.
23:16	Connection List Entry (N+2). Returns 1Ah (Pin Complex - LINE1) for N=0~3. Returns 14h (Pin Complex - FRONT) for N=4~7. Returns 00h for N>7.
15:8	Connection List Entry (N+1). Returns 19h (Pin Complex - MIC2) for N=0~3. Returns 1Dh (Pin Complex - PCBEEP) for N=4~7. Returns 00h for N>7.
7:0	Connection List Entry (N). Returns 18h (Pin Complex - MIC1) for N=0~3. Returns 1Ch (Pin Complex - CD) for N=4~7. Returns 0Bh (Mixer) for N=8~11. Returns 00h for N>11.

Codec Response for Other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.5. Verb – Get Processing State (Verb ID=F03h)

Table 40. Verb – Get Processing State (Verb ID=F03h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F03h	0's

Codec Response Format

Response [31:0]
32-bit response

Codec Response for All NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.6. Verb – Set Processing State (Verb ID=703h)

Table 41. Verb – Set Processing State (Verb ID=703h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=703h	Processing State [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for All NID

Bit	Description
31:0	0's.

8.7. Verb – Get Coefficient Index (Verb ID=Dh)

Table 42. Verb – Get Coefficient Index (Verb ID=Dh)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
CAd=X	Node ID=Xh	Verb ID=Dh	0's

Codec Response Format

Response [31:0]
Bit [15:0] are Coefficient Index

Codec Response for NID=20h (Realtek Defined Hidden Registers)

Bit	Description
31:16	Reserved. Read as 0's.
15:0	Coefficient Index.

Codec Response for Other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.8. Verb – Set Coefficient Index (Verb ID=5h)

Table 43. Verb – Set Coefficient Index (Verb ID=5h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
CAd=X	Node ID=Xh	Verb ID=5h	Coefficient Index [15:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for All NID

Bit	Description
31:0	0's.

8.9. Verb – Get Processing Coefficient (Verb ID=Ch)

Table 44. Verb – Get Processing Coefficient (Verb ID=Ch)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
CAd=X	Node ID=Xh	Verb ID=Ch	0's

Codec Response Format

Response [31:0]
Processing Coefficient [15:0]

Codec Response for NID=20h (Realtek Defined Hidden Registers)

Bit	Description
31:16	Reserved. Read as 0's.
15:0	Processing Coefficient.

Codec Response for Other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.10. Verb – Set Processing Coefficient (Verb ID=4h)

Table 45. Verb – Set Processing Coefficient (Verb ID=4h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
CAd=X	Node ID=Xh	Verb ID=4h	Coefficient [15:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for All NID

Bit	Description
31:0	0's.

8.11. Verb – Get Amplifier Gain (Verb ID=Bh)

This verb is used to get gain/attenuation settings from each widget.

Table 46. Verb – Get Amplifier Gain (Verb ID=Bh)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
CAd=X	Node ID=Xh	Verb ID=Bh	'Get' payload [15:0]

Codec Response Format

Response [31:0]
Bit[7:0] are responsible for 'Get'

'Get' Payload in Command Bit[15:0]

Bit	Description
15	Get Input/Output. 0: Input amplifier gain is requested1: Output amplifier gain is requested
14	Reserved. Read as 0.
13	Get Left/Right. 0: Right amplifier gain is requested 1: Left amplifier gain is requested
12:4	Reserved. Read as 0's.
3:0	Index[3:0] for Input Source. Select amplifier for this converter. If a widget has no multiple input sources, the index will be ignored

Codec Response for NID=07h (MIC ADC), 08h(LINE ADC) and 09h (MIX ADC)

Bit	Description
31:8	0's.
7	Bit-15 is 0 in 'Get Amplifier Gain': Input Amplifier Mute. 0: Unmute 1: Mute Bit-15 is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Mute).
6:0	Bit-15 is 0 in 'Get Amplifier Gain': Input Amplifier Gain [6:0]. 7-bit step value (0~31) specifying the volume from –16.5B~+30dB in 1.5dB steps. Bit-15 is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Mute).

Codec Response for NID=0Bh (MIXER Sum Widget)

Bit	Description
31:8	0's.
7	Bit-15 is 0 in 'Get Amplifier Gain': Input Amplifier Mute. 0: Unmute 1: Mute (Default for all Index). Bit-15 is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Mute).
6:0	Bit-15 is 0 in 'Get Amplifier Gain': Input Amplifier Gain [6:0]. 7-bit step value (0~31) specifying the volume from –34.5dB~+12dB in 1.5dB steps. Bit-15 is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Mute).

Codec Response for NID=0Ch~0Eh (Sum Widgets)

Bit	Description
31:8	0's.
7	Bit-15 is 0 in 'Get Amplifier Gain': Input Amplifier Mute. 0: Unmute 1: Mute Bit-15 is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Mute).
6:0	Bit-15 is 0 in 'Get Amplifier Gain': Read as 0 (No Input Amplifier Gain). Bit-15 is 1 in 'Get Amplifier Gain': Output Amplifier Gain [6:0]. 7-bit step value (0~31) specifying the volume from –46.5dB~0dB in 1.5dB steps.

Codec Response for NID=14h, 15h, 18h~1Bh (Pin Complex: LINE-OUT/HP-OUT/MIC1/MIC2/LINE1/LINE2)

Bit	Description
31:8	0's.
7	Bit-15 is 0 in 'Get Amplifier Gain': Read as 0. Bit-15 is 1 in 'Get Amplifier Gain': Output Amplifier Mute. 0:Unmute 1:Mute (Default=1)
6:0	Bit-15 is 0 in 'Get Amplifier Gain': Read as 0. Bit-15 is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Gain).

Codec Response for NID=22h, 23h, 24h (Sum Widgets) – In C version, NID=22h is a selector will not support this verb.

Bit	Description
31:8	0's.
7	Bit-15 is 0 in 'Get Amplifier Gain': Input Amplifier Mute. 0: Unmute 1: Mute Bit-15 is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Mute).
6:0	Bit-15 is 0 in 'Get Amplifier Gain': Read as 0 (No Input Amplifier Gain). Bit-15 is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Gain).

Codec Response to Other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.12. Verb – Set Amplifier Gain (Verb ID=3h)

This verb is used to set amplifier gain/attenuation in each widget.

Table 47. Verb – Set Amplifier Gain (Verb ID=3h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=3h	'Set' payload [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Set' Payload in Command Bit[15:0]

Bit	Description
15	Set Output Amp. '1' indicates output amplifier gain will be set.
14	Set Input Amp. '1' indicates input amplifier gain will be set.
13	Set Left Amp. '1' indicates left amplifier gain will be set.
12	Set Right Amp. '1' indicates right amplifier gain will be set.
11:8	Index Offset (for input amplifiers on Sum widgets and Selector Widgets). 5 bits index offset in connection list is used to select which input gain will be set on a Sum or a Selector widget. The index is ignored if the node is not a Sum or a Selector widget, or the 'Set Input Amp' bit is not set.
7	Mute. 0: Unmute 1: Mute (-∞gain)
6:0	Gain[6:0]. A 7-bit step value specifying the amplifier gain.

8.13. Verb – Get Converter Format (Verb ID=Ah)

Table 48. Verb – Get Converter Format (Verb ID=Ah)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
CAd=X	Node ID=Xh	Verb ID=Ah	0's

Codec Response Format

Response [31:0]
Bit[15:0] are converter format

Codec Response for NID=02h, 03h, 06h (Output Converters: LINE-OUT DAC, HP-OUT DAC, S/PDIF-OUT).
Codec Response for NID=07h~0Ah (Input Converters: MIC ADC, LINE ADC, MIX DAC, and S/PDIF-IN)

Bit	Description
31:16	Reserved. Read as 0.
15	Stream Type (TYPE). 0: PCM 1: Non-PCM
14	Sample Base Rate (BASE). 0: 48kHz 1: 44.1kHz
13:11	Sample Base Rate Multiple (MULT). 000b: *1 001b: *2 010b: *3 011b: *4 100b~111b: Reserved.
10:8	Sample Base Rate Divisor (DIV). 000b: /1 001b: /2 010b: /3 011b: /4 100b: /5 101b: /6 110b: /7 111b: /8 The ALC262 does not support Divisor. Always read as 000b.
7	Reserved. Read as 0.
6:4	Bits per Sample (BITS). 000b: 8 bits 001b: 16 bits 010b: 20 bits 011b: 24 bits 100b: 32 bits 101b~111b: Reserved
3:0	Number of Channels. 0: 1 channel 1: 2 channels 2: 3 channels …… 15: 16 channels

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.14. Verb – Set Converter Format (Verb ID=2h)

Table 49. Verb – Set Converter Format (Verb ID=2h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
CAd=X	Node ID=Xh	Verb ID=2h	Set format [15:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Set' Payload in Command Bit[15:0]

Bit	Description
31:16	Reserved. Read as 0.
15	Stream Type (TYPE). 0: PCM 1: Non-PCM
14	Sample Base Rate (BASE). 0: 48kHz 1: 44.1kHz
13:11	Sample Base Rate Multiple (MULT). 000b: *1 001b: *2 010b: *3 011b: *4 100b~111b: Reserved.
10:8	Sample Base Rate Divisor (DIV). 000b: /1 001b: /2 010b: /3 011b: /4 100b: /5 101b: /6 110b: /7 111b: /8
7	Reserved. Read as 0.
6:4	Bits per Sample (BITS). 000b: 8 bits 001b: 16 bits 010b: 20 bits 011b: 24 bits 100b: 32 bits 101b~111b: Reserved
3:0	Number of Channels. 0: 1 channel 1: 2 channels 2: 3 channels …… 15: 16 channels

8.15. Verb – Get Power State (Verb ID=F05h) (ALC262 A/B/C Version)

Table 50. Verb – Get Power State (Verb ID=F05h) (ALC262 A/B/C Version)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=Ah	0's

Codec Response Format

Response [31:0]
Power State [7:0]

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:6	Reserved. Read as 0's.
5:4	PS-Act. Actual Power State [1:0]. 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3 PS-Act indicates the actual power state of the referenced node. For Audio Function Group nodes (NID=01h), PS-Act is always equal to PS-Set.
3:2	Reserved. Read as 0's.
1:0	PS-Set. Set Power State [1:0]. 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3 PS-Set controls the current power setting of the referenced node.

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.16. Verb – Get Power State (Verb ID=F05h) (ALC262 D Version)

Table 51. Verb – Get Power State (Verb ID=F05h) (ALC262 D Version)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=Ah	0's

Codec Response Format

Response [31:0]
Power State [7:0]

Codec Response for NID=01h (Audio Function Group)
Codec Response for NID=02h, 03h, 07h, 08h, 09h (Analog Input/Output Converter)
Codec Response for NID=11h, 12h, 14h, 15h, 16h, 18h, 19h, 1Ah, 1Bh, 1Ch, 1Dh, 1Eh, 1Fh (Pin Widgets)
Codec Response for NID=06h, 0Ah, 10h (Digital Input/Output Converter)

Bit	Description
31:11	Reserved. Read as 0's.
10	PS-SettingsReset. 0: Setting of widgets has been reset during any low power state 1: Setting that were changed from the default have been reset to their default during any low power state
9	PS-ClkStopOk. 0: No capability to operate normally with BITCLK stop 1: Operate normally with no BICLK
8	PS-Error. No support in ALC262-VD.
7:4	PS-Act. Actual Power State [1:0]. 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3 PS-Act indicates the actual power state of the referenced node. For Audio Function Group nodes (NID=01h), PS-Act is always equal to PS-Set.
3:2	Reserved. Read as 0's.
1:0	PS-Set. Set Power State [1:0]. 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3 PS-Set controls the current power setting of the referenced node.

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.17. Verb – Set Power State (Verb ID=705h)

Table 52. Verb – Set Power State (Verb ID=705h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=705h	Power State [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Power State' in Command Bit[7:0]

Bit	Description
7:6	Reserved. Read as 0's.
5:4	PS-Act. Actual Power State [1:0]. 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3 PS-Act indicates the actual power state of the referenced node.
3:2	Reserved. Read as 0's.
1:0	PS-Set. Set Power State [1:0]. 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3

8.18. Verb – Get Converter Stream, Channel (Verb ID=F06h)

Table 51. Verb – Get Converter Stream, Channel (Verb ID=F06h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F06h	0's

Codec Response Format

Response [31:0]
Stream & Channel [7:0]

Codec Response for NID=02h, 03h, 06h (Output Converters: LINE-OUT DAC, HP-OUT DAC, S/PDIF-OUT).
Codec Response for NID=07h~0Ah (Input Converters: MIC ADC, LINE ADC, MIX DAC, and S/PDIF-IN)

Bit	Description
31:8	Reserved. Read as 0's.
7:4	Stream[3:0]. The link stream used by the converter. 0000b is stream 0, 0001b is stream 1, etc.
3:0	Channel[3:0]. The lowest channel used by the converter. A stereo converter will use the set channel n as well as n+1 for its left and right channel.

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.19. Verb – Set Converter Stream, Channel (Verb ID=706h)

Table 53. Verb – Set Converter Stream, Channel (Verb ID=706h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=706h	Stream & Channel [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Stream and Channel' in Command Bit[7:0]

Bit	Description
31:8	Reserved. Read as 0's.
7:4	Set Stream[3:0]. The link stream used by the converter. 0000b is stream 0, 0001b is stream 1, etc.
1:0	Set Channel[3:0]. The lowest channel used by the converter. A stereo converter will use the set channel n as well as n+1 for its left and right channel.

Note: This verb assigns stream and channel for output converters (NID=02h, 03h, 06h) and input converters (NID=07h~0Ah). Other widgets will ignore this verb.

8.20. Verb – Get Pin Widget Control (Verb ID=F07h)

Table 54. Verb – Get Pin Widget Control (Verb ID=F07h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F07h	0's

Codec Response Format

Response [31:0]
Pin Control [7:0]

Codec Response for NID=14h, 15h, 16h, 18h~1Bh (Pin Complex)

Bit	Description
31:1	Reserved. Read as 0's.
7	H-Phn Enable (Headphone Amplifier Enable, EN_AMP for an I/O unit). 0: Disabled 1: Enabled
6	Out Enable (Output Buffet Enable, EN_OBUF for an I/O unit). 0: Disabled 1: Enabled
5	In Enable (Input Buffer Enable, EN_IBUF for an I/O unit). 0: Disabled 1: Enabled
4:	Reserved.
2:0	VrefEn (Vrefout Enable Control). 000b: Hi-Z (Disabled) 001b: 50% of AVDD 010b: Ground 0V 011b: Reserved 100b: 80% of AVDD 101b: 100% of AVDD 110b~111b: Reserved

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.21. Verb – Set Pin Widget Control (Verb ID=707h)

Table 55. Verb – Set Pin Widget Control (Verb ID=707h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=707h	Pin Control [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Pin Control' in command [7:0]: (NID=14h, 15h, 16h, 18h~1Bh)

Bit	Description
31:1	Reserved. Read as 0's.
7	H-Phn Enable. 0: Disabled 1: Enabled
6	Out Enable. 0: Disabled 1: Enabled
5	In Enable (Input Buffer Enable, EN_IBUF for an I/O unit). 0: Disabled 1: Enabled
4:	Reserved.
2:0	VrefEn (Vrefout Enable Control). 000b: Hi-Z (Disabled) 001b: 50% of AVDD 010b: Ground 0V 011b: Reserved 100b: 80% of AVDD 101b: 100% of AVDD 110b~111b: Reserved

8.22. Verb – Get Unsolicited Response Control (Verb ID=F08h)

Determines whether a widget is enabled to send an unsolicited response. An HDA codec can use an unsolicited response to inform software of a real-time event.

Table 56. Verb – Get Unsolicited Response Control (Verb ID=F08h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F08h	0's

Codec Response Format

Response [31:0]
32-bit Response

Codec Response for NID=01h (GPIO), 0Ah (S/PDIF-IN), 14h~16h, 18h~1Bh (Port), 21h (Volume in Step)

Bit	Description
31:8	Reserved. Read as 0's.
7	Unsolicited Response is Enabled. 0: Disabled 1: Enabled
6:4	Reserved. Read as 0's.
3:0	Assigned Tag for Unsolicited Response. The tag[3:0] is assigned by software to determine which widget generates unsolicited responses.

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.23. Verb – Set Unsolicited Response Control (Verb ID=708h)

Enable a widget to generate an unsolicited response.

Table 57. Verb – Set Unsolicited Response Control (Verb ID=708h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=708h	EnableUnsol [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'EnableUnsol' in Command Bit[7:0]

Bit	Description
31:8	Reserved. Read as 0's.
7	Enable Unsolicited Response. 0: Disable 1: Enable
6:4	Reserved. Read as 0's.
3:0	Tag for Unsolicited Response. Tag[3:0] is defined by software to assign a 4-bit tag for nodes that are enabled to generate unsolicited responses.

8.24. Verb – Get Pin Sense (Verb ID=F09h)

Returns the Presence Detect status and the impedance of a device attached to the pin.

Table 58. Verb – Get Pin Sense (Verb ID=F09h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F09h	0's

Codec Response Format

Response [31:0]
32-bit Response

Codec Response for NID =14h~16h, 18h~1Bh, 1Eh, 1Fh

Bit	Description
31	Presence Detect Status. 0: No device is attached to the pin 1: Device is attached to the pin
30:0	Measured Impedance. 0x7FFFFFFF or 0xFFFFFFFF: Valid sense is not available or is busy.

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.25. Verb – Execute Pin Sense (Verb ID=709h)

Table 59. Verb – Execute Pin Sense (Verb ID=709h)

Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=709h	Right Channel[0]

Codec Response Format

Response [31:0]
0's for all nodes

'Payload' in Command Bit[7:0]

Bit	Description
7:1	Reserved. Read as 0's.
0	Right (Ring) Channel Select. 0: Sense Left channel (Tip) 1: Sense Right channel (Ring)

8.26. Verb – Get Configuration Default (Verb ID=F1Ch)

Read the 32-bit sticky register for each Pin Widget configured by software.

Table 60. Verb – Get Configuration Default (Verb ID=F1Ch)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F1Ch	0's

Codec Response Format

Response [31:0]
32-bit Response

Codec Response for NID=14h, 15h, 16h, 18h~1Fh

Bit	Description
31:0	32-bit configuration information for each pin widget.

Note: The 32-bit registers for each Pin Widget are sticky and will not be reset by a LINK Reset or Codec Reset (Function Reset Verb).

8.27. Verb – Set Configuration Default Bytes 0, 1, 2, 3 (Verb ID=71Ch/71Dh/71Eh/71Fh for Bytes 0, 1, 2, 3)

The BIOS can use this verb to figure out the default conditions for the Pin Widgets 14h~1Bh and 1Eh~1Fh such as placement and expected default device.

Table 61. Verb – Set Configuration Default Bytes 0, 1, 2, 3 (Verb ID=71Ch/71Dh/71Eh/71Fh for Bytes 0, 1, 2, 3)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=71Ch, 71Dh, 71Eh, 71Fh	Label [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

Note: Supported by Pin Widget NID=14h~16h, 18h~1Fh. Other widgets will ignore this verb.

Codec Response for All NID

Bit	Description
31:0	0's.

8.28. Verb – Get BEEP Generator (Verb ID=F0Ah)

Table 62. Verb – Get BEEP Generator (Verb ID=F0Ah)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F1Bh	0's

Codec Response Format

Response [31:0]
Divider [7:0]

'Response' for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:0	Frequency Divider, F[7:0]. The internal BEEP frequency is the result of dividing the 48kHz clock by 4 times the number specified in F[7:0]. The lowest tone is 48kHz/(255*4)=47Hz. The highest tone is 48kHz/(1*4)=12kHz. A value of 00h in F[7:0] disables internal BEEP generator and allows external PCBEEP input.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.29. Verb – Set BEEP Generator (Verb ID=70Ah)

Table 63. Verb – Set BEEP Generator (Verb ID=70Ah)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=71Bh	Divider [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Divider' in Set Command

Bit	Description
31:8	Reserved.
7:0	Frequency Divider, F[7:0]. The internal BEEP frequency is the result of dividing the 48kHz clock by 4 times the number specified in F[7:0]. The lowest tone is 48kHz/(255*4)=47Hz. The highest tone is 48kHz/(1*4)=12kHz. A value of 00h in F[7:0] disables the internal BEEP generator and allows external PCBEEP input.

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for All NID

Bit	Description
31:0	0's.

8.30. Verb – Get GPIO Data (Verb ID=F15h)

Table 64. Verb – Get GPIO Data (Verb ID=F15h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F15h	0's

Codec Response Format

Response [31:0]
32-bit Response

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:4	Reserved.
3:0	GPIO[3:0] Data. The value written (output) or sensed (input) on the corresponding pin if it is enabled.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.31. Verb – Set GPIO Data (Verb ID=715h)

Table 65. Verb – Set GPIO Data (Verb ID=715h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=715h	Data [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Data' in Set command for NID=01h (Audio Function Group)

Bit	Description
31:4	Reserved.
3:0	GPIO[3:0] Output Data. The value written determines the value driven on a pin that is configured as an output pin.

Codec Response for All NID

Bit	Description
31:0	0's.

8.32. Verb – Get GPIO Enable Mask (Verb ID=F16h)

Table 66. Verb – Get GPIO Enable Mask (Verb ID=F16h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F16h	0's

Codec Response Format

Response [31:0]
EnableMask [7:0]

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:4	Reserved.
3:0	GPIO[3:0] Enable Mask. 0: The corresponding GPIO pin is disabled and is in Hi-Z state 1: The corresponding GPIO pin is enabled. Its behavior is determined by the GPIO direction control

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.33. Verb – Set GPIO Enable Mask (Verb ID=716h)

Table 67. Verb – Set GPIO Enable Mask (Verb ID=716h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=716h	Enable Mask [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:4	Reserved.
3:0	GPIO[3:0] Enable Mask. 0: The corresponding GPIO pin is disabled and is in Hi-Z state 1: The corresponding GPIO pin is enabled. Its behavior is determined by the GPIO direction control

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for All NID

Bit	Description
31:0	0's.

8.34. Verb – Get GPIO Direction (Verb ID=F17h)

Table 68. Verb – Get GPIO Direction (Verb ID=F17h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F17h	0's

Codec Response Format

Response [31:0]
Direction [7:0]

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:4	Reserved.
3:0	GPIO[3:0] Direction Control. 0: The corresponding GPIO pin is configured as an input 1: The corresponding GPIO pin is configured as an output

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.35. Verb – Set GPIO Direction (Verb ID=717h)

Table 69. Verb – Set GPIO Direction (Verb ID=717h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=717h	Direction [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:4	Reserved.
3:0	GPIO[3:0] Direction Control. 0: The corresponding GPIO pin is configured as an input 1: The corresponding GPIO pin is configured as an output

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.36. Verb – Get GPIO Unsolicited Response Enable Mask (Verb ID=F19h)

Table 70. Verb – Get GPIO Unsolicited Response Enable Mask (Verb ID=F19h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F19h	0's

Codec Response Format

Response [31:0]
UnsolEnable [7:0]

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:4	Reserved.
3:0	GPIO[3:0] Unsolicited Enable Mask. 0: Unsolicited response will not be sent on link 1: Unsolicited response will be sent on link when state of corresponding GPIO has been changed

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.37. Verb – Set GPIO Unsolicited Response Enable Mask (Verb ID=719h)

Table 71. Verb – Set GPIO Unsolicited Response Enable Mask (Verb ID=719h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=719h	UnsolEnable [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:4	Reserved.
3:0	GPIO[3:0] Unsolicited Enable Mask. 0: Unsolicited response will not be sent on link 1: Unsolicited response will be sent on link when state of corresponding GPIO has been changed

Note 1: All nodes except the Audio Function Group (NID=01h) will ignore this verb.

Note 2: The unsolicited response of corresponding GPIO is enabled when it's 'Enable Mask' and Verb-'Unsolicited Response' for NID=01h are enabled.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.38. Verb – Function Reset (Verb ID=7FFh)

Table 72. Verb – Function Reset (Verb ID=7FFh)

Command Format (NID=01H)

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=01h	Verb ID=7FFh	0's

Codec Response Format

Response [31:0]
0's

Codec Response

Bit	Description
31:0	Reserved. Read as 0's.

Note: The Function Reset command causes all widgets in the ALC262 to return to their power on default state.

8.39. Verb – Get Digital Converter Control 1 & Control 2 (Verb ID=F0Dh, F0Eh)

Table 73. Verb – Get Digital Converter Control 1 & Control 2 (Verb ID=F0Dh, F0Eh)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F0Dh/F0Eh	0's

Codec Response Format

Response [31:0]
Bit[31:16]=0's, Bit[15:0] are SIC bit

NID=06h (S/PDIF-OUT) Response to 'Get verb' – F0Dh (Control 1 for SIC bit[15:0]).
NID=06h (S/PDIF-OUT) Response to 'Get verb' – F0Eh (Control 2 for SIC bit[15:0])

Bit	Description – SIC (S/PDIF IEC Control) Bit[7:0]
31:16	Read as 0's.
15	Reserved. Read as 0's.
14:8	CC[6:0] (Category Code).
7	LEVEL (Generation Level).
6	PRO (Professional or Consumer Format). 0: Consumer format 1: Professional format
5	/AUDIO (Non-Audio Data Type). 0: PCM data 1: AC3 or other digital non-audio data
4	COPY (Copyright). 0: Asserted 1: Not asserted
3	PRE (Pre-Emphasis). 0: None 1: Filter pre-emphasis is 50/15 microseconds
2	VCFG for Validity Control (control V bit and data in Sub-Frame).
1	V for Validity Control (control V bit and data in Sub-Frame).
0	Digital Enable. DigEn. 0: OFF 1: ON

NID=0Ah (S/PDIF-IN) Response to 'Get verb (F0Dh)'. NID=0Ah (S/PDIF-IN) Response to 'Get verb (F0Eh)'

Bit	Description (a part of S/PDIF-IN Channel Status)
31:16	Reserved. Read as 0's.
15	Reserved. Read as 0's.
14:8	CC[6:0] (Category Code).
7	LEVEL (Generation Level).
6	PRO (Professional or Consumer Format). 0: Consumer format 1: Professional format
5	/AUDIO (Non-Audio Data Type). 0: PCM data 1: AC3 or other digital non-audio data
4	COPY (Copyright). 0: Asserted 1: Not asserted
3	PRE (Pre-Emphasis). 0: None 1: Filter pre-emphasis is 50/15 microseconds
2	Reserved.
1	In'V'alid. V Bit in Sub-Frame of S/PDIF-IN. 0: Data X and Y are valid, or S/PDIF-IN is not locked 1: At least one of data X and Y is invalid
0	Digital Enable. DigEn. 0: OFF; 1: ON

Codec Response for Other NID

Bit	Description
31:0	0's.

8.40. Verb – Set Digital Converter Control 1 & Control 2 (Verb ID=70Dh, 70Eh)

Table 74. Verb – Set Digital Converter Control 1 & Control 2 (Verb ID=70Dh, 70Eh)

Set Command Format (Verb ID=70Xh, Set Control 1)

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=70Dh	SIC [7:0]

Codec Response Format

Response [31:0]
0's

Set Command Format (Verb ID=70Yh, Set Control 2)

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=70Eh	SIC [15:8]

Codec Response Format

Response [31:0]
0's

'Payload' in Set Control 1 for NID=06h (S/PDIF-OUT)

Bit	Description – SIC (S/PDIF IEC Control) Bit[7:0]
7	LEVEL (Generation Level).
6	PRO (Professional or Consumer Format). 0: Consumer format 1: Professional format
5	/AUDIO (Non-Audio Data Type). 0: PCM data 1: AC3 or other digital non-audio data
4	COPY (Copyright). 0: Asserted 1: Not asserted
3	PRE (Pre-Emphasis). 0: None 1: Filter pre-emphasis is 50/15 microseconds
2	VCFG for Validity Control (control V bit and data in Sub-Frame).
1	V for Validity Control (control V bit and data in Sub-Frame).
0	Digital Enable. DigEn. 0: OFF 1: ON

'Payload' in Set Control 2 for NID=06h (S/PDIF-OUT)

Bit	Description – SIC (S/PDIF IEC Control) Bit[7:0]
7	Reserved. Read as 0's.
6:0	CC[6:0] (Category Code).

'Payload' in Set Control 1 for NID=0Ah (S/PDIF-IN)

Bit	Description – SIC (S/PDIF IEC Control) Bit[7:0]
7:1	Reserved.
0	Digital Enable. DigEn. 0: OFF 1: ON

'Payload' in Set Control 2 for NID=0Ah (S/PDIF-IN)

Bit	Description – SIC (S/PDIF IEC Control) Bit[7:0]
7:0	Reserved. Read as 0's.

Note: Other widgets will ignore this verb.

8.41. Get/Set Volume Knob Widget (NID=21h) (Verb ID=F0Fh/70Fh)

Table 75. Get/Set Volume Knob Widget (NID=21h) (Verb ID=F0Fh/70Fh)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F0Fh	0's

Codec Response Format

Response [31:0]
Bit[31:8]=0's, Bit[7:0] is volume

Codec Response for NID=21h (Volume Knob Widget)

Bit	Description
31:8	Reserved.
7	Direct. 0: The volume generated by an external HW volume control will be sent by unsolicited response. Software is responsible for programming the amplifier appropriately 1: The volume generated by an external HW volume control will directly affect amplifier volume
6:0	Volume in steps.

Set Command Format (Verb ID=70Yh, Set Control 2)

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=70Fh	Bit[7] is 'Direct' control

Codec Response Format

Response [31:0]
0's

'Payload' in Set Command for NID=21h (Volume Knob Widget)

Bit	Description
31:8	Reserved.
7	Direct. 0: The volume generated by an external HW volume control will be sent by unsolicited response. Software is responsible for programming the amplifier appropriately 1: The volume generated by an external HW volume control will directly affect amplifier volume
6:0	Reserved.

Note: Other nodes will ignore this verb.

8.42. Get/Set Subsystem ID [31:0] (Verb ID=F20h/723h~720h to Set Bit[31:0])

Table 76. Get/Set Subsystem ID [31:0] (Verb ID=F20h / 723h~720h to Set Bit[31:0])

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F20h	0's

Codec Response Format

Response [31:0]
32 bits response

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:16	Subsystem ID[23:8]. (Default=10ECh).
15:8	Subsystem ID[7:0]. (Default=02h).
7:0	Assembly ID[7:0]. (Default=62h).

9. Electrical Characteristics

9.1. DC Characteristics

9.1.1. Absolute Maximum Ratings

Table 77. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power Supplies					
Digital Power for Core	DVDD-CORE	3.0	3.3	3.6	V
Digital Power for Link (C, D)*	DVDD-IO	1.3	3.3	3.6	V
Analog Power	AVDD**	3.0	3.3	5.5	V
Ambient Operating Temperature	Ta	0	-	+70	°C
Storage Temperature	Ts	-	-	+125	°C
ESD (Electrostatic Discharge)					
	Susceptibility Voltage				
Pin 33 (DCVOL) (ver. A/B/C)	3000V				
All Pins (ver. D)	4000V				

**: The digital link power DVDD-IO must be lower than the digital core power DVDD.*
***: The standard testing condition before shipping is AVDD = 5.0V unless specified. Customers designing with a different AVDD should contact Realtek technical support representatives for special testing support.*

9.1.2. Threshold Voltage

DVDD-IO=3.3V±5%, $T_{ambient}$=25°C, with 50pF external load.

Table 78. Threshold Voltage

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Voltage Range	V_{in}	-0.30	-	DVDD +0.30	V
Low Level Input Voltage (BCLK, RST#, SDO, SYNC, SDI)	V_{IL}	-	-	0.30*DVDD-IO	V
High Level Input Voltage (BCLK, RST#, SDO, SYNC, SDI)	V_{IH}	0.65*DVDD-IO	-	-	V
Low Level Input Voltage (S/PDIF-IN/OUT, GPIOs)	V_{IL}	-	-	0.44*DVDD (1.45)	V
High Level Input Voltage (S/PDIF-IN/OUT, GPIOs)	V_{IH}	0.56*DVDD (1.85)	-	-	V
High Level Output Voltage (BCLK, RST#, SDO, SYNC, SDI)	V_{OH}	0.9*DVDD-IO	-	-	V
Low Level Output Voltage (BCLK, RST#, SDO, SYNC, SDI)	V_{OL}	-	-	0.1*DVDD-IO	V
Input Leakage Current	-	-10	-	10	µA
Output Leakage Current (Hi-Z)	-	-10	-	10	µA
Output Buffer Drive Current	-	-	5	-	mA
Internal Pull Up Resistance	-	-	50k	-	Ω

9.1.3. Digital Filter Characteristics

Table 79. Digital Filter Characteristics

Filter	Symbol	Minimum	Typical	Maximum	Units
ADC Lowpass Filter	Passband (A/B silicon) Passband (C/D silicon)	0	-	19.2 (-3dB) 0.458*Fs (-1dB)	kHz kHz
	Stopband	0.6*Fs	-	-	kHz
	Stopband Rejection	-	-76.0	-	dB
	Passband Ripple (A/B) Passband Ripple (C/D)	- -	±0.20 ±0.05	- -	dB dB
DAC Lowpass Filter	Passband (A/B silicon) Passband (C/D silicon)	0 0	- -	19.2 (-3dB) 0.435*Fs (-1dB)	kHz kHz
	Stopband	0.6*Fs	-	-	kHz
	Stopband Rejection	-	-78.5	-	dB
	Passband Ripple (A/B) Passband Ripple (C/D)	- -	±0.20 ±0.03	- -	dB dB

9.1.4. S/PDIF Input/Output Characteristics

DVDD=3.3V, $T_{ambient}$=25°C, with 75Ω external load.

Table 80. S/PDIF Input/Output Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
S/PDIF-OUT High Level Output	V_{OH}	3.0	3.3	-	V
S/PDIF-OUT Low Level Output	V_{OL}	-	0	0.3	V
S/PDIF-IN High Level Input	V_{IH}	1.85	-	-	V
S/PDIF-IN Low Level Input	V_{IL}	-	-	1.45	V
S/PDIF-IN Bias Level	Vt	-	1.65	-	V

9.2. AC Characteristics

9.2.1. Link Reset and Initialization Timing

Table 81. Link Reset and Initialization Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
RESET# Active Low Pulse Width	T_{RST}	1.0	-	-	µs
RESET# Inactive to BCLK Startup Delay for PLL Ready Time	T_{PLL}	20	-	-	µs
SDI Initialization Request	T_{FRAME}	-	-	1	Frame Time

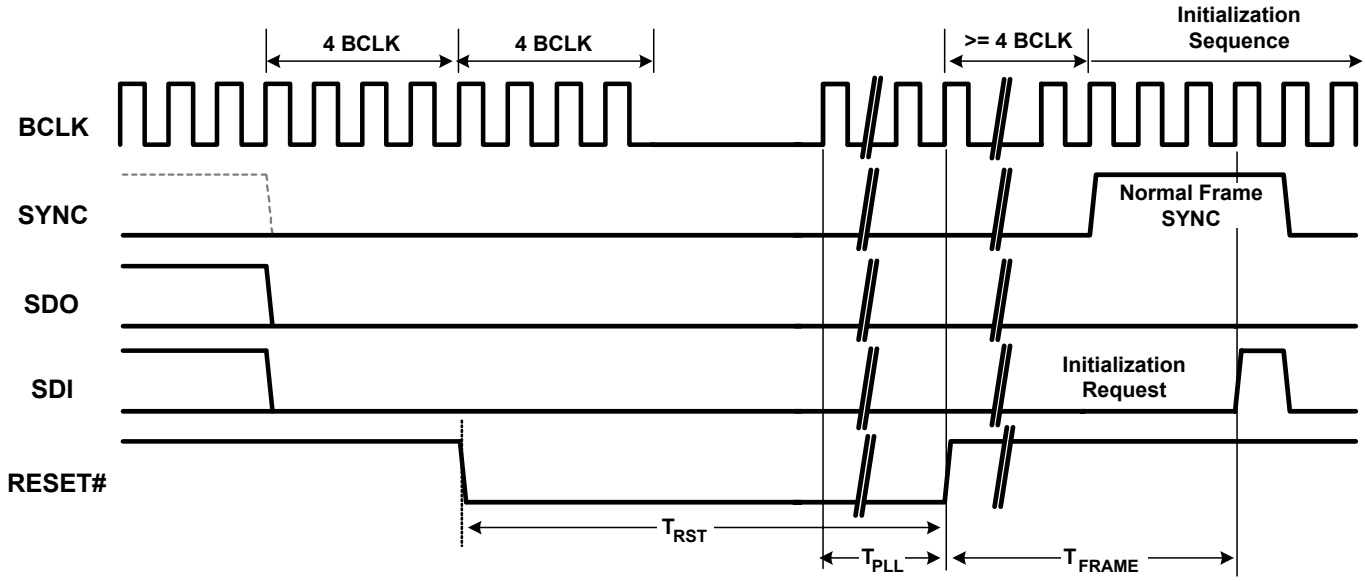


Figure 20. Link Reset and Initialization Timing

9.2.2. Link Timing Parameters at the Codec

Table 82. Link Timing Parameters at the Codec

Parameter	Symbol	Minimum	Typical	Maximum	Units
BCLK Frequency	-	-	24.0	-	MHz
BCLK Period	$T_{\_cycle}$	-	41.67	-	ns
BCLK Jitter	$T_{\_jitter}$	-	-	2.0	ns
BCLK High Pulse Width	$T_{\_high}$	17.5	-	24.16	ns
BCLK Low Pulse Width	$T_{\_low}$	17.5	-	24.16	ns
SDO Setup Time at Both Rising and Falling Edge of BCLK	$T_{\_setup}$	2.1	-	-	ns
SDO Hold Time at Both Rising and Falling Edge of BCLK	$T_{\_hold}$	2.1	-	-	ns
SDI Valid Time After Rising Edge of BCLK (1:50pF external load) (DVDD-IO=3.3V)	$T_{\_tco}$	-	7.5	-	ns
SDI Valid Time After Rising Edge of BCLK (1:50pF external load) (DVDD-IO=1.5V)	$T_{\_tco}$	-	10.0	-	ns
SDI Flight Time	$T_{\_flight}$	-	2.0	-	ns

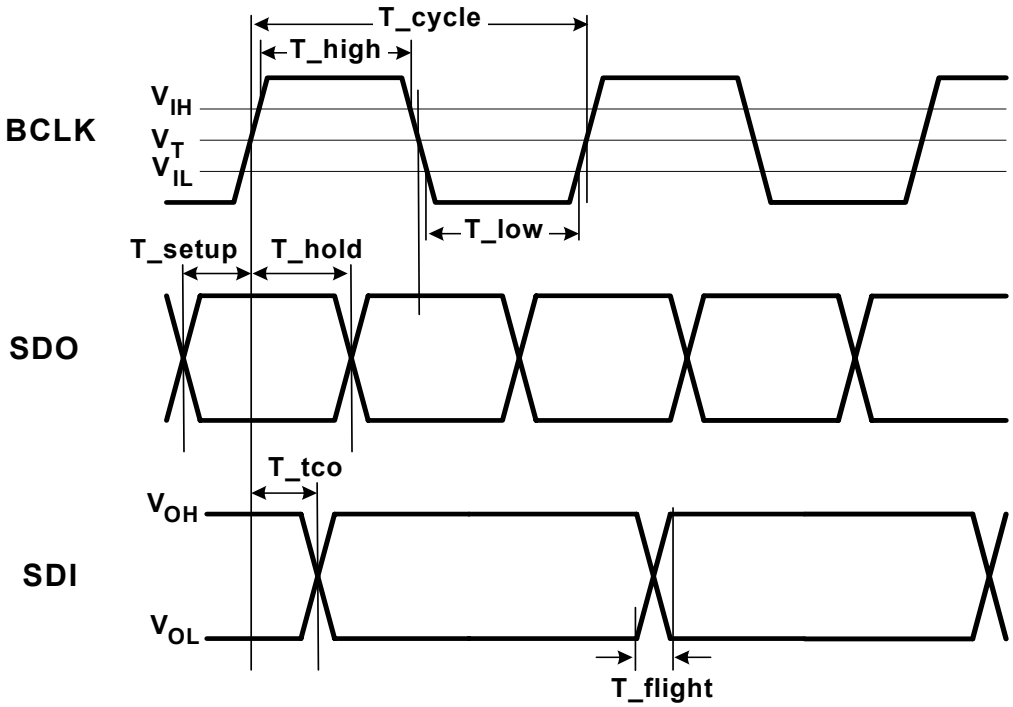


Figure 21. Link Signals Timing

9.2.3. S/PDIF Output and Input Timing

Table 83. S/PDIF Output and Input Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
S/PDIF-OUT Frequency*1	-	-	6.144	-	MHz
S/PDIF-OUT Period*1	T_{cycle}	-	162.8	-	ns
S/PDIF-OUT Jitter	T_{jitter}	-	-	4	ns
S/PDIF-OUT High Level Width*1	T_{High}	78.1 (48%)	81.4 (50%)	84.6 (52%)	ns (%)
S/PDIF-OUT Low Level Width*1	T_{Low}	78.1 (48%)	81.4 (50%)	84.6 (52%)	ns (%)
S/PDIF-OUT Rising Time	T_{rise}	-	2.0	-	ns
S/PDIF-OUT Falling Time	T_{fall}	-	2.0	-	ns
S/PDIF-IN Period*2	T_{cycle}	-	162.8	-	ns
S/PDIF-IN Jitter	T_{jitter}	-	-	10	ns
S/PDIF-IN High Level Width*2	T_{High}	73.2 (45%)	81.4 (50%)	89.5 (55%)	ns (%)
S/PDIF-IN Low Level Width*2	T_{Low}	73.2 (45%)	81.4 (50%)	89.5 (55%)	ns (%)

**1: Bit parameters for 48kHz sample rate of S/PDIF-OUT*

**2: Bit parameters for 48kHz sample rate of S/PDIF-IN*

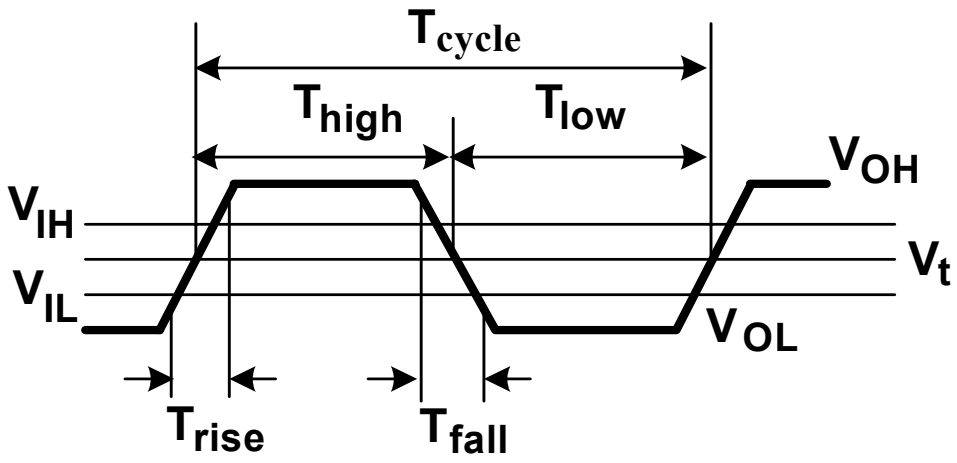


Figure 22. Output and Input Timing

9.2.4. Test Mode

The ALC262 series does not support codec test mode or Automatic Test Equipment (ATE) mode.

9.3. Analog Performance

Standard Test Conditions

- Tambient=25 oC, DVDD-CORE=3.3V ±5%, AVDD=5.0V±5%
- 1kHz input sine wave; Sampling frequency=48kHz; 0dB=1Vrms
- 10KΩ/50pF load; Test bench Characterization BW:10Hz~22kHz, 0dB attenuation

Table 84. Analog Performance

Parameter	Min	Typ	Max	Units
Full Scale Input Voltage				
All Inputs (Gain=0dB)	-	1.5	-	Vrms
All ADC	-	1.1	-	Vrms
Full Scale Output Voltage				
All DAC (Ver. A/B/C)	-	1.4	-	Vrms
All DAC (Ver. D)	-	1.2	-	Vrms
S/N (A Weighted)				
ADC	-	90	-	dB FSA
DAC	-	100	-	dB FSA
THD+N				
ADC	-	-82	-	dB FS
DAC	-	-87	-	dB FS
Headphone Out @32Ω Load (Version B0)	-	-75	-	dB FS
Frequency Response				
Mixers	10	-	22,000	Hz
ADC, DAC (Ver. B Silicon, -3dB Band Edge)	16	-	19,200	Hz
ADC, DAC (Ver. C/D Silicon, -1dB Band Edge)*	10	-	0.454*Fs	Hz
Power Supply Rejection	-	-40	-	dB
Total Out-of-Band Noise (28.8kHz~100kHz)	-	-60	-	dB
Amplifier Gain Step	-	1.5	-	dB
Crosstalk Between Input Channels	-	-80	-	dB
Input Impedance (Gain=0dB)	-	64	-	KΩ
Output Impedance				
Amplified Output	-	1	-	Ω
Non-Amplified Output	-	200	-	Ω
Digital Power Supply Current (Normal Operation) DVDD-CORE=3.3V, DVDD-IO=3.3V	-	40	-	mA
Digital Power Supply Current (Power Down Mode) DVDD-CORE=3.3V, DVDD-IO=3.3V	-	-	600	µA
Analog Power Supply Current (Normal Operation) AVDD=5.0V	-	52	-	mA
Analog Power Supply Current (Power Down Mode) AVDD=5.0V	-	-	600	µA
VREFOUTx Output Voltage	2.25	2.50	3.75	V
VREFOUTx Output Current	-	5	-	mA

**Fs = Sample rate.*

10. Application Notes

10.1. Application Circuit

Please contact Realtek for the latest application circuits. To get the best compatibility in hardware design and software driver, any modification should be confirmed by Realtek. Realtek may upload the latest application circuits onto our web site (www.realtek.com.tw) without modifying this datasheet.

10.2. Volume Control Via External Variable Resistor

The input range of DCVOL is from GND to AVDD. A 5-bit resolution ADC converts the DC level on the variable resistor into 32 steps for the Volume knob. DC level changes will be reflected to software to control the master volume.

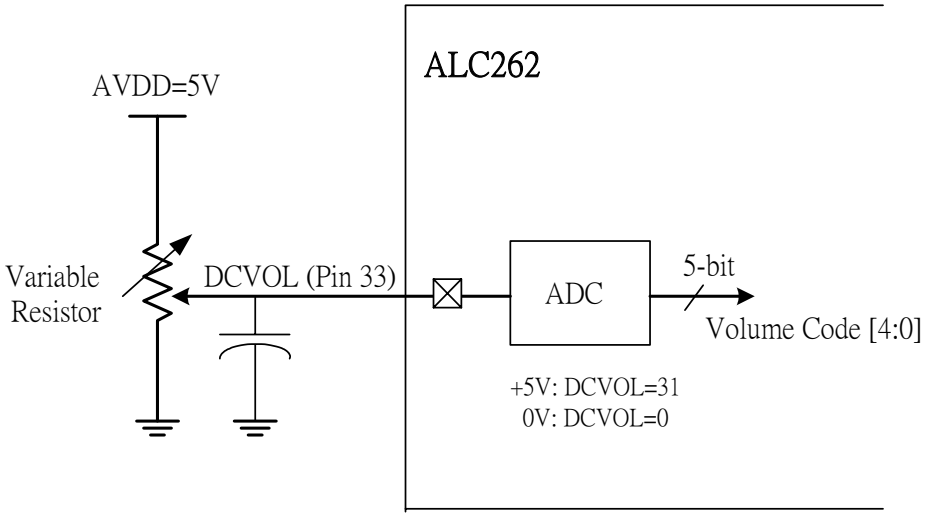


Figure 23. Volume Control by External Variable Resistor

10.3. Volume Control Via GPIO0/GPIO1

Detected low pulses generated at GPIO0 and GPIO1 are used to calculate the Up and Down count into 7 bits of volume steps. 'Mute' is also sampled to toggle the mute status. Hardware will not adjust volume. The count value will be reported via unsolicited response to software to control the master volume.

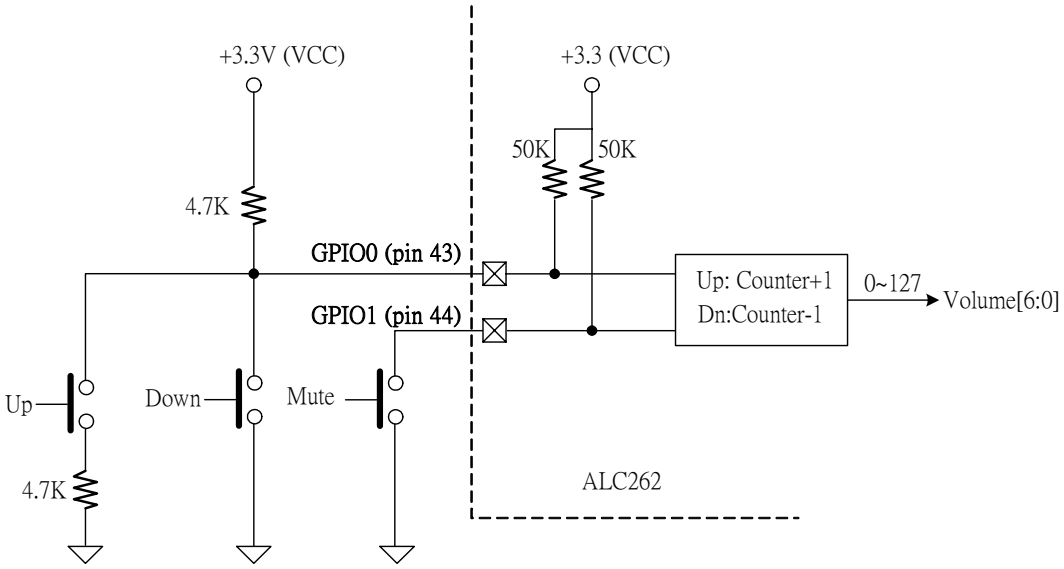


Figure 24. Volume Control via GPIO0 and GPIO1

10.4. Digital Microphone Implementation

This section describes the ALC262 digital microphone implementation. There is one Clock output pin and 1 Data input pin in the ALC262. The ALC262 provides the clock signal to the digital microphone. When the digital microphone receives the external sound input, it converts the analog signals to digital in a 1-bit format. The 1-bit data is delivered to the codec though the data input pin. The Digital Filter in the audio codec converts the 1-bit data stream into Pulse Code Modulation (PCM) data. The PCM data is sent to the HDA controller through the HDA link.

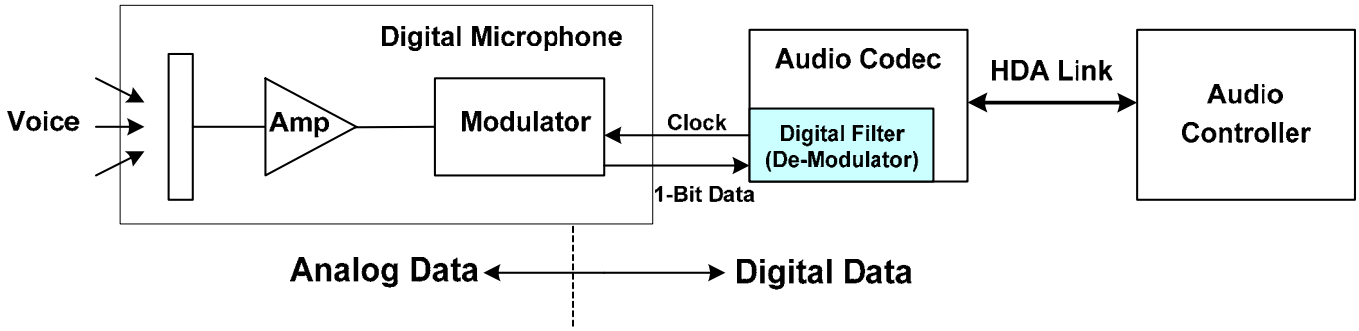


Figure 25. Digital Microphone Implementation-1

The ALC262 supports a two-wire interface for the digital microphone and operates in single channel (mono type) or stereo channels (stereo) digital microphone mode. One pin is clock output to the digital microphone, and the other is a serial pin. The default clock output is 2.048MHz.

In Type 1 (Figure 26), the ALC262 uses one data pin to support mono input from digital microphones with an LMV1024 (L), SPD0205ND (L), or AKU2000 (L).

In Type 2 (Figure 26), the ALC262 uses one data pin to support stereo inputs from digital microphones with an LMV1024/1026 (L/R), SPD0205ND (L & R), or AKU2000 (L & R).

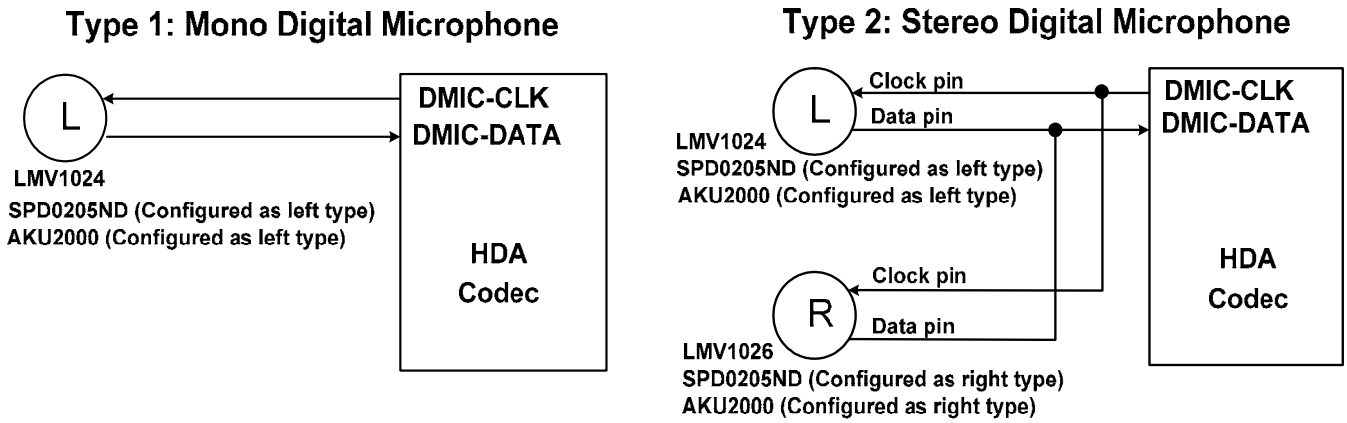


Figure 26. Digital Microphone Implementation-2

By default the left channel digital microphone data is sampled at the rising edge of clock, and the right channel data at the falling edge of clock. Figure 27 indicates 20nsec setup time and 5ns hold time are required to allow the ALC262 to get individual data correctly.

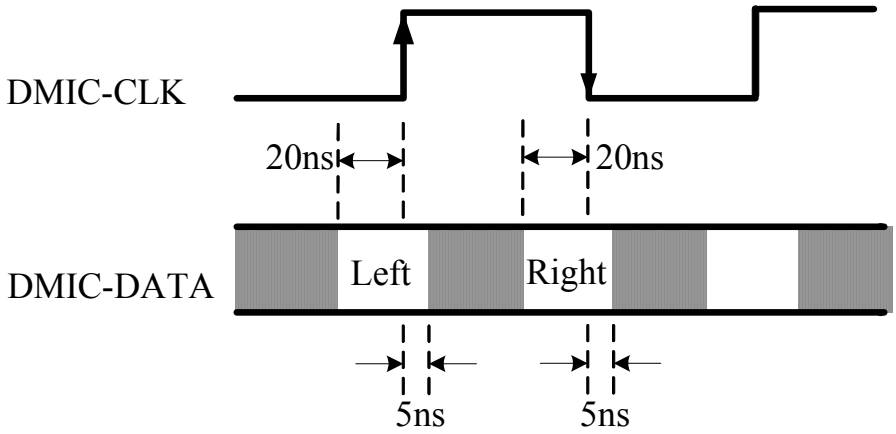
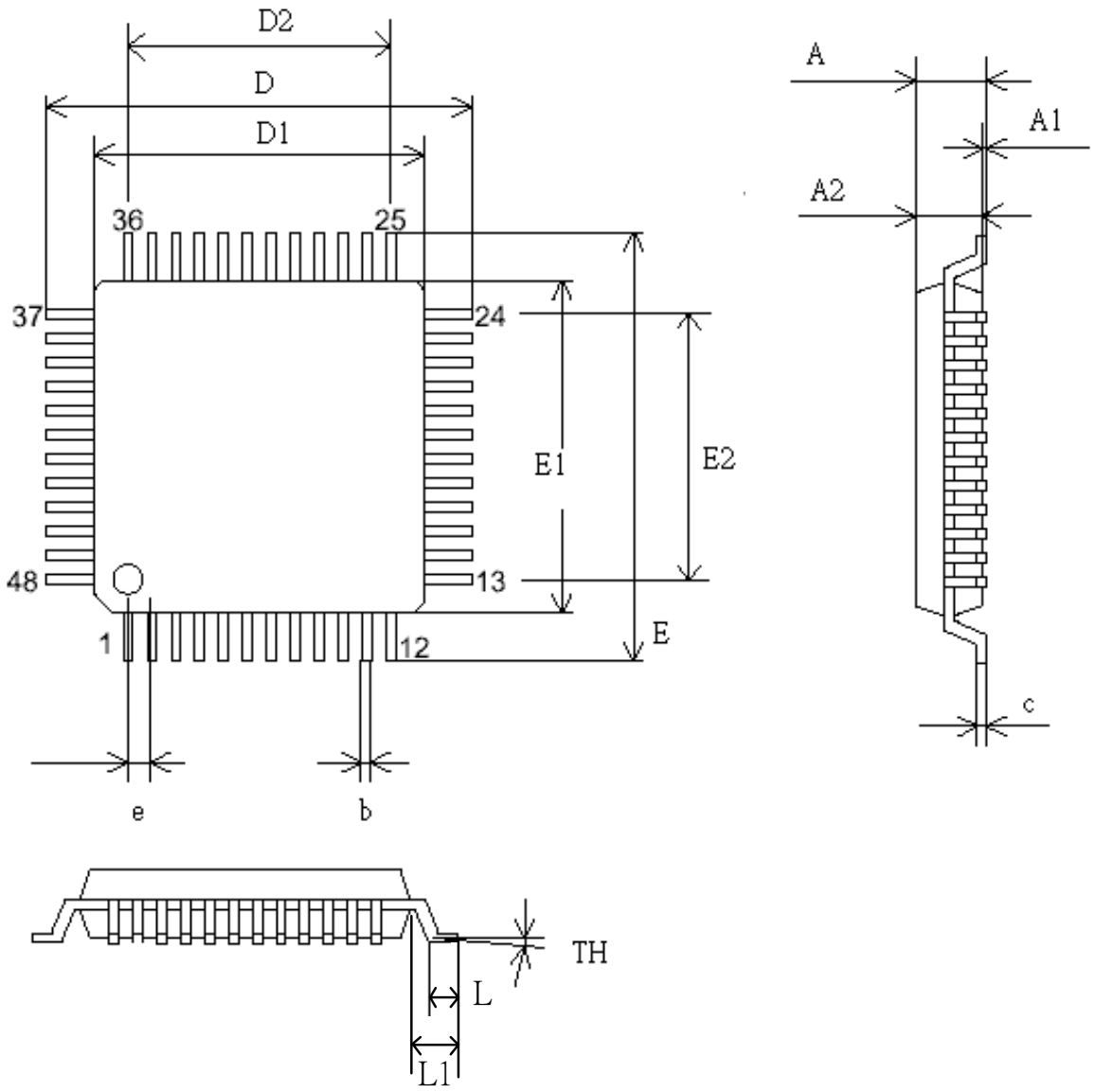


Figure 27. Digital Microphone Timing

11. Mechanical Dimensions



See the Mechanical Dimensions notes on the next page.

11.1. Mechanical Dimensions Notes

SYMBOL	MILLIMETER			INCH		
	MIN	TYP	MAX	MIN	TYP	MAX
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
c	0.09	-	0.20	0.004	-	0.008
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
D2	5.50			0.217		
E	9.00 BSC			0.354 BSC		
E1	7.00 BSC			0.276 BSC		
E2	5.50			0.217		
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC			0.0196 BSC		
TH	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.0236	0.030
L1	-	1.00	-	-	0.0393	-

TITLE: LQFP-48 (7.0x7.0x1.6mm) PACKAGE OUTLINE DRAWING, FOOTPRINT 2.0mm LEADFRAME MATERIAL			
APPROVE		DOC. NO.	
		VERSION	02
CHECK		DWG NO.	PKGC-065
		DATE	
REALTEK SEMICONDUCTOR CORP.			

12. Ordering Information

Table 85. Ordering Information

Part Number	Package	Status
ALC262-GR	Version A2 silicon, LQFP-48 &'Green' package	Production
ALC262-VB0-GR	Version B0 silicon, LQFP-48 &'Green' package	Production
ALC262SRS-GR	ALC262-VB0-GR + SRS TruSurround XT (software feature)	Production
ALC262H-GR	ALC262-VB0-GR + Dolby® Home Theater (software feature)	Production
ALC262-VC1-GR	Version C1 silicon, LQFP-48 &'Green' package	Production
ALC262-VC2-GR	Version C2 silicon, LQFP-48 &'Green' package	Production
ALC262-VD2-GR	Version D2 silicon, LQFP-48 &'Green' package	Production
ALC262W-VD2-GR	ALC262-VD2-GR + Waves MaxxAudio (software feature)	Production

Note 1: See section 5 Pin Assignments, page 10 for Green package and version identification.

Note 2: Above parts are tested under AVDD =5.0V. If customers have lower AVDD request, please contact Realtek sales representatives or agents.

Realtek Semiconductor Corp.
Headquarters
No. 2, Innovation Road II
Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com.tw