Nm9755

PCI Single Printer Port with ISA Bridge

Features

- Single 5V Operation
- Low Power
- PCI Compatible Printer Port
    - Multi-Mode Compatible Controller (SPP, PS2, EPP, ECP)
    - Fast Data Rates up to 1.5 MBps (Parallel Port)
    - 16-Byte FIFO (Parallel Port)
    - Re-Map function for Legacy Ports
    - Microsoft Compatible
    - Software Programmable Mode Selects
- ISA style I/O Interface
    - 3 address lines
    - 4 active high interrupts
    - 1 active low interrupt
    - 4 external chip selects
- 128-pin QFP Package

Applications

- Printer Server
- Portable Backup Units
- Printer Interface
- Add-On I/O Cards
- I/O Bridge
- Embedded Applications
- Monitoring Equipment

Application Note

- AN-9755

Evaluation Board

- Nm9755-EVB

General Description

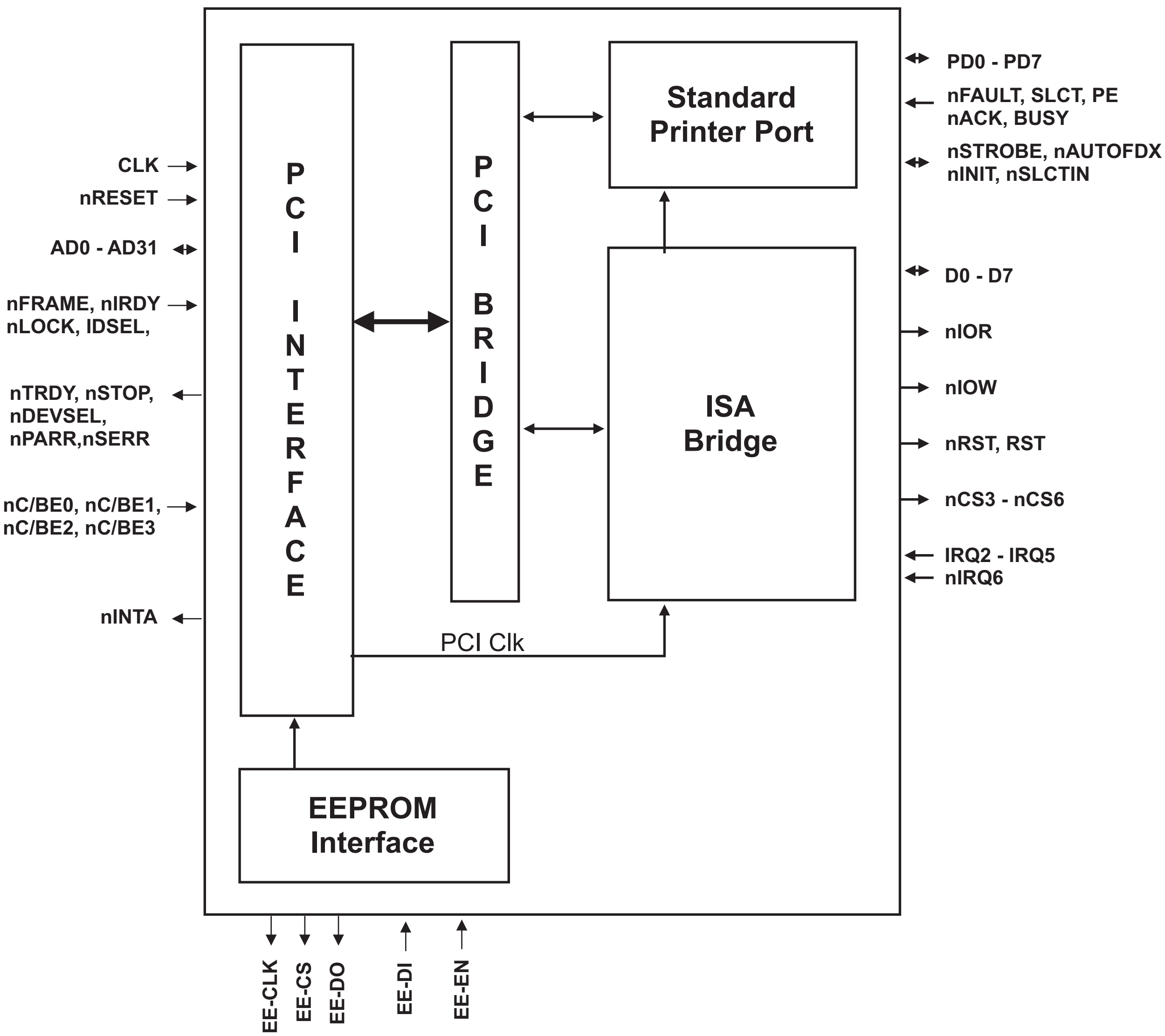
The Nm9755 is a PCI based printer port controller that also includes an ISA style Bus Interface. Nm9755 fully supports the existing Centronics printer interface as well as PS/2, EPP, and ECP modes.

The Nm9755 is ideally suited for PC applications, such as high speed parallel / serial ports. The Nm9755 is available in a 128-pin QFP package. It is fabricated using an advanced submicron CMOS process to achieve low drain power and high-speed requirements.

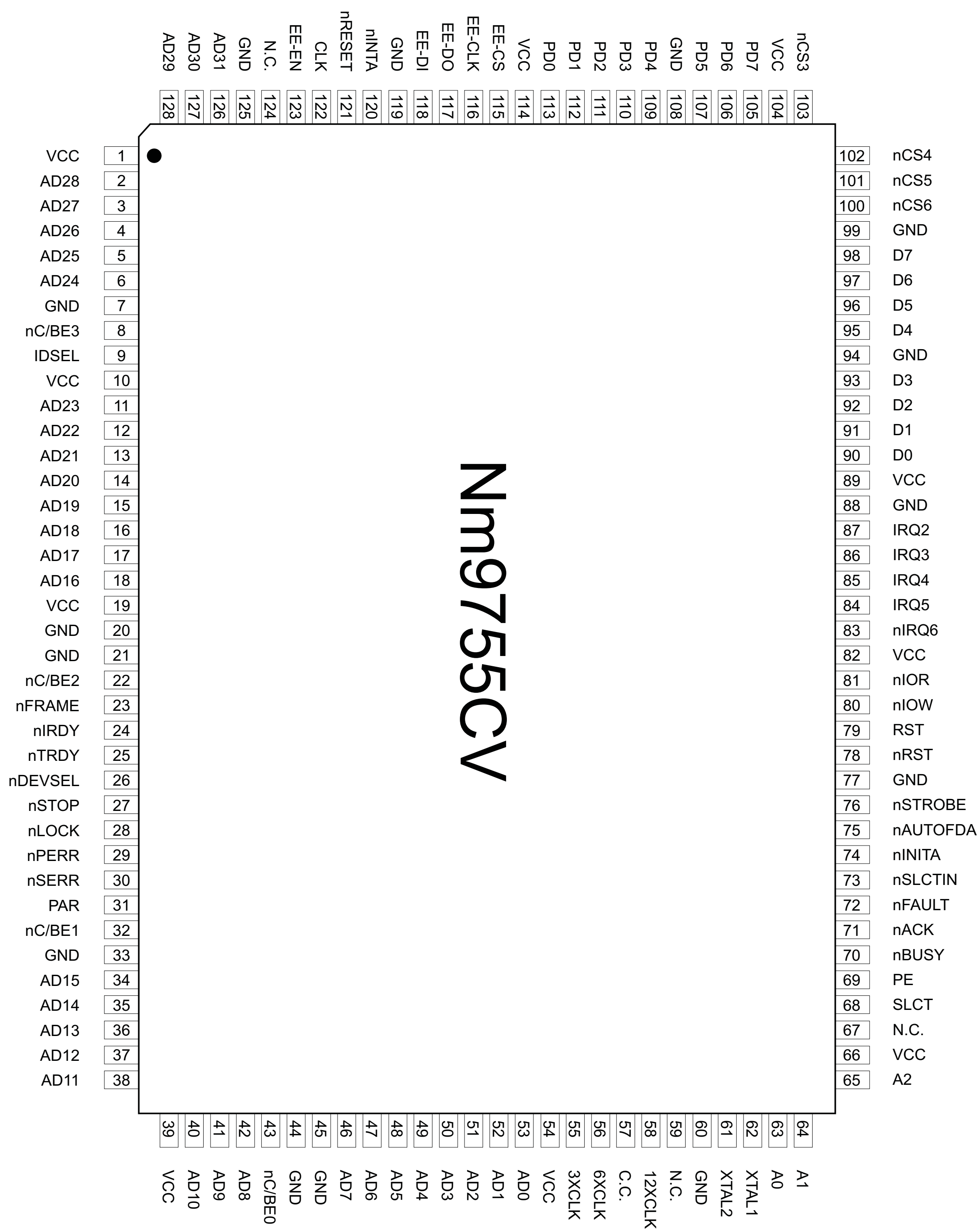
The Nm9755 supports 5V PCI signaling only. It is intended only for use in 5V PCI designs. This device requires a 5V power supply, and is not usable in 3.3V only designs.

Ordering Information		
Commercial Grade (0 °C to +70 °C)		
Nm9755CV	128-QFP	Non-RoHS

Block Diagram



Pin-Out


Nm9755CV
1 VCC
2 AD28
3 AD27
4 AD26
5 AD25
6 AD24
7 GND
8 nC/BE3
9 IDSEL
10 VCC
11 AD23
12 AD22
13 AD21
14 AD20
15 AD19
16 AD18
17 AD17
18 AD16
19 VCC
20 GND
21 GND
22 nC/BE2
23 nFRAME
24 nIRDY
25 nTRDY
26 nDEVSEL
27 nSTOP
28 nLOCK
29 nPERR
30 nSERR
31 PAR
32 nC/BE1
33 GND
34 AD15
35 AD14
36 AD13
37 AD12
38 AD11
39 VCC
40 AD10
41 AD9
42 AD8
43 nC/BE0
44 GND
45 GND
46 AD7
47 AD6
48 AD5
49 AD4
50 AD3
51 AD2
52 AD1
53 AD0
54 VCC
55 3XCLK
56 6XCLK
57 C.C.
58 12XCLK
59 N.C.
60 GND
61 XTAL2
62 XTAL1
63 A0
64 A1
65 A2
66 VCC
67 N.C.
68 SLCT
69 PE
70 nBUSY
71 nACK
72 nFAULT
73 nSLCTIN
74 nINITA
75 nAUTOFDA
76 nSTROBE
77 GND
78 nRST
79 RST
80 nIOW
81 nIOR
82 VCC
83 nIRQ6
84 IRQ5
85 IRQ4
86 IRQ3
87 IRQ2
88 GND
89 VCC
90 D0
91 D1
92 D2
93 D3
94 GND
95 D4
96 D5
97 D6
98 D7
99 GND
100 nCS6
101 nCS5
102 nCS4
103 nCS3
104 VCC
105 PD7
106 PD6
107 PD5
108 GND
109 PD4
110 PD3
111 PD2
112 PD1
113 PD0
114 VCC
115 EE-CS
116 EE-CLK
117 EE-DO
118 EE-DI
119 GND
120 nINTA
121 nRESET
122 CLK
123 EE-EN
124 N.C.
125 GND
126 AD31
127 AD30
128 AD29

Pin Assignments

Name	Pin	Type	Description
CLK	122	I	33 MHz PCI System Clock Input.
nRESET	121	I	PCI System Reset (active low). Resets all internal registers, sequencers, and signals to a consistent state. During the reset condition AD31-0 & nSER are tri-stated.
AD31-29	126-128	I/O	Multiplexed PCI address/data bus. A bus transaction consists of an address phase followed by one or more data phases. During the address phase, AD31-0 contain a physical address. Write data is stable and valid when nIRDY and nTRDY are asserted (active).
AD28-24	2-6	I/O	See AD31-29 description.
AD23-16	11-18	I/O	See AD31-29 description.
AD15-11	34-38	I/O	See AD31-29 description.
AD10-8	40-42	I/O	See AD31-29 description.
AD7-0	46-53	I/O	See AD31-29 description.
nFRAME	23	I	nFRAME is driven by the current Bus Master to indicate the beginning and duration of an access. nFRAME is asserted to indicate a Bus transaction is beginning. While nFRAME is active, data transfer continues.
nIRDY	24	I	Initiator Ready. During a write, nIRDY asserted indicates that the initiator is driving valid data onto the data bus. During a read, nIRDY asserted indicates that the initiator is ready to accept data from the target.
nTRDY	25	O	Target Ready (tri-state). This line is asserted when the target is ready to complete the current data phase.
nSTOP	27	O	nSTOP is asserted to indicate that the target wishes the initiator to stop the transaction in-process on the current data phase.
nLOCK	28	I	nLOCK indicates an atomic operation that may require multiple transactions to complete.
IDSEL	9	I	Initialization Device Select. It is used as a chip select during configuration read and write transactions.
nDEVSEL	26	O	Device Select (tri-state). A target asserts nDEVSEL when it has decoded one of its addresses.
nPERR	29	O	Parity Error (tri-state). Is used to report parity errors during all PCI transactions except a special cycle. The minimum duration of nPERR is one clock cycle.

Name	Pin	Type	Description
nSERR	30	O	System Error (open drain). This pin goes low when address parity errors are detected.
PAR	31	I/O	Even Parity. Parity is even parity across AD31-0 and nC/BE3-0. PAR is stable and valid one clock after the address phase. For the data phase, PAR is stable and valid one clock after either nIRDY is asserted on a write transaction, or nTRDY is asserted on a read transaction.
nC/BE3	8	I	Bus Command and Byte Enable. During the address phase of a transaction, nC/BE3-0 define the Bus Command. During the data phase, nC/BE3-0 are used as Byte Enables. nC/BE3 applies to Byte “3”.
nC/BE2	22	I	Bus Command and Byte Enable. During the address phase of a transaction, nC/BE3-0 define the Bus Command. During the data phase, nC/BE3-0 are used as Byte Enables. nC/BE3 applies to Byte “2”.
nC/BE1	32	I	Bus Command and Byte Enable. During the address phase of a transaction, nC/BE3-0 define the Bus Command. During the data phase, nC/BE3-0 are used as Byte Enables. nC/BE3 applies to Byte “1”.
nC/BE0	43	I	Bus Command and Byte Enable. During the address phase of a transaction, nC/BE3-0 define the Bus Command. During the data phase, nC/BE3-0 are used as Byte Enables. nC/BE3 applies to Byte “0”.
nINTA	120	O	PCI active low Interrupt Output (open-drain). This signal goes low (active) when an interrupt condition occurs.
EE-CS	115	O	External EEPROM chip select (active high). After Power-On Reset, The EEPROM is read and the read-only configuration registers are loaded sequentially from the first 64 Bytes in the EEPROM.
EE-CLK	116	O	External EEPROM Clock.
EE-DI	118	I	External EEPROM Data Input.
EE-DO	117	O	External EEPROM Data Output.
EE-EN	123	I	Enable external EEPROM (active high, internal pull-up). The external EEPROM can be disabled when this pin is tied to GND or pulled low. When disabled, default values for the PCI configuration registers will be used.

Name	Pin	Type	Description
XTAL1	62	I	Crystal oscillator input or external clock input pin (22.1184 MHz). This signal input is used in conjunction with XTAL2 to form a feedback circuit for the internal timing. Two external capacitors (10pF) connected from each side of the XTAL1 and XTAL2 to GND are required to form a crystal oscillator circuit.
XTAL2	61	O	Crystal oscillator output. See XTAL1 description.
12XCLK	58	O	External clock or crystal oscillator clock divided by 12 output (1.8432 MHz standard PC UART clock for 115.2k data rate).
6XCLK	56	O	External clock or crystal oscillator clock divided by 6 output (3.6864 MHz PC UART clock for 230.4k data rate).
3XCLK	55	O	External clock or crystal oscillator clock divided by 3 output (7.3728 MHz UART clock for 460.8k data rate).
SLCT	68	I	Peripheral/printer Selected (internal pull-up). This pin is set high by the peripheral/printer when it is selected.
PE	69	I	Paper Empty (internal pull-up). This pin is set high by the peripheral/printer when printer paper is empty.
BUSY	70	I	Peripheral/printer Busy (internal pull-up). This pin is set high by the peripheral/printer when it is not ready to accept data.
nACK	71	I	Peripheral/printer Data Acknowledge (internal pull-up). This pin is set low by the peripheral/printer to indicate a successful data transfer has taken place. During SPP mode when interrupts are enabled, the nINTA pin follows the nACK input pin state.
nFAULT	72	I	Peripheral/printer Data Error (internal pull-up). This pin is set low by the peripheral/printer during an error condition.
nSTROBE	76	I/O	Peripheral/printer Data Strobe (open drain, active low). Informs the printer there is valid data on the Bus.
nAUTOFDX	75	I/O	Peripheral/printer Auto Feed (open-drain, active low). Continuous autofed paper is selected when this pin is set low.
nINIT	74	I/O	Initialize the Peripheral/printer (open drain, active low). When set low, the peripheral/printer starts it’s initialization routine.
nSLCTIN	73	I/O	Peripheral/printer Select (open-drain, active low). Selects the peripheral/printer when it is set low.
PD7-PD4	105-107	I/O	Peripheral/printer Data bits.
PD3-PD0	109-113	I/O	Peripheral/printer Data bits.
nCS3	103	O	Chip Select 3 (Active-Low).

Name	Pin	Type	Description
nCS4	102	O	Chip Select 4 (Active-Low).
nCS5	101	O	Chip Select 5 (Active-Low).
nCS6	100	O	Chip Select 6 (Active-Low).
IRQ5-2	84-87	I	Active-High Interrupt inputs. All unused interrupts must be connected to GND for proper operation.
nIRQ6	83	I	Active-Low Interrupt input. This pin should be tied to Vcc if it is not used.
nIOR	81	O	External Peripheral Read signal (Active-Low).
nIOW	80	O	External Peripheral Write signal (Active-Low).
RST	79	O	External Peripheral Reset Signal (Active-High).
nRST	78	O	External Peripheral Reset Signal (Active-Low).
A0-2	63-65	O	External Peripheral Address Lines.
D7-D4	98-95	I/O	External Peripheral Data Bus.
D3-D0	93-90	I/O	External Peripheral Data Bus.
GND	7,20,21, 33,44,45, 60,77,88, 94,99,108 119,125	Pwr	Power and Signal Ground.
VCC	1,10,19, 39,54,66, 82,89,104 114	Pwr	Supply. Voltage

PCI Bus Operation:
The execution of PCI Bus transactions take place in broadly five stages: address phase; transaction claiming; data phase(s); final data transfer; and transaction completion.

Address Phase:
Every PCI transaction starts with an address phase, one PCI clock period in duration. During the address phase the initiator (also known as the current Bus Master) identifies the target device (via the address) and type of transaction (via the command). The initiator drives the 32-bit address onto the Address/Data Bus, and a 4-bit command onto the Command/Byte-Enable Bus. The initiator also asserts the nFRAME signal during the same clock cycle to indicate the presence of valid address and transaction information on those buses. The initiator supplies the starting address and command type for one PCI clock cycle. The target generates the subsequent sequential addresses for burst transfers. The Address/Data Bus becomes the Data Bus, and the Command/Byte-Enable Bus becomes the Byte-Enable Bus for the remainder of the clock cycles in that transaction. The target latches the address and command type on the next rising edge of PCI clock, as do all other devices on that PCI bus. Each device then decodes the address and determines whether it is the intended target, and also decodes the command to determine the type of transaction.

Claiming The Transaction:
When a device determines that it is the target of a transaction, it claims the transaction by asserting nDEVSEL.

Data Phase(s):
The data phase of a transaction is the period during which a data object is transferred between the initiator and the target. The number of data Bytes to be transferred during a data phase is determined by the number of Command/Byte-Enable signals that are asserted by the initiator during the data phase. Each data phase is at least one PCI clock period in duration. Both initiator and target must indicate that they are ready to complete a data phase. If not, the data phase is extended by a wait state of one clock period in duration. The initiator and the target indicate this by asserting nIRDY and nTRDY respectively and the data transfer is completed at the rising edge of the next PCI clock.

Transaction Duration:
The initiator, as stated earlier, gives only the starting address during the address phase. It does not tell the number of data transfers in a burst transfer transaction. The target will automatically generate the addresses for subsequent Data Phase transfers. The initiator indicates the completion of a transaction by asserting nIRDY and de-asserting nFRAME during the last data transfer phase. The transaction does not actually complete until the target has also asserted the nTRDY signal and the last data transfer takes place. At this point the nTRDY and nDEVSEL are de-asserted by the target.

Transaction Completion:
When all of nIRDY, nTRDY, nDEVSEL, and nFRAME are in the inactive state (high state), the bus is in idle state. The bus is then ready to be claimed by another Bus Master.

PCI Resource Allocation

PCI devices do not have "Hard-Wired" assignments for memory or I/O Ports like ISA devices do. PCI devices use "Plug & Play" to obtain the required resources each time the system boots up. Each PCI device can request up to six resource allocations. These can be blocks of memory (RAM) or blocks of I/O Registers. The size of each resource block requested can also be specified, allowing great flexibility. Each of these resource blocks is accessed by means of a Base-Address-Register (BAR). As the name suggests, this is a pointer to the start of the resource. Individual registers are then addressed using relative offsets from the Base-Address-Register contents. The important thing to note is: plugging the same PCI card into different machines will not necessarily result in the same addresses being assigned to it. For this reason, software (drivers, etc.) must always obtain the specific addresses for the device from the PCI System.

Each PCI device is assigned an entry in the PCI System's shared "Configuration Space". Every device is allocated 256 Bytes in the Configuration Space. The first 64 Bytes must follow the conventions of a standard PCI Configuration "Header". There are several pieces of information the device must present in specific fields within the header to allow the PCI System to properly identify it. These include the Vendor-ID, Device-ID and Class-Code. These three fields should provide enough information to allow the PCI System to associate the correct software driver with the hardware device. Other fields can be used to provide additional information to further refine the needs and capabilities of the device.

As part of the Enumeration process (discovery of which devices are present in the system) the Base-Address-Registers are configured for each device. The device tells the system how many registers (etc.) it requires, and the system maps that number into the system's resource space, reserving them for exclusive use by that particular device. No guarantees are made that any two requests for resources will have any predictable relationship to each other. Each PCI System is free to use its own allocation strategy when managing resources.

Multi-Function Devices

MosChip uses the Subsystem-ID field to indicate how many Serial Ports and Parallel Ports are provided by the current implementation. By changing the data in the Subsystem-ID field, and stuffing only the appropriate number of external components, the same board could be used for products with either one or two Ports. The least significant Hexadecimal digit of the Subsystem-ID field indicates the number of Serial Ports that are currently being provided by the device. The next higher digit indicates the number of Parallel Ports being provided. The table below shows several different combinations and the types of Ports that would be enabled. Some MosChip devices provide Serial Ports, some provide Parallel Ports, and some provide both types of Ports. This field is used as an aid to the software Drivers, allowing them to easily determine how many of each Port type to configure.

Subsystem-ID	Parallel Ports	Serial Ports
0001	0	1
0010	1	0
0012	1	2

This use of the term "Multi-Function Device" should not be confused with the more generic use of that term by the PCI System. Each "Function" within a "Unit" (physical device) gets its own Configuration Space Header. MosChip's devices do not need this extra layer of complexity, the six Base Address Registers provided by one PCI "Function" are more than adequate to allocate all of the desired resources.

External EEPROM

Data is read from the EEPROM immediately after a Hardware Reset, and the values obtained are used to update the Configuration before the PCI System first sees the device on the Bus. This allows a vendor to substitute their own ID codes in place of the MosChip codes for example. If no EEPROM is detected after a Hardware Reset, MosChip's default values for the configuration are provided by the chip itself.

PCI Configuration Space Header

Default values for several key fields are shown in the table below.

AD 31-23	AD 22-16	AD 15-8	AD 7-0	Offset (Hex)
Device ID (9755)		Vendor ID (9710)		00
Status		Command		04
Class Code (070002)			Revision ID (01)	08
BIST	Header Type	Latency Timer	Cache Size (08)	0C
Base Address Register (BAR) 0 – “Standard Registers” (Y)				10
Base Address Register (BAR) 1 – “Extended Registers” (W)				14
Base Address Register (BAR) 2 – “nCS3” (E3)				18
Base Address Register (BAR) 3 – “nCS4” (E4)				1C
Base Address Register (BAR) 4 – “nCS5” (E5)				20
Base Address Register (BAR) 5 – “nCS6” (E6)				24
Reserved				28
Subsystem ID (0010)		Subsystem Vendor ID (1000)		2C
Reserved				30
Reserved				34
Reserved				38
Max Latency (00)	Min Grant (00)	Interrupt Pin (01)	Interrupt Line	3C

Internal Address Select Configuration

The Nm9755 uses two Base Address Registers for its Parallel Port, and four for the ISA Bridge.
These essentially act as internal “Chip Select” logic.
Registers are addressed by using one of the Base Addresses plus an offset.

BAR	I/O Address Offset	Function
0 (Y)	00-07	Standard Parallel Port Registers
1 (W)	00	Configuration Register A
1 (W)	01	Configuration Register B
1 (W)	02	Extended Control Register (ECR)
2 (E3)	00-07	External Chip Select 3
3 (E4)	00-07	External Chip Select 4
4 (E5)	00-07	External Chip Select 5
5 (E6)	00-07	External Chip Select 6

Parallel Port Registers

CS	A2	A1	A0	Register	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Y	0	0	0	DPR	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Y	0	0	1	DSR	nBUSY	nACK	PE	SLCT	nFAULT	INT State	"0"	EPP TIMEOUT
Y	0	1	0	DCR	"0"	"0"	DIR	INTA	SLCTIN	nINIT	AUTOFDX	STROBE
Y	0	1	1	EPP Address	ADD-7	ADD-6	ADD-5	ADD-4	ADD-3	ADD-2	ADD-1	ADD-0
Y	1	0	0	EPP Data	DAT-7	DAT-6	DAT-5	DAT-4	DAT-3	DAT-2	DAT-1	DAT-0
Y	1	0	1	Res	Res	Res	Res	Res	Res	Res	Res	Res
Y	1	1	0	Res	Res	Res	Res	Res	Res	Res	Res	Res
Y	1	1	1	Res	Res	Res	Res	Res	Res	Res	Res	Res
W	0	0	0	C-FIFO	CDAT-7	CDAT-6	CDAT-5	CDAT-4	CDAT-3	CDAT-2	CDAT-1	CDAT-0
W	0	0	0	CONF-A	"1"	"0"	"0"	"1"	"0"	"1"	"0"	"0"
W	0	0	1	CONF-B	RLE	nINTA Pin	Interrupt Line			DMA Line		
W	0	1	0	ECR	Mode Select			ErrIntrEn Enable	DMA Enable	Service Interrupt	FIFO Full	FIFO Empty

Y: Standard Registers Chip Select
W: Extended Registers Chip Select

Master Reset Conditions

Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
DPR	X	X	X	X	X	X	X	X
DSR	0	1	1	1	1	0	0	0
DCR	0	0	0	0	1	1	0	0
EPP	0	0	0	0	0	0	0	0
C-FIFO	0	0	0	0	0	0	0	0
CONF-A	1	0	0	1	0	1	0	0
CONF-B	0	X	0	0	0	0	0	0
ECR	0	0	1	1	0	1	0	1

Data Register (DPR)
The Data register is cleared at initialization by RESET. During a write operation the contents of this register are buffered and output onto the PD7-PD0 pins. During a read operation PD7-PD0 pins are buffered and output to the host CPU.

Device Status Register

Note: Bit-7 of this register is logically inverted from the state of the electrical signal appearing at the physical device pin. When the printer is BUSY, this bit will read back as a zero.

DSR Bit-0: EPP Timeout

0 = Normal.

1 = 10μs timeout (EPP Mode only). Cleared by writing 1 into DSR register or consecutive reads (after the first read) always returns to “0”.

DSR Bit-1:

Not used, set to “0”.

DSR Bit-2: Interrupt State

0 = Interrupt Pending (nINTA follows the nACK pin when SPP mode is selected). Normal (no interrupt) when PS/2 mode is selected.

1 = Normal (no interrupt). This bit is set to “1” when the DSR is read.

DSR Bit-3: nFAULT

0 = Printer reports error condition.

1 = Normal operation.

DSR Bit-4: SLCT

0 = Printer is off-line.

1 = Printer is on-line.

DSR Bit-5: PE

0 = Normal operation.

1 = Paper end/empty is detected.

DSR Bit-6: nACK

0 = State of the nACK pin (nACK = low).

1 = State of the nACK pin (nACK = high).

DSR Bit-7: nBUSY

0 = BUSY pin is high, printer is not ready to take data.

1 = BUSY pin is low, printer is ready to take data.

Device Control Register

Note: Three bits (0, 1, & 3) of this register are logically inverted from the state of the electrical signals appearing at the physical device pins they control. The physical pins for these three bits are all Active-Low signals, so writing a “one” in this register will enable or activate the desired function. The physical pin associated with Bit-2 (nINIT) of this register is also an Active-Low electrical signal. This bit is not inverted however, so in order to start the Initialization process, that bit must be set LOW.

DCR Bit-0: STROBE

0 = Sets the nSTROBE pin to high.

1 = Sets the nSTROBE pin to low. PD7-PD0 data are latched into printer.

DCR Bit-1: AUTOFDX

0 = Sets the nAUTOFDX pin to high.

1 = Sets the nAUTOFDX pin to low. Printer generates auto line feed after each line is printed.

DCR Bit-2: nINIT

0 = Sets the nINIT pin to low. Peripheral/printer starts its initialization routine.

1 = Sets the nINIT pin to high.

DCR Bit-3: SLCTIN

0 = Sets the nSLCTIN pin to high.

1 = Sets the nSLCTIN pin to low. Selects the printer.

DCR Bit-4: INTA

0 = Disables Printer interrupt function. nACK pin has no effect on the nINTA pin.

1 = Enables Printer interrupt function. The nINTA pin follows the nACK input pin during standard mode, latches high on the rising edge of the nACK when PS/2 mode is selected.

DCR Bit-5: DIR

0 = PD7-PD0 pins are set to output mode.

1 = PD7-PD0 pins are set to input mode.

DCR Bits 7-6:

Not used, set to “0”.

EPP-Address Register
Reading this register typically returns the address currently selected within the printer or external device.

Writing to this register typically selects a different address or function within the external device that will be the target for subsequent data transfers. A multi-function device might use different addresses for Printing, Scanning and Faxing operations.

All handshaking for the EPP Protocol is performed automatically by the hardware. Software does not need to manually toggle strobe bits, check for acknowledgement that the data was received, etc. The software only needs to read or write a single Byte to this location to perform the entire transaction. This allows significantly faster transfers when compared to SPP Mode transfers.

EPP-Data Register
Reading this register returns the next Byte of data associated with the address currently selected within the printer or external device.

Writing to this register sends a Byte of data to the address currently selected within the printer or external device.

All handshaking for the EPP Protocol is performed automatically by the hardware. Software does not need to manually toggle strobe bits, check for acknowledgement that the data was received, etc. The software only needs to read or write a single Byte to this location to perform the entire transaction. This allows significantly faster transfers when compared to SPP Mode transfers.

C-FIFO Register
This register is used in Mode "110" (FIFO Test).

The FIFO Test Mode allows writing data into, and reading data back out of the FIFO without actually transferring any data to the printer. All flags (FIFO Full, FIFO Empty, etc.) are active in this mode so all aspects of the FIFO operation can be observed.

This register is accessed using the BAR1 (W) Base Address Register.

Config-A Register
This register is read only.
Reading this register always returns 10010100.
The meaning of these bits are:

Bit-7 = 1	Interrupts are Level-Triggered.
Bit-6:4 = 001	The Port only accepts 8-bit words.
Bit-3 = 0	Reserved
Bit-2 = 1	The Byte currently in the transmitter pipeline affects the "FIFO Full" flag.
Bit-1:0 = 00	In the case of an error, the unsent Byte is left in the FIFO.

This register is accessed using the BAR1 (W) Base Address Register.
This register can only be accessed when the Port is set to use Mode "111" (Config A/B Enable).

Config-B Register
Returns information about the ECP capabilities.

Bit 7: RLE
Set to "0". RLE is not supported.

Bit 6: nINTA Pin
0 = The current nINTA state is low.
1 = The current nINTA state is high.

Bit 5-3: Interrupt Line
Set to "000". The IRQ is set by the PCI System.

Bit 2-0: DMA Line
Set to "000". DMA is not used.

This register is accessed using the BAR1 (W) Base Address Register.
This register can only be accessed when the Port is set to use Mode "111" (Config A/B Enable).

Extended Control Register (ECR)
This register controls Mode Selection and returns Interrupt and FIFO Status.
This register is accessed using the BAR1 (W) Base Address Register.

ECR Bit-0: FIFO Empty
0 = One or more characters of data are in the FIFO.
1 = FIFO empty.

ECR Bit-1: FIFO Full
0 = One or more locations in the FIFO are available.
1 = FIFO full.

ECR Bit-2: Service Interrupt
1 = Disables the Service Interrupt. Writing a "1" to this bit will not cause an interrupt.
0 = Enables the Service Interrupt. A Service Interrupt occurs and this bit will be set to a "1" by the hardware when:

- Port Direction = Output (DCR Bit-5 = 0) and there are write interrupt threshold (4 characters) or more Bytes free in the FIFO.
- Port Direction = Input (DCR Bit-5 = 1) and there are read interrupt threshold (12 characters) or more Bytes to be read from the FIFO.

ECR Bit-3: DMA Enable
The Parallel Port does not support DMA. Equivalent transfer speeds are obtained automatically by using PCI Bus Master "burst" transfers.
This bit should always remain set to "0".

ECR Bit-4: Error Interrupt Enable.
0 = Enable nFAULT interrupt. The nFAULT pin is used as a source of interrupts.
1 = Disable nFAULT interrupt.

ECR Bit-7-5: Mode Select
The Parallel Port can operate in several different "Modes". These three bits are used to select the desired Mode.

Bit-7	Bit-6	Bit-5	Operating Mode
0	0	0	SPP
0	0	1	PS/2
0	1	0	Not used
0	1	1	ECP
1	0	0	EPP
1	0	1	Not used
1	1	0	FIFO Test
1	1	1	Config A/B Enable

Mode "000"
SPP/Centronics/Compatibility Mode

This mode operates in the forward direction only. The DIR bit is forced to "0" and PD7-PD0 are always set to the output direction. All control signals (nSTROBE etc.) are under software control. This mode defines the protocol used by most PCs to transfer data to a printer. Data is placed on the PD7-PD0 pins and the printer status is checked via the DSR register. If no error condition is flagged and the printer is not busy, software toggles the nSTROBE pin to latch the PD7-PD0 data into the printer. The printer/peripheral acknowledges receiving the data by pulsing the nACK and BUSY pins.

Nibble Mode

The Nibble mode is the most common way to get reverse channel data from a printer or peripheral. This mode is usually combined with the SPP/Centronics mode to create a bi-directional channel. Printer status bits are used as Nibble bits for the reverse channel data. The same Status bits are used for each Nibble, so special handshaking is required. When both Nibbles have been received, the PC must combine them to form the intended Byte of data.

Pin	Data Bit
BUSY	Bit-7
PE	Bit-6
SLCT	Bit-5
nFAULT	Bit-4
BUSY	Bit-3
PE	Bit-2
SLCT	Bit-1
nFAULT	Bit-0

Bit usage for Nibble Mode

Mode "001"
PS/2, (Byte) Mode

The Byte Mode protocol is used to transfer bi-directional data via the PD7-PD0 pins. The FIFO is not used in this mode. The direction of the port is controlled with the DIR bit in the DCR register. PS/2 (Byte) Mode uses the same handshaking protocol as SPP Mode for data transfers.

DCR Bit-5: DIR
0 = PD7-PD0 pins are set to output mode.
1 = PD7-PD0 pins are set to input mode.

Mode "011"
Extended Capability Port "ECP" Mode

ECP Mode is an advanced mode for communication with printers or peripherals. A 16-Byte FIFO provides a high performance bi-directional communication path. The following cycle types are provided in both the forward and reverse directions:

- Data cycle
- Command cycle
- Run-Length-Encoding (RLE)
- Channel Address

Run Length Encoding (RLE) provides data compression of up to 64:1. This is particularly useful for printers and peripherals that transfer raster images with long strings of identical data. In order for RLE to be enabled, both the host and peripheral must support it.

Channel addressing allows for multiple logical devices within a single physical unit, like Scanner/FAX/Printer in one physical package.

Mode "100"

Enhanced Parallel Port "EPP" Mode

In EPP Mode several control signals are used for different purposes than those described for the default SPP & PS/2 Modes. The nSLCTIN line is used as an "Address Strobe", and nAUTOFDX is used as the Data Strobe signal. The appropriate "Strobe" signal is automatically generated when data is read or written to one the EPP Specific registers. The nSTROBE signal is re-defined to indicate whether the current transfer is a write or read cycle. Separate I/O addresses are defined for "Data" and "Address" access, and when these locations are used handshaking is performed automatically by the chip.

Mode "110"

FIFO Test Mode

In this mode the FIFO can be written and read, but no data will be transmitted to the printer. Whatever data is in the FIFO may be output on the PD7-PD0 pins, but no control signals will be generated to signal a transfer is to take place. All of the status Flags (FIFO Full, FIFO Empty, etc.) are operational in this mode, so the complete operation of the FIFO can be observed without actually affecting the external device.

Mode "111"

Config A/B Enable Mode

This mode must be selected whenever the Config-A or Config-B registers are accessed. The Config-A register uses the same I/O Address as the FIFO Register. Only allowing access to the Configuration Registers when this special Mode is selected prevents the two registers from interfering with each other.

Mode Changes

After a hardware reset, PS/2 mode is selected as the default mode. When changing to a different mode, it is necessary to select mode 000 or 001 first, then any other desired mode configuration.

ISA Bridge
A PCI to ISA Bridge allows the product designer to increase the number of I/O Ports through the use of external components. Additional UARTs and Parallel Ports are easy to attach and configure.

Chip Selects
Four external Chip Select signals (nCS3-nCS6) are provided. Each Chip Select has its own Base Address Register (BAR) in the PCI Configuration Space. The Base Address Registers each point to a block of eight I/O registers. When any of the eight registers in the block assigned to one of the Base Address Registers are accessed, the Chip Select signal for that group will be activated. The following table shows the relationship between the Base Address Registers and the external Chip Select signals.

BAR	Offset	Chip Select
2 (E3)	00-07	nCS3
3 (E4)	00-07	nCS4
4 (E5)	00-07	nCS5
5 (E6)	00-07	nCS6

If BAR-3 contains the address 0xD800, then accessing any address between 0xD800 and 0xD807 will activate the nCS4 Chip Select line.

Common I/O Control Signals
In addition to the Chip Select signals, the other required ISA signals are also present. Separate nIOR (I/O Read) and nIOW (I/O Write) signals are provided, simplifying the interface to external components. An 8-bit bi-directional Data Bus is provided. Both Active-High and Active-Low Reset signals are provided, simplifying the connection to external devices. Three Address Lines (A0-2) allow each Chip Select to control eight registers.

Interrupts
ISA style devices typically use Active-High Interrupt Request signals. Four Active-High Interrupt Request inputs (IRQ2-5) are provided. A single Active-Low Interrupt Request input (nIRQ6) is also available providing even more flexibility. There is no mechanism provided to directly associate any of the Interrupt Request signals with any of the external Chip Select signals. The Interrupt Requests are simply passed on to the PCI system. All I/O Ports or devices (including those inside the chip) share a single PCI Interrupt Request line. The software Driver must poll all of the devices to determine which one is the source of an interrupt.

Other Devices
While the primary purpose of the ISA Bridge is to allow products to provide additional UARTs or Parallel Ports, it is not necessarily restricted to such devices. The signals provided should allow the inclusion of most ISA style components into a custom design. If custom (or other standard ISA) components are used, a custom software Driver will probably be required as well. The MosChip Drivers only support additional UARTs and Parallel Ports. Simple custom devices that always have the CPU initiate reads or writes to the device may work without any additional Drivers, but any design that adds external components that generate Interrupt Requests will definitely require custom Drivers.

Electrical Characteristics

Absolute Maximum Ratings

Supply Voltage	6 Volts
Voltage at any pin	GND - 0.3 V to V_{CC} + 0.3 V
Operating Temperature	-45 to +90 °C
Storage Temperature	-55 to +150 °C

Recommended Operating Conditions

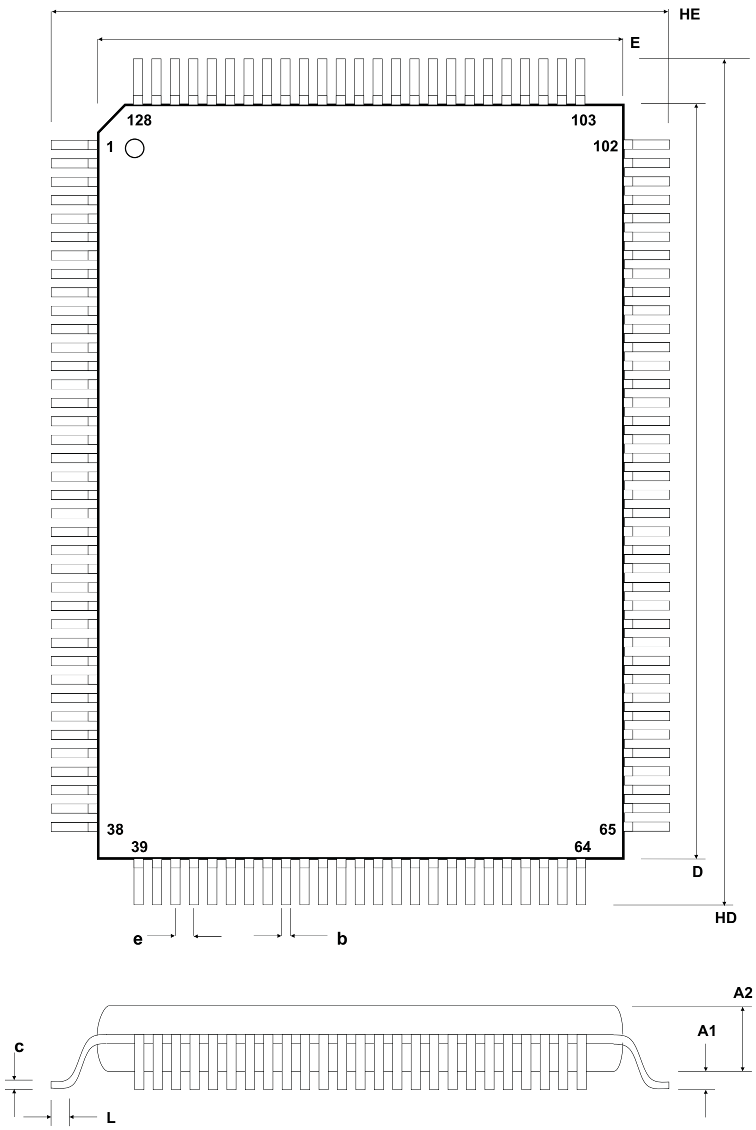
Symbol	Parameter	Min	Typ	Max	Unit	Condition
Vcc	Supply Voltage (Nm Series Device)	4.5	5.0	5.5	V	
Vin	Input Voltage	0		Vcc	V	
Tj	Junction Operating Temperature (Commercial)	0	25	115	°C	

General DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Condition
	Package Dissipation			500	mW	
	ESD			±2000	V	
	Latch up		220		mA	
Ii_L	Input Leakage Current	-1		1	µA	No Pull-Up or Pull-Down
Io_Z	Tri-State Leakage Current	-10		10	µA	
Cin	Input Capacitance		3		pF	
Cout	Output Capacitance		3		pF	
Cbid	Bi-Directional Buffer Capacitance		3		pF	

DC Electrical Characteristics (5V Operation)
Ambient Temp = 0 to +70 °C, V_{CC} = 4.75 to 5.25 V, Tj = 0 to +115 °C unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Condition
Vi_L	Input Voltage (Low)			0.3 * Vcc	V	CMOS
Vi_H	Input Voltage (High)	0.7 * Vcc			V	CMOS
Vi_L	Input Voltage (Low)			0.8	V	TTL
Vi_H	Input Voltage (High)	2.0			V	TTL
Vt-	Schmitt Trigger Negative-Going Threshold Voltage		1.84		V	CMOS
Vt+	Schmitt Trigger Positive-Going Threshold Voltage		3.22		V	CMOS
Vt-	Schmitt Trigger Negative-Going Threshold Voltage		1.10		V	TTL
Vt+	Schmitt Trigger Positive-Going Threshold Voltage		1.87		V	TTL
Vo_L	Output Voltage (Low)			0.4	V	Io_L = 2 to 24 mA
Vo_H	Output Voltage (High)	3.5			V	Io_H = 2 to 24 mA
Ri	Input Pull-Up/Pull-Down Resistance		50		KΩ	Vi_L = 0V or Vi_H = Vcc



128-Pin VQFP
Package Dimensions

Symbol	Millimeters			Inches		
	Min	Typ	Max	Min	Typ	Max
A1	0.10		0.30	0.004		0.012
A2	2.73		2.97	0.107		0.117
b	0.17		0.27	0.007		0.011
c	0.09		0.20	0.004		0.008
e		0.50			0.020	
L	0.70		1.03	0.029		0.041
HD	23.00		23.40	0.906		0.921
D	19.90		20.10	0.783		0.791
HE	17.00		17.40	0.669		0.685
E	13.90		14.10	0.547		0.555

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Revision History

Revision	Changes	Date
1.0	Initial Release	Jul-2000
2.0	Revised Data Sheet Format	28-Apr-2006