5.4 System Function Control-
Index Registers

The 82C351 has index registers for various system control functions. These registers are accessed through ports 22H and 23H. An indexing scheme is used to reduce the number I/O addresses required to access all registers needed to configure and control the CHIP set.Each access(either read or write) to an internal register is done by first writing its index into port 22H.Then read port 23H (if reading of the register is required) or write to port 23H (if writing of the selected index register is required.) Every access to port 23 should be preceded by writing index value to port 22H even if the same data port is being accessed again.

Port 92H can be accessed directly without going through indexing.

Port 92H Fast GATE A20 and RESET Register

This port is active only if Index 2B bit 6 is a 1
NOTE: This port is used by OS/2 and can be disabled by writing a 0 to index register 2B bit 6.

Address	Bits	Description
92H	7-2	Reserved
	1	Fast GATEA20
		0:Force CPU A20 low
		(1):Enable CPU A20
		Fast CPU enable
		(0):A 0 to 1 transition
		causes a CPU reset.

Index Registers (accesses are through IO ports 22 and 23).

Name: Revision Registers (READ ONLY)

Index	Bits	Values and Functions
04H	7-4	: Undefined
	3-0	: Revision Level

AT Bus Command Delays (READ/WRITE)

Index	Bits	Values and Functions
05H	7:6	(00) : Reserved
	5:4	AT bus 16 bit memory command delay
		(00):0 BCLK delay
		(01):1 BCLK delay
		10 :2 BCLK delay
		11 :3 BCLK delay
	3:2	AT bus 8 bit memory command delay
		00 :0 BCLK delay
		(01):1 BCLK delay
		10 :2 BCLK delay
		11 :3 BCLK delay
	1:0	AT bus I/O command delay
		00 :0 BCLK delay
		(01):1 BCLK delay
		10 :2 BCLK delay
		11 :3 BCLK delay

Name: AT bus Wait States (READ/WRITE)

Index Bits Values and Functions

06H   7:6 (00) : Reserved

5:4 16 bit AT bus wait states
(00):3 BUSCLK wait states
01:2 BUSCLK wait states
10:1 BUSCLK wait states
11:0 BUSCLK wait states

3:2 8 bit AT bus wait states
(00):5 BUSCLK wait states
01:4 BUSCLK wait states
10:3 BUSCLK wait states
11:2 BUSCLK wait states

1 AT bus address hold time. (Provides extra address time for adapter cards that require it for reliable operation)
(0):Disable extra address hold time on AT bus
1:Enable extra address hold time on AT bus (delays next cycle by one $T_r$state and holds current address valid.

0 Reserved

Name: AT Clock Source Select (READ/WRITE)

Index Bits Values Functions

07H   7:3 (0000) : Reserved

2:0 Bus Clock Source Select (BCLK). BUSCLK= BCLK/2
(000):CLK2IN/5
001:CLK2IN/4
010:CLK2IN/3
011:CLK2IN/2
100:ATCLK

Name: Initial Memory, CPU Speed (READ/WRITE)

Index	Bits	Values and Functions
08H	7:4	(00000) :Reserved

3   486 MODE
(0): Default
1 = EADS on VRAMSEL output
KEN on HLDA2 output

2   -AF32 assertion control
(0): Does not generate-AF32 for addresses
above 16MB.Should only be used if external
logic can recognize address above 16MB.
1 : Generates-AF32 for address above 16 MB.
Unless real physical memory is installed for
that address range. no memory cycles starts
and no -READY is given to the CPU.

1   Initial memory
(0): Only 512 K memory enabled.Registers
0C to 0F are ignored.Register 2A can also
affect the bottom 512K .
1: Registers 0C-0F can enable the memory
above 512K .

0   CPUCLK (CPU Clock) select
(0): Selects CLK2IN
1: Selects AT control logic clock (BCLK)

Bits 7 to 4 write protect RAM located in the BIOS
area in 64KB blocks.Bits 3 to 0 enable the substitution
of the BIOS ROM located below 1MB with RAM at the
same location in 64KB blocks. This should be done
after BIOS code is copied from the ROM and the RAM
locations have been protected using bits 7 to 4.
Make sure registers 0C-0F are enabled if RAM accesses
are required.

Index	Bits	Values and Functions
09H	7	64KB RAM at 768K C0000-CFFFFH(VIDEO) (0): 64KB of RAM at 768K is read/write 1: 64KB of RAM at 768K is read only
	6	64KB RAM type at 832K D0000-DFFFFH (0): 64KB of RAM at 832K is read/writ 1: 64KB of RAM at 832K is read only
	5	64KB RAM at 896K E0000-EFFFFH (0): 64KB of RAM at 896K is read/write 1: 64KB of RAM at 896K is read only
	4	64KB RAM type at 960K F0000-EFFFFH(SYSTEM) (0): 64KB of RAM at 960K is read/writ 1: 64KB of RAM at 960K is read only
	3	64KB ROM at 768K C0000-CFFFFH (VIDEO) (0): 64KB of ROM at 768K is disabled 1: 64KB of ROM at 768K is enabled
	2	64KB ROM at 832K D0000-DFFFFH (0): 64KB of ROM at 832K is disabled 1: 64KB of ROM at 832K is enabled
	1	64KB ROM at 896K E0000-EFFFFH (0): 64KB of ROM at 896K is disabled 1: 64KB of ROM at 896K is enabled
	0	64KB ROM type at 960K F0000-FFFFFH (SYSTEM (0): 64KB of ROM at 960K is disabled 1: 64KB of ROM at 960K is enabled

Index registers 0CH through 0FH control whether memory is located or controlled by the system board or the AT bus.   Each bit controls a 16KB block.   Bit 0 enables the lowest and bit 7 the highest 16K block in each 128KB memory area.   For example, bit 0 of index register 0CH controls the 16K block from 080000H to 083FFFH (512KB to 528KB).   This permits selective 16K blocks of memory to be disabled, allowing ROMs, memory expansion schemes (EMS ,EEMS or XMA) or memory mapped I/O devices to reside within the lower 1MB address space.

Index Bits Values and Functions

0CH 7:0   Memory enable map - 080000-09FFFFH (Read/Write)

0DH 7:0   Memory enable map - 0A0000-0BFFFFH (Read/Write)

0EH 7:0   Memory enable map - 0C0000-0DFFFFH (Read/Write)

0FH 7:0   Memory enable map - 0E0000-0FFFFH(Read/Write)

Enable bits for eight 16K blocks of memory
0: Address is on or controlled by the
system board: 16K block enabled
(1): Address is on the I/O channel;16K
block disable

Name: Bank 0/1 Type and Starting address (READ/ WRITE)

Index Bits Values and Functions

10H   7:6   DRAM type in bank 0/1
00:Bank0/1 disabled
(01):1Mx1 or 1Mx4 DRAMs
10 : 1Mx1 or 1Mx4 DRAMS
11:4Mx1 or 4Mx4 DRAMs

5:0 (000000) : Starting address for Block 0 A26 to A21.

256K usage A<26:21> (1MB per block, interleaved)
(2MB per block, non-interleaved)
1M   usage A<26:23> (4MB per block)
(8MB per block, non-interleaved)
4M   usage A<26:25> (16MB per block)
(32MB per block, non-interleaved)

Name: Bank 0/1 RAM timing (READ/WRITE)

Index   Bits   Values and Functions

11H   7:5   (000) : Reserved - write 000

             00:3 wait states
             01:4 wait states
             (10):5 wait states
             11:Reserved

         4:3   RAS precharge time, RAS $<0:1>$ non-interleaved, RAS $<0>$ interleave
             00:3 CPUCLKIN cycles
             01:4 CPUCLKIN cycles
             10:5 CPUCLKIN cycles
             (11)6 CPUCLKIN cycles

         2:1   -RAS Refresh pulse width (for all banks)
             00:4 CPUCLKIN cycles
             01:5 CPUCLKIN cycles
             10:6 CPUCLKIN cycles
             (11):7 CPUCLKIN cycles

         0   (0):Reserved - write 0

Name: Bank 2/3 Type and Starting address (READ/WRITE)

Index   Bits   Values and Functions

12H   7:6   DRAM type 1 in block 1
             00:Block 1 disabled
             (01):256Kx1 or 256Kx4 DRAMs
             10:1Mx1 or 1Mx4 DRAMs
             11:4Mx1 or 4Mx4 DRAMs

         5:0   (000000) Starting address for block 1

         256K usage   A$<26:21>$ (1MB per block, interleaved)
                        (2MB per block, non-interleaved)
         1M   usage   A$<26:23>$ (4MB per block)
                        (8MB per block, non-interleaved)
         4M   usage   A$<26:25>$ (16MB per block)
                        (32MB per block, non-interleaved)

Name: Bank 2/3 RAM timing (READ/WRITE)

Index	Bits	Values and Functions
13H	7:5	(000) Reserved - write 000

4:3 RAS percharge time
(RAS $<2:3>$ non-interleaved)
(RAS $<2>$ interleaved)
00:3 CPUCLKIN cycles
01:4 CPUCLKIN cycles
10:5 CPUCLKIN cycles
(11):6 CPUCLKIN cycles

2:0 (000) : Reserved - write 0

Name: Bank 4/5 Type and Starting address (READ/WRITE)

Index	Bits	Values and Functions
14H	7:6	DRAM type block 2

00:Bank0/1 disabled
(01):256Kx1 or 256Kx4 DRAMs
10:1Mx1 or 1Mx4 DRAMs
11:4Mx1 or 4Mx4 DRAMs

5:0 (000000) : Starting address for Block 2

256K usage A$<26:21>$ (2MB per block, interleaved)
(2MB per block, non-interleaved)
1M   usage A$<26:23>$ (8MB per block)
(8MB per block, non-interleaved)
4M   usage A$<26:25>$ (32MB per block)
(32MB per block, non-interleaved)

Name: Bank 4/5 RAM timing (READ/WRITE)

Index	Bits	Values and Functions

15H   7:5   (000) : Reserved - Write 000

        4:3   RAS percharge time RAS <4:5> non-interleaved
RAS <4> interleaved
00:3 CPUCLKIN cycles
01:4 CPUCLKIN cycles
10:5 CPUCLKIN cycles
(11):6 CPUCLKIN cycles

        2:0   (000) : Reserved - write 0

Name: Bank 6/7 Type and Starting address (READ/WRITE)

Index	Bits	Values and Functions

16H   7:6   DRAM type in Block 3
00:Block 3 disabled
(01):256Kx1 or 256Kx4 DRAMs
10:1Mx1 or 1Mx4 DRAMs
11:4Mx1 or 4Mx4 DRAMs

        5:0   Starting address for Block 3

            256K usage   A<26:21> (1MB per bank)
                                  (2MB per block, non-interleaved)
            1M   usage   A<26:23> (4MB per bank)
                                  (8MB per block, non-interleaved)
            4M   usage   A<26:25> (16MB per bank)
                                  (32MB per block, non-interleaved)

Name: Bank 6/7 RAM timing (READ/WRITE)

Index	Bits	Values and Functions
17H	7:5	(000) : Reserved - write 000
	4:3	RAS precharge time, RAS <6:7> non-interleaved, RAS <6> interleaved 00:3 CPUCLKIN cycles 01:4 CPUCLKIN cycles 10:5 CPUCLKIN cycles (11)6 CPUCLKIN cycles
	0	(0) : Reserved - write 0
	2:0	(000)

Name: Cache size (READ/WRITE)

Index	Bits	Values and Functions
18H	7:4	(0000) : Reserved
	3	Block 3 (Bank 6/7) (0) : Bank 6 populated only 1 : Banks 6 and 7 populated
	2	Block 2 (Bank 4/5) (0) : Bank 4 populated only (used for single bank and interleaved configurations) 1 : Banks 4 and 5 populated
	1	Block 1 (Bank 2/3) (0): Bank 2 populated only(used for single bank and interleaved configurations) 1. Banks 2 and 3 populated
	0	Block 0 (Bank 0/1) (0): Bank 0 populated only(used for single bank and interleaved configurations) 1: Banks 0 and Bank 1 populated

Name: Cache and tag test (READ/WRITE)

Index   Bits Values and Functions

19H   7   RAS compare test mode
              (0) : Disabled
              1 : Enabled

        6   Double CAS mode (2 or 4 CLK2 CAS)
              0 : Disabled
              (1) : Enabled

        5   RAS compare test mode
              (0) : Disabled
              1 : Enabled

        4   Early LDBEN
              (1) : LDBEN transitions high to low during
              first T2
              (0) : Normal

        3   Additional wait-states for all but consective
              write DRAM cycles
              (0) : 0 wait-state
              1 : 1 wait-state added

        2   Early MA signal release
              (0) : Enable
              1 : Disable

        1   Early CAS mode
              (0) : Disable
              1 : Enable

        0   Page Interleave Mode
              RAS 1,3,5,7 used as CASEN <0:3>
              (0) : Disable
              1 : Enable

Index   Bits Values and Functions

1AH   7   Read extra wait-state for page hit
              (0) : No extra wait-state
              1 : Add 1 wait-state

        6   Read page hit wait-state state selection
              (block 1). Note : Add one wait-state
              if non-pipeline mode is used.
              0 : 0 wait-state (pipeline mode)
              (1) :1 wait-state (pipeline mode)

        5:4   CAS low pulse width for READ RAS high Page
              Misses (block 1)
              00 : 3 CPUCLKIN cycles
              01 : 4 CPUCLKIN cycles
              10 : 3 CPUCLKIN cycles
              (11) : 6 CPUCLKIN cycles

        3   (0) : Reserved write 0

        2   Read page hit wait-state selection (block 2).
              Note : Add one wait-state if non-pipeline mode
              is used.
              0 : 0 wait-state (pipeline mode)
              (1) : 1 wait-state (pipeline mode)

        1:0   CAS low pulse width for READ RAS high or Page
              miss (block 2)
              00 : 3 CPUCLKIN cycles
              01 : 4 CPUCLKIN cycles
              10 : 5 CPUCLKIN cycles
              (11) : 6 CPUCLKIN cycles

Index   Bits   Values and Functions

1BH   7   7 CLK2 CAS pulse width
(0) : Normal
1 : 7 CLK CAS pulse width all banks

6   Read page hit wait-state (block 3) selection
Note : Add one wait-state if non-pipeline
mode is used.
0 : 0 wait-state (pipeline mode)
(1) :1 wait-state (pipeline mode)

5:4   CAS low pulse width for READ RAS high Page
Misses (block 3)
00 : 3 CPUCLKIN cycles
01 : 4 CPUCLKIN cycles
10 : 5 CPUCLKIN cycles
(11) : 6 CPUCLKIN cycles

3   (0) : Reserved write 0

2   Read page hit wait-state selection (block 2).
Note : Add one wait-state if non-pipeline mode
is used.
0 : 0 wait-state (pipeline mode)
(1) : 1 wait-state (pipeline mode)

1:0   CAS low pulse width for READ RAS high or Page
miss (block 2)
00 : 3 CPUCLKIN cycles
01 : 4 CPUCLKIN cycles
10 : 5 CPUCLKIN cycles
(11) : 6 CPUCLKIN cycles

Index	Bits	Values and Functions

1CH   7   Late, late mode for all blocks for write miss
and RAS High
0 : Normal CAS mode
(1): Late CAS mode (adds 1 wait-state to write
page miss write cycles)

   6   RAS to CAS delay section
0 : 2 CLK2 cycles
(1) : 3 CLK2 cycles

   5   Altermate RAS precharge values, defined by
registers 11,13,15,17 bits
<4:3> for Blocks A,B,C,D
0 : RAS precharge values = 3,4,5,6 CLK2s
(1) : RAS precharge values 4,6,6,6

   4   Force RAS high enable bit
(0) : Normal page mode operation
1 : Force RAS high after each cycle

   3   RAS active position
1 : Assert RAS at beginning of T1P/T2
(0) : Assert RAS in the middle of T1P/T2

   2:0   Interleave selection
(000) : non-interleave mode
001 : 2-waypage interleave; blocks 0 and 1
010 : 2-waypage interleave; blocks 2 and 3
011 : 2-waypage interleave; blocks 0 and 1
as well as banks 2 and 3 but separately
100 : 4-way page interleave; blocks 0,1,2 and 3
101-111 : Reserved combinations

Index   Bits Values and Functions

20H   7   Cache enable bit
              (0) : cache is disabled
              1 : cache is enabled

          6   Force Read miss cycle. This bit is used for
              initializing the data and tag SRAMs. When
              set to 1, all accesses are to DRAM, but the
              tag and data SRAMS are still updated for
              cacheable areas as if the cache is fully
              operating. Any block of 256KB (or size of the
              cache) consecutive locations are then read,
              followed by setting this bit to 0. The 256KB
              block used to initialize the tag must not be
              made non-cacheable afterward.
              (0) : No force read miss cycle (normal operation)
              1 : Forced read miss cycle enabled

          5   Freeze cache directory. A cache read miss will
              not cause a tag RAM update and change of data
              in the cache data RAM. Instead, a normal DRAM
              read operation will be performed. A cache write
              hit will update the cache data RAM.

          4   (0) : Reserved

          3   Refresh type selection
              0 : Hidden refresh
              (1) : AT style refresh

          2:0 (000) : Reserved

The following register controls the Ready
Timeout option. If any device accessed by
the CPU does not respond with -READY
within 128 clock cycles, the 83C351 AT
control logic will generate -READY itself.

Index Bits Values and Functions

26H   7:3   Reserved (See Volume IV: 82C356
              Peripheral Controller, Section
              2 : 356 Configuration Registers)

        2   -READY Timeout
              (0) : -READY Timeout disabled
              1 : -READY Timeout disabled
        1:0   Reserved (See Volume IV: 82C356
              Peripheral Controller, Section
              2 : 356 Configuration Registers)

Name: Parity error status register (READ/WRITE)

Index Bits Values and Functions

28H   7   Parity check enable
              (0):Parity check enabled (PEN is low)
              1:Parity is disabled (PEN is high)

        6:3   (0000): Reserved

        2:0   Parity error address bits A26:A24.   When a
              local parity error occurs the address A26-A24
              is latched into bits 2:0.   These bits are
              read only.

Name: Parity error address register (READ ONLY)

When a local parity error occurs address A23-A16 are
latched into this register.

Index   Bits Values and Functions

29   7:0   Parity error address bits A <24:A16>.
            When a local parity error occurs, the
            address A<26:16> is latched into this
            register. These bits are read only.

Name: Memory Enable Map 0-07FFFFH (READ/ WRITE)

Index   Bits Values and Functions

2AH   7   Ready Timeout Flag (R/W)
            (0): Default
            1 : RDY Timeout has occured

       6   CWE Pulse Width
            (0): Default
            1 : Increase PW by 3ns (TYP)

       5   Reserved
            (0) : Default
            1 : Write (1)

       4   Enables internal hidden refresh logic. Enable
            only if external work around is not present.
            (0) : Disabled : external work around present
            1 :   Enable

       3   SLODRD for 25 MHz Pipeline mode
            (0) : Default (non-pepeline mode)
            1 : Delay LBEN by 1/2 CLK2 for DRAM reads

       2   Reserved
            (0) : Default
            1 : Write (1)

       1   DMA Cycles
            (0) : Default
            1 : Drive A24-31 low for DMA cycles (HLDA1 active)

Name: Miscellaneous Control (READ/WRITE)

Index   Bits   Values and Functions

2BH   7   (0) : Reserved

         6   Enable port 92H
            (0):Disable port 92H
            1:Enable port 92H

       5:4   Ready generation for 387DX cycles
            (00):82C351 generates ready after 1 wait-state
            01:82C351 runs AT cycle for all NPX cycles
            10:82C351 does not generate ready at all
            11:Reserved

         3   Weitek Present bit (READ ONLY)
            1:Weitek coprocessor present
            (0):Weitek coprocessor not present

       2:1   (000) : Reserved

Name: Middle Boot Space RAM/ROM Configuration (READ/WRITE)

Index   Bits   Values and Functions

2CH   7   Type of 64KB RAM at 0FC0000H
            (0):64KB of RAM at 0FC0000H is R/W
            1:64KB of RAM at 0FC0000H is read only

         6   Type of 64KB RAM at 0FD0000H
            (0):64KB of RAM at 0FD0000H is R/W
            1:64KB of RAM at 0FD0000H is read only

— Continued —

5 Type of 64KB RAM at 0FE0000H
(O):64KB of RAM at 0FE0000H is R/W
1:64KB of RAM at 0FE0000H is read only

4 Type of 64KB RAM at 0FF0000H
(O):64KB of RAM at 0FF0000H is R/W
1:64KB of RAM at 0FF0000H is read only

3 Type of 64KB RAM at 0FC0000H
(O):64KB of RAM at 0FC0000H is disable
1:64KB of RAM at 0FC0000H is enable

2 Type of 64KB RAM at 0FD0000H
(O):64KB of RAM at 0FD0000H is disable
1:64KB of RAM at 0FD0000H is enable

1 Type of 64KB RAM at 0FE0000H
(O):64KB of RAM at 0FE0000H is disable
1:64KB of RAM at 0FEOOOOH is enable

0 Type of 64KB RAM at 0FE0000H
(O):64KB of RAM at oFEooooH is disable
1:64KB of RAM at 0FE0000H is enable

Name: DRAM timing control (READ/WRITE)

Index	Bits	Values and Functions

2FH 7:5 (000) : Reserved
4 Additional wait-state on consecutive cycles
(0):0 additional wait states
1: 1 additional wait-state

3 (0) Reserved write 0

2 Posted write wait-states. Determines the number
of wait-states for posted CPU write cycles. If
a posted write is already in progress wait-states
are added until the cycle is finished.
0 : zero wait-state posted writes
(1) : one wait-state posted writes

1 Posted DRAM write enable
0 : Enable posted writes
(1) : Disable posted writes

0 (0) : Reserved

Non cacheable blocks: the 82C351 provides programmable registers for defining a area of memory as non cacheable. For example the BIOS ROM area needs to be non cached. Four such areas can be declared non cacheable. The index registers 30 to 39 are used to set the starting address and the amount of memory for to be non cached. Block 0 to 3 are the four non cacheable blocks. Each block has three registers which define the starting address and the amount of memory. For example block 0 has register 30H, 31H and 38H. The register 31 contains the non cacheable size. The non cacheable size is 4K to 4MB.

Name: Block 0 Non-Cacheable address A23 to A16 (READ/WRITE)

Index   Bits Values and Functions

30H   7:0   (00000000) Block 0 Non-Cacheable address A23 to A16

Name: Block 0 Non-Cacheable address A15 to A12 and Size (READ/WRITE)

Index   Bits Values and Functions

31H   7:4   (0000) : Block 0 Non-Cacheable address A15 to A12
         3:0   Non-Cacheable Size
               (0000):Disabled
               0001:4KB
               0010:8KB
               0011:16KB
               0100:32KB
               0101:64KB
               0110:128KB
               0111:256KB
               1000:512KB
               1001:1MB
               1010:2MB
               1011:4MB

Name: Block 1 Non-Cacheable address A23 to A16 (READ/WRITE)

Index   Bits   Values and Functions

32H·   7:0   (00000000) : Block 1 Non-Cacheable address A23 to A16

Name: Block 1 Non-Cacheable address A15 to A12 and Size (READ/WRITE)

Index   Bits   Values and Functions

33H   7:4   (0000) : Block 1 Non-Cacheable address A15 to A12

    3:0   Non-Cacheable Size
      (0000):Disabled
      0001:4KB
      0010:8KB
      0011:16KB
      0100:32KB
      0101:64KB
      0110:128KB
      0111:256KB
      1000:512KB
      1001:1MB
      1010:2MB
      1011:4MB

Name: Block 2 Non-Cacheable address A23 to A16 (READ/WRITE)

Index   Bits   Values and Functions

34H   7:0   (00000000) : Block 2 Non-Cacheable address A23 to A16

Name: Block 2 Non-Cacheable address A15 to A12 and Size (READ/WRITE)

Index Bits Values and Functions
35H   7:4   (0000) : Block 2 Non-Cacheable address A15 to A12
        3:0   Non-Cacheable Size
            (0000):Disabled
            0001:4KB
            0010:8KB
            0011:16KB
            0100:32KB
            0101:64KB
            0110:128KB
            0111:256KB
            1000:512KB
            1001:1MB
            1010:2MB
            1011:4MB

Name: Block 3 Non-Cacheable address A23 to A16 (READ/WRITE)

Index Bits Values and Functions
36H   7:0   (00000000) : Block 3 Non-Cacheable address A23 to A16

Name: Block 3 Non-Cacheable address A15 to A12 and Size (READ/WRITE)

Index Bits Values and Functions
37H   7:4   (0000) : Block 3 Non-Cacheable address A15 to A12
        3:0   Non-Cacheable Size
            (0000):Disabled
            0001:4KB
            0010:8KB
            0011:16KB
            0100:32KB
            0101:64KB
            0110:128KB
            0111:256KB
            1000:512KB
            1001:1MB
            1010:2MB
            1011:4MB

Name: Non-Cacheable address A26 to A24
      (READ/WRITE)

Index   Bits   Values and Functions

38H   7:6   (00) : Reserved

        5:3   (000) : Block 1 Non-Cacheable address A26 to A24

        2:0   (000) : Block 0 Non-Cacheable address A26 to A24

Name: Non-Cacheable address A26 to A24 to A12
      (READ/WRITE)

Index   Bits   Values and Functions

39H   7:6   (00) : Reserved

        5:3   (000) : Block 3 Non-Cacheable address A26 to A24

        2:0   (000) : Block 2 Non-Cacheable address A26 to A24

Index   Bits   Values and Functions

60H   7:6   (00) : Reserved

        5   Alemate CPU reset. A low to high
              transition activates a CPU reset
              (RESET3)

        4:0   (00000) : Reserved

Name: Fast Reset Control Register

Direct Port   Bits Values and Functions
Access

       92H   7:2 (000000) Reserved

              1   Fast GATE A20
                   (0) : Force CPU A20 low
                   (1) : Enable CPU A20

              0   (1) : Enable CPU reset
                   (0) : A 0 to 1 transition causes a CPU reset

Note : This port is used by OS2 and is disabled by writing a 0
to register 2B bit 6.

6. Trouble Shooting

The simple inspection methods for end user

Situation	Solution
No screen No light for "Power LED" No fan	*Ensure your computer plug on and the power under the normal condition. *Ensure the connector of computer back site without unconnecting.
No screen No light for "Power LED" Have voice of fan	*Ensure power on the monitor and adjust to appropriate light of screen to avoid too dark to identfy signal.
Disability of booting for floppy disk & hard disk	*Confirm disk can be booted the "DOS". *Make sure disk is clean. *Make disk has been inserted at right site.
No way to key-in	*Please examine the power code of keyboard if connected with the printer. Besides, nothing put upon the keyboard while trun on to avoid misdiagnosis of keyboard status.
For new equipment installation	*Please contact with your local agency if you want to move the computer or add any new equipments.