Advance Information

This document contains information on a product under development. The parametric information contains target parameters that are subject to change.

BtV2115

MediaStream Controller

Applications

- Microsoft Windows™ 3.1, Win '95™, and NT™ GUI acceleration
- IBM OS/2™ GUI acceleration
- Xwindow System™ acceleration
- Video for Windows™ and Microsoft Windows MPC Audio™
- High Resolution Color Graphics
- Video-conferencing
- Multimedia Applications
- Video Playback Acceleration

Related Products

- BtV2487 PACDAC
- BtV2811 VideoStream Decoder
- BtV2300 AudioStream Interface

Distinguishing Features

- Local Bus Graphics Controller (glueless for):
  – PCI 2.0 bus
  – VESA VL 2.0 bus (32 bit)
- 32 bit VRAM (1MB to 4MB)
  – Samsung™ 256Kx8: -8,-7,-6 128Kx16:-8,-7,-6
  – Texas Instruments™ 256Kx16:-8,-7,-6
  – NEC™, Toshiba™, IBM™ 256Kx16:-8,-7,-6
- Up to 1MB of Flash ROM
- Supports Yamaha OPL2,3,4
- Resolutions:
  – 640x480: 4, 8, 16, 24, 32 b/pixel up to 76 Hz
  – 800x600: 4, 8, 16, 32 b/pixel up to 76 Hz
  – 1024x768: 4, 8, 16, 24 b/pixel up to 75 Hz
  – 1280x1024: 4, 8, 16 b/pixel up to 75 Hz
  – 1600x1280 interlaced: 4, 8 b/pixel 45/90 Hz
- VGA compatibility for modes 0x00 - 0x07 and 0x0D - 0x13
- Multimedia Solution
  – Glueless connectionBtV2811 VideoStream Decoder
  – Acceleration of two video planes with hardware double buffering
  – Hardware-accelerated video playback
  – Stereo audio in/out
  – Software encoded NTSC/PAL video out to VCR
  – MPEG raster-block assist
  – Stretch Blt and raster scaling
  – Legacy AudioPro™ compatibility
  – Digital Interface to consumer digital audio tape, minidisc, etc.
- Standard Interfaces
  – PCI bus 2.0 compliant
  – VESA VL bus 2.0
  – AES/EBU S/PDIF CP-340 (with full access to channel/user bits)
  – I^2C/ ACCESS.bus
  – VESA DDC1, DDC2A/B
  – VESA DPMS
- 208 pin Power Quad package

Functional Block Diagram

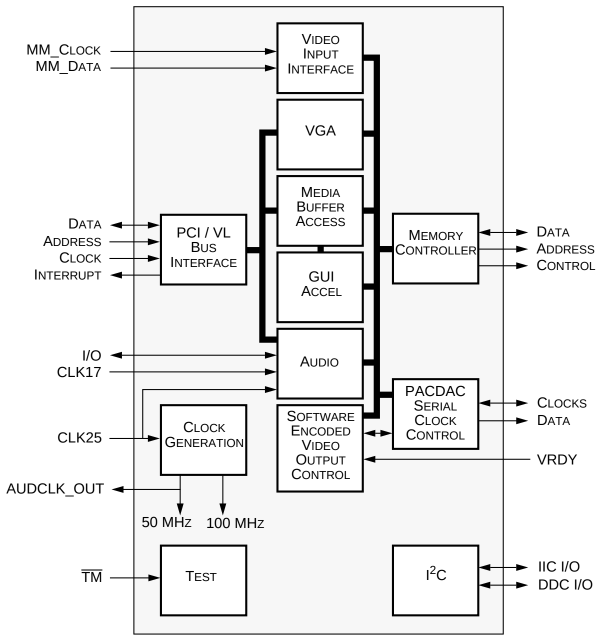

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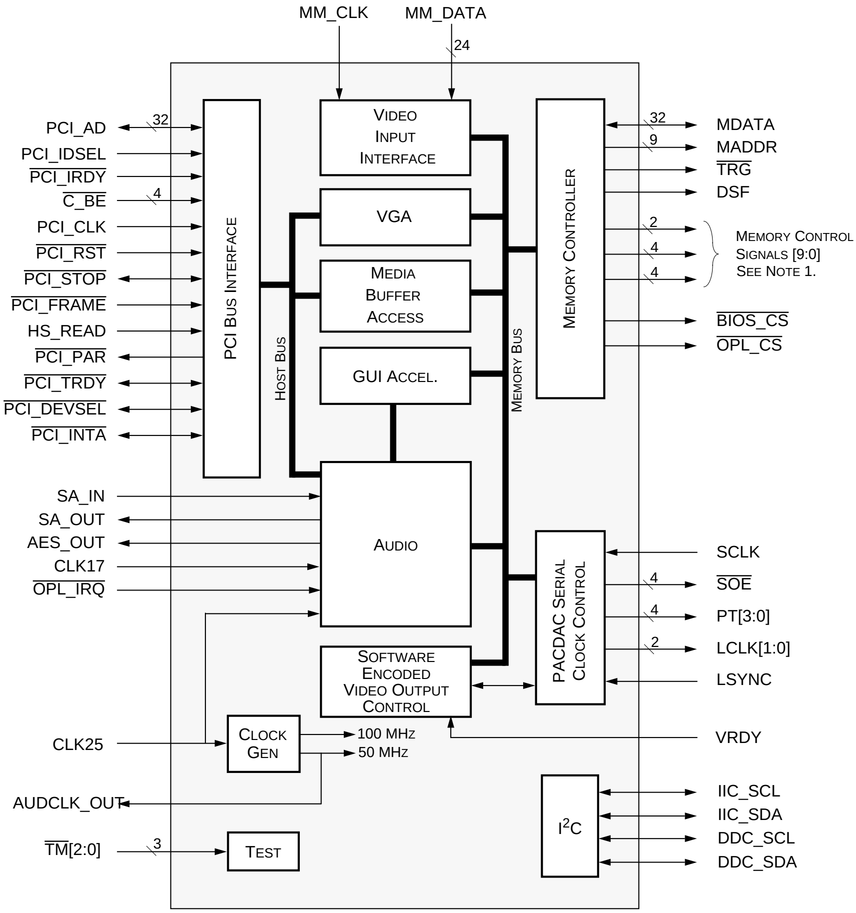
Figure 3. BtV2115 PCI-Bus Block Diagram



Note 1. Refer to Table 2 on page 17, column “VRAM Interface Pins” for details on the RAS, WE, and CAS memory control pins.