BE-M1000 Microprocessor
Datasheet

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1 Introduction

The BE-M1000 is a general purpose *System-on-a-Chip* (**SoC**) for computing systems, such as personal computers, microservers, networking equipment, multimedia and software-defined hardware, embedded systems and controllers that require high performance and low power consumption.

The SoC features eight Arm® Cortex™-A57 cores that operate at 1500 MHz and support the coherent caches L1, L2, and L3.

The video subsystem includes two video controllers (LVDS and HDMI), and a 4K video decoder. Arm® Mali™-T628 graphics coprocessor contains eight shader cores.

The SoC contains two DDR3/4 memory controllers and a wide range of peripheral interfaces: PCIe Gen3, 10 Gb Ethernet, 1 Gb Ethernet, USB 3.0, USB 2.0, SATA 6G, eMMC/SD, I^{2}S, SPI, UART, I^{2}C, GPIO, etc.

The SoC complies with Arm® TrustZone® technology and contains the capabilities necessary to build trusted systems.

1.1 Main Features

Table 1-1 Main Features

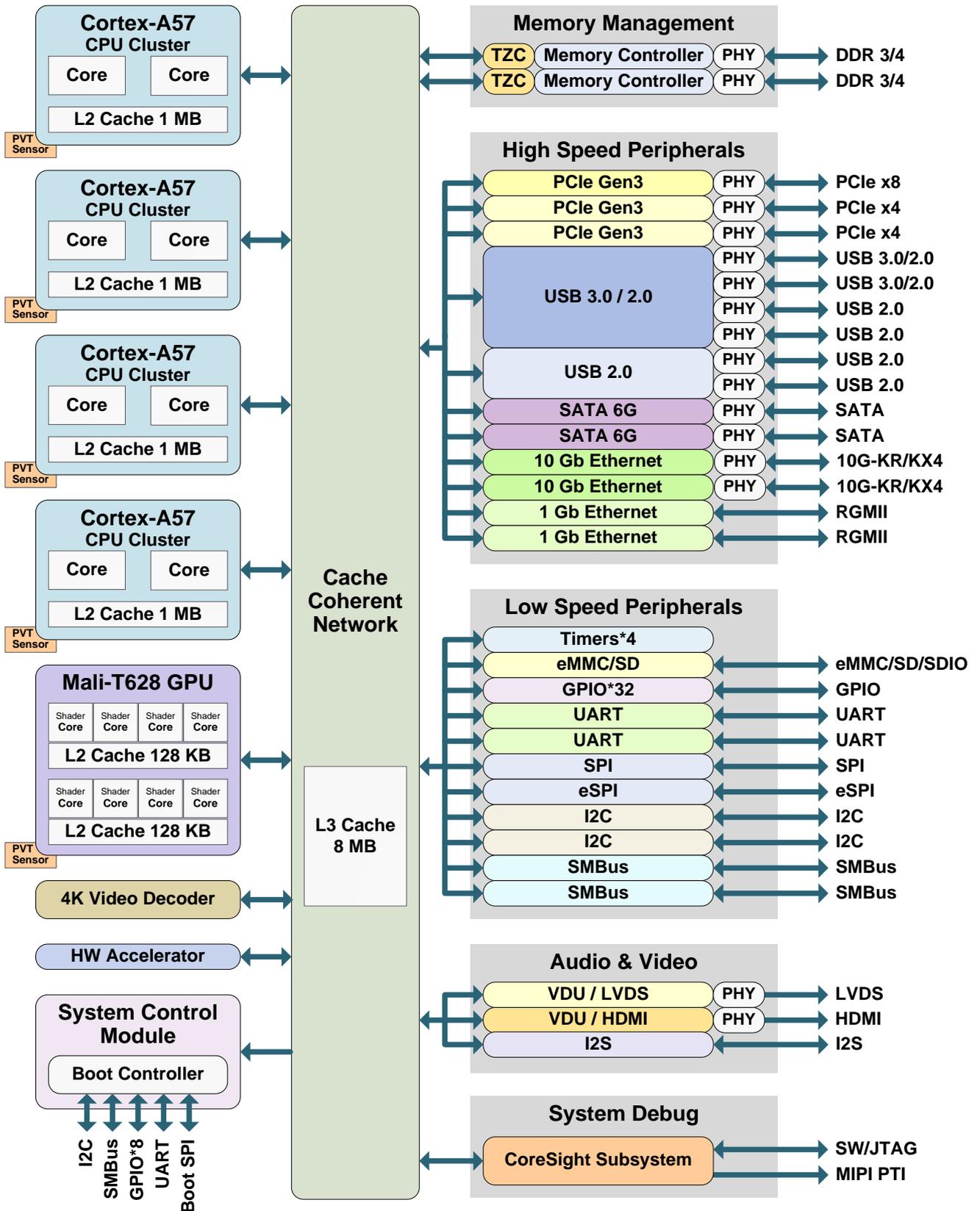| Feature	Description
Armv8-A Architecture	Four Arm Cortex-A57 clusters operating at 1500 MHz
	Two cores and 1 MB L2 cache in a cluster
Graphics Processing Unit	Arm Mali-T628 *graphics processing unit* (**GPU**) with 8 shader cores (two quad-core clusters) operating at 500 MHz
	128 KB L2 cache in a cluster
PVT Monitoring	Five *process, voltage and temperature* (**PVT**) sensors to monitor processes, voltage and temperature in Cortex clusters and GPU
L3 Cache	*Cache Coherent Network* (**CCN**) with 8 MB L3 cache memory
External Memory Interface	Two 64-bit *Dynamic Random Access Memory* (**DRAM**) interfaces with support of DDR4-2400/DDR3-1600 and *error correction code* (**ECC**)
High Speed Peripheral Interfaces	Three *PCI Express* (**PCIe**) Gen3: one PCIe x8 and two PCIe x4
	Two *Universal Serial Bus* (**USB**) 3.0/2.0 ports, four USB 2.0 ports
	Two *Serial ATA* (**SATA**) 6G
	Two 10 Gb Ethernet (10GBASE-KX4, 10GBASE-KR)
	Two 1 Gb Ethernet RGMII
Low Speed Peripheral Interfaces	*Embedded Multimedia Card* (**eMMC**)/*Secure Digital* (**SD**)/*Secure Data Input/Output* (**SDIO**)
	Four peripheral timers
	General Purpose I/O 32-bit (**GPIO*32**)
	Two *Universal Asynchronous Receiver-Transmitters* (**UARTs**)
	Serial Peripheral Interface (**SPI**)
	Enhanced Serial Peripheral Interface (**eSPI**)
	Two *Inter-Integrated Circuits* (**I²Cs**)
	Two *System Management Bus* (**SMBus**)
Multimedia	Video Controller with *low-voltage differential signaling* (**LVDS**) interface
	Video Controller with *high definition* (**HD**) display interface *HD Multimeda Interface* (**HDMI**) 2.0
	4K Video Decoder
	Inter-IC sound (**I²S**) interface
Security	Arm TrustZone architecture
	TrustZone Controller (**TZC**)
	Secure boot
System debug	Arm® CoreSight™ debug and trace architecture
Package	FCBGA-1521 40x40 mm, 1 mm pitch, 1521 pins
Power consumption	28.5 W max
Technology	CMOS 28 nm

1.2 Block Diagram

Figure 1-1 Block Diagram

2 Module List

Table 2-1 Module List

Module name	Brief description
Arm Cortex-A57 *Central Processing Unit* (**CPU**) Cluster	The SoC contains four Arm Cortex-A57 dual-core CPU clusters (8 cores in total). The Cortex-A57 cluster is a high-performance, low-power device that implements the Armv8-A architecture. Each cluster has two cores (1500 MHz) and L2 (1 MB) cache. Each core has 48 KB L1 instruction cache and 32 KB L1 data cache. A core can operate in one of two possible states, known as the Secure and Non-secure. By propagating the security state of the core through the on-chip interconnect to target based transaction filters, the TrustZone technology is extended into the SoC architecture, creating a robust platform supporting fully isolated Trusted and Non-trusted worlds.
DDR3/4 Memory Controller	The SoC contains two DDR memory control subsystems. The integration of the DDR3/4 controller and DDR PHY creates a complete solution for connecting the SoC to DDR memory devices of the following types: • 64/32-bit DDR3 (speed grades up to DDR3-1600) • 64/32-bit DDR4 (speed grades up to DDR4-2400) Each DDR memory control subsystem supports the following features: • Up to 64 GB physical memory • Up to 4 memory ranks • ECC: *single error correction*/*double error detection* (**SEC**/**DED**) • 1:2 frequency ratio mode • DDR3U and DDR3L, DDR4U and DDR4L • Industry standard UDIMMs and RDIMMs • Low area, low power architecture • Programmable support for 1T/2T memory command timing • Software programmable *quality of service* (**QoS**) • Automatic DDR3/4 low power mode operation DDR memory control subsystem is combined in the SoC with TrustZone controllers to provide capabilities for building trusted systems.

Table 2-1 Module List (continued)

Module name	Brief description
L3 CCN	Based on the Arm® CoreLink™ CCN-504, this module provides interconnection of the main SoC subsystems and manages the Level 3 cache for these subsystems. High-performance distributed system cache, 8 MB in capacity, includes an integrated *point-of-serialization* (**PoS**) and *point-of-coherency* (**PoC**) and can be used both for compute and *input/output* (**I/O**) caching. The CCN provides the following key features: - Dual simplex ring-bus interconnect topology - One 128-bit, dual simplex data channel - Broadcast snoop channel - DVM message transport between masters - QoS regulation for shaping traffic profiles - Monitoring performance-related events - Error signal gathering using an error bus, with a single point of interrupt coordination on errors - Separate caches for secure and non-secure transactions
Mali-T628 GPU	Provides a complete graphics acceleration platform based on open standards. It supports 2D graphics, 3D graphics, and *general purpose computing on GPU* (**GPGPU**). The graphics processor provides the following main features: - Two clusters - shader cores operating at 500 MHz in a cluster 128KB L2 Cache in a cluster - Seamless load balancing across active shader cores - ETC2, EAC1, ETC2-EAC compressed formats are supported - The following APIs are supported: - OpenGL ES 1.1, 2.0, 3.0, 3.1 - OpenCL 1.1 - RenderScript *Full scene anti-aliasing* (4x**FSAA**, 16x**FSAA**) with minimal performance drop *Adaptive scalable texture compression* (**ASTC**): l*ow dynamic range* (**LDR**) and *high dynamic range* (**HDR**) are supported - Native hardware support for 64-bit scalar and vector, integer and floating-point data types—fundamental to accelerate complex and computationally intensive algorithms It can work both in secure and non-secure modes.

Table 2-1 Module List (continued)

Module name	Brief description

System Control Module	This module is used to manage all the SoC subsystems.
	
	It contains the following main blocks:
	
	• System control processor that runs service functions such as:
	  o Starts the SoC
	  o Uses the boot controller for initial boot of the SoC
	  o Provides the initial configuration of all the SoC modules
	  o Monitors the state of the SoC by polling the built-in PVT sensors
	
	• Boot controller that contains dedicated SPI, I^{2}C, SMBus, UART, and GPIO*8 interfaces (unaccessible for Cortex-A57 cores) for initial boot of the SoC
	
	• Clock Management Unit that controls system clock and reset signals

PCIe Gen 3.0	The SoC contains three PCIe interfaces: two PCIe x4 and one PCIe x8.
	
	Each PCIe contains PCIe Root Complex controller that provides base PCIe functionality in accordance with the ***PCI Express Base Specification 3.0***.
	
	Each PCIe provides the following main features:
	
	• Transfer rates up to 8.0 GT/s (~1GB/s) per single lane
	• PCIe *active state power management* (**ASPM**)
	• PCIe *advanced error reporting* (**AER**) with Multiple Header Logging
	• Internal Address Translation Unit
	• Embedded multichannel DMA controller
	• Automatic Lane Reversal
	• ECRC Generation and Checking
	• Maximum Payload Size:
	  o 256 bytes for PCIe x4
	  o 512 bytes for PCIe x8
	• 1 Virtual Channel for PCIe x4, 2 Virtual Channels for PCIe x8
	
	Each PCIe can work both in secure and non-secure modes.

4K video decoder (**4KDec**)	Used to decode video streams encoded in the following formats: • H.265 (HEVC): up to 4096x2304 at 30 fps • H.264, MPEG4, MPEG2, VP8, VP6, VC1, AVS, RealVideo, and JPEG: up to 1080p at 60 fps The 4KDec loads the encoded video data from the system memory, decodes it and places the information ready to be sent to the video display unit into the frame buffer. It can work both in secure and non-secure modes.

Table 2-1 Module List (continued)

Module name	Brief description
Hardware accelerator (**HWA**)	Designed to improve the performance of computing, the HWA consists of hardware modules, which implement special algorithms of data processing.
USB 3.0/2.0	The module provides two USB 3.0 interfaces and two USB 2.0 interfaces. The USB 3.0/2.0 is compatible with the xHCI specification by Intel Corporation. It is optimized for the Super-Speed applications and systems and supports the following device types: • Super-Speed devices via USB 3.0 interface (4 Gbps IN and 4 Gbps OUT) • High-Speed, Full-Speed, and Low-Speed devices via any interface The interface contains multiple bus instances to support concurrent USB 3.0/2.0 transfers on each port. Therefore in the current configuration (four bus instances for two SS ports and two HS ports), the controller net throughput is 9.92 Gbps (2 * 4 Gbps+ 2* 480 Mbps IN and 2 * 4 Gbps+ 2* 480 Mbps OUT). This interface is targeted to the next generation of media storage, creation, and playback devices requiring high bandwidth for faster "sync-and-go" functionality between PCs and portable electronic devices, such as flash drives, solid state drives, camcorders, portable media players, and smartphones. Each USB 3.0/2.0 can work both in secure and non-secure modes.
USB 2.0	The module provides two USB 2.0 interfaces. The USB 2.0 is compatible with the xHCI specification by Intel Corporation. It is optimized for the high-bandwidth applications and systems and supports the following device types: • High-Speed (480 Mbps) • Full-Speed (12 Mbps) • Low-Speed (1.5 Mbps) Each USB 2.0 can work both in secure and non-secure modes.

Table 2-1 Module List (continued)

Module name	Brief description
SATA 6G	There are two 1-port SATA interfaces in the SoC. The SATA supports the following features: • SATA 6.0 Gb/s speeds • eSATA (external analog logic also needs to support eSATA) • Compliant with Serial ATA 3.2 and AHCI Revision 1.3 specifications • 8b/10b encoding/decoding • *Error correction code* (**ECC**) • Power management features including automatic partial-to-slumber transition • *Built-in self-test* (**BIST**) loopback modes • Internal DMA engine per port Each SATA can work both in secure and non-secure modes.
10 Gigabit Ethernet media access controller (**XGMAC**) with integrated *10 Gigabit Ethernet physical coding sublayer* (**XPCS**)	There are two XGMACs in the SoC. The XGMAC enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2008 standard for two types of 10 Gb/s Ethernet: 10GBASE-KX4 and 10GBASE-KR. The XGMAC has the following main features: • Full-duplex operation at 10 Gbps • Full compliance with Clause 71 (10GBASE-KX4) and Clause 72 (10GBASE-KR) of the IEEE 802.3-2008 standard • Full compliance with Clause 78 (*Energy Efficient Ethernet* (**EEE**) feature) of the IEEE 802.3az, standard for 10 Gbps operation • Programmable frame length, supporting standard or jumbo (extendable to 16 KB) Ethernet frames • Support for VLAN-tagged frame processing in compliance with the IEEE 802.1Q standard Each XGMAC can work both in secure and non-secure modes.
1 Gigabit media access controller (**GMAC**)	There are two GMACs in the SoC. The controller enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2008 standard. It has the following main features: • 10, 100, and 1000 Mbps data transfer rates with RGMII interface to communicate with an external gigabit PHY • Full-duplex operation support • Half-duplex operation support • Embedded DMA controller with independent Transmit and Receive engines Each GMAC can work both in secure and non-secure modes.

Table 2-1 Module List (continued)

Module name	Brief description
eMMC/SD/SDIO	Provides communication with memory cards targeted for the mobile/portable market and adheres to the SD UHS-I and eMMC specifications. The eMMC/SD supports the following features: • SD memory and SDIO digital interface protocol, and compliant with SD HCI specification • eMMC protocols including eMMC 5.1 • SD-HCI Host version 4 mode or less • Embedded DMA controller • Software tuning in SD UHS-I and eMMC modes
Peripheral Timers*4	The module contains four independent peripheral timers. Each peripheral timer is a 32-bit programmable timer supported "free-running" and "user-defined count" modes. In "user-defined count" mode, a timer counts down from a programmed value and generates an interrupt when the count reaches zero. Timer interrupt can be detected even when the system bus clock is stopped.
GPIO*32	Implements run-time 32-bit programmable interface for external communications. The GPIO controls the output data and direction of external I/O pads. It also can read back the data on external pads using memory-mapped registers. The interface contains 32 individually controllable signals in a single port.
UART	There are two UARTs in the SoC. The UART is programmable component that is used for serial communication with: • Peripherals • Data carrier equipment (for example, modems) • Data sets Each UART has a handshaking interface with the *DMA controller for low speed peripherals* (**DMA LSP**) that can request and control non-secure data transfers between the UART and memory. Data is written from a master (application processor or DMA controller for low speed peripherals) to the UART, and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master to read back. The UART contains registers that control: • Character length • Baud rates up to 1.5 M baud • Parity generation/checking • Interrupt generation

Table 2-1 Module List (continued)

Module name	Brief description
SPI	The SPI is a full-duplex master or slave-synchronous serial interface used for short distance communication. It has a handshaking interface with the DMA LSP that can request and control data transfers between the SPI and memory. A master (application processor or the DMA LSP) accesses data, control, and status information on the SPI through the APB interface. The SPI operates as a serial master. It can connect to a serial-slave peripheral device using Motorola SPI interface.
eSPI	The eSPI is a synchronous serial communication interface used for short distance communication. Additional eSPI signals in compare to SPI Interface: • `RESET` programmable as input or output • `ALERT` input interrupts eSPI device communicates in full-duplex mode using master-slave architecture with up to eight external slave SPI devices (SSx8). It supports Single/Dual/Quad SPI mode of operation.

I^2C	There are two general purpose I^2Cs in the SoC.
	
	 I^2C is a programmable serial interface that provides support for the communications link between the devices connected to the bus.
	
	 The I^2C support the following features:
	
	 • Three speeds:
	     o Standard mode (0 to 100 Kb/s)
	     o Fast mode (≤ 400 Kb/s) or fast mode plus (≤ 1000 Kb/s)
	     o High-speed mode (≤ 3.4 Mb/s)
	 • Master OR slave I^2C operation
	 • 7- or 10-bit addressing
	 • 7- or 10-bit combined format transfers
	
	 Each I^2C has a handshaking interface with the DMA LSP that can request and control non-secure data transfers between the I^2C and memory.

SMBus	The SoC includes two SMBus interfaces. This interface provides a two-wire bidirectional interface for transfer of bytes of information between multiple compliant I^2C devices, typically with a microprocessor behind the DB-I^2C master/slave controller and one or more master/slave devices.

Table 2-1 Module List (continued)

Module name	Brief description
Video display unit (**VDU**) with quad LVDS output interface	It is a general purpose display controller used to drive a wide range of display devices varying in size and capability. The module provides the following main features: • Wide range of programmable LCD Panel resolutions up to 4096x4096 • Color resolution of up to 24 bpp • 4-lane LVDS output interface • Embedded DMA Controller • Programmable vertical and horizontal timing parameters • Hardware cursor • Two overlay windows in addition to the base screen

VDU integrated with HDMI 2.0	Provides a complete HDMI interface for transmitting video and audio data to an HDMI-compliant source device, such as a computer monitor, video projector, digital television, or digital audio device.
	
	The subsystem has the following main features:
	
	• VDU features:
	    o Wide range of programmable LCD Panel resolutions up to 4096x4096
	    o Color resolution of up to 24 bpp
	    o Embedded DMA Controller
	    o Programmable vertical and horizontal timing parameters
	    o Hardware cursor
	    o Two overlay windows in addition to the base screen
	• Three TMDS data channels with 6 Gbps data rate per channel
	• Total maximum throughput of up to 18 Gbps (6 Gbps * 3 channels)
	• HDMI 2.0 specification features:
	    o All CEA-861-F video formats
	    o *Dynamic range and mastering infoframe* (**DRM**)
	• Embedded DMA Controller for Audio
	• Audio stream bit rate up to 24.576 Mbps
	• It can work both in secure and non-secure modes

Table 2-1 Module List (continued)

Module name	Brief description
I^{2}S	I^{2}S is a programmable module used for the serial communication with peripherals. It is designed to be used in systems that process digital audio signals, such as: • A/D and D/A converters • Digital signal processors • Error correction for compact disc and digital recording • Digital filters • Digital input/output interfaces
CoreSight Subsystem (further **CoreSight**)	Provides a standard implementation of the Arm Debug Interface for debug tools to work with: • Serial Wire or JTAG Debug Port • Trace Port Interface The subsystem supports the following methods of debugging the SoC: • "External" debug—conventional debug through the SW/JTAG interface • "Self-hosted" debug—conventional debug with the processor running using a debug monitor that resides in memory • Logging of hardware and software events in a trace, which is recorded in memory as well as transmitted through the *trace port interface* (**MIPI PTI**) to an external debug system It can work both in secure and non-secure modes.
DMA LSP	Implements capability of direct data transfer between a low speed device, which is connected to an UART, SPI, or I^{2}C, and memory without CPU usage. It helps in maximizing system performance by decreasing a load of the SoC cores. The DMA controller can only work in non-secure mode and has the following main features: • 8 channels, one per source and destination pair • Unidirectional channels—data transfers in one direction only • Multi-block transfers • Single FIFO per channel for source and destination • Automatic data packing or unpacking to fit FIFO width
DMA Controller for MEM2MEM Transfers	Provides direct data transfer between memory blocks of interacting subsystems without CPU usage. It implements TrustZone secure technology with one APB interface operating in the Secure state and the other operating in the Non-secure state. Dual APB interfaces enable the operation of the DMA to be partitioned into the Secure state and Non-secure state.

Table 2-1 Module List (continued)

Module name	Brief description
TZC	There are two TZCs in the SoC. A TZC is placed on the path to each DDR controller to implement memory access restrictions according to Arm TrustZone technology. To provide security address region control functions required for intended application, a TZC includes Control and Filter units. The TZC Control Unit contains programmable registers to configure a table of rules defining access restrictions for 8 continuous memory regions, particularly specifying if the memory region can be accessible in a specific mode—secure or non-secure. All the memory requests received by the controller are passed through the Filter Unit determining whether the requested address can be accessed by the current transaction, depending on its state—secure or non-secure. Also, memory access in non-secure mode can be restricted based on the source of the transaction—module that initiated the transaction.

PVT Sensor	The SoC contains five PVT sensors that are designed to monitor process, voltage and temperature variation in the Cortex-A57 clusters and Mali-T628 GPU.
	
	Each PVT sensor provides the following features:
	
	• Measured PVT values:
	    o Temperature
	    o Voltage
	    o Low-Vt (**LVT**) process
	    o Standard-Vt (**SVT**) process
	    o High-Vt (**HVT**) process
	
	• Measurement readiness is determined by polling data register or listening the interrupt line
	
	• Programmable upper and lower threshold values for the measured PVT parameters to produce out-of-range interrupts
	
	• Programmable timeout value for repetitive PVT parameters monitoring

3 Electrical Specifications

NOTE: The electrical characteristics are subject to change and clarification without extra notification

3.1 Power Supply Parameters

BE-M1000 requires six isolated voltage supplies and single unified ground supply as shown in the following table.

Table 3-1 BE-M1000 Power Domains

Supply Type	Package Pin Name	Voltage, V	Max Power, W
Core supply	VDD		
0.95V voltage supply	VDD_HDMI_09 VDD_USB2_09 VDD_USB3_0_09 VDD_USB3_1_09 VDD_USB3TX_0_09 VDD_USB3TX_1_09 VDD_USB3_VP_0_09 VDD_USB3_VP_1_09 VDD_PCIE4_0_09 VDD_PCIE4_1_09 VDD_PCIE8_09 VDD_SATA_09 VDD_SATATX_09 VDD_XG0_09 VDD_XG1_09	0.95 ± 5%	23
PLL supply	VDDPLL_0_09 VDDPLL_1_09 VDDPLL_2_09 VDDPLL_3_09 VDDPLL_HDMI_09	0.9 ± 10%	0.17
DDR supply	VDDQ_DDR0, VDDQ_DDR1	DDR3: 1.5 ± 5% DDR4: 1.2 ± 5%	3.0
1.5V voltage supply	VDD_PCIE4_0_15 VDD_PCIE4_1_15 VDD_PCIE8_15 VDD_XG0_15 VDD_XG1_15	1.5 ± 5%	1.0

Table 3-1 BE-M1000 Power Domains (continued)

Supply Type	Package Pin Name	Voltage, V	Max Power, W
1.8V voltage supply	VDD_DDR0_PLL VDD_DDR1_PLL VDD_HDMI_18 VDD_PVT_18 VDD_SATA_18 VDD_USB2_18 VDDIO	1.8 ± 10%	0.6
3.3V voltage supply	VDD_SD_33 VDD_USB2_0_33 VDD_USB2_1_33 VDD_USB2_2_33 VDD_USB2_3_33 VDD_USB3_33	3.3 -6.9% +4.8%	0.7
Ground	VSS	-	-
Total			**~28.47 W**

3.2   External Clocking

3.2.1 Reference Clock Signals

Table 3-2 Reference Clock Signals

Clock Signal	Pin Names	Frequency	Notes
Reference clock	CLK25M	25 MHz	-
XGbE PHY reference clock	XG0_REF_CLKN XG0_REF_CLKP XG1_REF_CLKN XG1_REF_CLKP	156.25 MHz	Diff. pair
PCIe PHY reference clock	PCIE4_0_REF_CLKN PCIE4_0_REF_CLKP PCIE4_1_REF_CLKN PCIE4_1_REF_CLKP PCIE8_REF_CLKN PCIE8_REF_CLKP	100 MHz	Diff. pair
SATA PHY reference clock	SATA_REFCLKP SATA_REFCLKM	100 MHz	Diff. pair

Table 3-2 Reference Clock Signals (continued)

Clock Signal	Pin Names	Frequency	Notes
USB3 PHY optional reference clock input	USB3_0_REFCLKN USB3_0_REFCLKP USB3_1_REFCLKN USB3_1_REFCLKP	100 MHz (typical)	Diff. pair
USB2 PHY: XI - crystal oscillator XO - crystal oscillator or board reference clock input	USB2_0_XI USB2_0_XO USB2_1_XI USB2_1_XO USB2_2_XI USB2_2_XO USB2_3_XI USB2_3_XO	50 MHz	
HDMI PLL reference clock input	HDMI_PLL_27M	27 MHz	
LVDS PLL reference clock input	LVDS_PLL_27M	27 MHz	

3.2.2 Reference Clock Requirements

3.2.2.1 Reference Clock (CLK25M)

Table 3-3 Reference Clock (CLK25M) Requirements

Parameter	Min	Typ	Max	Unit
Frequency range		25		MHz
Reference clock frequency offset	-50		50	ppm
Reference clock random jitter (RMS)		10		ps
Reference clock cycle to cycle jitter		6		ps
Startup time		1.5	3.0	ms
Disable time		20	100	ns
Disable Stand-by current			15	uA

3.2.2.2 SATA PHY Reference Clock

Table 3-4 SATA PHY Reference Clock Requirements

Parameter	Min	Typ	Max	Unit	Conditions
Frequency range		100		MHz	
Reference clock frequency offset	-350		350	ppm	

Table 3-4 SATA PHY Reference Clock Requirements (continued)

Parameter	Min	Typ	Max	Unit	Conditions
Reference clock random jitter (RMS)			3	ps	1.5 MHz to Nyquist frequency. For example, for 100 MHz reference clock, the Nyquist frequency is 50 MHz
Reference clock cycle to cycle jitter			150	ps	DJ across all frequencies
Duty cycle	40		60	%	
Common mode input level	0		vp	V	Differential inputs
Differential input swing	0.3			Vpp	Differential inputs[1]
Single-ended input logic low	-0.3		0.3	V	If single-ended input is used
Single- ended input logic high	vp-0.3		vp+0.3	V	If single-ended input is used
Input edge rate	0.6			V/ns	
Reference clock skew (±)			200	ps	

3.2.2.3 XGbE PHY Reference Clock

The PHY supports a differential reference clock source. The source may be driven through either external pads or internal pins. The chosen reference clock must meet specific requirements for signal swing and jitter. The following table summarizes the requirements of the reference clock provided to the PHY.

Table 3-5 XGbE PHY Reference Clock Requirements

Parameter	Min	Typ	Max	Unit	Conditions
Frequency range		156.25		MHz	
Frequency stability	-100		100	ppm	
Differential input swing	300		1890	mVppd	
Duty cycle	40		60	%	
Input edge rate	0.6			V/ns	
Coupling					AC coupling
Allowed jitter for 10GBASE-KR and slower			2.25	ps (rms)	Integrated from 12kHz to 20MHz
Allowed jitter for CEI-6G-SR, 10GBASE-KX4, XAUI			3.6	ps (rms)	Integrated from 12kHz to 20MHz
Peak to peak period jitter of the reference clock			20	ps	Period jitter measured over 10k samples

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[1] VDREF_CLK / 4 + VCMREF_CLK ≤ vp + diode forward-biasing voltage and VCMREF_CLK- VDREF_CLK/4 ≥ - diode forward biasing voltage

Table 3-5 XGbE PHY Reference Clock Requirements (continued)

Parameter	Min	Typ	Max	Unit	Conditions
Phase jitter			2	ps	Integrated from 1.5 MHz to Nyquist frequency. For example, for 100 MHz reference clock, the Nyquist frequency is 50 MHz

3.2.2.4 PCIe PHY Reference Clock

Table 3-6 PCIE PHY Reference Clock Requirements

Parameter	Min	Typ	Max	Unit	Conditions
Frequency range		100		MHz	
Frequency stability	-300		300	ppm	
Differential input swing	300		1890	mVppd	
Duty cycle	40		60	%	
Input edge rate	0.6			V/ns	
Coupling					AC coupling
Allowed jitter for 10GBASE-KR and slower			2.25	ps (rms)	Integrated from 12kHz to 20MHz
Allowed jitter for CEI-6G-SR, 10GBASE-KX4, XAUI			3.6	ps (rms)	Integrated from 12kHz to 20MHz
Peak to peak period jitter of the reference clock			20	ps	Period jitter measured over 10k samples
Phase jitter			2	ps	Integrated from 1.5 MHz to Nyquist frequency. For example, for 100 MHz reference clock, the Nyquist frequency is 50 MHz

NOTE: 100 MHz is the only PCIe standard compliant refclk frequency. When using a 125 MHz refclk, the PHY may not be compliant to all PCIe specifications, such as PLL bandwidth, peaking, and jitter.

3.2.2.5 USB3 PHY Reference Clock

The USB 3.0 PHY is designed to handle a wide range of input clock frequencies to support both host and device applications. The following table summarizes the requirements of the reference clock provided to the USB 3.0 PHY to support SuperSpeed only or both SuperSpeed and high-speed operations.

Table 3-7 USB3 PHY Reference Clock Requirements

Parameter	Min	Typ	Max	Unit	Conditions
Reference clock frequency	19.2	100	200	MHz	
Reference clock frequency stability	-300		300	ppm	

Table 3-7 USB3 PHY Reference Clock Requirements (continued)

Parameter	Min	Typ	Max	Unit	Conditions
Reference clock random jitter (RMS)			3	ps	1.5 MHz to Nyquist frequency. For example, for 100-MHz reference clock, the Nyquist frequency is 50 MHz
Reference clock skew			200	ps	
Reference clock cycle-to-cycle jitter			150	ps	DJ over all frequency
Duty cycle	40		60	%	
Common mode input level	0		1.32	V	Differential inputs
Differential input swing	0.3			Vpp	Differential inputs[2]
Single-ended input logic: Low	-0.3		0.3	V	If single-ended input is used
Single-ended input logic: High	vp-0.3		vp	V	If single-ended input is used
Input edge rate	0.6		4	V/ns	
Required external reference resistance		200		Ohms	± 1% accuracy

3.2.2.6 USB2 PHY Reference Clock

The USB2 PHY supports the following reference clock sources:

- **Crystal Oscillator connected to the USB2_*_XI and USB2_*_XO pins**: The crystal oscillator must have a frequency tolerance of ±400 ppm, peak jitter of ±100 ps, and an output differential voltage of no less than 500 mV with respect to the XI signal.

- **External Clock connected to the USB2_*_XO pin**: The clock must have a fundamental frequency of 50 MHz, with a frequency tolerance of ± 400 ppm, peak jitter of ± 100 ps, duty cycle between 40/60 and 60/40 percent, and signal swing of 1.8V.

3.2.2.7 HDMI PLL Reference Clock

Table 3-8 HDMI PLL Reference Clock Requirements

Parameter	Min	Typical	Max	Unit
Frequency range		27		MHz
Frequency stability	-50		50	ppm
Output		LVCMOS 1.8		V
Duty cycle	40		60	%

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[2] VDREF_CLK / 4 + VCMREF_CLK ≤ vp + diode forward biasing voltage and VCMREF_CLK – VDREF_CLK / 4 ≥ –diode forward biasing voltage

3.2.2.8 LVDS PLL Reference Clock

Table 3-9 LVDS PLL Reference Clock Requirements

Parameter	Min	Typical	Max	Unit
Frequency range		27		MHz
Frequency stability	-50		50	ppm
Output		LVCMOS 1.8		V
Duty cycle	40		60	%

4 Power-Up/Down

4.1 Power-Up Sequence

The following steps have to be performed to power up the SoC:

1. Provide the RESET_N reset signal (active is low)

2. Apply voltages to power pins according to Power Requirements in the following order:

   - 3.3V voltage supply

   - 1.5V voltage supply

   - PLL supply

   - DDR supply

   - 1.8V voltage supply

   - Core supply and 0.95V voltage supply

3. Provide all reference clocks

4. Wait at least 16 cycles of the reference clock

5. Deassert the RESET_N signal

Once the RESET_N signal is deasserted, the boot controller provides initialization of clock and reset signals for each SoC subsystem, loads and executes the Boot Loader, which is stored in the Boot SPI Flash.

4.2 Power-Down Sequence

Power down sequence is the reverse of the power up sequence.

5 Pin Assignment

5.1 Pinout List

The table below contains the list of I/O pins of the chip including the power-ground supplies.

Legend:

I	Input
O	Output
IO	Input/Output
A	Analog
P	Power supply
G	Ground
NC	Not connected

Table 5-1 Pinout List

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1	AG18	ARC_DBG_TF	SM	O	VDDIO_18	Indicates that a triple fault exception has occurred
2	AH18	ARC_WDT_RESET	SM	O	VDDIO_18	Watchdog reset
3	AM18	BOOT_ERR	SM	O	VDDIO_18	Internal SRAM data loading CRC error
4	AM19	TEST_0	SM	I	VDDIO_18	Test point 0
5	AJ16	CLK25M	Clocks	I	VDDIO_18	PLL Reference Clock 25MHz IN - SM
6	AG15	CS_CLK	CoreSight	O	VDDIO_18	Trace port clock
7	AG16	CS_CTRL	CoreSight	O	VDDIO_18	Trace port control
8	AE5	CS_DAT[0]	CoreSight	O	VDDIO_18	Trace port data
9	AE6	CS_DAT[1]	CoreSight	O	VDDIO_18	Trace port data
10	AF12	CS_DAT[10]	CoreSight	O	VDDIO_18	Trace port data
11	AG6	CS_DAT[11]	CoreSight	O	VDDIO_18	Trace port data
12	AG7	CS_DAT[12]	CoreSight	O	VDDIO_18	Trace port data
13	AG8	CS_DAT[13]	CoreSight	O	VDDIO_18	Trace port data
14	AG10	CS_DAT[14]	CoreSight	O	VDDIO_18	Trace port data
15	AG11	CS_DAT[15]	CoreSight	O	VDDIO_18	Trace port data
16	AE9	CS_DAT[2]	CoreSight	O	VDDIO_18	Trace port data
17	AE10	CS_DAT[3]	CoreSight	O	VDDIO_18	Trace port data
18	AE11	CS_DAT[4]	CoreSight	O	VDDIO_18	Trace port data
19	AF6	CS_DAT[5]	CoreSight	O	VDDIO_18	Trace port data
20	AF7	CS_DAT[6]	CoreSight	O	VDDIO_18	Trace port data
21	AF9	CS_DAT[7]	CoreSight	O	VDDIO_18	Trace port data

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
22	AF10	CS_DAT[8]	CoreSight	O	VDDIO_18	Trace port data
23	AF11	CS_DAT[9]	CoreSight	O	VDDIO_18	Trace port data
24	AE12	CS_SWCLK_TCK	CoreSight	I	VDDIO_18	Serial wire and TAP clock
25	AF13	CS_SWDIO_TMS	CoreSight	IO	VDDIO_18	Combined serial wire input/output
26	AG13	CS_TDI	CoreSight	I	VDDIO_18	JTAG TAP Data in
27	AH17	CS_TDO	CoreSight	O	VDDIO_18	JTAG TAP Data out
28	AG14	CS_TRST_N	CoreSight	I	VDDIO_18	TAP Asynchronous reset
29	K12	DDR0_A[0]	DDR 0	O	VDDQ_DDR0	SDRAM Address
30	M13	DDR0_A[1]	DDR 0	O	VDDQ_DDR0	SDRAM Address
31	AA9	DDR0_A[10]	DDR 0	O	VDDQ_DDR0	SDRAM Address
32	AC11	DDR0_A[11]	DDR 0	O	VDDQ_DDR0	SDRAM Address
33	Y13	DDR0_A[12]	DDR 0	O	VDDQ_DDR0	SDRAM Address
34	AC12	DDR0_A[13]	DDR 0	O	VDDQ_DDR0	SDRAM Address
35	AA11	DDR0_A[14]	DDR 0	O	VDDQ_DDR0	SDRAM WE
36	Y10	DDR0_A[15]	DDR 0	O	VDDQ_DDR0	SDRAM CAS
37	AB11	DDR0_A[16]	DDR 0	O	VDDQ_DDR0	SDRAM RAS
38	AA8	DDR0_A[17]	DDR 0	O	VDDQ_DDR0	SDRAM A[17]
39	J12	DDR0_A[2]	DDR 0	O	VDDQ_DDR0	SDRAM Address
40	T12	DDR0_A[3]	DDR 0	O	VDDQ_DDR0	SDRAM Address
41	L14	DDR0_A[4]	DDR 0	O	VDDQ_DDR0	SDRAM Address
42	AB12	DDR0_A[5]	DDR 0	O	VDDQ_DDR0	SDRAM Address
43	V13	DDR0_A[6]	DDR 0	O	VDDQ_DDR0	SDRAM Address
44	AB10	DDR0_A[7]	DDR 0	O	VDDQ_DDR0	SDRAM Address
45	V11	DDR0_A[8]	DDR 0	O	VDDQ_DDR0	SDRAM Address
46	Y11	DDR0_A[9]	DDR 0	O	VDDQ_DDR0	SDRAM Address
47	H10	DDR0_ACT_N	DDR 0	O	VDDQ_DDR0	When low, indicates the activate (open row) command
48	U12	DDR0_ALERT_N	DDR 0	I	VDDQ_DDR0	SDRAM CRC/Parity Error
49	U11	DDR0_ATO	DDR 0	A		Analog Test Output (test Pad)
50	J13	DDR0_BA[0]	DDR 0	O	VDDQ_DDR0	SDRAM Bank Address
51	J10	DDR0_BA[1]	DDR 0	O	VDDQ_DDR0	SDRAM Bank Address
52	U7	DDR0_BG[0]	DDR 0	O	VDDQ_DDR0	SDRAM Bank Group
53	M12	DDR0_BG[1]	DDR 0	O	VDDQ_DDR0	SDRAM Bank Group

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
54	L9	DDR0_CK[0]	DDR 0	O	VDDQ_DDR0	SDRAM Clock
55	M11	DDR0_CK[1]	DDR 0	O	VDDQ_DDR0	SDRAM Clock
56	N10	DDR0_CK[2]	DDR 0	O	VDDQ_DDR0	SDRAM Clock
57	P11	DDR0_CK[3]	DDR 0	O	VDDQ_DDR0	SDRAM Clock
58	M9	DDR0_CK_N[0]	DDR 0	O	VDDQ_DDR0	SDRAM Clock
59	L11	DDR0_CK_N[1]	DDR 0	O	VDDQ_DDR0	SDRAM Clock
60	P10	DDR0_CK_N[2]	DDR 0	O	VDDQ_DDR0	SDRAM Clock
61	R11	DDR0_CK_N[3]	DDR 0	O	VDDQ_DDR0	SDRAM Clock
62	R12	DDR0_CKE[0]	DDR 0	O	VDDQ_DDR0	SDRAM Clock enable
63	N13	DDR0_CKE[1]	DDR 0	O	VDDQ_DDR0	SDRAM Clock enable
64	AB13	DDR0_CKE[2]	DDR 0	O	VDDQ_DDR0	SDRAM Clock enable
65	W10	DDR0_CKE[3]	DDR 0	O	VDDQ_DDR0	SDRAM Clock enable
66	L13	DDR0_CS_N[0]	DDR 0	O	VDDQ_DDR0	SDRAM Chip Select
67	P13	DDR0_CS_N[1]	DDR 0	O	VDDQ_DDR0	SDRAM Chip Select
68	W9	DDR0_CS_N[2]	DDR 0	O	VDDQ_DDR0	SDRAM Chip Select
69	U10	DDR0_CS_N[3]	DDR 0	O	VDDQ_DDR0	SDRAM Chip Select
70	AB8	DDR0_DM[0]	DDR 0	IO	VDDQ_DDR0	SDRAM Data Mask
71	AC4	DDR0_DM[1]	DDR 0	IO	VDDQ_DDR0	SDRAM Data Mask
72	Y7	DDR0_DM[2]	DDR 0	IO	VDDQ_DDR0	SDRAM Data Mask
73	T2	DDR0_DM[3]	DDR 0	IO	VDDQ_DDR0	SDRAM Data Mask
74	L8	DDR0_DM[4]	DDR 0	IO	VDDQ_DDR0	SDRAM Data Mask
75	N3	DDR0_DM[5]	DDR 0	IO	VDDQ_DDR0	SDRAM Data Mask
76	K7	DDR0_DM[6]	DDR 0	IO	VDDQ_DDR0	SDRAM Data Mask
77	J3	DDR0_DM[7]	DDR 0	IO	VDDQ_DDR0	SDRAM Data Mask
78	P2	DDR0_DM[8]	DDR 0	IO	VDDQ_DDR0	SDRAM Data Mask
79	AD5	DDR0_DQ[0]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
80	AB7	DDR0_DQ[1]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
81	Y3	DDR0_DQ[10]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
82	Y4	DDR0_DQ[11]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
83	AB1	DDR0_DQ[12]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
84	AB2	DDR0_DQ[13]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
85	AB3	DDR0_DQ[14]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
86	AB4	DDR0_DQ[15]	DDR 0	IO	VDDQ_DDR0	SDRAM Data

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
87	V6	DDR0_DQ[16]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
88	V5	DDR0_DQ[17]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
89	Y5	DDR0_DQ[18]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
90	Y8	DDR0_DQ[19]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
91	AB6	DDR0_DQ[2]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
92	V7	DDR0_DQ[20]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
93	U5	DDR0_DQ[21]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
94	W8	DDR0_DQ[22]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
95	Y6	DDR0_DQ[23]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
96	V3	DDR0_DQ[24]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
97	V4	DDR0_DQ[25]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
98	T3	DDR0_DQ[26]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
99	T1	DDR0_DQ[27]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
100	V2	DDR0_DQ[28]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
101	W4	DDR0_DQ[29]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
102	AB5	DDR0_DQ[3]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
103	T4	DDR0_DQ[30]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
104	V1	DDR0_DQ[31]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
105	L5	DDR0_DQ[32]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
106	L6	DDR0_DQ[33]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
107	L7	DDR0_DQ[34]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
108	M8	DDR0_DQ[35]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
109	N5	DDR0_DQ[36]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
110	N6	DDR0_DQ[37]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
111	N7	DDR0_DQ[38]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
112	N8	DDR0_DQ[39]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
113	AD7	DDR0_DQ[4]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
114	K1	DDR0_DQ[40]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
115	K2	DDR0_DQ[41]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
116	K3	DDR0_DQ[42]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
117	L4	DDR0_DQ[43]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
118	M1	DDR0_DQ[44]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
119	M2	DDR0_DQ[45]	DDR 0	IO	VDDQ_DDR0	SDRAM Data

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
120	M3	DDR0_DQ[46]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
121	N4	DDR0_DQ[47]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
122	J5	DDR0_DQ[48]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
123	J7	DDR0_DQ[49]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
124	AD6	DDR0_DQ[5]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
125	J8	DDR0_DQ[50]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
126	J6	DDR0_DQ[51]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
127	G5	DDR0_DQ[52]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
128	G8	DDR0_DQ[53]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
129	G6	DDR0_DQ[54]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
130	G7	DDR0_DQ[55]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
131	F1	DDR0_DQ[56]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
132	F2	DDR0_DQ[57]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
133	F3	DDR0_DQ[58]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
134	G4	DDR0_DQ[59]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
135	AD8	DDR0_DQ[6]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
136	H1	DDR0_DQ[60]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
137	H2	DDR0_DQ[61]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
138	H3	DDR0_DQ[62]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
139	J4	DDR0_DQ[63]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
140	AC8	DDR0_DQ[7]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
141	Y1	DDR0_DQ[8]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
142	Y2	DDR0_DQ[9]	DDR 0	IO	VDDQ_DDR0	SDRAM Data
143	AC6	DDR0_DQS[0]	DDR 0	IO	VDDQ_DDR0	SDRAM Data Strobe
144	AA2	DDR0_DQS[1]	DDR 0	IO	VDDQ_DDR0	SDRAM Data Strobe
145	W5	DDR0_DQS[2]	DDR 0	IO	VDDQ_DDR0	SDRAM Data Strobe
146	U2	DDR0_DQS[3]	DDR 0	IO	VDDQ_DDR0	SDRAM Data Strobe
147	M5	DDR0_DQS[4]	DDR 0	IO	VDDQ_DDR0	SDRAM Data Strobe
148	L2	DDR0_DQS[5]	DDR 0	IO	VDDQ_DDR0	SDRAM Data Strobe
149	H5	DDR0_DQS[6]	DDR 0	IO	VDDQ_DDR0	SDRAM Data Strobe
150	G1	DDR0_DQS[7]	DDR 0	IO	VDDQ_DDR0	SDRAM Data Strobe
151	P3	DDR0_DQS[8]	DDR 0	IO	VDDQ_DDR0	SDRAM Data Strobe
152	AC5	DDR0_DQS_N[0]	DDR 0	IO	VDDQ_DDR0	SDRAM Data Strobe

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
153	AA1	DDR0_DQS_N[1]	DDR 0	IO	VDDQ_DDR0	SDRAM Data Strobe
154	W6	DDR0_DQS_N[2]	DDR 0	IO	VDDQ_DDR0	SDRAM Data Strobe
155	U1	DDR0_DQS_N[3]	DDR 0	IO	VDDQ_DDR0	SDRAM Data Strobe
156	M6	DDR0_DQS_N[4]	DDR 0	IO	VDDQ_DDR0	SDRAM Data Strobe
157	L1	DDR0_DQS_N[5]	DDR 0	IO	VDDQ_DDR0	SDRAM Data Strobe
158	H6	DDR0_DQS_N[6]	DDR 0	IO	VDDQ_DDR0	SDRAM Data Strobe
159	G2	DDR0_DQS_N[7]	DDR 0	IO	VDDQ_DDR0	SDRAM Data Strobe
160	R3	DDR0_DQS_N[8]	DDR 0	IO	VDDQ_DDR0	SDRAM Data Strobe
161	K10	DDR0_DTO[0]	DDR 0	O	VDDQ_DDR0	Digital Test Output (test Pad)
162	J9	DDR0_DTO[1]	DDR 0	O	VDDQ_DDR0	Digital Test Output (test Pad)
163	T6	DDR0_ECC[0]	DDR 0	IO	VDDQ_DDR0	SDRAM Data ECC
164	R6	DDR0_ECC[1]	DDR 0	IO	VDDQ_DDR0	SDRAM Data ECC
165	P6	DDR0_ECC[2]	DDR 0	IO	VDDQ_DDR0	SDRAM Data ECC
166	R5	DDR0_ECC[3]	DDR 0	IO	VDDQ_DDR0	SDRAM Data ECC
167	P1	DDR0_ECC[4]	DDR 0	IO	VDDQ_DDR0	SDRAM Data ECC
168	R1	DDR0_ECC[5]	DDR 0	IO	VDDQ_DDR0	SDRAM Data ECC
169	R2	DDR0_ECC[6]	DDR 0	IO	VDDQ_DDR0	SDRAM Data ECC
170	T5	DDR0_ECC[7]	DDR 0	IO	VDDQ_DDR0	SDRAM Data ECC
171	K13	DDR0_MIRROR	DDR 0	O	VDDQ_DDR0	SDRAM Mirror (optional DIMM signal)
172	AA13	DDR0_ODT[0]	DDR 0	O	VDDQ_DDR0	SDRAM On-Die termination
173	AC9	DDR0_ODT[1]	DDR 0	O	VDDQ_DDR0	SDRAM On-Die termination
174	V9	DDR0_ODT[2]	DDR 0	O	VDDQ_DDR0	SDRAM On-Die termination
175	P8	DDR0_ODT[3]	DDR 0	O	VDDQ_DDR0	SDRAM On-Die termination
176	T10	DDR0_PARITY	DDR 0	O	VDDQ_DDR0	SDRAM Parity
177	N12	DDR0_QCSEN_N	DDR 0	O	VDDQ_DDR0	SDRAM Quad CS Enable (optional DIMM signal)
178	J11	DDR0_RAM_RST_N	DDR 0	O	VDDQ_DDR0	SDRAM Reset
179	V12	DDR0_VREFI[0]	DDR 0	A		IO ring VREFI net
180	AB9	DDR0_VREFI[1]	DDR 0	A		IO ring VREFI net
181	W12	DDR0_VREFI[2]	DDR 0	A		IO ring VREFI net
182	T7	DDR0_VREFI[3]	DDR 0	A		IO ring VREFI net
183	R8	DDR0_VREFI[4]	DDR 0	A		IO ring VREFI net

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
184	K8	DDR0_VREFI[5]	DDR 0	A		IO ring VREFI net
185	P14	DDR0_VREFI[6]	DDR 0	A		IO ring VREFI net
186	L10	DDR0_VREFI[7]	DDR 0	A		IO ring VREFI net
187	U8	DDR0_VREFI[8]	DDR 0	A		IO ring VREFI net
188	T9	DDR0_VREFI[9]	DDR 0	A		IO ring VREFI net
189	AC10	DDR0_VREFI_ZQ	DDR 0	A		IO ring VREFI ZQ net
190	AC13	DDR0_ZQ	DDR 0	A		ZQ Resistor (to external calibration resistor)
191	AM27	DDR1_A[0]	DDR 1	O	VDDQ_DDR1	SDRAM Address
192	AT22	DDR1_A[1]	DDR 1	O	VDDQ_DDR1	SDRAM Address
193	AL25	DDR1_A[10]	DDR 1	O	VDDQ_DDR1	SDRAM Address
194	AL23	DDR1_A[11]	DDR 1	O	VDDQ_DDR1	SDRAM Address
195	AL32	DDR1_A[12]	DDR 1	O	VDDQ_DDR1	SDRAM Address
196	AM23	DDR1_A[13]	DDR 1	O	VDDQ_DDR1	SDRAM Address
197	AK28	DDR1_A[14]	DDR 1	O	VDDQ_DDR1	SDRAM WE
198	AN32	DDR1_A[15]	DDR 1	O	VDDQ_DDR1	SDRAM CAS
199	AM26	DDR1_A[16]	DDR 1	O	VDDQ_DDR1	SDRAM RAS
200	AN31	DDR1_A[17]	DDR 1	O	VDDQ_DDR1	SDRAM A[17]
201	AR22	DDR1_A[2]	DDR 1	O	VDDQ_DDR1	SDRAM Address
202	AM24	DDR1_A[3]	DDR 1	O	VDDQ_DDR1	SDRAM Address
203	AP21	DDR1_A[4]	DDR 1	O	VDDQ_DDR1	SDRAM Address
204	AL22	DDR1_A[5]	DDR 1	O	VDDQ_DDR1	SDRAM Address
205	AM31	DDR1_A[6]	DDR 1	O	VDDQ_DDR1	SDRAM Address
206	AM25	DDR1_A[7]	DDR 1	O	VDDQ_DDR1	SDRAM Address
207	AK31	DDR1_A[8]	DDR 1	O	VDDQ_DDR1	SDRAM Address
208	AL31	DDR1_A[9]	DDR 1	O	VDDQ_DDR1	SDRAM Address
209	AK25	DDR1_ACT_N	DDR 1	O	VDDQ_DDR1	When low, indicates the activate (open row) command.
210	AN29	DDR1_ALERT_N	DDR 1	I	VDDQ_DDR1	SDRAM CRC/Parity Error
211	AM30	DDR1_ATO	DDR 1	A		Analog Test Output (test Pad)
212	AP24	DDR1_BA[0]	DDR 1	O	VDDQ_DDR1	SDRAM Bank Address
213	AK27	DDR1_BA[1]	DDR 1	O	VDDQ_DDR1	SDRAM Bank Address
214	AK29	DDR1_BG[0]	DDR 1	O	VDDQ_DDR1	SDRAM Bank Group
215	AP23	DDR1_BG[1]	DDR 1	O	VDDQ_DDR1	SDRAM Bank Group

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
216	AT24	DDR1_CK[0]	DDR 1	O	VDDQ_DDR1	SDRAM Clock
217	AR26	DDR1_CK[1]	DDR 1	O	VDDQ_DDR1	SDRAM Clock
218	AR25	DDR1_CK[2]	DDR 1	O	VDDQ_DDR1	SDRAM Clock
219	AR27	DDR1_CK[3]	DDR 1	O	VDDQ_DDR1	SDRAM Clock
220	AR24	DDR1_CK_N[0]	DDR 1	O	VDDQ_DDR1	SDRAM Clock
221	AT26	DDR1_CK_N[1]	DDR 1	O	VDDQ_DDR1	SDRAM Clock
222	AP25	DDR1_CK_N[2]	DDR 1	O	VDDQ_DDR1	SDRAM Clock
223	AP27	DDR1_CK_N[3]	DDR 1	O	VDDQ_DDR1	SDRAM Clock
224	AU21	DDR1_CKE[0]	DDR 1	O	VDDQ_DDR1	SDRAM Clock enable
225	AT21	DDR1_CKE[1]	DDR 1	O	VDDQ_DDR1	SDRAM Clock enable
226	AN28	DDR1_CKE[2]	DDR 1	O	VDDQ_DDR1	SDRAM Clock enable
227	AK30	DDR1_CKE[3]	DDR 1	O	VDDQ_DDR1	SDRAM Clock enable
228	AV22	DDR1_CS_N[0]	DDR 1	O	VDDQ_DDR1	SDRAM Chip Select
229	AW22	DDR1_CS_N[1]	DDR 1	O	VDDQ_DDR1	SDRAM Chip Select
230	AV21	DDR1_CS_N[2]	DDR 1	O	VDDQ_DDR1	SDRAM Chip Select
231	AN26	DDR1_CS_N[3]	DDR 1	O	VDDQ_DDR1	SDRAM Chip Select
232	AW34	DDR1_DM[0]	DDR 1	IO	VDDQ_DDR1	SDRAM Data Mask
233	AW25	DDR1_DM[1]	DDR 1	IO	VDDQ_DDR1	SDRAM Data Mask
234	AV38	DDR1_DM[2]	DDR 1	IO	VDDQ_DDR1	SDRAM Data Mask
235	AV29	DDR1_DM[3]	DDR 1	IO	VDDQ_DDR1	SDRAM Data Mask
236	AN34	DDR1_DM[4]	DDR 1	IO	VDDQ_DDR1	SDRAM Data Mask
237	AN37	DDR1_DM[5]	DDR 1	IO	VDDQ_DDR1	SDRAM Data Mask
238	AJ36	DDR1_DM[6]	DDR 1	IO	VDDQ_DDR1	SDRAM Data Mask
239	AJ37	DDR1_DM[7]	DDR 1	IO	VDDQ_DDR1	SDRAM Data Mask
240	AR32	DDR1_DM[8]	DDR 1	IO	VDDQ_DDR1	SDRAM Data Mask
241	AV32	DDR1_DQ[0]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
242	AW32	DDR1_DQ[1]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
243	AU25	DDR1_DQ[10]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
244	AV25	DDR1_DQ[11]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
245	AU23	DDR1_DQ[12]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
246	AW23	DDR1_DQ[13]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
247	AW24	DDR1_DQ[14]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
248	AV23	DDR1_DQ[15]	DDR 1	IO	VDDQ_DDR1	SDRAM Data

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
249	AW36	DDR1_DQ[16]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
250	AU36	DDR1_DQ[17]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
251	AV36	DDR1_DQ[18]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
252	AU38	DDR1_DQ[19]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
253	AU32	DDR1_DQ[2]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
254	AV39	DDR1_DQ[20]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
255	AU39	DDR1_DQ[21]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
256	AW39	DDR1_DQ[22]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
257	AW37	DDR1_DQ[23]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
258	AU27	DDR1_DQ[24]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
259	AW27	DDR1_DQ[25]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
260	AV27	DDR1_DQ[26]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
261	AW28	DDR1_DQ[27]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
262	AU29	DDR1_DQ[28]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
263	AU30	DDR1_DQ[29]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
264	AW33	DDR1_DQ[3]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
265	AW30	DDR1_DQ[30]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
266	AV30	DDR1_DQ[31]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
267	AN35	DDR1_DQ[32]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
268	AM35	DDR1_DQ[33]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
269	AM36	DDR1_DQ[34]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
270	AR36	DDR1_DQ[35]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
271	AM34	DDR1_DQ[36]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
272	AR35	DDR1_DQ[37]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
273	AR34	DDR1_DQ[38]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
274	AP34	DDR1_DQ[39]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
275	AU34	DDR1_DQ[4]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
276	AP37	DDR1_DQ[40]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
277	AR37	DDR1_DQ[41]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
278	AR38	DDR1_DQ[42]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
279	AR39	DDR1_DQ[43]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
280	AM37	DDR1_DQ[44]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
281	AN39	DDR1_DQ[45]	DDR 1	IO	VDDQ_DDR1	SDRAM Data

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
282	AN38	DDR1_DQ[46]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
283	AM38	DDR1_DQ[47]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
284	AH34	DDR1_DQ[48]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
285	AL36	DDR1_DQ[49]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
286	AV34	DDR1_DQ[5]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
287	AL34	DDR1_DQ[50]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
288	AK34	DDR1_DQ[51]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
289	AL35	DDR1_DQ[52]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
290	AH36	DDR1_DQ[53]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
291	AH35	DDR1_DQ[54]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
292	AJ34	DDR1_DQ[55]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
293	AH37	DDR1_DQ[56]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
294	AL37	DDR1_DQ[57]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
295	AL38	DDR1_DQ[58]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
296	AL39	DDR1_DQ[59]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
297	AU35	DDR1_DQ[6]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
298	AH38	DDR1_DQ[60]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
299	AK37	DDR1_DQ[61]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
300	AJ38	DDR1_DQ[62]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
301	AH39	DDR1_DQ[63]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
302	AV35	DDR1_DQ[7]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
303	AU26	DDR1_DQ[8]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
304	AV26	DDR1_DQ[9]	DDR 1	IO	VDDQ_DDR1	SDRAM Data
305	AU33	DDR1_DQS[0]	DDR 1	IO	VDDQ_DDR1	SDRAM Data Strobe
306	AU24	DDR1_DQS[1]	DDR 1	IO	VDDQ_DDR1	SDRAM Data Strobe
307	AU37	DDR1_DQS[2]	DDR 1	IO	VDDQ_DDR1	SDRAM Data Strobe
308	AU28	DDR1_DQS[3]	DDR 1	IO	VDDQ_DDR1	SDRAM Data Strobe
309	AP36	DDR1_DQS[4]	DDR 1	IO	VDDQ_DDR1	SDRAM Data Strobe
310	AP38	DDR1_DQS[5]	DDR 1	IO	VDDQ_DDR1	SDRAM Data Strobe
311	AJ35	DDR1_DQS[6]	DDR 1	IO	VDDQ_DDR1	SDRAM Data Strobe
312	AK38	DDR1_DQS[7]	DDR 1	IO	VDDQ_DDR1	SDRAM Data Strobe
313	AR30	DDR1_DQS[8]	DDR 1	IO	VDDQ_DDR1	SDRAM Data Strobe
314	AV33	DDR1_DQS_N[0]	DDR 1	IO	VDDQ_DDR1	SDRAM Data Strobe

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
315	AV24	DDR1_DQS_N[1]	DDR 1	IO	VDDQ_DDR1	SDRAM Data Strobe
316	AV37	DDR1_DQS_N[2]	DDR 1	IO	VDDQ_DDR1	SDRAM Data Strobe
317	AV28	DDR1_DQS_N[3]	DDR 1	IO	VDDQ_DDR1	SDRAM Data Strobe
318	AP35	DDR1_DQS_N[4]	DDR 1	IO	VDDQ_DDR1	SDRAM Data Strobe
319	AP39	DDR1_DQS_N[5]	DDR 1	IO	VDDQ_DDR1	SDRAM Data Strobe
320	AK35	DDR1_DQS_N[6]	DDR 1	IO	VDDQ_DDR1	SDRAM Data Strobe
321	AK39	DDR1_DQS_N[7]	DDR 1	IO	VDDQ_DDR1	SDRAM Data Strobe
322	AP30	DDR1_DQS_N[8]	DDR 1	IO	VDDQ_DDR1	SDRAM Data Strobe
323	AK26	DDR1_DTO[0]	DDR 1	O	VDDQ_DDR1	Digital Test Output (test Pad)
324	AK24	DDR1_DTO[1]	DDR 1	O	VDDQ_DDR1	Digital Test Output (test Pad)
325	AT30	DDR1_ECC[0]	DDR 1	IO	VDDQ_DDR1	SDRAM Data ECC
326	AR29	DDR1_ECC[1]	DDR 1	IO	VDDQ_DDR1	SDRAM Data ECC
327	AT29	DDR1_ECC[2]	DDR 1	IO	VDDQ_DDR1	SDRAM Data ECC
328	AT31	DDR1_ECC[3]	DDR 1	IO	VDDQ_DDR1	SDRAM Data ECC
329	AP29	DDR1_ECC[4]	DDR 1	IO	VDDQ_DDR1	SDRAM Data ECC
330	AP31	DDR1_ECC[5]	DDR 1	IO	VDDQ_DDR1	SDRAM Data ECC
331	AT32	DDR1_ECC[6]	DDR 1	IO	VDDQ_DDR1	SDRAM Data ECC
332	AP32	DDR1_ECC[7]	DDR 1	IO	VDDQ_DDR1	SDRAM Data ECC
333	AP22	DDR1_MIRROR	DDR 1	O	VDDQ_DDR1	SDRAM Mirror (optional DIMM signal)
334	AK22	DDR1_ODT[0]	DDR 1	O	VDDQ_DDR1	SDRAM On-Die termination
335	AM28	DDR1_ODT[1]	DDR 1	O	VDDQ_DDR1	SDRAM On-Die termination
336	AW21	DDR1_ODT[2]	DDR 1	O	VDDQ_DDR1	SDRAM On-Die termination
337	AM22	DDR1_ODT[3]	DDR 1	O	VDDQ_DDR1	SDRAM On-Die termination
338	AL27	DDR1_PARITY	DDR 1	O	VDDQ_DDR1	SDRAM Parity
339	AN22	DDR1_QCSEN_N	DDR 1	O	VDDQ_DDR1	SDRAM Quad CS Enable (optional DIMM signal)
340	AN24	DDR1_RAM_RST_N	DDR 1	O	VDDQ_DDR1	SDRAM Reset
341	AJ22	DDR1_VREFI[0]	DDR 1	A		IO ring VREFI net
342	AG23	DDR1_VREFI[1]	DDR 1	A		IO ring VREFI net
343	AG24	DDR1_VREFI[2]	DDR 1	A		IO ring VREFI net
344	AG25	DDR1_VREFI[3]	DDR 1	A		IO ring VREFI net
345	AG26	DDR1_VREFI[4]	DDR 1	A		IO ring VREFI net

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
346	AH27	DDR1_VREFI[5]	DDR 1	A		IO ring VREFI net
347	AH26	DDR1_VREFI[6]	DDR 1	A		IO ring VREFI net
348	AJ25	DDR1_VREFI[7]	DDR 1	A		IO ring VREFI net
349	AJ24	DDR1_VREFI[8]	DDR 1	A		IO ring VREFI net
350	AH23	DDR1_VREFI[9]	DDR 1	A		IO ring VREFI net
351	AH22	DDR1_VREFI_ZQ	DDR 1	A		IO ring VREFI ZQ net
352	AG22	DDR1_ZQ	DDR 1	A		ZQ Resistor (to external calibration resistor)
353	C35	ESPI_ALERT[0]	eSPI	I	VDDIO_18	eSPI Alert
354	C37	ESPI_ALERT[1]	eSPI	I	VDDIO_18	eSPI Alert
355	C38	ESPI_ALERT[2]	eSPI	I	VDDIO_18	eSPI Alert
356	D35	ESPI_ALERT[3]	eSPI	I	VDDIO_18	eSPI Alert
357	D36	ESPI_ALERT[4]	eSPI	I	VDDIO_18	eSPI Alert
358	D37	ESPI_ALERT[5]	eSPI	I	VDDIO_18	eSPI Alert
359	E35	ESPI_ALERT[6]	eSPI	I	VDDIO_18	eSPI Alert
360	E34	ESPI_ALERT[7]	eSPI	I	VDDIO_18	eSPI Alert
361	A38	ESPI_CLK	eSPI	IO	VDDIO_18	eSPI clock
362	A39	ESPI_DAT[0]	eSPI	IO	VDDIO_18	eSPI data
363	B39	ESPI_DAT[1]	eSPI	IO	VDDIO_18	eSPI data
364	C39	ESPI_DAT[2]	eSPI	IO	VDDIO_18	eSPI data
365	D39	ESPI_DAT[3]	eSPI	IO	VDDIO_18	eSPI data
366	D34	ESPI_RST	eSPI	IO	VDDIO_18	eSPI reset
367	A35	ESPI_SS_N[0]	eSPI	IO	VDDIO_18	eSPI Slave Select
368	A36	ESPI_SS_N[1]	eSPI	IO	VDDIO_18	eSPI Slave Select
369	A37	ESPI_SS_N[2]	eSPI	IO	VDDIO_18	eSPI Slave Select
370	B35	ESPI_SS_N[3]	eSPI	IO	VDDIO_18	eSPI Slave Select
371	B36	ESPI_SS_N[4]	eSPI	IO	VDDIO_18	eSPI Slave Select
372	B37	ESPI_SS_N[5]	eSPI	IO	VDDIO_18	eSPI Slave Select
373	C33	ESPI_SS_N[6]	eSPI	IO	VDDIO_18	eSPI Slave Select
374	C34	ESPI_SS_N[7]	eSPI	IO	VDDIO_18	eSPI Slave Select
375	E4	G0_GP_IN	GMAC 0	I	VDDIO_18	GPIO
376	E3	G0_GP_OUT	GMAC 0	O	VDDIO_18	GPIO
377	E1	G0_MDC	GMAC 0	O	VDDIO_18	MDIO Interface
378	E2	G0_MDIO	GMAC 0	IO	VDDIO_18	MDIO Interface

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
379	C7	G0_RX_CLK	GMAC 0	I	VDDIO_18	Receive reference clock
380	C5	G0_RX_DAT[0]	GMAC 0	I	VDDIO_18	Receive Data
381	C6	G0_RX_DAT[1]	GMAC 0	I	VDDIO_18	Receive Data
382	D5	G0_RX_DAT[2]	GMAC 0	I	VDDIO_18	Receive Data
383	D6	G0_RX_DAT[3]	GMAC 0	I	VDDIO_18	Receive Data
384	D7	G0_RX_DEN	GMAC 0	I	VDDIO_18	Receive Data Enable
385	C4	G0_TX_CLK	GMAC 0	O	VDDIO_18	Transmit reference clock
386	C1	G0_TX_DAT[0]	GMAC 0	O	VDDIO_18	Transmit Data
387	C2	G0_TX_DAT[1]	GMAC 0	O	VDDIO_18	Transmit Data
388	C3	G0_TX_DAT[2]	GMAC 0	O	VDDIO_18	Transmit Data
389	D2	G0_TX_DAT[3]	GMAC 0	O	VDDIO_18	Transmit Data
390	D4	G0_TX_DEN	GMAC 0	O	VDDIO_18	Transmit Data Enable
391	E7	G1_GP_IN	GMAC 1	I	VDDIO_18	GPIO
392	E8	G1_GP_OUT	GMAC 1	O	VDDIO_18	GPIO
393	E5	G1_MDC	GMAC 1	O	VDDIO_18	MDIO Interface
394	E6	G1_MDIO	GMAC 1	IO	VDDIO_18	MDIO Interface
395	A7	G1_RX_CLK	GMAC 1	I	VDDIO_18	Receive reference clock
396	A5	G1_RX_DAT[0]	GMAC 1	I	VDDIO_18	Receive Data
397	A6	G1_RX_DAT[1]	GMAC 1	I	VDDIO_18	Receive Data
398	B5	G1_RX_DAT[2]	GMAC 1	I	VDDIO_18	Receive Data
399	B6	G1_RX_DAT[3]	GMAC 1	I	VDDIO_18	Receive Data
400	B7	G1_RX_DEN	GMAC 1	I	VDDIO_18	Receive Data Enable
401	A3	G1_TX_CLK	GMAC 1	O	VDDIO_18	Transmit reference clock
402	A1	G1_TX_DAT[0]	GMAC 1	O	VDDIO_18	Transmit Data
403	A2	G1_TX_DAT[1]	GMAC 1	O	VDDIO_18	Transmit Data
404	B1	G1_TX_DAT[2]	GMAC 1	O	VDDIO_18	Transmit Data
405	B2	G1_TX_DAT[3]	GMAC 1	O	VDDIO_18	Transmit Data
406	B3	G1_TX_DEN	GMAC 1	O	VDDIO_18	Transmit Data Enable
407	G35	GPIO32[0]	GPIO32	IO	VDDIO_18	GPIO Data
408	G36	GPIO32[1]	GPIO32	IO	VDDIO_18	GPIO Data
409	J36	GPIO32[10]	GPIO32	IO	VDDIO_18	GPIO Data
410	K31	GPIO32[11]	GPIO32	IO	VDDIO_18	GPIO Data
411	K32	GPIO32[12]	GPIO32	IO	VDDIO_18	GPIO Data

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
412	L31	GPIO32[13]	GPIO32	IO	VDDIO_18	GPIO Data
413	L32	GPIO32[14]	GPIO32	IO	VDDIO_18	GPIO Data
414	L33	GPIO32[15]	GPIO32	IO	VDDIO_18	GPIO Data
415	M29	GPIO32[16]	GPIO32	IO	VDDIO_18	GPIO Data
416	M30	GPIO32[17]	GPIO32	IO	VDDIO_18	GPIO Data
417	M31	GPIO32[18]	GPIO32	IO	VDDIO_18	GPIO Data
418	N30	GPIO32[19]	GPIO32	IO	VDDIO_18	GPIO Data
419	G37	GPIO32[2]	GPIO32	IO	VDDIO_18	GPIO Data
420	N31	GPIO32[20]	GPIO32	IO	VDDIO_18	GPIO Data
421	N32	GPIO32[21]	GPIO32	IO	VDDIO_18	GPIO Data
422	P32	GPIO32[22]	GPIO32	IO	VDDIO_18	GPIO Data
423	P33	GPIO32[23]	GPIO32	IO	VDDIO_18	GPIO Data
424	R28	GPIO32[24]	GPIO32	IO	VDDIO_18	GPIO Data
425	R29	GPIO32[25]	GPIO32	IO	VDDIO_18	GPIO Data
426	R30	GPIO32[26]	GPIO32	IO	VDDIO_18	GPIO Data
427	R31	GPIO32[27]	GPIO32	IO	VDDIO_18	GPIO Data
428	R33	GPIO32[28]	GPIO32	IO	VDDIO_18	GPIO Data
429	R34	GPIO32[29]	GPIO32	IO	VDDIO_18	GPIO Data
430	H32	GPIO32[3]	GPIO32	IO	VDDIO_18	GPIO Data
431	T32	GPIO32[30]	GPIO32	IO	VDDIO_18	GPIO Data
432	T33	GPIO32[31]	GPIO32	IO	VDDIO_18	GPIO Data
433	H33	GPIO32[4]	GPIO32	IO	VDDIO_18	GPIO Data
434	H34	GPIO32[5]	GPIO32	IO	VDDIO_18	GPIO Data
435	H36	GPIO32[6]	GPIO32	IO	VDDIO_18	GPIO Data
436	H37	GPIO32[7]	GPIO32	IO	VDDIO_18	GPIO Data
437	J34	GPIO32[8]	GPIO32	IO	VDDIO_18	GPIO Data
438	J35	GPIO32[9]	GPIO32	IO	VDDIO_18	GPIO Data
439	AN17	GPIO8[0]	GPIO8 SM	IO	VDDIO_18	SM GPIO Data
440	AM17	GPIO8[1]	GPIO8 SM	IO	VDDIO_18	SM GPIO Data
441	AK17	GPIO8[2]	GPIO8 SM	IO	VDDIO_18	SM GPIO Data
442	AJ18	GPIO8[3]	GPIO8 SM	IO	VDDIO_18	SM GPIO Data
443	AJ19	GPIO8[4]	GPIO8 SM	IO	VDDIO_18	SM GPIO Data

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
444	AJ20	GPIO8[5]	GPIO8 SM	IO	VDDIO_18	SM GPIO Data
445	AH19	GPIO8[6]	GPIO8 SM	IO	VDDIO_18	SM GPIO Data
446	AH20	GPIO8[7]	GPIO8 SM	IO	VDDIO_18	SM GPIO Data
447	C32	-	-	NC	-	Reserved
448	A32	24_MHZ_FREQ_OUT	-	O	VDDIO_18	Output clock 48MHz/2, In some USB purposes
449	D32	-	-	NC	-	Reserved
450	A34	-	-	NC	-	Reserved
451	B33	-	-	NC	-	Reserved
452	A33	-	-	NC	-	Reserved
453	B32	-	-	NC	-	Reserved
454	D33	-	-	NC	-	Reserved
455	B8	HDMI_CLKN	HDMI	O		TMDS clock
456	C8	HDMI_CLKP	HDMI	O		TMDS clock
457	B9	HDMI_DATN[0]	HDMI	O		TMDS data
458	E9	HDMI_DATN[1]	HDMI	O		TMDS data
459	C10	HDMI_DATN[2]	HDMI	O		TMDS data
460	A9	HDMI_DATP[0]	HDMI	O		TMDS data
461	D9	HDMI_DATP[1]	HDMI	O		TMDS data
462	B10	HDMI_DATP[2]	HDMI	O		TMDS data
463	K18	HDMI_DB_BISTDONE	HDMI	O	VDDIO_18	HDMI PHY Debug Interface
464	J18	HDMI_DB_BISTEN	HDMI	I	VDDIO_18	HDMI PHY Debug Interface
465	L17	HDMI_DB_BISTOK	HDMI	O	VDDIO_18	HDMI PHY Debug Interface
466	M16	HDMI_DB_DAT[0]	HDMI	O	VDDIO_18	HDMI PHY Debug Interface
467	N16	HDMI_DB_DAT[1]	HDMI	O	VDDIO_18	HDMI PHY Debug Interface
468	M17	HDMI_DB_DAT[2]	HDMI	O	VDDIO_18	HDMI PHY Debug Interface
469	N17	HDMI_DB_DAT[3]	HDMI	O	VDDIO_18	HDMI PHY Debug Interface
470	N18	HDMI_DB_DAT[4]	HDMI	O	VDDIO_18	HDMI PHY Debug Interface
471	P18	HDMI_DB_DAT[5]	HDMI	O	VDDIO_18	HDMI PHY Debug Interface
472	M19	HDMI_DB_DAT[6]	HDMI	O	VDDIO_18	HDMI PHY Debug Interface
473	N19	HDMI_DB_DAT[7]	HDMI	O	VDDIO_18	HDMI PHY Debug Interface
474	P19	HDMI_DB_DAT[8]	HDMI	O	VDDIO_18	HDMI PHY Debug Interface

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
475	M20	HDMI_DB_DAT[9]	HDMI	O	VDDIO_18	HDMI PHY Debug Interface
476	N20	HDMI_DB_EN	HDMI	I	VDDIO_18	HDMI PHY Debug Interface
477	P20	HDMI_DB_ENHPDRXSENSE	HDMI	I	VDDIO_18	HDMI PHY Debug Interface
478	H22	HDMI_DB_EXTERNAL	HDMI	I	VDDIO_18	HDMI PHY Debug Interface
479	J22	HDMI_DB_PHY_RESET	HDMI	I	VDDIO_18	HDMI PHY Debug Interface
480	K22	HDMI_DB_PHYDTB0	HDMI	O	VDDIO_18	HDMI PHY Debug Interface
481	M21	HDMI_DB_PHYDTB1	HDMI	O	VDDIO_18	HDMI PHY Debug Interface
482	N21	HDMI_DB_PDDQ	HDMI	I	VDDIO_18	HDMI PHY Debug Interface
483	P21	HDMI_DB_RXSENSE	HDMI	O	VDDIO_18	HDMI PHY Debug Interface
484	N22	HDMI_DB_SNK_DET_I	HDMI	O	VDDIO_18	HDMI PHY Debug Interface
485	P22	HDMI_DB_SVSRET_MODEZ	HDMI	I	VDDIO_18	HDMI PHY Debug Interface
486	R22	HDMI_DB_TX_PWRON	HDMI	I	VDDIO_18	HDMI PHY Debug Interface
487	R16	HDMI_DB_TX_READY	HDMI	O	VDDIO_18	HDMI PHY Debug Interface
488	D10	HDMI_DDCCEC	HDMI	IO		Ground reference for the Hot Plug Detect signal
489	H9	HDMI_HPD	HDMI	IO		Hot Plug Detect signal for HDMI
490	T14	HDMI_PLL_27M	Clocks	I	VDDIO_18	PLL Reference Clock 27MHz IN - HDMI
491	E10	HDMI_RESREF	HDMI	A		Reference resistor connection
492	G9	HDMI_SCL	HDMI	IO	VDDIO_18	HDMI I2C clock input
493	G10	HDMI_SDA	HDMI	IO	VDDIO_18	HDMI I2C data input
494	AL20	I2C0_SCL	I2C_0 SM	IO	VDDIO_18	SM I2C clock
495	AL19	I2C0_SDA	I2C_0 SM	IO	VDDIO_18	SM I2C data
496	G33	I2C1_SCL	I2C_1	IO	VDDIO_18	LSP I2C1 clock
497	G32	I2C1_SDA	I2C_1	IO	VDDIO_18	LSP I2C1 data
498	K30	I2C2_SCL	I2C_2	IO	VDDIO_18	LSP I2C2 clock
499	H30	I2C2_SDA	I2C_2	IO	VDDIO_18	LSP I2C2 data
500	F32	I2S_SCK	I2S	I	VDDIO_18	I2S continuous serial clock
501	G31	I2S_SDI	I2S	I	VDDIO_18	I2S serial data input
502	F33	I2S_SDO	I2S	O	VDDIO_18	I2S serial data output
503	E33	I2S_WS	I2S	I	VDDIO_18	I2S word select
504	V33	LED_PWM	LVDS	O	VDDIO_18	Brightness Control

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
505	AC39	LVDS_L0_CLKN	LVDS	O	VDDIO_18	LVDS clock
506	AC38	LVDS_L0_CLKP	LVDS	O	VDDIO_18	LVDS clock
507	AF37	LVDS_L0_DATN[0]	LVDS	O	VDDIO_18	LVDS data
508	AE38	LVDS_L0_DATN[1]	LVDS	O	VDDIO_18	LVDS data
509	AD38	LVDS_L0_DATN[2]	LVDS	O	VDDIO_18	LVDS data
510	AB37	LVDS_L0_DATN[3]	LVDS	O	VDDIO_18	LVDS data
511	AA38	LVDS_L0_DATN[4]	LVDS	O	VDDIO_18	LVDS data
512	AF38	LVDS_L0_DATP[0]	LVDS	O	VDDIO_18	LVDS data
513	AE39	LVDS_L0_DATP[1]	LVDS	O	VDDIO_18	LVDS data
514	AD37	LVDS_L0_DATP[2]	LVDS	O	VDDIO_18	LVDS data
515	AB38	LVDS_L0_DATP[3]	LVDS	O	VDDIO_18	LVDS data
516	AA39	LVDS_L0_DATP[4]	LVDS	O	VDDIO_18	LVDS data
517	U39	LVDS_L1_CLKN	LVDS	O	VDDIO_18	LVDS clock
518	U38	LVDS_L1_CLKP	LVDS	O	VDDIO_18	LVDS clock
519	Y37	LVDS_L1_DATN[0]	LVDS	O	VDDIO_18	LVDS data
520	W39	LVDS_L1_DATN[1]	LVDS	O	VDDIO_18	LVDS data
521	V37	LVDS_L1_DATN[2]	LVDS	O	VDDIO_18	LVDS data
522	T38	LVDS_L1_DATN[3]	LVDS	O	VDDIO_18	LVDS data
523	R38	LVDS_L1_DATN[4]	LVDS	O	VDDIO_18	LVDS data
524	Y38	LVDS_L1_DATP[0]	LVDS	O	VDDIO_18	LVDS data
525	W38	LVDS_L1_DATP[1]	LVDS	O	VDDIO_18	LVDS data
526	V38	LVDS_L1_DATP[2]	LVDS	O	VDDIO_18	LVDS data
527	T37	LVDS_L1_DATP[3]	LVDS	O	VDDIO_18	LVDS data
528	R39	LVDS_L1_DATP[4]	LVDS	O	VDDIO_18	LVDS data
529	AC36	LVDS_L2_CLKN	LVDS	O	VDDIO_18	LVDS clock
530	AC35	LVDS_L2_CLKP	LVDS	O	VDDIO_18	LVDS clock
531	AF35	LVDS_L2_DATN[0]	LVDS	O	VDDIO_18	LVDS data
532	AE35	LVDS_L2_DATN[1]	LVDS	O	VDDIO_18	LVDS data
533	AD35	LVDS_L2_DATN[2]	LVDS	O	VDDIO_18	LVDS data
534	AB34	LVDS_L2_DATN[3]	LVDS	O	VDDIO_18	LVDS data
535	AA35	LVDS_L2_DATN[4]	LVDS	O	VDDIO_18	LVDS data
536	AF34	LVDS_L2_DATP[0]	LVDS	O	VDDIO_18	LVDS data
537	AE36	LVDS_L2_DATP[1]	LVDS	O	VDDIO_18	LVDS data

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
538	AD34	LVDS_L2_DATP[2]	LVDS	O	VDDIO_18	LVDS data
539	AB35	LVDS_L2_DATP[3]	LVDS	O	VDDIO_18	LVDS data
540	AA36	LVDS_L2_DATP[4]	LVDS	O	VDDIO_18	LVDS data
541	U36	LVDS_L3_CLKN	LVDS	O	VDDIO_18	LVDS clock
542	U35	LVDS_L3_CLKP	LVDS	O	VDDIO_18	LVDS clock
543	Y34	LVDS_L3_DATN[0]	LVDS	O	VDDIO_18	LVDS data
544	W35	LVDS_L3_DATN[1]	LVDS	O	VDDIO_18	LVDS data
545	V34	LVDS_L3_DATN[2]	LVDS	O	VDDIO_18	LVDS data
546	T34	LVDS_L3_DATN[3]	LVDS	O	VDDIO_18	LVDS data
547	R35	LVDS_L3_DATN[4]	LVDS	O	VDDIO_18	LVDS data
548	Y35	LVDS_L3_DATP[0]	LVDS	O	VDDIO_18	LVDS data
549	W36	LVDS_L3_DATP[1]	LVDS	O	VDDIO_18	LVDS data
550	V35	LVDS_L3_DATP[2]	LVDS	O	VDDIO_18	LVDS data
551	T35	LVDS_L3_DATP[3]	LVDS	O	VDDIO_18	LVDS data
552	R36	LVDS_L3_DATP[4]	LVDS	O	VDDIO_18	LVDS data
553	AF24	LVDS_PLL_27M	Clocks	I	VDDIO_18	PLL Reference Clock 27MHz IN - LVDS
554	AD33	LVDS_VREF	LVDS	A		Signal reference
555	AT16	PCIE4_0_AMON	PCIe x4 0	O	VDD_PCIE4_0_15	Analog monitor bump
556	AU15	PCIE4_0_ATT_BUT	PCIe x4 0	I	VDDIO_18	Attention button pressed
557	AR11	PCIE4_0_ATT_IND[0]	PCIe x4 0	O	VDDIO_18	Controls the system attention indicator
558	AM16	PCIE4_0_ATT_IND[1]	PCIe x4 0	O	VDDIO_18	Controls the system attention indicator
559	AR16	PCIE4_0_CMD_INT	PCIe x4 0	I	VDDIO_18	Hot-plug controller command completed interrupt
560	AL15	PCIE4_0_DMON	PCIe x4 0	O	VDD_PCIE4_0_09	Differential digital monitor bump
561	AM15	PCIE4_0_DMONB	PCIe x4 0	O	VDD_PCIE4_0_09	Differential digital monitor bump
562	AT18	PCIE4_0_INTRL_CTRL	PCIe x4 0	O	VDDIO_18	Electromechanical Interlock Control
563	AT17	PCIE4_0_INTRL_ENG	PCIe x4 0	I	VDDIO_18	SystemElectromechanical Interlock Engaged
564	AP17	PCIE4_0_MRL_SENS	PCIe x4 0	I	VDDIO_18	MRL sensor state
565	AU16	PCIE4_0_PRES_ST	PCIe x4 0	I	VDDIO_18	Presence detect state
566	AP16	PCIE4_0_PWR_CTRL	PCIe x4 0	O	VDDIO_18	Controls the system power controller
567	AR9	PCIE4_0_PWR_FAULT	PCIe x4 0	I	VDDIO_18	Power fault detect
568	AP10	PCIE4_0_PWR_IND[0]	PCIe x4 0	O	VDDIO_18	Controls the system power indicator

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
569	AP11	PCIE4_0_PWR_IND[1]	PCIe x4 0	O	VDDIO_18	Controls the system power indicator
570	AV17	PCIE4_0_RBIAS	PCIe x4 0	IO	VDD_PCIE4_0_15	Bias resistor bump
571	AW15	PCIE4_0_REF_CLKN	PCIe x4 0	I	VDD_PCIE4_0_15	Differential reference clocks from pads
572	AW16	PCIE4_0_REF_CLKP	PCIe x4 0	I	VDD_PCIE4_0_15	Differential reference clocks from pads
573	AV14	PCIE4_0_RXN[0]	PCIe x4 0	I	VDD_PCIE4_0_15	Receive data diff pair
574	AW12	PCIE4_0_RXN[1]	PCIe x4 0	I	VDD_PCIE4_0_15	Receive data diff pair
575	AV10	PCIE4_0_RXN[2]	PCIe x4 0	I	VDD_PCIE4_0_15	Receive data diff pair
576	AW9	PCIE4_0_RXN[3]	PCIe x4 0	I	VDD_PCIE4_0_15	Receive data diff pair
577	AV13	PCIE4_0_RXP[0]	PCIe x4 0	I	VDD_PCIE4_0_15	Receive data diff pair
578	AW13	PCIE4_0_RXP[1]	PCIe x4 0	I	VDD_PCIE4_0_15	Receive data diff pair
579	AV11	PCIE4_0_RXP[2]	PCIe x4 0	I	VDD_PCIE4_0_15	Receive data diff pair
580	AW10	PCIE4_0_RXP[3]	PCIe x4 0	I	VDD_PCIE4_0_15	Receive data diff pair
581	AT14	PCIE4_0_TXN[0]	PCIe x4 0	O	VDD_PCIE4_0_15	Transmit data diff pair
582	AU13	PCIE4_0_TXN[1]	PCIe x4 0	O	VDD_PCIE4_0_15	Transmit data diff pair
583	AT11	PCIE4_0_TXN[2]	PCIe x4 0	O	VDD_PCIE4_0_15	Transmit data diff pair
584	AU10	PCIE4_0_TXN[3]	PCIe x4 0	O	VDD_PCIE4_0_15	Transmit data diff pair
585	AT13	PCIE4_0_TXP[0]	PCIe x4 0	O	VDD_PCIE4_0_15	Transmit data diff pair
586	AU12	PCIE4_0_TXP[1]	PCIe x4 0	O	VDD_PCIE4_0_15	Transmit data diff pair
587	AT10	PCIE4_0_TXP[2]	PCIe x4 0	O	VDD_PCIE4_0_15	Transmit data diff pair
588	AU9	PCIE4_0_TXP[3]	PCIe x4 0	O	VDD_PCIE4_0_15	Transmit data diff pair
589	AP13	PCIE4_1_AMON	PCIe x4 1	O	VDD_PCIE4_1_15	Analog monitor bump
590	AR7	PCIE4_1_ATT_BUT	PCIe x4 1	I	VDDIO_18	Attention button pressed
591	AM12	PCIE4_1_ATT_IND[0]	PCIe x4 1	O	VDDIO_18	Controls the system attention indicator
592	AN13	PCIE4_1_ATT_IND[1]	PCIe x4 1	O	VDDIO_18	Controls the system attention indicator
593	AJ13	PCIE4_1_CMD_INT	PCIe x4 1	I	VDDIO_18	Hot-plug controller command completed interrupt
594	AR12	PCIE4_1_DMON	PCIe x4 1	O	VDD_PCIE4_1_09	Differential digital monitor bump
595	AP12	PCIE4_1_DMONB	PCIe x4 1	O	VDD_PCIE4_1_09	Differential digital monitor bump
596	AP9	PCIE4_1_INTRL_CTRL	PCIe x4 1	O	VDDIO_18	Electromechanical Interlock Control
597	AU8	PCIE4_1_INTRL_ENG	PCIe x4 1	I	VDDIO_18	SystemElectromechanical Interlock Engaged
598	AK14	PCIE4_1_MRL_SENS	PCIe x4 1	I	VDDIO_18	MRL sensor state
599	AT8	PCIE4_1_PRES_ST	PCIe x4 1	I	VDDIO_18	Presence detect state

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
600	AL11	PCIE4_1_PWR_CTRL	PCIe x4 1	O	VDDIO_18	Controls the system power controller
601	AK13	PCIE4_1_PWR_FAULT	PCIe x4 1	I	VDDIO_18	Power fault detect
602	AL12	PCIE4_1_PWR_IND[0]	PCIe x4 1	O	VDDIO_18	Controls the system power indicator
603	AM13	PCIE4_1_PWR_IND[1]	PCIe x4 1	O	VDDIO_18	Controls the system power indicator
604	AV8	PCIE4_1_RBIAS	PCIe x4 1	IO	VDD_PCIE4_1_15	Bias resistor bump
605	AV7	PCIE4_1_REF_CLKN	PCIe x4 1	I	VDD_PCIE4_1_15	Differential reference clocks from pads
606	AW7	PCIE4_1_REF_CLKP	PCIe x4 1	I	VDD_PCIE4_1_15	Differential reference clocks from pads
607	AV6	PCIE4_1_RXN[0]	PCIe x4 1	I	VDD_PCIE4_1_15	Receive data diff pair
608	AW5	PCIE4_1_RXN[1]	PCIe x4 1	I	VDD_PCIE4_1_15	Receive data diff pair
609	AV3	PCIE4_1_RXN[2]	PCIe x4 1	I	VDD_PCIE4_1_15	Receive data diff pair
610	AW2	PCIE4_1_RXN[3]	PCIe x4 1	I	VDD_PCIE4_1_15	Receive data diff pair
611	AV5	PCIE4_1_RXP[0]	PCIe x4 1	I	VDD_PCIE4_1_15	Receive data diff pair
612	AW4	PCIE4_1_RXP[1]	PCIe x4 1	I	VDD_PCIE4_1_15	Receive data diff pair
613	AV2	PCIE4_1_RXP[2]	PCIe x4 1	I	VDD_PCIE4_1_15	Receive data diff pair
614	AW1	PCIE4_1_RXP[3]	PCIe x4 1	I	VDD_PCIE4_1_15	Receive data diff pair
615	AT6	PCIE4_1_TXN[0]	PCIe x4 1	O	VDD_PCIE4_1_15	Transmit data diff pair
616	AU5	PCIE4_1_TXN[1]	PCIe x4 1	O	VDD_PCIE4_1_15	Transmit data diff pair
617	AT3	PCIE4_1_TXN[2]	PCIe x4 1	O	VDD_PCIE4_1_15	Transmit data diff pair
618	AU2	PCIE4_1_TXN[3]	PCIe x4 1	O	VDD_PCIE4_1_15	Transmit data diff pair
619	AT5	PCIE4_1_TXP[0]	PCIe x4 1	O	VDD_PCIE4_1_15	Transmit data diff pair
620	AU4	PCIE4_1_TXP[1]	PCIe x4 1	O	VDD_PCIE4_1_15	Transmit data diff pair
621	AT2	PCIE4_1_TXP[2]	PCIe x4 1	O	VDD_PCIE4_1_15	Transmit data diff pair
622	AU1	PCIE4_1_TXP[3]	PCIe x4 1	O	VDD_PCIE4_1_15	Transmit data diff pair
623	AK6	PCIE8_AMON0	PCIe x8	O	VDD_PCIE8_15	Analog monitor bump
624	AJ8	PCIE8_AMON1	PCIe x8	O	VDD_PCIE8_15	Analog monitor bump
625	AM9	PCIE8_ATT_BUT	PCIe x8	I	VDDIO_18	Attention button pressed
626	AN7	PCIE8_ATT_IND[0]	PCIe x8	O	VDDIO_18	Controls the system attention indicator
627	AN8	PCIE8_ATT_IND[1]	PCIe x8	O	VDDIO_18	Controls the system attention indicator
628	AJ5	PCIE8_CMD_INT	PCIe x8	I	VDDIO_18	Hot-plug controller command completed interrupt
629	AL8	PCIE8_DMON0	PCIe x8	O	VDD_PCIE8_09	Differential digital monitor bump
630	AK9	PCIE8_DMON1	PCIe x8	O	VDD_PCIE8_09	Differential digital monitor bump

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
631	AL9	PCIE8_DMONB0	PCIe x8	O	VDD_PCIE8_09	Differential digital monitor bump
632	AK8	PCIE8_DMONB1	PCIe x8	O	VDD_PCIE8_09	Differential digital monitor bump
633	AM8	PCIE8_INTRL_CTRL	PCIe x8	O	VDDIO_18	Electromechanical Interlock Control
634	AM7	PCIE8_INTRL_ENG	PCIe x8	I	VDDIO_18	SystemElectromechanical Interlock Engaged
635	AH9	PCIE8_MRL_SENS	PCIe x8	I	VDDIO_18	MRL sensor state
636	AL10	PCIE8_PRES_ST	PCIe x8	I	VDDIO_18	Presence detect state
637	AJ6	PCIE8_PWR_CTRL	PCIe x8	O	VDDIO_18	Controls the system power controller
638	AJ7	PCIE8_PWR_FAULT	PCIe x8	I	VDDIO_18	Power fault detect
639	AH7	PCIE8_PWR_IND[0]	PCIe x8	O	VDDIO_18	Controls the system power indicator
640	AH8	PCIE8_PWR_IND[1]	PCIe x8	O	VDDIO_18	Controls the system power indicator
641	AN5	PCIE8_RBIAS0	PCIe x8	IO	VDD_PCIE8_15	Bias resistor bump
642	AP6	PCIE8_RBIAS1	PCIe x8	IO	VDD_PCIE8_15	Bias resistor bump
643	AL5	PCIE8_REF_CLKN	PCIe x8	I	VDD_PCIE8_15	Differential reference clocks from pads
644	AL6	PCIE8_REF_CLKP	PCIe x8	I	VDD_PCIE8_15	Differential reference clocks from pads
645	AR1	PCIE8_RXN[0]	PCIe x8	I	VDD_PCIE8_15	Receive data diff pair
646	AP2	PCIE8_RXN[1]	PCIe x8	I	VDD_PCIE8_15	Receive data diff pair
647	AM1	PCIE8_RXN[2]	PCIe x8	I	VDD_PCIE8_15	Receive data diff pair
648	AL2	PCIE8_RXN[3]	PCIe x8	I	VDD_PCIE8_15	Receive data diff pair
649	AH1	PCIE8_RXN[4]	PCIe x8	I	VDD_PCIE8_15	Receive data diff pair
650	AG2	PCIE8_RXN[5]	PCIe x8	I	VDD_PCIE8_15	Receive data diff pair
651	AE1	PCIE8_RXN[6]	PCIe x8	I	VDD_PCIE8_15	Receive data diff pair
652	AD2	PCIE8_RXN[7]	PCIe x8	I	VDD_PCIE8_15	Receive data diff pair
653	AP1	PCIE8_RXP[0]	PCIe x8	I	VDD_PCIE8_15	Receive data diff pair
654	AN2	PCIE8_RXP[1]	PCIe x8	I	VDD_PCIE8_15	Receive data diff pair
655	AL1	PCIE8_RXP[2]	PCIe x8	I	VDD_PCIE8_15	Receive data diff pair
656	AK2	PCIE8_RXP[3]	PCIe x8	I	VDD_PCIE8_15	Receive data diff pair
657	AJ1	PCIE8_RXP[4]	PCIe x8	I	VDD_PCIE8_15	Receive data diff pair
658	AH2	PCIE8_RXP[5]	PCIe x8	I	VDD_PCIE8_15	Receive data diff pair
659	AF1	PCIE8_RXP[6]	PCIe x8	I	VDD_PCIE8_15	Receive data diff pair
660	AE2	PCIE8_RXP[7]	PCIe x8	I	VDD_PCIE8_15	Receive data diff pair
661	AR4	PCIE8_TXN[0]	PCIe x8	O	VDD_PCIE8_15	Transmit data diff pair
662	AP3	PCIE8_TXN[1]	PCIe x8	O	VDD_PCIE8_15	Transmit data diff pair

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
663	AM4	PCIE8_TXN[2]	PCIe x8	O	VDD_PCIE8_15	Transmit data diff pair
664	AL3	PCIE8_TXN[3]	PCIe x8	O	VDD_PCIE8_15	Transmit data diff pair
665	AH4	PCIE8_TXN[4]	PCIe x8	O	VDD_PCIE8_15	Transmit data diff pair
666	AG3	PCIE8_TXN[5]	PCIe x8	O	VDD_PCIE8_15	Transmit data diff pair
667	AE4	PCIE8_TXN[6]	PCIe x8	O	VDD_PCIE8_15	Transmit data diff pair
668	AD3	PCIE8_TXN[7]	PCIe x8	O	VDD_PCIE8_15	Transmit data diff pair
669	AP4	PCIE8_TXP[0]	PCIe x8	O	VDD_PCIE8_15	Transmit data diff pair
670	AN3	PCIE8_TXP[1]	PCIe x8	O	VDD_PCIE8_15	Transmit data diff pair
671	AL4	PCIE8_TXP[2]	PCIe x8	O	VDD_PCIE8_15	Transmit data diff pair
672	AK3	PCIE8_TXP[3]	PCIe x8	O	VDD_PCIE8_15	Transmit data diff pair
673	AJ4	PCIE8_TXP[4]	PCIe x8	O	VDD_PCIE8_15	Transmit data diff pair
674	AH3	PCIE8_TXP[5]	PCIe x8	O	VDD_PCIE8_15	Transmit data diff pair
675	AF4	PCIE8_TXP[6]	PCIe x8	O	VDD_PCIE8_15	Transmit data diff pair
676	AE3	PCIE8_TXP[7]	PCIe x8	O	VDD_PCIE8_15	Transmit data diff pair
677	AJ15	RESET_N	Resets	I	VDDIO_18	System Reset, active low
678	D31	SATA_P0ACTLED	SATA	O	VDDIO_18	P0 Activity LED
679	E31	SATA_P0CPDET	SATA	I	VDDIO_18	Cold Presence Detect P0
680	E30	SATA_P0CPPOD	SATA	O	VDDIO_18	Cold Presence Power-On Device P0
681	F30	SATA_P0MPSW	SATA	I	VDDIO_18	Mechanical Presence Switch P0
682	F29	SATA_P1ACTLED	SATA	O	VDDIO_18	P1 Activity LED
683	G29	SATA_P1CPDET	SATA	I	VDDIO_18	Cold Presence Detect P1
684	F28	SATA_P1CPPOD	SATA	O	VDDIO_18	Cold Presence Power-On Device P1
685	G28	SATA_P1MPSW	SATA	I	VDDIO_18	Mechanical Presence Switch P1
686	A31	SATA_REFCLKM	SATA	I	VDD_SATA_09	Reference clk diff pair
687	B31	SATA_REFCLKP	SATA	I	VDD_SATA_09	Reference clk diff pair
688	D29	SATA_RESREF	SATA	A		Reference Resistor
689	C30	SATA_RXN[0]	SATA	I	VDD_SATA_09	Receive data diff pair port 0
690	B28	SATA_RXN[1]	SATA	I	VDD_SATA_09	Receive data diff pair port 1
691	B30	SATA_RXP[0]	SATA	I	VDD_SATA_09	Receive data diff pair port 0
692	C28	SATA_RXP[1]	SATA	I	VDD_SATA_09	Receive data diff pair port 1
693	B29	SATA_TXN[0]	SATA	O	VDD_SATATX_09	Transmit data diff pair port 0

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
694	A27	**SATA_TXN[1]**	SATA	O	VDD_SATATX_09	Transmit data diff pair port 1
695	A29	**SATA_TXP[0]**	SATA	O	VDD_SATATX_09	Transmit data diff pair port 0
696	B27	**SATA_TXP[1]**	SATA	O	VDD_SATATX_09	Transmit data diff pair port 1
697	L36	SD_CAP0	SD Card	A		Connected to 1uF capacitor for stabilyzing LDO output voltage
698	M35	SD_CAP1	SD Card	A		Connected to 1uF capacitor for stabilyzing LDO output voltage
699	K36	SD_CARD_DETECT_N	SD Card	I	VDDIO_18	Card Detect, active low
700	N39	SD_CLK	SD Card	O	VDD_SD_33	SD card transmit/receive clock
701	K34	SD_CMD	SD Card	IO	VDD_SD_33	SD card Command
702	L38	SD_DAT[0]	SD Card	IO	VDD_SD_33	SD card Data
703	L37	SD_DAT[1]	SD Card	IO	VDD_SD_33	SD card Data
704	M39	SD_DAT[2]	SD Card	IO	VDD_SD_33	SD card Data
705	M38	SD_DAT[3]	SD Card	IO	VDD_SD_33	SD card Data
706	M37	SD_DAT[4]	SD Card	IO	VDD_SD_33	SD card Data
707	N38	SD_DAT[5]	SD Card	IO	VDD_SD_33	SD card Data
708	N37	SD_DAT[6]	SD Card	IO	VDD_SD_33	SD card Data
709	N36	SD_DAT[7]	SD Card	IO	VDD_SD_33	SD card Data
710	M34	SD_LED_CTRL	SD Card	O	VDDIO_18	SD card LED control
711	N34	SD_REG_VOL_STABLE	SD Card	I	VDDIO_18	Voltage regulator voltage stable
712	P36	SD_RST_N	SD Card	O	VDD_SD_33	eMMC device reset, active low
713	L34	SD_VDD_ON	SD Card	O	VDDIO_18	Voltage regulator VDD1 enable
714	M33	SD_VDD_SEL[0]	SD Card	O	VDDIO_18	Voltage regulator VDD1 select
715	N33	SD_VDD_SEL[1]	SD Card	O	VDDIO_18	Voltage regulator VDD1 select
716	P34	SD_VDD_SEL[2]	SD Card	O	VDDIO_18	Voltage regulator VDD1 select
717	K35	SD_WRITE_PROT	SD Card	I	VDDIO_18	Card Write Protect, active high
718	AV18	SMB0_CLK	SMBUS SM	IO	VDDIO_18	SM SMBus clock
719	AW18	SMB0_DAT	SMBUS SM	IO	VDDIO_18	SM SMBus data
720	G39	SMB1_CLK	SMBUS 1	IO	VDDIO_18	LSP SMBus1 clock
721	H39	SMB1_DAT	SMBUS 1	IO	VDDIO_18	LSP SMBus1 data
722	G38	SMB2_CLK	SMBUS 2	IO	VDDIO_18	LSP SMBus2 clock
723	H38	SMB2_DAT	SMBUS 2	IO	VDDIO_18	LSP SMBus2 data

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
724	AL18	TEST_1	SM	I	VDDIO_18	Test point 1
725	AW19	SPI0_CLK	BC SPI 0 SM	O	VDDIO_18	Output Clock
726	AT19	SPI0_RXD	BC SPI 0 SM	I	VDDIO_18	Receive data
727	AR19	SPI0_SS_N[0]	BC SPI 0 SM	O	VDDIO_18	Slave Select
728	AP19	SPI0_SS_N[1]	BC SPI 0 SM	O	VDDIO_18	Slave Select
729	AN20	SPI0_SS_N[2]	BC SPI 0 SM	O	VDDIO_18	Slave Select
730	AM20	SPI0_SS_N[3]	BC SPI 0 SM	O	VDDIO_18	Slave Select
731	AU19	SPI0_TXD	BC SPI 0 SM	O	VDDIO_18	Transmit data
732	F39	SPI1_CLK	SPI 1	O	VDDIO_18	Output Clock
733	E38	SPI1_RXD	SPI 1	I	VDDIO_18	Receive data
734	E37	SPI1_SS_N[0]	SPI 1	O	VDDIO_18	Slave Select
735	F37	SPI1_SS_N[1]	SPI 1	O	VDDIO_18	Slave Select
736	F36	SPI1_SS_N[2]	SPI 1	O	VDDIO_18	Slave Select
737	F35	SPI1_SS_N[3]	SPI 1	O	VDDIO_18	Slave Select
738	E39	SPI1_TXD	SPI 1	O	VDDIO_18	Transmit data
739	AJ12	-	-	NC	-	Reserved
740	AH11	-	-	NC	-	Reserved
741	AH12	-	-	NC	-	Reserved
742	AH14	-	-	NC	-	Reserved
743	AH13	-	-	NC	-	Reserved
744	AK18	UART0_RXD	UART SM	I	VDDIO_18	Receive data
745	AK19	UART0_TXD	UART SM	O	VDDIO_18	Transmit data
746	J38	UART1_RXD	UART1	I	VDDIO_18	Receive data
747	J39	UART1_TXD	UART1	O	VDDIO_18	Transmit data
748	K38	UART2_RXD	UART2	I	VDDIO_18	Receive data
749	K39	UART2_TXD	UART2	O	VDDIO_18	Transmit data
750	K27	USB2_0_CTRL	USB2 0	O	VDDIO_18	Port Power Control
751	D19	USB2_0_DM0	USB2 0	IO	VDD_USB2_0_33	USB D- Signal
752	E19	USB2_0_DP0	USB2 0	IO	VDD_USB2_0_33	USB D+ Signal
753	P24	USB2_0_ID0	USB2 0	IO	VDD_USB2_18	USB Mini-Receptacle Identifier
754	P23	USB2_0_OVCUR	USB2 0	I	VDDIO_18	Port Overcurrent
755	N23	USB2_0_RT	USB2 0	IO	VDD_USB2_18	Trasmitter Resistor Tune Pin

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
756	M23	USB2_0_VBUS0	USB2 0	A		USB 5 V Signal
757	F20	USB2_0_XI	USB2 0	I	VDD_USB2_18	Crystal Oscillator XI Pin
758	G20	USB2_0_XO	USB2 0	I	VDD_USB2_18	Crystal Oscillator XO Pin or Board Reference Clock Input
759	K28	USB2_1_CTRL	USB2 1	O	VDDIO_18	Port Power Control
760	E22	USB2_1_DM0	USB2 1	IO	VDD_USB2_1_33	USB D- Signal
761	F22	USB2_1_DP0	USB2 1	IO	VDD_USB2_1_33	USB D+ Signal
762	N27	USB2_1_ID0	USB2 1	IO	VDD_USB2_18	USB Mini-Receptacle Identifier
763	N24	USB2_1_OVCUR	USB2 1	I	VDDIO_18	Port Overcurrent
764	N25	USB2_1_RT	USB2 1	IO	VDD_USB2_18	Trasmitter Resistor Tune Pin
765	M25	USB2_1_VBUS0	USB2 1	A		USB 5 V Signal
766	F21	USB2_1_XI	USB2 1	I	VDD_USB2_18	Crystal Oscillator XI Pin
767	G21	USB2_1_XO	USB2 1	I	VDD_USB2_18	Crystal Oscillator XO Pin or Board Reference Clock Input
768	H28	USB2_2_CTRL	USB2 2	O	VDDIO_18	Port Power Control
769	D23	USB2_2_DM0	USB2 2	IO	VDD_USB2_2_33	USB D- Signal
770	E23	USB2_2_DP0	USB2 2	IO	VDD_USB2_2_33	USB D+ Signal
771	N26	USB2_2_ID0	USB2 2	IO	VDD_USB2_18	USB Mini-Receptacle Identifier
772	M26	USB2_2_OVCUR	USB2 2	I	VDDIO_18	Port Overcurrent
773	H26	USB2_2_RT	USB2 2	IO	VDD_USB2_18	Trasmitter Resistor Tune Pin
774	G26	USB2_2_VBUS0	USB2 2	A		USB 5 V Signal
775	F24	USB2_2_XI	USB2 2	I	VDD_USB2_18	Crystal Oscillator XI Pin
776	G24	USB2_2_XO	USB2 2	I	VDD_USB2_18	Crystal Oscillator XO Pin or Board Reference Clock Input
777	H29	USB2_3_CTRL	USB2 3	O	VDDIO_18	Port Power Control
778	D26	USB2_3_DM0	USB2 3	IO	VDD_USB2_3_33	USB D- Signal
779	E26	USB2_3_DP0	USB2 3	IO	VDD_USB2_3_33	USB D+ Signal
780	G27	USB2_3_ID0	USB2 3	IO	VDD_USB2_18	USB Mini-Receptacle Identifier
781	E28	USB2_3_OVCUR	USB2 3	I	VDDIO_18	Port Overcurrent
782	F27	USB2_3_RT	USB2 3	IO		Trasmitter Resistor Tune Pin
783	E27	USB2_3_VBUS0	USB2 3	A		USB 5 V Signal
784	F25	USB2_3_XI	USB2 3	I	VDD_USB2_18	Crystal Oscillator XI Pin

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
785	G25	USB2_3_XO	USB2 3	I	VDD_USB2_18	Crystal Oscillator XO Pin or Board Reference Clock Input
786	K25	USB2_4_CTRL	USB3 0	O	VDDIO_18	Port Power Control - USB2 part
787	L24	USB2_4_OVCUR	USB3 0	I	VDDIO_18	Port Overcurrent - USB2 part
788	J20	USB2_5_CTRL	USB3 1	O	VDDIO_18	Port Power Control - USB2 part
789	L19	USB2_5_OVCUR	USB3 1	I	VDDIO_18	Port Overcurrent - USB2 part
790	J24	USB3_0_CTRL	USB3 0	O	VDDIO_18	Port Power Control - USB3 part
791	C26	USB3_0_DM0	USB3 0	IO	VDD_USB3_33	USB2 D- Signal
792	B26	USB3_0_DP0	USB3 0	IO	VDD_USB3_33	USB2 D+ Signal
793	L23	USB3_0_ID0	USB3 0	IO		USB2 Mini-Receptacle Identifier
794	K24	USB3_0_OVCUR	USB3 0	I	VDDIO_18	Port Overcurrent - USB3 part
795	B25	USB3_0_REFCLKN	USB3 0	I	VDD_USB3VP_0_09	USB3 Optional Reference Clock Input
796	A25	USB3_0_REFCLKP	USB3 0	I	VDD_USB3VP_0_09	USB3 Optional Reference Clock Input
797	J23	USB3_0_RESREF	USB3 0	A		USB3 External Reference Resistor
798	A23	USB3_0_RXON	USB3 0	I	VDD_USB3VP_0_09	USB3 Receive Pin
799	B23	USB3_0_RXOP	USB3 0	I	VDD_USB3VP_0_09	USB3 Receive Pin
800	B24	USB3_0_TXON	USB3 0	O	VDD_USB3TX_0_09	USB3 Transmit Pin
801	C24	USB3_0_TXOP	USB3 0	O	VDD_USB3TX_0_09	USB3 Transmit Pin
802	D24	USB3_0_VBUS0	USB3 0	A		USB 5 V Power Supply Pin
803	J19	USB3_1_CTRL	USB3 1	O	VDDIO_18	Port Power Control - USB3 part
804	C22	USB3_1_DM0	USB3 1	IO	VDD_USB3_33	USB2 D- Signal
805	B22	USB3_1_DP0	USB3 1	IO	VDD_USB3_33	USB2 D+ Signal
806	H19	USB3_1_ID0	USB3 1	IO		USB2 Mini-Receptacle Identifier
807	K19	USB3_1_OVCUR	USB3 1	I	VDDIO_18	Port Overcurrent - USB3 part
808	B21	USB3_1_REFCLKN	USB3 1	I	VDD_USB3VP_1_09	USB3 Optional Reference Clock Input
809	A21	USB3_1_REFCLKP	USB3 1	I	VDD_USB3VP_1_09	USB3 Optional Reference Clock Input
810	H20	USB3_1_RESREF	USB3 1	A		USB3 External Reference Resistor
811	A19	USB3_1_RXON	USB3 1	I	VDD_USB3VP_1_09	USB3 Receive Pin
812	B19	USB3_1_RXOP	USB3 1	I	VDD_USB3VP_1_09	USB3 Receive Pin
813	B20	USB3_1_TXON	USB3 1	O	VDD_USB3TX_1_09	USB3 Transmit Pin

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
814	C20	USB3_1_TXOP	USB3 1	O	VDD_USB3TX_1_09	USB3 Transmit Pin
815	D20	USB3_1_VBUS0	USB3 1	A		USB 5 V Power Supply Pin
816	AB16	VDD	VDD	P		Core power
817	AB17	VDD	VDD	P		Core power
818	AB18	VDD	VDD	P		Core power
819	AB19	VDD	VDD	P		Core power
820	AB20	VDD	VDD	P		Core power
821	AB21	VDD	VDD	P		Core power
822	AB22	VDD	VDD	P		Core power
823	AB23	VDD	VDD	P		Core power
824	AB24	VDD	VDD	P		Core power
825	AB25	VDD	VDD	P		Core power
826	AB26	VDD	VDD	P		Core power
827	AB27	VDD	VDD	P		Core power
828	AB28	VDD	VDD	P		Core power
829	AB29	VDD	VDD	P		Core power
830	AD14	VDD	VDD	P		Core power
831	AD15	VDD	VDD	P		Core power
832	AD16	VDD	VDD	P		Core power
833	AD17	VDD	VDD	P		Core power
834	AD18	VDD	VDD	P		Core power
835	AD19	VDD	VDD	P		Core power
836	AD20	VDD	VDD	P		Core power
837	AD21	VDD	VDD	P		Core power
838	AD22	VDD	VDD	P		Core power
839	AD23	VDD	VDD	P		Core power
840	AD24	VDD	VDD	P		Core power
841	AD25	VDD	VDD	P		Core power
842	AD26	VDD	VDD	P		Core power
843	AD27	VDD	VDD	P		Core power
844	AD28	VDD	VDD	P		Core power
845	AD29	VDD	VDD	P		Core power
846	AD30	VDD	VDD	P		Core power

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
847	AD31	VDD	VDD	P		Core power
848	AD32	VDD	VDD	P		Core power
849	AF26	VDD	VDD	P		Core power
850	AF27	VDD	VDD	P		Core power
851	AF30	VDD	VDD	P		Core power
852	AG28	VDD	VDD	P		Core power
853	T15	VDD	VDD	P		Core power
854	T16	VDD	VDD	P		Core power
855	T17	VDD	VDD	P		Core power
856	T18	VDD	VDD	P		Core power
857	T19	VDD	VDD	P		Core power
858	T20	VDD	VDD	P		Core power
859	T21	VDD	VDD	P		Core power
860	T22	VDD	VDD	P		Core power
861	T23	VDD	VDD	P		Core power
862	T24	VDD	VDD	P		Core power
863	T25	VDD	VDD	P		Core power
864	T26	VDD	VDD	P		Core power
865	T27	VDD	VDD	P		Core power
866	T28	VDD	VDD	P		Core power
867	T29	VDD	VDD	P		Core power
868	T30	VDD	VDD	P		Core power
869	V15	VDD	VDD	P		Core power
870	V16	VDD	VDD	P		Core power
871	V17	VDD	VDD	P		Core power
872	V18	VDD	VDD	P		Core power
873	V19	VDD	VDD	P		Core power
874	V20	VDD	VDD	P		Core power
875	V21	VDD	VDD	P		Core power
876	V22	VDD	VDD	P		Core power
877	V23	VDD	VDD	P		Core power
878	V24	VDD	VDD	P		Core power
879	V25	VDD	VDD	P		Core power

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
880	V26	VDD	VDD	P		Core power
881	V27	VDD	VDD	P		Core power
882	V28	VDD	VDD	P		Core power
883	Y16	VDD	VDD	P		Core power
884	Y17	VDD	VDD	P		Core power
885	Y18	VDD	VDD	P		Core power
886	Y19	VDD	VDD	P		Core power
887	Y20	VDD	VDD	P		Core power
888	Y21	VDD	VDD	P		Core power
889	Y22	VDD	VDD	P		Core power
890	Y23	VDD	VDD	P		Core power
891	Y24	VDD	VDD	P		Core power
892	Y25	VDD	VDD	P		Core power
893	Y26	VDD	VDD	P		Core power
894	Y27	VDD	VDD	P		Core power
895	Y28	VDD	VDD	P		Core power
896	Y29	VDD	VDD	P		Core power
897	AB14	VDD_DDR0_PLL	DDR 0	P		PLL power supply
898	AB15	VDD_DDR0_PLL	DDR 0	P		PLL power supply
899	AD13	VDD_DDR0_PLL	DDR 0	P		PLL power supply
900	V14	VDD_DDR0_PLL	DDR 0	P		PLL power supply
901	Y14	VDD_DDR0_PLL	DDR 0	P		PLL power supply
902	Y15	VDD_DDR0_PLL	DDR 0	P		PLL power supply
903	AG29	VDD_DDR1_PLL	DDR 1	P		PLL power supply
904	AG30	VDD_DDR1_PLL	DDR 1	P		PLL power supply
905	AH28	VDD_DDR1_PLL	DDR 1	P		PLL power supply
906	AH29	VDD_DDR1_PLL	DDR 1	P		PLL power supply
907	AH30	VDD_DDR1_PLL	DDR 1	P		PLL power supply
908	AJ29	VDD_DDR1_PLL	DDR 1	P		PLL power supply
909	AF21	**VDD_18**	VDD SM	P		SM power supply
910	F9	VDD_HDMI_09	HDMI	P		0.9 V analog power supply
911	F10	**VDD_HDMI_18**	HDMI	P		1.8V analog power supply
912	AN14	VDD_PCIE4_0_09	PCIe x4 0	P		PCIe PHY analog 0.95V

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
913	AP14	VDD_PCIE4_0_09	PCIe x4 0	P		PCIe PHY analog 0.95V
914	AR15	VDD_PCIE4_0_09	PCIe x4 0	P		PCIe PHY analog 0.95V
915	AR8	VDD_PCIE4_0_15	PCIe x4 0	P		PCIe PHY IO 1.5V
916	AM10	VDD_PCIE4_1_09	PCIe x4 1	P		PCIe PHY analog 0.95V
917	AN10	VDD_PCIE4_1_09	PCIe x4 1	P		PCIe PHY analog 0.95V
918	AN11	VDD_PCIE4_1_09	PCIe x4 1	P		PCIe PHY analog 0.95V
919	AP8	VDD_PCIE4_1_15	PCIe x4 1	P		PCIe PHY IO 1.5V
920	AF5	VDD_PCIE8_09	PCIe x8	P		PCIe PHY analog 0.95V
921	AH5	VDD_PCIE8_09	PCIe x8	P		PCIe PHY analog 0.95V
922	AM6	VDD_PCIE8_09	PCIe x8	P		PCIe PHY analog 0.95V
923	AP5	VDD_PCIE8_09	PCIe x8	P		PCIe PHY analog 0.95V
924	AP7	VDD_PCIE8_09	PCIe x8	P		PCIe PHY analog 0.95V
925	AR6	VDD_PCIE8_09	PCIe x8	P		PCIe PHY analog 0.95V
926	AJ10	VDD_PCIE8_15	PCIe x8	P		PCIe PHY IO 1.5V
927	AJ11	VDD_PCIE8_15	PCIe x8	P		PCIe PHY IO 1.5V
928	M27	VDD_PVT_18	PVT VDD	P		PVT sensor power
929	J26	VDD_SATA_09	SATA	P		SATA PHY analog and digital supply
930	K26	VDD_SATA_18	SATA	P		SATA PHY High-voltage power supply
931	J27	VDD_SATATX_09	SATA	P		SATA PHY transmit supply
932	P37	VDD_SD_33	SD Card	P		3.3V SD Supply
933	P38	VDD_SD_33	SD Card	P		3.3V SD Supply
934	F19	VDD_USB2_0_33	USB2 0	P		3.3V Analog Power Supply
935	J21	VDD_USB2_09	USB2 3	P		Digital Power Supply
936	K21	VDD_USB2_09	USB2 1	P		Digital Power Supply
937	G19	VDD_USB2_1_33	USB2 1	P		3.3V Analog Power Supply
938	G23	VDD_USB2_18	USB2 2	P		1.8V Analog Power Supply
939	H23	VDD_USB2_18	USB2 0	P		1.8V Analog Power Supply
940	H24	VDD_USB2_2_33	USB2 2	P		3.3V Analog Power Supply
941	H25	VDD_USB2_3_33	USB2 3	P		3.3V Analog Power Supply
942	A20	VDD_USB3_0_09	USB3 0	P		0.9 V PHY analog and digital high-speed supply

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
943	A24	VDD_USB3_1_09	USB3 1	P		0.9 V PHY analog and digital high-speed supply
944	K20	**VDD_USB3_33**	USB3 0	P		3.3V High supply for HS operation & SS operation
945	K23	**VDD_USB3_33**	USB3 1	P		3.3V High supply for HS operation & SS operation
946	L18	**VDD_USB3_33**	USB3 0	P		3.3V High supply for HS operation & SS operation
947	M22	**VDD_USB3_33**	USB3 1	P		3.3V High supply for HS operation & SS operation
948	D25	VDD_USB3TX_0_09	USB3 0	P		0.9 V PHY transmit supply
949	C21	VDD_USB3TX_1_09	USB3 1	P		0.9 V PHY transmit supply
950	E25	VDD_USB3VP_0_09	USB3 0	P		0.9 V PHY analog and digital SuperSpeed supply
951	D21	VDD_USB3VP_1_09	USB3 1	P		0.9 V PHY analog and digital SuperSpeed supply
952	F11	VDD_XG0_09	XGBE 0	P		XGbE PHY analog 0.95V
953	G11	VDD_XG0_09	XGBE 0	P		XGbE PHY analog 0.95V
954	H11	VDD_XG0_09	XGBE 0	P		XGbE PHY analog 0.95V
955	F13	VDD_XG0_15	XGBE 0	P		XGbE PHY IO 1.5V
956	K16	VDD_XG1_09	XGBE 1	P		XGbE PHY analog 0.95V
957	K17	VDD_XG1_09	XGBE 1	P		XGbE PHY analog 0.95V
958	L16	VDD_XG1_09	XGBE 1	P		XGbE PHY analog 0.95V
959	J17	VDD_XG1_15	XGBE 1	P		XGbE PHY IO 1.5V
960	AB30	**VDDIO_18**	VDDIO	P		IO power
961	AB31	**VDDIO_18**	VDDIO	P		IO power
962	AF14	**VDDIO_18**	VDDIO	P		IO power
963	AF15	**VDDIO_18**	VDDIO	P		IO power
964	AF16	**VDDIO_18**	VDDIO	P		IO power
965	AF17	**VDDIO_18**	VDDIO	P		IO power
966	AF18	**VDDIO_18**	VDDIO	P		IO power
967	AF19	**VDDIO_18**	VDDIO	P		IO power
968	J15	**VDDIO_18**	VDDIO	P		IO power
969	K15	**VDDIO_18**	VDDIO	P		IO power

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
970	V29	**VDDIO_18**	VDDIO	P		IO power
971	V30	**VDDIO_18**	VDDIO	P		IO power
972	V31	**VDDIO_18**	VDDIO	P		IO power
973	V32	**VDDIO_18**	VDDIO	P		IO power
974	Y30	**VDDIO_18**	VDDIO	P		IO power
975	Y31	**VDDIO_18**	LVDS	P		Output driver power, 1.8V
976	Y32	**VDDIO_18**	VDDIO	P		IO power
977	Y33	**VDDIO_18**	VDDIO	P		IO power
978	P16	VDDPLL_0_09	PLL POWER	P		PLL power
979	W31	VDDPLL_1_09	PLL POWER	P		PLL power
980	AF32	VDDPLL_2_09	PLL POWER	P		PLL power
981	AN19	VDDPLL_3_09	PLL POWER	P		PLL power
982	J14	VDDPLL_HDMI_09	PLL POWER	P		HDMI PLL power
983	AA10	VDDQ_DDR0	DDR 0	P		VDDQ voltage supply
984	AC7	VDDQ_DDR0	DDR 0	P		VDDQ voltage supply
985	K11	VDDQ_DDR0	DDR 0	P		VDDQ voltage supply
986	K9	VDDQ_DDR0	DDR 0	P		VDDQ voltage supply
987	L12	VDDQ_DDR0	DDR 0	P		VDDQ voltage supply
988	L15	VDDQ_DDR0	DDR 0	P		VDDQ voltage supply
989	N14	VDDQ_DDR0	DDR 0	P		VDDQ voltage supply
990	N15	VDDQ_DDR0	DDR 0	P		VDDQ voltage supply
991	P9	VDDQ_DDR0	DDR 0	P		VDDQ voltage supply
992	R14	VDDQ_DDR0	DDR 0	P		VDDQ voltage supply
993	R15	VDDQ_DDR0	DDR 0	P		VDDQ voltage supply
994	R7	VDDQ_DDR0	DDR 0	P		VDDQ voltage supply
995	R9	VDDQ_DDR0	DDR 0	P		VDDQ voltage supply
996	T13	VDDQ_DDR0	DDR 0	P		VDDQ voltage supply
997	U13	VDDQ_DDR0	DDR 0	P		VDDQ voltage supply
998	U9	VDDQ_DDR0	DDR 0	P		VDDQ voltage supply
999	V10	VDDQ_DDR0	DDR 0	P		VDDQ voltage supply
1000	V8	VDDQ_DDR0	DDR 0	P		VDDQ voltage supply
1001	Y12	VDDQ_DDR0	DDR 0	P		VDDQ voltage supply

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1002	AG34	VDDQ_DDR1	DDR 1	P		VDDQ voltage supply
1003	AG36	VDDQ_DDR1	DDR 1	P		VDDQ voltage supply
1004	AH31	VDDQ_DDR1	DDR 1	P		VDDQ voltage supply
1005	AH33	VDDQ_DDR1	DDR 1	P		VDDQ voltage supply
1006	AJ30	VDDQ_DDR1	DDR 1	P		VDDQ voltage supply
1007	AJ32	VDDQ_DDR1	DDR 1	P		VDDQ voltage supply
1008	AK21	VDDQ_DDR1	DDR 1	P		VDDQ voltage supply
1009	AL29	VDDQ_DDR1	DDR 1	P		VDDQ voltage supply
1010	AL33	VDDQ_DDR1	DDR 1	P		VDDQ voltage supply
1011	AM21	VDDQ_DDR1	DDR 1	P		VDDQ voltage supply
1012	AM32	VDDQ_DDR1	DDR 1	P		VDDQ voltage supply
1013	AN21	VDDQ_DDR1	DDR 1	P		VDDQ voltage supply
1014	AN30	VDDQ_DDR1	DDR 1	P		VDDQ voltage supply
1015	AP33	VDDQ_DDR1	DDR 1	P		VDDQ voltage supply
1016	AR28	VDDQ_DDR1	DDR 1	P		VDDQ voltage supply
1017	AT34	VDDQ_DDR1	DDR 1	P		VDDQ voltage supply
1018	AT36	VDDQ_DDR1	DDR 1	P		VDDQ voltage supply
1019	AT38	VDDQ_DDR1	DDR 1	P		VDDQ voltage supply
1020	AU31	VDDQ_DDR1	DDR 1	P		VDDQ voltage supply
1021	AW31	VDDQ_DDR1	DDR 1	P		VDDQ voltage supply
1022	A10	**VSS**	SD Card	G		Core ground
1023	A12	**VSS**	SD Card	G		Core ground
1024	A14	**VSS**	DDR 0	G		VSSQ ground
1025	A16	**VSS**	DDR 1	G		VSSQ ground
1026	A18	**VSS**	HDMI	G		Analog ground
1027	A22	**VSS**	VSS	G		Core ground
1028	A26	**VSS**	VSS	G		Core ground
1029	A28	**VSS**	VSS	G		Core ground
1030	A30	**VSS**	VSS	G		Core ground
1031	A8	**VSS**	VSS	G		Core ground
1032	AA12	**VSS**	VSS	G		Core ground
1033	AA14	**VSS**	VSS	G		Core ground
1034	AA15	**VSS**	VSS	G		Core ground

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1035	AA16	**VSS**	VSS	G		Core ground
1036	AA17	**VSS**	VSS	G		Core ground
1037	AA18	**VSS**	VSS	G		Core ground
1038	AA19	**VSS**	VSS	G		Core ground
1039	AA20	**VSS**	VSS	G		Core ground
1040	AA21	**VSS**	VSS	G		Core ground
1041	AA22	**VSS**	VSS	G		Core ground
1042	AA23	**VSS**	VSS	G		Core ground
1043	AA24	**VSS**	VSS	G		Core ground
1044	AA25	**VSS**	VSS	G		Core ground
1045	AA26	**VSS**	VSS	G		Core ground
1046	AA27	**VSS**	VSS	G		Core ground
1047	AA3	**VSS**	VSS	G		Core ground
1048	AA32	**VSS**	VSS	G		Core ground
1049	AA33	**VSS**	VSS	G		Core ground
1050	AA34	**VSS**	VSS	G		Core ground
1051	AA37	**VSS**	VSS	G		Core ground
1052	AA4	**VSS**	VSS	G		Core ground
1053	AA5	**VSS**	VSS	G		Core ground
1054	AA6	**VSS**	VSS	G		Core ground
1055	AA7	**VSS**	VSS	G		Core ground
1056	AB32	**VSS**	VSS	G		Core ground
1057	AB33	**VSS**	VSS	G		Core ground
1058	AB36	**VSS**	VSS	G		Core ground
1059	AB39	**VSS**	VSS	G		Core ground
1060	AC1	**VSS**	VSS	G		Core ground
1061	AC14	**VSS**	VSS	G		Core ground
1062	AC16	**VSS**	VSS	G		Core ground
1063	AC17	**VSS**	VSS	G		Core ground
1064	AC18	**VSS**	VSS	G		Core ground
1065	AC19	**VSS**	VSS	G		Core ground
1066	AC2	**VSS**	VSS	G		Core ground
1067	AC20	**VSS**	VSS	G		Core ground

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1068	AC21	**VSS**	VSS	G		Core ground
1069	AC22	**VSS**	VSS	G		Core ground
1070	AC23	**VSS**	VSS	G		Core ground
1071	AC24	**VSS**	VSS	G		Core ground
1072	AC25	**VSS**	VSS	G		Core ground
1073	AC26	**VSS**	VSS	G		Core ground
1074	AC27	**VSS**	VSS	G		Core ground
1075	AC3	**VSS**	VSS	G		Core ground
1076	AC32	**VSS**	VSS	G		Core ground
1077	AC33	**VSS**	VSS	G		Core ground
1078	AC34	**VSS**	VSS	G		Core ground
1079	AC37	**VSS**	VSS	G		Core ground
1080	AD1	**VSS**	VSS	G		Core ground
1081	AD11	**VSS**	VSS	G		Core ground
1082	AD36	**VSS**	VSS	G		Core ground
1083	AD39	**VSS**	VSS	G		Core ground
1084	AD4	**VSS**	VSS	G		Core ground
1085	AD9	**VSS**	VSS	G		Core ground
1086	AE13	**VSS**	VSS	G		Core ground
1087	AE14	**VSS**	VSS	G		Core ground
1088	AE15	**VSS**	VSS	G		Core ground
1089	AE16	**VSS**	VSS	G		Core ground
1090	AE17	**VSS**	VSS	G		Core ground
1091	AE18	**VSS**	VSS	G		Core ground
1092	AE19	**VSS**	VSS	G		Core ground
1093	AE20	**VSS**	VSS	G		Core ground
1094	AE21	**VSS**	VSS	G		Core ground
1095	AE22	**VSS**	VSS	G		Core ground
1096	AE23	**VSS**	VSS	G		Core ground
1097	AE24	**VSS**	VSS	G		Core ground
1098	AE25	**VSS**	VSS	G		Core ground
1099	AE26	**VSS**	VSS	G		Core ground
1100	AE27	**VSS**	VSS	G		Core ground

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1101	AE28	**VSS**	VSS	G		Core ground
1102	AE29	**VSS**	VSS	G		Core ground
1103	AE30	**VSS**	VSS	G		Core ground
1104	AE31	**VSS**	VSS	G		Core ground
1105	AE32	**VSS**	VSS	G		Core ground
1106	AE33	**VSS**	VSS	G		Core ground
1107	AE34	**VSS**	VSS	G		Core ground
1108	AE37	**VSS**	VSS	G		Core ground
1109	AE8	**VSS**	VSS	G		Core ground
1110	AF2	**VSS**	VSS	G		Core ground
1111	AF20	**VSS**	VSS	G		Core ground
1112	AF22	**VSS**	VSS	G		Core ground
1113	AF23	**VSS**	VSS	G		Core ground
1114	AF25	**VSS**	VSS	G		Core ground
1115	AF28	**VSS**	VSS	G		Core ground
1116	AF29	**VSS**	VSS	G		Core ground
1117	AF3	**VSS**	VSS	G		Core ground
1118	AF31	**VSS**	VSS	G		Core ground
1119	AF36	**VSS**	VSS	G		Core ground
1120	AF39	**VSS**	VSS	G		Core ground
1121	AG1	**VSS**	VSS	G		Core ground
1122	AG12	**VSS**	VSS	G		Core ground
1123	AG17	**VSS**	VSS	G		Core ground
1124	AG19	**VSS**	VSS	G		Core ground
1125	AG20	**VSS**	VSS	G		Core ground
1126	AG21	**VSS**	VSS	G		Core ground
1127	AG27	**VSS**	VSS	G		Core ground
1128	AG31	**VSS**	VSS	G		Core ground
1129	AG32	**VSS**	VSS	G		Core ground
1130	AG33	**VSS**	VSS	G		Core ground
1131	AG35	**VSS**	VSS	G		Core ground
1132	AG37	**VSS**	VSS	G		Core ground
1133	AG38	**VSS**	VSS	G		Core ground

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1134	AG39	**VSS**	VSS	G		Core ground
1135	AG4	**VSS**	VSS	G		Core ground
1136	AG5	**VSS**	VSS	G		Core ground
1137	AH10	**VSS**	VSS	G		Core ground
1138	AH15	**VSS**	VSS	G		Core ground
1139	AH16	**VSS**	VSS	G		Core ground
1140	AH21	**VSS**	VSS	G		Core ground
1141	AH24	**VSS**	VSS	G		Core ground
1142	AH25	**VSS**	VSS	G		Core ground
1143	AH32	**VSS**	VSS	G		Core ground
1144	AH6	**VSS**	VSS	G		Core ground
1145	AJ14	**VSS**	VSS	G		Core ground
1146	AJ17	**VSS**	VSS	G		Core ground
1147	AJ2	**VSS**	VSS	G		Core ground
1148	AJ21	**VSS**	VSS	G		Core ground
1149	AJ23	**VSS**	VSS	G		Core ground
1150	AJ26	**VSS**	VSS	G		Core ground
1151	AJ27	**VSS**	VSS	G		Core ground
1152	AJ28	**VSS**	VSS	G		Core ground
1153	AJ3	**VSS**	VSS	G		Core ground
1154	AJ31	**VSS**	VSS	G		Core ground
1155	AJ33	**VSS**	VSS	G		Core ground
1156	AJ39	**VSS**	VSS	G		Core ground
1157	AJ9	**VSS**	VSS	G		Core ground
1158	AK1	**VSS**	VSS	G		Core ground
1159	AK10	**VSS**	VSS	G		Core ground
1160	AK11	**VSS**	VSS	G		Core ground
1161	AK12	**VSS**	VSS	G		Core ground
1162	AK15	**VSS**	VSS	G		Core ground
1163	AK16	**VSS**	VSS	G		Core ground
1164	AK20	**VSS**	VSS	G		Core ground
1165	AK23	**VSS**	VSS	G		Core ground
1166	AK32	**VSS**	VSS	G		Core ground

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1167	AK33	**VSS**	VSS	G		Core ground
1168	AK36	**VSS**	VSS	G		Core ground
1169	AK4	**VSS**	VSS	G		Core ground
1170	AK5	**VSS**	VSS	G		Core ground
1171	AK7	**VSS**	VSS	G		Core ground
1172	AL13	**VSS**	VSS	G		Core ground
1173	AL14	**VSS**	VSS	G		Core ground
1174	AL16	**VSS**	VSS	G		Core ground
1175	AL17	**VSS**	VSS	G		Core ground
1176	AL21	**VSS**	VSS	G		Core ground
1177	AL24	**VSS**	VSS	G		Core ground
1178	AL26	**VSS**	VSS	G		Core ground
1179	AL28	**VSS**	VSS	G		Core ground
1180	AL30	**VSS**	VSS	G		Core ground
1181	AL7	**VSS**	VSS	G		Core ground
1182	AM11	**VSS**	VSS	G		Core ground
1183	AM14	**VSS**	VSS	G		Core ground
1184	AM2	**VSS**	VSS	G		Core ground
1185	AM29	**VSS**	VSS	G		Core ground
1186	AM3	**VSS**	VSS	G		Core ground
1187	AM33	**VSS**	VSS	G		Core ground
1188	AM39	**VSS**	VSS	G		Core ground
1189	AM5	**VSS**	VSS	G		Core ground
1190	AN1	**VSS**	VSS	G		Core ground
1191	AN12	**VSS**	VSS	G		Core ground
1192	AN15	**VSS**	VSS	G		Core ground
1193	AN16	**VSS**	VSS	G		Core ground
1194	AN18	**VSS**	VSS	G		Core ground
1195	AN23	**VSS**	VSS	G		Core ground
1196	AN25	**VSS**	VSS	G		Core ground
1197	AN27	**VSS**	VSS	G		Core ground
1198	AN33	**VSS**	VSS	G		Core ground
1199	AN36	**VSS**	VSS	G		Core ground

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1200	AN4	**VSS**	VSS	G		Core ground
1201	AN6	**VSS**	VSS	G		Core ground
1202	AN9	**VSS**	VSS	G		Core ground
1203	AP15	**VSS**	VSS	G		Core ground
1204	AP20	**VSS**	VSS	G		Core ground
1205	AP26	**VSS**	VSS	G		Core ground
1206	AP28	**VSS**	VSS	G		Core ground
1207	AR10	**VSS**	VSS	G		Core ground
1208	AR13	**VSS**	VSS	G		Core ground
1209	AR14	**VSS**	VSS	G		Core ground
1210	AR17	**VSS**	VSS	G		Core ground
1211	AR18	**VSS**	VSS	G		Core ground
1212	AR2	**VSS**	VSS	G		Core ground
1213	AR20	**VSS**	VSS	G		Core ground
1214	AR21	**VSS**	VSS	G		Core ground
1215	AR23	**VSS**	VSS	G		Core ground
1216	AR3	**VSS**	VSS	G		Core ground
1217	AR31	**VSS**	VSS	G		Core ground
1218	AR33	**VSS**	VSS	G		Core ground
1219	AR5	**VSS**	VSS	G		Core ground
1220	AT1	**VSS**	VSS	G		Core ground
1221	AT12	**VSS**	VSS	G		Core ground
1222	AT15	**VSS**	VSS	G		Core ground
1223	AT20	**VSS**	VSS	G		Core ground
1224	AT23	**VSS**	VSS	G		Core ground
1225	AT25	**VSS**	VSS	G		Core ground
1226	AT27	**VSS**	VSS	G		Core ground
1227	AT28	**VSS**	VSS	G		Core ground
1228	AT33	**VSS**	VSS	G		Core ground
1229	AT35	**VSS**	VSS	G		Core ground
1230	AT37	**VSS**	VSS	G		Core ground
1231	AT39	**VSS**	VSS	G		Core ground
1232	AT4	**VSS**	VSS	G		Core ground

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1233	AT7	**VSS**	VSS	G		Core ground
1234	AT9	**VSS**	VSS	G		Core ground
1235	AU11	**VSS**	VSS	G		Core ground
1236	AU14	**VSS**	VSS	G		Core ground
1237	AU17	**VSS**	VSS	G		Core ground
1238	AU18	**VSS**	VSS	G		Core ground
1239	AU20	**VSS**	VSS	G		Core ground
1240	AU22	**VSS**	VSS	G		Core ground
1241	AU3	**VSS**	VSS	G		Core ground
1242	AU6	**VSS**	VSS	G		Core ground
1243	AU7	**VSS**	VSS	G		Core ground
1244	AV1	**VSS**	VSS	G		Core ground
1245	AV12	**VSS**	VSS	G		Core ground
1246	AV15	**VSS**	VSS	G		Core ground
1247	AV16	**VSS**	VSS	G		Core ground
1248	AV19	**VSS**	VSS	G		Core ground
1249	AV20	**VSS**	VSS	G		Core ground
1250	AV31	**VSS**	VSS	G		Core ground
1251	AV4	**VSS**	VSS	G		Core ground
1252	AV9	**VSS**	VSS	G		Core ground
1253	AW11	**VSS**	VSS	G		Core ground
1254	AW14	**VSS**	VSS	G		Core ground
1255	AW17	**VSS**	VSS	G		Core ground
1256	AW20	**VSS**	VSS	G		Core ground
1257	AW26	**VSS**	VSS	G		Core ground
1258	AW29	**VSS**	VSS	G		Core ground
1259	AW3	**VSS**	VSS	G		Core ground
1260	AW35	**VSS**	VSS	G		Core ground
1261	AW38	**VSS**	VSS	G		Core ground
1262	AW6	**VSS**	VSS	G		Core ground
1263	AW8	**VSS**	VSS	G		Core ground
1264	B34	**VSS**	VSS	G		Core ground
1265	B38	**VSS**	VSS	G		Core ground

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1266	C11	**VSS**	VSS	G		Core ground
1267	C13	**VSS**	VSS	G		Core ground
1268	C15	**VSS**	VSS	G		Core ground
1269	C17	**VSS**	VSS	G		Core ground
1270	C19	**VSS**	VSS	G		Core ground
1271	C23	**VSS**	VSS	G		Core ground
1272	C25	**VSS**	VSS	G		Core ground
1273	C27	**VSS**	VSS	G		Core ground
1274	C29	**VSS**	VSS	G		Core ground
1275	C31	**VSS**	VSS	G		Core ground
1276	C36	**VSS**	VSS	G		Core ground
1277	C9	**VSS**	VSS	G		Core ground
1278	D12	**VSS**	VSS	G		Core ground
1279	D14	**VSS**	VSS	G		Core ground
1280	D16	**VSS**	VSS	G		Core ground
1281	D18	**VSS**	VSS	G		Core ground
1282	D22	**VSS**	VSS	G		Core ground
1283	D27	**VSS**	VSS	G		Core ground
1284	D28	**VSS**	VSS	G		Core ground
1285	D30	**VSS**	VSS	G		Core ground
1286	D38	**VSS**	VSS	G		Core ground
1287	D8	**VSS**	VSS	G		Core ground
1288	E20	**VSS**	VSS	G		Core ground
1289	E21	**VSS**	VSS	G		Core ground
1290	E24	**VSS**	VSS	G		Core ground
1291	E29	**VSS**	VSS	G		Core ground
1292	E32	**VSS**	VSS	G		Core ground
1293	E36	**VSS**	VSS	G		Core ground
1294	F15	**VSS**	VSS	G		Core ground
1295	F17	**VSS**	VSS	G		Core ground
1296	F23	**VSS**	VSS	G		Core ground
1297	F26	**VSS**	VSS	G		Core ground
1298	F31	**VSS**	VSS	G		Core ground

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1299	F34	**VSS**	VSS	G		Core ground
1300	F38	**VSS**	VSS	G		Core ground
1301	F4	**VSS**	VSS	G		Core ground
1302	F5	**VSS**	VSS	G		Core ground
1303	F6	**VSS**	VSS	G		Core ground
1304	F7	**VSS**	VSS	G		Core ground
1305	F8	**VSS**	VSS	G		Core ground
1306	G14	**VSS**	VSS	G		Core ground
1307	G16	**VSS**	VSS	G		Core ground
1308	G18	**VSS**	VSS	G		Core ground
1309	G22	**VSS**	VSS	G		Core ground
1310	G3	**VSS**	VSS	G		Core ground
1311	G30	**VSS**	VSS	G		Core ground
1312	G34	**VSS**	VSS	G		Core ground
1313	H21	**VSS**	VSS	G		Core ground
1314	H27	**VSS**	VSS	G		Core ground
1315	H31	**VSS**	VSS	G		Core ground
1316	H4	**VSS**	VSS	G		Core ground
1317	H7	**VSS**	VSS	G		Core ground
1318	H8	**VSS**	VSS	G		Core ground
1319	J1	**VSS**	VSS	G		Core ground
1320	J2	**VSS**	VSS	G		Core ground
1321	J25	**VSS**	VSS	G		Core ground
1322	J28	**VSS**	VSS	G		Core ground
1323	J29	**VSS**	VSS	G		Core ground
1324	J30	**VSS**	VSS	G		Core ground
1325	J31	**VSS**	VSS	G		Core ground
1326	J32	**VSS**	VSS	G		Core ground
1327	K29	**VSS**	VSS	G		Core ground
1328	K33	**VSS**	VSS	G		Core ground
1329	K37	**VSS**	VSS	G		Core ground
1330	K4	**VSS**	VSS	G		Core ground
1331	K5	**VSS**	VSS	G		Core ground

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1332	K6	VSS	VSS	G		Core ground
1333	L20	VSS	VSS	G		Core ground
1334	L21	VSS	VSS	G		Core ground
1335	L22	VSS	VSS	G		Core ground
1336	L25	VSS	VSS	G		Core ground
1337	L26	VSS	VSS	G		Core ground
1338	L27	VSS	VSS	G		Core ground
1339	L28	VSS	VSS	G		Core ground
1340	L29	VSS	VSS	G		Core ground
1341	L3	VSS	VSS	G		Core ground
1342	L35	VSS	VSS	G		Core ground
1343	L39	VSS	VSS	G		Core ground
1344	M10	VSS	VSS	G		Core ground
1345	M14	VSS	VSS	G		Core ground
1346	M15	VSS	VSS	G		Core ground
1347	M18	VSS	VSS	G		Core ground
1348	M24	VSS	VSS	G		Core ground
1349	M36	VSS	VSS	G		Core ground
1350	M4	VSS	VSS	G		Core ground
1351	M7	VSS	VSS	G		Core ground
1352	N1	VSS	VSS	G		Core ground
1353	N11	VSS	VSS	G		Core ground
1354	N2	VSS	VSS	G		Core ground
1355	N28	VSS	VSS	G		Core ground
1356	N35	VSS	VSS	G		Core ground
1357	N9	VSS	VSS	G		Core ground
1358	P12	VSS	VSS	G		Core ground
1359	P25	VSS	VSS	G		Core ground
1360	P26	VSS	VSS	G		Core ground
1361	P27	VSS	VSS	G		Core ground
1362	P28	VSS	VSS	G		Core ground
1363	P29	VSS	VSS	G		Core ground
1364	P30	VSS	VSS	G		Core ground

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1365	P35	VSS	VSS	G		Core ground
1366	P39	VSS	VSS	G		Core ground
1367	P4	VSS	VSS	G		Core ground
1368	P5	VSS	VSS	G		Core ground
1369	P7	VSS	VSS	G		Core ground
1370	R10	VSS	VSS	G		Core ground
1371	R13	VSS	VSS	G		Core ground
1372	R17	VSS	VSS	G		Core ground
1373	R23	VSS	VSS	G		Core ground
1374	R24	VSS	VSS	G		Core ground
1375	R25	VSS	VSS	G		Core ground
1376	R26	VSS	VSS	G		Core ground
1377	R27	VSS	VSS	G		Core ground
1378	R37	VSS	VSS	G		Core ground
1379	R4	VSS	VSS	G		Core ground
1380	T11	VSS	VSS	G		Core ground
1381	T31	VSS	VSS	G		Core ground
1382	T36	VSS	VSS	G		Core ground
1383	T39	VSS	VSS	G		Core ground
1384	T8	VSS	VSS	G		Core ground
1385	U14	VSS	VSS	G		Core ground
1386	U15	VSS	VSS	G		Core ground
1387	U16	VSS	VSS	G		Core ground
1388	U17	VSS	VSS	G		Core ground
1389	U18	VSS	VSS	G		Core ground
1390	U19	VSS	VSS	G		Core ground
1391	U20	VSS	VSS	G		Core ground
1392	U21	VSS	VSS	G		Core ground
1393	U22	VSS	VSS	G		Core ground
1394	U23	VSS	VSS	G		Core ground
1395	U24	VSS	VSS	G		Core ground
1396	U25	VSS	VSS	G		Core ground
1397	U26	VSS	VSS	G		Core ground

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1398	U27	**VSS**	VSS	G		Core ground
1399	U3	**VSS**	VSS	G		Core ground
1400	U32	**VSS**	VSS	G		Core ground
1401	U33	**VSS**	VSS	G		Core ground
1402	U34	**VSS**	VSS	G		Core ground
1403	U37	**VSS**	VSS	G		Core ground
1404	U4	**VSS**	VSS	G		Core ground
1405	U6	**VSS**	VSS	G		Core ground
1406	V36	**VSS**	PCIe x4 0	G		PCIe ground
1407	V39	**VSS**	PCIe x4 0	G		PCIe ground
1408	W1	**VSS**	PCIe x4 0	G		PCIe ground
1409	W11	**VSS**	PCIe x4 1	G		PCIe ground
1410	W13	**VSS**	PCIe x4 1	G		PCIe ground
1411	W14	**VSS**	PCIe x4 1	G		PCIe ground
1412	W15	**VSS**	PCIe x8	G		PCIe ground
1413	W16	**VSS**	PCIe x8	G		PCIe ground
1414	W17	**VSS**	PCIe x8	G		PCIe ground
1415	W18	**VSS**	PCIe x8	G		PCIe ground
1416	W19	**VSS**	PCIe x8	G		PCIe ground
1417	W2	**VSS**	PCIe x8	G		PCIe ground
1418	W20	**VSS**	SATA	G		SATA GD (PHY ground)
1419	W21	**VSS**	USB2 0	G		Ground Supply
1420	W22	**VSS**	USB2 0	G		Ground Supply
1421	W23	**VSS**	USB2 1	G		Ground Supply
1422	W24	**VSS**	USB2 2	G		Ground Supply
1423	W25	**VSS**	USB2 3	G		Ground Supply
1424	W26	**VSS**	USB3 0	G		PHY ground
1425	W27	**VSS**	USB3 1	G		PHY ground
1426	W3	**VSS**	USB3 0	G		PHY ground
1427	W33	**VSS**	USB3 1	G		PHY ground
1428	W34	**VSS**	XGBE 0	G		XGbE ground
1429	W37	**VSS**	XGBE 0	G		XGbE ground
1430	W7	**VSS**	XGBE 0	G		XGbE ground

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1431	Y36	**VSS**	XGBE 1	G		XGbE ground
1432	Y39	**VSS**	XGBE 1	G		XGbE ground
1433	Y9	**VSS**	XGBE 1	G		XGbE ground
1434	M28	**VSS_PVT**	PVT VSS	G		PVT sensor ground
1435	A4	**VSSIO**	VSSIO	G		IO ground
1436	AA28	**VSSIO**	VSSIO	G		IO ground
1437	AA29	**VSSIO**	VSSIO	G		IO ground
1438	AA30	**VSSIO**	VSSIO	G		IO ground
1439	AA31	**VSSIO**	VSSIO	G		IO ground
1440	AC15	**VSSIO**	VSSIO	G		IO ground
1441	AC28	**VSSIO**	VSSIO	G		IO ground
1442	AC29	**VSSIO**	VSSIO	G		IO ground
1443	AC30	**VSSIO**	VSSIO	G		IO ground
1444	AC31	**VSSIO**	VSSIO	G		IO ground
1445	AD10	**VSSIO**	VSSIO	G		IO ground
1446	AD12	**VSSIO**	VSSIO	G		IO ground
1447	AE7	**VSSIO**	VSSIO	G		IO ground
1448	AF8	**VSSIO**	VSSIO	G		IO ground
1449	AG9	**VSSIO**	VSSIO	G		IO ground
1450	B4	**VSSIO**	VSSIO	G		IO ground
1451	D1	**VSSIO**	VSSIO	G		IO ground
1452	D3	**VSSIO**	VSSIO	G		IO ground
1453	H35	**VSSIO**	VSSIO	G		IO ground
1454	J33	**VSSIO**	VSSIO	G		IO ground
1455	J37	**VSSIO**	VSSIO	G		IO ground
1456	L30	**VSSIO**	VSSIO	G		IO ground
1457	M32	**VSSIO**	VSSIO	G		IO ground
1458	N29	**VSSIO**	VSSIO	G		IO ground
1459	P15	**VSSIO**	VSSIO	G		IO ground
1460	P31	**VSSIO**	VSSIO	G		IO ground
1461	R18	**VSSIO**	VSSIO	G		IO ground
1462	R19	**VSSIO**	VSSIO	G		IO ground
1463	R20	**VSSIO**	VSSIO	G		IO ground

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1464	R21	VSSIO	VSSIO	G		IO ground
1465	R32	VSSIO	VSSIO	G		IO ground
1466	U28	VSSIO	VSSIO	G		IO ground
1467	U29	VSSIO	VSSIO	G		IO ground
1468	U30	VSSIO	VSSIO	G		IO ground
1469	U31	VSSIO	VSSIO	G		IO ground
1470	W28	VSSIO	VSSIO	G		IO ground
1471	W29	VSSIO	VSSIO	G		IO ground
1472	W30	VSSIO	VSSIO	G		IO ground
1473	P17	VSSPLL_0	PLL GROUND	G		PLL ground
1474	W32	VSSPLL_1	PLL GROUND	G		PLL ground
1475	AF33	VSSPLL_2	PLL GROUND	G		PLL ground
1476	AP18	VSSPLL_3	PLL GROUND	G		PLL ground
1477	K14	VSSPLL_HDMI	PLL GROUND	G		HDMI PLL ground
1478	H14	XG0_AMON	XGBE 0	O	VDD_XG0_15	Analog monitor bump
1479	G13	XG0_DMON	XGBE 0	O	VDD_XG0_09	Differential digital monitor bump
1480	H13	XG0_DMONB	XGBE 0	O	VDD_XG0_09	Differential digital monitor bump
1481	H15	XG0_RBIAS	XGBE 0	IO	VDD_XG0_15	Bias resistor bump
1482	H12	XG0_REF_CLKN	XGBE 0	I	VDD_XG0_15	Differential reference clocks from pads
1483	G12	XG0_REF_CLKP	XGBE 0	I	VDD_XG0_15	Differential reference clocks from pads
1484	A11	XG0_RXN[0]	XGBE 0	I	VDD_XG0_15	Receive data diff pair
1485	B12	XG0_RXN[1]	XGBE 0	I	VDD_XG0_15	Receive data diff pair
1486	A13	XG0_RXN[2]	XGBE 0	I	VDD_XG0_15	Receive data diff pair
1487	B14	XG0_RXN[3]	XGBE 0	I	VDD_XG0_15	Receive data diff pair
1488	B11	XG0_RXP[0]	XGBE 0	I	VDD_XG0_15	Receive data diff pair
1489	C12	XG0_RXP[1]	XGBE 0	I	VDD_XG0_15	Receive data diff pair
1490	B13	XG0_RXP[2]	XGBE 0	I	VDD_XG0_15	Receive data diff pair
1491	C14	XG0_RXP[3]	XGBE 0	I	VDD_XG0_15	Receive data diff pair
1492	D11	XG0_TXN[0]	XGBE 0	O	VDD_XG0_15	Transmit data diff pair
1493	E12	XG0_TXN[1]	XGBE 0	O	VDD_XG0_15	Transmit data diff pair
1494	D13	XG0_TXN[2]	XGBE 0	O	VDD_XG0_15	Transmit data diff pair
1495	E14	XG0_TXN[3]	XGBE 0	O	VDD_XG0_15	Transmit data diff pair

Table 5-1 Pinout List (continued)

№	Pin ID	Package Pin Name	Group	Type	Power Supply	Description
1496	E11	XG0_TXP[0]	XGBE 0	O	VDD_XG0_15	Transmit data diff pair
1497	F12	XG0_TXP[1]	XGBE 0	O	VDD_XG0_15	Transmit data diff pair
1498	E13	XG0_TXP[2]	XGBE 0	O	VDD_XG0_15	Transmit data diff pair
1499	F14	XG0_TXP[3]	XGBE 0	O	VDD_XG0_15	Transmit data diff pair
1500	H18	XG1_AMON	XGBE 1	O	VDD_XG1_15	Analog monitor bump
1501	G17	XG1_DMON	XGBE 1	O	VDD_XG1_09	Differential digital monitor bump
1502	H17	XG1_DMONB	XGBE 1	O	VDD_XG1_09	Differential digital monitor bump
1503	G15	XG1_RBIAS	XGBE 1	IO	VDD_XG1_15	Bias resistor bump
1504	J16	XG1_REF_CLKN	XGBE 1	I	VDD_XG1_15	Differential reference clocks from pads
1505	H16	XG1_REF_CLKP	XGBE 1	I	VDD_XG1_15	Differential reference clocks from pads
1506	B18	XG1_RXN[0]	XGBE 1	I	VDD_XG1_15	Receive data diff pair
1507	A17	XG1_RXN[1]	XGBE 1	I	VDD_XG1_15	Receive data diff pair
1508	B16	XG1_RXN[2]	XGBE 1	I	VDD_XG1_15	Receive data diff pair
1509	A15	XG1_RXN[3]	XGBE 1	I	VDD_XG1_15	Receive data diff pair
1510	C18	XG1_RXP[0]	XGBE 1	I	VDD_XG1_15	Receive data diff pair
1511	B17	XG1_RXP[1]	XGBE 1	I	VDD_XG1_15	Receive data diff pair
1512	C16	XG1_RXP[2]	XGBE 1	I	VDD_XG1_15	Receive data diff pair
1513	B15	XG1_RXP[3]	XGBE 1	I	VDD_XG1_15	Receive data diff pair
1514	E18	XG1_TXN[0]	XGBE 1	O	VDD_XG1_15	Transmit data diff pair
1515	D17	XG1_TXN[1]	XGBE 1	O	VDD_XG1_15	Transmit data diff pair
1516	E16	XG1_TXN[2]	XGBE 1	O	VDD_XG1_15	Transmit data diff pair
1517	D15	XG1_TXN[3]	XGBE 1	O	VDD_XG1_15	Transmit data diff pair
1518	F18	XG1_TXP[0]	XGBE 1	O	VDD_XG1_15	Transmit data diff pair
1519	E17	XG1_TXP[1]	XGBE 1	O	VDD_XG1_15	Transmit data diff pair
1520	F16	XG1_TXP[2]	XGBE 1	O	VDD_XG1_15	Transmit data diff pair
1521	E15	XG1_TXP[3]	XGBE 1	O	VDD_XG1_15	Transmit data diff pair

5.2   Package Ball Map

The diagrams below show pinout from the top view of the package.

Power & Ground

	VDD
	VDD 0.9V, 0.95V
	VDD 1.2V, 1.5V
	VDD 1.8V
	VDD 3.3V
	VDD DDR PLL
	VSS
	VSSIO
	VSSPLL

System Control & Debug

	System Control
	System Debug

Memory

	DDR0
	DDR1

High Speed Peripherals

	PCIE x8
	PCIE x4_0, PCIE x4_1
	USB 3.0/2.0
	USB 2.0
	SATA_0, SATA_1
	XGMAC0, XGMAC1
	GMAC0, GMAC1

Low Speed Peripherals

	eMMC/SD
	GPIO*32
	UART_1
	SPI_1
	eSPI
	I2C_1
	SMBus_1

Audio & Video

	LVDS
	HDMI
	I2S

Figure 5-1 Ball Map

5.2.1 Power and Ground
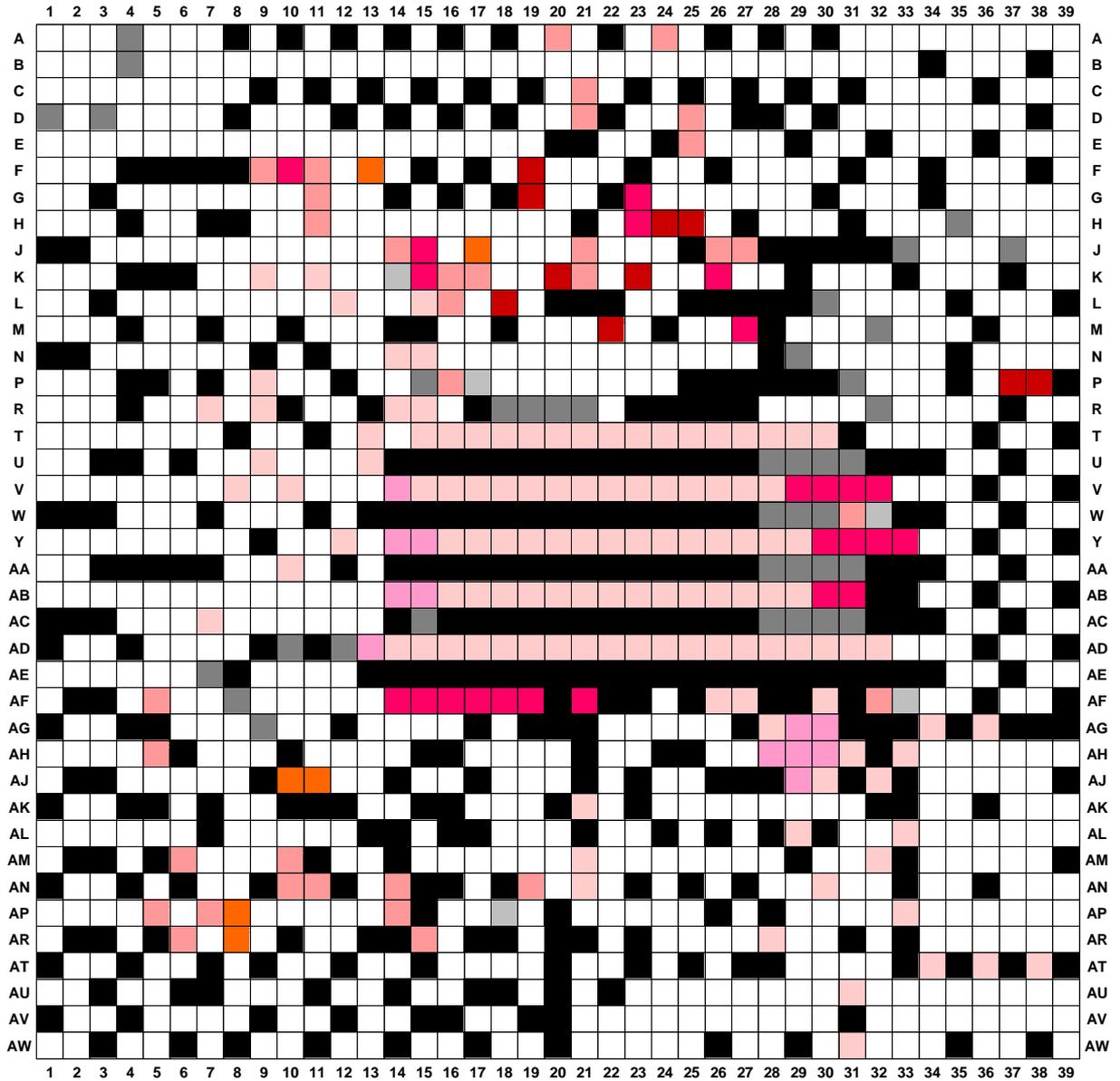
	VDD
	VDD 0.9V, 0.95V
	VDD 1.2V, 1.5V
	VDD 1.8V
	VDD 3.3V
	VDD DDR PLL
	VSS
	VSSIO
	VSSPLL

Figure 5-2 Power and Ground Pin Placement

5.2.2 High Speed Peripherals
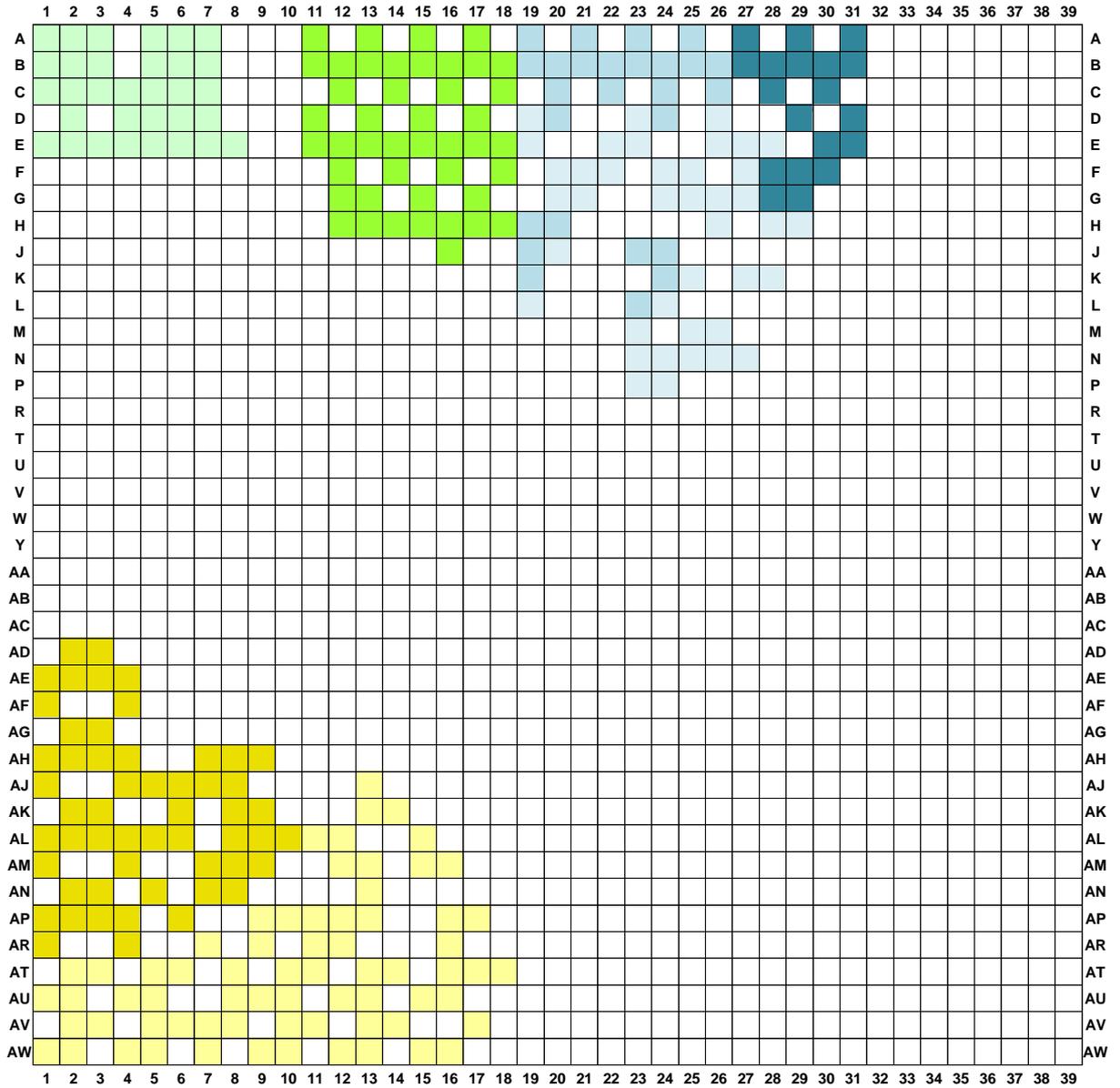
	PCIE x8
	PCIE x4_0, PCIE x4_1
	USB 3.0/2.0
	USB 2.0
	SATA_0, SATA_1
	XGMAC0, XGMAC1
	GMAC0, GMAC1

Figure 5-3 High Speed Peripherals Pin Placement

5.2.3 Low Speed Peripherals
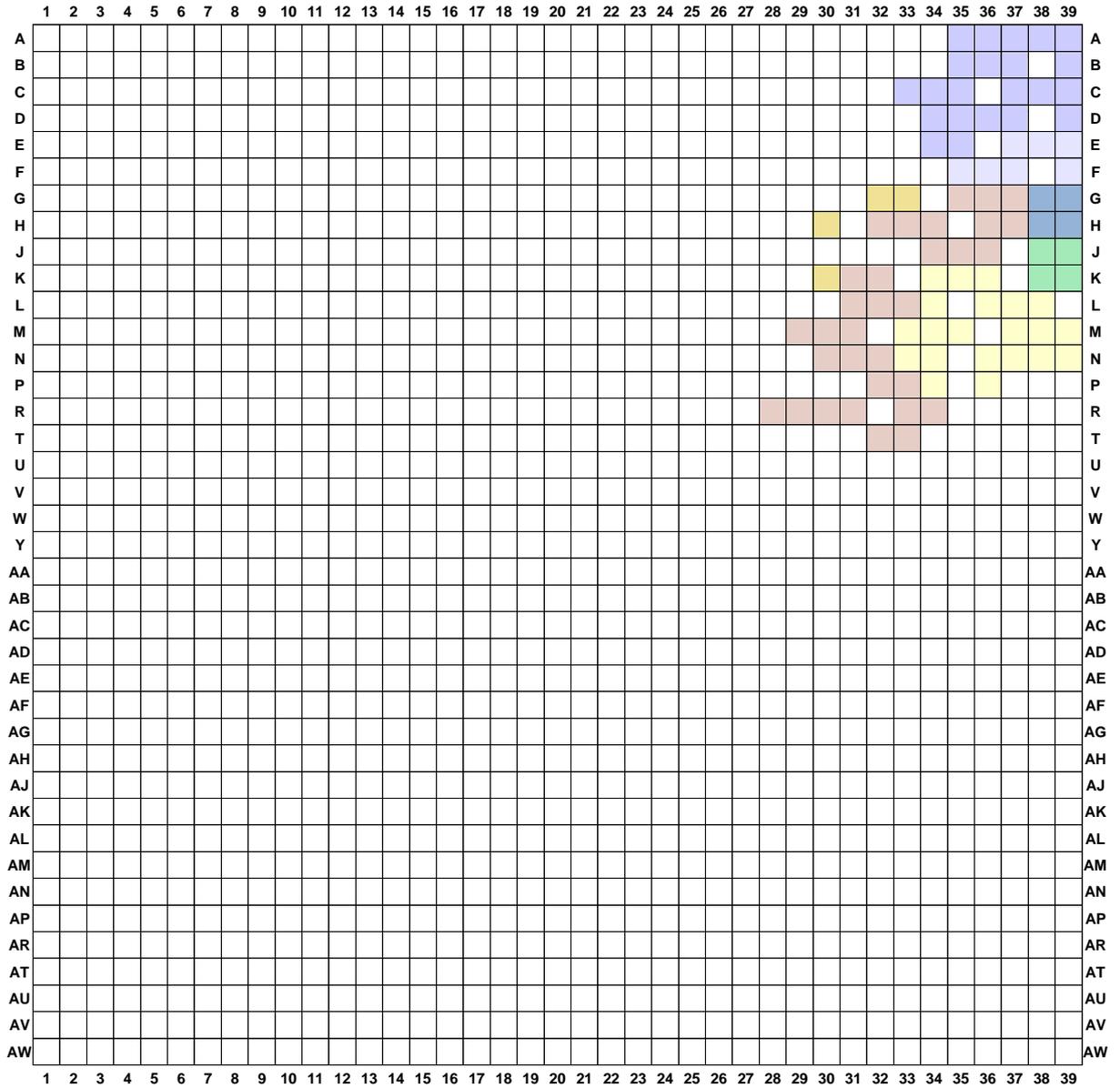
	eMMC/SD
	GPIO*32
	UART_1, UART_2
	SPI
	eSPI
	I2C_1, I2C_2
	SMBus_1, SMBus_2

Figure 5-4 Low Speed Peripherals Pin Placement

5.2.4 Memory

	DDR0
	DDR1
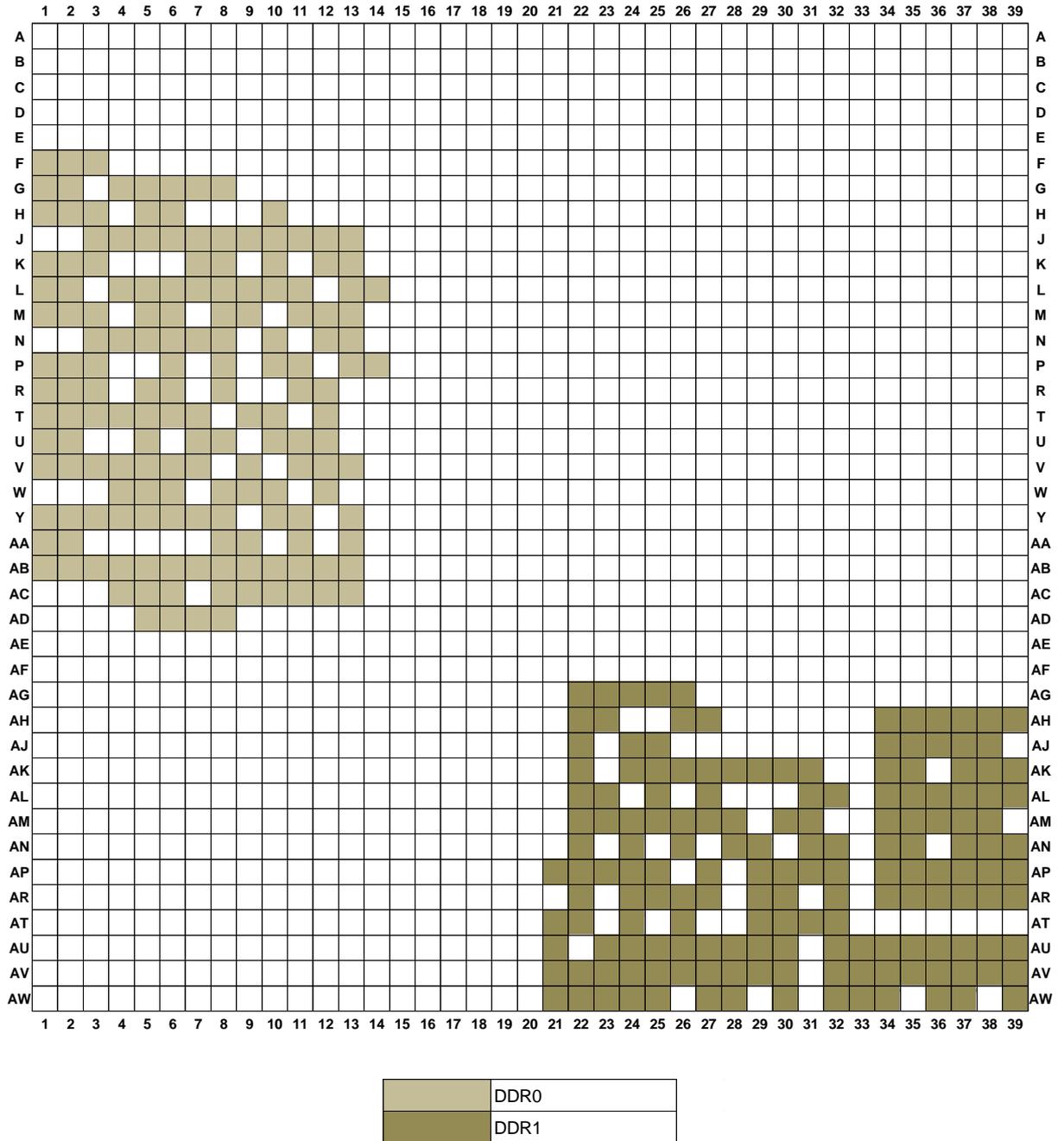
Figure 5-5 Memory Pin Placement

5.2.5 Audio and Video
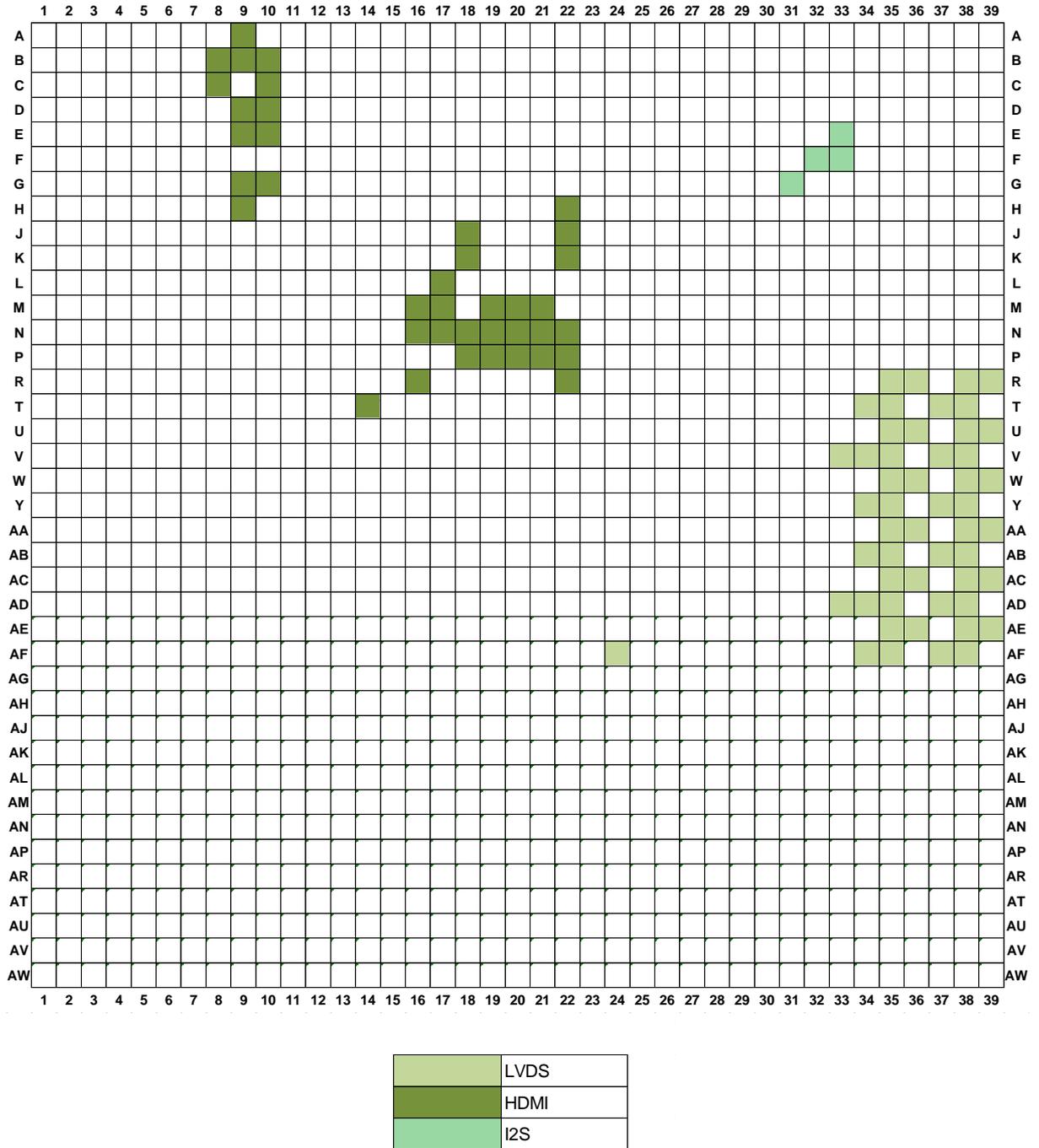
Figure 5-6 Audio and Video Pin Placement

5.2.6 System Control and Debug
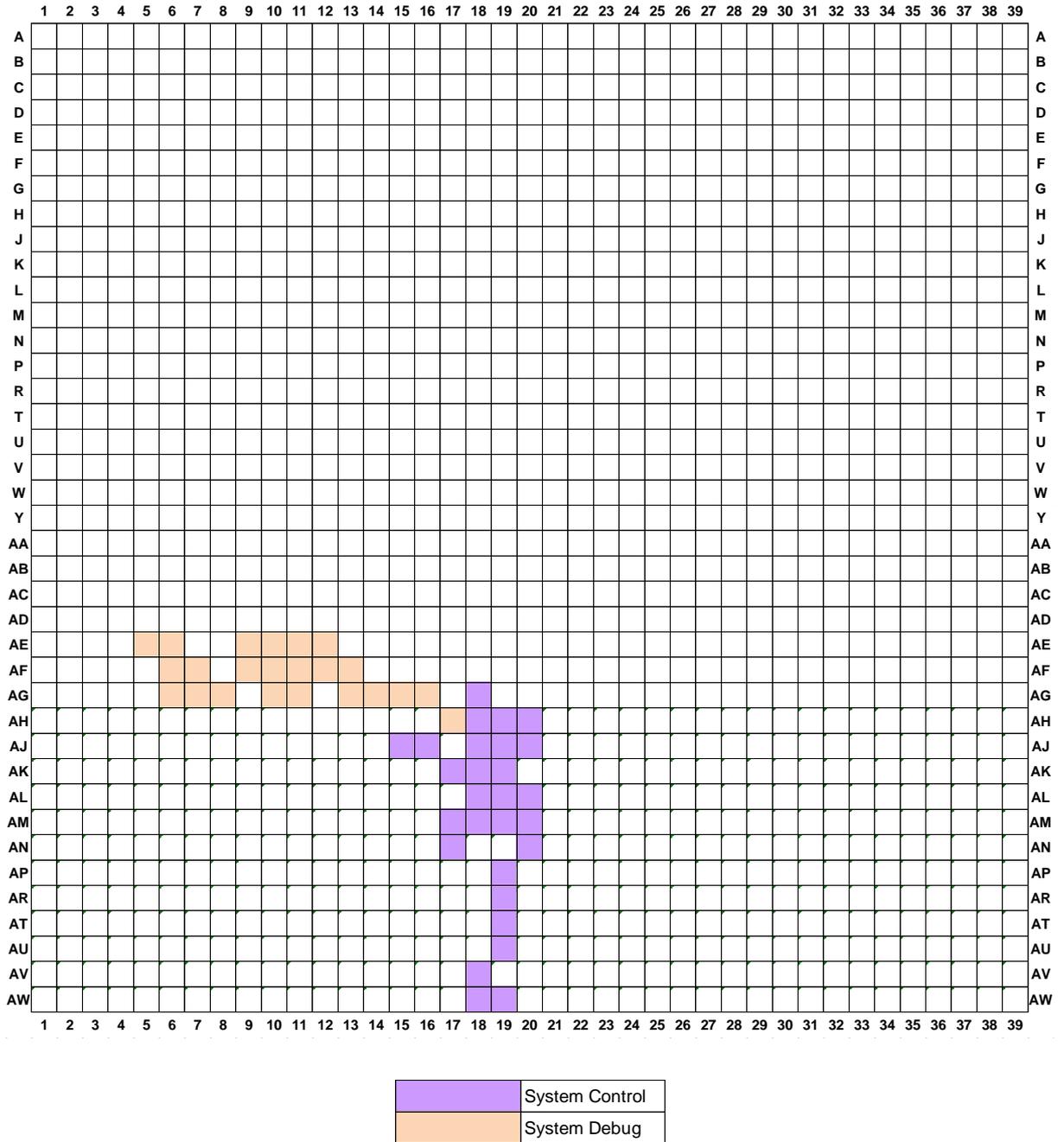
Figure 5-7 System Control and Debug Pin Placement

6 Package Information

6.1 FCBGA-1521 Package

SoC is mounted into FCBGA-1521 package. Main package parameters are shown it the figures and table below.
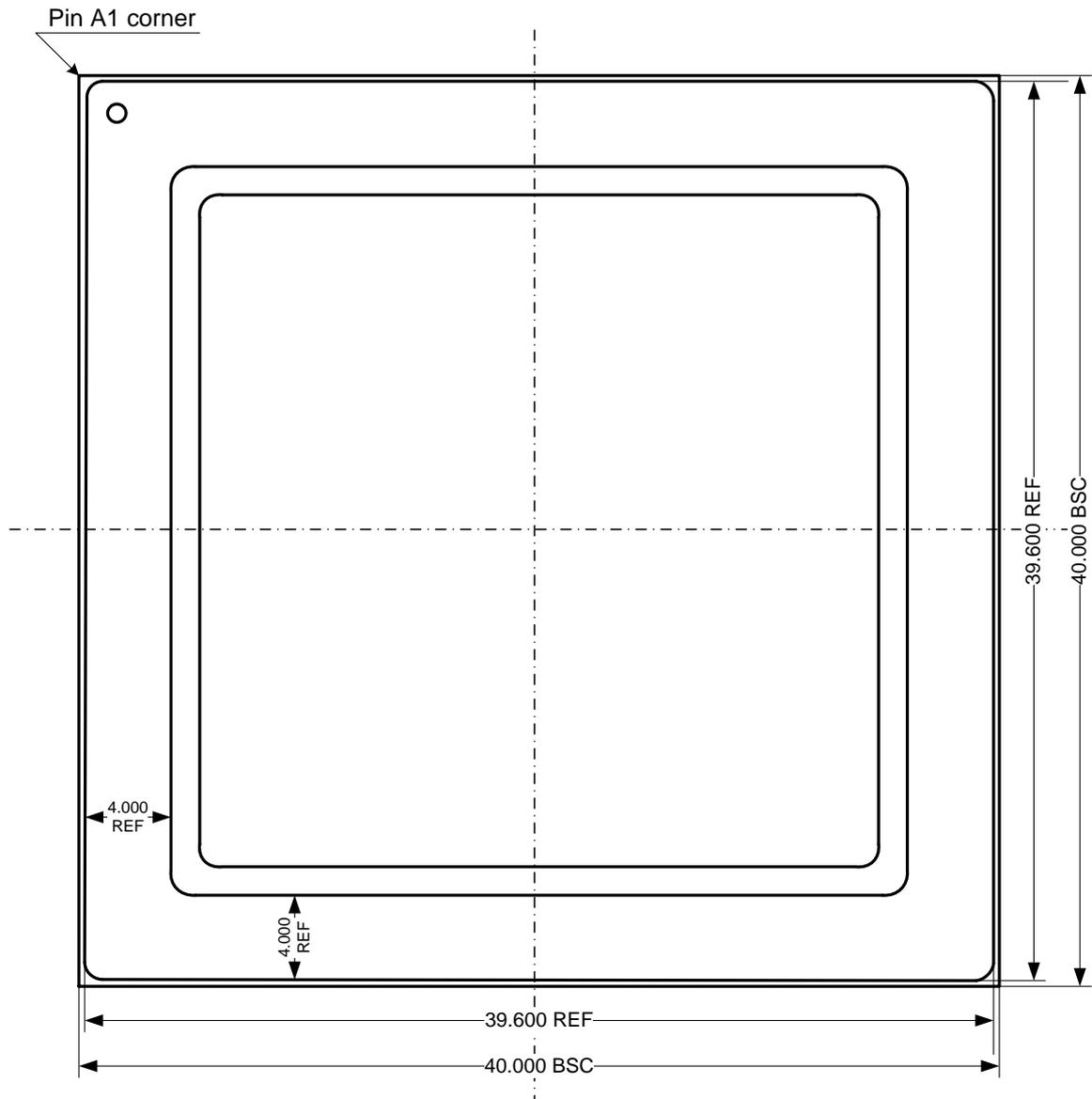
Figure 6-1 SoC package. Top View
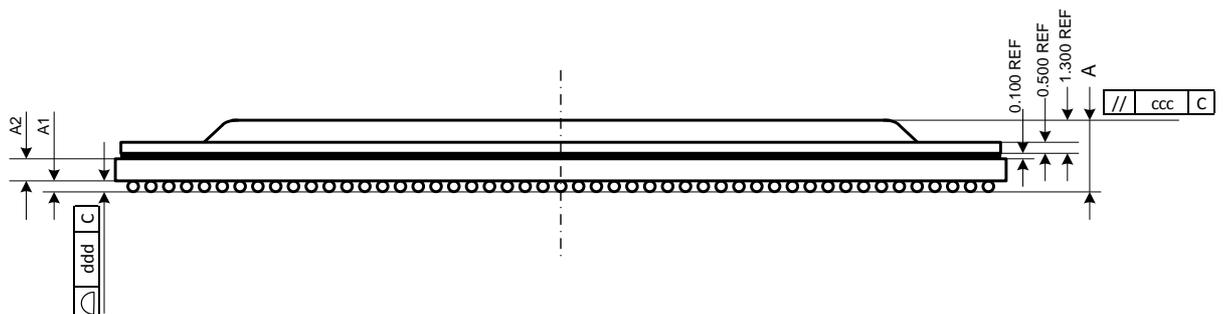
Figure 6-2 SoC package. Side View
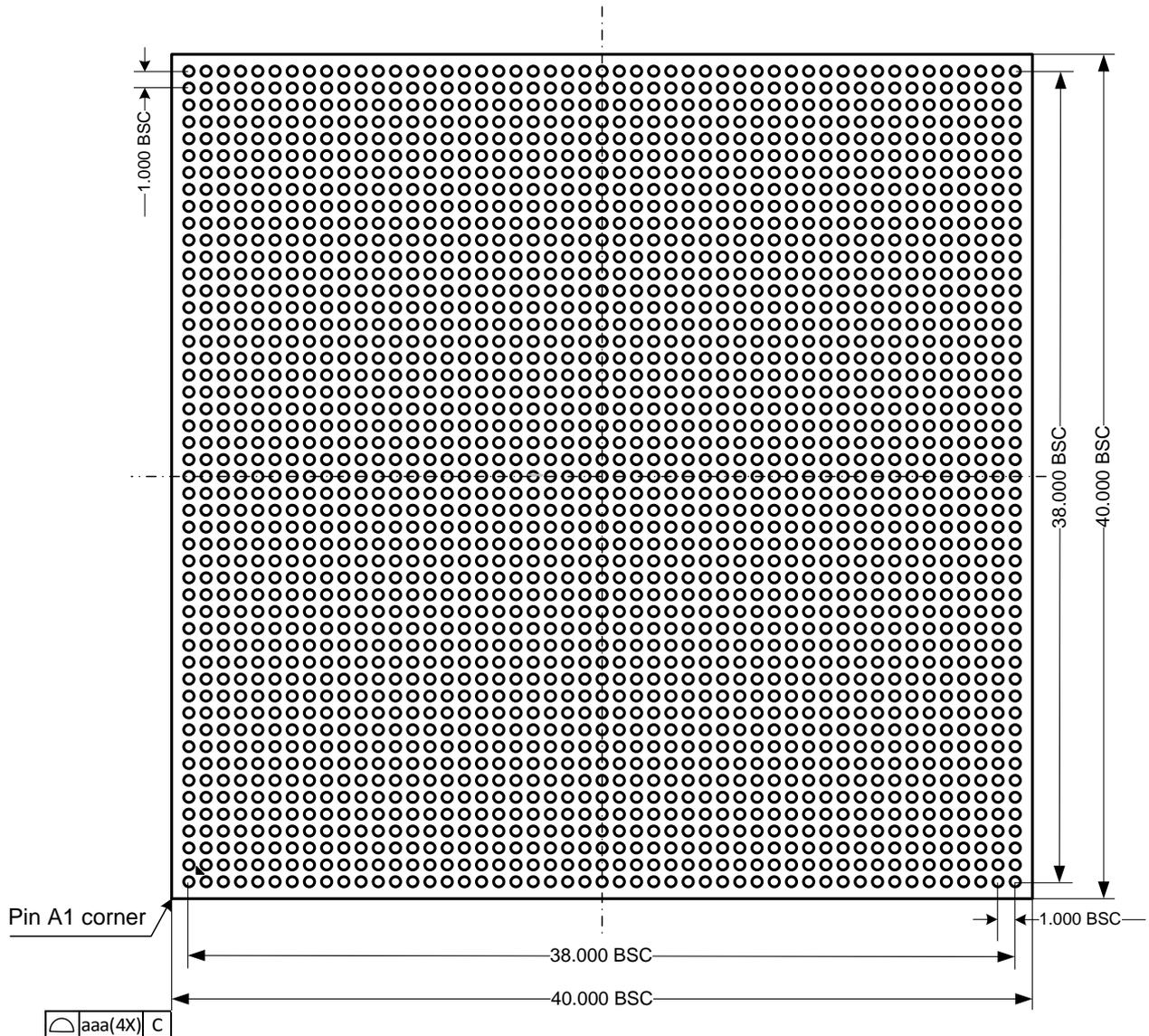
Figure 6-3 SoC package. Bottom View

The following table shows the package parameters.

Table 6-1 Package Parameters

Dimension	Symbol	Value		
		Min.	Nom.	Max.
Total thickness	A	2.676	2.976	3.176
Stand off	A1	0.400	-	0.600
Substrate thickness	A2	1.026 REF		
Body size		40.000 BSC		
		40.000 BSC		
Ball diameter		0.600		
Ball width		0.500	-	0.700
Ball pitch		1.000 BSC		

Table 6-1 Package Parameters (continued)

Dimension	Symbol	Value
Ball count		1521
Edge ball center to center		38.000 BSC
		38.000 BSC
Package edge tolerance	aaa	0.200
Top parallelism	ccc	0.350
Coplanarity	ddd	0.200

6.2   Soldering

SoC mounting to PCB should be accomplished in accordance to the soldering profile recommended for Pb-Free packages. Corresponding modes and temperatures are described in the following table and figure.

Table 6-2 Temperature Profile for SoC Soldering to PCB

Profile Feature	Description	Temperature	Duration
A	Preheat stage	150-200°C	60-120 seconds
B	Melting stage	>217°C	60-150 seconds
C	Ramp-up rate	3°C/sec max.	
D	Peak temperature	245°C	
E	Soldering stage	>240°C	30 seconds min.
F	Time from room temperature to peak temperature		< 8 minutes max.
G	Ramp-down rate	6°C/sec max.	

All temperatures refer to topside of the package, measured on the package body surface.
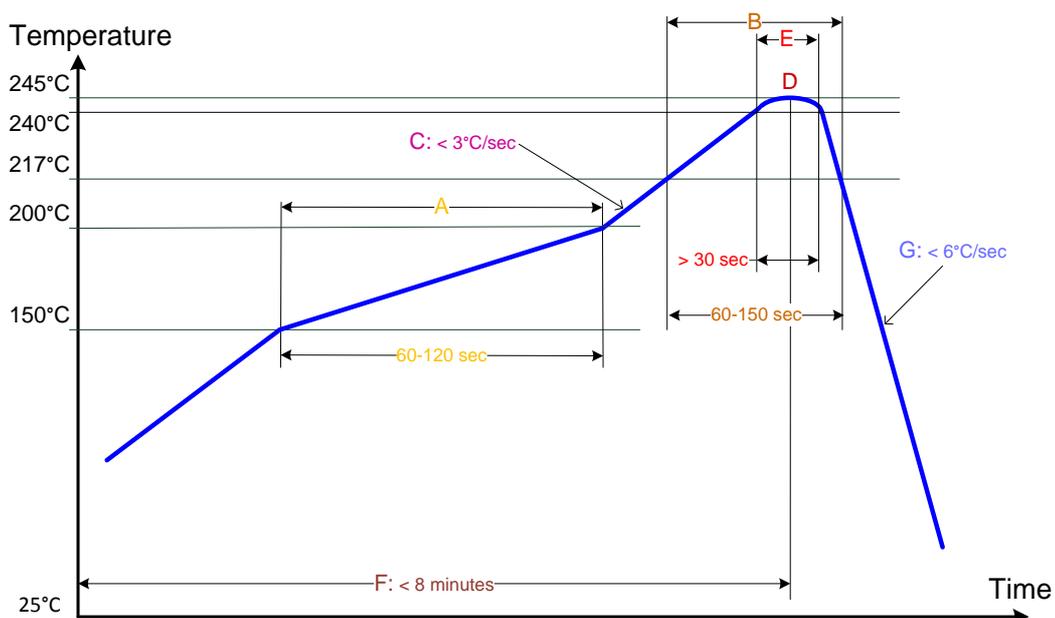
Figure 6-4 Soldering Profile

7 Ordering Information

BE-M1000 is orderable part number. Designation of each field in the part number is shown in a table below.

Table 7-1 Ordering information

BE	-	M	1	0	0	0
Baikal Electronics	field delimiter	product line	generation	modification	reserved field	packaging

BE-M1000 is the first product in BE-M product line.

To order BE-M1000 please contact Baikal Electronics company referred in the next page.

Contact Info

Baikal Electronics: https://www.baikalelectronics.com/

Head Office: https://www.baikalelectronics.com/contacts/

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Phone: +7 495 221-39-47

Revision History

Revision	Date	Substantive change(s)
0.65	02.07.2019	Initial version
0.70	01.11.2019	The Section 4 has some corrections: • Correction of power-up order • The information about power-up sequence
0.72	11.12.2019	The Section 4 has the information about power-down. In Section 5 the information about pins AM19 and AL18 is changed
0.73	16.12.2019	The following pins changed pin IDs: DDR0_DQ[18], DDR0_DQ[19], DDR0_DQ[20], DDR0_DQ[21], DDR0_DQ[26], DDR0_DQ[27], DDR0_DQ[28], DDR0_DQ[29], DDR0_DQ[41], DDR0_DQ[44], DDR0_DQ[48], DDR0_DQ[51], DDR0_DQ[52], DDR0_DQ[53], DDR0_DQ[56], DDR0_DQ[63]
0.74	04.03.2020	The System Control Module line of table 2-1 (page 6) has the information about unaccessability of boot controller's dedicated interfaces for Cortex-A57 cores
0.75	10.03.2020	Minor edits
0.76	20.03.2020	The Datsheet has the following corrections: • Table 1 1 has the following corrections: o The name of **High Speed Peripherals** line changed to **High Speed Peripheral Interfaces** o The name of **Low Speed Peripherals** line changed to **Low Speed Peripheral Interfaces** • Table 2-1 has the following corrections: o In the Arm Cortex-A57 *central processing unit* (**CPU**) Cluster line (page 4) 48K and 32K changed to 48 KB and 32 KB respectively o DDR3/4 Memory Controller line (page 4) has the following corrections: ▪ DDR4U and DDR4L support ▪ Industry standard LRDIMM is not supported o PCIe Gen 3.0 line (page 6) has the following corrections: ▪ Transfer rates up to 8.0 GT/s (~1GB/s) per single lane ▪ Maximum payload size and number of virtual channels are given for PCIe x4 and PCIe x8 o Descriprion of eSPI (page 10) is updated