BE-M1000 Microprocessor
Preliminary Datasheet

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1 Introduction

The BE-M1000 is a general purpose *System-on-a-Chip* (**SoC**) for computing systems, such as personal computers, microservers, networking equipment, multimedia and software-defined hardware, embedded systems and controllers that require high performance and low power consumption.

The SoC features eight Arm® Cortex™-A57 cores that operate at 1.5 GHz and support the coherent caches L1, L2, and L3.

The video subsystem includes two video controllers (LVDS and HDMI), and HD video decoder. Arm Mali™-T628 graphics coprocessor contains eight shader cores.

The SoC contains two DDR3/4 memory controllers and a wide range of peripheral interfaces: PCIe Gen3, 10 Gb Ethernet, 1 Gb Ethernet, USB 3.0, USB 2.0, SATA 6G, eMMC/SD, I^{2}S, SPI, UART, I^{2}C, GPIO, etc.

The SoC complies with Arm TrustZone® technology and contains the capabilities necessary to build trusted systems.

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1.1 Main Features

Table 1-1 Main Features

Feature	Description
Armv8-A Architecture	8 Arm Cortex-A57 cores operating up to 1.5 GHz
	4 core clusters (2 cores and 1 MB L2 cache in a cluster)
Graphics Processing Unit	Arm Mali-T628 *graphics processing unit* (**GPU**) with 8 shader cores (two quad-core clusters) operating at 750 MHz
	128 KB L2 cache in a cluster
L3 Cache	*Cache Coherent Network* (**CCN**) with 8 MB L3 cache memory
External Memory Interface	Two 64-bit *Dynamic Random Access Memory* (**DRAM**) interfaces with support of DDR4-2400/DDR3-1600 and *error correction code* (**ECC**)
High Speed Peripheral Interfaces	Three PCIe Gen3 interfaces: one PCIe x8 and two PCIe x4
	Two USB 3.0/2.0 ports and four USB 2.0 ports
	Two SATA 6G subsystems
	Two 10 Gb Ethernet interfaces (10GBASE-KX4/10GBASE-KR)
	Two 1 Gb Ethernet RGMII
	eMMC/SD/SDIO
Low Speed Peripheral Interfaces	Four peripheral timers
	GPIO*32
	Two UARTs
	SPI
	eSPI
	Two I^{2}Cs
	Two SMBus interfaces
Multimedia	Video Controller with LVDS interface
	Video Controller with HDMI 2.0
	HD Video Decoder
	HD Audio Controller
	I^{2}S interface
Security	Arm TrustZone architecture
	Two TrustZone controllers
	Secure boot
System Monitoring and Debug	Five PVT controllers
	Arm CoreSight™ debug and trace architecture
Package	FCBGA-1521 40x40 mm, 1 mm pitch, 1521 pins
Power Consumption	35W max
Operating Temperature	From 0 to +70°C
Technology	CMOS 28 nm

1.2 Block Diagram

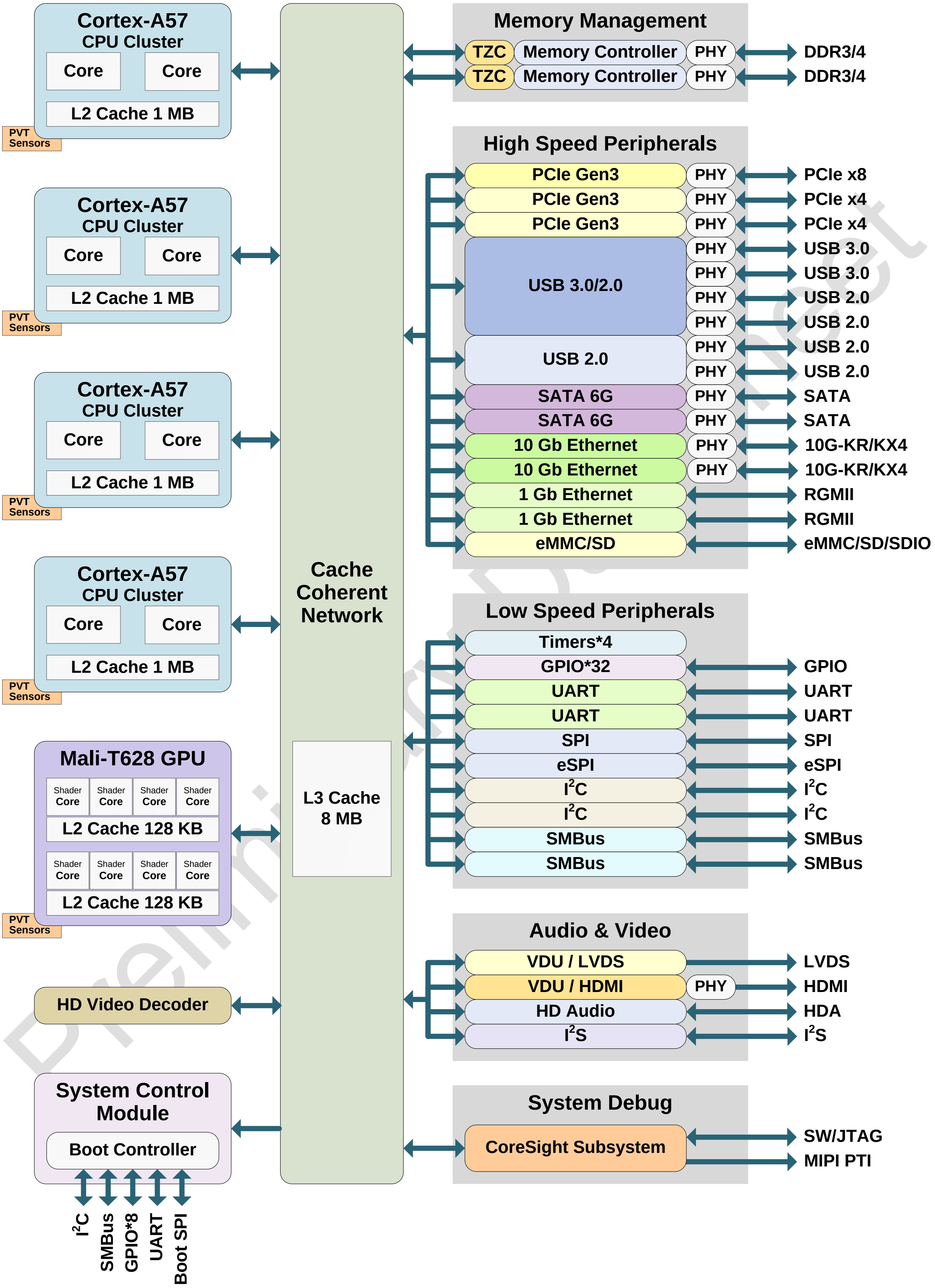

Figure 1-1 Block Diagram

2 Detailed Description

2.1 Arm Cortex-A57 CPU Clusters

The SoC contains 8 Arm Cortex-A57 cores in 4 clusters.

The Cortex-A57 cluster is a high-performance, low-power device that implements the Armv8-A architecture.

Each cluster has two cores (up to 1.5 GHz) and L2 (1 MB) cache.

Each core has 48 KB L1 instruction cache and 32 KB L1 data cache.

None of the cores in the clusters include optional Arm Cortex-A57 core Cryptographic Engine.

A core can operate in one of two possible states, known as the secure and non-secure. By propagating the security state of the core through the on-chip interconnect to target based transaction filters, the TrustZone technology is extended into the SoC architecture, creating a robust platform supporting fully isolated Trusted and Non-trusted worlds.

2.2 Memory Management

The SoC supports two memory channels. Each channel contains TrustZone controller, DDR controller and DDR PHY.

2.2.1 DDR3/4 Memory Subsystem

The SoC contains two DDR3/4 memory subsystems.

Each subsystem supports the following features:

- Up to 64 GB physical memory per channel
- Up to 4 memory ranks per channel
- Integrated PHY
- 64/32-bit DDR3 (speed grades up to DDR3-1600)
- 64/32-bit DDR4 (speed grades up to DDR4-2400)
- ECC: *single error correction/double error detection* (**SEC**/**DED**)
- 1:2 frequency ratio mode
- Low area, low power architecture
- Programmable support for 1T/2T memory command timing
- Software programmable *quality of service* (**QoS**)
- Automatic DDR3/4 low power mode operation

DDR memory control subsystems are combined in the SoC with TrustZone controllers to provide capabilities for building trusted systems.

2.2.2 DMA Controller for Low Speed Peripherals

The DMA LSP implements capability of direct data transfer between a low speed device, which is connected to a low speed peripheral interface, and memory without CPU usage.

It helps in maximizing system performance by decreasing a load of the SoC cores.

The DMA controller can only work in non-secure mode and has the following main features:

- Handshaking interface with two UARTs, SPI, and two I^{2}C controllers

- 8 channels, one per source and destination pair
- Unidirectional channels: data transfers in one direction only
- Multi-block transfers
- Single FIFO per channel for source and destination
- Automatic data packing or unpacking to fit FIFO width

2.3 Cache Coherent Network

Based on the Arm CoreLink™ CCN-504, CCN provides interconnection of the main SoC subsystems and manages the Level 3 cache for these subsystems.

The CCN provides the following key features:

- Dual simplex ring-bus interconnect topology
- Broadcast snoop channel
- DVM message transport between masters
- QoS regulation for shaping traffic profiles
- Monitoring performance-related events
- Error signal gathering using an error bus, with a single point of interrupt coordination on errors
- Separate caches for secure and non-secure transactions

2.4 System Control Module

The System Control Module is used to manage all the SoC subsystems.

It contains the following main blocks:

- *System control processor* (**SCP**) that runs service functions such as
    - Starts the SoC
    - Provides the initial configuration of all the SoC modules
    - Monitors the state of the SoC
- Boot controller that contains dedicated SPI used for initial boot
- UART, SMBus, GPIO*8, and I^{2}C controllers used for system control functions
- *Clock Management Unit* (**CMU**) that controls system clock and reset signals

2.5 High Speed Peripherals

2.5.1 PCIe Gen 3.0

The SoC contains three *PCI Express* (**PCIe**) interfaces:

- PCIe x8 with 64 GT/s transfer rate
- Two PCIe x4, each with 32 GT/s transfer rate

Each PCIe subsystem contains PCIe Root Complex controller that provides base PCIe functionality in accordance with the ***PCI Express Base Specification 3.0***.

Each PCIe provides the following main features:

- Integrated PHY
- Transfer rates up to 8.0 GT/s (~1GB/s) per single lane
- PCIe *active state power management* (**ASPM**)
- PCIe *advanced error reporting* (**AER**) with Multiple Header Logging
- *Internal address Translation Unit* (**iATU**)
- Embedded multichannel DMA controller
- Automatic Lane Reversal
- ECRC Generation and Checking
- Maximum Payload Size:
    - 256 bytes for PCIe x4
    - 512 bytes for PCIe x8
- 1 Virtual Channel for PCIe x4, 2 Virtual Channels for PCIe x8

Each PCIe can work both in secure and non-secure modes.

2.5.2 USB 3.0/2.0

The SoC contains two *Universal Serial Bus* (**USB**) controllers (USB 3.0/2.0 and USB 2.0) and six integrated PHY that provide six interfaces: two USB 3.0 interfaces and four USB 2.0 interfaces.

USB 3.0/2.0 controller is compatible with the ***xHCI Specification*** by Intel Corporation. It is optimized for the Super-Speed applications and systems and supports the following device types:

- Super-Speed devices via USB 3.0 interface (4 Gbps IN and 4 Gbps OUT)
- High-Speed, Full-Speed, and Low-Speed devices via any interface

USB 3.0/2.0 can work both in secure and non-secure modes.

USB 2.0 controller is compatible with the ***xHCI Specification*** by Intel Corporation. It is optimized for the high-bandwidth applications and systems and supports the following device types:

- High-Speed (480 Mbps)
- Full-Speed (12 Mbps)
- Low-Speed (1.5 Mbps)

USB 2.0 can work both in secure and non-secure modes.

2.5.3 SATA 6G

The SoC contains two identical *Serial ATA* (**SATA**) subsystems. Each SATA supports the following features:

- Integrated PHY
- SATA 6.0 Gb/s speeds
- Compliant with ***Serial ATA 3.2*** and ***AHCI Revision 1.3*** specifications
- 8b/10b encoding/decoding
- Error correction code
- Power management features including automatic partial-to-slumber transition

- Internal DMA engine per port

Each SATA can work both in secure and non-secure modes.

2.5.4 10 Gb Ethernet

The SoC contains two identical 10 Gb Ethernet interfaces, which enable to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2008 standard for two types of 10 Gb/s Ethernet: 10GBASE-KX4 and 10GBASE-KR.

Each interface contains a *10 Gb Ethernet media access controller* (**XGMAC**) with integrated *10 Gigabit Ethernet Physical Coding Sublayer* (**XPCS**) and 10 Gb Ethernet PHY.

Each XGMAC has the following main features:

- Full-duplex operation at 10 Gbps
- Full compliance with Clause 71 (10GBASE-KX4) and Clause 72 (10GBASE-KR) of the IEEE 802.3-2008 standard
- Full compliance with Clause 78 (*Energy Efficient Ethernet* (**EEE**) feature) of the IEEE 802.3az, standard for 10 Gbps operation
- Programmable frame length, supporting standard or jumbo (extendable to 16 KB) Ethernet frames
- Support for VLAN-tagged frame processing in compliance with the IEEE 802.1Q standard

Each XGMAC can work both in secure and non-secure modes.

2.5.5 1 Gb Ethernet

The module provides two identical *1 Gigabit media access controllers* (further **GMAC**).

Each controller enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2008 standard.

Each GMAC has the following main features:

- 10, 100, and 1000 Mbps data transfer rates with RGMII interface to communicate with an external gigabit PHY
- Full-duplex and half-duplex operation support
- Embedded DMA controller with independent Transmit and Receive engines

Each GMAC can work both in secure and non-secure modes.

2.5.6 eMMC/SD

It provides communication with memory cards targeted for the mobile/portable market and adheres to the ***SD UHS-I*** and ***eMMC*** Specifications.

The *Embedded Multimedia Card* (**eMMC**)/*Secure Digital* (**SD**) controller supports the following features:

- SD memory and *Secure Data Input/Output* (**SDIO**) digital interface protocol, and compliant with ***SD HCI Specification***
- eMMC protocols including eMMC 5.1
- SD-HCI Host version 4 mode or less
- Embedded DMA controller
- Software tuning in SD UHS-I and eMMC modes

2.6 Low Speed Peripherals

2.6.1 GPIO*32

General Purpose Input/Output (**GPIO**) implements run-time 32-bit programmable interface for external communications. The GPIO controls the output data and direction of external I/O pads. It also can read back the data on external pads using memory-mapped registers.

The interface contains 32 individually controllable signals in a single port.

2.6.2 UART

There are two identical *Universal Asynchronous Receiver-Transmitters* (**UART**) in the SoC.

Each UART has a handshaking interface with the DMA LSP that can request and control non-secure data transfers between the UART and memory.

Each UART contains registers that control:

- Character length
- Baud rates up to 1.5 Mbaud
- Parity generation/checking
- Interrupt generation

2.6.3 SPI

The *Serial Peripheral Interface* (**SPI**) is a full-duplex master or slave-synchronous serial interface used for short distance communication with up to four external slave devices (SSx4).

It has a handshaking interface with the DMA LSP that can request and control data transfers between the SPI and memory.

A master (application processor or the DMA LSP) accesses data, control, and status information on the SPI through the APB interface.

The SPI operates as a serial master. It can connect to a serial-slave peripheral device.

2.6.4 eSPI

The *Enhanced Serial Peripheral Interface* (**eSPI**) is a synchronous serial communication interface used for short distance communication with up to eight external slave devices (SSx8).

Additional eSPI signals in compare to SPI Interface:

- `RESET` programmable as input or output
- `ALERT` input interrupts

An eSPI device communicates in full-duplex mode using master-slave architecture with up to eight external slave SPI devices (SSx8). It supports Single/Dual/Quad SPI mode of operation.

2.6.5 I^{2}C

There are two identical general purpose *Inter-Integrated Circuits* (**I^{2}C**) in the SoC.

The I^{2}C is a programmable serial interface that provides support for the communications link between the devices connected to the bus.

Each I^{2}C support the following features:

- Three speeds:
    - Standard mode (0 to 100 Kb/s)
    - Fast mode (≤ 400 Kb/s) or fast mode plus (≤ 1000 Kb/s)
    - High-speed mode (≤ 3.4 Mb/s)
- Master OR slave I^{2}C operation
- 7- or 10-bit addressing
- 7- or 10-bit combined format transfers

Each I^{2}C has a handshaking interface with the DMA LSP that can request and control non-secure data transfers between the I^{2}C and memory.

2.6.6 SMBus

The SoC includes two identical *System Management Bus* (**SMBus**) interfaces.

This interface provides a two-wire bidirectional interface for transfer of bytes of information between multiple compliant I^{2}C devices, typically with a microprocessor behind the DB-I^{2}C master/slave controller and one or more master/slave devices.

2.7 Audio & Video

2.7.1 Arm Mali-T628 GPU

Provides a complete graphics acceleration platform based on open standards. It supports 2D graphics, 3D graphics, and *general purpose computing on GPU* (**GPGPU**).

The graphics processor provides the following main features:

- Two clusters
- 4 shader cores operating at 750 MHz per each cluster
- 128KB L2 Cache per each cluster
- Seamless load balancing across active shader cores
- The following APIs are supported:
    - OpenGL ES 1.1, 2.0, 3.0, 3.1
    - OpenCL 1.1
    - RenderScript
- *Full scene anti-aliasing* (4x**FSAA**, 16x**FSAA**) with minimal performance drop
- *Adaptive scalable texture compression* (**ASTC**): *low dynamic range* (**LDR**) and *high dynamic range* (**HDR**) are supported
- Native hardware support for 64-bit scalar and vector, integer and floating-point data types – fundamental to accelerate complex and computationally intensive algorithms

It can work both in secure and non-secure modes.

2.7.2 HD Video Decoder

Used to decode video streams encoded in the following formats:

- H.265 (HEVC)

- H.264, MPEG4, MPEG2, VP8, VP6, VC1, AVS, RealVideo, and JPEG: up to 1080p at 60 fps

The decoder loads the encoded video data from the system memory, decodes it and places the information ready to be sent to the video display unit into the frame buffer.

It can work both in secure and non-secure modes.

2.7.3 VDU with Quad LVDS

Visual Display Unit (**VDU**) with quad *Low-Voltage Differential Signaling* (**LVDS**) is a general purpose display controller used to drive a wide range of display devices varying in size and capability.

The module provides the following main features:

- Display resolution up to 2560x1440
- Color resolution of up to 24 bpp
- Embedded DMA controller
- Programmable vertical and horizontal timing parameters

2.7.4 VDU with HDMI 2.0

VDU with *High Definition Multimeda Interface* (**HDMI**) provides a complete HDMI interface for transmitting video and audio data to an HDMI-compliant source device, such as a computer monitor, video projector, digital television, or digital audio device.

The subsystem has the following main features:

- Display resolution up to 2560x1440
- VDU features:
  - Color resolution of up to 24 bpp
  - Embedded DMA Controller
  - Programmable vertical and horizontal timing parameters
- Three TMDS data channels with 6 Gbps data rate per channel
- Total maximum throughput of up to 18 Gbps (6 Gbps * 3 channels)
- HDMI 2.0 specification features:
  - All CEA-861-F video formats
  - *Dynamic range and mastering infoframe* (**DRM**)
- Embedded DMA controller for audio
- Audio stream bit rate up to 24.576 Mbps
- It can work both in secure and non-secure modes

2.7.5 HD Audio

The HD Audio cotroller is a bus mastering I/O peripheral, which is attached to system memory via interconnect. It contains one or more DMA engines, each of which can be set up to transfer a single audio “stream” to memory from the codec or from memory to the codec depending on the DMA type.

The controller supports the following features:

- Maximum number of input streams : 4

- Maximum number of output streams : 4
- Number of SDO outputs: 2 (SDO 0 and SDO 1: outputs to the codecs)
- Number of SDI inputs: 2 (SDI 0 and SDI 1: inputs from the codecs)
- Sample rate: up to 192 kHz
- Bit width per stream: up to 32 bit
- Number of channels: up to 10
- Number of SDO DMA engines: 4 (unidirectional)
- Number of SDI DMA engines: 4 (unidirectional)
- Memory banks:
  - 512x40
  - 512x32
  - 32x32

2.7.6 *I²S*

The *Inter-IC Sound* (**I²S**) is a programmable module used for the serial communication with peripherals.

It is designed to be used in systems that process digital audio signals, such as:

- A/D and D/A converters
- Digital signal processors
- Error correction for compact disc and digital recording
- Digital filters
- Digital input/output interfaces

2.8 System Monitoring and Debug

2.8.1 *PVT Controllers*

The SoC contains five *Process, Voltage and Temperature* (**PVT**) controllers used to monitor the Cortex-A57 clusters and Mali-T628 GPU.

2.8.2 *CoreSight Subsystem*

Provides a standard implementation of the Arm Debug Interface for debug tools to work with:

- Serial Wire or JTAG Debug Port
- Trace Port Interface

The subsystem supports the following methods of debugging the SoC:

- “External” debug—conventional debug through the SW/JTAG interface
- “Self-hosted” debug—conventional debug with the processor running using a debug monitor that resides in memory
- Logging of hardware and software events in a trace, which is recorded in memory as well as transmitted through the *trace port interface* (**MIPI PTI**) to an external debug system

It can work both in secure and non-secure modes.

3 Electrical Specifications

NOTE: The electrical characteristics are subject to change and clarification without extra notification.

3.1 Power Supply Parameters

BE-M1000 requires six isolated voltage supplies and single unified ground supply as shown in the following table.

Table 3-1 BE-M1000 Power Domains

Supply Type	Package Pin Name	Voltage, V	Max Power, W
Core supply	VDD	0.95 ± 5%	24
0.95V voltage supply	VDD_HDMI_09 VDD_USB2_09 VDD_USB3_0_09 VDD_USB3_1_09 VDD_USB3TX_0_09 VDD_USB3TX_1_09 VDD_USB3_VP_0_09 VDD_USB3_VP_1_09 VDD_PCIE4_0_09 VDD_PCIE4_1_09 VDD_PCIE8_09 VDD_SATA_09 VDD_SATATX_09 VDD_XG0_09 VDD_XG1_09		
PLL supply	VDDPLL_0_09 VDDPLL_1_09 VDDPLL_2_09 VDDPLL_3_09 VDDPLL_HDMI_09	0.95 ± 5%	0.20
DDR supply	VDDQ_DDR0 VDDQ_DDR1	DDR4: 1.2 ± 5%	6.0
1.5V voltage supply	VDD_PCIE4_0_15 VDD_PCIE4_1_15 VDD_PCIE8_15 VDD_XG0_15 VDD_XG1_15	1.5 ± 5%	2.0

Supply Type	Package Pin Name	Voltage, V	Max Power, W
1.8V voltage supply	VDD_DDR0_PLL VDD_DDR1_PLL VDD_HDMI_18 VDD_PVT_18 VDD_SATA_18 VDD_USB2_18 VDDIO	1.8 ± 10%	1.8
3.3V voltage supply	VDD_SD_33 VDD_USB2_0_33 VDD_USB2_1_33 VDD_USB2_2_33 VDD_USB2_3_33 VDD_USB3_33	3.3 -6.9% +4.8%	0.7
Ground	VSS	-	-
Total			**~34.7W**

3.2 External Clocking

3.2.1 Reference Clock Signals

Table 3-2 Reference Clock Signals

Clock Signal	Pin Names	Frequency	Notes
Reference clock	CLK25M	25 MHz	-
XGbE PHY reference clock	XG0_REF_CLKN[1,2] XG0_REF_CLKP[1,2] XG1_REF_CLKN[1,2] XG1_REF_CLKP[1,2]	156.25 MHz	Differential pair . Terminated[3] and unterminated[4] clocks
PCIe PHY reference clock	PCIE4_0_REF_CLKN[1,2] PCIE4_0_REF_CLKP[1,2] PCIE4_1_REF_CLKN[1,2] PCIE4_1_REF_CLKP[1,2] PCIE8_REF_CLKN[1,2] PCIE8_REF_CLKP[1,2]	100 MHz	Differential pair . Terminated[3] and unterminated[4] clocks
SATA PHY reference clock	SATA_REFCLKP[1,2] SATA_REFCLKM[1,2]	100 MHz	Differential pair . Terminated[3] and unterminated[4] clocks

Clock Signal	Pin Names	Frequency	Notes
USB 3.0 PHY optional reference clock input	USB3_0_REFCLKN[1,2] USB3_0_REFCLKP[1,2] USB3_1_REFCLKN[1,2] USB3_1_REFCLKP[1,2]	100 MHz (typical)	Differential . pair
USB 2.0 PHY: XI - crystal oscillator XO - crystal oscillator or board reference clock input	USB2_0_XI[1,2] USB2_0_XO[1,2] USB2_1_XI[1,2] USB2_1_XO[1,2] USB2_2_XI[1,2] USB2_2_XO[1,2] USB2_3_XI[1,2] USB2_3_XO[1,2]	50 MHz	
HDMI PLL reference clock input	HDMI_PLL_27M[1,2]	27 MHz	
LVDS PLL reference clock input	LVDS_PLL_27M[1,2]	27 MHz	

NOTE:

1 If the reference clock pins are unused, they should be tied off to the ground potential

2 Reference clocks connect as needed

3 With terminated clocks, a 50 Ohms termination resistor is soldered on the board close to the SoC, preventing clock reflections while providing a clock source to the PHY

4 If the board clocks are unterminated, the clock's signal level will double as it hits the high-impedance input of the PHY reference clock inputs. This effect can also be used to provide a clean clock to the PHY, but ensure that the signal swing of the reference clock is not too high after doubling the amplitude

3.2.2 Reference Clock Requirements

3.2.2.1 Reference Clock (CLK25M)

Table 3-3 Reference Clock (CLK25M) Requirements

Parameter	Min	Typ	Max	Unit
Frequency range		25		MHz
Reference clock frequency offset	-50		50	ppm
Reference clock random jitter (RMS)		10		ps
Reference clock cycle to cycle jitter		6		ps
Startup time		1.5	3.0	ms
Disable time		20	100	ns
Disable stand-by current			15	uA

3.2.2.2 SATA PHY Reference Clock

Table 3-4 SATA PHY Reference Clock Requirements

Parameter	Min	Typ	Max	Unit	Conditions
Frequency range		100		MHz	
Reference clock frequency offset	-350		350	ppm	
Reference clock random jitter (RMS)			3	ps	1.5 MHz to Nyquist frequency. For example, for 100 MHz reference clock, the Nyquist frequency is 50 MHz
Reference clock cycle to cycle jitter			150	ps	DJ across all frequencies
Duty cycle	40		60	%	
Common mode input level	0		vp	V	Differential inputs
Differential input swing	0.3			Vpp	Differential inputs[1]
Single-ended input logic low	-0.3		0.3	V	If single-ended input is used
Single-ended input logic high	vp-0.3		vp+0.3	V	If single-ended input is used
Input edge rate	0.6			V/ns	
Reference clock skew (±)			200	ps	

3.2.2.3 XGbE PHY Reference Clock

The PHY supports a differential reference clock source. The source may be driven through either external pads or internal pins. The chosen reference clock must meet specific requirements for signal swing and jitter. The following table summarizes the requirements of the reference clock provided to the PHY.

Table 3-5 XGbE PHY Reference Clock Requirements

Parameter	Min	Typ	Max	Unit	Conditions
Frequency range		156.25		MHz	
Frequency stability	-100		100	ppm	
Differential input swing	300		1890	mVppd	
Duty cycle	40		60	%	
Input edge rate	0.6			V/ns	
Coupling					AC coupling
Allowed jitter for 10GBASE-KR and slower			2.25	ps (rms)	Integrated from 12 kHz to 20 MHz
Allowed jitter for 10GBASE-KX4			3.6	ps (rms)	Integrated from 12 kHz to 20 MHz
Peak to peak period jitter of the reference clock			20	ps	Period jitter measured over 10k samples

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[1] VDREF_CLK/4 + VCMREF_CLK ≤ vp + diode forward-biasing voltage and VCMREF_CLK-VDREF_CLK/4 ≥ - diode forward biasing voltage

Parameter	Min	Typ	Max	Unit	Conditions
Phase jitter			2	ps	Integrated from 1.5 MHz to Nyquist frequency. For example, for 100 MHz reference clock, the Nyquist frequency is 50 MHz

3.2.2.4 PCIe PHY Reference Clock

Table 3-6 PCIe PHY Reference Clock Requirements

Parameter	Min	Typ	Max	Unit	Conditions
Frequency range		100		MHz	
Frequency stability	-300		300	ppm	
Differential input swing	300		1890	mVppd	
Duty cycle	40		60	%	
Input edge rate	0.6			V/ns	
Coupling					AC coupling

NOTE: 100 MHz is the only PCIe standard compliant frequency. When using a 125 MHz frequency, the PHY may not be compliant to all PCIe specifications, such as PLL bandwidth, peaking, and jitter.

3.2.2.5 USB 3.0 PHY Reference Clock

The USB 3.0 PHY is designed to handle a wide range of input clock frequencies to support both host and device applications. The following table summarizes the requirements of the reference clock provided to the USB 3.0 PHY to support SuperSpeed only or both SuperSpeed and high-speed operations.

Table 3-7 USB 3.0 PHY Reference Clock Requirements

Parameter	Min	Typ	Max	Unit	Conditions
Reference clock frequency	19.2	100	200	MHz	
Reference clock frequency stability	-300		300	ppm	
Reference clock random jitter (RMS)			3	ps	1.5 MHz to Nyquist frequency. For example, for 100 MHz reference clock, the Nyquist frequency is 50 MHz
Reference clock skew			200	ps	
Reference clock cycle-to-cycle jitter			150	ps	DJ over all frequency
Duty cycle	40		60	%	
Common mode input level	0		1.32	V	Differential inputs

Parameter	Min	Typ	Max	Unit	Conditions
Differential input swing	0.3			Vpp	Differential inputs[1]
Single-ended input logic: Low	-0.3		0.3	V	If single-ended input is used
Single-ended input logic: High	vp-0.3		vp	V	If single-ended input is used
Input edge rate	0.6		4	V/ns	
Required external reference resistance		200		Ohms	± 1% accuracy

3.2.2.6 USB 2.0 PHY Reference Clock

The USB 2.0 PHY supports the following reference clock sources:

- **Crystal Oscillator connected to the USB2_*_XI and USB2_*_XO pins**: The crystal oscillator must have a frequency tolerance of ±400 ppm, peak jitter of ±100 ps, and an output differential voltage of no less than 500 mV with respect to the XI signal
- **External Clock connected to the USB2_*_XO pin**: The clock must have a fundamental frequency of 50 MHz, with a frequency tolerance of ± 400 ppm, peak jitter of ± 100 ps, duty cycle between 40/60 and 60/40 percent, and signal swing of 1.8V.

3.2.2.7 HDMI PLL Reference Clock

Table 3-8 HDMI PLL Reference Clock Requirements

Parameter	Min	Typical	Max	Unit
Frequency range		27		MHz
Frequency stability	-50		50	ppm
Output		LVCMOS 1.8		V
Duty cycle	40		60	%

3.2.2.8 LVDS PLL Reference Clock

Table 3-9 LVDS PLL Reference Clock Requirements

Parameter	Min	Typical	Max	Unit
Frequency range		27		MHz
Frequency stability	-50		50	ppm
Output		LVCMOS 1.8		V
Duty cycle	40		60	%

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[1] VDREF_CLK / 4 + VCMREF_CLK ≤ vp + diode forward biasing voltage and VCMREF_CLK – VDREF_CLK / 4 ≥ –diode forward biasing voltage

4 Power-Up/Down

4.1 Power-Up Sequence

The following steps have to be performed to power up the SoC:

1. Provide the `RESET_N` reset signal (active is low)
2. Apply voltages to power pins according to Power Supply Parameters in the following order:
    - 3.3V voltage supply
    - 1.5V voltage supply
    - PLL supply
    - DDR supply
3. Provide the `CS_TRST_N` reset signal
4. Provide the `TRSTN` reset signal
5. Apply voltages to power pins according to Power Supply Parameters in the following order:
    - 1.8V voltage supply
    - Core supply and 0.95V voltage supply
6. Provide all reference clocks
7. Wait at least 16 cycles of the reference clock
8. Deassert the `RESET_N` signal

Once the `RESET_N` signal is deasserted, the boot controller provides initialization of clock and reset signals for each SoC subsystem, loads and executes the Boot Loader, which is stored in the Boot SPI Flash.

4.2 Power-Down Sequence

Power-down sequence is the reverse of the power-up sequence.

5 Pin Assignment

5.1 Pinout List

The following tables contain the list of I/O pins of the SoC including the power supply and ground pins. The following legend is applied for the following tables.

Legend:

I	Input
O	Output
IO	Input/Output
A	Analog
P	Power supply
G	Ground
NC	Not connected

5.1.1 Memory Management

5.1.1.1 DDR3/4

Table 5-1 DDR Pins

Pin ID	Package Pin Name	Type	Power Supply	Description
K12	DDR0_A[0]	O	VDDQ_DDR0	SDRAM address
M13	DDR0_A[1]	O	VDDQ_DDR0	SDRAM address
AA9	DDR0_A[10]	O	VDDQ_DDR0	SDRAM address
AC11	DDR0_A[11]	O	VDDQ_DDR0	SDRAM address
Y13	DDR0_A[12]	O	VDDQ_DDR0	SDRAM address
AC12	DDR0_A[13]	O	VDDQ_DDR0	SDRAM address
AA11	DDR0_A[14]	O	VDDQ_DDR0	SDRAM WE
Y10	DDR0_A[15]	O	VDDQ_DDR0	SDRAM CAS
AB11	DDR0_A[16]	O	VDDQ_DDR0	SDRAM RAS
AA8	DDR0_A[17]	O	VDDQ_DDR0	SDRAM A[17]
J12	DDR0_A[2]	O	VDDQ_DDR0	SDRAM address
T12	DDR0_A[3]	O	VDDQ_DDR0	SDRAM address
L14	DDR0_A[4]	O	VDDQ_DDR0	SDRAM address
AB12	DDR0_A[5]	O	VDDQ_DDR0	SDRAM address
V13	DDR0_A[6]	O	VDDQ_DDR0	SDRAM address
AB10	DDR0_A[7]	O	VDDQ_DDR0	SDRAM address
V11	DDR0_A[8]	O	VDDQ_DDR0	SDRAM address
Y11	DDR0_A[9]	O	VDDQ_DDR0	SDRAM address
H10	DDR0_ACT_N	O	VDDQ_DDR0	When low, indicates the activate (open row) command
U12	DDR0_ALERT_N	I	VDDQ_DDR0	SDRAM CRC/parity error

Pin ID	Package Pin Name	Type	Power Supply	Description
U11	DDR0_ATO	A		Analog test output (test Pad) Reserved in BN Package and BK Package
J13	DDR0_BA[0]	O	VDDQ_DDR0	SDRAM bank address
J10	DDR0_BA[1]	O	VDDQ_DDR0	SDRAM bank address
U7	DDR0_BG[0]	O	VDDQ_DDR0	SDRAM bank Group
M12	DDR0_BG[1]	O	VDDQ_DDR0	SDRAM bank Group
L9	DDR0_CK[0]	O	VDDQ_DDR0	SDRAM clock
M11	DDR0_CK[1]	O	VDDQ_DDR0	SDRAM clock
N10	DDR0_CK[2]	O	VDDQ_DDR0	SDRAM clock
P11	DDR0_CK[3]	O	VDDQ_DDR0	SDRAM clock
M9	DDR0_CK_N[0]	O	VDDQ_DDR0	SDRAM clock
L11	DDR0_CK_N[1]	O	VDDQ_DDR0	SDRAM clock
P10	DDR0_CK_N[2]	O	VDDQ_DDR0	SDRAM clock
R11	DDR0_CK_N[3]	O	VDDQ_DDR0	SDRAM clock
R12	DDR0_CKE[0]	O	VDDQ_DDR0	SDRAM clock enable
N13	DDR0_CKE[1]	O	VDDQ_DDR0	SDRAM clock enable
AB13	DDR0_CKE[2]	O	VDDQ_DDR0	SDRAM clock enable
W10	DDR0_CKE[3]	O	VDDQ_DDR0	SDRAM clock enable
L13	DDR0_CS_N[0]	O	VDDQ_DDR0	SDRAM chip select
P13	DDR0_CS_N[1]	O	VDDQ_DDR0	SDRAM chip select
W9	DDR0_CS_N[2]	O	VDDQ_DDR0	SDRAM chip select
U10	DDR0_CS_N[3]	O	VDDQ_DDR0	SDRAM chip select
AB8	DDR0_DM[0]	IO	VDDQ_DDR0	SDRAM data mask
AC4	DDR0_DM[1]	IO	VDDQ_DDR0	SDRAM data mask
Y7	DDR0_DM[2]	IO	VDDQ_DDR0	SDRAM data mask
T2	DDR0_DM[3]	IO	VDDQ_DDR0	SDRAM data mask
L8	DDR0_DM[4]	IO	VDDQ_DDR0	SDRAM data mask
N3	DDR0_DM[5]	IO	VDDQ_DDR0	SDRAM data mask
K7	DDR0_DM[6]	IO	VDDQ_DDR0	SDRAM data mask
J3	DDR0_DM[7]	IO	VDDQ_DDR0	SDRAM data mask
P2	DDR0_DM[8]	IO	VDDQ_DDR0	SDRAM data mask
AD5	DDR0_DQ[0]	IO	VDDQ_DDR0	SDRAM data
AB7	DDR0_DQ[1]	IO	VDDQ_DDR0	SDRAM data
Y3	DDR0_DQ[10]	IO	VDDQ_DDR0	SDRAM data

Pin ID	Package Pin Name	Type	Power Supply	Description
Y4	DDR0_DQ[11]	IO	VDDQ_DDR0	SDRAM data
AB1	DDR0_DQ[12]	IO	VDDQ_DDR0	SDRAM data
AB2	DDR0_DQ[13]	IO	VDDQ_DDR0	SDRAM data
AB3	DDR0_DQ[14]	IO	VDDQ_DDR0	SDRAM data
AB4	DDR0_DQ[15]	IO	VDDQ_DDR0	SDRAM data
V6	DDR0_DQ[16]	IO	VDDQ_DDR0	SDRAM data
V5	DDR0_DQ[17]	IO	VDDQ_DDR0	SDRAM data
Y5	DDR0_DQ[18]	IO	VDDQ_DDR0	SDRAM data
Y8	DDR0_DQ[19]	IO	VDDQ_DDR0	SDRAM data
AB6	DDR0_DQ[2]	IO	VDDQ_DDR0	SDRAM data
V7	DDR0_DQ[20]	IO	VDDQ_DDR0	SDRAM data
U5	DDR0_DQ[21]	IO	VDDQ_DDR0	SDRAM data
W8	DDR0_DQ[22]	IO	VDDQ_DDR0	SDRAM data
Y6	DDR0_DQ[23]	IO	VDDQ_DDR0	SDRAM data
V3	DDR0_DQ[24]	IO	VDDQ_DDR0	SDRAM data
V4	DDR0_DQ[25]	IO	VDDQ_DDR0	SDRAM data
T3	DDR0_DQ[26]	IO	VDDQ_DDR0	SDRAM data
T1	DDR0_DQ[27]	IO	VDDQ_DDR0	SDRAM data
V2	DDR0_DQ[28]	IO	VDDQ_DDR0	SDRAM data
W4	DDR0_DQ[29]	IO	VDDQ_DDR0	SDRAM data
AB5	DDR0_DQ[3]	IO	VDDQ_DDR0	SDRAM data
T4	DDR0_DQ[30]	IO	VDDQ_DDR0	SDRAM data
V1	DDR0_DQ[31]	IO	VDDQ_DDR0	SDRAM data
L5	DDR0_DQ[32]	IO	VDDQ_DDR0	SDRAM data
L6	DDR0_DQ[33]	IO	VDDQ_DDR0	SDRAM data
L7	DDR0_DQ[34]	IO	VDDQ_DDR0	SDRAM data
M8	DDR0_DQ[35]	IO	VDDQ_DDR0	SDRAM data
N5	DDR0_DQ[36]	IO	VDDQ_DDR0	SDRAM data
N6	DDR0_DQ[37]	IO	VDDQ_DDR0	SDRAM data
N7	DDR0_DQ[38]	IO	VDDQ_DDR0	SDRAM data
N8	DDR0_DQ[39]	IO	VDDQ_DDR0	SDRAM data
AD7	DDR0_DQ[4]	IO	VDDQ_DDR0	SDRAM data
K1	DDR0_DQ[40]	IO	VDDQ_DDR0	SDRAM data
K2	DDR0_DQ[41]	IO	VDDQ_DDR0	SDRAM data

Pin ID	Package Pin Name	Type	Power Supply	Description
K3	DDR0_DQ[42]	IO	VDDQ_DDR0	SDRAM data
L4	DDR0_DQ[43]	IO	VDDQ_DDR0	SDRAM data
M1	DDR0_DQ[44]	IO	VDDQ_DDR0	SDRAM data
M2	DDR0_DQ[45]	IO	VDDQ_DDR0	SDRAM data
M3	DDR0_DQ[46]	IO	VDDQ_DDR0	SDRAM data
N4	DDR0_DQ[47]	IO	VDDQ_DDR0	SDRAM data
J5	DDR0_DQ[48]	IO	VDDQ_DDR0	SDRAM data
J7	DDR0_DQ[49]	IO	VDDQ_DDR0	SDRAM data
AD6	DDR0_DQ[5]	IO	VDDQ_DDR0	SDRAM data
J8	DDR0_DQ[50]	IO	VDDQ_DDR0	SDRAM data
J6	DDR0_DQ[51]	IO	VDDQ_DDR0	SDRAM data
G5	DDR0_DQ[52]	IO	VDDQ_DDR0	SDRAM data
G8	DDR0_DQ[53]	IO	VDDQ_DDR0	SDRAM data
G6	DDR0_DQ[54]	IO	VDDQ_DDR0	SDRAM data
G7	DDR0_DQ[55]	IO	VDDQ_DDR0	SDRAM data
F1	DDR0_DQ[56]	IO	VDDQ_DDR0	SDRAM data
F2	DDR0_DQ[57]	IO	VDDQ_DDR0	SDRAM data
F3	DDR0_DQ[58]	IO	VDDQ_DDR0	SDRAM data
G4	DDR0_DQ[59]	IO	VDDQ_DDR0	SDRAM data
AD8	DDR0_DQ[6]	IO	VDDQ_DDR0	SDRAM data
H1	DDR0_DQ[60]	IO	VDDQ_DDR0	SDRAM data
H2	DDR0_DQ[61]	IO	VDDQ_DDR0	SDRAM data
H3	DDR0_DQ[62]	IO	VDDQ_DDR0	SDRAM data
J4	DDR0_DQ[63]	IO	VDDQ_DDR0	SDRAM data
AC8	DDR0_DQ[7]	IO	VDDQ_DDR0	SDRAM data
Y1	DDR0_DQ[8]	IO	VDDQ_DDR0	SDRAM data
Y2	DDR0_DQ[9]	IO	VDDQ_DDR0	SDRAM data
AC6	DDR0_DQS[0]	IO	VDDQ_DDR0	SDRAM data strobe
AA2	DDR0_DQS[1]	IO	VDDQ_DDR0	SDRAM data strobe
W5	DDR0_DQS[2]	IO	VDDQ_DDR0	SDRAM data strobe
U2	DDR0_DQS[3]	IO	VDDQ_DDR0	SDRAM data strobe
M5	DDR0_DQS[4]	IO	VDDQ_DDR0	SDRAM data strobe
L2	DDR0_DQS[5]	IO	VDDQ_DDR0	SDRAM data strobe
H5	DDR0_DQS[6]	IO	VDDQ_DDR0	SDRAM data strobe

Pin ID	Package Pin Name	Type	Power Supply	Description
G1	DDR0_DQS[7]	IO	VDDQ_DDR0	SDRAM data strobe
P3	DDR0_DQS[8]	IO	VDDQ_DDR0	SDRAM data strobe
AC5	DDR0_DQS_N[0]	IO	VDDQ_DDR0	SDRAM data strobe
AA1	DDR0_DQS_N[1]	IO	VDDQ_DDR0	SDRAM data strobe
W6	DDR0_DQS_N[2]	IO	VDDQ_DDR0	SDRAM data strobe
U1	DDR0_DQS_N[3]	IO	VDDQ_DDR0	SDRAM data strobe
M6	DDR0_DQS_N[4]	IO	VDDQ_DDR0	SDRAM data strobe
L1	DDR0_DQS_N[5]	IO	VDDQ_DDR0	SDRAM data strobe
H6	DDR0_DQS_N[6]	IO	VDDQ_DDR0	SDRAM data strobe
G2	DDR0_DQS_N[7]	IO	VDDQ_DDR0	SDRAM data strobe
R3	DDR0_DQS_N[8]	IO	VDDQ_DDR0	SDRAM data strobe
K10	DDR0_DTO[0]	O	VDDQ_DDR0	Digital test output (test pad) Reserved in BN Package and BK Package
J9	DDR0_DTO[1]	O	VDDQ_DDR0	Digital test output (test pad) Reserved in BN Package and BK Package
T6	DDR0_ECC[0]	IO	VDDQ_DDR0	SDRAM data ECC
R6	DDR0_ECC[1]	IO	VDDQ_DDR0	SDRAM data ECC
P6	DDR0_ECC[2]	IO	VDDQ_DDR0	SDRAM data ECC
R5	DDR0_ECC[3]	IO	VDDQ_DDR0	SDRAM data ECC
P1	DDR0_ECC[4]	IO	VDDQ_DDR0	SDRAM data ECC
R1	DDR0_ECC[5]	IO	VDDQ_DDR0	SDRAM data ECC
R2	DDR0_ECC[6]	IO	VDDQ_DDR0	SDRAM data ECC
T5	DDR0_ECC[7]	IO	VDDQ_DDR0	SDRAM data ECC
K13	DDR0_MIRROR	O	VDDQ_DDR0	SDRAM mirror (optional DIMM signal)
AA13	DDR0_ODT[0]	O	VDDQ_DDR0	SDRAM on-die termination
AC9	DDR0_ODT[1]	O	VDDQ_DDR0	SDRAM on-die termination
V9	DDR0_ODT[2]	O	VDDQ_DDR0	SDRAM on-die termination
P8	DDR0_ODT[3]	O	VDDQ_DDR0	SDRAM on-die termination
T10	DDR0_PARITY	O	VDDQ_DDR0	SDRAM parity
N12	DDR0_QCSEN_N	O	VDDQ_DDR0	SDRAM quad CS enable (optional DIMM signal)
J11	DDR0_RAM_RST_N	O	VDDQ_DDR0	SDRAM reset
V12	DDR0_VREFI[0]	A		IO ring VREFI net Reserved in BK Package

Pin ID	Package Pin Name	Type	Power Supply	Description
AB9	DDR0_VREFI[1]	A		IO ring VREFI net Reserved in BK Package
W12	DDR0_VREFI[2]	A		IO ring VREFI net Reserved in BK Package
T7	DDR0_VREFI[3]	A		IO ring VREFI net Reserved in BK Package
R8	DDR0_VREFI[4]	A		IO ring VREFI net Reserved in BK Package
K8	DDR0_VREFI[5]	A		IO ring VREFI net Reserved in BK Package
P14	DDR0_VREFI[6]	A		IO ring VREFI net Reserved in BK Package
L10	DDR0_VREFI[7]	A		IO ring VREFI net Reserved in BK Package
U8	DDR0_VREFI[8]	A		IO ring VREFI net Reserved in BK Package
T9	DDR0_VREFI[9]	A		IO ring VREFI net Reserved in BK Package
AC10	DDR0_VREFI_ZQ	A		IO ring VREFI ZQ net
AC13	DDR0_ZQ	A		ZQ resistor (to external calibration resistor)
AM27	DDR1_A[0]	O	VDDQ_DDR1	SDRAM address
AT22	DDR1_A[1]	O	VDDQ_DDR1	SDRAM address
AL25	DDR1_A[10]	O	VDDQ_DDR1	SDRAM address
AL23	DDR1_A[11]	O	VDDQ_DDR1	SDRAM address
AL32	DDR1_A[12]	O	VDDQ_DDR1	SDRAM address
AM23	DDR1_A[13]	O	VDDQ_DDR1	SDRAM address
AK28	DDR1_A[14]	O	VDDQ_DDR1	SDRAM WE
AN32	DDR1_A[15]	O	VDDQ_DDR1	SDRAM CAS
AM26	DDR1_A[16]	O	VDDQ_DDR1	SDRAM RAS
AN31	DDR1_A[17]	O	VDDQ_DDR1	SDRAM A[17]
AR22	DDR1_A[2]	O	VDDQ_DDR1	SDRAM address
AM24	DDR1_A[3]	O	VDDQ_DDR1	SDRAM address
AP21	DDR1_A[4]	O	VDDQ_DDR1	SDRAM address
AL22	DDR1_A[5]	O	VDDQ_DDR1	SDRAM address
AM31	DDR1_A[6]	O	VDDQ_DDR1	SDRAM address
AM25	DDR1_A[7]	O	VDDQ_DDR1	SDRAM address
AK31	DDR1_A[8]	O	VDDQ_DDR1	SDRAM address

Pin ID	Package Pin Name	Type	Power Supply	Description
AL31	DDR1_A[9]	O	VDDQ_DDR1	SDRAM address
AK25	DDR1_ACT_N	O	VDDQ_DDR1	When low, indicates the activate (open row) command
AN29	DDR1_ALERT_N	I	VDDQ_DDR1	SDRAM CRC/parity error
AM30	DDR1_ATO	A		Analog test output (test pad) Reserved in BN Package and BK Package
AP24	DDR1_BA[0]	O	VDDQ_DDR1	SDRAM bank address
AK27	DDR1_BA[1]	O	VDDQ_DDR1	SDRAM bank address
AK29	DDR1_BG[0]	O	VDDQ_DDR1	SDRAM bank Group
AP23	DDR1_BG[1]	O	VDDQ_DDR1	SDRAM bank Group
AT24	DDR1_CK[0]	O	VDDQ_DDR1	SDRAM clock
AR26	DDR1_CK[1]	O	VDDQ_DDR1	SDRAM clock
AR25	DDR1_CK[2]	O	VDDQ_DDR1	SDRAM clock
AR27	DDR1_CK[3]	O	VDDQ_DDR1	SDRAM clock
AR24	DDR1_CK_N[0]	O	VDDQ_DDR1	SDRAM clock
AT26	DDR1_CK_N[1]	O	VDDQ_DDR1	SDRAM clock
AP25	DDR1_CK_N[2]	O	VDDQ_DDR1	SDRAM clock
AP27	DDR1_CK_N[3]	O	VDDQ_DDR1	SDRAM clock
AU21	DDR1_CKE[0]	O	VDDQ_DDR1	SDRAM clock enable
AT21	DDR1_CKE[1]	O	VDDQ_DDR1	SDRAM clock enable
AN28	DDR1_CKE[2]	O	VDDQ_DDR1	SDRAM clock enable
AK30	DDR1_CKE[3]	O	VDDQ_DDR1	SDRAM clock enable
AV22	DDR1_CS_N[0]	O	VDDQ_DDR1	SDRAM chip select
AW22	DDR1_CS_N[1]	O	VDDQ_DDR1	SDRAM chip select
AV21	DDR1_CS_N[2]	O	VDDQ_DDR1	SDRAM chip select
AN26	DDR1_CS_N[3]	O	VDDQ_DDR1	SDRAM chip select
AW34	DDR1_DM[0]	IO	VDDQ_DDR1	SDRAM data mask
AW25	DDR1_DM[1]	IO	VDDQ_DDR1	SDRAM data mask
AV38	DDR1_DM[2]	IO	VDDQ_DDR1	SDRAM data mask
AV29	DDR1_DM[3]	IO	VDDQ_DDR1	SDRAM data mask
AN34	DDR1_DM[4]	IO	VDDQ_DDR1	SDRAM data mask
AN37	DDR1_DM[5]	IO	VDDQ_DDR1	SDRAM data mask
AJ36	DDR1_DM[6]	IO	VDDQ_DDR1	SDRAM data mask
AJ37	DDR1_DM[7]	IO	VDDQ_DDR1	SDRAM data mask

Pin ID	Package Pin Name	Type	Power Supply	Description
AR32	DDR1_DM[8]	IO	VDDQ_DDR1	SDRAM data mask
AV32	DDR1_DQ[0]	IO	VDDQ_DDR1	SDRAM data
AW32	DDR1_DQ[1]	IO	VDDQ_DDR1	SDRAM data
AU25	DDR1_DQ[10]	IO	VDDQ_DDR1	SDRAM data
AV25	DDR1_DQ[11]	IO	VDDQ_DDR1	SDRAM data
AU23	DDR1_DQ[12]	IO	VDDQ_DDR1	SDRAM data
AW23	DDR1_DQ[13]	IO	VDDQ_DDR1	SDRAM data
AW24	DDR1_DQ[14]	IO	VDDQ_DDR1	SDRAM data
AV23	DDR1_DQ[15]	IO	VDDQ_DDR1	SDRAM data
AW36	DDR1_DQ[16]	IO	VDDQ_DDR1	SDRAM data
AU36	DDR1_DQ[17]	IO	VDDQ_DDR1	SDRAM data
AV36	DDR1_DQ[18]	IO	VDDQ_DDR1	SDRAM data
AU38	DDR1_DQ[19]	IO	VDDQ_DDR1	SDRAM data
AU32	DDR1_DQ[2]	IO	VDDQ_DDR1	SDRAM data
AV39	DDR1_DQ[20]	IO	VDDQ_DDR1	SDRAM data
AU39	DDR1_DQ[21]	IO	VDDQ_DDR1	SDRAM data
AW39	DDR1_DQ[22]	IO	VDDQ_DDR1	SDRAM data
AW37	DDR1_DQ[23]	IO	VDDQ_DDR1	SDRAM data
AU27	DDR1_DQ[24]	IO	VDDQ_DDR1	SDRAM data
AW27	DDR1_DQ[25]	IO	VDDQ_DDR1	SDRAM data
AV27	DDR1_DQ[26]	IO	VDDQ_DDR1	SDRAM data
AW28	DDR1_DQ[27]	IO	VDDQ_DDR1	SDRAM data
AU29	DDR1_DQ[28]	IO	VDDQ_DDR1	SDRAM data
AU30	DDR1_DQ[29]	IO	VDDQ_DDR1	SDRAM data
AW33	DDR1_DQ[3]	IO	VDDQ_DDR1	SDRAM data
AW30	DDR1_DQ[30]	IO	VDDQ_DDR1	SDRAM data
AV30	DDR1_DQ[31]	IO	VDDQ_DDR1	SDRAM data
AN35	DDR1_DQ[32]	IO	VDDQ_DDR1	SDRAM data
AM35	DDR1_DQ[33]	IO	VDDQ_DDR1	SDRAM data
AM36	DDR1_DQ[34]	IO	VDDQ_DDR1	SDRAM data
AR36	DDR1_DQ[35]	IO	VDDQ_DDR1	SDRAM data
AM34	DDR1_DQ[36]	IO	VDDQ_DDR1	SDRAM data
AR35	DDR1_DQ[37]	IO	VDDQ_DDR1	SDRAM data
AR34	DDR1_DQ[38]	IO	VDDQ_DDR1	SDRAM data

Pin ID	Package Pin Name	Type	Power Supply	Description
AP34	DDR1_DQ[39]	IO	VDDQ_DDR1	SDRAM data
AU34	DDR1_DQ[4]	IO	VDDQ_DDR1	SDRAM data
AP37	DDR1_DQ[40]	IO	VDDQ_DDR1	SDRAM data
AR37	DDR1_DQ[41]	IO	VDDQ_DDR1	SDRAM data
AR38	DDR1_DQ[42]	IO	VDDQ_DDR1	SDRAM data
AR39	DDR1_DQ[43]	IO	VDDQ_DDR1	SDRAM data
AM37	DDR1_DQ[44]	IO	VDDQ_DDR1	SDRAM data
AN39	DDR1_DQ[45]	IO	VDDQ_DDR1	SDRAM data
AN38	DDR1_DQ[46]	IO	VDDQ_DDR1	SDRAM data
AM38	DDR1_DQ[47]	IO	VDDQ_DDR1	SDRAM data
AH34	DDR1_DQ[48]	IO	VDDQ_DDR1	SDRAM data
AL36	DDR1_DQ[49]	IO	VDDQ_DDR1	SDRAM data
AV34	DDR1_DQ[5]	IO	VDDQ_DDR1	SDRAM data
AL34	DDR1_DQ[50]	IO	VDDQ_DDR1	SDRAM data
AK34	DDR1_DQ[51]	IO	VDDQ_DDR1	SDRAM data
AL35	DDR1_DQ[52]	IO	VDDQ_DDR1	SDRAM data
AH36	DDR1_DQ[53]	IO	VDDQ_DDR1	SDRAM data
AH35	DDR1_DQ[54]	IO	VDDQ_DDR1	SDRAM data
AJ34	DDR1_DQ[55]	IO	VDDQ_DDR1	SDRAM data
AH37	DDR1_DQ[56]	IO	VDDQ_DDR1	SDRAM data
AL37	DDR1_DQ[57]	IO	VDDQ_DDR1	SDRAM data
AL38	DDR1_DQ[58]	IO	VDDQ_DDR1	SDRAM data
AL39	DDR1_DQ[59]	IO	VDDQ_DDR1	SDRAM data
AU35	DDR1_DQ[6]	IO	VDDQ_DDR1	SDRAM data
AH38	DDR1_DQ[60]	IO	VDDQ_DDR1	SDRAM data
AK37	DDR1_DQ[61]	IO	VDDQ_DDR1	SDRAM data
AJ38	DDR1_DQ[62]	IO	VDDQ_DDR1	SDRAM data
AH39	DDR1_DQ[63]	IO	VDDQ_DDR1	SDRAM data
AV35	DDR1_DQ[7]	IO	VDDQ_DDR1	SDRAM data
AU26	DDR1_DQ[8]	IO	VDDQ_DDR1	SDRAM data
AV26	DDR1_DQ[9]	IO	VDDQ_DDR1	SDRAM data
AU33	DDR1_DQS[0]	IO	VDDQ_DDR1	SDRAM data strobe
AU24	DDR1_DQS[1]	IO	VDDQ_DDR1	SDRAM data strobe
AU37	DDR1_DQS[2]	IO	VDDQ_DDR1	SDRAM data strobe

Pin ID	Package Pin Name	Type	Power Supply	Description
AU28	DDR1_DQS[3]	IO	VDDQ_DDR1	SDRAM data strobe
AP36	DDR1_DQS[4]	IO	VDDQ_DDR1	SDRAM data strobe
AP38	DDR1_DQS[5]	IO	VDDQ_DDR1	SDRAM data strobe
AJ35	DDR1_DQS[6]	IO	VDDQ_DDR1	SDRAM data strobe
AK38	DDR1_DQS[7]	IO	VDDQ_DDR1	SDRAM data strobe
AR30	DDR1_DQS[8]	IO	VDDQ_DDR1	SDRAM data strobe
AV33	DDR1_DQS_N[0]	IO	VDDQ_DDR1	SDRAM data strobe
AV24	DDR1_DQS_N[1]	IO	VDDQ_DDR1	SDRAM data strobe
AV37	DDR1_DQS_N[2]	IO	VDDQ_DDR1	SDRAM data strobe
AV28	DDR1_DQS_N[3]	IO	VDDQ_DDR1	SDRAM data strobe
AP35	DDR1_DQS_N[4]	IO	VDDQ_DDR1	SDRAM data strobe
AP39	DDR1_DQS_N[5]	IO	VDDQ_DDR1	SDRAM data strobe
AK35	DDR1_DQS_N[6]	IO	VDDQ_DDR1	SDRAM data strobe
AK39	DDR1_DQS_N[7]	IO	VDDQ_DDR1	SDRAM data strobe
AP30	DDR1_DQS_N[8]	IO	VDDQ_DDR1	SDRAM data strobe
AK26	DDR1_DTO[0]	O	VDDQ_DDR1	Digital test output (test pad) Reserved in BK Package
AK24	DDR1_DTO[1]	O	VDDQ_DDR1	Digital test output (test pad) Reserved in BK Package
AT30	DDR1_ECC[0]	IO	VDDQ_DDR1	SDRAM data ECC
AR29	DDR1_ECC[1]	IO	VDDQ_DDR1	SDRAM data ECC
AT29	DDR1_ECC[2]	IO	VDDQ_DDR1	SDRAM data ECC
AT31	DDR1_ECC[3]	IO	VDDQ_DDR1	SDRAM data ECC
AP29	DDR1_ECC[4]	IO	VDDQ_DDR1	SDRAM data ECC
AP31	DDR1_ECC[5]	IO	VDDQ_DDR1	SDRAM data ECC
AT32	DDR1_ECC[6]	IO	VDDQ_DDR1	SDRAM data ECC
AP32	DDR1_ECC[7]	IO	VDDQ_DDR1	SDRAM data ECC
AP22	DDR1_MIRROR	O	VDDQ_DDR1	SDRAM mirror (optional DIMM signal)
AK22	DDR1_ODT[0]	O	VDDQ_DDR1	SDRAM on-die termination
AM28	DDR1_ODT[1]	O	VDDQ_DDR1	SDRAM on-die termination
AW21	DDR1_ODT[2]	O	VDDQ_DDR1	SDRAM on-die termination
AM22	DDR1_ODT[3]	O	VDDQ_DDR1	SDRAM on-die termination
AL27	DDR1_PARITY	O	VDDQ_DDR1	SDRAM parity
AN22	DDR1_QCSEN_N	O	VDDQ_DDR1	SDRAM quad CS enable (optional DIMM signal)
AN24	DDR1_RAM_RST_N	O	VDDQ_DDR1	SDRAM reset

Pin ID	Package Pin Name	Type	Power Supply	Description
AJ22	DDR1_VREFI[0]	A		IO ring VREFI net Reserved in BK Package
AG23	DDR1_VREFI[1]	A		IO ring VREFI net Reserved in BK Package
AG24	DDR1_VREFI[2]	A		IO ring VREFI net Reserved in BK Package
AG25	DDR1_VREFI[3]	A		IO ring VREFI net Reserved in BK Package
AG26	DDR1_VREFI[4]	A		IO ring VREFI net Reserved in BK Package
AH27	DDR1_VREFI[5]	A		IO ring VREFI net Reserved in BK Package
AH26	DDR1_VREFI[6]	A		IO ring VREFI net Reserved in BK Package
AJ25	DDR1_VREFI[7]	A		IO ring VREFI net Reserved in BK Package
AJ24	DDR1_VREFI[8]	A		IO ring VREFI net Reserved in BK Package
AH23	DDR1_VREFI[9]	A		IO ring VREFI net Reserved in BK Package
AH22	DDR1_VREFI_ZQ	A		IO ring VREFI ZQ net
AG22	DDR1_ZQ	A		ZQ resistor (to external calibration resistor)

5.1.2 High Speed Peripherals

5.1.2.1 PCIe x8

Table 5-2 PCIe x8 Pins

Pin ID	Package Pin Name	Type	Power Supply	Description
AK6	PCIE8_AMON0	O	VDD_PCIE8_15	Analog monitor bump Reserved in BK Package **Voltage range:** 0 – 1.575 V
AJ8	PCIE8_AMON1	O	VDD_PCIE8_15	Analog monitor bump Reserved in BK Package **Voltage range:** 0 – 1.575 V
AM9	PCIE8_ATT_BUT	I	VDDIO_18	Indicates that the system attention button was pressed Reserved in BK Package
AN7	PCIE8_ATT_IND[0]	O	VDDIO_18	Controls the system attention indicator Reserved in BK Package
AN8	PCIE8_ATT_IND[1]	O	VDDIO_18	Controls the system attention indicator Reserved in BK Package

Pin ID	Package Pin Name	Type	Power Supply	Description
AJ5	PCIE8_CMD_INT	I	VDDIO_18	Hot-plug controller command completed interrupt Reserved in BK Package
AL8	PCIE8_DMON0	O	VDD_PCIE8_09	Differential digital monitor bump Reserved in BK Package **Voltage range:** 0 – 0.9975 V
AK9	PCIE8_DMON1	O	VDD_PCIE8_09	Differential digital monitor bump Reserved in BK Package **Voltage range:** 0 – 0.9975 V
AL9	PCIE8_DMONB0	O	VDD_PCIE8_09	Differential digital monitor bump Reserved in BK Package **Voltage range:** 0 – 0.9975 V
AK8	PCIE8_DMONB1	O	VDD_PCIE8_09	Differential digital monitor bump Reserved in BK Package **Voltage range:** 0 – 0.9975 V
AM8	PCIE8_INTRL_CTRL	O	VDDIO_18	Electromechanical Interlock Control Reserved in BK Package
AM7	PCIE8_INTRL_ENG	I	VDDIO_18	System Electromechanical Interlock Engaged Reserved in BK Package
AH9	PCIE8_MRL_SENS	I	VDDIO_18	MRL sensor state Reserved in BK Package
AL10	PCIE8_PRES_ST	I	VDDIO_18	Presence detect state Reserved in BK Package
AJ6	PCIE8_PWR_CTRL	O	VDDIO_18	Controls the system power controller Reserved in BK Package
AJ7	PCIE8_PWR_FAULT	I	VDDIO_18	Power fault detect Reserved in BK Package
AH7	PCIE8_PWR_IND[0]	O	VDDIO_18	Controls the system power indicator Reserved in BK Package
AH8	PCIE8_PWR_IND[1]	O	VDDIO_18	Controls the system power indicator Reserved in BK Package
AN5	PCIE8_RBIAS0	IO	VDD_PCIE8_15	Bias resistor bump **Voltage range:** 0 – 1.575 V
AP6	PCIE8_RBIAS1	IO	VDD_PCIE8_15	Bias resistor bump **Voltage range:** 0 – 1.575 V
AL5	PCIE8_REF_CLKN	I	VDD_PCIE8_15	Differential reference clocks from pads
AL6	PCIE8_REF_CLKP	I	VDD_PCIE8_15	Differential reference clocks from pads
AR1	PCIE8_RXN[0]	I	VDD_PCIE8_15	Receive data differential pair
AP2	PCIE8_RXN[1]	I	VDD_PCIE8_15	Receive data differential pair
AM1	PCIE8_RXN[2]	I	VDD_PCIE8_15	Receive data differential pair
AL2	PCIE8_RXN[3]	I	VDD_PCIE8_15	Receive data differential pair

Pin ID	Package Pin Name	Type	Power Supply	Description
AH1	PCIE8_RXN[4]	I	VDD_PCIE8_15	Receive data differential pair
AG2	PCIE8_RXN[5]	I	VDD_PCIE8_15	Receive data differential pair
AE1	PCIE8_RXN[6]	I	VDD_PCIE8_15	Receive data differential pair
AD2	PCIE8_RXN[7]	I	VDD_PCIE8_15	Receive data differential pair
AP1	PCIE8_RXP[0]	I	VDD_PCIE8_15	Receive data differential pair
AN2	PCIE8_RXP[1]	I	VDD_PCIE8_15	Receive data differential pair
AL1	PCIE8_RXP[2]	I	VDD_PCIE8_15	Receive data differential pair
AK2	PCIE8_RXP[3]	I	VDD_PCIE8_15	Receive data differential pair
AJ1	PCIE8_RXP[4]	I	VDD_PCIE8_15	Receive data differential pair
AH2	PCIE8_RXP[5]	I	VDD_PCIE8_15	Receive data differential pair
AF1	PCIE8_RXP[6]	I	VDD_PCIE8_15	Receive data differential pair
AE2	PCIE8_RXP[7]	I	VDD_PCIE8_15	Receive data differential pair
AR4	PCIE8_TXN[0]	O	VDD_PCIE8_15	Transmit data differential pair
AP3	PCIE8_TXN[1]	O	VDD_PCIE8_15	Transmit data differential pair
AM4	PCIE8_TXN[2]	O	VDD_PCIE8_15	Transmit data differential pair
AL3	PCIE8_TXN[3]	O	VDD_PCIE8_15	Transmit data differential pair
AH4	PCIE8_TXN[4]	O	VDD_PCIE8_15	Transmit data differential pair
AG3	PCIE8_TXN[5]	O	VDD_PCIE8_15	Transmit data differential pair
AE4	PCIE8_TXN[6]	O	VDD_PCIE8_15	Transmit data differential pair
AD3	PCIE8_TXN[7]	O	VDD_PCIE8_15	Transmit data differential pair
AP4	PCIE8_TXP[0]	O	VDD_PCIE8_15	Transmit data differential pair
AN3	PCIE8_TXP[1]	O	VDD_PCIE8_15	Transmit data differential pair
AL4	PCIE8_TXP[2]	O	VDD_PCIE8_15	Transmit data differential pair
AK3	PCIE8_TXP[3]	O	VDD_PCIE8_15	Transmit data differential pair
AJ4	PCIE8_TXP[4]	O	VDD_PCIE8_15	Transmit data differential pair
AH3	PCIE8_TXP[5]	O	VDD_PCIE8_15	Transmit data differential pair
AF4	PCIE8_TXP[6]	O	VDD_PCIE8_15	Transmit data differential pair
AE3	PCIE8_TXP[7]	O	VDD_PCIE8_15	Transmit data differential pair

5.1.2.2 PCIe x4

Table 5-3 PCIe x4 Pins

Pin ID	Package Pin Name	Type	Power Supply	Description
AT16	PCIE4_0_AMON	O	VDD_PCIE4_0_15	Analog monitor bump Reserved in BK Package **Voltage range:** 0 – 1.575 V

Pin ID	Package Pin Name	Type	Power Supply	Description
AU15	PCIE4_0_ATT_BUT	I	VDDIO_18	Attention button pressed Reserved in BK Package
AR11	PCIE4_0_ATT_IND[0]	O	VDDIO_18	Controls the system attention indicator Reserved in BK Package
AM16	PCIE4_0_ATT_IND[1]	O	VDDIO_18	Controls the system attention indicator Reserved in BK Package
AR16	PCIE4_0_CMD_INT	I	VDDIO_18	Hot-plug controller command completed interrupt Reserved in BK Package
AL15	PCIE4_0_DMON	O	VDD_PCIE4_0_09	Differential digital monitor bump Reserved in BK Package **Voltage range:** 0 – 0.9975 V
AM15	PCIE4_0_DMONB	O	VDD_PCIE4_0_09	Differential digital monitor bump Reserved in BK Package **Voltage range:** 0 – 0.9975 V
AT18	PCIE4_0_INTRL_CTRL	O	VDDIO_18	Electromechanical Interlock Control Reserved in BK Package
AT17	PCIE4_0_INTRL_ENG	I	VDDIO_18	System Electromechanical Interlock Engaged Reserved in BK Package
AP17	PCIE4_0_MRL_SENS	I	VDDIO_18	MRL sensor state Reserved in BK Package
AU16	PCIE4_0_PRES_ST	I	VDDIO_18	Presence detect state Reserved in BK Package
AP16	PCIE4_0_PWR_CTRL	O	VDDIO_18	Controls the system power controller Reserved in BK Package
AR9	PCIE4_0_PWR_FAULT	I	VDDIO_18	Power fault detect Reserved in BK Package
AP10	PCIE4_0_PWR_IND[0]	O	VDDIO_18	Controls the system power indicator Reserved in BK Package
AP11	PCIE4_0_PWR_IND[1]	O	VDDIO_18	Controls the system power indicator Reserved in BK Package
AV17	PCIE4_0_RBIAS	IO	VDD_PCIE4_0_15	Bias resistor bump **Voltage range:** 0 – 1.575 V
AW15	PCIE4_0_REF_CLKN	I	VDD_PCIE4_0_15	Differential reference clocks from pads
AW16	PCIE4_0_REF_CLKP	I	VDD_PCIE4_0_15	Differential reference clocks from pads
AV14	PCIE4_0_RXN[0]	I	VDD_PCIE4_0_15	Receive data differential pair
AW12	PCIE4_0_RXN[1]	I	VDD_PCIE4_0_15	Receive data differential pair
AV10	PCIE4_0_RXN[2]	I	VDD_PCIE4_0_15	Receive data differential pair
AW9	PCIE4_0_RXN[3]	I	VDD_PCIE4_0_15	Receive data differential pair
AV13	PCIE4_0_RXP[0]	I	VDD_PCIE4_0_15	Receive data differential pair
AW13	PCIE4_0_RXP[1]	I	VDD_PCIE4_0_15	Receive data differential pair

Pin ID	Package Pin Name	Type	Power Supply	Description
AV11	PCIE4_0_RXP[2]	I	VDD_PCIE4_0_15	Receive data differential pair
AW10	PCIE4_0_RXP[3]	I	VDD_PCIE4_0_15	Receive data differential pair
AT14	PCIE4_0_TXN[0]	O	VDD_PCIE4_0_15	Receive data differential pair
AU13	PCIE4_0_TXN[1]	O	VDD_PCIE4_0_15	Receive data differential pair
AT11	PCIE4_0_TXN[2]	O	VDD_PCIE4_0_15	Receive data differential pair
AU10	PCIE4_0_TXN[3]	O	VDD_PCIE4_0_15	Receive data differential pair
AT13	PCIE4_0_TXP[0]	O	VDD_PCIE4_0_15	Receive data differential pair
AU12	PCIE4_0_TXP[1]	O	VDD_PCIE4_0_15	Receive data differential pair
AT10	PCIE4_0_TXP[2]	O	VDD_PCIE4_0_15	Receive data differential pair
AU9	PCIE4_0_TXP[3]	O	VDD_PCIE4_0_15	Receive data differential pair
AP13	PCIE4_1_AMON	O	VDD_PCIE4_1_15	Analog monitor bump Reserved in BK Package **Voltage range:** 0 – 1.575 V
AR7	PCIE4_1_ATT_BUT	I	VDDIO_18	Attention button pressed Reserved in BK Package
AM12	PCIE4_1_ATT_IND[0]	O	VDDIO_18	Controls the system attention indicator Reserved in BK Package
AN13	PCIE4_1_ATT_IND[1]	O	VDDIO_18	Controls the system attention indicator Reserved in BK Package
AJ13	PCIE4_1_CMD_INT	I	VDDIO_18	Hot-plug controller command completed interrupt Reserved in BK Package
AR12	PCIE4_1_DMON	O	VDD_PCIE4_1_09	Differential digital monitor bump Reserved in BK Package **Voltage range:** 0 – 0.9975 V
AP12	PCIE4_1_DMONB	O	VDD_PCIE4_1_09	Differential digital monitor bump Reserved in BK Package **Voltage range:** 0 – 0.9975 V
AP9	PCIE4_1_INTRL_CTRL	O	VDDIO_18	Electromechanical Interlock Control Reserved in BK Package
AU8	PCIE4_1_INTRL_ENG	I	VDDIO_18	System Electromechanical Interlock Engaged Reserved in BK Package
AK14	PCIE4_1_MRL_SENS	I	VDDIO_18	MRL sensor state Reserved in BK Package
AT8	PCIE4_1_PRES_ST	I	VDDIO_18	Presence detect state Reserved in BK Package
AL11	PCIE4_1_PWR_CTRL	O	VDDIO_18	Controls the system power controller Reserved in BK Package
AK13	PCIE4_1_PWR_FAULT	I	VDDIO_18	Power fault detect Reserved in BK Package

Pin ID	Package Pin Name	Type	Power Supply	Description
AL12	PCIE4_1_PWR_IND[0]	O	VDDIO_18	Controls the system power indicator Reserved in BK Package
AM13	PCIE4_1_PWR_IND[1]	O	VDDIO_18	Controls the system power indicator Reserved in BK Package
AV8	PCIE4_1_RBIAS	IO	VDD_PCIE4_1_15	Bias resistor bump **Voltage range:** 0 – 1.575 V
AV7	PCIE4_1_REF_CLKN	I	VDD_PCIE4_1_15	Differential reference clocks from pads
AW7	PCIE4_1_REF_CLKP	I	VDD_PCIE4_1_15	Differential reference clocks from pads
AV6	PCIE4_1_RXN[0]	I	VDD_PCIE4_1_15	Receive data differential pair
AW5	PCIE4_1_RXN[1]	I	VDD_PCIE4_1_15	Receive data differential pair
AV3	PCIE4_1_RXN[2]	I	VDD_PCIE4_1_15	Receive data differential pair
AW2	PCIE4_1_RXN[3]	I	VDD_PCIE4_1_15	Receive data differential pair
AV5	PCIE4_1_RXP[0]	I	VDD_PCIE4_1_15	Receive data differential pair
AW4	PCIE4_1_RXP[1]	I	VDD_PCIE4_1_15	Receive data differential pair
AV2	PCIE4_1_RXP[2]	I	VDD_PCIE4_1_15	Receive data differential pair
AW1	PCIE4_1_RXP[3]	I	VDD_PCIE4_1_15	Receive data differential pair
AT6	PCIE4_1_TXN[0]	O	VDD_PCIE4_1_15	Receive data differential pair
AU5	PCIE4_1_TXN[1]	O	VDD_PCIE4_1_15	Receive data differential pair
AT3	PCIE4_1_TXN[2]	O	VDD_PCIE4_1_15	Receive data differential pair
AU2	PCIE4_1_TXN[3]	O	VDD_PCIE4_1_15	Receive data differential pair
AT5	PCIE4_1_TXP[0]	O	VDD_PCIE4_1_15	Receive data differential pair
AU4	PCIE4_1_TXP[1]	O	VDD_PCIE4_1_15	Receive data differential pair
AT2	PCIE4_1_TXP[2]	O	VDD_PCIE4_1_15	Receive data differential pair
AU1	PCIE4_1_TXP[3]	O	VDD_PCIE4_1_15	Receive data differential pair

5.1.2.3 USB 3.0/2.0

Table 5-4 USB Pins

Pin ID	Package Pin Name	Type	Power Supply	Description
K27	USB2_0_CTRL	O	VDDIO_18	Port power control
D19	USB2_0_DM0	IO	VDD_USB2_0_33	USB D- signal. In normal operation it carries USB data to and from the USB 2.0 PHY. In *High-Speed* (**HS**) operation, this pin receives/transmits a maximum of 800 mV or 400 mV nominally. In *Full-Speed* (**FS**) or *Low-Speed* (**LS**) operation, this pin receives/transmits 3.3V nominally **Voltage range:** 0 – 3.3 V (In a 5V short condition, the signal can have a maximum of 5.25V on it with respect to the ground)

Pin ID	Package Pin Name	Type	Power Supply	Description
E19	USB2_0_DP0	IO	VDD_USB2_0_33	USB D+ signal. In normal operation it carries USB data to and from the USB 2.0 PHY. In *High-Speed* (**HS**) operation, this pin receives/transmits a maximum of 800 mV or 400 mV nominally. In *Full-Speed* (**FS**) or *Low-Speed* (**LS**) operation, this pin receives/transmits 3.3V nominally **Voltage range:** 0 – 3.3 V (In a 5V short condition, the signal can have a maximum of 5.25V on it with respect to the ground)
P24	USB2_0_ID0	IO	VDD_USB2_18	USB mini-receptacle identifier or alternate test point for DC points probes inside USB 2.0 PHY **Voltage range:** 0 – 1.8 V
P23	USB2_0_OVCUR	I	VDDIO_18	Port overcurrent
N23	USB2_0_RT	IO	VDD_USB2_18	Transmitter resistor tune pin. It connects to an external resistor that adjusts the USB 2.0 PHY's high-speed source impedance **Voltage range:** 0 – 1.8 V
M23	USB2_0_VBUS0	A		USB 5V signal. This is the USB 5V supply. A charge pump external to the USB 2.0 PHY must provide power to this pin. The nominal voltage for this pin is 5V **Voltage range:** 0 – 5.25 V
F20	USB2_0_XI	I	VDD_USB2_18	Crystal oscillator XI pin **Voltage range:** 0 – 1.8 V
G20	USB2_0_XO	I	VDD_USB2_18	Crystal oscillator XO pin or board reference clock input. **NOTE:** When the reference clock source is a crystal, XO pin is a connection to a crystal. When the reference clock source is an aexternal board clock, XO is an input. For modeling and simulation purposes, XO is declared as a pure input **Voltage range:** 0 – 1.8 V
K28	USB2_1_CTRL	O	VDDIO_18	Port power control
E22	USB2_1_DM0	IO	VDD_USB2_1_33	USB D- signal. In normal operation it carries USB data to and from the USB 2.0 PHY. In *High-Speed* (**HS**) operation, this pin receives/transmits a maximum of 800 mV or 400 mV nominally. In *Full-Speed* (**FS**) or *Low-Speed* (**LS**) operation, this pin receives/transmits 3.3V nominally **Voltage range:** 0 – 3.3 V (In a 5V short condition, the signal can have a maximum of 5.25V on it with respect to the ground)

Pin ID	Package Pin Name	Type	Power Supply	Description
F22	USB2_1_DP0	IO	VDD_USB2_1_33	USB D+ signal. In normal operation it carries USB data to and from the USB 2.0 PHY. In *High-Speed* (**HS**) operation, this pin receives/transmits a maximum of 800 mV or 400 mV nominally. In *Full-Speed* (**FS**) or *Low-Speed* (**LS**) operation, this pin receives/transmits 3.3V nominally **Voltage range:** 0 – 3.3 V (In a 5V short condition, the signal can have a maximum of 5.25V on it with respect to the ground)
N27	USB2_1_ID0	IO	VDD_USB2_18	USB mini-receptacle identifier or alternate test point for DC points probes inside USB 2.0 PHY **Voltage range:** 0 – 1.8 V
N24	USB2_1_OVCUR	I	VDDIO_18	Port overcurrent
N25	USB2_1_RT	IO	VDD_USB2_18	Transmitter resistor tune pin. It connects to an external resistor that adjusts the USB 2.0 PHY's high-speed source impedance **Voltage range:** 0 – 1.8 V
M25	USB2_1_VBUS0	A		USB 5V signal. This is the USB 5V supply. A charge pump external to the USB 2.0 PHY must provide power to this pin. The nominal voltage for this pin is 5V **Voltage range:** 0 – 5.25 V
F21	USB2_1_XI	I	VDD_USB2_18	Crystal oscillator XI pin **Voltage range:** 0 – 1.8 V
G21	USB2_1_XO	I	VDD_USB2_18	Crystal oscillator XO pin or board reference clock input. **NOTE:** When the reference clock source is a crystal, XO pin is a connection to a crystal. When the reference clock source is an aexternal board clock, XO is an input. For modeling and simulation purposes, XO is declared as a pure input **Voltage range:** 0 – 1.8 V
H28	USB2_2_CTRL	O	VDDIO_18	Port power control
D23	USB2_2_DM0	IO	VDD_USB2_2_33	USB D- signal. In normal operation it carries USB data to and from the USB 2.0 PHY. In *High-Speed* (**HS**) operation, this pin receives/transmits a maximum of 800 mV or 400 mV nominally. In *Full-Speed* (**FS**) or *Low-Speed* (**LS**) operation, this pin receives/transmits 3.3V nominally **Voltage range:** 0 – 3.3 V (In a 5V short condition, the signal can have a maximum of 5.25V on it with respect to the ground)

Pin ID	Package Pin Name	Type	Power Supply	Description
E23	USB2_2_DP0	IO	VDD_USB2_2_33	USB D+ signal. In normal operation it carries USB data to and from the USB 2.0 PHY. In *High-Speed* (**HS**) operation, this pin receives/transmits a maximum of 800 mV or 400 mV nominally. In *Full-Speed* (**FS**) or *Low-Speed* (**LS**) operation, this pin receives/transmits 3.3V nominally **Voltage range:** 0 – 3.3 V (In a 5V short condition, the signal can have a maximum of 5.25V on it with respect to the ground)
N26	USB2_2_ID0	IO	VDD_USB2_18	USB mini-receptacle identifier or alternate test point for DC points probes inside USB 2.0 PHY **Voltage range:** 0 – 1.8 V
M26	USB2_2_OVCUR	I	VDDIO_18	Port overcurrent
H26	USB2_2_RT	IO	VDD_USB2_18	Transmitter resistor tune pin. It connects to an external resistor that adjusts the USB 2.0 PHY's high-speed source impedance **Voltage range:** 0 – 1.8 V
G26	USB2_2_VBUS0	A		USB 5V signal. This is the USB 5V supply. A charge pump external to the USB 2.0 PHY must provide power to this pin. The nominal voltage for this pin is 5V **Voltage range:** 0 – 5.25 V
F24	USB2_2_XI	I	VDD_USB2_18	Crystal oscillator XI pin **Voltage range:** 0 – 1.8 V
G24	USB2_2_XO	I	VDD_USB2_18	Crystal oscillator XO pin or board reference clock input. **NOTE:** When the reference clock source is a crystal, XO pin is a connection to a crystal. When the reference clock source is an aexternal board clock, XO is an input. For modeling and simulation purposes, XO is declared as a pure input **Voltage range:** 0 – 1.8 V
H29	USB2_3_CTRL	O	VDDIO_18	Port power control
D26	USB2_3_DM0	IO	VDD_USB2_3_33	USB D- signal. In normal operation it carries USB data to and from the USB 2.0 PHY. In *High-Speed* (**HS**) operation, this pin receives/transmits a maximum of 800 mV or 400 mV nominally. In *Full-Speed* (**FS**) or *Low-Speed* (**LS**) operation, this pin receives/transmits 3.3V nominally **Voltage range:** 0 – 3.3 V (In a 5V short condition, the signal can have a maximum of 5.25V on it with respect to the ground)

Pin ID	Package Pin Name	Type	Power Supply	Description
E26	USB2_3_DP0	IO	VDD_USB2_3_33	USB D+ signal. In normal operation it carries USB data to and from the USB 2.0 PHY. In *High-Speed* (**HS**) operation, this pin receives/transmits a maximum of 800 mV or 400 mV nominally. In *Full-Speed* (**FS**) or *Low-Speed* (**LS**) operation, this pin receives/transmits 3.3V nominally **Voltage range:** 0 – 3.3 V (In a 5V short condition, the signal can have a maximum of 5.25V on it with respect to the ground)
G27	USB2_3_ID0	IO	VDD_USB2_18	USB mini-receptacle identifier or alternate test point for DC points probes inside USB 2.0 PHY **Voltage range:** 0 – 1.8 V
E28	USB2_3_OVCUR	I	VDDIO_18	Port overcurrent
F27	USB2_3_RT	IO		Transmitter resistor tune pin. It connects to an external resistor that adjusts the USB 2.0 PHY's high-speed source impedance **Voltage range:** 0 – 1.8 V
E27	USB2_3_VBUS0	A		USB 5V signal. This is the USB 5V supply. A charge pump external to the USB 2.0 PHY must provide power to this pin. The nominal voltage for this pin is 5V **Voltage range:** 0 – 5.25 V
F25	USB2_3_XI	I	VDD_USB2_18	Crystal oscillator XI pin **Voltage range:** 0 – 1.8 V
G25	USB2_3_XO	I	VDD_USB2_18	Crystal oscillator XO pin or board reference clock input. **NOTE:** When the reference clock source is a crystal, XO pin is a connection to a crystal. When the reference clock source is an aexternal board clock, XO is an input. For modeling and simulation purposes, XO is declared as a pure input **Voltage range:** 0 – 1.8 V
K25	USB2_4_CTRL	O	VDDIO_18	Port power control – USB 2.0 part
L24	USB2_4_OVCUR	I	VDDIO_18	Port overcurrent – USB 2.0 part
J20	USB2_5_CTRL	O	VDDIO_18	Port power control – USB 2.0 part
L19	USB2_5_OVCUR	I	VDDIO_18	Port overcurrent – USB 2.0 part
J24	USB3_0_CTRL	O	VDDIO_18	Port power control – USB 3.0 part

Pin ID	Package Pin Name	Type	Power Supply	Description
C26	USB3_0_DM0	IO	VDD_USB3_33	USB 2.0 D- signal. This bidirectional pin carries USB 2.0 data to and from the USB 3.0 PHY. In HS operation, this pin receives/transmits a maximum of 800 mV or 400 mV nominally. In FS or LS operation, this pin receives/transmits 3.3V nominally **Voltage range:** 0 – 3.3 V
B26	USB3_0_DP0	IO	VDD_USB3_33	USB 2.0 D+ signal. This bidirectional pin carries USB 2.0 data to and from the USB 3.0 PHY. In HS operation, this pin receives/transmits a maximum of 800 mV or 400 mV nominally. In FS or LS operation, this pin receives/transmits 3.3V nominally **Voltage range:** 0 – 3.3 V
L23	USB3_0_ID0	IO		USB 2.0 mini-receptacle identifier **Voltage range:** 0 – 1.8 V
K24	USB3_0_OVCUR	I	VDDIO_18	Port overcurrent – USB 3.0 part
B25	USB3_0_REFCLKN	I	VDD_USB3VP_0_09	USB 3.0 optional reference clock input **Voltage range:** 0 – 0.9 V
A25	USB3_0_REFCLKP	I	VDD_USB3VP_0_09	USB 3.0 optional reference clock input **Voltage range:** 0 – 0.9 V
J23	USB3_0_RESREF	A		USB 3.0 external reference resistor. This pin is for a 200 Ohms (±1%) 100-ppm/C precision resistor-to-ground on the board **Voltage range:** 0 – 250 mV
A23	USB3_0_RXON	I	VDD_USB3VP_0_09	USB 3.0 receive pin **Voltage range:** 0 – 0.9 V
B23	USB3_0_RXOP	I	VDD_USB3VP_0_09	USB 3.0 receive pin **Voltage range:** 0 – 0.9 V
B24	USB3_0_TXON	O	VDD_USB3TX_0_09	USB 3.0 transmit pin **Voltage range:** 0 – 0.9 V
C24	USB3_0_TXOP	O	VDD_USB3TX_0_09	USB 3.0 transmit pin **Voltage range:** 0 – 0.9 V
D24	USB3_0_VBUS0	A		USB 5V power supply pin. A charge pump external to the USB 3.0 PHY must provide power to this pin. The nominal voltage for this pin is 5V **Voltage range:** 0 – 5.25 V
J19	USB3_1_CTRL	O	VDDIO_18	Port power control – USB 3.0 part
C22	USB3_1_DM0	IO	VDD_USB3_33	USB 2.0 D- signal. This bidirectional pin carries USB 2.0 data to and from the USB 3.0 PHY. In HS operation, this pin receives/transmits a maximum of 800 mV or 400 mV nominally. In FS or LS operation, this pin receives/transmits 3.3V nominally **Voltage range:** 0 – 3.3 V

Pin ID	Package Pin Name	Type	Power Supply	Description
B22	USB3_1_DP0	IO	VDD_USB3_33	USB 2.0 D+ signal. This bidirectional pin carries USB 2.0 data to and from the USB 3.0 PHY. In HS operation, this pin receives/transmits a maximum of 800 mV or 400 mV nominally. In FS or LS operation, this pin receives/transmits 3.3V nominally **Voltage range:** 0 – 3.3 V
H19	USB3_1_ID0	IO		USB 2.0 mini-receptacle identifier **Voltage range:** 0 – 1.8 V
K19	USB3_1_OVCUR	I	VDDIO_18	Port overcurrent – USB 3.0 part
B21	USB3_1_REFCLKN	I	VDD_USB3VP_1_09	USB 3.0 optional reference clock input **Voltage range:** 0 – 0.9 V
A21	USB3_1_REFCLKP	I	VDD_USB3VP_1_09	USB 3.0 optional reference clock input **Voltage range:** 0 – 0.9 V
H20	USB3_1_RESREF	A		USB 3.0 external reference resistor. This pin is for a 200 Ohms (±1%) 100-ppm/C precision resistor-to-ground on the board **Voltage range:** 0 – 250 mV
A19	USB3_1_RXON	I	VDD_USB3VP_1_09	USB 3.0 receive pin **Voltage range:** 0 – 0.9 V
B19	USB3_1_RXOP	I	VDD_USB3VP_1_09	USB 3.0 receive pin **Voltage range:** 0 – 0.9 V
B20	USB3_1_TXON	O	VDD_USB3TX_1_09	USB 3.0 transmit pin **Voltage range:** 0 – 0.9 V
C20	USB3_1_TXOP	O	VDD_USB3TX_1_09	USB 3.0 transmit pin **Voltage range:** 0 – 0.9 V
D20	USB3_1_VBUS0	A		USB 5V power supply pin. A charge pump external to the USB 3.0 PHY must provide power to this pin. The nominal voltage for this pin is 5V **Voltage range:** 0 – 5.25 V

5.1.2.4 SATA

Table 5-5 SATA Pins

Pin ID	Package Pin Name	Type	Power Supply	Description
D31	SATA_P0ACTLED	O	VDDIO_18	P0 activity LED. It drives an external LED based on the port activity
E31	SATA_P0CPDET	I	VDDIO_18	Cold presence detect P0. It detects addition or removal of the powered-down device
E30	SATA_P0CPPOD	O	VDDIO_18	Cold presence power-on device P0. It enables power to the external device when asserted
F30	SATA_P0MPSW	I	VDDIO_18	Mechanical presence switch P0. It indicates the state of the external device presence switch

Pin ID	Package Pin Name	Type	Power Supply	Description
F29	SATA_P1ACTLED	O	VDDIO_18	P1 Activity LED. It drives an external LED based on the port activity
G29	SATA_P1CPDET	I	VDDIO_18	Cold Presence Detect P1. It detects addition or removal of the powered-down device
F28	SATA_P1CPPOD	O	VDDIO_18	Cold Presence Power-On Device P1. It enables power to the external device when asserted
G28	SATA_P1MPSW	I	VDDIO_18	Mechanical Presence Switch P1. It indicates the state of the external device presence switch
A31	SATA_REFCLKM	I	VDD_SATA_09	Reference clock differential pair **Voltage range:** 0 – 0.9 V
B31	SATA_REFCLKP	I	VDD_SATA_09	Reference clock differential pair **Voltage range:** 0 – 0.9 V
D29	SATA_RESREF	A		Reference resistor. This pin is for a 200 Ohms (±1%) 100-ppm/C precision resistor-to-ground on the board **Voltage range:** 0 – 250 mV
C30	SATA_RXN[0]	I	VDD_SATA_09	Receive data differential pair port 0 **Voltage range:** 0 – 0.9 V
B28	SATA_RXN[1]	I	VDD_SATA_09	Receive data differential pair port 1 **Voltage range:** 0 – 0.9 V
B30	SATA_RXP[0]	I	VDD_SATA_09	Receive data differential pair port 0 **Voltage range:** 0 – 0.9 V
C28	SATA_RXP[1]	I	VDD_SATA_09	Receive data differential pair port 1 **Voltage range:** 0 – 0.9 V
B29	SATA_TXN[0]	O	VDD_SATATX_09	Transmit data differential pair port 0 **Voltage range:** 0 – 0.9 V
A27	SATA_TXN[1]	O	VDD_SATATX_09	Transmit data differential pair port 1 **Voltage range:** 0 – 0.9 V
A29	SATA_TXP[0]	O	VDD_SATATX_09	Transmit data differential pair port 0 **Voltage range:** 0 – 0.9 V
B27	SATA_TXP[1]	O	VDD_SATATX_09	Transmit data differential pair port 1 **Voltage range:** 0 – 0.9 V

5.1.2.5 10 Gb Ethernet

Table 5-6 XGbE Pins

Pin ID	Package Pin Name	Type	Power Supply	Description
H14	XG0_AMON	O	VDD_XG0_15	Analog monitor bump Reserved in BK Package **Voltage range:** 0 – 1.575 V
G13	XG0_DMON	O	VDD_XG0_09	Differential digital monitor bump Reserved in BK Package **Voltage range:** 0 – 1.575 V

Pin ID	Package Pin Name	Type	Power Supply	Description
H13	XG0_DMONB	O	VDD_XG0_09	Differential digital monitor bump Reserved in BK Package **Voltage range:** 0 – 1.575 V
H15	XG0_RBIAS	IO	VDD_XG0_15	Bias resistor bump **Voltage range:** 0 – 1.575 V
H12	XG0_REF_CLKN	I	VDD_XG0_15	Differential reference clocks from pads
G12	XG0_REF_CLKP	I	VDD_XG0_15	Differential reference clocks from pads
A11	XG0_RXN[0]	I	VDD_XG0_15	Receive data differential pair This lane is used for 10GBASE-KR
B12	XG0_RXN[1]	I	VDD_XG0_15	Receive data differential pair
A13	XG0_RXN[2]	I	VDD_XG0_15	Receive data differential pair
B14	XG0_RXN[3]	I	VDD_XG0_15	Receive data differential pair
B11	XG0_RXP[0]	I	VDD_XG0_15	Receive data differential pair This lane is used for 10GBASE-KR
C12	XG0_RXP[1]	I	VDD_XG0_15	Receive data differential pair
B13	XG0_RXP[2]	I	VDD_XG0_15	Receive data differential pair
C14	XG0_RXP[3]	I	VDD_XG0_15	Receive data differential pair
D11	XG0_TXN[0]	O	VDD_XG0_15	Transmit data differential pair This lane is used for 10GBASE-KR
E12	XG0_TXN[1]	O	VDD_XG0_15	Transmit data differential pair
D13	XG0_TXN[2]	O	VDD_XG0_15	Transmit data differential pair
E14	XG0_TXN[3]	O	VDD_XG0_15	Transmit data differential pair
E11	XG0_TXP[0]	O	VDD_XG0_15	Transmit data differential pair This lane is used for 10GBASE-KR
F12	XG0_TXP[1]	O	VDD_XG0_15	Transmit data differential pair
E13	XG0_TXP[2]	O	VDD_XG0_15	Transmit data differential pair
F14	XG0_TXP[3]	O	VDD_XG0_15	Transmit data differential pair
H18	XG1_AMON	O	VDD_XG1_15	Analog monitor bump Reserved in BK Package **Voltage range:** 0 – 1.575 V
G17	XG1_DMON	O	VDD_XG1_09	Differential digital monitor bump Reserved in BK Package **Voltage range:** 0 – 1.575 V
H17	XG1_DMONB	O	VDD_XG1_09	Differential digital monitor bump Reserved in BK Package **Voltage range:** 0 – 1.575 V
G15	XG1_RBIAS	IO	VDD_XG1_15	Bias resistor bump **Voltage range:** 0 – 1.575 V
J16	XG1_REF_CLKN	I	VDD_XG1_15	Differential reference clocks from pads

Pin ID	Package Pin Name	Type	Power Supply	Description
H16	XG1_REF_CLKP	I	VDD_XG1_15	Differential reference clocks from pads
B18	XG1_RXN[0]	I	VDD_XG1_15	Receive data differential pair This lane is used for 10GBASE-KR
A17	XG1_RXN[1]	I	VDD_XG1_15	Receive data differential pair
B16	XG1_RXN[2]	I	VDD_XG1_15	Receive data differential pair
A15	XG1_RXN[3]	I	VDD_XG1_15	Receive data differential pair
C18	XG1_RXP[0]	I	VDD_XG1_15	Receive data differential pair This lane is used for 10GBASE-KR
B17	XG1_RXP[1]	I	VDD_XG1_15	Receive data differential pair
C16	XG1_RXP[2]	I	VDD_XG1_15	Receive data differential pair
B15	XG1_RXP[3]	I	VDD_XG1_15	Receive data differential pair
E18	XG1_TXN[0]	O	VDD_XG1_15	Transmit data differential pair This lane is used for 10GBASE-KR
D17	XG1_TXN[1]	O	VDD_XG1_15	Transmit data differential pair
E16	XG1_TXN[2]	O	VDD_XG1_15	Transmit data differential pair
D15	XG1_TXN[3]	O	VDD_XG1_15	Transmit data differential pair
F18	XG1_TXP[0]	O	VDD_XG1_15	Transmit data differential pair This lane is used for 10GBASE-KR
E17	XG1_TXP[1]	O	VDD_XG1_15	Transmit data differential pair
F16	XG1_TXP[2]	O	VDD_XG1_15	Transmit data differential pair
E15	XG1_TXP[3]	O	VDD_XG1_15	Transmit data differential pair

5.1.2.6 1 Gb Ethernet

Table 5-7 GMAC Pins

Pin ID	Package Pin Name	Type	Power Supply	Description
E4	G0_GP_IN	I	VDDIO_18	General purpose input
E3	G0_GP_OUT	O	VDDIO_18	General purpose output
E1	G0_MDC	O	VDDIO_18	Management data clock. The maximum frequency of this clock is 2.5 MHz. This clock is generated from the application clock through a clock divider
E2	G0_MDIO	IO	VDDIO_18	*Management Data Input/Output* (**MDIO**)
C7	G0_RX_CLK	I	VDDIO_18	Receive reference clock (125 MHz in 1 Gbps, 25 MHz in 100 Mbps, 2.5 MHz in 10 Mbps mode)
C5	G0_RX_DAT[0]	I	VDDIO_18	Receive data
C6	G0_RX_DAT[1]	I	VDDIO_18	Receive data
D5	G0_RX_DAT[2]	I	VDDIO_18	Receive data
D6	G0_RX_DAT[3]	I	VDDIO_18	Receive data

Pin ID	Package Pin Name	Type	Power Supply	Description
D7	G0_RX_DEN	I	VDDIO_18	Receive data
C4	G0_TX_CLK	O	VDDIO_18	Transmit reference clock (125 MHz in 1 Gbps, 25 MHz in 100 Mbps, 2.5 MHz in 10 Mbps mode)
C1	G0_TX_DAT[0]	O	VDDIO_18	Transmit data
C2	G0_TX_DAT[1]	O	VDDIO_18	Transmit data
C3	G0_TX_DAT[2]	O	VDDIO_18	Transmit data
D2	G0_TX_DAT[3]	O	VDDIO_18	Transmit data
D4	G0_TX_DEN	O	VDDIO_18	Transmit data enable
E7	G1_GP_IN	I	VDDIO_18	General purpose input
E8	G1_GP_OUT	O	VDDIO_18	General purpose output
E5	G1_MDC	O	VDDIO_18	Management data clock. The maximum frequency of this clock is 2.5 MHz. This clock is generated from the application clock through a clock divider
E6	G1_MDIO	IO	VDDIO_18	*Management Data Input/Output* (**MDIO**)
A7	G1_RX_CLK	I	VDDIO_18	Receive reference clock (125 MHz in 1 Gbps, 25 MHz in 100 Mbps, 2.5 MHz in 10 Mbps mode)
A5	G1_RX_DAT[0]	I	VDDIO_18	Receive data
A6	G1_RX_DAT[1]	I	VDDIO_18	Receive data
B5	G1_RX_DAT[2]	I	VDDIO_18	Receive data
B6	G1_RX_DAT[3]	I	VDDIO_18	Receive data
B7	G1_RX_DEN	I	VDDIO_18	Receive data
A3	G1_TX_CLK	O	VDDIO_18	Transmit reference clock (125 MHz in 1 Gbps, 25 MHz in 100 Mbps, 2.5 MHz in 10 Mbps mode)
A1	G1_TX_DAT[0]	O	VDDIO_18	Transmit data
A2	G1_TX_DAT[1]	O	VDDIO_18	Transmit data
B1	G1_TX_DAT[2]	O	VDDIO_18	Transmit data
B2	G1_TX_DAT[3]	O	VDDIO_18	Transmit data
B3	G1_TX_DEN	O	VDDIO_18	Transmit data enable

5.1.2.7 eMMC/SD

Table 5-8 eMMC/SD Pins

Pin ID	Package Pin Name	Type	Power Supply	Description
L36	SD_CAP0	A		Connected to 1 uF capacitor for stabilyzing LDO output voltage
M35	SD_CAP1	A		Connected to 1 uF capacitor for stabilyzing LDO output voltage

Pin ID	Package Pin Name	Type	Power Supply	Description
K36	SD_CARD_DETECT_N	I	VDDIO_18	Card detect signal, active low. When this is 0, it represents card is connected. When this signal goes from 0 to 1 card insertion interrupt is generated if enabled **NOTE:** This signal should be connected to ground if an eMMC device is connected to BE-M1000. As eMMC device is non-removable, card detection is not required.
N39	SD_CLK	O	VDD_SD_33	SD card transmit/receive clock
K34	SD_CMD	IO	VDD_SD_33	SD card command
L38	SD_DAT[0]	IO	VDD_SD_33	SD card data **NOTE:** Input data line must be pulled high, even if it is not used
L37	SD_DAT[1]	IO	VDD_SD_33	SD card data **NOTE:** Input data line must be pulled high, even if it is not used
M39	SD_DAT[2]	IO	VDD_SD_33	SD card data **NOTE:** Input data line must be pulled high, even if it is not used
M38	SD_DAT[3]	IO	VDD_SD_33	SD card data **NOTE:** Input data line must be pulled high, even if it is not used
M37	SD_DAT[4]	IO	VDD_SD_33	SD card data **NOTE:** Input data line must be pulled high, even if it is not used
N38	SD_DAT[5]	IO	VDD_SD_33	SD card data **NOTE:** Input data line must be pulled high, even if it is not used
N37	SD_DAT[6]	IO	VDD_SD_33	SD card data **NOTE:** Input data line must be pulled high, even if it is not used
N36	SD_DAT[7]	IO	VDD_SD_33	SD card data **NOTE:** Input data line must be pulled high, even if it is not used
M34	SD_LED_CTRL	O	VDDIO_18	SD card LED control. It warns user not to remove card while it is being accessed
N34	SD_REG_VOL_STABLE	I	VDDIO_18	Check whether host regulator voltage is stable
P36	SD_RST_N	O	VDD_SD_33	eMMC device reset, active low
L34	SD_VDD_ON	O	VDDIO_18	Switch on VDD1/VDD bus power for SD/eMMC card
M33	SD_VDD_SEL[0]	O	VDDIO_18	Select 1.8V voltage level for SD card
N33	SD_VDD_SEL[1]	O	VDDIO_18	Select 3V voltage level for SD card
P34	SD_VDD_SEL[2]	O	VDDIO_18	Select 3.3V voltage level for SD card

Pin ID	Package Pin Name	Type	Power Supply	Description
K35	SD_WRITE_PROT	I	VDDIO_18	Card write protect, active high. When this is 1, it represents card is write protected **NOTE:** This signal should be connected to ground if an eMMC device is connected to BE-M1000. As eMMC device does not have write protect physical switch similar to SD card, this signal is not required

5.1.3 Low Speed Peripherals

5.1.3.1 GPIO*32

Table 5-9 GPIO*32 Pins

Pin ID	Package Pin Name	Type	Power Supply	Description
G35	GPIO32[0]	IO	VDDIO_18	GPIO data
G36	GPIO32[1]	IO	VDDIO_18	GPIO data
J36	GPIO32[10]	IO	VDDIO_18	GPIO data
K31	GPIO32[11]	IO	VDDIO_18	GPIO data
K32	GPIO32[12]	IO	VDDIO_18	GPIO data
L31	GPIO32[13]	IO	VDDIO_18	GPIO data
L32	GPIO32[14]	IO	VDDIO_18	GPIO data
L33	GPIO32[15]	IO	VDDIO_18	GPIO data
M29	GPIO32[16]	IO	VDDIO_18	GPIO data
M30	GPIO32[17]	IO	VDDIO_18	GPIO data
M31	GPIO32[18]	IO	VDDIO_18	GPIO data
N30	GPIO32[19]	IO	VDDIO_18	GPIO data
G37	GPIO32[2]	IO	VDDIO_18	GPIO data
N31	GPIO32[20]	IO	VDDIO_18	GPIO data
N32	GPIO32[21]	IO	VDDIO_18	GPIO data
P32	GPIO32[22]	IO	VDDIO_18	GPIO data
P33	GPIO32[23]	IO	VDDIO_18	GPIO data
R28	GPIO32[24]	IO	VDDIO_18	GPIO data
R29	GPIO32[25]	IO	VDDIO_18	GPIO data
R30	GPIO32[26]	IO	VDDIO_18	GPIO data
R31	GPIO32[27]	IO	VDDIO_18	GPIO data
R33	GPIO32[28]	IO	VDDIO_18	GPIO data
R34	GPIO32[29]	IO	VDDIO_18	GPIO data
H32	GPIO32[3]	IO	VDDIO_18	GPIO data

Pin ID	Package Pin Name	Type	Power Supply	Description
T32	GPIO32[30]	IO	VDDIO_18	GPIO data
T33	GPIO32[31]	IO	VDDIO_18	GPIO data
H33	GPIO32[4]	IO	VDDIO_18	GPIO data
H34	GPIO32[5]	IO	VDDIO_18	GPIO data
H36	GPIO32[6]	IO	VDDIO_18	GPIO data
H37	GPIO32[7]	IO	VDDIO_18	GPIO data
J34	GPIO32[8]	IO	VDDIO_18	GPIO data
J35	GPIO32[9]	IO	VDDIO_18	GPIO data

5.1.3.2 UART

Table 5-10 UART Pins

Pin ID	Package Pin Name	Type	Power Supply	Description
J38	UART1_RXD	I	VDDIO_18	Receive data
J39	UART1_TXD	O	VDDIO_18	Transmit data
K38	UART2_RXD	I	VDDIO_18	Receive data
K39	UART2_TXD	O	VDDIO_18	Transmit data

5.1.3.3 SPI

Table 5-11 SPI Pins

Pin ID	Package Pin Name	Type	Power Supply	Description
F39	SPI1_CLK	O	VDDIO_18	Output clock
E38	SPI1_RXD	I	VDDIO_18	Receive data
E37	SPI1_SS_N[0]	O	VDDIO_18	Slave select
F37	SPI1_SS_N[1]	O	VDDIO_18	Slave select
F36	SPI1_SS_N[2]	O	VDDIO_18	Slave select
F35	SPI1_SS_N[3]	O	VDDIO_18	Slave select
E39	SPI1_TXD	O	VDDIO_18	Transmit data

5.1.3.4 eSPI

Table 5-12 eSPI Pins

Pin ID	Package Pin Name	Type	Power Supply	Description
C35	ESPI_ALERT[0]	I	VDDIO_18	eSPI alert
C37	ESPI_ALERT[1]	I	VDDIO_18	eSPI alert
C38	ESPI_ALERT[2]	I	VDDIO_18	eSPI alert
D35	ESPI_ALERT[3]	I	VDDIO_18	eSPI alert
D36	ESPI_ALERT[4]	I	VDDIO_18	eSPI alert

Pin ID	Package Pin Name	Type	Power Supply	Description
D37	ESPI_ALERT[5]	I	VDDIO_18	eSPI alert
E35	ESPI_ALERT[6]	I	VDDIO_18	eSPI alert
E34	ESPI_ALERT[7]	I	VDDIO_18	eSPI alert
A38	ESPI_CLK	IO	VDDIO_18	eSPI clock
A39	ESPI_DAT[0]	IO	VDDIO_18	eSPI data
B39	ESPI_DAT[1]	IO	VDDIO_18	eSPI data
C39	ESPI_DAT[2]	IO	VDDIO_18	eSPI data
D39	ESPI_DAT[3]	IO	VDDIO_18	eSPI data
D34	ESPI_RST	IO	VDDIO_18	eSPI reset
A35	ESPI_SS_N[0]	IO	VDDIO_18	eSPI slave select
A36	ESPI_SS_N[1]	IO	VDDIO_18	eSPI slave select
A37	ESPI_SS_N[2]	IO	VDDIO_18	eSPI slave select
B35	ESPI_SS_N[3]	IO	VDDIO_18	eSPI slave select
B36	ESPI_SS_N[4]	IO	VDDIO_18	eSPI slave select
B37	ESPI_SS_N[5]	IO	VDDIO_18	eSPI slave select
C33	ESPI_SS_N[6]	IO	VDDIO_18	eSPI slave select
C34	ESPI_SS_N[7]	IO	VDDIO_18	eSPI slave select

5.1.3.5 I^{2}C

Table 5-13 I^{2}C Bus Pins

Pin ID	Package Pin Name	Type	Power Supply	Description
G33	I2C1_SCL	IO	VDDIO_18	LSP I^{2}C #1 clock
G32	I2C1_SDA	IO	VDDIO_18	LSP I^{2}C #1 data
K30	I2C2_SCL	IO	VDDIO_18	LSP I^{2}C #2 clock
H30	I2C2_SDA	IO	VDDIO_18	LSP I^{2}C #2 data

5.1.3.6 SMBus

Table 5-14 SMBus Pins

Pin ID	Package Pin Name	Type	Power Supply	Description
G39	SMB1_CLK	IO	VDDIO_18	LSP SMBus #1 clock
H39	SMB1_DAT	IO	VDDIO_18	LSP SMBus #1 data
G38	SMB2_CLK	IO	VDDIO_18	LSP SMBus #2 clock
H38	SMB2_DAT	IO	VDDIO_18	LSP SMBus #2 data

5.1.4 Audio & Video

5.1.4.1 LVDS

Table 5-15 LVDS Pins

Pin ID	Package Pin Name	Type	Power Supply	Description
V33	LED_PWM	O	VDDIO_18	Brightness control
AC39	LVDS_L0_CLKN	O	VDDIO_18	LVDS clock
AC38	LVDS_L0_CLKP	O	VDDIO_18	LVDS clock
AF37	LVDS_L0_DATN[0]	O	VDDIO_18	LVDS data
AE38	LVDS_L0_DATN[1]	O	VDDIO_18	LVDS data
AD38	LVDS_L0_DATN[2]	O	VDDIO_18	LVDS data
AB37	LVDS_L0_DATN[3]	O	VDDIO_18	LVDS data
AF38	LVDS_L0_DATP[0]	O	VDDIO_18	LVDS data
AE39	LVDS_L0_DATP[1]	O	VDDIO_18	LVDS data
AD37	LVDS_L0_DATP[2]	O	VDDIO_18	LVDS data
AB38	LVDS_L0_DATP[3]	O	VDDIO_18	LVDS data
U39	LVDS_L1_CLKN	O	VDDIO_18	LVDS clock
U38	LVDS_L1_CLKP	O	VDDIO_18	LVDS clock
Y37	LVDS_L1_DATN[0]	O	VDDIO_18	LVDS data
W39	LVDS_L1_DATN[1]	O	VDDIO_18	LVDS data
V37	LVDS_L1_DATN[2]	O	VDDIO_18	LVDS data
T38	LVDS_L1_DATN[3]	O	VDDIO_18	LVDS data
Y38	LVDS_L1_DATP[0]	O	VDDIO_18	LVDS data
W38	LVDS_L1_DATP[1]	O	VDDIO_18	LVDS data
V38	LVDS_L1_DATP[2]	O	VDDIO_18	LVDS data
T37	LVDS_L1_DATP[3]	O	VDDIO_18	LVDS data
AC36	LVDS_L2_CLKN	O	VDDIO_18	LVDS clock
AC35	LVDS_L2_CLKP	O	VDDIO_18	LVDS clock
AF35	LVDS_L2_DATN[0]	O	VDDIO_18	LVDS data
AE35	LVDS_L2_DATN[1]	O	VDDIO_18	LVDS data
AD35	LVDS_L2_DATN[2]	O	VDDIO_18	LVDS data
AB34	LVDS_L2_DATN[3]	O	VDDIO_18	LVDS data
AF34	LVDS_L2_DATP[0]	O	VDDIO_18	LVDS data
AE36	LVDS_L2_DATP[1]	O	VDDIO_18	LVDS data
AD34	LVDS_L2_DATP[2]	O	VDDIO_18	LVDS data
AB35	LVDS_L2_DATP[3]	O	VDDIO_18	LVDS data

Pin ID	Package Pin Name	Type	Power Supply	Description
U36	LVDS_L3_CLKN	O	VDDIO_18	LVDS clock
U35	LVDS_L3_CLKP	O	VDDIO_18	LVDS clock
Y34	LVDS_L3_DATN[0]	O	VDDIO_18	LVDS data
W35	LVDS_L3_DATN[1]	O	VDDIO_18	LVDS data
V34	LVDS_L3_DATN[2]	O	VDDIO_18	LVDS data
T34	LVDS_L3_DATN[3]	O	VDDIO_18	LVDS data
Y35	LVDS_L3_DATP[0]	O	VDDIO_18	LVDS data
W36	LVDS_L3_DATP[1]	O	VDDIO_18	LVDS data
V35	LVDS_L3_DATP[2]	O	VDDIO_18	LVDS data
T35	LVDS_L3_DATP[3]	O	VDDIO_18	LVDS data
AF24	LVDS_PLL_27M	I	VDDIO_18	PLL reference clock 27 MHz IN – LVDS
AD33	LVDS_VREF	A		Signal reference

5.1.4.2 *HDMI*

Table 5-16 HDMI Pins

Pin ID	Package Pin Name	Type	Power Supply	Description
B8	HDMI_CLKN	O		Negative TMDS differential line driver clock output **Voltage range:** For the permitted voltage range, refer to ***High-Definition Multimedia Interface Specification***, Version 2.0, “Electrical Specification” section
C8	HDMI_CLKP	O		Positive TMDS differential line driver clock output **Voltage range:** For the permitted voltage range, refer to ***High-Definition Multimedia Interface Specification***, Version 2.0, “Electrical Specification” section
B9	HDMI_DATN[0]	O		TMDS data **Voltage range:** For the permitted voltage range, refer to ***High-Definition Multimedia Interface Specification***, Version 2.0, “Electrical Specification” section
E9	HDMI_DATN[1]	O		TMDS data **Voltage range:** For the permitted voltage range, refer to ***High-Definition Multimedia Interface Specification***, Version 2.0, “Electrical Specification” section

Pin ID	Package Pin Name	Type	Power Supply	Description
C10	HDMI_DATN[2]	O		TMDS data **Voltage range:** For the permitted voltage range, refer to ***High-Definition Multimedia Interface Specification***, Version 2.0, "Electrical Specification" section
A9	HDMI_DATP[0]	O		TMDS data **Voltage range:** For the permitted voltage range, refer to ***High-Definition Multimedia Interface Specification***, Version 2.0, "Electrical Specification" section
D9	HDMI_DATP[1]	O		TMDS data **Voltage range:** For the permitted voltage range, refer to ***High-Definition Multimedia Interface Specification***, Version 2.0, "Electrical Specification" section
B10	HDMI_DATP[2]	O		TMDS data **Voltage range:** For the permitted voltage range, refer to ***High-Definition Multimedia Interface Specification***, Version 2.0, "Electrical Specification" section
K18	HDMI_DB_BISTDONE	O	VDDIO_18	Indication of *Built-In Self Test* (**BIST**) test completion
J18	HDMI_DB_BISTEN	I	VDDIO_18	Control enable signal for BIST test
L17	HDMI_DB_BISTOK	O	VDDIO_18	Indication of BIST Test pass
M16	HDMI_DB_DAT[0]	O	VDDIO_18	Indication that path between I/O pad and *analog front end* (**AFE**) is valid Reserved in BN Package and BK Package
N16	HDMI_DB_DAT[1]	O	VDDIO_18	Indication that path between I/O pad and AFE is valid Reserved in BN Package and BK Package
M17	HDMI_DB_DAT[2]	O	VDDIO_18	Indication that path between I/O pad and AFE is valid Reserved in BN Package and BK Package
N17	HDMI_DB_DAT[3]	O	VDDIO_18	Indication that path between I/O pad and AFE is valid Reserved in BN Package and BK Package
N18	HDMI_DB_DAT[4]	O	VDDIO_18	Indication that path between I/O pad and AFE is valid Reserved in BN Package and BK Package

Pin ID	Package Pin Name	Type	Power Supply	Description
P18	HDMI_DB_DAT[5]	O	VDDIO_18	Indication that path between I/O pad and AFE is valid Reserved in BN Package and BK Package
M19	HDMI_DB_DAT[6]	O	VDDIO_18	Indication that path between I/O pad and AFE is valid Reserved in BN Package and BK Package
N19	HDMI_DB_DAT[7]	O	VDDIO_18	Indication that path between I/O pad and AFE is valid Reserved in BN Package and BK Package
P19	HDMI_DB_DAT[8]	O	VDDIO_18	Indication that path between I/O pad and AFE is valid Reserved in BN Package and BK Package
M20	HDMI_DB_DAT[9]	O	VDDIO_18	Indication that path between I/O pad and AFE is valid Reserved in BN Package and BK Package
N20	HDMI_DB_EN	I	VDDIO_18	Control enable signal for I/O continuity test Reserved in BK Package
P20	HDMI_DB_ENHPDRXSENSE	I	VDDIO_18	Enables hot plug detect and RXSENSE for HDMI operation
H22	HDMI_DB_EXTERNAL	I	VDDIO_18	HDMI PHY Debug Interface
N21	HDMI_DB_PDDQ	I	VDDIO_18	Shuts off low-to-high bias voltage generators in the MPLL and support blocks, because the generators are not under direct power-down control
J22	HDMI_DB_PHY_RESET	I	VDDIO_18	PHY reset. This signal places the digital section of the macro into a reset state
K22	HDMI_DB_PHYDTB0	O	VDDIO_18	Digital test bus Reserved in BN Package and BK Package
M21	HDMI_DB_PHYDTB1	O	VDDIO_18	Digital test bus Reserved in BN Package and BK Package
P21	HDMI_DB_RXSENSE	O	VDDIO_18	Rx presence detection signal for all TMDS data lanes for HDMI mode of operation. Asserted high if TMDS lines have a 3.3V pull-up resistor connected to them
N22	HDMI_DB_SNK_DET_I	O	VDDIO_18	Sink detected signal for HDMI Reserved in BK Package
P22	HDMI_DB_SVSRET_MODEZ	I	VDDIO_18	Enables retention mode

Pin ID	Package Pin Name	Type	Power Supply	Description
R22	HDMI_DB_TX_PWRON	I	VDDIO_18	Power-on input. This signal is used to power up the entire macro. All analog blocks are released from power-down mode
R16	HDMI_DB_TX_READY	O	VDDIO_18	Indicates that the HDMI PHY is ready to transmit data
D10	HDMI_DDCCEC	IO		Ground reference for the hot plug detect signal
H9	HDMI_HPD	IO		Hot plug detect signal for HDMI
T14	HDMI_PLL_27M	I	VDDIO_18	PLL Reference Clock 27MHz IN – HDMI
E10	HDMI_RESREF	A		Reference resistor connection. This pin is for a 1620 Ohms (± 1%) reference resistor (connected to ground)
G9	HDMI_SCL	IO	VDDIO_18	HDMI I^{2}C clock input
G10	HDMI_SDA	IO	VDDIO_18	HDMI I^{2}C data input

5.1.4.3 HDA

Table 5-17 HDA Pins

Pin ID	Package Pin Name	Type	Power Supply	Description
C32	HDA_BCLK	O	VDDIO_18	Codec link 24 MHz frequency
D32	HDA_RST_N	O	VDDIO_18	Codec reset, active low
A34	HDA_SDI[0]	IO	VDDIO_18	Codec serial data input
B33	HDA_SDI[1]	IO	VDDIO_18	Codec serial data input
A33	HDA_SDO[0]	IO	VDDIO_18	Codec serial data output
B32	HDA_SDO[1]	IO	VDDIO_18	Codec serial data output
D33	HDA_SYNC	O	VDDIO_18	Codec 48 kHz frame synchronization

5.1.4.4 I^{2}S

Table 5-18 I^{2}S Pins

Pin ID	Package Pin Name	Type	Power Supply	Description
F32	I2S_SCK	I	VDDIO_18	I^{2}S continuous serial clock
G31	I2S_SDI	I	VDDIO_18	I^{2}S serial data input
F33	I2S_SDO	O	VDDIO_18	I^{2}S serial data output
E33	I2S_WS	I	VDDIO_18	I^{2}S word select

5.1.5 System Control

Table 5-19 System Control Pins

Pin ID	Package Pin Name	Type	Power Supply	Description
AG18	ARC_DBG_TF	O	VDDIO_18	Indicates that a triple fault exception has occurred

Pin ID	Package Pin Name	Type	Power Supply	Description
AH18	ARC_WDT_RESET	O	VDDIO_18	Watchdog reset
A32	CLK24M_OUT	O	VDDIO_18	Output clock 48 MHz/2, In some USB purposes
AJ16	CLK25M	I	VDDIO_18	PLL Reference Clock 25 MHz
AN17	GPIO8[0]	IO	VDDIO_18	SM GPIO Data
AM17	GPIO8[1]	IO	VDDIO_18	SM GPIO Data
AK17	GPIO8[2]	IO	VDDIO_18	SM GPIO Data
AJ18	GPIO8[3]	IO	VDDIO_18	SM GPIO Data
AJ19	GPIO8[4]	IO	VDDIO_18	SM GPIO Data
AJ20	GPIO8[5]	IO	VDDIO_18	SM GPIO Data
AH19	GPIO8[6]	IO	VDDIO_18	SM GPIO Data
AH20	GPIO8[7]	IO	VDDIO_18	SM GPIO Data
AL20	I2C0_SCL	IO	VDDIO_18	SM I^{2}C clock
AL19	I2C0_SDA	IO	VDDIO_18	SM I^{2}C data
AJ15	RESET_N	I	VDDIO_18	System reset, active low
AV18	SMB0_CLK	IO	VDDIO_18	SM SMBus clock
AW18	SMB0_DAT	IO	VDDIO_18	SM SMBus data
AW19	SPI0_CLK	O	VDDIO_18	Output clock
AT19	SPI0_RXD	I	VDDIO_18	Receive data
AR19	SPI0_SS_N[0]	O	VDDIO_18	Slave select
AP19	SPI0_SS_N[1]	O	VDDIO_18	Slave select
AN20	SPI0_SS_N[2]	O	VDDIO_18	Slave select
AM20	SPI0_SS_N[3]	O	VDDIO_18	Slave select
AU19	SPI0_TXD	O	VDDIO_18	Transmit data
AM19	TEST_0	I	VDDIO_18	Test point 0 Reserved in BK Package
AL18	TURBO_BOOT	I	VDDIO_18	Controls boot mode of the System Control Processor: 0 – 500 MHz (TURBO): 1 – 250 MHz
AH13	TRSTN	I	VDDIO_18	Test reset
AK18	UART0_RXD	I	VDDIO_18	Receive data
AK19	UART0_TXD	O	VDDIO_18	Transmit data

5.1.6 System Debug

Table 5-20 System Debug Pins

Pin ID	Package Pin Name	Type	Power Supply	Description
AG15	CS_CLK	O	VDDIO_18	Trace port clock Reserved in BK Package
AG16	CS_CTRL	O	VDDIO_18	Trace port control Reserved in BK Package
AE5	CS_DAT[0]	O	VDDIO_18	Trace port data Reserved in BK Package
AE6	CS_DAT[1]	O	VDDIO_18	Trace port data Reserved in BK Package
AF12	CS_DAT[10]	O	VDDIO_18	Trace port data Reserved in BK Package
AG6	CS_DAT[11]	O	VDDIO_18	Trace port data Reserved in BK Package
AG7	CS_DAT[12]	O	VDDIO_18	Trace port data Reserved in BK Package
AG8	CS_DAT[13]	O	VDDIO_18	Trace port data Reserved in BK Package
AG10	CS_DAT[14]	O	VDDIO_18	Trace port data Reserved in BK Package
AG11	CS_DAT[15]	O	VDDIO_18	Trace port data Reserved in BK Package
AE9	CS_DAT[2]	O	VDDIO_18	Trace port data Reserved in BK Package
AE10	CS_DAT[3]	O	VDDIO_18	Trace port data Reserved in BK Package
AE11	CS_DAT[4]	O	VDDIO_18	Trace port data Reserved in BK Package
AF6	CS_DAT[5]	O	VDDIO_18	Trace port data Reserved in BK Package
AF7	CS_DAT[6]	O	VDDIO_18	Trace port data Reserved in BK Package
AF9	CS_DAT[7]	O	VDDIO_18	Trace port data Reserved in BK Package
AF10	CS_DAT[8]	O	VDDIO_18	Trace port data Reserved in BK Package
AF11	CS_DAT[9]	O	VDDIO_18	Trace port data Reserved in BK Package
AE12	CS_SWCLK_TCK	I	VDDIO_18	Serial wire and TAP clock
AF13	CS_SWDIO_TMS	IO	VDDIO_18	Combined serial wire input/output
AG13	CS_TDI	I	VDDIO_18	JTAG TAP data IN
AH17	CS_TDO	O	VDDIO_18	JTAG TAP data OUT

Pin ID	Package Pin Name	Type	Power Supply	Description
AG14	CS_TRST_N	I	VDDIO_18	TAP Asynchronous reset

5.1.7 Power and Ground

5.1.7.1 Core Supply

Table 5-21 Core Supply Pins

Pin ID	Package Pin Name	Type	Description
AB16	VDD	P	Core power
AB17	VDD	P	Core power
AB18	VDD	P	Core power
AB19	VDD	P	Core power
AB20	VDD	P	Core power
AB21	VDD	P	Core power
AB22	VDD	P	Core power
AB23	VDD	P	Core power
AB24	VDD	P	Core power
AB25	VDD	P	Core power
AB26	VDD	P	Core power
AB27	VDD	P	Core power
AB28	VDD	P	Core power
AB29	VDD	P	Core power
AD14	VDD	P	Core power
AD15	VDD	P	Core power
AD16	VDD	P	Core power
AD17	VDD	P	Core power
AD18	VDD	P	Core power
AD19	VDD	P	Core power
AD20	VDD	P	Core power
AD21	VDD	P	Core power
AD22	VDD	P	Core power
AD23	VDD	P	Core power
AD24	VDD	P	Core power
AD25	VDD	P	Core power
AD26	VDD	P	Core power
AD27	VDD	P	Core power
AD28	VDD	P	Core power

Pin ID	Package Pin Name	Type	Description
AD29	VDD	P	Core power
AD30	VDD	P	Core power
AD31	VDD	P	Core power
AD32	VDD	P	Core power
AF26	VDD	P	Core power
AF27	VDD	P	Core power
AF30	VDD	P	Core power
AG28	VDD	P	Core power
T15	VDD	P	Core power
T16	VDD	P	Core power
T17	VDD	P	Core power
T18	VDD	P	Core power
T19	VDD	P	Core power
T20	VDD	P	Core power
T21	VDD	P	Core power
T22	VDD	P	Core power
T23	VDD	P	Core power
T24	VDD	P	Core power
T25	VDD	P	Core power
T26	VDD	P	Core power
T27	VDD	P	Core power
T28	VDD	P	Core power
T29	VDD	P	Core power
T30	VDD	P	Core power
V15	VDD	P	Core power
V16	VDD	P	Core power
V17	VDD	P	Core power
V18	VDD	P	Core power
V19	VDD	P	Core power
V20	VDD	P	Core power
V21	VDD	P	Core power
V22	VDD	P	Core power
V23	VDD	P	Core power
V24	VDD	P	Core power

Pin ID	Package Pin Name	Type	Description
V25	VDD	P	Core power
V26	VDD	P	Core power
V27	VDD	P	Core power
V28	VDD	P	Core power
Y16	VDD	P	Core power
Y17	VDD	P	Core power
Y18	VDD	P	Core power
Y19	VDD	P	Core power
Y20	VDD	P	Core power
Y21	VDD	P	Core power
Y22	VDD	P	Core power
Y23	VDD	P	Core power
Y24	VDD	P	Core power
Y25	VDD	P	Core power
Y26	VDD	P	Core power
Y27	VDD	P	Core power
Y28	VDD	P	Core power
Y29	VDD	P	Core power

5.1.7.2 0.95V Voltage Supply

Table 5-22 0.95V Voltage Supply Pins

Pin ID	Package Pin Name	Type	Description
F9	VDD_HDMI_09	P	0.9V analog power supply
AN14	VDD_PCIE4_0_09	P	PCIe PHY analog 0.95V
AP14	VDD_PCIE4_0_09	P	PCIe PHY analog 0.95V
AR15	VDD_PCIE4_0_09	P	PCIe PHY analog 0.95V
AM10	VDD_PCIE4_1_09	P	PCIe PHY analog 0.95V
AN10	VDD_PCIE4_1_09	P	PCIe PHY analog 0.95V
AN11	VDD_PCIE4_1_09	P	PCIe PHY analog 0.95V
AF5	VDD_PCIE8_09	P	PCIe PHY analog 0.95V
AH5	VDD_PCIE8_09	P	PCIe PHY analog 0.95V
AM6	VDD_PCIE8_09	P	PCIe PHY analog 0.95V
AP5	VDD_PCIE8_09	P	PCIe PHY analog 0.95V
AP7	VDD_PCIE8_09	P	PCIe PHY analog 0.95V
AR6	VDD_PCIE8_09	P	PCIe PHY analog 0.95V

Pin ID	Package Pin Name	Type	Description
J26	VDD_SATA_09	P	SATA PHY analog and digital supply
J27	VDD_SATATX_09	P	SATA PHY transmit supply
J21	VDD_USB2_09	P	Digital Power Supply
K21	VDD_USB2_09	P	Digital Power Supply
A20	VDD_USB3_0_09	P	0.9 V PHY analog and digital high-speed supply
A24	VDD_USB3_1_09	P	0.9 V PHY analog and digital high-speed supply
D25	VDD_USB3TX_0_09	P	0.9 V PHY transmit supply
C21	VDD_USB3TX_1_09	P	0.9 V PHY transmit supply
E25	VDD_USB3VP_0_09	P	0.9 V PHY analog and digital SuperSpeed supply
D21	VDD_USB3VP_1_09	P	0.9 V PHY analog and digital SuperSpeed supply
F11	VDD_XG0_09	P	XGbE PHY analog 0.95V
G11	VDD_XG0_09	P	XGbE PHY analog 0.95V
H11	VDD_XG0_09	P	XGbE PHY analog 0.95V
K16	VDD_XG1_09	P	XGbE PHY analog 0.95V
K17	VDD_XG1_09	P	XGbE PHY analog 0.95V
L16	VDD_XG1_09	P	XGbE PHY analog 0.95V

5.1.7.3 PLL Supply

Table 5-23 PLL Supply Pins

Pin ID	Package Pin Name	Type	Description
P16	VDDPLL_0_09	P	PLL power
W31	VDDPLL_1_09	P	PLL power
AF32	VDDPLL_2_09	P	PLL power
AN19	VDDPLL_3_09	P	PLL power
J14	VDDPLL_HDMI_09	P	HDMI PLL power

5.1.7.4 DDR Supply

Table 5-24 DDR Supply Pins

Pin ID	Package Pin Name	Type	Description
AA10	VDDQ_DDR0	P	VDDQ voltage supply
AC7	VDDQ_DDR0	P	VDDQ voltage supply
K11	VDDQ_DDR0	P	VDDQ voltage supply
K9	VDDQ_DDR0	P	VDDQ voltage supply
L12	VDDQ_DDR0	P	VDDQ voltage supply
L15	VDDQ_DDR0	P	VDDQ voltage supply

Pin ID	Package Pin Name	Type	Description
N14	VDDQ_DDR0	P	VDDQ voltage supply
N15	VDDQ_DDR0	P	VDDQ voltage supply
P9	VDDQ_DDR0	P	VDDQ voltage supply
R14	VDDQ_DDR0	P	VDDQ voltage supply
R15	VDDQ_DDR0	P	VDDQ voltage supply
R7	VDDQ_DDR0	P	VDDQ voltage supply
R9	VDDQ_DDR0	P	VDDQ voltage supply
T13	VDDQ_DDR0	P	VDDQ voltage supply
U13	VDDQ_DDR0	P	VDDQ voltage supply
U9	VDDQ_DDR0	P	VDDQ voltage supply
V10	VDDQ_DDR0	P	VDDQ voltage supply
V8	VDDQ_DDR0	P	VDDQ voltage supply
Y12	VDDQ_DDR0	P	VDDQ voltage supply
AG34	VDDQ_DDR1	P	VDDQ voltage supply
AG36	VDDQ_DDR1	P	VDDQ voltage supply
AH31	VDDQ_DDR1	P	VDDQ voltage supply
AH33	VDDQ_DDR1	P	VDDQ voltage supply
AJ30	VDDQ_DDR1	P	VDDQ voltage supply
AJ32	VDDQ_DDR1	P	VDDQ voltage supply
AK21	VDDQ_DDR1	P	VDDQ voltage supply
AL29	VDDQ_DDR1	P	VDDQ voltage supply
AL33	VDDQ_DDR1	P	VDDQ voltage supply
AM21	VDDQ_DDR1	P	VDDQ voltage supply
AM32	VDDQ_DDR1	P	VDDQ voltage supply
AN21	VDDQ_DDR1	P	VDDQ voltage supply
AN30	VDDQ_DDR1	P	VDDQ voltage supply
AP33	VDDQ_DDR1	P	VDDQ voltage supply
AR28	VDDQ_DDR1	P	VDDQ voltage supply
AT34	VDDQ_DDR1	P	VDDQ voltage supply
AT36	VDDQ_DDR1	P	VDDQ voltage supply
AT38	VDDQ_DDR1	P	VDDQ voltage supply
AU31	VDDQ_DDR1	P	VDDQ voltage supply
AW31	VDDQ_DDR1	P	VDDQ voltage supply

5.1.7.5 1.5V Voltage Supply

Table 5-25 1.5V Voltage Supply Pins

Pin ID	Package Pin Name	Type	Description
AR8	VDD_PCIE4_0_15	P	PCIe PHY IO 1.5V
AP8	VDD_PCIE4_1_15	P	PCIe PHY IO 1.5V
AJ10	VDD_PCIE8_15	P	PCIe PHY IO 1.5V
AJ11	VDD_PCIE8_15	P	PCIe PHY IO 1.5V
F13	VDD_XG0_15	P	XGbE PHY IO 1.5V
J17	VDD_XG1_15	P	XGbE PHY IO 1.5V

5.1.7.6 1.8V Voltage Supply

Table 5-26 1.8V Voltage Supply Pins

Pin ID	Package Pin Name	Type	Description
AB14	VDD_DDR0_PLL	P	PLL power supply
AB15	VDD_DDR0_PLL	P	PLL power supply
AD13	VDD_DDR0_PLL	P	PLL power supply
V14	VDD_DDR0_PLL	P	PLL power supply
Y14	VDD_DDR0_PLL	P	PLL power supply
Y15	VDD_DDR0_PLL	P	PLL power supply
AG29	VDD_DDR1_PLL	P	PLL power supply
AG30	VDD_DDR1_PLL	P	PLL power supply
AH28	VDD_DDR1_PLL	P	PLL power supply
AH29	VDD_DDR1_PLL	P	PLL power supply
AH30	VDD_DDR1_PLL	P	PLL power supply
AJ29	VDD_DDR1_PLL	P	PLL power supply
F10	VDD_HDMI_18	P	1.8V analog power supply
M27	VDD_PVT_18	P	PVT sensor power
K26	VDD_SATA_18	P	SATA PHY High-voltage power supply
G23	VDD_USB2_18	P	1.8V Analog Power Supply
H23	VDD_USB2_18	P	1.8V Analog Power Supply
AB30	VDDIO_18	P	IO power
AB31	VDDIO_18	P	IO power
AF14	VDDIO_18	P	IO power
AF15	VDDIO_18	P	IO power
AF16	VDDIO_18	P	IO power
AF17	VDDIO_18	P	IO power

Pin ID	Package Pin Name	Type	Description
AF18	VDDIO_18	P	IO power
AF19	VDDIO_18	P	IO power
J15	VDDIO_18	P	IO power
K15	VDDIO_18	P	IO power
V29	VDDIO_18	P	IO power
V30	VDDIO_18	P	IO power
V31	VDDIO_18	P	IO power
V32	VDDIO_18	P	IO power
Y30	VDDIO_18	P	IO power
Y31	VDDIO_18	P	Output driver power, 1.8V
Y32	VDDIO_18	P	IO power
Y33	VDDIO_18	P	IO power

5.1.7.7 3.3V Voltage Supply

Table 5-27 3.3V Voltage Supply Pins

Pin ID	Package Pin Name	Type	Description
P37	VDD_SD_33	P	3.3V SD Supply
P38	VDD_SD_33	P	3.3V SD Supply
F19	VDD_USB2_0_33	P	3.3V Analog Power Supply
G19	VDD_USB2_1_33	P	3.3V Analog Power Supply
H24	VDD_USB2_2_33	P	3.3V Analog Power Supply
H25	VDD_USB2_3_33	P	3.3V Analog Power Supply
K20	VDD_USB3_33	P	3.3V High supply for HS operation & SS operation
K23	VDD_USB3_33	P	3.3V High supply for HS operation & SS operation
L18	VDD_USB3_33	P	3.3V High supply for HS operation & SS operation
M22	VDD_USB3_33	P	3.3V High supply for HS operation & SS operation

5.1.7.8 Ground

Table 5-28 Ground Pins

Pin ID	Package Pin Name	Type	Description
A10	VSS	G	eMMC/SD ground
A12	VSS	G	eMMC/SD ground
A14	VSS	G	DDR 0 ground
A16	VSS	G	DDR 1 ground
A18	VSS	G	HDMI ground

Pin ID	Package Pin Name	Type	Description
A22	VSS	G	Core ground
A26	VSS	G	Core ground
A28	VSS	G	Core ground
A30	VSS	G	Core ground
A8	VSS	G	Core ground
AA12	VSS	G	Core ground
AA14	VSS	G	Core ground
AA15	VSS	G	Core ground
AA16	VSS	G	Core ground
AA17	VSS	G	Core ground
AA18	VSS	G	Core ground
AA19	VSS	G	Core ground
AA20	VSS	G	Core ground
AA21	VSS	G	Core ground
AA22	VSS	G	Core ground
AA23	VSS	G	Core ground
AA24	VSS	G	Core ground
AA25	VSS	G	Core ground
AA26	VSS	G	Core ground
AA27	VSS	G	Core ground
AA3	VSS	G	Core ground
AA32	VSS	G	Core ground
AA33	VSS	G	Core ground
AA34	VSS	G	Core ground
AA37	VSS	G	Core ground
AA4	VSS	G	Core ground
AA5	VSS	G	Core ground
AA6	VSS	G	Core ground
AA7	VSS	G	Core ground
AB32	VSS	G	Core ground
AB33	VSS	G	Core ground
AB36	VSS	G	Core ground
AB39	VSS	G	Core ground
AC1	VSS	G	Core ground

Pin ID	Package Pin Name	Type	Description
AC14	VSS	G	Core ground
AC16	VSS	G	Core ground
AC17	VSS	G	Core ground
AC18	VSS	G	Core ground
AC19	VSS	G	Core ground
AC2	VSS	G	Core ground
AC20	VSS	G	Core ground
AC21	VSS	G	Core ground
AC22	VSS	G	Core ground
AC23	VSS	G	Core ground
AC24	VSS	G	Core ground
AC25	VSS	G	Core ground
AC26	VSS	G	Core ground
AC27	VSS	G	Core ground
AC3	VSS	G	Core ground
AC32	VSS	G	Core ground
AC33	VSS	G	Core ground
AC34	VSS	G	Core ground
AC37	VSS	G	Core ground
AD1	VSS	G	Core ground
AD11	VSS	G	Core ground
AD36	VSS	G	Core ground
AD39	VSS	G	Core ground
AD4	VSS	G	Core ground
AD9	VSS	G	Core ground
AE13	VSS	G	Core ground
AE14	VSS	G	Core ground
AE15	VSS	G	Core ground
AE16	VSS	G	Core ground
AE17	VSS	G	Core ground
AE18	VSS	G	Core ground
AE19	VSS	G	Core ground
AE20	VSS	G	Core ground
AE21	VSS	G	Core ground

Pin ID	Package Pin Name	Type	Description
AE22	VSS	G	Core ground
AE23	VSS	G	Core ground
AE24	VSS	G	Core ground
AE25	VSS	G	Core ground
AE26	VSS	G	Core ground
AE27	VSS	G	Core ground
AE28	VSS	G	Core ground
AE29	VSS	G	Core ground
AE30	VSS	G	Core ground
AE31	VSS	G	Core ground
AE32	VSS	G	Core ground
AE33	VSS	G	Core ground
AE34	VSS	G	Core ground
AE37	VSS	G	Core ground
AE8	VSS	G	Core ground
AF2	VSS	G	Core ground
AF20	VSS	G	Core ground
AF22	VSS	G	Core ground
AF23	VSS	G	Core ground
AF25	VSS	G	Core ground
AF28	VSS	G	Core ground
AF29	VSS	G	Core ground
AF3	VSS	G	Core ground
AF31	VSS	G	Core ground
AF36	VSS	G	Core ground
AF39	VSS	G	Core ground
AG1	VSS	G	Core ground
AG12	VSS	G	Core ground
AG17	VSS	G	Core ground
AG19	VSS	G	Core ground
AG20	VSS	G	Core ground
AG21	VSS	G	Core ground
AG27	VSS	G	Core ground
AG31	VSS	G	Core ground

Pin ID	Package Pin Name	Type	Description
AG32	VSS	G	Core ground
AG33	VSS	G	Core ground
AG35	VSS	G	Core ground
AG37	VSS	G	Core ground
AG38	VSS	G	Core ground
AG39	VSS	G	Core ground
AG4	VSS	G	Core ground
AG5	VSS	G	Core ground
AH10	VSS	G	Core ground
AH15	VSS	G	Core ground
AH16	VSS	G	Core ground
AH21	VSS	G	Core ground
AH24	VSS	G	Core ground
AH25	VSS	G	Core ground
AH32	VSS	G	Core ground
AH6	VSS	G	Core ground
AJ14	VSS	G	Core ground
AJ17	VSS	G	Core ground
AJ2	VSS	G	Core ground
AJ21	VSS	G	Core ground
AJ23	VSS	G	Core ground
AJ26	VSS	G	Core ground
AJ27	VSS	G	Core ground
AJ28	VSS	G	Core ground
AJ3	VSS	G	Core ground
AJ31	VSS	G	Core ground
AJ33	VSS	G	Core ground
AJ39	VSS	G	Core ground
AJ9	VSS	G	Core ground
AK1	VSS	G	Core ground
AK10	VSS	G	Core ground
AK11	VSS	G	Core ground
AK12	VSS	G	Core ground
AK15	VSS	G	Core ground

Pin ID	Package Pin Name	Type	Description
AK16	VSS	G	Core ground
AK20	VSS	G	Core ground
AK23	VSS	G	Core ground
AK32	VSS	G	Core ground
AK33	VSS	G	Core ground
AK36	VSS	G	Core ground
AK4	VSS	G	Core ground
AK5	VSS	G	Core ground
AK7	VSS	G	Core ground
AL13	VSS	G	Core ground
AL14	VSS	G	Core ground
AL16	VSS	G	Core ground
AL17	VSS	G	Core ground
AL21	VSS	G	Core ground
AL24	VSS	G	Core ground
AL26	VSS	G	Core ground
AL28	VSS	G	Core ground
AL30	VSS	G	Core ground
AL7	VSS	G	Core ground
AM11	VSS	G	Core ground
AM14	VSS	G	Core ground
AM2	VSS	G	Core ground
AM29	VSS	G	Core ground
AM3	VSS	G	Core ground
AM33	VSS	G	Core ground
AM39	VSS	G	Core ground
AM5	VSS	G	Core ground
AN1	VSS	G	Core ground
AN12	VSS	G	Core ground
AN15	VSS	G	Core ground
AN16	VSS	G	Core ground
AN18	VSS	G	Core ground
AN23	VSS	G	Core ground
AN25	VSS	G	Core ground

Pin ID	Package Pin Name	Type	Description
AN27	VSS	G	Core ground
AN33	VSS	G	Core ground
AN36	VSS	G	Core ground
AN4	VSS	G	Core ground
AN6	VSS	G	Core ground
AN9	VSS	G	Core ground
AP15	VSS	G	Core ground
AP20	VSS	G	Core ground
AP26	VSS	G	Core ground
AP28	VSS	G	Core ground
AR10	VSS	G	Core ground
AR13	VSS	G	Core ground
AR14	VSS	G	Core ground
AR17	VSS	G	Core ground
AR18	VSS	G	Core ground
AR2	VSS	G	Core ground
AR20	VSS	G	Core ground
AR21	VSS	G	Core ground
AR23	VSS	G	Core ground
AR3	VSS	G	Core ground
AR31	VSS	G	Core ground
AR33	VSS	G	Core ground
AR5	VSS	G	Core ground
AT1	VSS	G	Core ground
AT12	VSS	G	Core ground
AT15	VSS	G	Core ground
AT20	VSS	G	Core ground
AT23	VSS	G	Core ground
AT25	VSS	G	Core ground
AT27	VSS	G	Core ground
AT28	VSS	G	Core ground
AT33	VSS	G	Core ground
AT35	VSS	G	Core ground
AT37	VSS	G	Core ground

Pin ID	Package Pin Name	Type	Description
AT39	VSS	G	Core ground
AT4	VSS	G	Core ground
AT7	VSS	G	Core ground
AT9	VSS	G	Core ground
AU11	VSS	G	Core ground
AU14	VSS	G	Core ground
AU17	VSS	G	Core ground
AU18	VSS	G	Core ground
AU20	VSS	G	Core ground
AU22	VSS	G	Core ground
AU3	VSS	G	Core ground
AU6	VSS	G	Core ground
AU7	VSS	G	Core ground
AV1	VSS	G	Core ground
AV12	VSS	G	Core ground
AV15	VSS	G	Core ground
AV16	VSS	G	Core ground
AV19	VSS	G	Core ground
AV20	VSS	G	Core ground
AV31	VSS	G	Core ground
AV4	VSS	G	Core ground
AV9	VSS	G	Core ground
AW11	VSS	G	Core ground
AW14	VSS	G	Core ground
AW17	VSS	G	Core ground
AW20	VSS	G	Core ground
AW26	VSS	G	Core ground
AW29	VSS	G	Core ground
AW3	VSS	G	Core ground
AW35	VSS	G	Core ground
AW38	VSS	G	Core ground
AW6	VSS	G	Core ground
AW8	VSS	G	Core ground
B34	VSS	G	Core ground

Pin ID	Package Pin Name	Type	Description
B38	VSS	G	Core ground
C11	VSS	G	Core ground
C13	VSS	G	Core ground
C15	VSS	G	Core ground
C17	VSS	G	Core ground
C19	VSS	G	Core ground
C23	VSS	G	Core ground
C25	VSS	G	Core ground
C27	VSS	G	Core ground
C29	VSS	G	Core ground
C31	VSS	G	Core ground
C36	VSS	G	Core ground
C9	VSS	G	Core ground
D12	VSS	G	Core ground
D14	VSS	G	Core ground
D16	VSS	G	Core ground
D18	VSS	G	Core ground
D22	VSS	G	Core ground
D27	VSS	G	Core ground
D28	VSS	G	Core ground
D30	VSS	G	Core ground
D38	VSS	G	Core ground
D8	VSS	G	Core ground
E20	VSS	G	Core ground
E21	VSS	G	Core ground
E24	VSS	G	Core ground
E29	VSS	G	Core ground
E32	VSS	G	Core ground
E36	VSS	G	Core ground
F15	VSS	G	Core ground
F17	VSS	G	Core ground
F23	VSS	G	Core ground
F26	VSS	G	Core ground
F31	VSS	G	Core ground

Pin ID	Package Pin Name	Type	Description
F34	VSS	G	Core ground
F38	VSS	G	Core ground
F4	VSS	G	Core ground
F5	VSS	G	Core ground
F6	VSS	G	Core ground
F7	VSS	G	Core ground
F8	VSS	G	Core ground
G14	VSS	G	Core ground
G16	VSS	G	Core ground
G18	VSS	G	Core ground
G22	VSS	G	Core ground
G3	VSS	G	Core ground
G30	VSS	G	Core ground
G34	VSS	G	Core ground
H21	VSS	G	Core ground
H27	VSS	G	Core ground
H31	VSS	G	Core ground
H4	VSS	G	Core ground
H7	VSS	G	Core ground
H8	VSS	G	Core ground
J1	VSS	G	Core ground
J2	VSS	G	Core ground
J25	VSS	G	Core ground
J28	VSS	G	Core ground
J29	VSS	G	Core ground
J30	VSS	G	Core ground
J31	VSS	G	Core ground
J32	VSS	G	Core ground
K29	VSS	G	Core ground
K33	VSS	G	Core ground
K37	VSS	G	Core ground
K4	VSS	G	Core ground
K5	VSS	G	Core ground
K6	VSS	G	Core ground

Pin ID	Package Pin Name	Type	Description
L20	VSS	G	Core ground
L21	VSS	G	Core ground
L22	VSS	G	Core ground
L25	VSS	G	Core ground
L26	VSS	G	Core ground
L27	VSS	G	Core ground
L28	VSS	G	Core ground
L29	VSS	G	Core ground
L3	VSS	G	Core ground
L35	VSS	G	Core ground
L39	VSS	G	Core ground
M10	VSS	G	Core ground
M14	VSS	G	Core ground
M15	VSS	G	Core ground
M18	VSS	G	Core ground
M24	VSS	G	Core ground
M36	VSS	G	Core ground
M4	VSS	G	Core ground
M7	VSS	G	Core ground
N1	VSS	G	Core ground
N11	VSS	G	Core ground
N2	VSS	G	Core ground
N28	VSS	G	Core ground
N35	VSS	G	Core ground
N9	VSS	G	Core ground
P12	VSS	G	Core ground
P25	VSS	G	Core ground
P26	VSS	G	Core ground
P27	VSS	G	Core ground
P28	VSS	G	Core ground
P29	VSS	G	Core ground
P30	VSS	G	Core ground
P35	VSS	G	Core ground
P39	VSS	G	Core ground

Pin ID	Package Pin Name	Type	Description
P4	VSS	G	Core ground
P5	VSS	G	Core ground
P7	VSS	G	Core ground
R10	VSS	G	Core ground
R13	VSS	G	Core ground
R17	VSS	G	Core ground
R23	VSS	G	Core ground
R24	VSS	G	Core ground
R25	VSS	G	Core ground
R26	VSS	G	Core ground
R27	VSS	G	Core ground
R37	VSS	G	Core ground
R4	VSS	G	Core ground
T11	VSS	G	Core ground
T31	VSS	G	Core ground
T36	VSS	G	Core ground
T39	VSS	G	Core ground
T8	VSS	G	Core ground
U14	VSS	G	Core ground
U15	VSS	G	Core ground
U16	VSS	G	Core ground
U17	VSS	G	Core ground
U18	VSS	G	Core ground
U19	VSS	G	Core ground
U20	VSS	G	Core ground
U21	VSS	G	Core ground
U22	VSS	G	Core ground
U23	VSS	G	Core ground
U24	VSS	G	Core ground
U25	VSS	G	Core ground
U26	VSS	G	Core ground
U27	VSS	G	Core ground
U3	VSS	G	Core ground
U32	VSS	G	Core ground

Pin ID	Package Pin Name	Type	Description
U33	VSS	G	Core ground
U34	VSS	G	Core ground
U37	VSS	G	Core ground
U4	VSS	G	Core ground
U6	VSS	G	Core ground
V36	VSS	G	PCIe x4 0 ground
V39	VSS	G	PCIe x4 0 ground
W1	VSS	G	PCIe x4 0 ground
W11	VSS	G	PCIe x4 1 ground
W13	VSS	G	PCIe x4 1 ground
W14	VSS	G	PCIe x4 1 ground
W15	VSS	G	PCIe x8 ground
W16	VSS	G	PCIe x8 ground
W17	VSS	G	PCIe x8 ground
W18	VSS	G	PCIe x8 ground
W19	VSS	G	PCIe x8 ground
W2	VSS	G	PCIe x8 ground
W20	VSS	G	SATA (PHY) ground
W21	VSS	G	USB 2 0 ground
W22	VSS	G	USB 2 0 ground
W23	VSS	G	USB 2 1 ground
W24	VSS	G	USB 2 2 ground
W25	VSS	G	USB 2 3 ground
W26	VSS	G	USB 3 0 PHY ground
W27	VSS	G	USB 3 1 PHY ground
W3	VSS	G	USB 3 0 PHY ground
W33	VSS	G	USB 3 1 PHY ground
W34	VSS	G	XGbE 0 ground
W37	VSS	G	XGbE 0 ground
W7	VSS	G	XGbE 0 ground
Y36	VSS	G	XGbE 1 ground
Y39	VSS	G	XGbE 1 ground
Y9	VSS	G	XGbE 1 ground
M28	VSS_PVT	G	PVT sensor ground

Pin ID	Package Pin Name	Type	Description
A4	VSSIO	G	IO ground
AA28	VSSIO	G	IO ground
AA29	VSSIO	G	IO ground
AA30	VSSIO	G	IO ground
AA31	VSSIO	G	IO ground
AC15	VSSIO	G	IO ground
AC28	VSSIO	G	IO ground
AC29	VSSIO	G	IO ground
AC30	VSSIO	G	IO ground
AC31	VSSIO	G	IO ground
AD10	VSSIO	G	IO ground
AD12	VSSIO	G	IO ground
AE7	VSSIO	G	IO ground
AF8	VSSIO	G	IO ground
AG9	VSSIO	G	IO ground
B4	VSSIO	G	IO ground
D1	VSSIO	G	IO ground
D3	VSSIO	G	IO ground
H35	VSSIO	G	IO ground
J33	VSSIO	G	IO ground
J37	VSSIO	G	IO ground
L30	VSSIO	G	IO ground
M32	VSSIO	G	IO ground
N29	VSSIO	G	IO ground
P15	VSSIO	G	IO ground
P31	VSSIO	G	IO ground
R18	VSSIO	G	IO ground
R19	VSSIO	G	IO ground
R20	VSSIO	G	IO ground
R21	VSSIO	G	IO ground
R32	VSSIO	G	IO ground
U28	VSSIO	G	IO ground
U29	VSSIO	G	IO ground
U30	VSSIO	G	IO ground

Pin ID	Package Pin Name	Type	Description
U31	VSSIO	G	IO ground
W28	VSSIO	G	IO ground
W29	VSSIO	G	IO ground
W30	VSSIO	G	IO ground
P17	VSSPLL_0	G	PLL ground
W32	VSSPLL_1	G	PLL ground
AF33	VSSPLL_2	G	PLL ground
AP18	VSSPLL_3	G	PLL ground
K14	VSSPLL_HDMI	G	HDMI PLL ground

5.1.8 Requirements for Unused Pins

The following table shows the requirements for unused pins of the BE-M1000. Please follow these requirements if you are not going to use any interface from **Pinout List**.

Table 5-29 Requirements for Unused Pins

Type	Requirements
Input pins	Tie to ground potential If active low level, tie to power supply
Output pins	Leave floating
Power pins	Always use
Reserved pins	Leave floating

5.2 Package Ball Map

The diagrams below show pinout from the top view of the package.

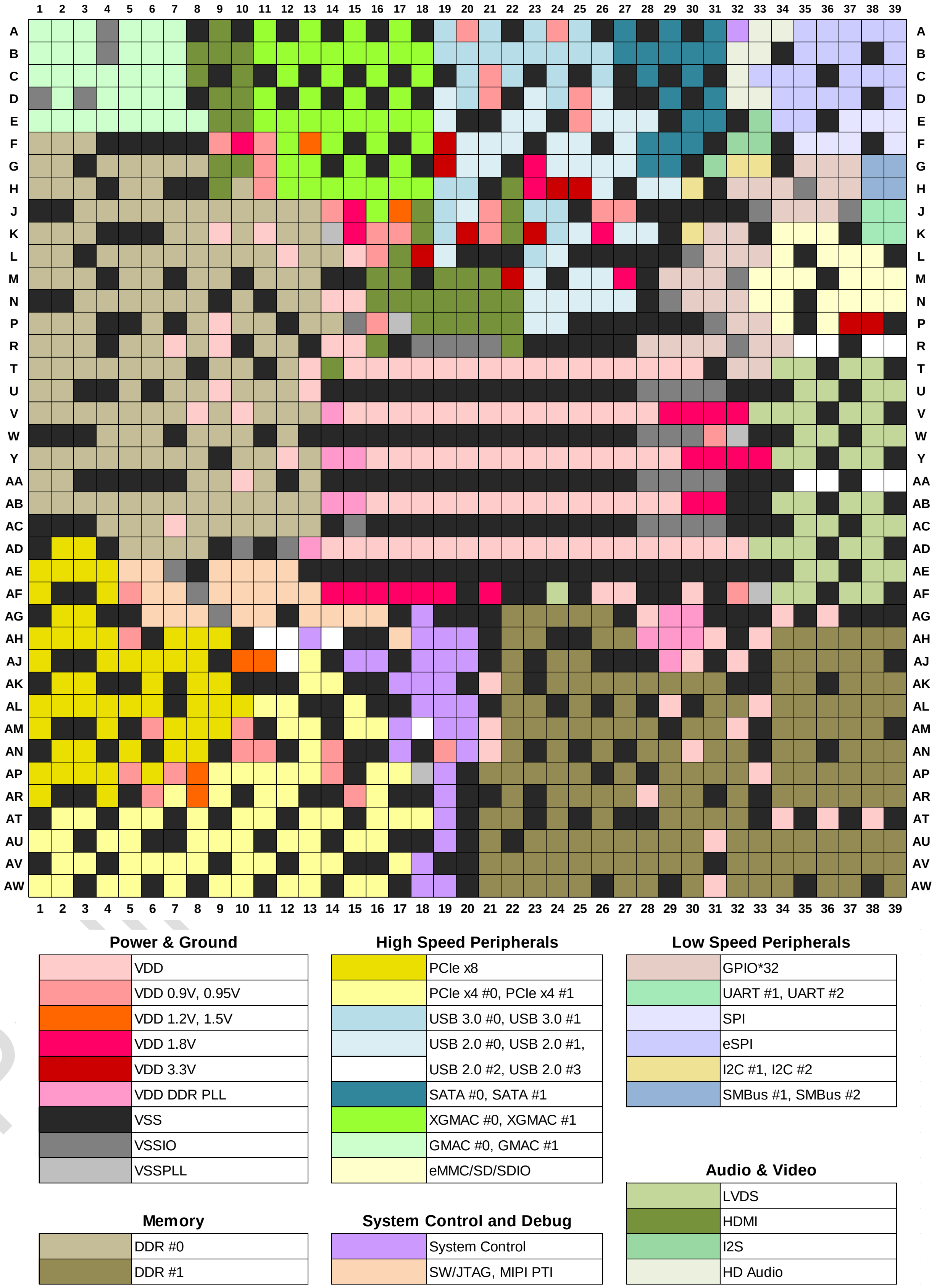


Figure 5-1 BE-M1000 Ball Map

5.2.1 *Power and Ground*

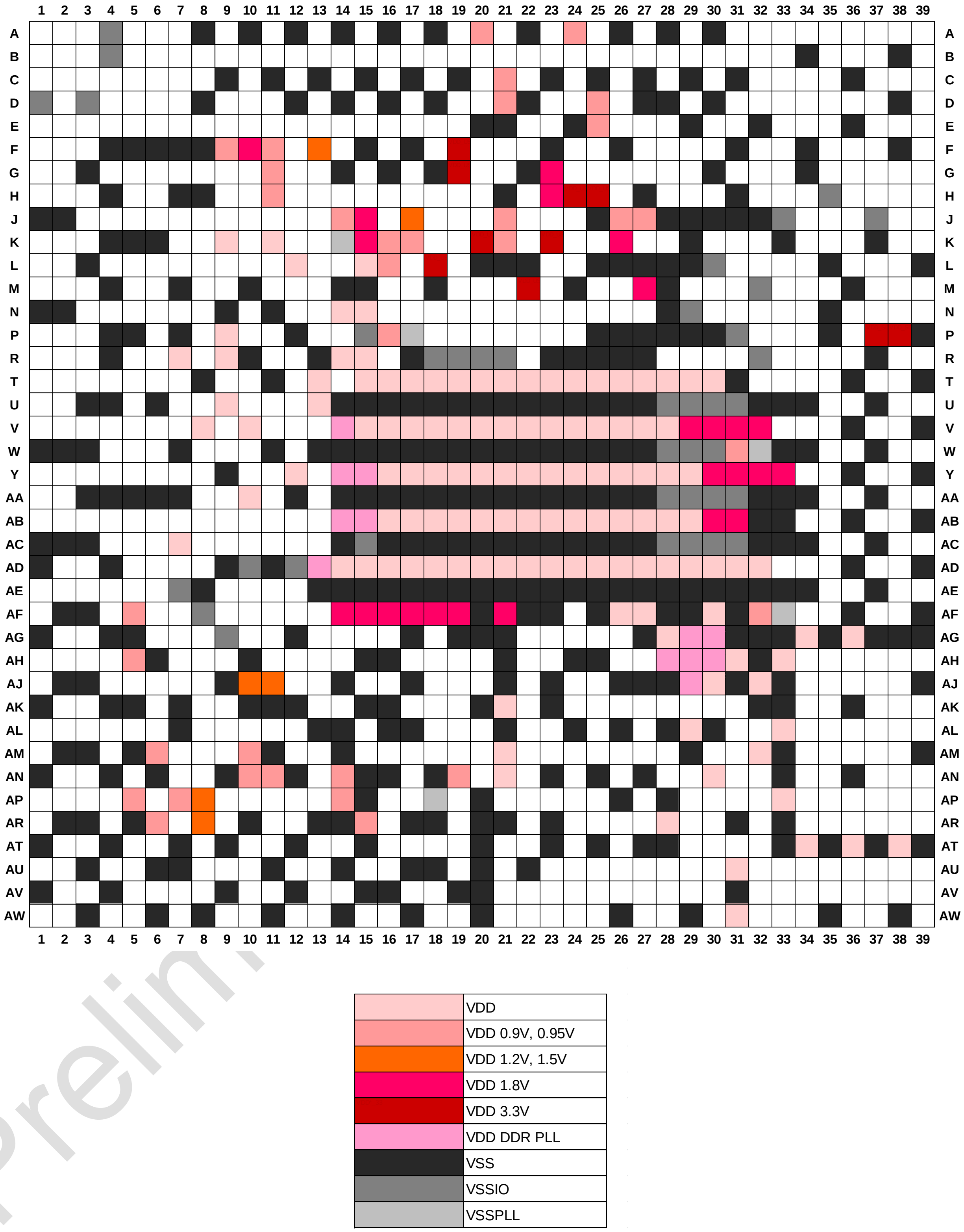


Figure 5-2 Power and Ground Pin Placement

5.2.2 High Speed Peripherals

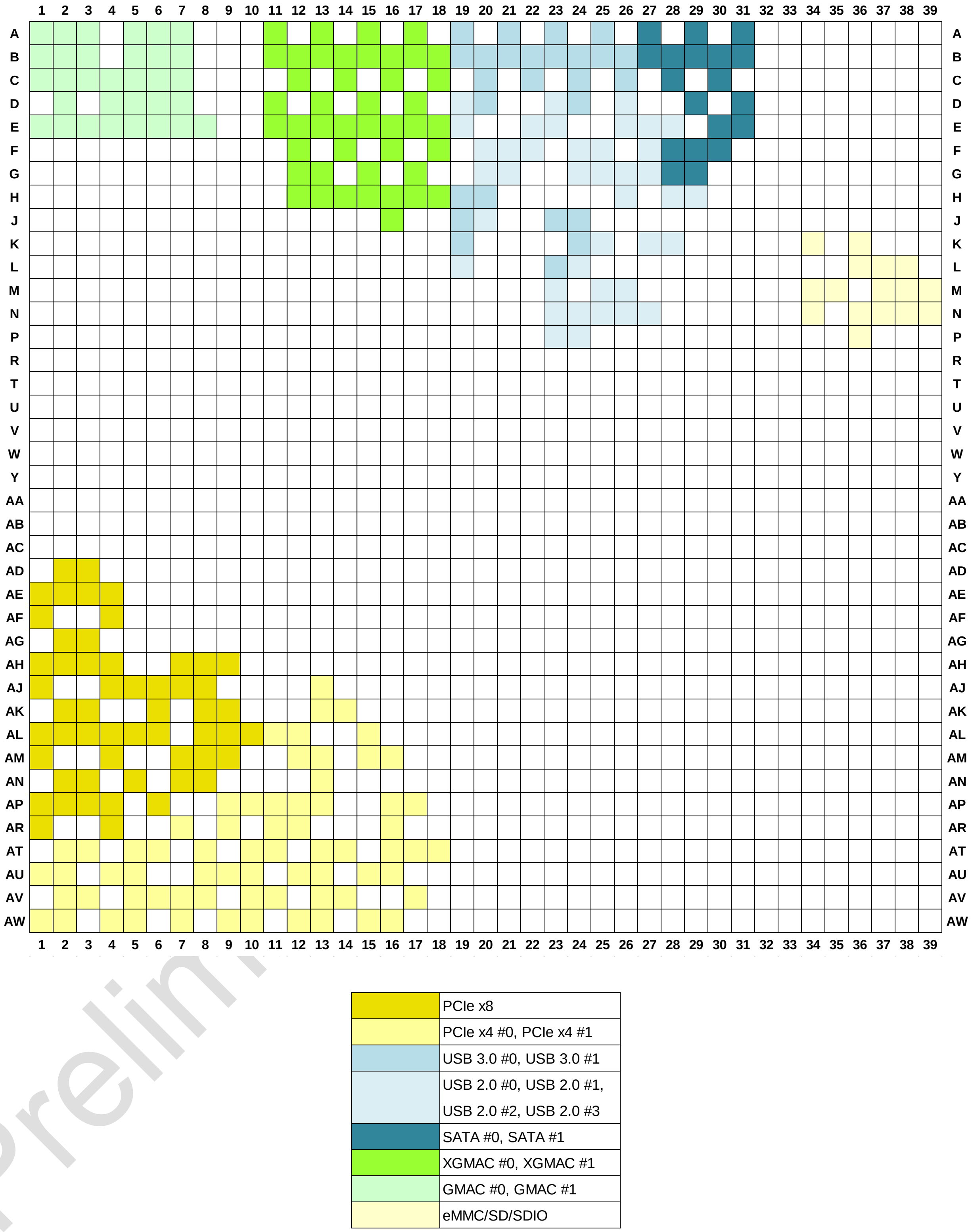
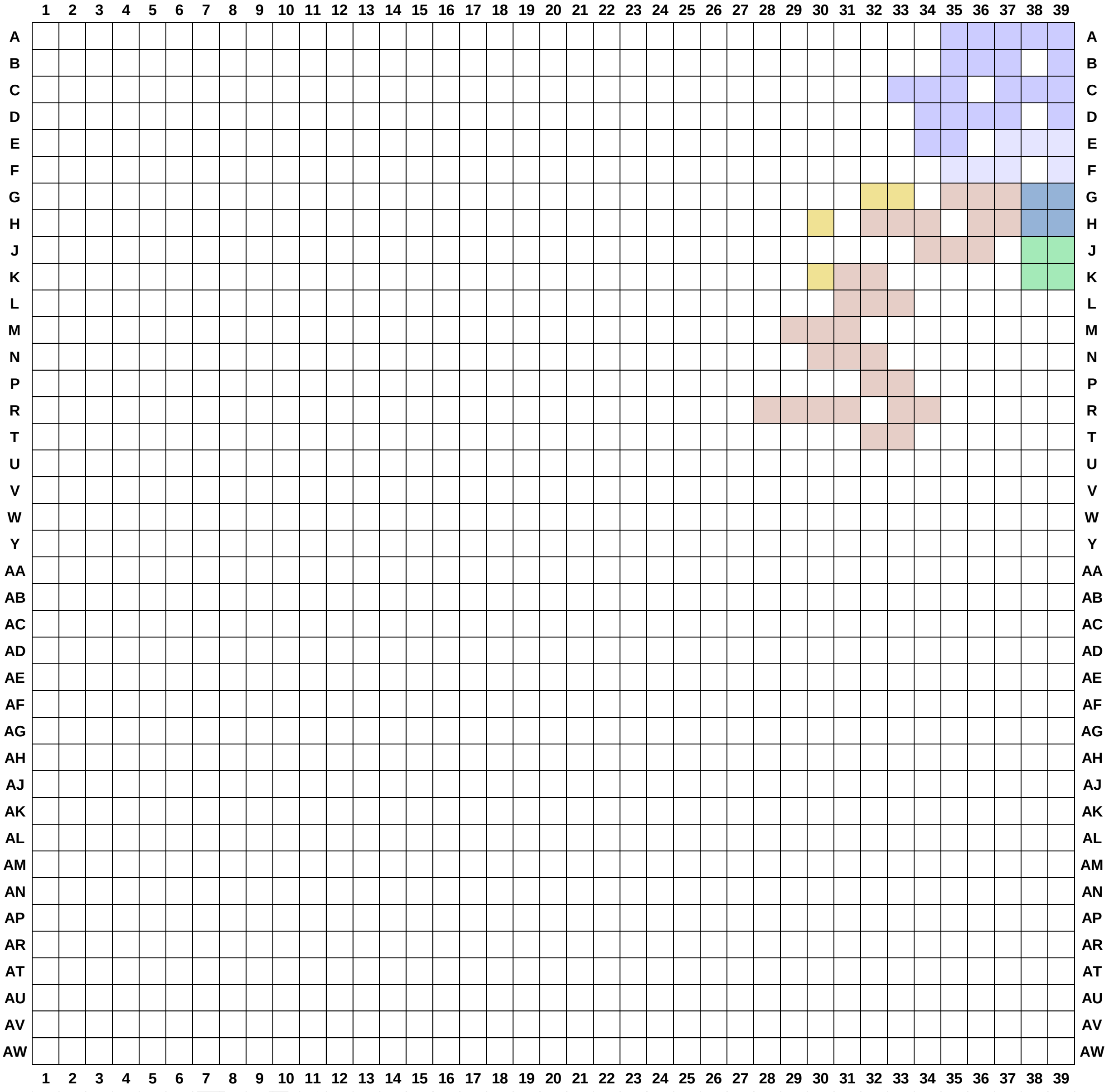


Figure 5-3 High Speed Peripherals Pin Placement

5.2.3 Low Speed Peripherals



🟫	GPIO*32
🟩	UART #1, UART #2
⬜	SPI
🟪	eSPI
🟨	I2C #1, I2C #2
🟦	SMBus #1, SMBus #2

Figure 5-4 Low Speed Peripherals Pin Placement

5.2.4 *Memory*

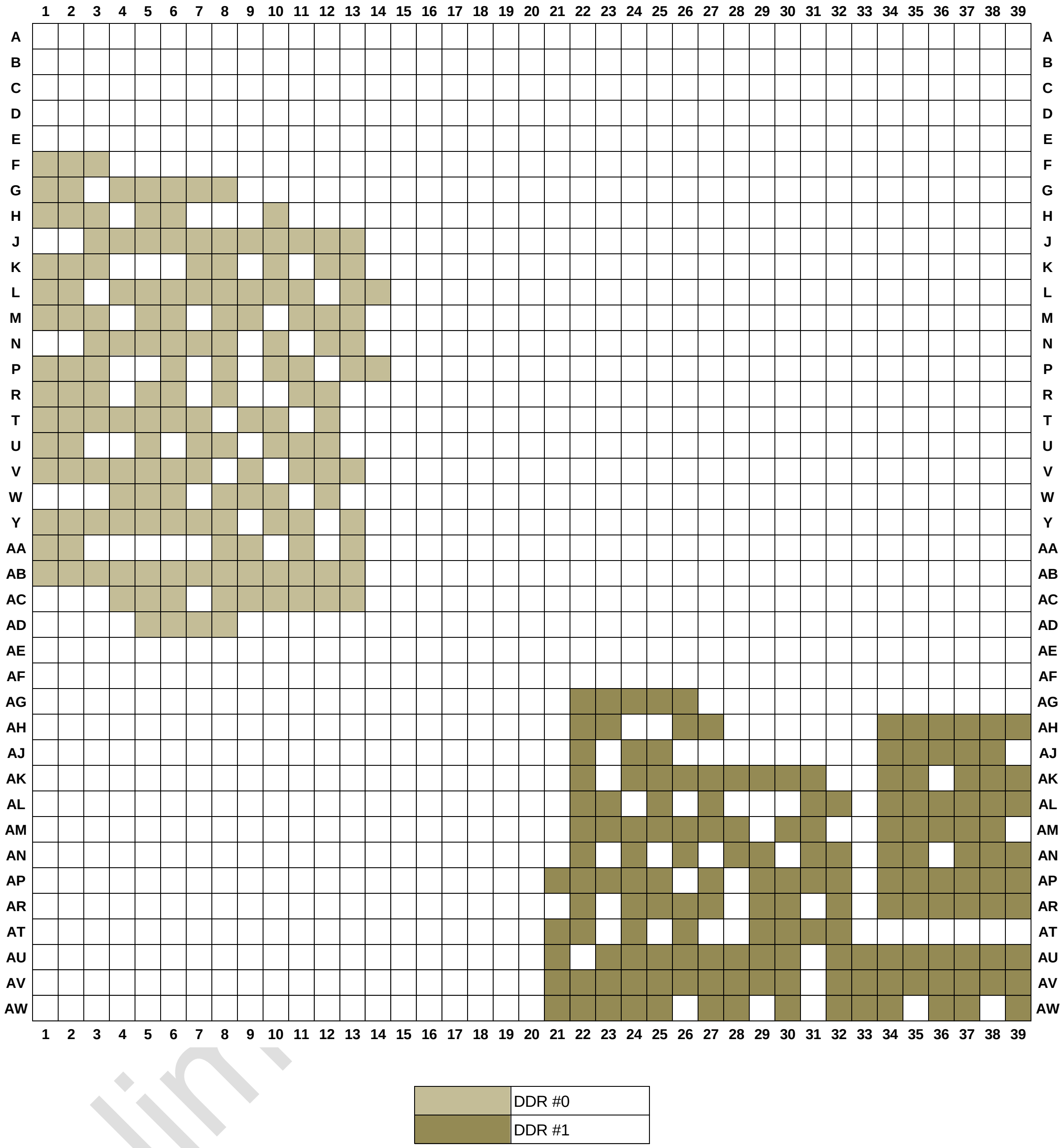
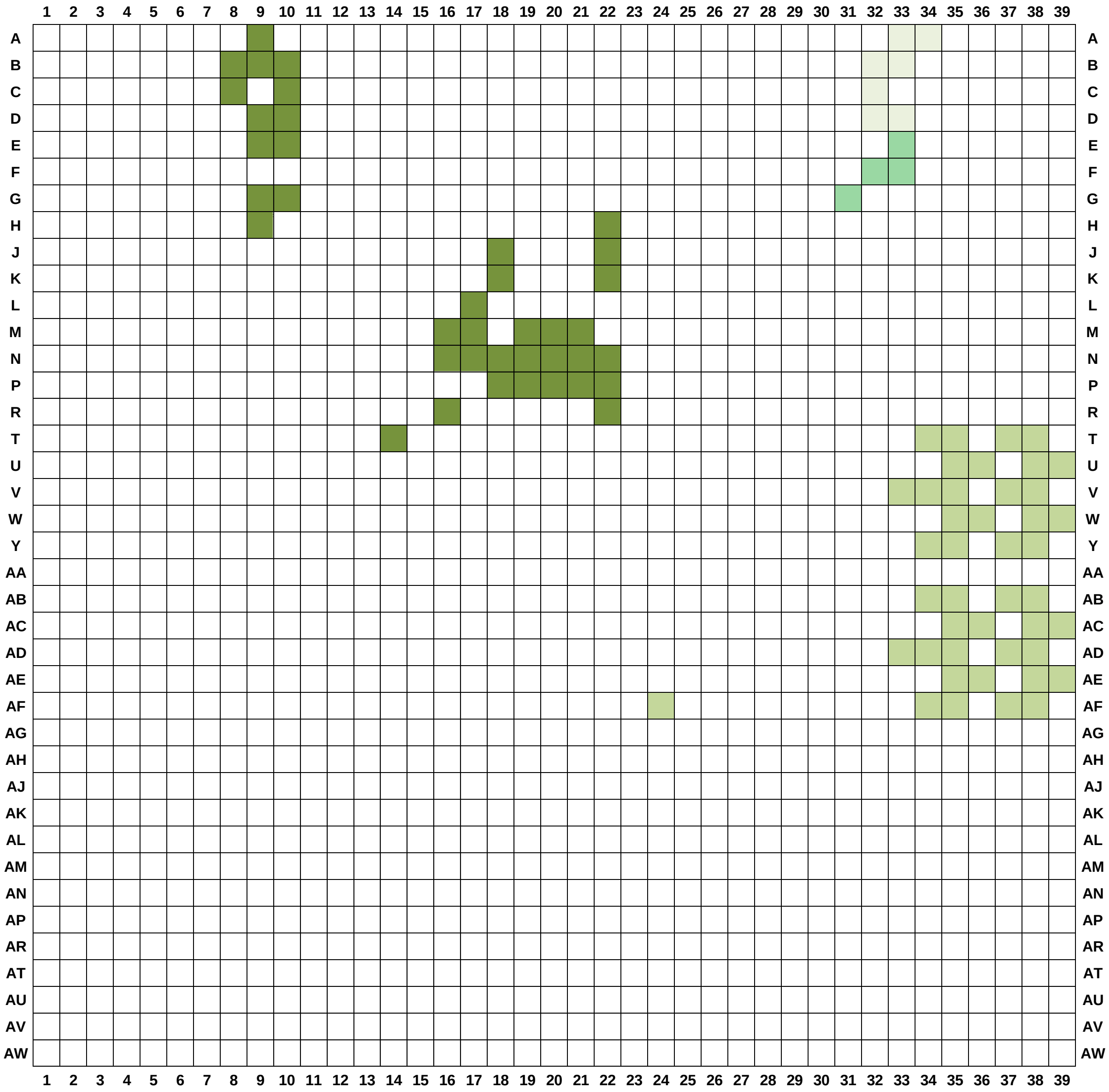


Figure 5-5 Memory Pin Placement

5.2.5 Audio and Video



🟩	LVDS
🟩	HDMI
🟩	I2S
⬜	HD Audio

Figure 5-6 Audio and Video Pin Placement

5.2.6 System Control and Debug

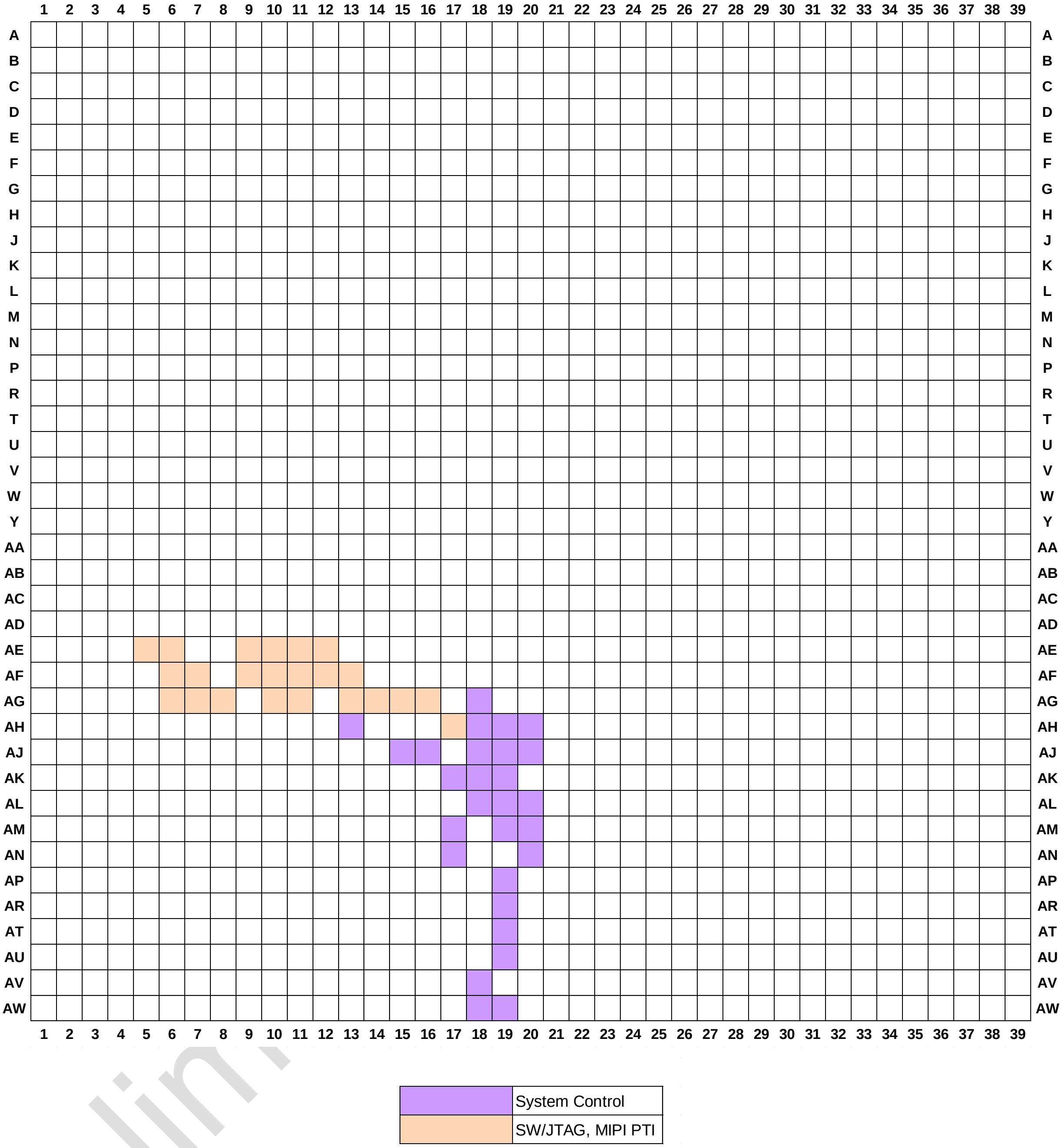


Figure 5-7 System Control and Debug Pin Placement

6 Package Information

6.1 Marking

The following table shows designation of each field in the package marking of BE-M1000.

Table 6-1 BE-M1000 Package Marking

XX	.	YY	WW
Package Type	Field Delimiter	Year	Week

The following table describes the options of package marking.

Table 6-2 BE-M1000 Package Marking Options

Marking	Package Type
BA.YYWW	BA Package
BN.YYWW	BN Package
BK.YYWW	BK Package

6.1.1 BA Package

The following figure shows the top view of the BE-M1000 microprocessor in the BA package.

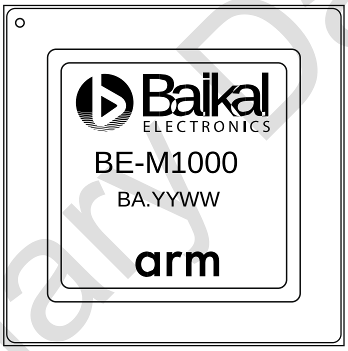


Figure 6-1 BE-M1000 in the BA Package. Top View

6.1.2 BN Package

The following figure shows the top view of the BE-M1000 microprocessor in the BN package.

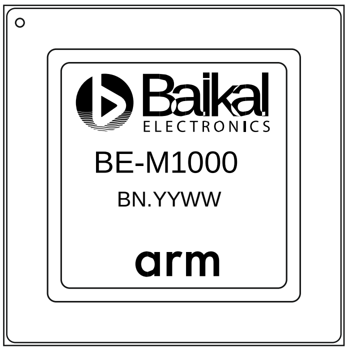


Figure 6-2 BE-M1000 in the BN Package. Top View

6.1.3 BK Package

The following figure shows the top view of the BE-M1000 microprocessor in the BK package.

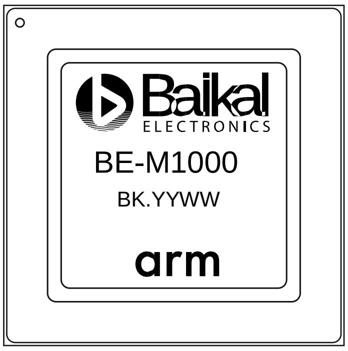


Figure 6-3 BE-M1000 in the BK Package. Top View

6.2 FCBGA-1521 Package

The SoC is mounted into FCBGA-1521 package. Main package parameters are shown it the figures and table below.

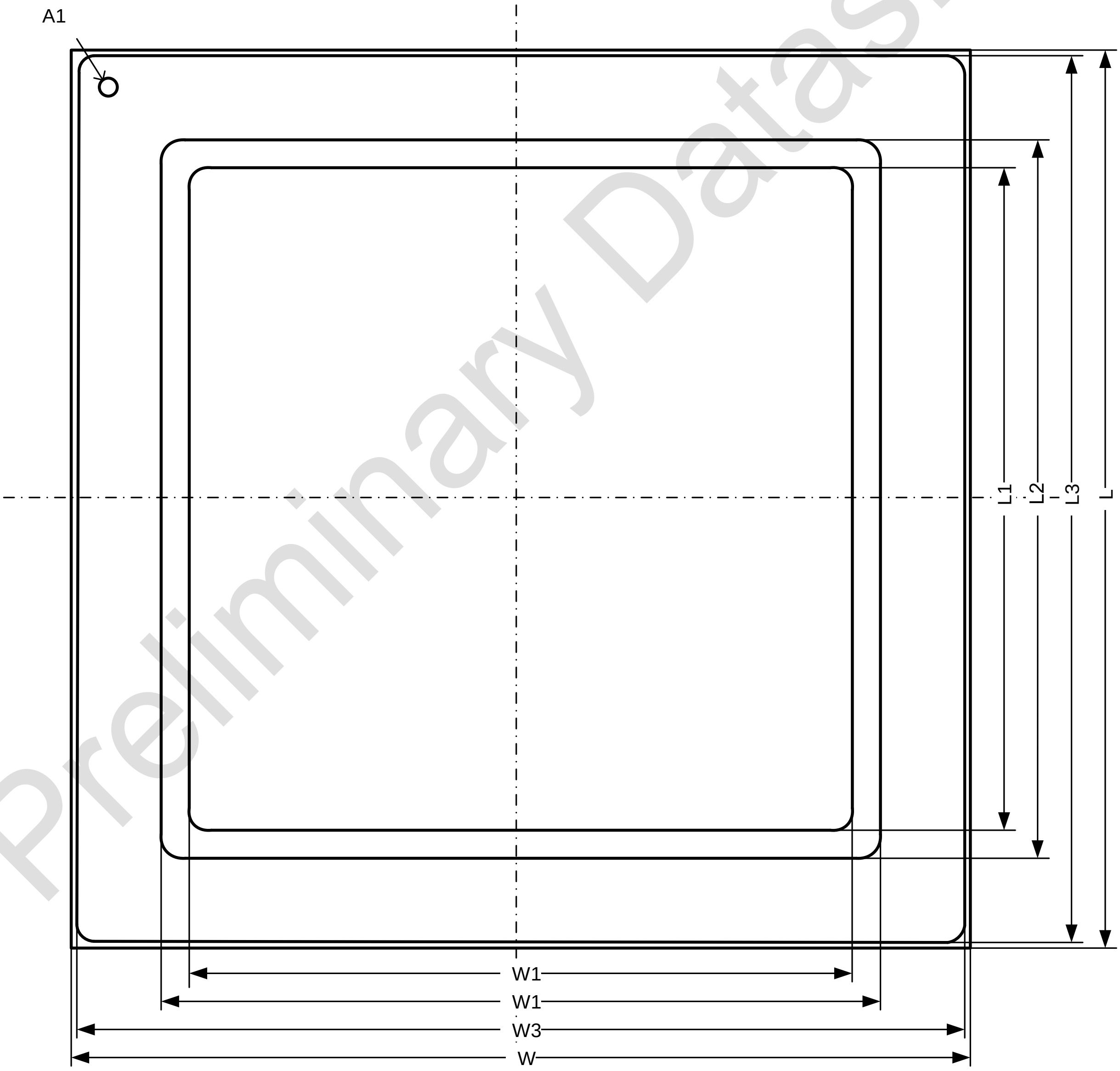


Figure 6-4 SoC Package. Top View

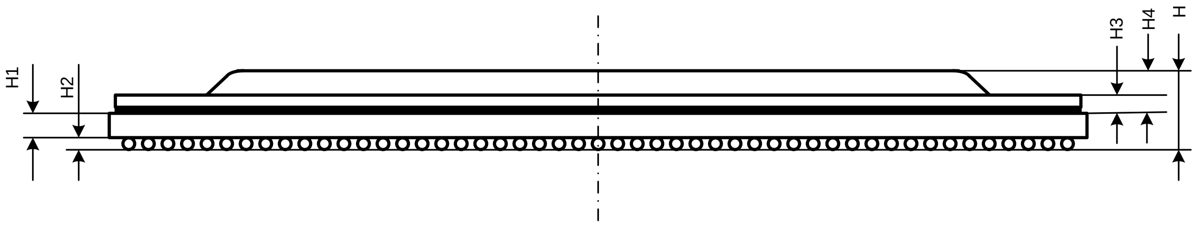


Figure 6-5 SoC Package. Side View

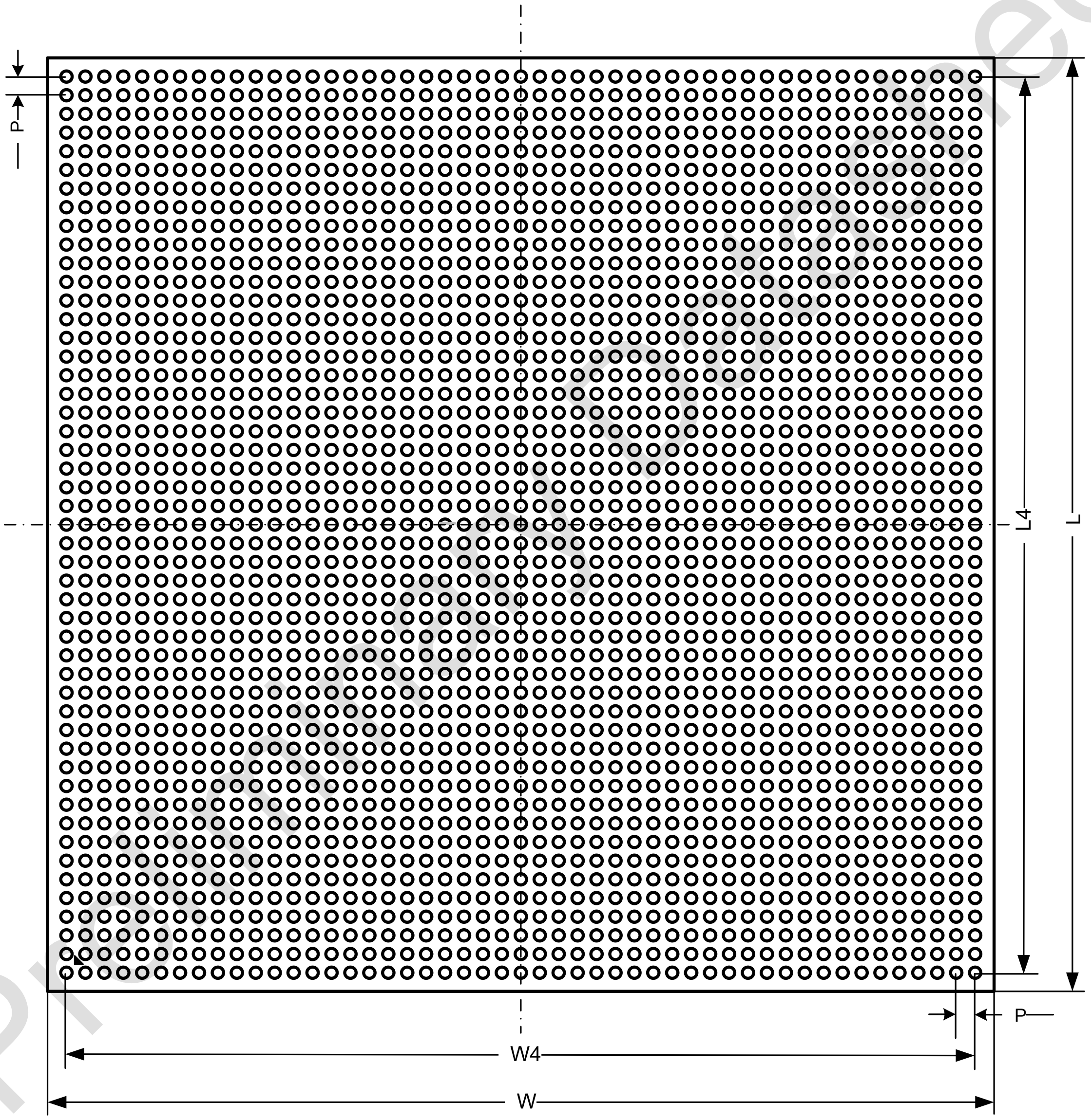


Figure 6-6 SoC Package. Bottom View

The following table shows the package parameters.

Table 6-3 Package Parameters

Symbol	Value, mm	Description
L	40,00	Package length
L1	28,40	Upper cover part length
L2	31,60	Bottom cover part length
L3	39,60	Cover length
L4	38,00	Edge ball center to center
W	40,00	Package width
W1	28,40	Upper cover part width
W2	31,60	Bottom cover part width
W3	39,60	Cover width
W4	38,00	Edge ball center to center
H	2,676…3,176	Package thickness including balls
H1	1,026	Substrate thickness
H2	0,40	Ball height
H3	0,50	Heat sink cover thickness
H4	1,30	Heat sink cover height
D	0,60	Ball diameter
P	1,00	Ball pitch

6.3 Soldering

SoC mounting to PCB should be accomplished in accordance to the soldering profile recommended for Pb-Free packages. Corresponding modes and temperatures are described in the following table and figure.

Table 6-4 Temperature Profile for SoC Soldering to PCB

Profile Feature	Description	Temperature	Duration
A	Preheat stage	150…200°C	60…120 seconds
B	Melting stage	>217°C	60…150 seconds
C	Ramp-up rate	3°C/sec max.	
D	Peak temperature	245°C	
E	Soldering stage	>240°C	30 seconds min.
F	Time from room temperature to peak temperature		< 8 minutes max.
G	Ramp-down rate	6°C/sec max.	

All temperatures refer to topside of the package, measured on the package body surface.

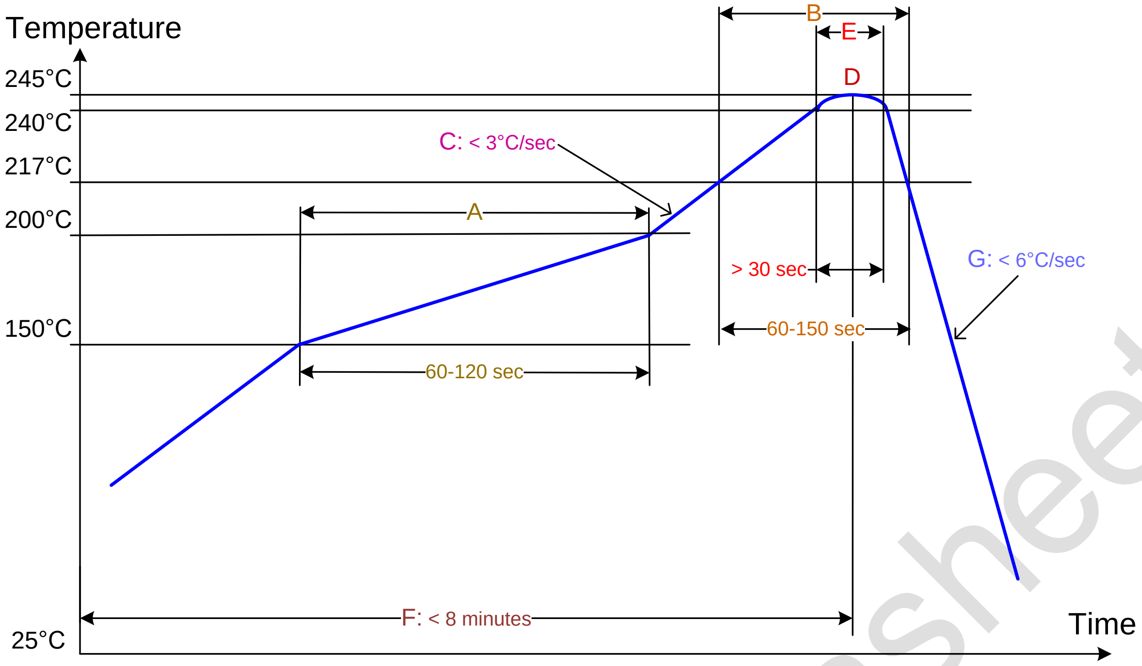


Figure 6-7 Soldering Profile

7 Ordering Information

BE-M1000 is orderable part number. Designation of each field in the part number is shown in a table below.

Table 7-1 Ordering information

BE	-	M	1	0	0	0
Baikal Electronics	Field Delimiter	Product Line	Generation	Modification	Reserved Field	Reserved Field

BE-M1000 is the first product in BE-M product line.

To order BE-M1000 please contact Baikal Electronics company referred in the next page.

Contact Info

Baikal Electronics: https://www.baikalelectronics.com/

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Revision History

Revision	Date	Substantive change(s)
0.65	02.07.2019	Initial version
0.70	01.11.2019	The chapter **4 Power-Up/Down**: • Correction of power-up order • The information about power-up sequence
0.72	11.12.2019	The chapter **4 Power-Up/Down**: • The information about power-down
0.73	16.12.2019	The section **5.1 Pinout List**: • The following pins changed pin IDs: DDR0_DQ[18], DDR0_DQ[19], DDR0_DQ[20], DDR0_DQ[21], DDR0_DQ[26], DDR0_DQ[27], DDR0_DQ[28], DDR0_DQ[29], DDR0_DQ[41], DDR0_DQ[44], DDR0_DQ[48], DDR0_DQ[51], DDR0_DQ[52], DDR0_DQ[53], DDR0_DQ[56], DDR0_DQ[63]
0.74	04.03.2020	The section **2.4 System Control Module**: • The information about unaccessability of boot controller's dedicated interfaces for Cortex-A57 cores
0.82	25.05.2020	The section **4.1 Power-Up Sequence**: • New steps between DDR supply and 1.8V voltage supply
0.83	13.07.2020	The operating frequency value of Arm Mali T-628 GPU shader cores changed from **500 MHz** to **700 MHz**
0.84	22.10.2020	**Mali T-628 GPU**: the operating frequency value shader cores changed from **700 MHz** to **750 MHz** **4K Video Decoder** has been renamed to **HD Video Decoder** due to limited support for 4K@30fps video formats **LVDS:** maximum display resolution changed to **up to 2560x1440** **HDMI:** maximum display resolution changed to **up to 3840x2160** **Table 3–1 BE-M1000 Power Domains**: • PLL supply value changed from **0.9 ± 10 %** to **0.95 ± 5 %** V • Max power value of 0.95V voltage supply changed from **23W** to **24W** • Max power value of PLL supply changed from **0.17W** to **0.20W** • Max power value of 1.5V voltage supply changed from **1.0W** to **2.0W** • Max power value of 1.8V voltage supply changed from **0.6W** to **1.8W** • In accordance to changes of max power values for differential erent supply types, total max power value of microprocessor changed from **~28.47W** to **~34.7W** The section **5.1 Pinout List**: • A11, B11, D11 and E11 pins are complemented with information

Revision	Date	Substantive change(s)
		about their use for 10GBASE-KR - The section is complemented with section ***5.1.1 Requirements for Unused Pins***
0.85	11.11.2020	AA38, AA39, R38, R39, AA35, AA36, R35 R36 pins moved to N/C group and marked as Reserved because LVDS_*[4] pins are not used
0.88	04.06.2021	Display resolution of ***VDU with HDMI 2.0*** changed from **3840x2160** to **2560x1440**
0.89	15.06.2021	The chapter **3 Electrical Specifications** is updated
0.91	28.06.2021	The section **1.1 Main Features** is updated
0.92	14.07.2021	**Package Pin Name** and **Description** of AL18 pin is changed in the section **5.1.5 System Control**
0.93	13.08.2021	The section **5.1 Pinout List** is supplemented with **Voltage range** in pin descriptions
0.94	11.10.2021	The document is supplemented with the following sections: - **2.7.5 HD Audio** - **6.1 Marking** The section **5.1 Pinout List**: - New section ***5.1.4.3 HDA*** - **Pin Description** column is supplemented with information about reserved pins for BN and BK packages
0.95	15.10.2021	Minor edits