

BE-M1000 Microprocessor Preliminary Datasheet

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1 Introduction

The BE-M1000 is a general purpose *System-on-a-Chip (SoC)* for computing systems, such as personal computers, microservers, networking equipment, multimedia and software-defined hardware, embedded systems and controllers that require high performance and low power consumption.

The SoC features eight Arm[®] Cortex[™]-A57 cores that operate at 1.5 GHz and support the coherent caches L1, L2, and L3.

The video subsystem includes two video controllers (LVDS and HDMI), and HD video decoder. Arm Mali[™]-T628 graphics coprocessor contains eight shader cores.

The SoC contains two DDR3/4 memory controllers and a wide range of peripheral interfaces: PCIe Gen3, 10 Gb Ethernet, 1 Gb Ethernet, USB 3.0, USB 2.0, SATA 6G, eMMC/SD, I²S, SPI, UART, I²C, GPIO, etc.

The SoC complies with Arm TrustZone[®] technology and contains the capabilities necessary to build trusted systems.

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1.1 Main Features

Table 1-1 Main Features

Feature	Description
Armv8-A Architecture	8 Arm Cortex-A57 cores operating up to 1.5 GHz
	4 core clusters (2 cores and 1 MB L2 cache in a cluster)
Graphics Processing Unit	Arm Mali-T628 <i>graphics processing unit (GPU)</i> with 8 shader cores (two quad-core clusters) operating at 750 MHz
	128 KB L2 cache in a cluster
L3 Cache	<i>Cache Coherent Network (CCN)</i> with 8 MB L3 cache memory
External Memory Interface	Two 64-bit <i>Dynamic Random Access Memory (DRAM)</i> interfaces with support of DDR4-2400/DDR3-1600 and <i>error correction code (ECC)</i>
High Speed Peripheral Interfaces	Three PCIe Gen3 interfaces: one PCIe x8 and two PCIe x4
	Two USB 3.0/2.0 ports and four USB 2.0 ports
	Two SATA 6G subsystems
	Two 10 Gb Ethernet interfaces (10GBASE-KX4/10GBASE-KR)
	Two 1 Gb Ethernet RGMII
	eMMC/SD/SDIO
Low Speed Peripheral Interfaces	Four peripheral timers
	GPIO*32
	Two UARTs
	SPI
	eSPI
	Two I ² Cs
	Two SMBus interfaces
Multimedia	Video Controller with LVDS interface
	Video Controller with HDMI 2.0
	HD Video Decoder
	HD Audio Controller
	I ² S interface
Security	Arm TrustZone architecture
	Two TrustZone controllers
	Secure boot
System Monitoring and Debug	Five PVT controllers
	Arm CoreSight™ debug and trace architecture
Package	FCBGA-1521 40x40 mm, 1 mm pitch, 1521 pins
Power Consumption	35W max
Operating Temperature	From 0 to +70°C
Technology	CMOS 28 nm

1.2 Block Diagram

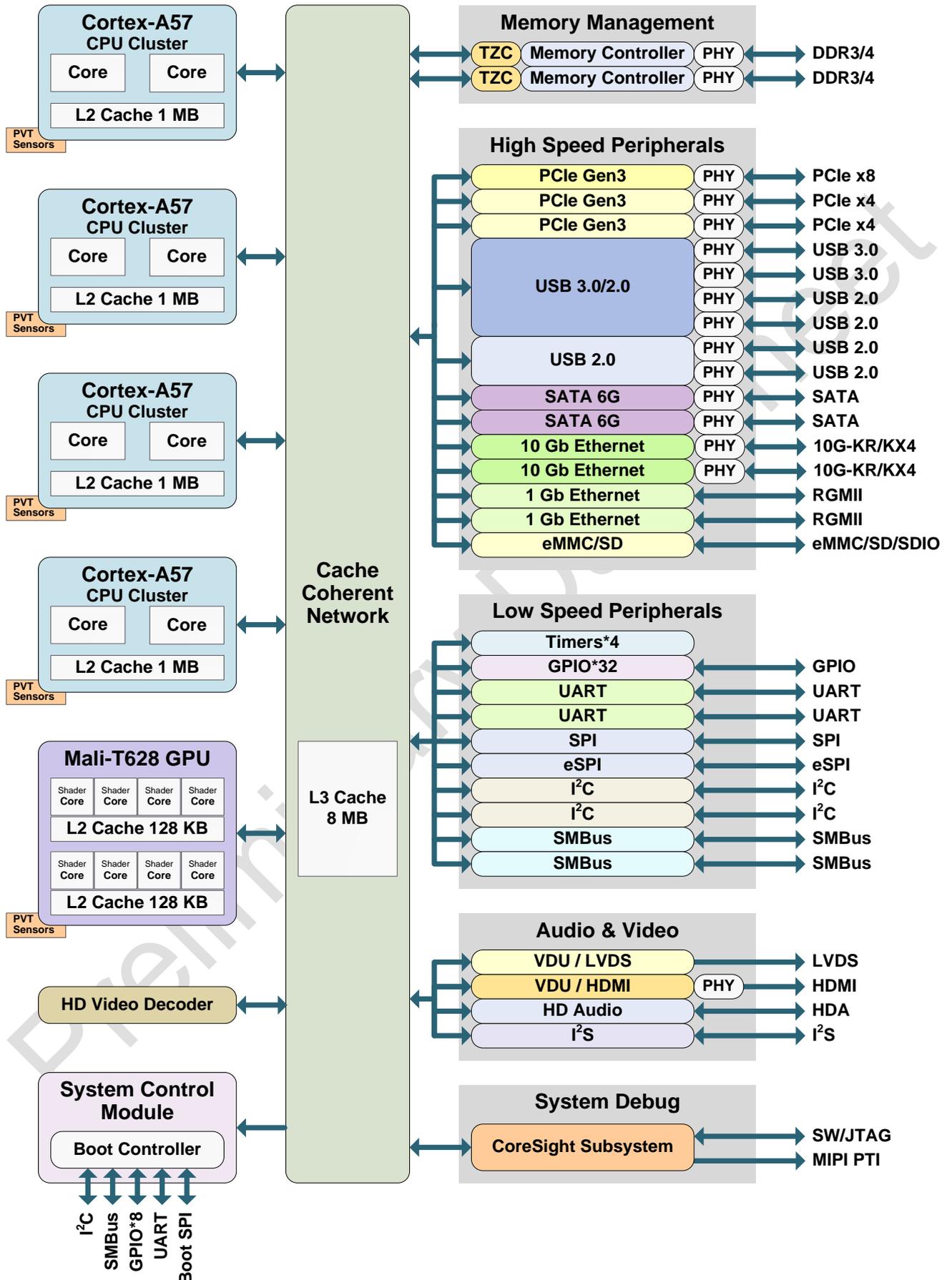


Figure 1-1 Block Diagram

2 Detailed Description

2.1 Arm Cortex-A57 CPU Clusters

The SoC contains 8 Arm Cortex-A57 cores in 4 clusters.

The Cortex-A57 cluster is a high-performance, low-power device that implements the [Armv8-A architecture](#).

Each cluster has two cores (up to 1.5 GHz) and L2 (1 MB) cache.

Each core has 48 KB L1 instruction cache and 32 KB L1 data cache.

None of the cores in the clusters include optional Arm Cortex-A57 core Cryptographic Engine.

A core can operate in one of two possible states, known as the secure and non-secure. By propagating the security state of the core through the on-chip interconnect to target based transaction filters, the TrustZone technology is extended into the SoC architecture, creating a robust platform supporting fully isolated Trusted and Non-trusted worlds.

2.2 Memory Management

2.2.1 DDR3/4 Memory Subsystem

The SoC supports two memory channels. Each channel contains TrustZone controller, DDR controller and DDR PHY.

Each subsystem supports the following features:

- Up to 64 GB physical memory per channel
- Up to 4 memory ranks per channel
- Integrated PHY
- Integrated TrustZone controller to provide capabilities for building trusted systems
- 64/32-bit DDR3 (speed grades up to DDR3-1600)
- 64/32-bit DDR4 (speed grades up to DDR4-2400)
- ECC: *single error correction/double error detection* (**SEC/DED**)
- 1:2 frequency ratio mode
- Low area, low power architecture
- Programmable support for 1T/2T memory command timing
- Software programmable *quality of service* (**QoS**)
- Automatic DDR3/4 low power mode operation

2.2.2 DMA Controller for Low Speed Peripherals

The DMAC LSP implements capability of direct data transfer between a low speed device, which is connected to a low speed peripheral interface, and memory without CPU usage.

It helps in maximizing system performance by decreasing a load of the SoC cores.

The DMAC can only work in non-secure mode and has the following main features:

- Handshaking interface with two UARTs, SPI, and two I²C controllers
- 8 channels, one per source and destination pair

- Unidirectional channels: data transfers in one direction only
- Multi-block transfers
- Single FIFO per channel for source and destination
- Automatic data packing or unpacking to fit FIFO width

2.3 Cache Coherent Network

Based on the Arm CoreLink™ CCN-504, CCN provides interconnection of the main SoC subsystems and manages the Level 3 cache for these subsystems.

The CCN provides the following key features:

- Dual simplex ring-bus interconnect topology
- Broadcast snoop channel
- DVM message transport between masters
- QoS regulation for shaping traffic profiles
- Monitoring performance-related events
- Error signal gathering using an error bus, with a single point of interrupt coordination on errors
- Separate caches for secure and non-secure transactions

2.4 System Control Module

The System Control Module is used to manage all the SoC subsystems.

It contains the following main blocks:

- *System control processor (SCP)* that runs service functions such as
 - Starts the SoC
 - Provides the initial configuration of all the SoC modules
 - Monitors the state of the SoC
- Boot controller that contains dedicated SPI used for initial boot
- UART, SMBus, GPIO*8, and I²C controllers used for system control functions
- *Clock Management Unit (CMU)* that controls system clock and reset signals

2.5 High Speed Peripherals

2.5.1 PCIe Gen 3.0

The SoC contains three *PCI Express (PCIe)* interfaces:

- PCIe x8 with 64 GT/s transfer rate
- Two PCIe x4, each with 32 GT/s transfer rate

Each PCIe subsystem contains PCIe Root Complex controller that provides base PCIe functionality in accordance with the **PCI Express Base Specification 3.0**.

Each PCIe provides the following main features:

- Integrated PHY

- Transfer rates up to 8.0 GT/s (~1GB/s) per single lane
- PCIe *active state power management* (**ASPM**)
- PCIe *advanced error reporting* (**AER**) with Multiple Header Logging
- *Internal address Translation Unit* (**iATU**)
- Embedded multichannel DMA controller
- Automatic Lane Reversal
- ECRC Generation and Checking
- Maximum Payload Size:
 - 256 bytes for PCIe x4
 - 512 bytes for PCIe x8
- 1 Virtual Channel for PCIe x4, 2 Virtual Channels for PCIe x8

Each PCIe can work both in secure and non-secure modes.

2.5.2 USB 3.0/2.0

The SoC contains two *Universal Serial Bus* (**USB**) controllers (USB 3.0/2.0 and USB 2.0) and six integrated PHY that provide six interfaces: two USB 3.0 interfaces and four USB 2.0 interfaces.

USB 3.0/2.0 controller is compatible with the **xHCI Specification** by Intel Corporation. It is optimized for the Super-Speed applications and systems and supports the following device types:

- Super-Speed devices via USB 3.0 interface (4 Gbps IN and 4 Gbps OUT)
- High-Speed, Full-Speed, and Low-Speed devices via any interface

USB 3.0/2.0 can work both in secure and non-secure modes.

USB 2.0 controller is compatible with the **xHCI Specification** by Intel Corporation. It is optimized for the high-bandwidth applications and systems and supports the following device types:

- High-Speed (480 Mbps)
- Full-Speed (12 Mbps)
- Low-Speed (1.5 Mbps)

USB 2.0 can work both in secure and non-secure modes.

2.5.3 SATA 6G

The SoC contains two identical *Serial ATA* (**SATA**) subsystems. Each SATA supports the following features:

- Integrated PHY
- SATA 6.0 Gb/s speeds
- Compliant with **Serial ATA 3.2** and **AHCI Revision 1.3** specifications
- 8b/10b encoding/decoding
- Error correction code
- Power management features including automatic partial-to-slumber transition
- Internal DMA engine per port

Each SATA can work both in secure and non-secure modes.

2.5.4 10 Gb Ethernet

The SoC contains two identical 10 Gb Ethernet interfaces, which enable to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2008 standard for two types of 10 Gb/s Ethernet: 10GBASE-KX4 and 10GBASE-KR.

Each interface contains a *10 Gb Ethernet media access controller (XGMAC)* with integrated *10 Gigabit Ethernet Physical Coding Sublayer (XPCS)* and 10 Gb Ethernet PHY.

Each XGMAC has the following main features:

- Full-duplex operation at 10 Gbps
- Full compliance with Clause 71 (10GBASE-KX4) and Clause 72 (10GBASE-KR) of the IEEE 802.3-2008 standard
- Full compliance with Clause 78 (*Energy Efficient Ethernet (EEE)* feature) of the IEEE 802.3az, standard for 10 Gbps operation
- Programmable frame length, supporting standard or jumbo (extendable to 16 KB) Ethernet frames
- Support for VLAN-tagged frame processing in compliance with the IEEE 802.1Q standard

Each XGMAC can work both in secure and non-secure modes.

2.5.5 1 Gb Ethernet

The module provides two identical *1 Gigabit media access controllers* (further **GMAC**).

Each controller enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2008 standard.

Each GMAC has the following main features:

- 10, 100, and 1000 Mbps data transfer rates with RGMII interface to communicate with an external gigabit PHY
- Full-duplex and half-duplex operation support
- Embedded DMA controller with independent Transmit and Receive engines

Each GMAC can work both in secure and non-secure modes.

2.5.6 eMMC/SD

It provides communication with memory cards targeted for the mobile/portable market and adheres to the **SD UHS-I** and **eMMC** Specifications.

The *Embedded Multimedia Card (eMMC)/Secure Digital (SD)* controller supports the following features:

- SD memory and *Secure Data Input/Output (SDIO)* digital interface protocol, and compliant with **SD HCI Specification**
- eMMC protocols including eMMC 5.1
- SD-HCI Host version 4 mode or less
- Embedded DMA controller
- Software tuning in SD UHS-I and eMMC modes

2.6 Low Speed Peripherals

2.6.1 GPIO*32

General Purpose Input/Output (GPIO) implements run-time 32-bit programmable interface for external communications. The GPIO controls the output data and direction of external I/O pads. It also can read back the data on external pads using memory-mapped registers.

The interface contains 32 individually controllable signals in a single port.

2.6.2 UART

There are two identical *Universal Asynchronous Receiver-Transmitters (UART)* in the SoC.

Each UART has a handshaking interface with the DMA LSP that can request and control non-secure data transfers between the UART and memory.

Each UART contains registers that control:

- Character length
- Baud rates up to 1.5 Mbaud
- Parity generation/checking
- Interrupt generation

2.6.3 SPI

The *Serial Peripheral Interface (SPI)* is a full-duplex master or slave-synchronous serial interface used for short distance communication with up to four external slave devices (SSx4).

It has a handshaking interface with the DMA LSP that can request and control data transfers between the SPI and memory.

A master (application processor or the DMA LSP) accesses data, control, and status information on the SPI through the APB interface.

The SPI operates as a serial master. It can connect to a serial-slave peripheral device.

2.6.4 eSPI

The *Enhanced Serial Peripheral Interface (eSPI)* is a synchronous serial communication interface used for short distance communication with up to eight external slave devices (SSx8).

Additional eSPI signals in compare to SPI Interface:

- RESET programmable as input or output
- ALERT input interrupts

An eSPI device communicates in full-duplex mode using master-slave architecture with up to eight external slave SPI devices (SSx8). It supports Single/Dual/Quad SPI mode of operation.

2.6.5 I²C

There are two identical general purpose *Inter-Integrated Circuits (I²C)* in the SoC.

The I²C is a programmable serial interface that provides support for the communications link between the devices connected to the bus.

Each I²C support the following features:

- Three speeds:
 - Standard mode (0 to 100 Kb/s)
 - Fast mode (≤ 400 Kb/s) or fast mode plus (≤ 1000 Kb/s)
 - High-speed mode (≤ 3.4 Mb/s)
- Master OR slave I²C operation
- 7- or 10-bit addressing
- 7- or 10-bit combined format transfers

Each I²C has a handshaking interface with the DMA LSP that can request and control non-secure data transfers between the I²C and memory.

2.6.6 SMBus

The SoC includes two identical *System Management Bus* (**SMBus**) interfaces.

This interface provides a two-wire bidirectional interface for transfer of bytes of information between multiple compliant I²C devices, typically with a microprocessor behind the DB-I²C master/slave controller and one or more master/slave devices.

2.7 Audio & Video

2.7.1 Arm Mali-T628 GPU

Provides a complete graphics acceleration platform based on open standards. It supports 2D graphics, 3D graphics, and *general purpose computing on GPU* (**GPGPU**).

The graphics processor provides the following main features:

- Two clusters
- 4 shader cores operating at 750 MHz per each cluster
- 128KB L2 Cache per each cluster
- Seamless load balancing across active shader cores
- The following APIs are supported:
 - OpenGL ES 1.1, 2.0, 3.0, 3.1
 - OpenCL 1.1
 - RenderScript
- *Full scene anti-aliasing* (4x**FSAA**, 16x**FSAA**) with minimal performance drop
- *Adaptive scalable texture compression* (**ASTC**): *low dynamic range* (**LDR**) and *high dynamic range* (**HDR**) are supported
- Native hardware support for 64-bit scalar and vector, integer and floating-point data types – fundamental to accelerate complex and computationally intensive algorithms

It can work both in secure and non-secure modes.

2.7.2 HD Video Decoder

Used to decode video streams encoded in the following formats:

- H.265 (HEVC)

- H.264, MPEG4, MPEG2, VP8, VP6, VC1, AVS, RealVideo, and JPEG: up to 1080p at 60 fps

The decoder loads the encoded video data from the system memory, decodes it and places the information ready to be sent to the video display unit into the frame buffer.

It can work both in secure and non-secure modes.

2.7.3 VDU with Quad LVDS

Visual Display Unit (VDU) with quad *Low-Voltage Differential Signaling (LVDS)* is a general purpose display controller used to drive a wide range of display devices varying in size and capability.

The module provides the following main features:

- Display resolution up to 2560x1440
- Color resolution of up to 24 bpp
- Embedded DMA controller
- Programmable vertical and horizontal timing parameters

2.7.4 VDU with HDMI 2.0

VDU with *High Definition Multimedia Interface (HDMI)* provides a complete HDMI interface for transmitting video and audio data to an HDMI-compliant source device, such as a computer monitor, video projector, digital television, or digital audio device.

The subsystem has the following main features:

- Display resolution up to 2560x1440
- VDU features:
 - Color resolution of up to 24 bpp
 - Embedded DMA Controller
 - Programmable vertical and horizontal timing parameters
- Three TMDS data channels with 6 Gbps data rate per channel
- Total maximum throughput of up to 18 Gbps (6 Gbps * 3 channels)
- HDMI 2.0 specification features:
 - All CEA-861-F video formats
 - *Dynamic range and mastering infoframe (DRM)*
- Embedded DMA controller for audio
- Audio stream bit rate up to 24.576 Mbps
- It can work both in secure and non-secure modes

2.7.5 HD Audio

The HD Audio controller is a bus mastering I/O peripheral, which is attached to system memory via interconnect. It contains one or more DMA engines, each of which can be set up to transfer a single audio "stream" to memory from the codec or from memory to the codec depending on the DMA type.

The HD Audio controller has the following features:

- Maximum number of input streams : 4

- Maximum number of output streams : 4
- Number of Serial Data Outputs (SDO): 2 (SDO 0 and SDO 1 : outputs to the codecs)
- Number of Serial Data Inputs (SDI): 2 (SDI 0 and SDI 1 : inputs from the codecs)
- Sample rate: up to 192 kHz
- Bit width per stream: up to 32 bit
- Number of channels: 10 (7.1 surround sound + 2)
- Number of SDO DMA engines: 4
- Number of SDI DMA engines: 4

NOTE: The HD Audio controller supports only Sample Base Rate of 48 kHz with a divider (2..8) and multiplier (2..4) for this base rate.

To support another sampling rate, for example, 44.1 or 11.025 kHz, you have to provide software resampling.

2.7.6 I²S

The *Inter-IC Sound (I²S)* is a programmable module used for the serial communication with peripherals.

It is designed to be used in systems that process digital audio signals, such as:

- A/D and D/A converters
- Digital signal processors
- Error correction for compact disc and digital recording
- Digital filters
- Digital input/output interfaces

2.8 System Monitoring and Debug

2.8.1 PVT Controllers

The SoC contains five *Process, Voltage and Temperature (PVT)* controllers used to monitor the Cortex-A57 clusters and Mali-T628 GPU.

2.8.2 CoreSight Subsystem

Provides a standard implementation of the Arm Debug Interface for debug tools to work with:

- Serial Wire or JTAG Debug Port
- Trace Port Interface

The subsystem supports the following methods of debugging the SoC:

- “External” debug—conventional debug through the SW/JTAG interface
- “Self-hosted” debug—conventional debug with the processor running using a debug monitor that resides in memory
- Logging of hardware and software events in a trace, which is recorded in memory as well as transmitted through the *trace port interface (MIPI PTI)* to an external debug system

It can work both in secure and non-secure modes.

3 Electrical Specifications

NOTE: The electrical characteristics are subject to change and clarification without extra notification.

3.1 Power Supply Parameters

BE-M1000 requires six isolated voltage supplies and single unified ground supply as shown in the following table.

Table 3-1 BE-M1000 Power Domains

Supply Type	Package Pin Name	Voltage, V	Max Power, W
Core supply	VDD		
0.95V voltage supply	VDD_HDMI_09 VDD_USB2_09 VDD_USB3_0_09 VDD_USB3_1_09 VDD_USB3TX_0_09 VDD_USB3TX_1_09 VDD_USB3_VP_0_09 VDD_USB3_VP_1_09 VDD_PCIE4_0_09 VDD_PCIE4_1_09 VDD_PCIE8_09 VDD_SATA_09 VDD_SATATX_09 VDD_XG0_09 VDD_XG1_09	0.95 ± 5%	24
PLL supply	VDDPLL_0_09 VDDPLL_1_09 VDDPLL_2_09 VDDPLL_3_09 VDDPLL_HDMI_09	0.95 ± 5%	0.20
DDR supply	VDDQ_DDR0 VDDQ_DDR1	DDR4: 1.2 ± 5%	6.0
1.5V voltage supply	VDD_PCIE4_0_15 VDD_PCIE4_1_15 VDD_PCIE8_15 VDD_XG0_15 VDD_XG1_15	1.5 ± 5%	2.0

Supply Type	Package Pin Name	Voltage, V	Max Power, W
1.8V voltage supply	VDD_DDR0_PLL VDD_DDR1_PLL VDD_HDMI_18 VDD_PVT_18 VDD_SATA_18 VDD_USB2_18 VDDIO	1.8 ± 10%	1.8
3.3V voltage supply	VDD_SD_33 VDD_USB2_0_33 VDD_USB2_1_33 VDD_USB2_2_33 VDD_USB2_3_33 VDD_USB3_33	3.3 -6.9% +4.8%	0.7
Ground	VSS	-	-
Total			~34.7W

3.2 External Clocking

3.2.1 Reference Clock Signals

Table 3-2 Reference Clock Signals

Clock Signal	Pin Names	Frequency	Notes
Reference clock	CLK25M	25 MHz	-
XGbE PHY reference clock	XG0_REF_CLKN ^{1,2} XG0_REF_CLKP ^{1,2} XG1_REF_CLKN ^{1,2} XG1_REF_CLKP ^{1,2}	156.25 MHz	Differential pair Terminated ³ and unterminated ⁴ clocks
PCIe PHY reference clock	PCIE4_0_REF_CLKN ^{1,2} PCIE4_0_REF_CLKP ^{1,2} PCIE4_1_REF_CLKN ^{1,2} PCIE4_1_REF_CLKP ^{1,2} PCIE8_REF_CLKN ^{1,2} PCIE8_REF_CLKP ^{1,2}	100 MHz	Differential pair Terminated ³ and unterminated ⁴ clocks
SATA PHY reference clock	SATA_REFCLKP ^{1,2} SATA_REFCLKM ^{1,2}	100 MHz	Differential pair Terminated ³ and unterminated ⁴ clocks

Clock Signal	Pin Names	Frequency	Notes
USB 3.0 PHY optional reference clock input	USB3_0_REFCLKN ^{1,2} USB3_0_REFCLKP ^{1,2} USB3_1_REFCLKN ^{1,2} USB3_1_REFCLKP ^{1,2}	100 MHz (typical)	Differential pair
USB 2.0 PHY: XI - crystal oscillator XO - crystal oscillator or board reference clock input	USB2_0_XI ^{1,2} USB2_0_XO ^{1,2} USB2_1_XI ^{1,2} USB2_1_XO ^{1,2} USB2_2_XI ^{1,2} USB2_2_XO ^{1,2} USB2_3_XI ^{1,2} USB2_3_XO ^{1,2}	50 MHz	
HDMI PLL reference clock input	HDMI_PLL_27M ^{1,2}	27 MHz	
LVDS PLL reference clock input	LVDS_PLL_27M ^{1,2}	27 MHz	

NOTE:

- 1 If the reference clock pins are unused, they should be tied off to the ground potential
- 2 Reference clocks connect as needed
- 3 With terminated clocks, a 50 Ohms termination resistor is soldered on the board close to the SoC, preventing clock reflections while providing a clock source to the PHY
- 4 If the board clocks are unterminated, the clock's signal level will double as it hits the high-impedance input of the PHY reference clock inputs. This effect can also be used to provide a clean clock to the PHY, but ensure that the signal swing of the reference clock is not too high after doubling the amplitude

3.2.2 Reference Clock Requirements

3.2.2.1 Reference Clock (CLK25M)

Table 3-3 Reference Clock (CLK25M) Requirements

Parameter	Min	Typ	Max	Unit
Frequency range		25		MHz
Reference clock frequency offset	-50		50	ppm
Reference clock random jitter (RMS)		10		ps
Reference clock cycle to cycle jitter		6		ps
Startup time		1.5	3.0	ms
Disable time		20	100	ns
Disable stand-by current			15	uA

3.2.2.2 SATA PHY Reference Clock

Table 3-4 SATA PHY Reference Clock Requirements

Parameter	Min	Typ	Max	Unit	Conditions
Frequency range		100		MHz	
Reference clock frequency offset	-350		350	ppm	
Reference clock random jitter (RMS)			3	ps	1.5 MHz to Nyquist frequency. For example, for 100 MHz reference clock, the Nyquist frequency is 50 MHz
Reference clock cycle to cycle jitter			150	ps	DJ across all frequencies
Duty cycle	40		60	%	
Common mode input level	0		vp	V	Differential inputs
Differential input swing	0.3			Vpp	Differential inputs ¹
Single-ended input logic low	-0.3		0.3	V	If single-ended input is used
Single-ended input logic high	vp-0.3		vp+0.3	V	If single-ended input is used
Input edge rate	0.6			V/ns	
Reference clock skew (±)			200	ps	

3.2.2.3 XGbE PHY Reference Clock

The PHY supports a differential reference clock source. The source may be driven through either external pads or internal pins. The chosen reference clock must meet specific requirements for signal swing and jitter. The following table summarizes the requirements of the reference clock provided to the PHY.

Table 3-5 XGbE PHY Reference Clock Requirements

Parameter	Min	Typ	Max	Unit	Conditions
Frequency range		156.25		MHz	
Frequency stability	-100		100	ppm	
Differential input swing	300		1890	mVppd	
Duty cycle	40		60	%	
Input edge rate	0.6			V/ns	
Coupling					AC coupling
Allowed jitter for 10GBASE-KR and slower			2.25	ps (rms)	Integrated from 12 kHz to 20 MHz
Allowed jitter for 10GBASE-KX4			3.6	ps (rms)	Integrated from 12 kHz to 20 MHz
Peak to peak period jitter of the reference clock			20	ps	Period jitter measured over 10k samples

¹ $VDREF_CLK/4 + VCMREF_CLK \leq vp + \text{diode forward-biasing voltage}$ and $VCMREF_CLK - VDREF_CLK/4 \geq -\text{diode forward biasing voltage}$

Parameter	Min	Typ	Max	Unit	Conditions
Phase jitter			2	ps	Integrated from 1.5 MHz to Nyquist frequency. For example, for 100 MHz reference clock, the Nyquist frequency is 50 MHz

3.2.2.4 PCIe PHY Reference Clock

Table 3-6 PCIe PHY Reference Clock Requirements

Parameter	Min	Typ	Max	Unit	Conditions
Frequency range		100		MHz	
Frequency stability	-300		300	ppm	
Differential input swing	300		1890	mVppd	
Duty cycle	40		60	%	
Input edge rate	0.6			V/ns	
Coupling					AC coupling

NOTE: 100 MHz is the only PCIe standard compliant frequency. When using a 125 MHz frequency, the PHY may not be compliant to all PCIe specifications, such as PLL bandwidth, peaking, and jitter.

3.2.2.5 USB 3.0 PHY Reference Clock

The USB 3.0 PHY is designed to handle a wide range of input clock frequencies to support both host and device applications. The following table summarizes the requirements of the reference clock provided to the USB 3.0 PHY to support SuperSpeed only or both SuperSpeed and high-speed operations.

Table 3-7 USB 3.0 PHY Reference Clock Requirements

Parameter	Min	Typ	Max	Unit	Conditions
Reference clock frequency	19.2	100	200	MHz	
Reference clock frequency stability	-300		300	ppm	
Reference clock random jitter (RMS)			3	ps	1.5 MHz to Nyquist frequency. For example, for 100 MHz reference clock, the Nyquist frequency is 50 MHz
Reference clock skew			200	ps	
Reference clock cycle-to-cycle jitter			150	ps	DJ over all frequency
Duty cycle	40		60	%	
Common mode input level	0		1.32	V	Differential inputs

Parameter	Min	Typ	Max	Unit	Conditions
Differential input swing	0.3			V _{pp}	Differential inputs ¹
Single-ended input logic: Low	-0.3		0.3	V	If single-ended input is used
Single-ended input logic: High	vp-0.3		vp	V	If single-ended input is used
Input edge rate	0.6		4	V/ns	
Required external reference resistance		200		Ohms	± 1% accuracy

3.2.2.6 USB 2.0 PHY Reference Clock

The USB 2.0 PHY supports the following reference clock sources:

- **Crystal Oscillator connected to the USB2*_XI and USB2*_XO pins:** The crystal oscillator must have a frequency tolerance of ±400 ppm, peak jitter of ±100 ps, and an output differential voltage of no less than 500 mV with respect to the XI signal
- **External Clock connected to the USB2*_XO pin:** The clock must have a fundamental frequency of 50 MHz, with a frequency tolerance of ± 400 ppm, peak jitter of ± 100 ps, duty cycle between 40/60 and 60/40 percent, and signal swing of 1.8V.

3.2.2.7 HDMI PLL Reference Clock

Table 3-8 HDMI PLL Reference Clock Requirements

Parameter	Min	Typical	Max	Unit
Frequency range		27		MHz
Frequency stability	-50		50	ppm
Output		LVCMOS 1.8		V
Duty cycle	40		60	%

3.2.2.8 LVDS PLL Reference Clock

Table 3-9 LVDS PLL Reference Clock Requirements

Parameter	Min	Typical	Max	Unit
Frequency range		27		MHz
Frequency stability	-50		50	ppm
Output		LVCMOS 1.8		V
Duty cycle	40		60	%

¹ $VDREF_CLK / 4 + VCMREF_CLK \leq vp + \text{diode forward biasing voltage}$ and $VCMREF_CLK - VDREF_CLK / 4 \geq -\text{diode forward biasing voltage}$

4 Power-Up/Down

4.1 Power-Up Sequence

The following steps have to be performed to power up the SoC:

1. Provide the `RESET_N` reset signal (active is low)
2. Apply voltages to power pins according to [Power Supply Parameters](#) in the following order:
 - 3.3V voltage supply
 - 1.5V voltage supply
 - PLL supply
 - DDR supply
3. Provide the `CS_TRST_N` reset signal
4. Provide the `TRSTN` reset signal
5. Apply voltages to power pins according to [Power Supply Parameters](#) in the following order:
 - 1.8V voltage supply
 - Core supply and 0.95V voltage supply
6. Provide all reference clocks
7. Wait at least 16 cycles of the reference clock
8. Deassert the `RESET_N` signal

Once the `RESET_N` signal is deasserted, the boot controller provides initialization of clock and reset signals for each SoC subsystem, loads and executes the Boot Loader, which is stored in the Boot SPI Flash.

4.2 Power-Down Sequence

Power-down sequence is the reverse of the power-up sequence.

5 Pin Assignment

5.1 Pinout List

The following tables contain the list of I/O pins of the SoC including the power supply and ground pins. The following legend is applied for the following tables.

Legend:

I	Input
O	Output
IO	Input/Output
A	Analog
P	Power supply
G	Ground
NC	Not connected

NOTE: Pin IDs are represented in *BE-M1000 Pinout List*. The file is available in the description of BE-M1000 on [Baikal Electronics website](#).

5.1.1 Memory Management

5.1.1.1 DDR3/4

Table 5-1 DDR Pins

Pin Name	Type	Power Domain	Description
DDR0_A[13:0]	O	VDDQ_DDR0	SDRAM address
DDR0_A[14]	O	VDDQ_DDR0	SDRAM WE
DDR0_A[15]	O	VDDQ_DDR0	SDRAM CAS
DDR0_A[16]	O	VDDQ_DDR0	SDRAM RAS
DDR0_A[17]	O	VDDQ_DDR0	SDRAM A[17]
DDR0_ACT_N	O	VDDQ_DDR0	When low, indicates the activate (open row) command
DDR0_ALERT_N	I	VDDQ_DDR0	SDRAM CRC/parity error
DDR0_ATO	A		Analog test output (test pad) NOTE: Reserved in BE-M1000 manufactured since 2021
DDR0_BA[1:0]	O	VDDQ_DDR0	SDRAM bank address
DDR0_BG[1:0]	O	VDDQ_DDR0	SDRAM bank group
DDR0_CK[3:0]	O	VDDQ_DDR0	SDRAM clock
DDR0_CK_N[3:0]	O	VDDQ_DDR0	SDRAM clock
DDR0_CKE[3:0]	O	VDDQ_DDR0	SDRAM clock enable
DDR0_CS_N[3:0]	O	VDDQ_DDR0	SDRAM chip select
DDR0_DM[8:0]	IO	VDDQ_DDR0	SDRAM data mask
DDR0_DQ[63:0]	IO	VDDQ_DDR0	SDRAM data
DDR0_DQS[8:0]	IO	VDDQ_DDR0	SDRAM data strobe
DDR0_DQS_N[8:0]	IO	VDDQ_DDR0	SDRAM data strobe

Pin Name	Type	Power Domain	Description
DDR0.DTO[1:0]	O	VDDQ_DDR0	Digital test output (test pad) NOTE: Reserved in BE-M1000 manufactured since 2021
DDR0.ECC[7:0]	IO	VDDQ_DDR0	SDRAM data ECC
DDR0.MIRROR	O	VDDQ_DDR0	SDRAM mirror (optional DIMM signal)
DDR0.ODT[3:0]	O	VDDQ_DDR0	SDRAM on-die termination
DDR0.PARITY	O	VDDQ_DDR0	SDRAM parity
DDR0.QCSEN_N	O	VDDQ_DDR0	SDRAM quad CS enable (optional DIMM signal)
DDR0.RAM_RST_N	O	VDDQ_DDR0	SDRAM reset
DDR0.VREFI[9:0]	A		IO ring VREFI net NOTE: Reserved in BE-M1000 manufactured since 2021
DDR0.VREFI_ZQ	A		IO ring VREFI ZQ net
DDR0.ZQ	A		ZQ resistor (to external calibration resistor). Connect the pin through an external $240 \pm 1\%$ Ohms resistor to ground
DDR1.A[13:0]	O	VDDQ_DDR1	SDRAM address
DDR1.A[14]	O	VDDQ_DDR1	SDRAM WE
DDR1.A[15]	O	VDDQ_DDR1	SDRAM CAS
DDR1.A[16]	O	VDDQ_DDR1	SDRAM RAS
DDR1.A[17]	O	VDDQ_DDR1	SDRAM A[17]
DDR1.ACT_N	O	VDDQ_DDR1	When low, indicates the activate (open row) command
DDR1.ALERT_N	I	VDDQ_DDR1	SDRAM CRC/parity error
DDR1.ATO	A		Analog test output (test pad) NOTE: Reserved in BE-M1000 manufactured since 2021
DDR1.BA[1:0]	O	VDDQ_DDR1	SDRAM bank address
DDR1.BG[1:0]	O	VDDQ_DDR1	SDRAM bank Group
DDR1.CK[3:0]	O	VDDQ_DDR1	SDRAM clock
DDR1.CK_N[3:0]	O	VDDQ_DDR1	SDRAM clock
DDR1.CKE[3:0]	O	VDDQ_DDR1	SDRAM clock enable
DDR1.CS_N[3:0]	O	VDDQ_DDR1	SDRAM chip select
DDR1.DM[8:0]	IO	VDDQ_DDR1	SDRAM data mask
DDR1.DQ[63:0]	IO	VDDQ_DDR1	SDRAM data
DDR1.DQS[8:0]	IO	VDDQ_DDR1	SDRAM data strobe
DDR1.DQS_N[8:0]	IO	VDDQ_DDR1	SDRAM data strobe

Pin Name	Type	Power Domain	Description
DDR1_DTO[1:0]	O	VDDQ_DDR1	Digital test output (test pad) NOTE: Reserved in BE-M1000 manufactured since 2021
DDR1_ECC[7:0]	IO	VDDQ_DDR1	SDRAM data ECC
DDR1_MIRROR	O	VDDQ_DDR1	SDRAM mirror (optional DIMM signal)
DDR1_ODT[3:0]	O	VDDQ_DDR1	SDRAM on-die termination
DDR1_PARITY	O	VDDQ_DDR1	SDRAM parity
DDR1_QCSEN_N	O	VDDQ_DDR1	SDRAM quad CS enable (optional DIMM signal)
DDR1_RAM_RST_N	O	VDDQ_DDR1	SDRAM reset
DDR1_VREFI[9:0]	A		IO ring VREFI net NOTE: Reserved in BE-M1000 manufactured since 2021
DDR1_VREFI_ZQ	A		IO ring VREFI ZQ net
DDR1_ZQ	A		ZQ resistor (to external calibration resistor). Connect the pin through an external $240 \pm 1\%$ Ohms resistor to ground

5.1.2 High Speed Peripherals

5.1.2.1 PCIe x8

Table 5-2 PCIe x8 Pins

Pin Name	Type	Power Domain	Description
PCIE8_AMON0	O	VDD_PCIE8_15	Analog monitor bump NOTE: Reserved in BE-M1000 manufactured since 2021 Voltage range: 0 – 1.575 V
PCIE8_AMON1	O	VDD_PCIE8_15	Analog monitor bump NOTE: Reserved in BE-M1000 manufactured since 2021 Voltage range: 0 – 1.575 V
PCIE8_ATT_BUT	I	VDDIO_18	Indicates that the system attention button was pressed NOTE: Reserved in BE-M1000 manufactured since 2021
PCIE8_ATT_IND[1:0]	O	VDDIO_18	Controls the system attention indicator NOTE: Reserved in BE-M1000 manufactured since 2021
PCIE8_CMD_INT	I	VDDIO_18	Hot-plug controller command completed interrupt NOTE: Reserved in BE-M1000 manufactured since 2021
PCIE8_DMON0	O	VDD_PCIE8_09	Differential digital monitor bump NOTE: Reserved in BE-M1000 manufactured since 2021 Voltage range: 0 – 0.9975 V

Pin Name	Type	Power Domain	Description
PCIE8_DMON1	O	VDD_PCIE8_09	Differential digital monitor bump NOTE: Reserved in BE-M1000 manufactured since 2021 Voltage range: 0 – 0.9975 V
PCIE8_DMONB0	O	VDD_PCIE8_09	Differential digital monitor bump NOTE: Reserved in BE-M1000 manufactured since 2021 Voltage range: 0 – 0.9975 V
PCIE8_DMONB1	O	VDD_PCIE8_09	Differential digital monitor bump NOTE: Reserved in BE-M1000 manufactured since 2021 Voltage range: 0 – 0.9975 V
PCIE8_INTRL_CTRL	O	VDDIO_18	Electromechanical Interlock Control NOTE: Reserved in BE-M1000 manufactured since 2021
PCIE8_INTRL_ENG	I	VDDIO_18	System Electromechanical Interlock Engaged NOTE: Reserved in BE-M1000 manufactured since 2021
PCIE8_MRL_SENS	I	VDDIO_18	MRL sensor state. Indicates the state of the <i>manually-operated retention latch (MRL)</i> sensor: <ul style="list-style-type: none"> • 0: MRL is closed • 1: MRL is open NOTE: Reserved in BE-M1000 manufactured since 2021
PCIE8_PRES_ST	I	VDDIO_18	Presence detect state NOTE: Reserved in BE-M1000 manufactured since 2021
PCIE8_PWR_CTRL	O	VDDIO_18	Controls the system power controller NOTE: Reserved in BE-M1000 manufactured since 2021
PCIE8_PWR_FAULT	I	VDDIO_18	Power fault detect NOTE: Reserved in BE-M1000 manufactured since 2021
PCIE8_PWR_IND[1:0]	O	VDDIO_18	Controls the system power indicator NOTE: Reserved in BE-M1000 manufactured since 2021
PCIE8_RBIAS0	IO	VDD_PCIE8_15	Bias resistor bump. The pin connects to 1 kOhms ± 1% precision resistor on board Voltage range: 0 – 1.575 V
PCIE8_RBIAS1	IO	VDD_PCIE8_15	Bias resistor bump. The pin connects to 1 kOhms ± 1% precision resistor on board Voltage range: 0 – 1.575 V
PCIE8_REF_CLKN	I	VDD_PCIE8_15	Reference clock differential pair
PCIE8_REF_CLKP	I	VDD_PCIE8_15	Reference clock differential pair
PCIE8_RXN[7:0]	I	VDD_PCIE8_15	Receive data differential pair

Pin Name	Type	Power Domain	Description
PCIE8_RXP[7:0]	I	VDD_PCIE8_15	Receive data differential pair
PCIE8_TXN[7:0]	O	VDD_PCIE8_15	Transmit data differential pair
PCIE8_TXP[7:0]	O	VDD_PCIE8_15	Transmit data differential pair

5.1.2.2 PCIe x4

Table 5-3 PCIe x4 Pins

Pin Name	Type	Power Domain	Description
PCIE4_0_AMON	O	VDD_PCIE4_0_15	Analog monitor bump NOTE: Reserved in BE-M1000 manufactured since 2021 Voltage range: 0 – 1.575 V
PCIE4_0_ATT_BUT	I	VDDIO_18	Attention button pressed NOTE: Reserved in BE-M1000 manufactured since 2021
PCIE4_0_ATT_IND[1:0]	O	VDDIO_18	Controls the system attention indicator NOTE: Reserved in BE-M1000 manufactured since 2021
PCIE4_0_CMD_INT	I	VDDIO_18	Hot-plug controller command completed interrupt NOTE: Reserved in BE-M1000 manufactured since 2021
PCIE4_0_DMON	O	VDD_PCIE4_0_09	Differential digital monitor bump NOTE: Reserved in BE-M1000 manufactured since 2021 Voltage range: 0 – 0.9975 V
PCIE4_0_DMONB	O	VDD_PCIE4_0_09	Differential digital monitor bump NOTE: Reserved in BE-M1000 manufactured since 2021 Voltage range: 0 – 0.9975 V
PCIE4_0_INTRL_CTRL	O	VDDIO_18	Electromechanical Interlock Control NOTE: Reserved in BE-M1000 manufactured since 2021
PCIE4_0_INTRL_ENG	I	VDDIO_18	System Electromechanical Interlock Engaged NOTE: Reserved in BE-M1000 manufactured since 2021
PCIE4_0_MRL_SENS	I	VDDIO_18	MRL sensor state. Indicates the state of the <i>manually-operated retention latch (MRL)</i> sensor: <ul style="list-style-type: none"> • 0: MRL is closed • 1: MRL is open NOTE: Reserved in BE-M1000 manufactured since 2021
PCIE4_0_PRES_ST	I	VDDIO_18	Presence detect state NOTE: Reserved in BE-M1000 manufactured since 2021

Pin Name	Type	Power Domain	Description
PCIE4_0_PWR_CTRL	O	VDDIO_18	Controls the system power controller NOTE: Reserved in BE-M1000 manufactured since 2021
PCIE4_0_PWR_FAULT	I	VDDIO_18	Power fault detect NOTE: Reserved in BE-M1000 manufactured since 2021
PCIE4_0_PWR_IND[1:0]	O	VDDIO_18	Controls the system power indicator NOTE: Reserved in BE-M1000 manufactured since 2021
PCIE4_0_RBIAS	IO	VDD_PCIE4_0_15	Bias resistor bump. The pin connects to 1 kOhms ± 1% precision resistor on board Voltage range: 0 – 1.575 V
PCIE4_0_REF_CLKN	I	VDD_PCIE4_0_15	Reference clock differential pair
PCIE4_0_REF_CLKP	I	VDD_PCIE4_0_15	Reference clock differential pair
PCIE4_0_RXN[3:0]	I	VDD_PCIE4_0_15	Receive data differential pair
PCIE4_0_RXP[3:0]	I	VDD_PCIE4_0_15	Receive data differential pair
PCIE4_0_TXN[3:0]	O	VDD_PCIE4_0_15	Transmit data differential pair
PCIE4_0_TXP[3:0]	O	VDD_PCIE4_0_15	Transmit data differential pair
PCIE4_1_AMON	O	VDD_PCIE4_1_15	Analog monitor bump NOTE: Reserved in BE-M1000 manufactured since 2021 Voltage range: 0 – 1.575 V
PCIE4_1_ATT_BUT	I	VDDIO_18	Attention button pressed NOTE: Reserved in BE-M1000 manufactured since 2021
PCIE4_1_ATT_IND[1:0]	O	VDDIO_18	Controls the system attention indicator NOTE: Reserved in BE-M1000 manufactured since 2021
PCIE4_1_CMD_INT	I	VDDIO_18	Hot-plug controller command completed interrupt NOTE: Reserved in BE-M1000 manufactured since 2021
PCIE4_1_DMON	O	VDD_PCIE4_1_09	Differential digital monitor bump NOTE: Reserved in BE-M1000 manufactured since 2021 Voltage range: 0 – 0.9975 V
PCIE4_1_DMONB	O	VDD_PCIE4_1_09	Differential digital monitor bump NOTE: Reserved in BE-M1000 manufactured since 2021 Voltage range: 0 – 0.9975 V
PCIE4_1_INTRL_CTRL	O	VDDIO_18	Electromechanical Interlock Control NOTE: Reserved in BE-M1000 manufactured since 2021

Pin Name	Type	Power Domain	Description
PCIE4_1_INTRL_ENG	I	VDDIO_18	System Electromechanical Interlock Engaged NOTE: Reserved in BE-M1000 manufactured since 2021
PCIE4_1_MRL_SENS	I	VDDIO_18	MRL sensor state. Indicates the state of the <i>manually-operated retention latch (MRL)</i> sensor: <ul style="list-style-type: none"> 0: MRL is closed 1: MRL is open NOTE: Reserved in BE-M1000 manufactured since 2021
PCIE4_1_PRES_ST	I	VDDIO_18	Presence detect state NOTE: Reserved in BE-M1000 manufactured since 2021
PCIE4_1_PWR_CTRL	O	VDDIO_18	Controls the system power controller NOTE: Reserved in BE-M1000 manufactured since 2021
PCIE4_1_PWR_FAULT	I	VDDIO_18	Power fault detect NOTE: Reserved in BE-M1000 manufactured since 2021
PCIE4_1_PWR_IND[1:0]	O	VDDIO_18	Controls the system power indicator NOTE: Reserved in BE-M1000 manufactured since 2021
PCIE4_1_RBIAS	IO	VDD_PCIE4_1_15	Bias resistor bump. The pin connects to 1 kOhms ± 1% precision resistor on board Voltage range: 0 – 1.575 V
PCIE4_1_REF_CLKN	I	VDD_PCIE4_1_15	Reference clock differential pair
PCIE4_1_REF_CLKP	I	VDD_PCIE4_1_15	Reference clock differential pair
PCIE4_1_RXN[3:0]	I	VDD_PCIE4_1_15	Receive data differential pair
PCIE4_1_RXP[3:0]	I	VDD_PCIE4_1_15	Receive data differential pair
PCIE4_1_TXN[3:0]	O	VDD_PCIE4_1_15	Transmit data differential pair
PCIE4_1_TXP[3:0]	O	VDD_PCIE4_1_15	Transmit data differential pair

5.1.2.3 USB 3.0/2.0

Table 5-4 USB Pins

Pin Name	Type	Power Domain	Description
USB2_0_CTRL	O	VDDIO_18	Port power control

Pin Name	Type	Power Domain	Description
USB2_0_DM0	IO	VDD_USB2_0_33	USB D- signal. In normal operation it carries USB data to and from the USB 2.0 PHY. In <i>High-Speed (HS)</i> operation, this pin receives/transmits a maximum of 800 mV or 400 mV nominally. In <i>Full-Speed (FS)</i> or <i>Low-Speed (LS)</i> operation, this pin receives/transmits 3.3V nominally Voltage range: 0 – 3.3 V (In a 5V short condition, the signal can have a maximum of 5.25V on it with respect to the ground)
USB2_0_DP0	IO	VDD_USB2_0_33	USB D+ signal. In normal operation it carries USB data to and from the USB 2.0 PHY. In <i>High-Speed (HS)</i> operation, this pin receives/transmits a maximum of 800 mV or 400 mV nominally. In <i>Full-Speed (FS)</i> or <i>Low-Speed (LS)</i> operation, this pin receives/transmits 3.3V nominally Voltage range: 0 – 3.3 V (In a 5V short condition, the signal can have a maximum of 5.25V on it with respect to the ground)
USB2_0_ID0	IO	VDD_USB2_18	USB mini-receptacle identifier or alternate test point for DC points probes inside USB 2.0 PHY Voltage range: 0 – 1.8 V
USB2_0_OVCUR	I	VDDIO_18	Port overcurrent
USB2_0_RT	IO	VDD_USB2_18	Transmitter resistor tune pin. It connects to an external resistor (200 ± 1% Ohms) that adjusts the USB 2.0 PHY's high-speed source impedance Voltage range: 0 – 1.8 V
USB2_0_VBUS0	A		USB 5V signal. This is the USB 5V supply. A charge pump external to the USB 2.0 PHY must provide power to this pin. The nominal voltage for this pin is 5V Voltage range: 0 – 5.25 V
USB2_0_XI	I	VDD_USB2_18	Crystal oscillator XI pin Voltage range: 0 – 1.8 V
USB2_0_XO	I	VDD_USB2_18	Crystal oscillator XO pin or board reference clock input. NOTE: When the reference clock source is a crystal, XO pin is a connection to a crystal. When the reference clock source is an aexternal board clock, XO is an input. For modeling and simulation purposes, XO is declared as a pure input Voltage range: 0 – 1.8 V
USB2_1_CTRL	O	VDDIO_18	Port power control

Pin Name	Type	Power Domain	Description
USB2_1_DM0	IO	VDD_USB2_1_33	USB D- signal. In normal operation it carries USB data to and from the USB 2.0 PHY. In <i>High-Speed (HS)</i> operation, this pin receives/transmits a maximum of 800 mV or 400 mV nominally. In <i>Full-Speed (FS)</i> or <i>Low-Speed (LS)</i> operation, this pin receives/transmits 3.3V nominally Voltage range: 0 – 3.3 V (In a 5V short condition, the signal can have a maximum of 5.25V on it with respect to the ground)
USB2_1_DP0	IO	VDD_USB2_1_33	USB D+ signal. In normal operation it carries USB data to and from the USB 2.0 PHY. In <i>High-Speed (HS)</i> operation, this pin receives/transmits a maximum of 800 mV or 400 mV nominally. In <i>Full-Speed (FS)</i> or <i>Low-Speed (LS)</i> operation, this pin receives/transmits 3.3V nominally Voltage range: 0 – 3.3 V (In a 5V short condition, the signal can have a maximum of 5.25V on it with respect to the ground)
USB2_1_ID0	IO	VDD_USB2_18	USB mini-receptacle identifier or alternate test point for DC points probes inside USB 2.0 PHY Voltage range: 0 – 1.8 V
USB2_1_OVCUR	I	VDDIO_18	Port overcurrent
USB2_1_RT	IO	VDD_USB2_18	Transmitter resistor tune pin. It connects to an external resistor (200 ± 1% Ohms) that adjusts the USB 2.0 PHY's high-speed source impedance Voltage range: 0 – 1.8 V
USB2_1_VBUS0	A		USB 5V signal. This is the USB 5V supply. A charge pump external to the USB 2.0 PHY must provide power to this pin. The nominal voltage for this pin is 5V Voltage range: 0 – 5.25 V
USB2_1_XI	I	VDD_USB2_18	Crystal oscillator XI pin Voltage range: 0 – 1.8 V
USB2_1_XO	I	VDD_USB2_18	Crystal oscillator XO pin or board reference clock input. NOTE: When the reference clock source is a crystal, XO pin is a connection to a crystal. When the reference clock source is an aexternal board clock, XO is an input. For modeling and simulation purposes, XO is declared as a pure input Voltage range: 0 – 1.8 V
USB2_2_CTRL	O	VDDIO_18	Port power control

Pin Name	Type	Power Domain	Description
USB2_2_DM0	IO	VDD_USB2_2_33	USB D- signal. In normal operation it carries USB data to and from the USB 2.0 PHY. In <i>High-Speed (HS)</i> operation, this pin receives/transmits a maximum of 800 mV or 400 mV nominally. In <i>Full-Speed (FS)</i> or <i>Low-Speed (LS)</i> operation, this pin receives/transmits 3.3V nominally Voltage range: 0 – 3.3 V (In a 5V short condition, the signal can have a maximum of 5.25V on it with respect to the ground)
USB2_2_DP0	IO	VDD_USB2_2_33	USB D+ signal. In normal operation it carries USB data to and from the USB 2.0 PHY. In <i>High-Speed (HS)</i> operation, this pin receives/transmits a maximum of 800 mV or 400 mV nominally. In <i>Full-Speed (FS)</i> or <i>Low-Speed (LS)</i> operation, this pin receives/transmits 3.3V nominally Voltage range: 0 – 3.3 V (In a 5V short condition, the signal can have a maximum of 5.25V on it with respect to the ground)
USB2_2_ID0	IO	VDD_USB2_18	USB mini-receptacle identifier or alternate test point for DC points probes inside USB 2.0 PHY Voltage range: 0 – 1.8 V
USB2_2_OVCUR	I	VDDIO_18	Port overcurrent
USB2_2_RT	IO	VDD_USB2_18	Transmitter resistor tune pin. It connects to an external resistor (200 ± 1% Ohms) that adjusts the USB 2.0 PHY's high-speed source impedance Voltage range: 0 – 1.8 V
USB2_2_VBUS0	A		USB 5V signal. This is the USB 5V supply. A charge pump external to the USB 2.0 PHY must provide power to this pin. The nominal voltage for this pin is 5V Voltage range: 0 – 5.25 V
USB2_2_XI	I	VDD_USB2_18	Crystal oscillator XI pin Voltage range: 0 – 1.8 V
USB2_2_XO	I	VDD_USB2_18	Crystal oscillator XO pin or board reference clock input. NOTE: When the reference clock source is a crystal, XO pin is a connection to a crystal. When the reference clock source is an aexternal board clock, XO is an input. For modeling and simulation purposes, XO is declared as a pure input Voltage range: 0 – 1.8 V
USB2_3_CTRL	O	VDDIO_18	Port power control

Pin Name	Type	Power Domain	Description
USB2_3_DM0	IO	VDD_USB2_3_33	USB D- signal. In normal operation it carries USB data to and from the USB 2.0 PHY. In <i>High-Speed (HS)</i> operation, this pin receives/transmits a maximum of 800 mV or 400 mV nominally. In <i>Full-Speed (FS)</i> or <i>Low-Speed (LS)</i> operation, this pin receives/transmits 3.3V nominally Voltage range: 0 – 3.3 V (In a 5V short condition, the signal can have a maximum of 5.25V on it with respect to the ground)
USB2_3_DP0	IO	VDD_USB2_3_33	USB D+ signal. In normal operation it carries USB data to and from the USB 2.0 PHY. In <i>High-Speed (HS)</i> operation, this pin receives/transmits a maximum of 800 mV or 400 mV nominally. In <i>Full-Speed (FS)</i> or <i>Low-Speed (LS)</i> operation, this pin receives/transmits 3.3V nominally Voltage range: 0 – 3.3 V (In a 5V short condition, the signal can have a maximum of 5.25V on it with respect to the ground)
USB2_3_ID0	IO	VDD_USB2_18	USB mini-receptacle identifier or alternate test point for DC points probes inside USB 2.0 PHY Voltage range: 0 – 1.8 V
USB2_3_OVCUR	I	VDDIO_18	Port overcurrent
USB2_3_RT	IO		Transmitter resistor tune pin. It connects to an external resistor (200 ± 1% Ohms) that adjusts the USB 2.0 PHY's high-speed source impedance Voltage range: 0 – 1.8 V
USB2_3_VBUS0	A		USB 5V signal. This is the USB 5V supply. A charge pump external to the USB 2.0 PHY must provide power to this pin. The nominal voltage for this pin is 5V Voltage range: 0 – 5.25 V
USB2_3_XI	I	VDD_USB2_18	Crystal oscillator XI pin Voltage range: 0 – 1.8 V
USB2_3_XO	I	VDD_USB2_18	Crystal oscillator XO pin or board reference clock input. NOTE: When the reference clock source is a crystal, XO pin is a connection to a crystal. When the reference clock source is an aexternal board clock, XO is an input. For modeling and simulation purposes, XO is declared as a pure input Voltage range: 0 – 1.8 V
USB2_4_CTRL	O	VDDIO_18	Port power control – USB 2.0 part
USB2_4_OVCUR	I	VDDIO_18	Port overcurrent – USB 2.0 part
USB2_5_CTRL	O	VDDIO_18	Port power control – USB 2.0 part
USB2_5_OVCUR	I	VDDIO_18	Port overcurrent – USB 2.0 part

Pin Name	Type	Power Domain	Description
USB3_0_CTRL	O	VDDIO_18	Port power control – USB 3.0 part
USB3_0_DM0	IO	VDD_USB3_33	USB 2.0 D- signal. This bidirectional pin carries USB 2.0 data to and from the USB 3.0 PHY. In HS operation, this pin receives/transmits a maximum of 800 mV or 400 mV nominally. In FS or LS operation, this pin receives/transmits 3.3V nominally Voltage range: 0 – 3.3 V
USB3_0_DP0	IO	VDD_USB3_33	USB 2.0 D+ signal. This bidirectional pin carries USB 2.0 data to and from the USB 3.0 PHY. In HS operation, this pin receives/transmits a maximum of 800 mV or 400 mV nominally. In FS or LS operation, this pin receives/transmits 3.3V nominally Voltage range: 0 – 3.3 V
USB3_0_ID0	IO		USB 2.0 mini-receptacle identifier Voltage range: 0 – 1.8 V
USB3_0_OVCUR	I	VDDIO_18	Port overcurrent – USB 3.0 part
USB3_0_REFCLKN	I	VDD_USB3VP_0_09	USB 3.0 optional reference clock input Voltage range: 0 – 0.9 V
USB3_0_REFCLKP	I	VDD_USB3VP_0_09	USB 3.0 optional reference clock input Voltage range: 0 – 0.9 V
USB3_0_RESREF	A		USB 3.0 external reference resistor. This pin is for a 200 Ohms ($\pm 1\%$) 100-ppm/C precision resistor-to-ground on the board Voltage range: 0 – 250 mV
USB3_0_RXON	I	VDD_USB3VP_0_09	USB 3.0 receive pin Voltage range: 0 – 0.9 V
USB3_0_RXOP	I	VDD_USB3VP_0_09	USB 3.0 receive pin Voltage range: 0 – 0.9 V
USB3_0_TXON	O	VDD_USB3TX_0_09	USB 3.0 transmit pin Voltage range: 0 – 0.9 V
USB3_0_TXOP	O	VDD_USB3TX_0_09	USB 3.0 transmit pin Voltage range: 0 – 0.9 V
USB3_0_VBUS0	A		USB 5V power supply pin. A charge pump external to the USB 3.0 PHY must provide power to this pin. The nominal voltage for this pin is 5V Voltage range: 0 – 5.25 V
USB3_1_CTRL	O	VDDIO_18	Port power control – USB 3.0 part
USB3_1_DM0	IO	VDD_USB3_33	USB 2.0 D- signal. This bidirectional pin carries USB 2.0 data to and from the USB 3.0 PHY. In HS operation, this pin receives/transmits a maximum of 800 mV or 400 mV nominally. In FS or LS operation, this pin receives/transmits 3.3V nominally Voltage range: 0 – 3.3 V

Pin Name	Type	Power Domain	Description
USB3_1_DP0	IO	VDD_USB3_33	USB 2.0 D+ signal. This bidirectional pin carries USB 2.0 data to and from the USB 3.0 PHY. In HS operation, this pin receives/transmits a maximum of 800 mV or 400 mV nominally. In FS or LS operation, this pin receives/transmits 3.3V nominally Voltage range: 0 – 3.3 V
USB3_1_ID0	IO		USB 2.0 mini-receptacle identifier Voltage range: 0 – 1.8 V
USB3_1_OVCUR	I	VDDIO_18	Port overcurrent – USB 3.0 part
USB3_1_REFCLKN	I	VDD_USB3VP_1_09	USB 3.0 optional reference clock input Voltage range: 0 – 0.9 V
USB3_1_REFCLKP	I	VDD_USB3VP_1_09	USB 3.0 optional reference clock input Voltage range: 0 – 0.9 V
USB3_1_RESREF	A		USB 3.0 external reference resistor. This pin is for a 200 Ohms ($\pm 1\%$) 100-ppm/C precision resistor-to-ground on the board Voltage range: 0 – 250 mV
USB3_1_RXON	I	VDD_USB3VP_1_09	USB 3.0 receive pin Voltage range: 0 – 0.9 V
USB3_1_RXOP	I	VDD_USB3VP_1_09	USB 3.0 receive pin Voltage range: 0 – 0.9 V
USB3_1_TXON	O	VDD_USB3TX_1_09	USB 3.0 transmit pin Voltage range: 0 – 0.9 V
USB3_1_TXOP	O	VDD_USB3TX_1_09	USB 3.0 transmit pin Voltage range: 0 – 0.9 V
USB3_1_VBUS0	A		USB 5V power supply pin. A charge pump external to the USB 3.0 PHY must provide power to this pin. The nominal voltage for this pin is 5V Voltage range: 0 – 5.25 V

5.1.2.4 SATA

Table 5-5 SATA Pins

Pin Name	Type	Power Domain	Description
SATA_P0ACTLED	O	VDDIO_18	P0 activity LED. It drives an external LED based on the port activity
SATA_P0CPDET	I	VDDIO_18	Cold presence detect P0. It detects addition or removal of the powered-down device
SATA_P0CPP0D	O	VDDIO_18	Cold presence power-on device P0. It enables power to the external device when asserted
SATA_P0MPSW	I	VDDIO_18	Mechanical presence switch P0. It indicates the state of the external device presence switch
SATA_P1ACTLED	O	VDDIO_18	P1 Activity LED. It drives an external LED based on the port activity

Pin Name	Type	Power Domain	Description
SATA_P1CPDET	I	VDDIO_18	Cold Presence Detect P1. It detects addition or removal of the powered-down device
SATA_P1CPPOD	O	VDDIO_18	Cold Presence Power-On Device P1. It enables power to the external device when asserted
SATA_P1MPSW	I	VDDIO_18	Mechanical Presence Switch P1. It indicates the state of the external device presence switch
SATA_REFCLKM	I	VDD_SATA_09	Reference clock differential pair Voltage range: 0 – 0.9 V
SATA_REFCLKP	I	VDD_SATA_09	Reference clock differential pair Voltage range: 0 – 0.9 V
SATA_RESREF	A		Reference resistor. This pin is for a 200 Ohms ($\pm 1\%$) 100-ppm/C precision resistor-to-ground on the board Voltage range: 0 – 250 mV
SATA_RXN[1:0]	I	VDD_SATA_09	Receive data differential pair port 0 or port 1 Voltage range: 0 – 0.9 V
SATA_RXP[1:0]	I	VDD_SATA_09	Receive data differential pair port 0 or port 1 Voltage range: 0 – 0.9 V
SATA_TXN[1:0]	O	VDD_SATATX_09	Transmit data differential pair port 0 or port 1 Voltage range: 0 – 0.9 V
SATA_TXP[1:0]	O	VDD_SATATX_09	Transmit data differential pair port 0 or port 1 Voltage range: 0 – 0.9 V

5.1.2.5 10 Gb Ethernet

Table 5-6 XGbE Pins

Pin Name	Type	Power Domain	Description
XG0_AMON	O	VDD_XG0_15	Analog monitor bump NOTE: Reserved in BE-M1000 manufactured since 2021 Voltage range: 0 – 1.575 V
XG0_DMON	O	VDD_XG0_09	Differential digital monitor bump NOTE: Reserved in BE-M1000 manufactured since 2021 Voltage range: 0 – 1.575 V
XG0_DMONB	O	VDD_XG0_09	Differential digital monitor bump NOTE: Reserved in BE-M1000 manufactured since 2021 Voltage range: 0 – 1.575 V
XG0_RBIAS	IO	VDD_XG0_15	Bias resistor bump. The pin connects to 1 kOhms $\pm 1\%$ precision resistor on board Voltage range: 0 – 1.575 V
XG0_REF_CLKN	I	VDD_XG0_15	Differential reference clocks from pads
XG0_REF_CLKP	I	VDD_XG0_15	Differential reference clocks from pads

Pin Name	Type	Power Domain	Description
XG0_RXN[3:0]	I	VDD_XG0_15	Receive data differential pair This lane is used for 10GBASE-KR
XG0_RXP[3:0]	I	VDD_XG0_15	Receive data differential pair This lane is used for 10GBASE-KR
XG0_TXN[3:0]	O	VDD_XG0_15	Transmit data differential pair This lane is used for 10GBASE-KR
XG0_TXP[3:0]	O	VDD_XG0_15	Transmit data differential pair This lane is used for 10GBASE-KR
XG1_AMON	O	VDD_XG1_15	Analog monitor bump NOTE: Reserved in BE-M1000 manufactured since 2021 Voltage range: 0 – 1.575 V
XG1_DMON	O	VDD_XG1_09	Differential digital monitor bump NOTE: Reserved in BE-M1000 manufactured since 2021 Voltage range: 0 – 1.575 V
XG1_DMONB	O	VDD_XG1_09	Differential digital monitor bump NOTE: Reserved in BE-M1000 manufactured since 2021 Voltage range: 0 – 1.575 V
XG1_RBIAS	IO	VDD_XG1_15	Bias resistor bump. The pin connects to 1 kOhms ± 1% precision resistor on board Voltage range: 0 – 1.575 V
XG1_REF_CLKN	I	VDD_XG1_15	Differential reference clocks from pads
XG1_REF_CLKP	I	VDD_XG1_15	Differential reference clocks from pads
XG1_RXN[3:0]	I	VDD_XG1_15	Receive data differential pair This lane is used for 10GBASE-KR
XG1_RXP[3:0]	I	VDD_XG1_15	Receive data differential pair This lane is used for 10GBASE-KR
XG1_TXN[3:0]	O	VDD_XG1_15	Transmit data differential pair This lane is used for 10GBASE-KR
XG1_TXP[3:0]	O	VDD_XG1_15	Transmit data differential pair This lane is used for 10GBASE-KR

5.1.2.6 1 Gb Ethernet

Table 5-7 GMAC Pins

Pin Name	Type	Power Domain	Description
G0_GP_IN	I	VDDIO_18	General purpose input
G0_GP_OUT	O	VDDIO_18	General purpose output
G0_MDC	O	VDDIO_18	Management data clock. The maximum frequency of this clock is 2.5 MHz. This clock is generated from the application clock through a clock divider
G0_MDIO	IO	VDDIO_18	Management Data Input/Output (MDIO)

Pin Name	Type	Power Domain	Description
G0_RX_CLK	I	VDDIO_18	Receive reference clock (125 MHz in 1 Gbps, 25 MHz in 100 Mbps, 2.5 MHz in 10 Mbps mode)
G0_RX_DAT[3:0]	I	VDDIO_18	Receive data
G0_RX_DEN	I	VDDIO_18	Receive data
G0_TX_CLK	O	VDDIO_18	Transmit reference clock (125 MHz in 1 Gbps, 25 MHz in 100 Mbps, 2.5 MHz in 10 Mbps mode)
G0_TX_DAT[3:0]	O	VDDIO_18	Transmit data
G0_TX_DEN	O	VDDIO_18	Transmit data enable
G1_GP_IN	I	VDDIO_18	General purpose input
G1_GP_OUT	O	VDDIO_18	General purpose output
G1_MDC	O	VDDIO_18	Management data clock. The maximum frequency of this clock is 2.5 MHz. This clock is generated from the application clock through a clock divider
G1_MDIO	IO	VDDIO_18	<i>Management Data Input/Output (MDIO)</i>
G1_RX_CLK	I	VDDIO_18	Receive reference clock (125 MHz in 1 Gbps, 25 MHz in 100 Mbps, 2.5 MHz in 10 Mbps mode)
G1_RX_DAT[3:0]	I	VDDIO_18	Receive data
G1_RX_DEN	I	VDDIO_18	Receive data
G1_TX_CLK	O	VDDIO_18	Transmit reference clock (125 MHz in 1 Gbps, 25 MHz in 100 Mbps, 2.5 MHz in 10 Mbps mode)
G1_TX_DAT[3:0]	O	VDDIO_18	Transmit data
G1_TX_DEN	O	VDDIO_18	Transmit data enable

5.1.2.7 eMMC/SD

Table 5-8 eMMC/SD Pins

Pin Name	Type	Power Domain	Description
SD_CAP0	A		Connected to 1 uF capacitor for stabilizing LDO output voltage
SD_CAP1	A		Connected to 1 uF capacitor for stabilizing LDO output voltage
SD_CARD_DETECT_N	I	VDDIO_18	Card detect signal, active low. When this is 0, it represents card is connected. When this signal goes from 0 to 1 card insertion interrupt is generated if enabled NOTE: This signal should be connected to ground if an eMMC device is connected to BE-M1000. As eMMC device is non-removable, card detection is not required.
SD_CLK	O	VDD_SD_33	SD card transmit/receive clock

Pin Name	Type	Power Domain	Description
SD_CMD	IO	VDD_SD_33	SD card command
SD_DAT[7:0]	IO	VDD_SD_33	SD card data NOTE: Input data line must be pulled high, even if it is not used
SD_LED_CTRL	O	VDDIO_18	SD card LED control. It warns user not to remove card while it is being accessed
SD_REG_VOL_STABLE	I	VDDIO_18	Check whether host regulator voltage is stable, active high
SD_RST_N	O	VDD_SD_33	eMMC device reset, active low
SD_VDD_ON	O	VDDIO_18	Switch on VDD1/VDD bus power for SD/eMMC card
SD_VDD_SEL[0]	O	VDDIO_18	Select 1.8V voltage level for SD card
SD_VDD_SEL[1]	O	VDDIO_18	Select 3V voltage level for SD card
SD_VDD_SEL[2]	O	VDDIO_18	Select 3.3V voltage level for SD card
SD_WRITE_PROT	I	VDDIO_18	Card write protect, active high. When this is 1, it represents card is write protected NOTE: This signal should be connected to ground if an eMMC device is connected to BE-M1000. As eMMC device does not have write protect physical switch similar to SD card, this signal is not required

5.1.3 Low Speed Peripherals

5.1.3.1 GPIO*32

Table 5-9 GPIO*32 Pins

Pin Name	Type	Power Domain	Description
GPIO32[31:0]	IO	VDDIO_18	GPIO data

5.1.3.2 UART

Table 5-10 UART Pins

Pin Name	Type	Power Domain	Description
UART1_RXD	I	VDDIO_18	Receive data
UART1_TXD	O	VDDIO_18	Transmit data
UART2_RXD	I	VDDIO_18	Receive data
UART2_TXD	O	VDDIO_18	Transmit data

5.1.3.3 SPI

Table 5-11 SPI Pins

Pin Name	Type	Power Domain	Description
SPI1_CLK	O	VDDIO_18	Output clock
SPI1_RXD	I	VDDIO_18	Receive data

Pin Name	Type	Power Domain	Description
SPI1_SS_N[3:0]	O	VDDIO_18	Slave select
SPI1_TXD	O	VDDIO_18	Transmit data

5.1.3.4 eSPI

Table 5-12 eSPI Pins

Pin Name	Type	Power Domain	Description
ESPI_ALERT[7:0]	I	VDDIO_18	eSPI alert
ESPI_CLK	IO	VDDIO_18	eSPI clock
ESPI_DAT[3:0]	IO	VDDIO_18	eSPI data
ESPI_RST	IO	VDDIO_18	eSPI reset
ESPI_SS_N[7:0]	IO	VDDIO_18	eSPI slave select

5.1.3.5 I²C

Table 5-13 I²C Bus Pins

Pin Name	Type	Power Domain	Description
I2C1_SCL	IO	VDDIO_18	I ² C #1 clock
I2C1_SDA	IO	VDDIO_18	I ² C #1 data
I2C2_SCL	IO	VDDIO_18	I ² C #2 clock
I2C2_SDA	IO	VDDIO_18	I ² C #2 data

5.1.3.6 SMBus

Table 5-14 SMBus Pins

Pin Name	Type	Power Domain	Description
SMB1_CLK	IO	VDDIO_18	SMBus #1 clock
SMB1_DAT	IO	VDDIO_18	SMBus #1 data
SMB2_CLK	IO	VDDIO_18	SMBus #2 clock
SMB2_DAT	IO	VDDIO_18	SMBus #2 data

5.1.4 Audio & Video

5.1.4.1 LVDS

Table 5-15 LVDS Pins

Pin Name	Type	Power Domain	Description
LED_PWM	O	VDDIO_18	Brightness control
LVDS_L0_CLKN	O	VDDIO_18	LVDS clock
LVDS_L0_CLKP	O	VDDIO_18	LVDS clock
LVDS_L0_DATN[3:0]	O	VDDIO_18	LVDS data

Pin Name	Type	Power Domain	Description
LVDS_L0_DATP[3:0]	O	VDDIO_18	LVDS data
LVDS_L1_CLKN	O	VDDIO_18	LVDS clock
LVDS_L1_CLKP	O	VDDIO_18	LVDS clock
LVDS_L1_DATN[3:0]	O	VDDIO_18	LVDS data
LVDS_L1_DATP[3:0]	O	VDDIO_18	LVDS data
LVDS_L2_CLKN	O	VDDIO_18	LVDS clock
LVDS_L2_CLKP	O	VDDIO_18	LVDS clock
LVDS_L2_DATN[3:0]	O	VDDIO_18	LVDS data
LVDS_L2_DATP[3:0]	O	VDDIO_18	LVDS data
LVDS_L3_CLKN	O	VDDIO_18	LVDS clock
LVDS_L3_CLKP	O	VDDIO_18	LVDS clock
LVDS_L3_DATN[3:0]	O	VDDIO_18	LVDS data
LVDS_L3_DATP[3:0]	O	VDDIO_18	LVDS data
LVDS_PLL_27M	I	VDDIO_18	PLL reference clock 27 MHz IN – LVDS
LVDS_VREF	A		Signal reference

5.1.4.2 HDMI

Table 5-16 HDMI Pins

Pin Name	Type	Power Domain	Description
HDMI_CLKN	O		Negative TMDS differential line driver clock output Voltage range: For the permitted voltage range, refer to <i>High-Definition Multimedia Interface Specification</i> , Version 2.0, “Electrical Specification” section
HDMI_CLKP	O		Positive TMDS differential line driver clock output Voltage range: For the permitted voltage range, refer to <i>High-Definition Multimedia Interface Specification</i> , Version 2.0, “Electrical Specification” section
HDMI_DATN[2:0]	O		TMDS data Voltage range: For the permitted voltage range, refer to <i>High-Definition Multimedia Interface Specification</i> , Version 2.0, “Electrical Specification” section
HDMI_DATP[2:0]	O		TMDS data Voltage range: For the permitted voltage range, refer to <i>High-Definition Multimedia Interface Specification</i> , Version 2.0, “Electrical Specification” section
HDMI_DB_BISTDONE	O	VDDIO_18	Indication of <i>Built-In Self Test (BIST)</i> test completion

Pin Name	Type	Power Domain	Description
HDMI_DB_BISTEN	I	VDDIO_18	Control enable signal for BIST test
HDMI_DB_BISTOK	O	VDDIO_18	Indication of BIST test pass
HDMI_DB_DAT[9:0]	O	VDDIO_18	Indication that path between I/O pad and <i>analog front end (AFE)</i> is valid NOTE: Reserved in BE-M1000 manufactured since 2021
HDMI_DB_EN	I	VDDIO_18	Control enable signal for I/O continuity test NOTE: Reserved in BE-M1000 manufactured since 2021
HDMI_DB_ENHPDRXSENSE	I	VDDIO_18	Enables hot plug detect and RXSENSE for HDMI operation
HDMI_DB_EXTERNAL	I	VDDIO_18	HDMI PHY debug interface
HDMI_DB_PDDQ	I	VDDIO_18	Shuts off low-to-high bias voltage generators in the MPLL and support blocks, because the generators are not under direct power-down control
HDMI_DB_PHY_RESET	I	VDDIO_18	PHY reset. This signal places the digital section of the macro into a reset state
HDMI_DB_PHYDTB0	O	VDDIO_18	Digital test bus NOTE: Reserved in BE-M1000 manufactured since 2021
HDMI_DB_PHYDTB1	O	VDDIO_18	Digital test bus NOTE: Reserved in BE-M1000 manufactured since 2021
HDMI_DB_RXSENSE	O	VDDIO_18	Rx presence detection signal for all TMDS data lanes for HDMI mode of operation. Asserted high if TMDS lines have a 3.3V pull-up resistor connected to them
HDMI_DB_SNK_DET_I	O	VDDIO_18	Sink detected signal for HDMI NOTE: Reserved in BE-M1000 manufactured since 2021
HDMI_DB_SVSRET_MODEZ	I	VDDIO_18	Enables retention mode
HDMI_DB_TX_PWRON	I	VDDIO_18	Power-on input. This signal is used to power up the entire macro. All analog blocks are released from power-down mode
HDMI_DB_TX_READY	O	VDDIO_18	Indicates that the HDMI PHY is ready to transmit data
HDMI_DDCCEC	IO		Ground reference for the hot plug detect signal
HDMI_HPD	IO		Hot plug detect signal for HDMI
HDMI_PLL_27M	I	VDDIO_18	PLL reference clock 27 MHz IN – HDMI
HDMI_RESREF	A		Reference resistor connection. This pin is for a $1.62 \pm 1\%$ kOhms reference resistor (connected to ground)
HDMI_SCL	IO	VDDIO_18	HDMI I ² C clock input
HDMI_SDA	IO	VDDIO_18	HDMI I ² C data input

5.1.4.3 HDA

Table 5-17 HDA Pins

Pin Name	Type	Power Domain	Description
HDA_BCLK	O	VDDIO_18	Codec link 24 MHz frequency NOTE: Reserved in BE-M1000 manufactured before 2021
HDA_RST_N	O	VDDIO_18	Codec reset, active low NOTE: Reserved in BE-M1000 manufactured before 2021
HDA_SDI[1:0]	IO	VDDIO_18	Codec serial data input NOTE: Reserved in BE-M1000 manufactured before 2021
HDA_SDO[1:0]	IO	VDDIO_18	Codec serial data output NOTE: Reserved in BE-M1000 manufactured before 2021
HDA_SYNC	O	VDDIO_18	Codec 48 kHz frame synchronization NOTE: Reserved in BE-M1000 manufactured before 2021

5.1.4.4 I²S

Table 5-18 I²S Pins

Pin Name	Type	Power Domain	Description
I2S_SCK	I	VDDIO_18	I ² S continuous serial clock
I2S_SDI	I	VDDIO_18	I ² S serial data input
I2S_SDO	O	VDDIO_18	I ² S serial data output
I2S_WS	I	VDDIO_18	I ² S word select

5.1.5 System Control

Table 5-19 System Control Pins

Pin Name	Type	Power Domain	Description
ARC_DBG_TF	O	VDDIO_18	Indicates that a triple fault exception has occurred
ARC_WDT_RESET	O	VDDIO_18	Watchdog reset
CLK24M_OUT	O	VDDIO_18	Output clock 48 MHz/2, In some USB purposes
CLK25M	I	VDDIO_18	PLL Reference Clock 25 MHz
GPIO8[7:0]	IO	VDDIO_18	SM GPIO Data
I2C0_SCL	IO	VDDIO_18	SM I ² C clock
I2C0_SDA	IO	VDDIO_18	SM I ² C data
RESET_N	I	VDDIO_18	System reset, active low
SMB0_CLK	IO	VDDIO_18	SM SMBus clock
SMB0_DAT	IO	VDDIO_18	SM SMBus data

Pin Name	Type	Power Domain	Description
SPI0_CLK	O	VDDIO_18	Output clock
SPI0_RXD	I	VDDIO_18	Receive data
SPI0_SS_N[3:0]	O	VDDIO_18	Slave select
SPI0_TXD	O	VDDIO_18	Transmit data
TEST_0	I	VDDIO_18	Test point 0 NOTE: Reserved in BE-M1000 manufactured since 2021
TURBO_BOOT	I	VDDIO_18	Controls boot mode of the System Control Processor: 0 – 500 MHz (TURBO): 1 – 250 MHz
TRSTN	I	VDDIO_18	Test reset
UART0_RXD	I	VDDIO_18	Receive data
UART0_TXD	O	VDDIO_18	Transmit data

5.1.6 System Debug

Table 5-20 System Debug Pins

Pin Name	Type	Power Domain	Description
CS_CLK	O	VDDIO_18	Trace port clock
CS_CTRL	O	VDDIO_18	Trace port control
CS_DAT[15:0]	O	VDDIO_18	Trace port data
CS_SWCLK_TCK	I	VDDIO_18	Serial wire and TAP clock
CS_SWDIO_TMS	IO	VDDIO_18	Combined serial wire input/output
CS_TDI	I	VDDIO_18	JTAG TAP data IN
CS_TDO	O	VDDIO_18	JTAG TAP data OUT
CS_TRST_N	I	VDDIO_18	TAP Asynchronous reset

5.1.7 Power and Ground

5.1.7.1 Core Supply

Table 5-21 Core Supply Pins

Pin Name	Type	Description
VDD	P	Core power

5.1.7.2 0.95V Voltage Supply

Table 5-22 0.95V Voltage Supply Pins

Pin Name	Type	Description
VDD_HDMI_09	P	0.9V analog power supply
VDD_PCIE4_0_09	P	PCIe PHY analog 0.95V
VDD_PCIE4_1_09	P	PCIe PHY analog 0.95V

Pin Name	Type	Description
VDD_PCIE8_09	P	PCIe PHY analog 0.95V
VDD_SATA_09	P	SATA PHY analog and digital supply
VDD_SATATX_09	P	SATA PHY transmit supply
VDD_USB2_09	P	Digital Power Supply
VDD_USB3_0_09	P	0.9 V PHY analog and digital high-speed supply
VDD_USB3_1_09	P	0.9 V PHY analog and digital high-speed supply
VDD_USB3TX_0_09	P	0.9 V PHY transmit supply
VDD_USB3TX_1_09	P	0.9 V PHY transmit supply
VDD_USB3VP_0_09	P	0.9 V PHY analog and digital SuperSpeed supply
VDD_USB3VP_1_09	P	0.9 V PHY analog and digital SuperSpeed supply
VDD_XG0_09	P	XGbE PHY analog 0.95V
VDD_XG1_09	P	XGbE PHY analog 0.95V

5.1.7.3 PLL Supply

Table 5-23 PLL Supply Pins

Pin Name	Type	Description
VDDPLL_0_09	P	PLL power
VDDPLL_1_09	P	PLL power
VDDPLL_2_09	P	PLL power
VDDPLL_3_09	P	PLL power
VDDPLL_HDMI_09	P	HDMI PLL power

5.1.7.4 DDR Supply

Table 5-24 DDR Supply Pins

Pin Name	Type	Description
VDDQ_DDR0	P	VDDQ voltage supply
VDDQ_DDR1	P	VDDQ voltage supply

5.1.7.5 1.5V Voltage Supply

Table 5-25 1.5V Voltage Supply Pins

Pin Name	Type	Description
VDD_PCIE4_0_15	P	PCIe PHY IO 1.5V
VDD_PCIE4_1_15	P	PCIe PHY IO 1.5V
VDD_PCIE8_15	P	PCIe PHY IO 1.5V
VDD_XG0_15	P	XGbE PHY IO 1.5V
VDD_XG1_15	P	XGbE PHY IO 1.5V

5.1.7.6 1.8V Voltage Supply
Table 5-26 1.8V Voltage Supply Pins

Pin Name	Type	Description
VDD_DDR0_PLL	P	PLL power supply
VDD_DDR1_PLL	P	PLL power supply
VDD_HDMI_18	P	1.8V analog power supply
VDD_PVT_18	P	PVT sensor power
VDD_SATA_18	P	SATA PHY High-voltage power supply
VDD_USB2_18	P	1.8V Analog Power Supply
VDDIO_18	P	IO power
VDDIO_18	P	Output driver power, 1.8V

5.1.7.7 3.3V Voltage Supply
Table 5-27 3.3V Voltage Supply Pins

Pin Name	Type	Description
VDD_SD_33	P	3.3V SD Supply
VDD_USB2_0_33	P	3.3V Analog Power Supply
VDD_USB2_1_33	P	3.3V Analog Power Supply
VDD_USB2_2_33	P	3.3V Analog Power Supply
VDD_USB2_3_33	P	3.3V Analog Power Supply
VDD_USB3_33	P	3.3V High supply for HS operation & SS operation

5.1.7.8 Ground
Table 5-28 Ground Pins

Pin Name	Type	Description
VSS	G	Core ground supply
VSSIO	G	IO ground
VSSPLL_0	G	PLL ground
VSSPLL_1	G	PLL ground
VSSPLL_2	G	PLL ground
VSSPLL_3	G	PLL ground
VSSPLL_HDMI	G	HDMI PLL ground

5.1.8 Requirements for Unused Pins

The following table shows the requirements for unused pins of the BE-M1000. Please follow these requirements if you are not going to use any interface from [Pinout List](#).

Table 5-29 Requirements for Unused Pins

Type	Requirements
Input pins	Tie to ground potential If active low level, tie to power supply
Output pins	Leave floating
Power pins	Always use
Reserved pins	Leave floating

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5.2 Pin Map Overview

The diagrams below show pinout from the top view of the package.

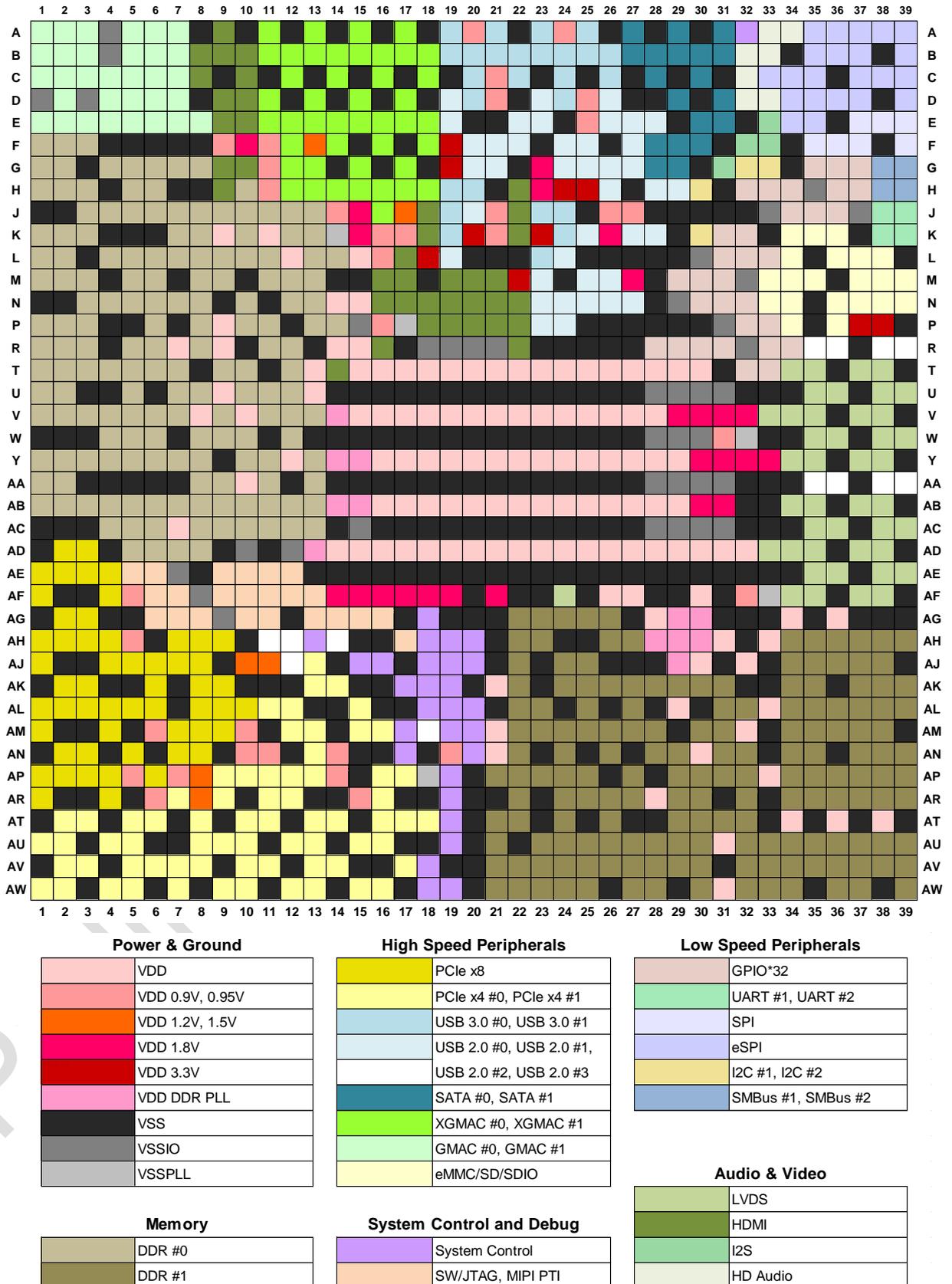


Figure 5-1 BE-M1000 Pin Map

5.2.1 Power and Ground

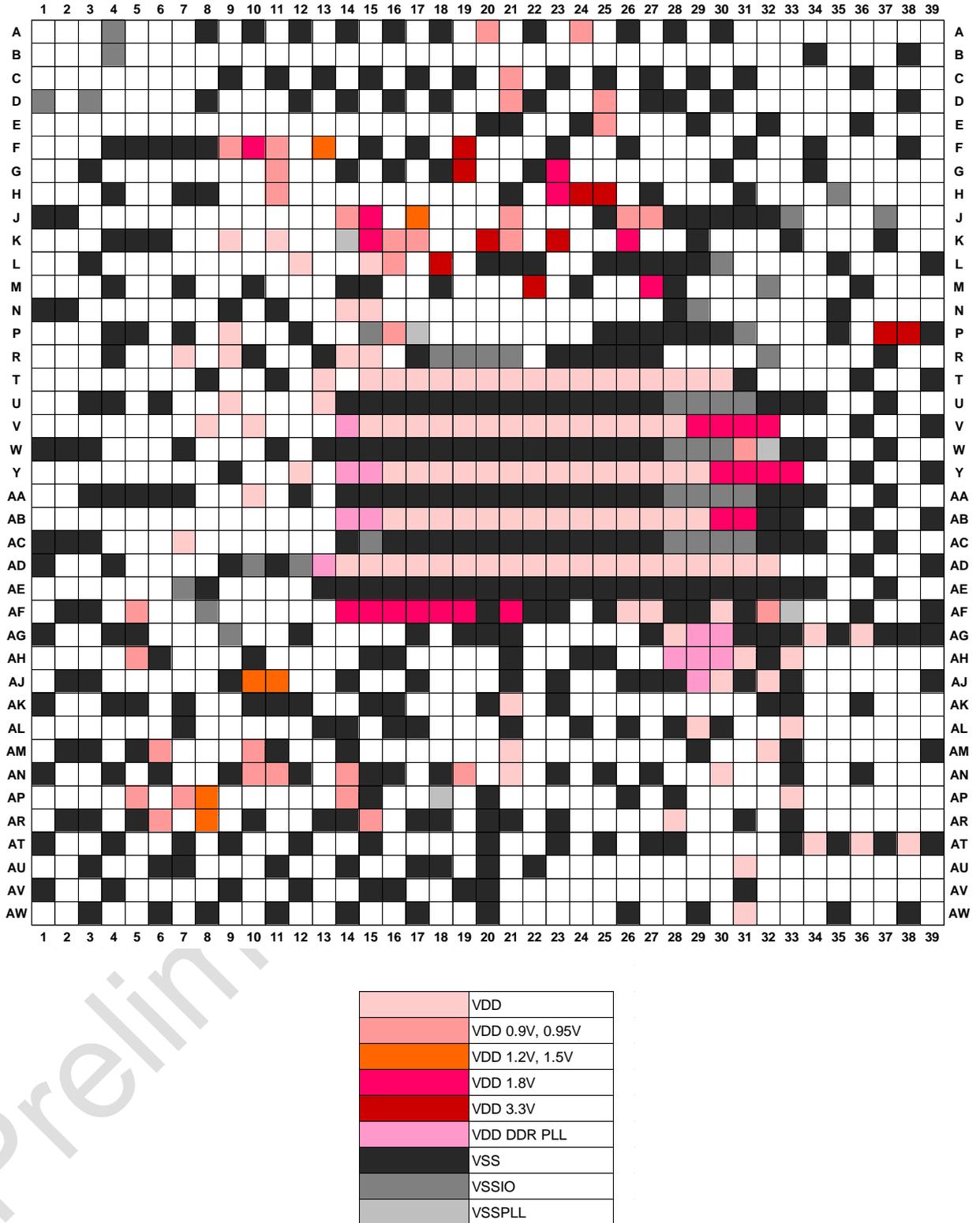
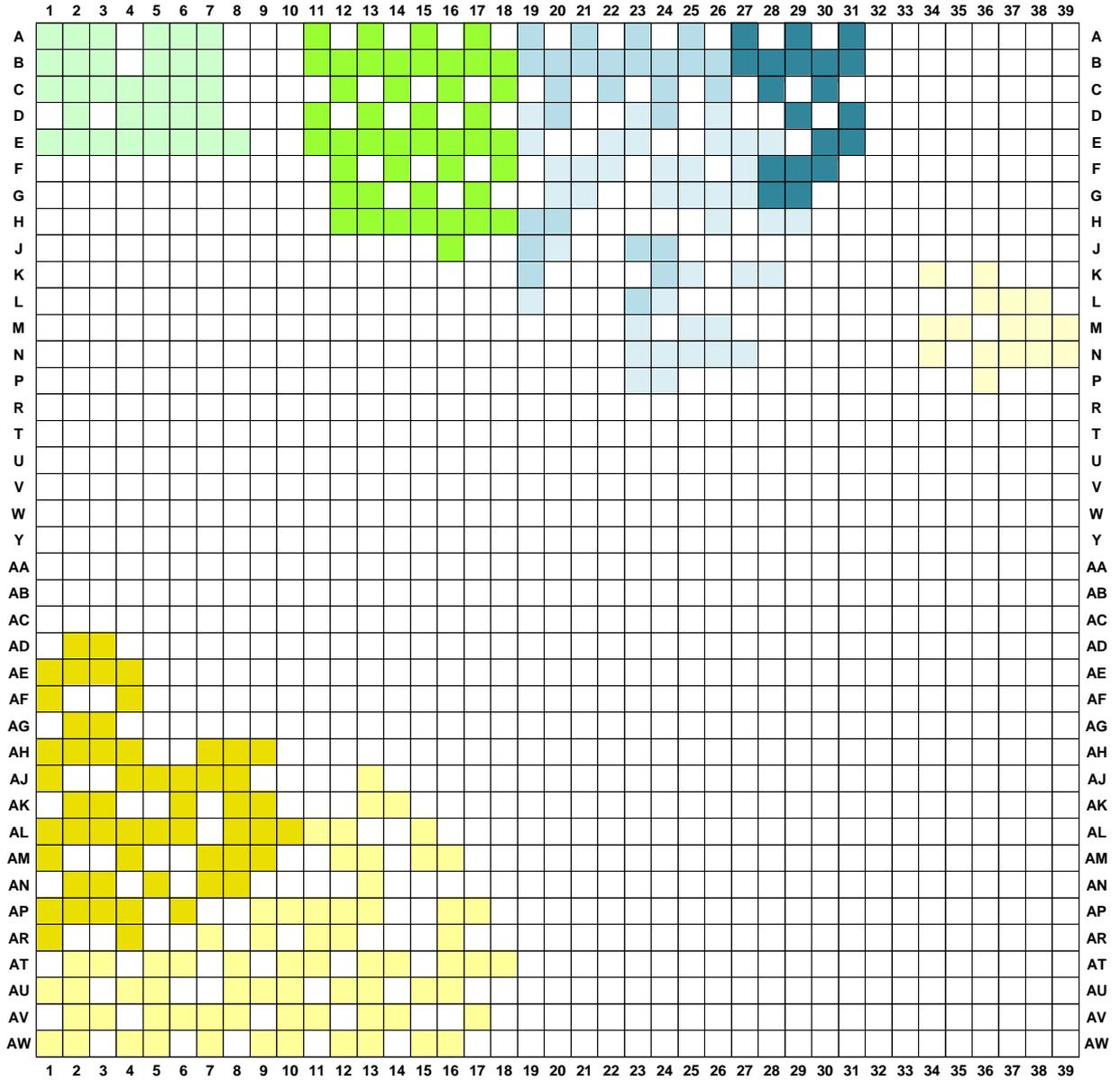


Figure 5-2 Power and Ground Pin Placement

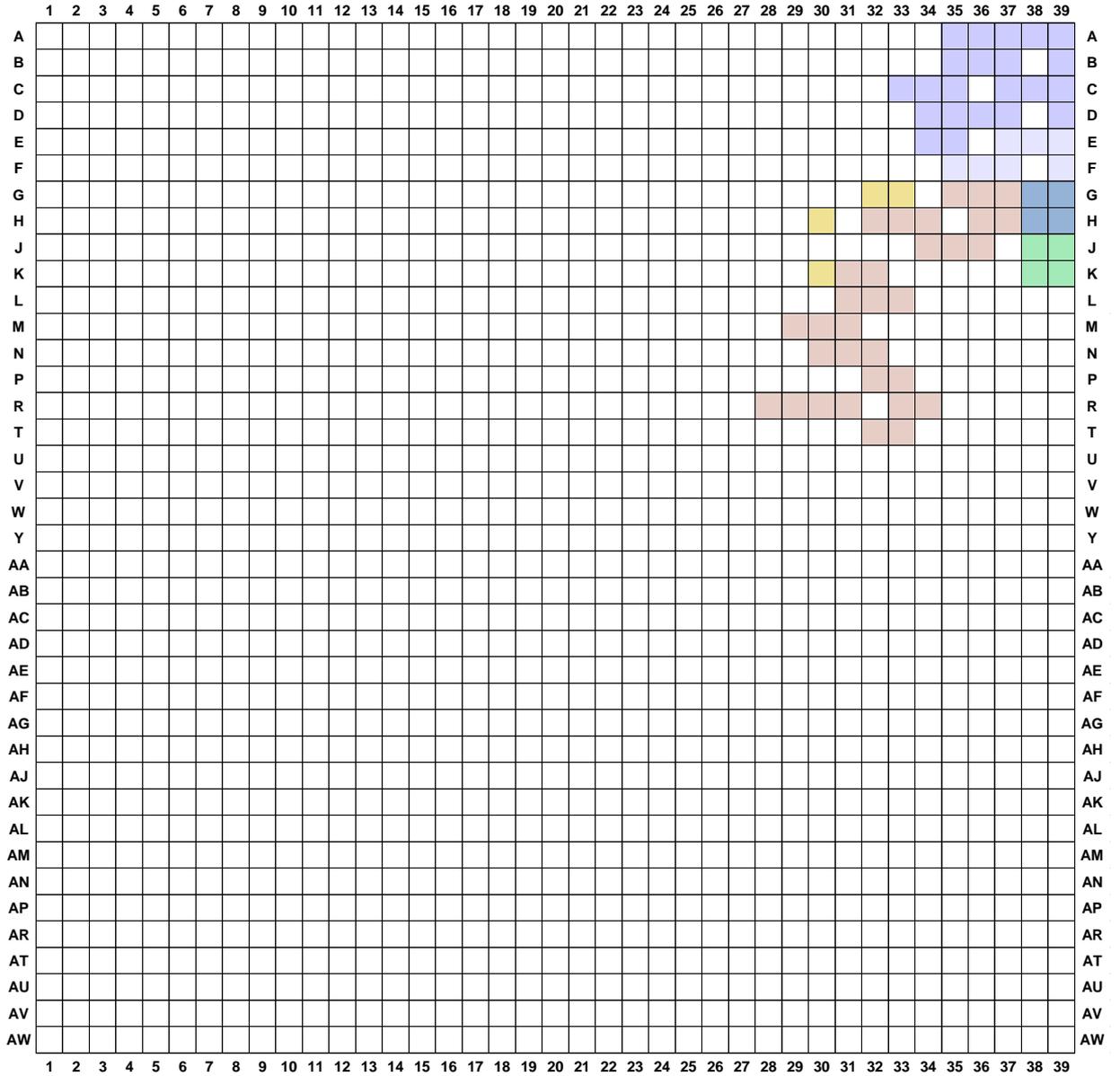
5.2.2 High Speed Peripherals



	PCIe x8
	PCIe x4 #0, PCIe x4 #1
	USB 3.0 #0, USB 3.0 #1
	USB 2.0 #0, USB 2.0 #1, USB 2.0 #2, USB 2.0 #3
	SATA #0, SATA #1
	XGMAC #0, XGMAC #1
	GMAC #0, GMAC #1
	eMMC/SD/SDIO

Figure 5-3 High Speed Peripherals Pin Placement

5.2.3 Low Speed Peripherals



	GPIO*32
	UART #1, UART #2
	SPI
	eSPI
	I2C #1, I2C #2
	SMBus #1, SMBus #2

Figure 5-4 Low Speed Peripherals Pin Placement

5.2.4 Memory

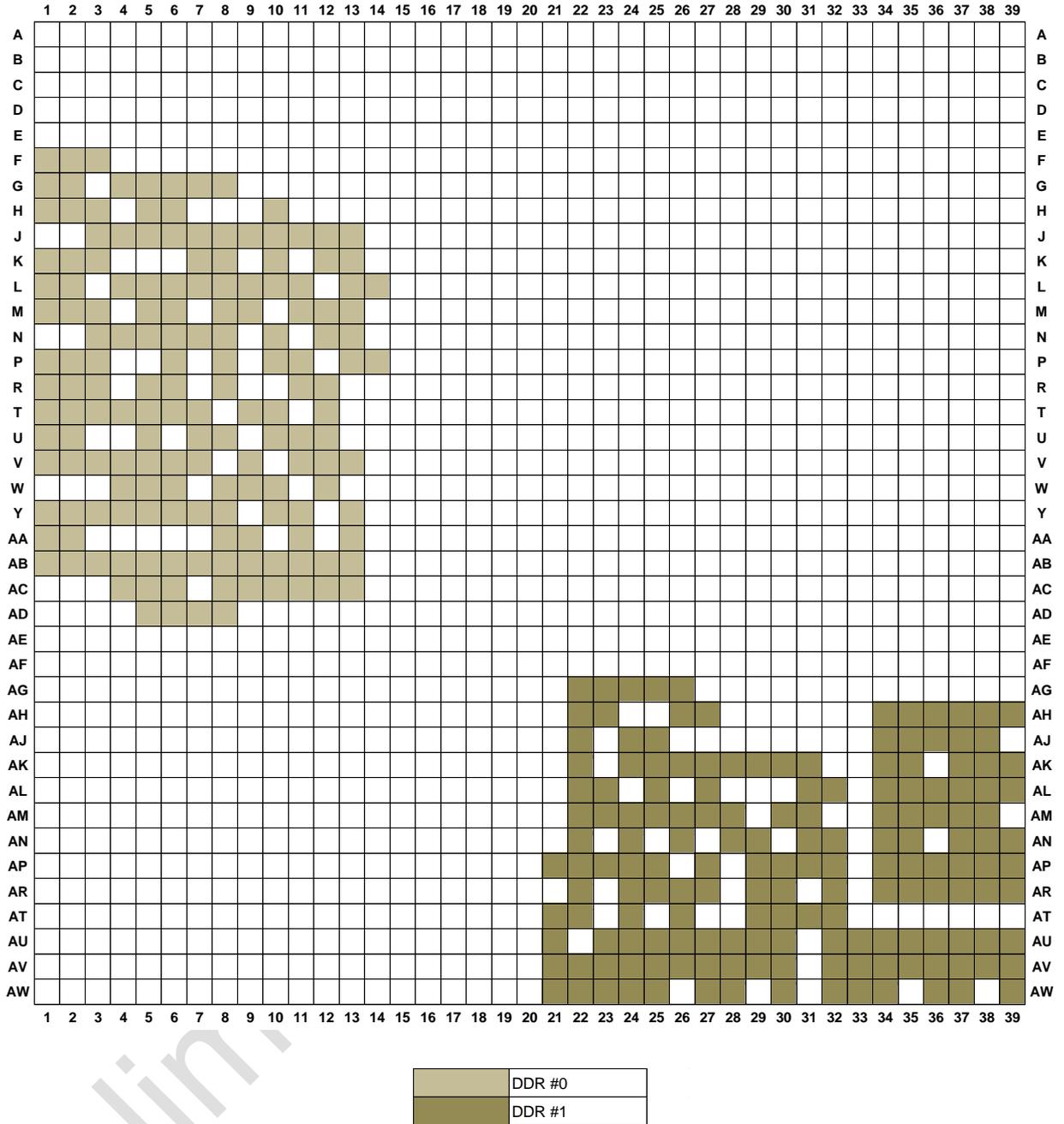


Figure 5-5 Memory Pin Placement

5.2.5 Audio and Video

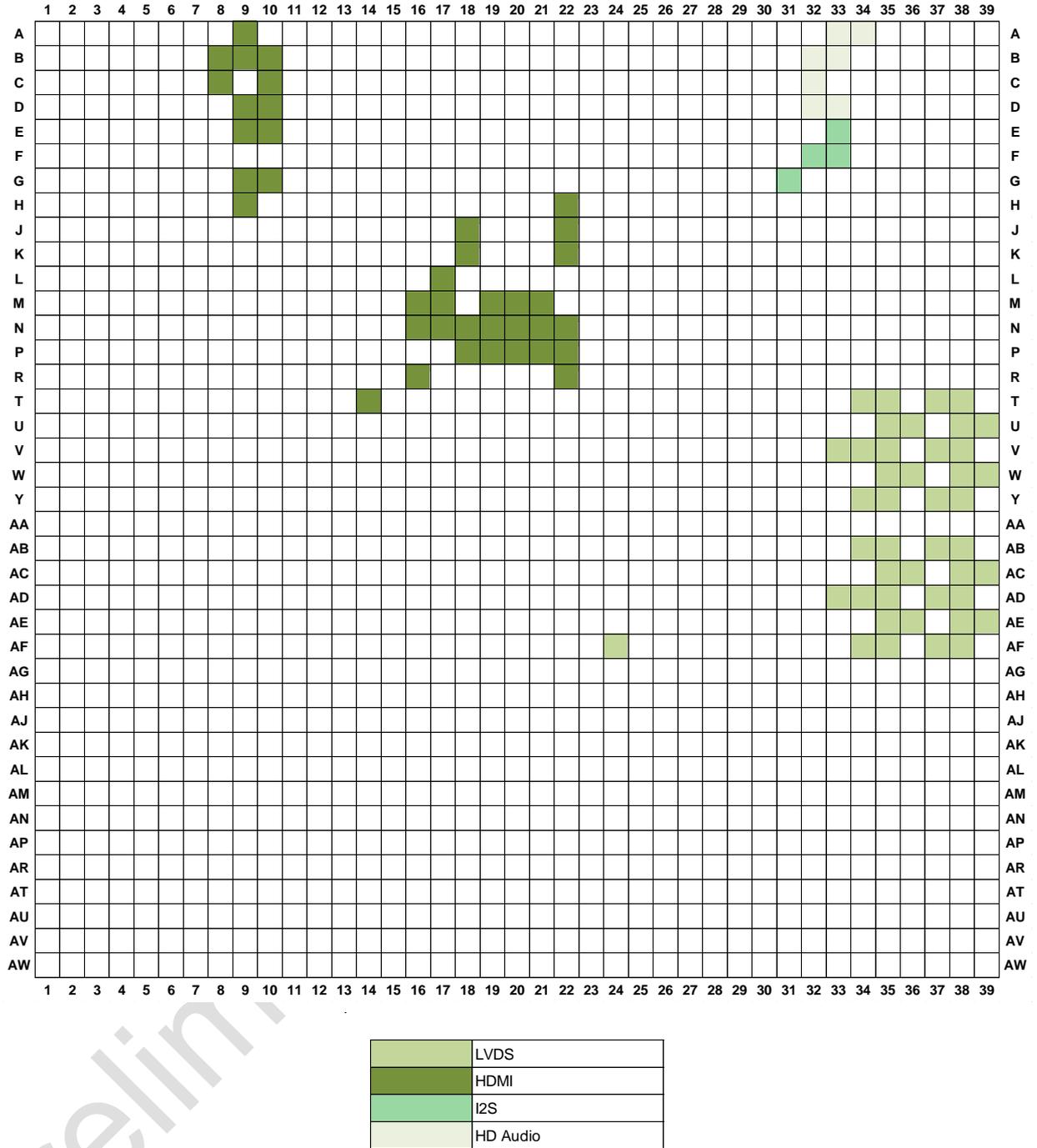


Figure 5-6 Audio and Video Pin Placement

5.2.6 System Control and Debug

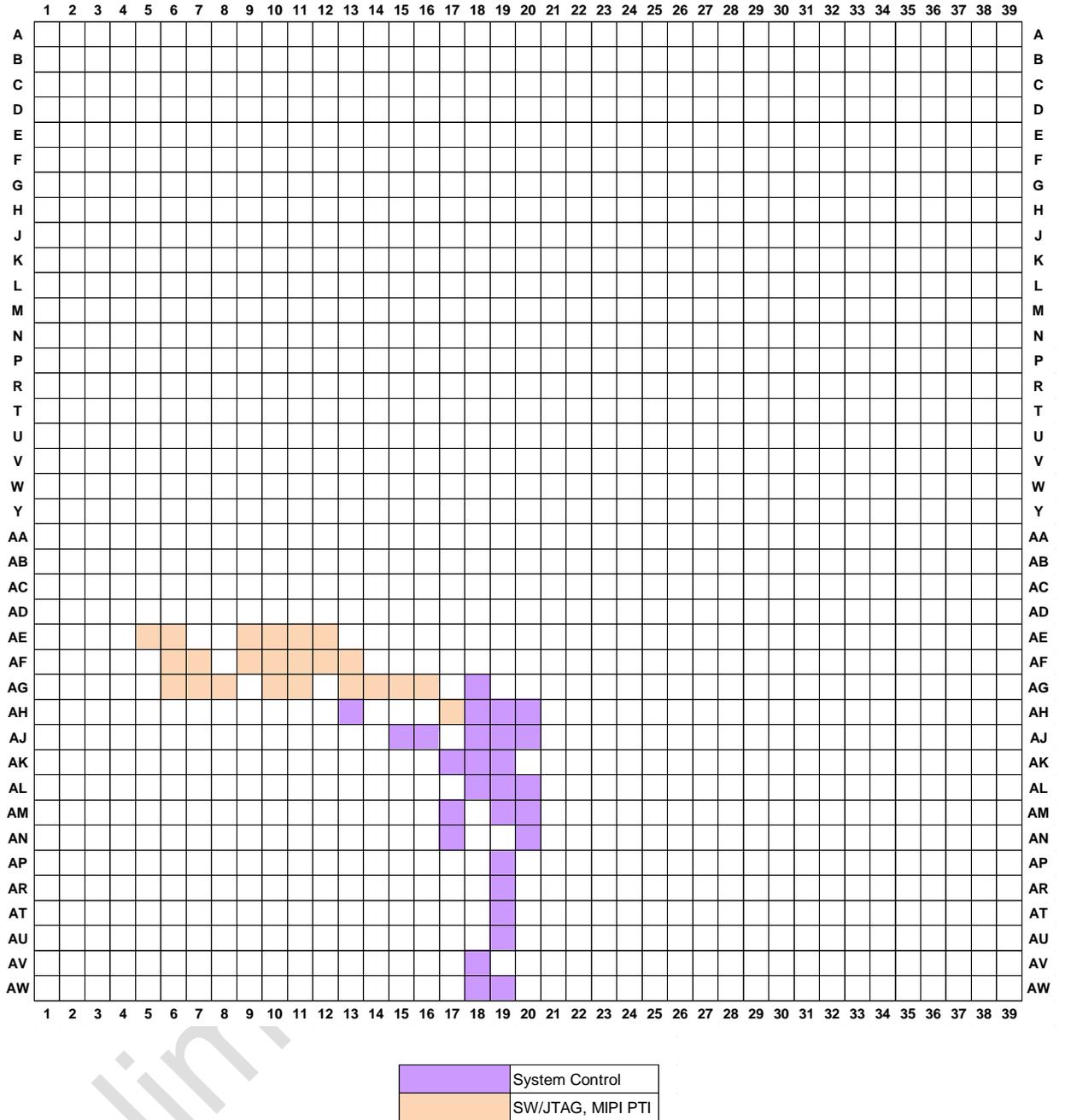


Figure 5-7 System Control and Debug Pin Placement

6 Package Information

6.1 Marking

The following table describes the options of BE-M1000 marking.

Table 6-1 BE-M1000 Package Marking Options

	Marking	Arm Logo
1	WW.YYYY	ARM
2	WW.YYYY	arm
3	BA.YYWW	arm
4	BN.YYWW	arm
5	BK.YYWW	arm

The following table shows designation of each field in the package marking of BE-M1000 #1 and #2 packages.

Table 6-2 BE-M1000 #1 and #2 Packages Marking

WW	.	YYYY
Week	Field Delimiter	Year

The following table shows designation of each field in the package marking of BE-M1000 #3 to #5 packages.

Table 6-3 BE-M1000 #3 to #5 Packages Marking

XX	.	YY	WW
Package Type	Field Delimiter	Year	Week

The following figures show the top view of the BE-M1000 microprocessors in different packages.



Figure 6-1 BE-M1000. Top View

6.2 FCBGA-1521 Package

The SoC is mounted into FCBGA-1521 package. Main package parameters are shown in the figures and table below.

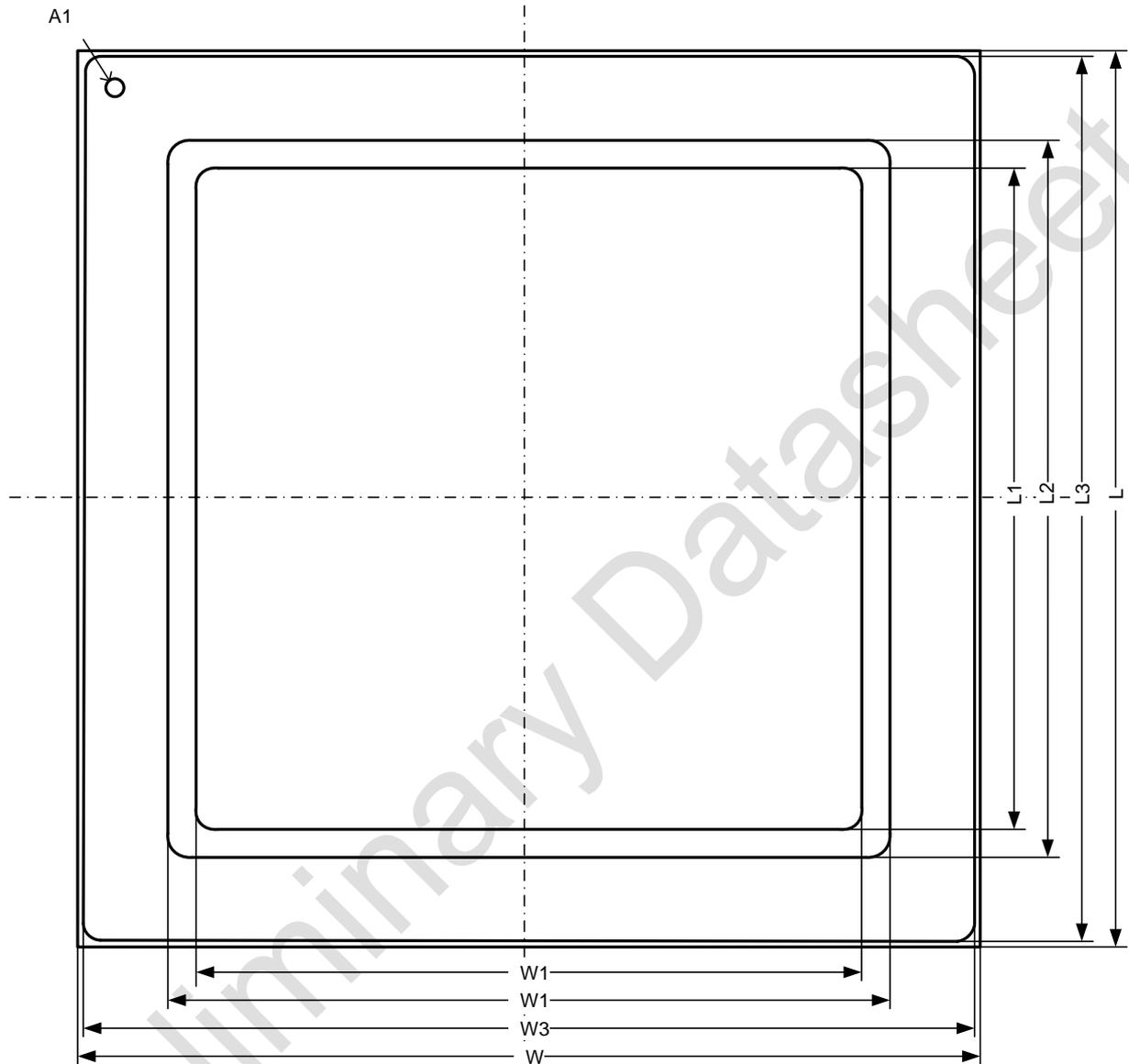


Figure 6-2 SoC Package. Top View

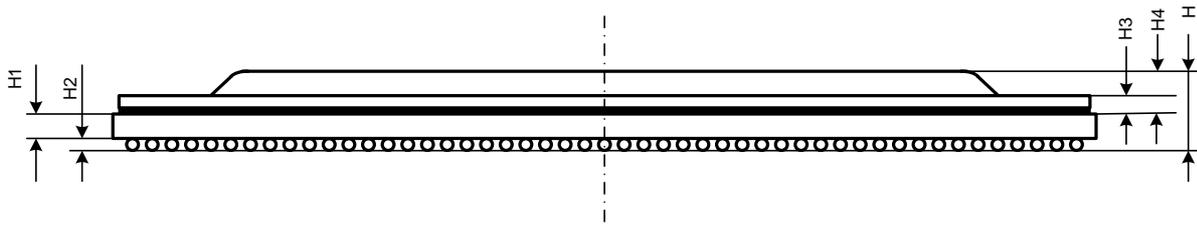


Figure 6-3 SoC Package. Side View

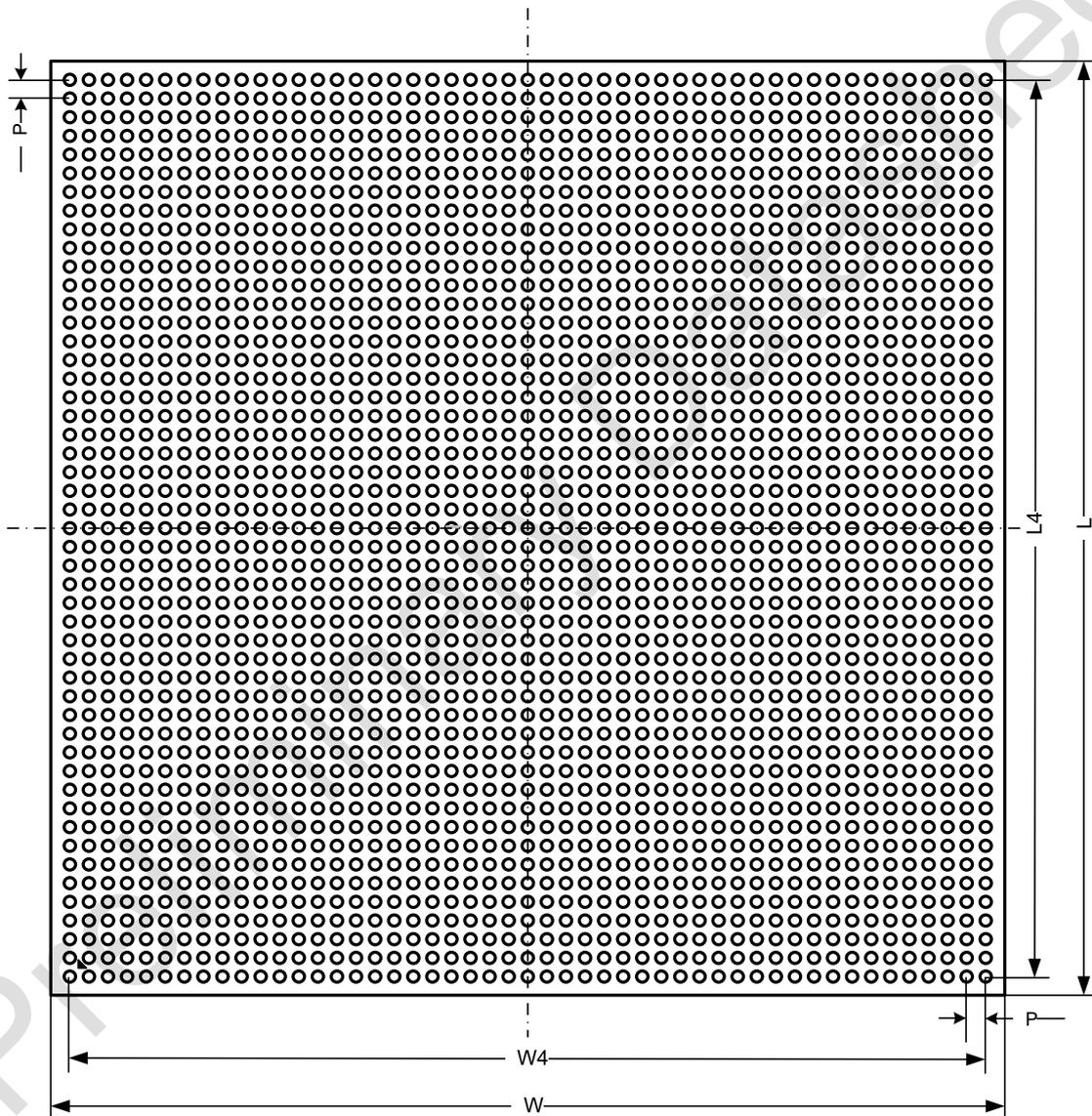


Figure 6-4 SoC Package. Bottom View

The following table shows the package parameters.

Table 6-4 Package Parameters

Symbol	Value, mm	Description
L	40,00	Package length
L1	28,40	Upper cover part length
L2	31,60	Bottom cover part length
L3	39,60	Cover length
L4	38,00	Edge ball center to center
W	40,00	Package width
W1	28,40	Upper cover part width
W2	31,60	Bottom cover part width
W3	39,60	Cover width
W4	38,00	Edge ball center to center
H	2,676...3,176	Package thickness including balls
H1	1,026	Substrate thickness
H2	0,40	Ball height
H3	0,50	Heat sink cover thickness
H4	1,30	Heat sink cover height
D	0,60	Ball diameter
P	1,00	Ball pitch

6.3 Soldering

SoC mounting to PCB should be accomplished in accordance to the soldering profile recommended for Pb-Free packages. Corresponding modes and temperatures are described in the following table and figure.

Table 6-5 Temperature Profile for SoC Soldering to PCB

Profile Feature	Description	Temperature	Duration
A	Preheat stage	150...200°C	60...120 seconds
B	Melting stage	>217°C	60...150 seconds
C	Ramp-up rate	3°C/sec max.	
D	Peak temperature	245°C	
E	Soldering stage	>240°C	30 seconds min.
F	Time from room temperature to peak temperature		< 8 minutes max.
G	Ramp-down rate	6°C/sec max.	

All temperatures refer to topside of the package, measured on the package body surface.

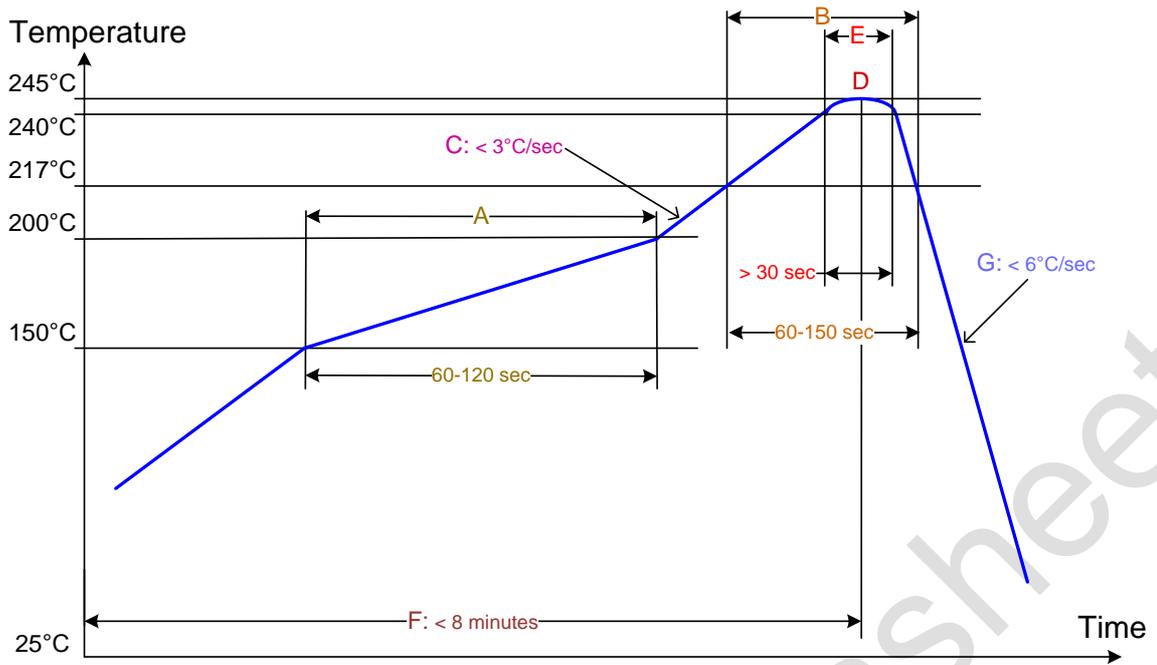


Figure 6-5 Soldering Profile

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7 Ordering Information

BE-M1000 is orderable part number. Designation of each field in the part number is shown in a table below.

Table 7-1 Ordering information

BE	-	M	1	0	0	0
Baikal Electronics	Field Delimiter	Product Line	Generation	Modification	Reserved Field	Reserved Field

BE-M1000 is the first product in BE-M product line.

To order BE-M1000 please contact Baikal Electronics company referred in the next page.

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Contact Info

Baikal Electronics: <https://www.baikalelectronics.com/>

Head Office: <https://www.baikalelectronics.com/contacts/>

Mail: info@baikalelectronics.ru

Phone: [+7 495 221-39-47](tel:+74952213947)

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Revision History

Revision	Date	Substantive change(s)
0.65	02.07.2019	Initial version
0.70	01.11.2019	<p>Chapter 4 Power-Up/Down:</p> <ul style="list-style-type: none"> • Correction of power-up order • The information about power-up sequence
0.72	11.12.2019	<p>Chapter 4 Power-Up/Down:</p> <ul style="list-style-type: none"> • The information about power-down
0.73	16.12.2019	<p>Section 5.1 Pinout List:</p> <ul style="list-style-type: none"> • The following pins changed pin IDs: DDR0_DQ[18], DDR0_DQ[19], DDR0_DQ[20], DDR0_DQ[21], DDR0_DQ[26], DDR0_DQ[27], DDR0_DQ[28], DDR0_DQ[29], DDR0_DQ[41], DDR0_DQ[44], DDR0_DQ[48], DDR0_DQ[51], DDR0_DQ[52], DDR0_DQ[53], DDR0_DQ[56], DDR0_DQ[63]
0.74	04.03.2020	<p>Section 2.4 System Control Module:</p> <ul style="list-style-type: none"> • The information about unaccessability of boot controller's dedicated interfaces for Cortex-A57 cores
0.82	25.05.2020	<p>Section 4.1 Power-Up Sequence:</p> <ul style="list-style-type: none"> • New steps between DDR supply and 1.8V voltage supply
0.83	13.07.2020	The operating frequency value of Arm Mali T-628 GPU shader cores changed from 500 MHz to 700 MHz
0.84	22.10.2020	<p>Mali T-628 GPU: the operating frequency value shader cores changed from 700 MHz to 750 MHz</p> <p>4K Video Decoder has been renamed to HD Video Decoder due to limited support for 4K@30fps video formats</p> <p>LVDS: maximum display resolution changed to up to 2560x1440</p> <p>HDMI: maximum display resolution changed to up to 3840x2160</p> <p>Table 3–1 BE-M1000 Power Domains:</p> <ul style="list-style-type: none"> • PLL supply value changed from 0.9 ± 10 % to 0.95 ± 5 % V • Max power value of 0.95V voltage supply changed from 23W to 24W • Max power value of PLL supply changed from 0.17W to 0.20W • Max power value of 1.5V voltage supply changed from 1.0W to 2.0W • Max power value of 1.8V voltage supply changed from 0.6W to 1.8W • In accordance to changes of max power values for differential erent supply types, total max power value of microprocessor changed from ~28.47W to ~34.7W <p>Section 5.1 Pinout List:</p> <ul style="list-style-type: none"> • A11, B11, D11 and E11 pins are complemented with information

Revision	Date	Substantive change(s)
		about their use for 10GBASE-KR <ul style="list-style-type: none"> The section is complemented with section 5.1.1 Requirements for Unused Pins
0.85	11.11.2020	AA38, AA39, R38, R39, AA35, AA36, R35 R36 pins moved to N/C group and marked as Reserved because LVDS_*[4] pins are not used
0.88	04.06.2021	Display resolution of VDU with HDMI 2.0 changed from 3840x2160 to 2560x1440
0.89	15.06.2021	Chapter 3 Electrical Specifications is updated
0.91	28.06.2021	Section 1.1 Main Features is updated
0.92	14.07.2021	Pin Name and Description of AL18 pin is changed in the section 5.1.5 System Control
0.93	13.08.2021	Section 5.1 Pinout List is supplemented with Voltage range in pin descriptions
0.94	11.10.2021	The document is supplemented with the following sections: <ul style="list-style-type: none"> 2.7.5 HD Audio 6.1 Marking Section 5.1 Pinout List : <ul style="list-style-type: none"> New section 5.1.4.3 HDA Pin Description column is supplemented with information about differences in packages
0.953	13.01.2022	Section 6.1 Marking is updated