ASMEDIA TECHNOLOGY INC

ASM3142 Data Sheet

PCIe to two USB3.1 Gen-II ports xHCI 1.1 Host Controller, supporting Multiple INs

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Environmentally hazardous materials are not used in this product.

Revision History

Rev.	Date	Description
0.1	Feb. 21, 2017	Initial Release
0.2	March 14, 2017	Rename ASM3142
0.3	March 30, 2017	Correct the typo of product name in figure 2 & 3
1.0	May 31, 2017	Add top marking Release mass production
1.1	April 29, 2019	Correct the typo on Page 17
1.2	Sept. 5, 2019	Remove I2C function in pin description
1.3	Dec. 18, 2019	Add timing spec of strapping
1.4	April 27, 2020	Modify pin3 from RSV to PECLKREQ#
1.5	May 11, 2020	Add maximum power consumption for each power domain in section 6.3

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1. General Description

ASMedia ASM3142 is the next generation Universal Series Bus xhci host controller, bridging PCI Express to USB3.1 Gen-II, compliant with USB3.1 Specification Revision 1.0 and Intel eXtensible Host Controller Interface specification revision 1.1. It also supports backward compatible with legacy USB function and devices, compliant with USB Attach SCSI Protocol revision 1.0, supporting the function of debugport on port A of USB.

ASMedia ASM3142 also supports the new feature of USB3.1 Gen2, named Multiple INs to achieve fully utilization rate of 10Gbps data rate, taking advantage of the available bandwidth of USB3.1 Gen2 bus.

ASM3142 supports two USB3.1 Gen-II ports and perform trusting high speed bandwidth with PCI Express Gen-III x2 supporting. It uses advance process with low voltage supply, following standard PCI Express/USB bus power management and advance chip power management to reduce total power consumption efficiently under idle/standby state.

ASM3142 integrates ASMedia self-designed PCI Express/SuperSpeed USB/USB2.0 PHY, supporting the proprietary driver for Windows 7 and in box driver for Windows 8.0, Windows 8.1, Windows 10 and various Linux kernels. The application of ASM3142 includes Motherboard, Desktop PC, Notebooks, Workstations, Servers, Add-in cards, PCI Express based embedded platform.

2. Features

General Feature

- ◇ Bridge PCI Express to USB3.1
- ◇ Integrate eXtensible Host Controller
- ◇ Compliant with eXtensible Host Controller Interface specification Revision 1.1
- ◇ Upload firmware through external SPI ROM
- ◇ External 20MHz differential crystal
- ◇ Support driver on Windows7, Windows8, Windows 8.1, and Windows 10
- ◇ Support various Linux kernels

PCI Express Feature

- ◇ Support PCI Express Gen-III x2
- ◇ Support high bandwidth performance with low latency
- ◇ Support PCI Express Link power management
- ◇ Compliant with PCI Express Base 3.0 Specification
- ◇ Compliant with PCI Express Card Electromechanical 2.0 specification
- ◇ Compliant with PCI Express Mini Card Electromechanical 1.2 specification
- ◇ Compliant with PCI Bus Power Management Interface Specification Revision 1.2
- ◇ Compliant with PCI Local Bus Specification Revision 3.0
- ◇ Integrate Spread Spectrum Controller for PCI Express interface
- ◇ Overclock capability on PCI Express bus
- ◇ Support SRIS mode
- ◇ Not support lane reversal

USB Feature

- ◇ Support two ports of USB3.1
- ◇ Up to USB3.1 Gen-II 10Gbps
- ◇ Compliant with Universal Serial Bus 3.1 Specification Revision 1.0
- ◇ Compliant with Universal Serial Bus Specification Revision 2.0
- ◇ Compliant with USB Attached SCSI Protocol Revision 1.0
- ◇ Support Muliple INs function
- ◇ Support USB3.1 and USB2.0 Link Power Management

- ◇ Support Control, Bulk, Stream, Interrupt, Isochronous transfer type
- ◇ Support independent port power control
- ◇ Support overcurrent detection
- ◇ Support Remote/Wakeup event
- ◇ Integrate Spread Spectrum Controller for USB3.1 interface
- ◇ Backward compatible with Legacy USB function and device
- ◇ Support the Debugport

Package Type

- ◇ Green Package 9x9 QFN64 (Pb-free) - RoHS Compliance

3. Functional Diagram

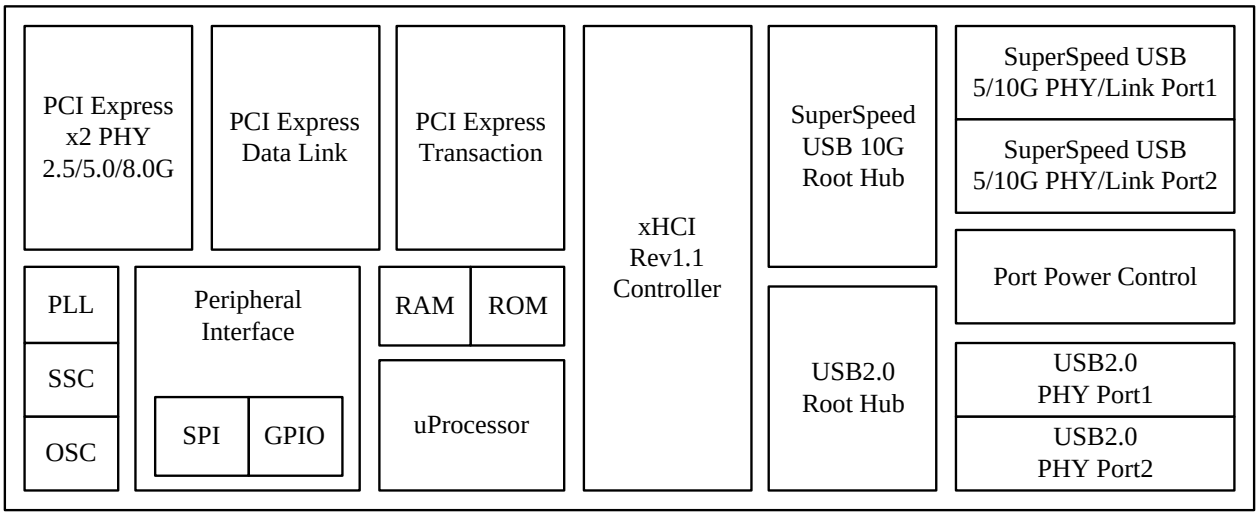


Figure 1: Functional Diagram of ASM3142

4. Pinout Diagrams

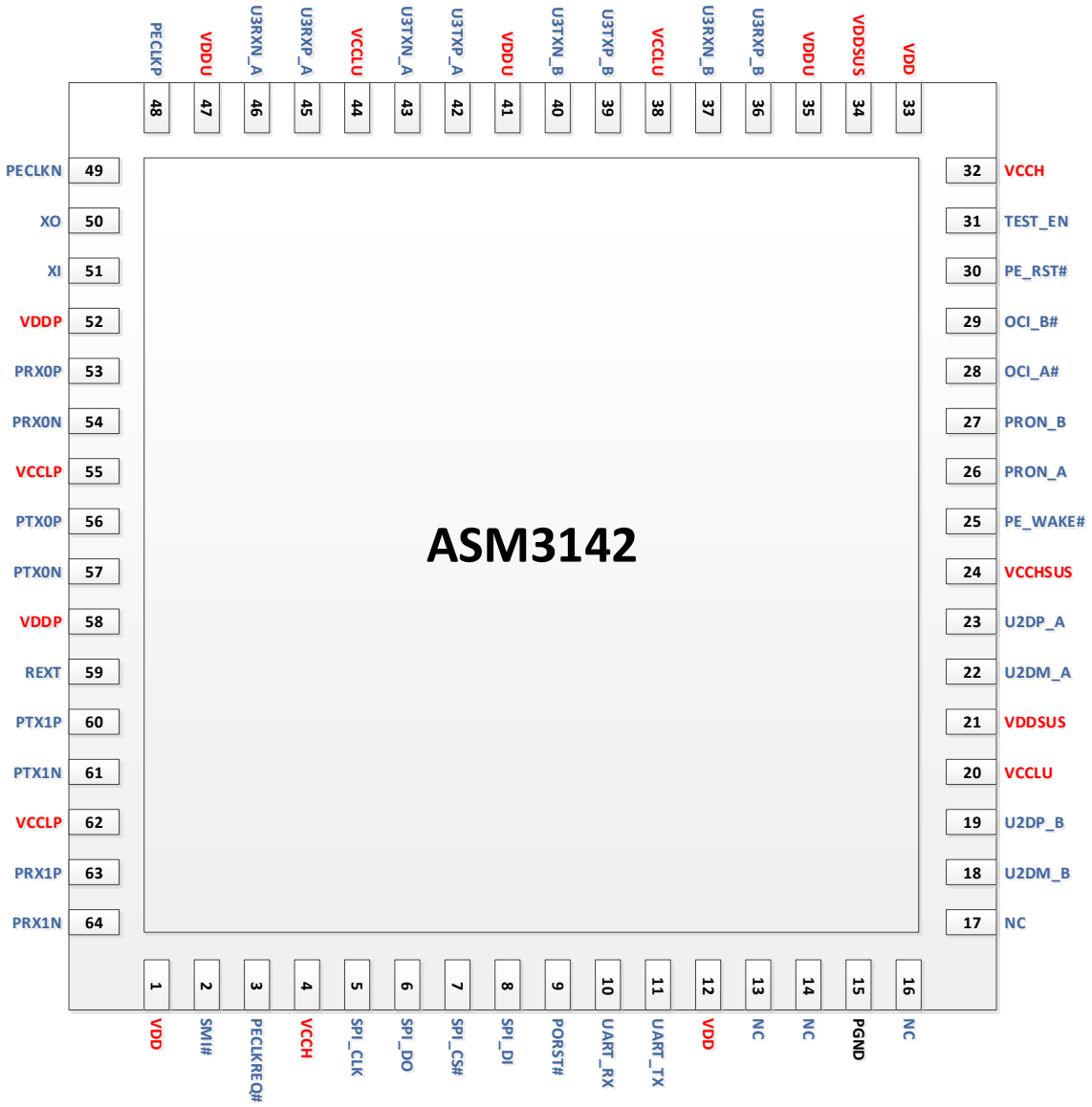


Figure 2: ASM3142 QFN64 pinout

5. Pin Descriptions

This section provides a detailed description of each signal. The following notations are used to describe the signal type.

I/O Type	Definition
I	Input pin
O	Output pin
P	Power pin
G	Ground pin
OD	Open Drain

PCI Express Interface

QFN64	Name	PWR	TYPE	Descriptions
53	PRX0P	VCCLP	I	PCI Express Differential Receive Signal +
54	PRX0N	VCCLP	I	PCI Express Differential Receive Signal -
56	PTX0P	VCCLP	O	PCI Express Differential Transmit Signal +
57	PTX0N	VCCLP	O	PCI Express Differential Transmit Signal -
63	PRX1P	VCCLP	I	PCI Express Differential Receive Signal +
64	PRX1N	VCCLP	I	PCI Express Differential Receive Signal -
60	PTX1P	VCCLP	O	PCI Express Differential Transmit Signal +
61	PTX1N	VCCLP	O	PCI Express Differential Transmit Signal -
48	PE_CLKP	VCCLP	I	PCI Express Differential Clock Signal+
49	PE_CLKN	VCCLP	I	PCI Express Differential Clock Signal-
25	PE_WAKE#	VCCHSUS	O	PCI Express Remote/Wakeup Internal pull up resistor
30	PE_RST#	VCCHSUS	I	PCI Express Reset
3	PECLKREQ#	VCCH	O	PCI Express Reference clock request

USB Interface

QFN64	Name	PWR	TYPE	Descriptions
18	U2DM_B	VCCHSUS	IO	USB2.0 Differential Signal- for Port B
19	U2DP_B	VCCHSUS	IO	USB2.0 Differential Signal+ for Port B
22	U2DM_A	VCCHSUS	IO	USB2.0 Differential Signal- for Port A
23	U2DP_A	VCCHSUS	IO	USB2.0 Differential Signal+ for Port A
36	U3RXP_B	VCCLU	I	USB3.1 Differential Receive Signal + for Port B
37	U3RXN_B	VCCLU	I	USB3.1 Differential Receive Signal - for Port B
39	U3TXP_B	VCCLU	O	USB3.1 Differential Transmit Signal + for Port B
40	U3TXN_B	VCCLU	O	USB3.1 Differential Transmit Signal - for Port B
42	U3TXP_A	VCCLU	O	USB3.1 Differential Transmit Signal + for Port A
43	U3TXN_A	VCCLU	O	USB3.1 Differential Transmit Signal - for Port A
45	U3RXP_A	VCCLU	I	USB3.1 Differential Receive Signal + for Port A
46	U3RXN_A	VCCLU	I	USB3.1 Differential Receive Signal - for Port A
26	PRON_A	VCCHSUS	O	Port Power Control for Port A
27	PRON_B	VCCHSUS	O	Port Power Control for Port B
28	OCI_A#	VCCHSUS	I	Overcurrent Signal for Port A Internal pull up resistor
29	OCI_B#	VCCHSUS	I	Overcurrent Signal for Port B Internal pull up resistor

SPI Interface

QFN64	Name	PWR	TYPE	Descriptions
5	SPI_CLK	VCCH	O	Clock of Serial Peripheral Interface Strapping pin for AUX_EN

QFN64	Name	PWR	TYPE	Descriptions
				Internal pull up resistor
6	SPI_DO	VCCH	O	Data Output of Serial Peripheral Interface Internal pull up resistor
7	SPI_CS#	VCCH	O	Chip Select of Serial Peripheral Interface Internal pull up resistor
8	SPI_DI	VCCH	I	Data Input of Serial Peripheral Interface Internal pull up resistor

System Interface

QFN64	Name		TYPE	Descriptions
10	UART_RX	VCCH	I	UART Rx Signal, Strapping pin for Clock Select Internal pull up resistor
11	UART_TX	VCCH	O	UART Tx Signal, Internal pull up resistor
9	PORST#	VCCH	I	Power On Rest
59	REXT	VCCH	I	External Reference 12.1Kohm+/-1% Resistor to GND
31	TEST_EN	VCCHSUS	I	Test Mode Enable Internal pull down resistor
2	SMI#	VCCH	O	System management Interrupt Internal pull up resistor IO type is configurable as open-drain or push-pull mode by firmware
50	XO	VCCH	B	20MHz Crystal Output
51	XI	VCCH	I	20MHz Crystal Input
13 14 16 17	NC			Not connect

Power and Ground

QFN64	Name	TYPE	Descriptions
4, 32	VCCH	**P**	3.3V IO Power
1, 12, 33	VDD	**P**	1.1V Core Power
20, 38, 44	VCCLU	**P**	2.5V Analog Power for USB
35, 41, 47	VDDU	**P**	1.1V Analog Power for USB
55, 62	VCCLP	**P**	2.5V Analog Power for PCI Express
52, 58	VDDP	**P**	1.1V Analog Power for PCI Express
24	VCCHSUS	**P**	3.3V Suspend Power
21, 34	VDDSUS	**P**	1.1V Suspend Power
65	GND	**G**	Common Ground
15	PGND	**G**	Analog Ground

Strapping Table

	Function	Description
UART_RX	Clock Select	1: Asynchronous mode with External 20MHz Crystal (Default) 0: SRIS mode with External 20MHz Crystal
SPI_CLK	AUX_EN	1:support remote/wakeup with suspend power existed 0:not support

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

The below stress value parameter shows absolute maximum rating which may cause the device to have permanent damage. This is a stress rating only, and the function operating of the device at these or any other conditions over those parameter in the recommended operating condition is not implied. It is recommended to have a clamp circuit to protect the device with abnormal voltage spikes while power is switched on or off.

Parameter	Range	Unit
Power Supply for VCC	-0.5 ~ VCCX+0.5	V
Power Supply for VDD	-0.5 ~ VDDX+0.5	V
DC Input Voltage	-0.5 ~ VCCX+0.5	V
Output Voltage	-0.5 ~ VCCX+0.5	V
Storage Temperature	JEDEC J-STD-033B MSL 3	

6.2 Recommended Operating Conditions

Symbols	Parameter	Min.	Typ.	Max.	Units	Remark
VCCH	Normal Power Supply for IO	3.0	3.3	3.6	V	
VCCLU, VCCLP	Normal Power Supply for PHY	2.3	2.5	2.7	V	
VDD, VDDU, VDDP	Normal Power Supply for Core Logic	1.05	1.1	1.15	V	
VCCHSUS	Suspend Power Supply for PHY	3.0	3.3	3.6	V	
VDDSUS	Suspend Power Supply for Logic	1.05	1.1	1.15	V	
T_J	Operating Junction Temperature	0	25	125	ºC	
T_C	Operating Case Temperature	0		85	ºC	
HBM ESD	Human Body Mode ESD capability	4			KV	
MM ESD	Machine mode ESD capability	200			V	

Chip Temperature (T_J, T_C) Calculation

Symbols	Parameter	How to get?
T_A	Ambient temperature	Measure temperature around chip
T_J	Operating junction temperature	$T_J = \Theta_{JA}$ * Power + T_A
T_C	Operating case temperature	$T_C = T_J - \Psi_{JT}$ * Power
R_{JA}	Junction to Ambient thermal resistance	23.8 (data from package vender)
R_{JC}	Junction to case thermal resistance	5.4 (data from package vender)
Ψ_{JT}	Junction to top thermal characterization	0.08 (data from package vender)
Power	Chip power consumption	Measure chip power consumption

- Thermal test board condition, please refer to JEDEC JESD51-5
- Thermal test method environmental conditions refer to JESD51-2
- Example: If chip power consumption is 1.25W; T_A=55^{0}C
  T_J = 23.8*1.25 + 60 = 84.75^{0}C
  T_C = 84.75 – 0.08*1.25 = 84.65^{0}C

6.3 AC/DC Characteristics

Digital Pin Specification

Symbols	Parameter	Min.	Typ.	Max.	Units	Remark
V_{IH}	Input High Level	2.0		VCCH	V	
V_{IL}	Input Low Level	-0.5		0.8	V	
I_{LEAK}	Input Leakage Level			10	uA	
V_{OH}	Output High Level	2.4		VCCH	V	
V_{OL}	Output Low Level	-0.5		0.5	V	

PCI Express Electrical Specification
(Refer to PCI Express Base Specification Rev. 3.0)

USB3.1 Electrical Specification
(Refer to Universal Serial Bus 3.1 Specification Rev. 1.0)

USB2.0 Electrical Specification
(Refer to Universal Serial Bus Specification Rev. 2.0)

PCI Express Differential Reference Clock Input Ranges

Symbols	Parameter	Min	Typ	Max	Unit	Remark
$F_{IN-DIFF}$	The input frequency is 100 MHz + 300 ppm and max. – 5000 including SSC-dictated variations Differential input frequency		100		MHz	
	Rising Edge Rate	0.6		4.0	V/ns	
	Falling Edge Rate	0.6		4.0	V/ns	
V_{IH}	Differential Input High Voltage	150			mV	
V_{IL}	Differential Input Low Voltage			-150	mV	
V_{CROSS}	Absolute crossing point voltage	250		550	mV	
$V_{CROSS-DELTA}$	Variation of VCROSS over all rising clock edges			140	mV	
V_{RB}	Ring-back Voltage Margin	-100		100	mV	
T_{STABLE}	Time before VRB is allowed	500			ps	
$T_{PERIOD-AVG}$	Average Clock Period Accuracy	-300		2800	ppm	
$T_{PERIOD-ABS}$	Absolute Period (including Jitter and Spread Spectrum)	9.847		10.203	ns	
$T_{CC-JITTER}$	Cycle to Cycle Jitter			150	ps	
V_{MAX}	Absolute Max input voltage			1.15	V	
V_{MIN}	Absolute Min input voltage			-0.3	V	
	Duty Cycle	40		60	%	
R/F Matching	Rising edge rate (REFCLK+) to Falling edge rate (REFCLK-) matching			20	%	
Z_{C-DC}	Clock source DC impedance	40		60	Ω	

20MHz Crystal Electrical Specification

Note: please refer to the figure 3

Symbol	Parameter	Min.	Typ	Max.	Unit
f_{XTAL}	Frequency		20		MHz
$\triangle f_{XTAL}$	Long Term Stability (at 250C)	-30		30	ppm
T_C	Temperature Stability	-30		30	ppm
F_A	Aging	-5		5	ppm
C_L	Load Capacitance (Single-end mode)		16		pF
C_0	Shunt Capacitance	1	3	7	pF

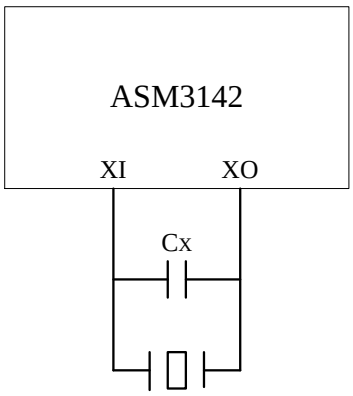


Figure 3: Differential Crystal Design

20MHz Clock input Electrical Specification (from 20MHz crystal)

Note: please refer to the figure 3

Symbol	Parameter	Min.	Typ	Max.	Unit
f_{CLK}	Frequency		20		MHz
$\triangle f_{CLK}$	Long Term Stability (all condition)	-150		150	ppm
C_X	External Load Capacitance (Differential mode)		C_{TOTAL}-C_O		pf
C_{TOTAL}	Total External Equivalent Capacitance from XI pin to XO pin (Differential mode)	9	11	15	Pf
R_{TOTAL}	Total External Equivalent Series Resistance from XI pin to XO pin			60	Ω

Power Consumption design

Symbol	Parameter	Max.	Unit
VCCH	Normal Power Supply for IO	2	mA
VCCLx	Normal Power Supply for PHY	300	mA
VDD	Normal Power Supply for Core Logic	800	mA
VCCHSUS	Suspend Power Supply for PHY	20	mA
VDDSUS	Suspend Power Supply for Logic	20	mA

7. Timing Diagram

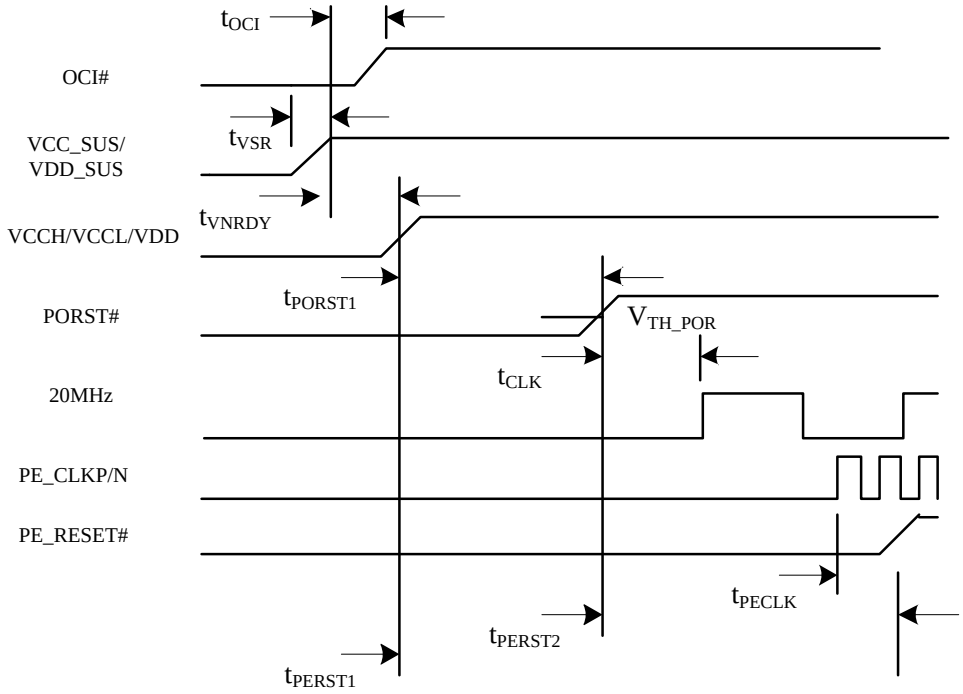


Figure 4: Power On Sequence for Asynchronous mode

Power On Sequence Timing Specification for Asynchronous mode

Symbols	Parameter	Min	Typ	Max	Unit	Remark
V_{TH_POR}	Threshold voltage for PORST# pins	1.38	1.6	1.8	V	
t_{OCI}	OCI# ready after Suspend Power Ready			12	ms	
t_{VSR}	Rising time for Suspend and normal Power Ready			10	ms	
t_{VNRDY}	Timing for all normal power Ready	50			ms	Note 1
t_{PORST1}	Timing for all normal Power Ready to Power On Reset (when suspend power domains are existed)	10		80	ms	
	Timing for all normal Power Ready to Power On Reset (when suspen powers connect to normal power directly)	60		80	ms	
t_{PECLK}	Timing for PE_CLK Ready to PE_RST#	100			µs	
t_{CLK}	Timing for 20MHz Crytsal Clock Ready to Power On Reset **(relate to max value of V_{TH_POR})**			4	ms	
t_{PERST1}	Timing for PE_RST# delay after Normal Power Ready (D3Cold)	210			ms	
	Timing for PE_RST# delay after Normal Power Ready (D3Hot)	250			ms	
t_{PERST2}	Timing for PE_RST# delay after PORST# comes up	200			ms	

Note:

1. When ASM3142 configures as D3Hot mode, the suspend power should connect with normal power for each voltage domain. The tVNRDY should be 0 ms.
2. For the timing of tPORST1, it should be measured from 90% of last power domain ready to PORST# ramping up.

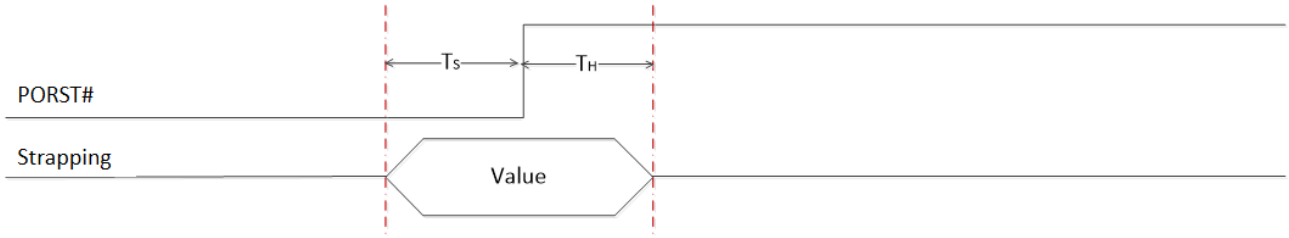


Figure 5: timing for strapping

Power On Sequence Timing Specification for Strapping

Symbols	Parameter	Min	Typ	Max	Unit	Remark
Ts	Setup time for capture	1			ms	
TH	Hold time for capture	1			ms	

8. PCB Design Guide under Thermal Pad

To improve the thermal efficiency and signal integrity, it is recommended to place the thermal-via under or near to thermal pad. To avoid process issues, please make sure the thermal-via is completely filled with solder paste covered by solder mask. It is recommended to follow up the pattern on PCB as Figure 6 or Figure 7.

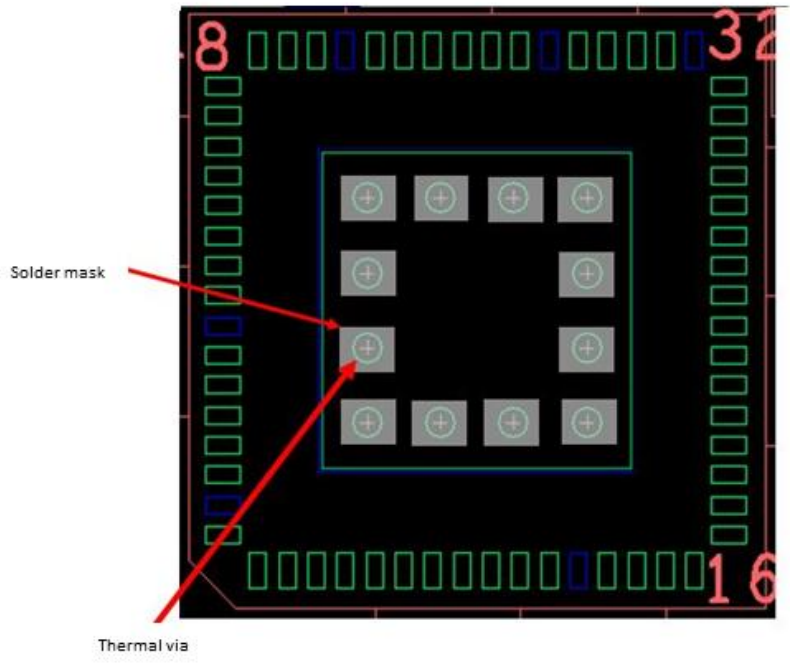


Figure 6: Symbol 1 for via design rule under Thermal pad

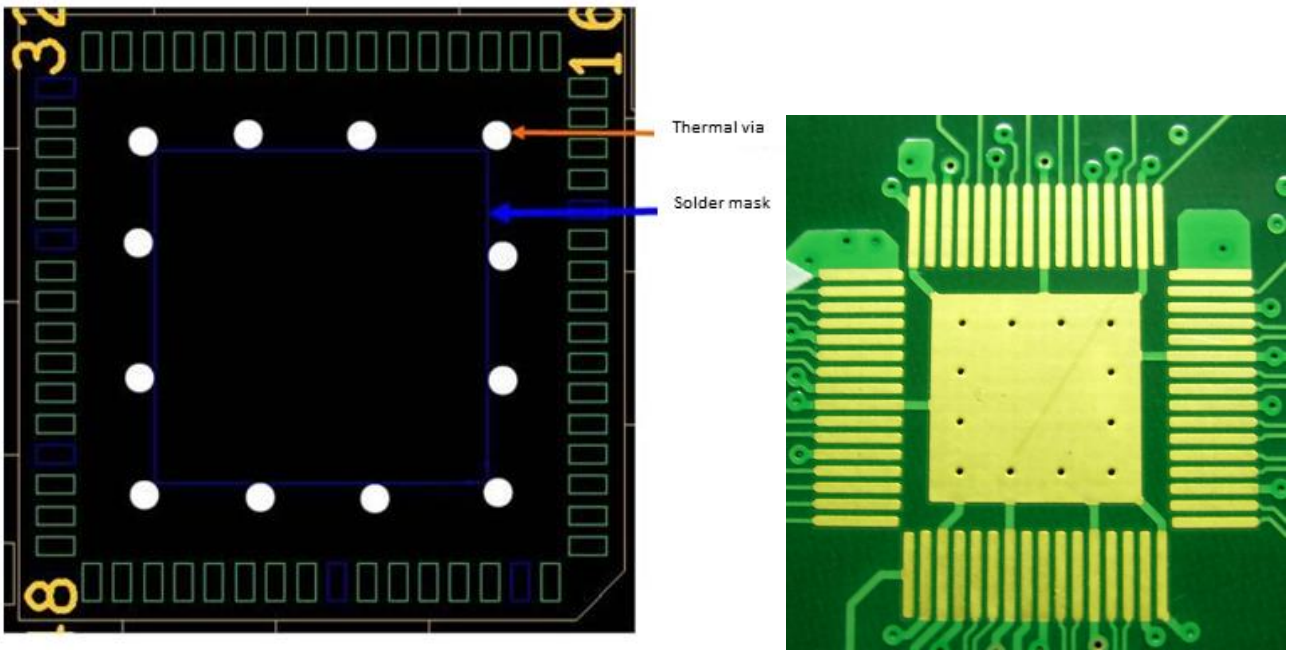
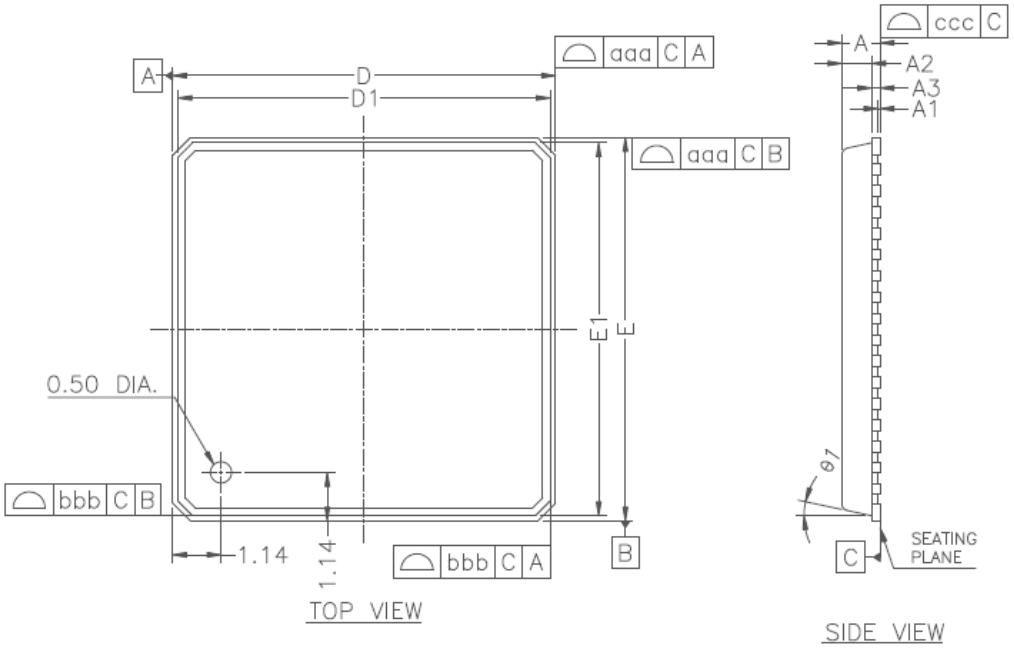
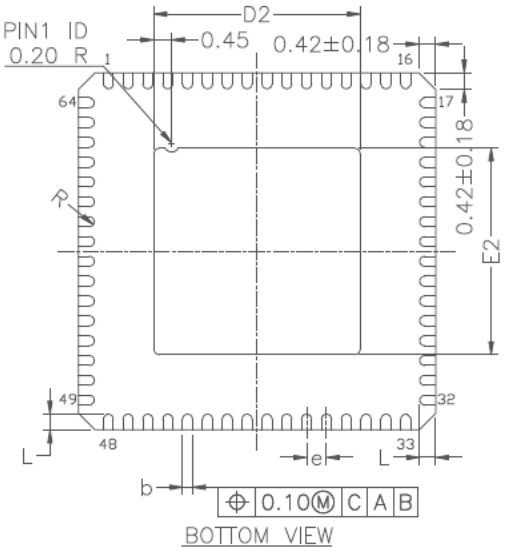


Figure 7: Symbol 2 for via design rule under Thermal pad

9. Package Information





NOTES :

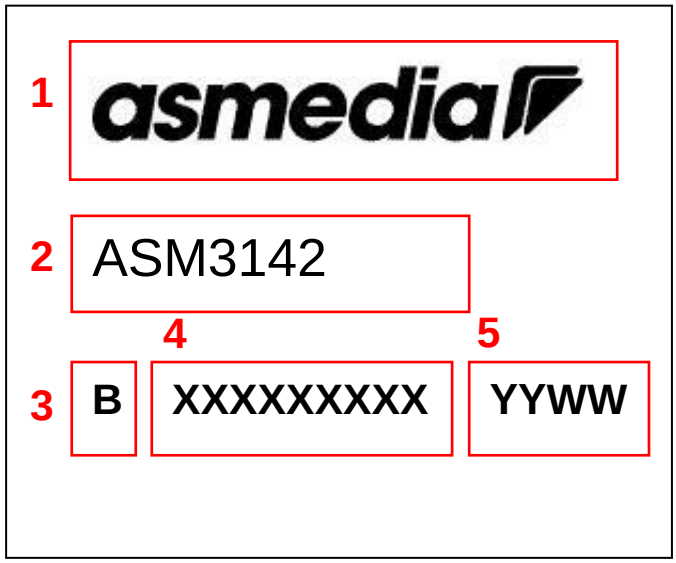
1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3.DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. −1994.
4.DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED
BETWEEN 0.20 AND 0.25 mm FROM TERMINALTIP.
5.THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE
PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6.EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7.PACKAGE WARPAGE MAX 0.08 mm.
8.APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED
PAD FROM MEASURING.
9.APPLIED ONLY TO TERMINALS.
10.PACKAGE CORNERS UNLESS
OTHERWISE SPECIPIED
ARE R0.175±0.025 mm.

*CONTROLLING DIMENSION : MM

SYMBOL	MILLMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.90	---	---	0.035
A1	0.00	0.01	0.05	0.00	0.0004	0.002
A2	---	0.65	0.70	---	0.026	0.028
A3	0.20 REF.			0.008 REF.		
b	0.20	0.25	0.30	0.008	0.010	0.012
D/E	9.00 bsc			0.354 bsc		
D1/E1	8.75 bsc			0.344 bsc		
D2/E2	5.007	5.207	5.407	0.197	0.205	0.213
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.50 bsc			0.020 bsc		
θ1	0^0	---	12^0	0^0	---	12^0
R	0.10	---	---	0.004	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

Figure 8: Mechanical Specification – QFN 64

10. Top Marking Information



1. asmedia: ASMedia Logo
2. ASM3142: Product Name
3. B: Version of ASMedia Logo
4. XXXXXXXXX: Serial No. Reserved for Vendor
5. YYWW: Date Code