ASM1085 Data Sheet

PCIE to PCI Bridge

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Office:
ASMedia Technology, Inc.
6F, No.115, Minquan Rd., Xindian City, Taipei County 231, Taiwan, R.O.C.
http://www.asmedia.com.tw
Tel: 886-2-2219-6088
Fax: 886-2-2219-6080

Environmentally hazardous materials are not used in this product.

Revision History

Rev.	Date	Description
0.1	March. 24, 2010	Initial Release
0.2	March. 31, 2010	Sync Pin diagram and Pin description
0.3	April. 16, 2010	Add Power/Reset/Clock sequence
0.4	May. 28, 2010	Change product name to ASM1083 Add legacy mode support Add PCI clock control signal Change register set
0.5	June. 14, 2010	Add register for fixed design Change GPIO11,12 to NC pin Add power consumption table
0.6	June. 23, 2010	Sync Pin list table with real chip
1.0	July.1, 2010	Formal release
1.1	July. 23, 2010	Fix Pin PE_EC_SEL and M66EN direction Remove clock sync mode
1.2	Aug. 25, 2010	Fix REXT value to 12.1K
1.3	Sep. 16, 2010	Fix GPIO2 description Package type is LQFP128
1.4	Sep. 21, 2010	Remove 66MHz feature
1.5	April. 19, 2011	Change M66EN pin description
1.6	April. 21, 2011	Add Top Marking Information
1.7	Aug. 30, 2011	Pin 47 is not VCC33, remove it
1.8	Nov. 30, 2011	Modify for B2
1.9	Feb. 6, 2012	Add Pin80 as GND; Remove “preliminary” title
2.0	May. 11, 2012	No ASPM support
2.1	Oct. 22, 2012	Modify register
2.2	June. 7,2013	Remove core power typical value
2.3	June. 18, 2013	Modify register set offset44, 45
MOD	Feb. 18, 2025	Change product name to ASM1085 and added missing pins for PCI master 4 and 5

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1. General Description

Engaged in High Speed I/O solution development, Asmedia Technology is committed to enlarging product portfolio with introducing PCI Express Bridge Products. The ASM1085, x1 PCI Express to 32-bit PCI Bridge, enable users to connect legacy parallel bus devices to the advanced serial PCI Express interface. The ASM1085 is a PCI Express-to-PCI forward bridge, fully compliant with PCI-SIG PCI Express-to-PCI Bridge Specification1.0.

2. Features

General Features

- I2C Serial EEPROM support
- Extensive PME support
- 3.3/1.2V power supply
- Legacy mode support
- Industry Specifications Compliance:
  PCI Express Base Specification Rev. 1.0a/ 1.1
  PCI Bus Power Management Interface Rev.2.0
  PCI Express Card Electromechanical Rev.2.0
  PCI Specification Rev.3.0
  PCIE to PCI/PCIX Bridge Specification Rev.1.0
- 14mmx14mm 128-pin LQFP package
- Green package with RoHs compliance

PCI Express Features

- x1 PCI Express lane, at 2.5GHz signaling
- Single virtual channel
- SSC support
- ECRC and Advanced Error Reporting capability
- 100-MHz differential PCI Express reference clock in
- Maximum Payload Size up to 128 bytes
- No PCIe ASPM support

PCI Features

- Support PCI bus 33 MHz
- Support 5 PCI masters
- CLKRUN support
- PME support

3. Package Type

◇ LQFP 128L

4. Functional Diagram

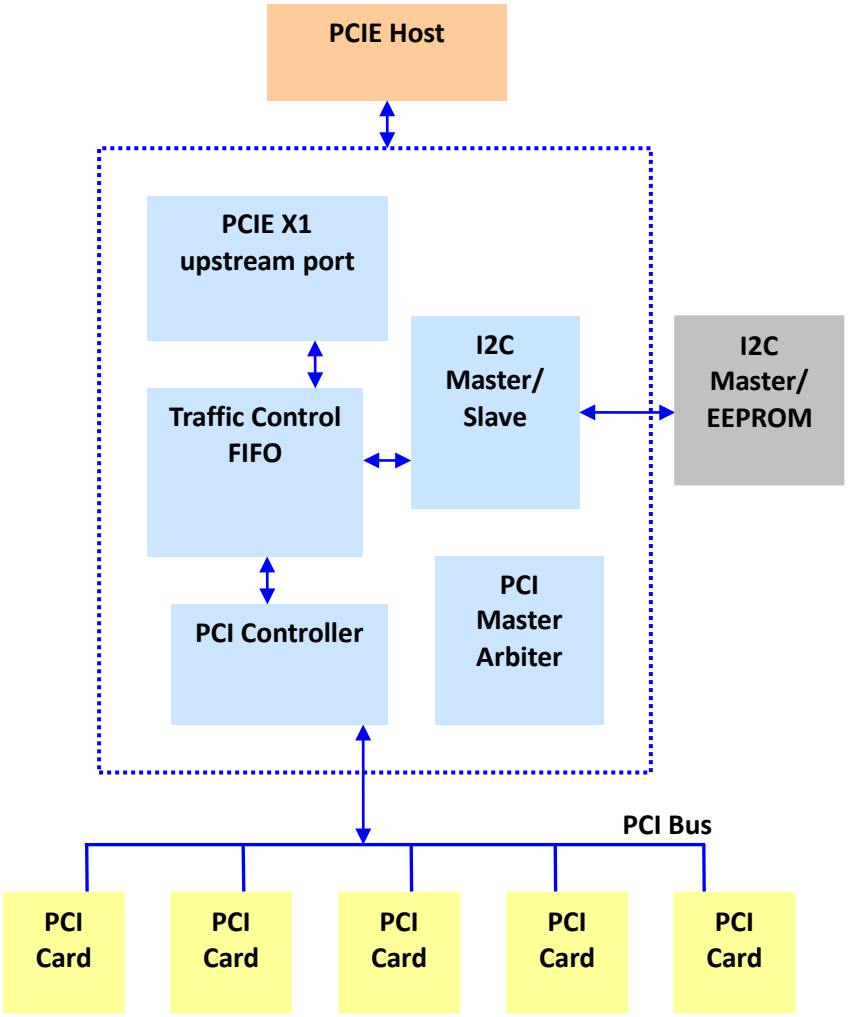


Figure 1: Functional Diagram

5. Pinout Diagrams

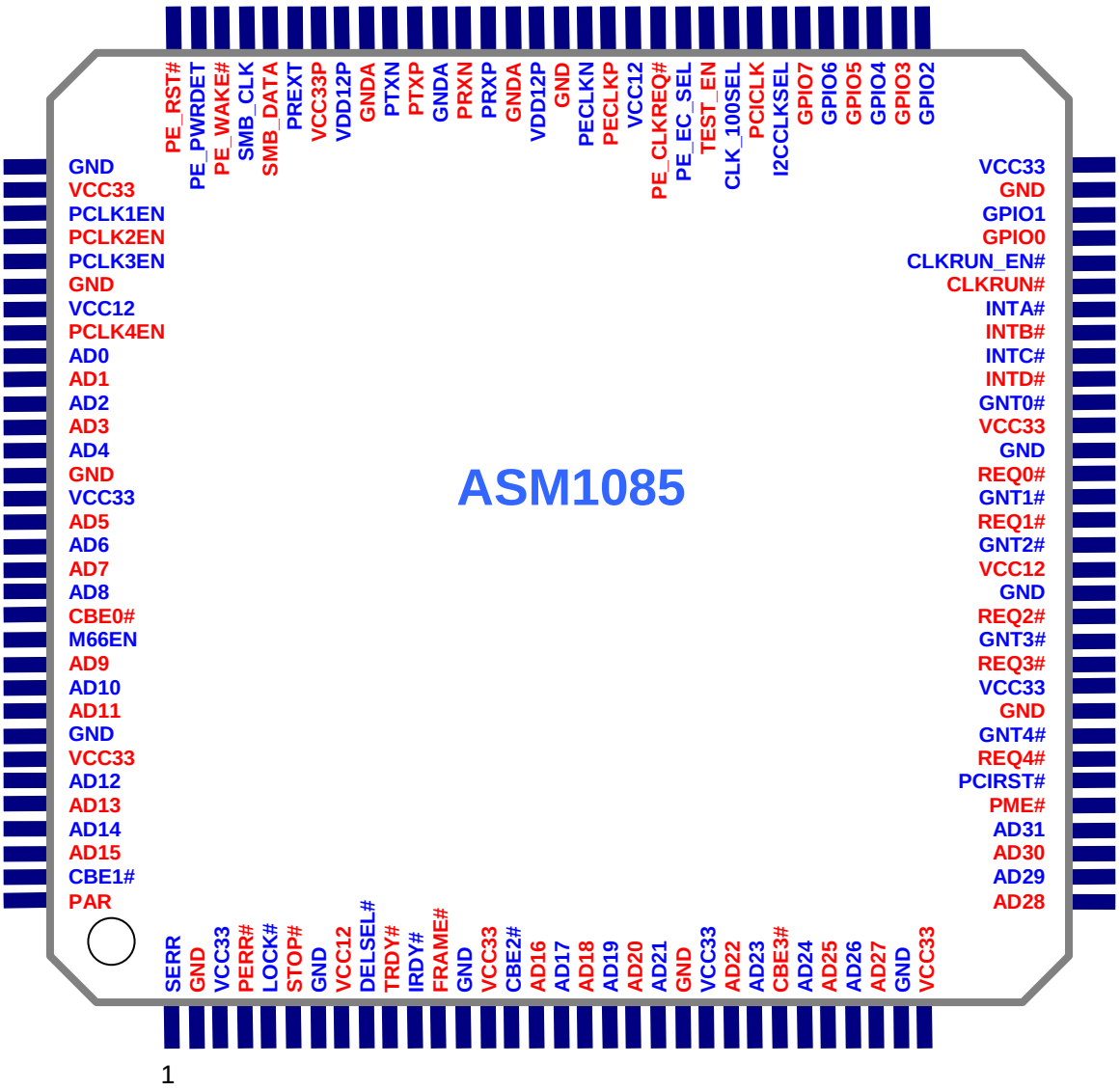


Figure 2: ASM1085

6. Pin Descriptions

This section provides a detailed description of each signal. The following notations are used to describe the signal type.

I/O Type	Definition
I	Input pin
O	Output pin
B	Bi-directional pin
TS	Tri-State bidirection
STS	Sustain Tri-State, Active Low
P	Power pin
G	Ground pin
OD	Open Drain

Pin Name	Pin Number	I/O	Descriptions
PCIE Signals			
PREXT	91	I	External Resistor for PCIE PHY. A 12.1K ohm+/-1% external resistor should be connected this pin to ground.
PRXP	83	I	PCIE Receiver Rx+ Signal
PRXN	84	I	PCIE Receiver Rx- Signal
PTXN	87	O	PCIE Transmitter Tx- Signal
PTXP	86	O	PCIE Transmitter Tx+ Signal
PECLKP	78	I	PCIE Diffriential Clock Input+
PECLKN	79	I	PCIE Diffriential Clock Input-
PE_WAKE#	94	O	PCIE wake up signal
PE_RST#	96	I	PCIE reset, also the global reset of whole chip
PE_PWRDET#	95	I	Power detector
PE_CLKREQ#	76	O	PCIE clock request
PE_EC_SEL	75	I	PCIExpress card select
PCI Signals			
AD0	105	TS	PCI Data Bus
AD1	106	TS	PCI Data Bus
AD2	107	TS	PCI Data Bus
AD3	108	TS	PCI Data Bus
AD4	109	TS	PCI Data Bus
AD5	112	TS	PCI Data Bus
AD6	113	TS	PCI Data Bus
AD7	114	TS	PCI Data Bus
AD8	115	TS	PCI Data Bus
AD9	118	TS	PCI Data Bus
AD10	119	TS	PCI Data Bus
AD11	120	TS	PCI Data Bus
AD12	123	TS	PCI Data Bus
AD13	124	TS	PCI Data Bus
AD14	125	TS	PCI Data Bus
AD15	126	TS	PCI Data Bus
AD16	16	TS	PCI Data Bus
AD17	17	TS	PCI Data Bus
AD18	18	TS	PCI Data Bus

Pin Name	Pin Number	I/O	Descriptions
AD19	19	TS	PCI Data Bus
AD20	20	TS	PCI Data Bus
AD21	21	TS	PCI Data Bus
AD22	24	TS	PCI Data Bus
AD23	25	TS	PCI Data Bus
AD24	27	TS	PCI Data Bus
AD25	28	TS	PCI Data Bus
AD26	29	TS	PCI Data Bus
AD27	30	TS	PCI Data Bus
AD28	33	TS	PCI Data Bus
AD29	34	TS	PCI Data Bus
AD30	35	TS	PCI Data Bus
AD31	36	TS	PCI Data Bus
CBE0#	116	TS	PCI Command/ByteEnable
CBE1#	127	TS	PCI Command/ByteEnable
CBE2#	15	TS	PCI Command/ByteEnable
CBE3#	26	TS	PCI Command/ByteEnable
PAR	128	TS	PCI Parity
PCIRST#	38	O	PCI reset, reset all PCI slots
FRAME#	12	STS	PCI Bus Control Signal, PCI Frame, A Pullup resister is needed.
IRDY#	11	STS	PCI Bus Control Signal, PCI Initial Ready, A Pullup resister is needed.
TRDY#	10	STS	PCI Bus Control Signal, PCI Target Ready, A Pullup resister is needed.
STOP#	6	STS	PCI Bus Control Signal, PCI Stop, A Pullup resister is needed.
DEVSEL#	9	STS	PCI Bus Control Signal, PCI Device Select, A Pullup resister is needed.
LOCK#	5	STS	PCI Bus Control Signal, PCI Lock, A Pullup resister is needed.
SERR#	1	OD	PCI Bus Control Signal, System Error, A Pullup resister is needed.
PERR#	4	STS	PCI Bus Control Signal, Parity Error, A Pullup resister is needed.
PME#	37	I	PCI Wakeup Signal, Power managerment event. , A Pullup resister is needed.
REQ0#	51	TS	PCI Request Signal for master 0. A Pullup resister is needed.
GNT0#	54	O	PCI Grant Signal for master 0
REQ1#	49	TS	PCI Request Signal for master 1. A Pullup resister is needed.
GNT1#	50	O	PCI Grant Signal for master 1
REQ2#	45	TS	PCI Request Signal for master 2. A Pullup resister is needed.
GNT2#	48	O	PCI Grant Signal for master 2
REQ3#	43	TS	PCI Request Signal for master 3. A Pullup resister is needed.
GNT3#	44	O	PCI Grant Signal for master 3
REQ4#	39	TS	PCI Request Signal for master 4. A Pullup resister is needed.
GNT4#	40	O	PCI Grant Signal for master 4
INTA#	58	OD	Interrupt A. A Pullup resister is needed.
INTB#	57	OD	Interrupt B. A Pullup resister is needed.
INTC#	56	OD	Interrupt C. A Pullup resister is needed.
INTD#	55	OD	Interrupt D. A Pullup resister is needed.
CLKRUN#	59	STS	PCI Clock Run Control Signal. A Pullup resister is needed.
CLKRUN_EN#	60	I	A Strapping Pin. PCI Clock Run Control Enable
M66EN	117	I	No 66MHz support, connect to GND
PCICLK	72	I	PCI 33MHz Input Clock. PCI Clock Source.
CLK100SEL	73	I	Test pin, a pull down resistor is needed
MISC Signals			
TEST_EN	74	I	Test Mode Enable
SMB_CLK	93	B	I2C Clock Signal
SMB_DATA	92	B	I2C Data Signal

Pin Name	Pin Number	I/O	Descriptions
GPIO0	61	O	GPIO0, If TEST_EN=0, It's PCI Output Clock for Master 0 (PCLKO0). If TEST_EN=1, It's test mode function select
GPIO1	62	O	GPIO1, If TEST_EN=0, It's PCI Output Clock for Master 1 (PCLKO1). If TEST_EN=1, It's test mode function select
GPIO2	65	O	GPIO2, If TEST_EN=0, It's PCI Output Clock for Master 2 (PCLKO2). If TEST_EN=1, It's test mode function select
GPIO3	66	O	GPIO3, If TEST_EN=0, It's PCI Output Clock for Master 3 (PCLKO3). If TEST_EN=1, It's test mode function select
GPIO4	67	O	GPIO4, If TEST_EN=0, It's PCI Output Clock for Master 4 (PCLKO4). If TEST_EN=1, It's test mode function select
GPIO5	68	B	Reaserved For Debug
GPIO6	69	B	Reaserved For Debug
GPIO7	70	B	Reaserved For Debug
I2CCLKSEL	71	B	I2C clock select; 0: 67.5KHz; 1: 135KHz
PCLK1EN	99	B	1. PCLKO1 Clock enable; 2.Reaserved For Debug
PCLK2EN	100	B	1. PCLKO2 Clock enable; 2.Reaserved For Debug
PCLK3EN	101	B	1. PCLKO3 Clock enable; 2.Reaserved For Debug
PCLK4EN	104	B	1. PCLKO4 Clock enable; 2.Reaserved For Debug
VCC12	8, 47, 77, 103	P	1.2V Power Input, core power
VCC12P	81,89	P	1.2V Power Input for PCIE PHY
VCC33	3, 14, 23, 32, 42, 53, 64, 98, 111, 122	P	3.3V Power Input, for PCI Pad
VCC33P	90	P	3.3V Power Input, for PCIE PHY
GND	2, 7, 13, 22, 31, 41, 46, 52, 63, 80, 97, 110, 102, 121	G	Ground, for Core and PCI Pad
GNDA	82, 85, 88	G	Ground, for PCIE PHY & PLL

7. Function Description

1. The content described here are only for specific functions in ASM1085. PCIE and PCI bus functions can be found in PCIE and PCI specifications.

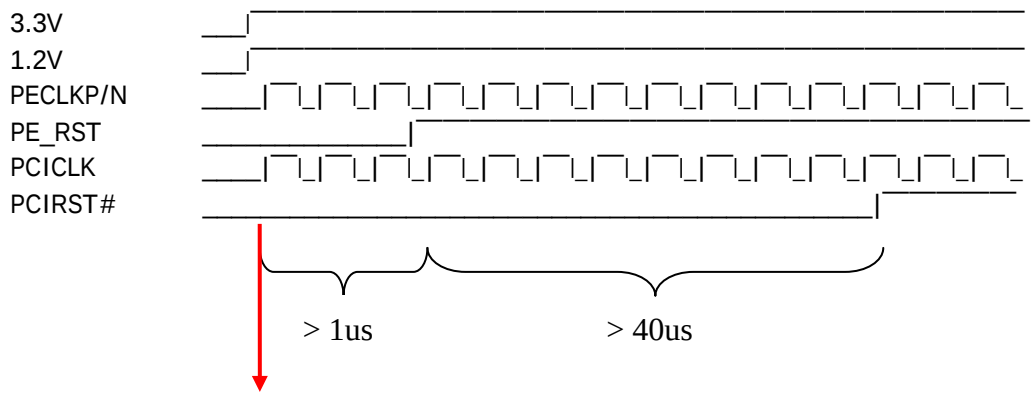
2. “PEWAKE#” signal of chipset can be directly connected with PCI device signal “PME#”. It implies PCI devices can wake up system directly.

3. PCLK1(GPIO1), PCLK2(GPIO2), PCLK3(GPIO3), PCLK4(GPIO4) can be disabled if there is no slot or onboard device if there is no slot or onboard device connected. It can save unnecessary power.

	CLOCK ON	CLKOCK OFF
PCLKO1	PCLK1EN = VCC or NC	PCLK1EN = GND
PCLKO2	PCLK2EN = VCC or NC	PCLK2EN = GND
PCLKO3	PCLK3EN = VCC or NC	PCLK3EN = GND
PCLKO4	PCLK4EN = VCC or NC	PCLK4EN = GND

4. About I2C bus. ASM1085 is a I2C master before PCIRST is released. To read table in EEPROM (if exist) to set vendor defined value into register area. It changes to a I2C slave for debugging after PCIRST is released.

5. Power/Reset/Clock sequence



1. No sequence among 3.3V, 1.2V, PECLKP/N and PCICLK, but be sure these four signals are ready before PE_RST is released.
2. PCIRST# will be released after PE_RST is released.

8. Register Description

Register Attribute	Definition
RO	**Read-only register**: Register bits are read-only and cannot be altered by software.
RW	**Read-Write register**: Register bits are read-write and may be either set or cleared by software to the desired state.
HwInit	**Hardware Initialized**: Register bits are initialized by firmware or hardware mechanisms such as pin strapping or serial EEPROM. Bits are read-only after initialization and can only be reset (for write-once by firmware) with Fundamental Reset.
RW1C	**Read-only status, Write-1-to-clear status register**: Register bits indicate status when read, a set bit indicating a status event may be cleared by writing a 1. Writing a 0 to RW1C bits has no effect.
ROS	**Sticky – Read-only register:** Registers are read-only and cannot be altered by software. Registers are not initialized or modified by hot reset.
RWS	**Sticky – Read-Write register**: Registers are read-write and may be either set or cleared by software to the desired state. Bits are not initialized or modified by hot reset.
RW1CS	**Sticky – Read-only status, Write-1-to-clear status register**: Registers indicate status when read, a set bit indicating a status event may be cleared by writing a 1. Writing a 0 to RW1CS bits has no effect. Bits are not initialized or modified by hot reset.
RWO	**Read-Write Once**: Register can only be written once
Rsvd	**Reserved:** Reserved for future RW

8.1 Regiater Mapping

Type1 Configuration Header Register				
31:24	23:16	15:8	7:0	Byte Offset
Device ID		Vendor ID		000h
Status		Command		004h
Class Code			Revision ID	008h
			Cache Line	00Ch
Base Address 0				010h
Base Address 1				014h
Sec Bus Latency	Sub Bus Number	Sec Bus Number	Prim Bus Number	018h
Secondary Status		I/O Limit	I/O Base	01Ch
Memory Limit		Memory Base		020h
Prefetchable Memory Limit		Prefetchable Memory Base		024h
Prefetchable Base Upper 32-bits				028h
Prefetchable Limit Upper 32-bits				02Ch
I/O Limit Upper 16-bits		I/O Base Upper 16-bits		030h
			Capabilities PTR	034h
Expansion ROM base address				038h

Bridge Control			Interrupt Pin	Interrupt Line	03Ch
MSI Capability Register					
31:24	23:16	15:8	7:0		Byte Offset
Message Control		Next Pointer	Capabilities ID		050h
Message Address					054h
Message Upper Address					058h
		Message Data			05Ch
Power Management Capability Register					
31:24	23:16	15:8	7:3	2:0	Byte Offset
Capabilities Register		Next Pointer	Capabilities ID		078h
Data	**PM Control / Status Bridge Extensions**	Power Management Status & Control			07Ch
PCI Express Capability Register					
31:24	23:16	15:8	7:0		Byte Offset
Capabilities Register		Next Pointer	Capabilities ID		080h
Device Capabilities					084h
Device Status		Device Control			088h
Link Capabilities					08Ch
Link Status		Link Control			090h
Slot Capabilities					094h
Slot Status		Slot Control			098h
SSID / SSVID Capability Register					
31:24	23:16	15:8	7:0		Byte Offset
		Next Pointer	Capabilities ID		0C0h
SSID		SSVID			0C4h
Virtual Channel Capability Register					
31:24	23:16	15:8	7:0		Byte Offset
Next Point & Version		Extended Capabilities ID			100h
		Port VC Capabilities 1			104h
VAT offset			VC arbit. cap		108h
Port VC Status		Port VC Control			10Ch
PAT offset 0	VC Resource Capability Register 0				110h
VC Resource Control Register 0					114h
VC Resource Status Register					118h
PCI Express AER Extended Capability Register					
31:24	23:16	15:8	7:0		Byte Offset
PCI Express Enhanced Capability Header					200h
Uncorrectable Error Status Register					204h
Uncorrectable Error Mask Register					208h
Uncorrectable Error Severity Register					20Ch
Correctable Error Status Register					210h
Correctable Error Mask Register					214h
Advanced Error Capabilities and Control Register					218h
Header Log Register					21Ch
					220h
					224h
					228h
Secondary Uncorrectable Error Status Register					22Ch
Secondary Uncorrectable Error Mask Register					230h
Secondary Uncorrectable Error Severity Register					234h
Secondary Error Capabilities and Control Register					238h

Secondary Header Log Register				23Ch
				240h
				244h
				248h
TOP Register				
31:24	23:16	15:8	7:0	Byte Offset
				260h
		Clock Control	Interrupt MAP	264h

8.2 Register Content

8.2.1 Type1 Configuration Header Registers

Register Name: Vendor ID
Address: OFFSET 00h
Size: 16 bits

Bit	Attrib	Description	Default
15:0	RO	Vendor ID	16'h 1B21

Register Name: Device ID
Address: OFFSET 02h
Size: 16 bits

Bit	Attrib	Description	Default
15:0	RO	Device ID	16'h 1080

Register Name: Command
Address: OFFSET 04h
Size: 16 bits

Bit	Attrib	Description	Default
15:11	Rsvd	Reserved	5'h00
10	RW	Interrupt Disable	0
9	RO	Fast Back-to-Back Transaction Enable	0
7	RW	SERR# Enable	0
6	RW	Parity Error Response	0
5	RO	VGA Palette Snoop	0
4	RW	Memory Write and Invalidate	0
3	RO	Special Cycle Enable	0
2	RW	Bus Master Enable	0
1	RW	Memory Space Enable	0
0	RW	I/O Space Enable	0

Register Name: Status
Address: OFFSET 06h
Size: 16 bits

Bit	Attrib	Description	Default
15	RW1C	Detected Parity Error	0
14	RW1C	Signaled System Error	0
13	RW1C	Received Master-Abort	0
12	RW1C	Received Target-Abort	0
11	RW1C	Signaled Target-Abort	0
10:9	RO	DEVSEL# Timing	0
8	RW1C	Master Data Parity Error	0
7	RO	Fast Back-to-Back Transaction Capable	0
6	Rsvd	Reserved	0
5	RO	66 MHz Capable	0
4	RO	Capabilities List	1
3	RO	Interrupt Status	0
2:0	Rsvd	Reserved	3'h0

Register Name: Class Code
Address: OFFSET 09h
Size: 24 bits

Bit	Attrib	Description	Default
23:16	RO	Class Code	8'h06
15:8	RO	Sub-Class Code	8'h04
7:0	RO	Programming Interface	8'h00

Register Name: Cache Line
Address: OFFSET 0Ch
Size: 8 bits

Bit	Attrib	Description	Default
7:0	RW	Cache Line	8'h00

Register Name: Base Address 0
Address: OFFSET 10h
Size: 32 bits

Bit	Attrib	Description	Default
31:0	RO	Base Address 0	32'h00000000

Register Name: Base Address 1
Address: OFFSET 14h
Size: 32 bits

Bit	Attrib	Description	Default
31:0	RO	Base Address 1	32'h00000000

Register Name: Primary Bus Number

Address: OFFSET 18h
Size: 8 bits

Bit	Attrib	Description	Default
7:0	RW	Primary Bus Number	8'h00

Register Name: Secondary Bus Number
Address: OFFSET 19h
Size: 8 bits

Bit	Attrib	Description	Default
7:0	RW	Secondary Bus Number	8'h00

Register Name: Subordinate Bus Number
Address: OFFSET 1Ah
Size: 8 bits

Bit	Attrib	Description	Default
7:0	RW	Subordinate Bus Number	8'h00

Register Name: Secondary Latency Timer
Address: OFFSET 1Bh
Size: 8 bits

Bit	Attrib	Description	Default
7:0	RW	Secondary Latency Timer	8'h00

Register Name: I/O Base and I/O Limit
Address: OFFSET 1Ch
Size: 16 bits

Bit	Attrib	Description	Default
15:8	RW	I/O Limit	8'h00
7:0	RW	I/O Base	8'h00

Register Name: Secondary Status
Address: OFFSET 1Eh
Size: 16 bits

Bit	Attrib	Description	Default
15	RW1C	Detected Parity Error	0
14	RW1C	Received System Error	0
13	RW1C	Received Master-Abort	0
12	RW1C	Received Target-Abort	0
11	RW1C	Signaled Target-Abort	0
10:9	RO	DEVSEL Timing	2'b00
8	RW1C	Master Data parity Error	0
7	RO	Fast Back-to-Back Transactions Capable	0

6	Rsvd	Reserved	0
5	RO	66 MHz Capable	1
4:0	Rsvd	Reserved	5'h00

Register Name: Memory Base and Memory Limit
Address: OFFSET 20h
Size: 32 bits

Bit	Attrib	Description	Default
31:16	RW	Memory Limit	16'h0000
15:0	RW	Memory Base	16'h0000

Register Name: Prefetchable Memory Base and Prefetchable Memory Limit
Address: OFFSET 24h
Size: 32 bits

Bit	Attrib	Description	Default
31:16	RW	Prefetchable Memory Limit	16'h0000
15:0	RW	Prefetchable Memory Base	16'h0000

Register Name: Prefetchable Base Upper 32-bits
Address: OFFSET 28h
Size: 32 bits

Bit	Attrib	Description	Default
31:0	RW	Prefetchable Base Upper 32-bits	32'h00000000

Register Name: Prefetchable Limit Upper 32-bits
Address: OFFSET 2Ch
Size: 32 bits

Bit	Attrib	Description	Default
31:0	RW	Prefetchable Limit Upper 32-bits	32'h00000000

Register Name: I/O Base Upper 16-bits and I/O Limit Upper 16bits
Address: OFFSET 30h
Size: 16 bits

Bit	Attrib	Description	Default
15:8	RW	I/O Limit Upper 16-bits	8'h00
7:0	RW	I/O Base Upper 16-bits	8'h00

Register Name: Capabilities Pointer

Address: OFFSET 34h
Size: 8 bits

Bit	Attrib	Description	Default
7:0	RO	Capabilities Pointer	8'h50

Register Name: Expansion ROM base address
Address: OFFSET 38h
Size: 32 bits

Bit	Attrib	Description	Default
31:0	RW	Expansion ROM base address	32'h00000000

Register Name: Interrupt Line
Address: OFFSET 3Ch
Size: 8 bits

Bit	Attrib	Description	Default
7:0	RW	Interrupt Line	8'h00

Register Name: Interrupt Pin
Address: OFFSET 3Dh
Size: 8 bits

Bit	Attrib	Description	Default
7:0	RO	Interrupt Pin	8'h01

Register Name: Bridge Control
Address: OFFSET 3Eh
Size: 16 bits

Bit	Attrib	Description	Default
15:12	Rsvd	Reserved	4'h0
11	RW	Discard Timer SERR# Enable	0
10	RW1C	Discard Timer Status	0
9	RW	Secondary Discard Timer	0
8	RO	Primary Discard Timer	0
7	RW	Fast Back-to-Back Enable	0
6	RW	Secondary Bus Reset	0
5	RW	Master-Abort Mode	0
4	RW	VGA 16-bt Decode	0
3	RW	VGA Enable	0
2	RW	ISA Enable	0
1	RW	SERR# Enable	0
0	RW	Parity Error Response Enable	0

8.2.2 Specific registers

Register Name: Hiding register
Address: OFFSET 40h
Size: 8 bits

Bit	Attrib	Description	Default
7	Rsvd	Reserved	
6	RW	Patch subtractive decode enable (Legacy enable)	1'b0
5	RW	Set zero on device number field with type1 configuration cycle	1'b1
4	RW	Reserved	
3	RW	Reserved	
2	RW	Hiding Device 2 : masking AD18	1'b0
1	RW	Hiding Device 1 : masking AD17	1'b0
0	RW	Hiding Device 0 : masking AD16	1'b0

Register Name: Legacy mode register
Address: OFFSET 41h
Size: 8 bits

Bit	Attrib	Description	Default
7	Rsvd	Reserved	
6	RW	Supported SSID/SSVID capability register set when legacy mode is enabled. 0: disable 1: enable	1'b0
5	RW	In legacy mode enable INTx message upward to TX when set 1 and offset 40[6] set 1.	1'b0
4	RW	In legacy mode enable PME message upward to TX when set 1 and offset 40[6] set 1.	1'b0
3	Rsvd	Reserved	
2	RW	PCI pad with internal pull-up resistance enable	1'b0
1	RW	Legacy policy configuration	1'b0
0	RW	Legacy policy configuration	1'b0

Register Name: GPIO PAD register
Address: OFFSET 44h
Size: 8 bits

Bit	Attrib	Description	Default
7	RW	GPIO7 PAD output	1'b0
6	RW	GPIO6 PAD output	1'b0
5	RW	GPIO5 PAD output	1'b0
4	RW	GPIO4 PAD output	1'b0
3	RW	GPIO7 PAD output enable	1'b0
2	RW	GPIO6 PAD output enable	1'b0
1	RW	GPIO5 PAD output enable	1'b0
0	RW	GPIO4 PAD output enable 0: input 1:output	1'b0

Register Name: GPIO PAD register
Address: OFFSET 45h
Size: 8 bits

Bit	Attrib	Description	Default
7:4	Rsvd	Reserved	
3	RO	GPIO7 PAD input	1'b0
2	RO	GPIO6 PAD input	1'b0
1	RO	GPIO5 PAD input	1'b0
0	RO	GPIO4 PAD input	1'b0

8.2.3 MSI Capability Registers

Register Name: Capabilities ID
Address: OFFSET 50h
Size: 8 bits

Bit	Attrib	Description	Default
7:0	RO	Capabilities ID	8'h05

Register Name: Next Pointer
Address: OFFSET 51h
Size: 8 bits

Bit	Attrib	Description	Default
7:0	RO	Next Pointer	8'h78

Register Name: Message Control
Address: OFFSET 52h
Size: 16 bits

Bit	Attrib	Description	Default
15:8	Rsvd	Reserved	16'h0000
7	RO	64-bit Address Capable	1
6:4	RW	Multiple Message Enable	3'h0
3:1	RO	Multiple Message Capable	3'h0
0	RW	MSI Enable	0

Register Name: Message Address
Address: OFFSET 54h
Size: 32 bits

Bit	Attrib	Description	Default
31:0	RW	Message Address	32'h00000000

Register Name: Message Upper Address
Address: OFFSET 58h
Size: 32 bits

Bit	Attrib	Description	Default
31:0	RW	Message Upper Address	32'h00000000

Register Name: Message Data
Address: OFFSET 5Ch
Size: 16 bits

Bit	Attrib	Description	Default
15:0	RW	Message Data	16'h0000

8.2.4 Power Management Capability Registers

Register Name: Capabilities ID
Address: OFFSET 78h
Size: 8 bits

Bit	Attrib	Description	Default
7:0	RO	Capabilities ID	8'h01

Register Name: Next Pointer
Address: OFFSET 79h
Size: 8 bits

Bit	Attrib	Description	Default
7:0	RO	Next Pointer	8'h80

Register Name: Power Management Capabilities
Address: OFFSET 7Ah
Size: 16 bits

Bit	Attrib	Description	Default
15:11	RO	PME Support Bit[11] D0 support PME message Bit[12] D1 support PME message Bit[13] D2 support PME message Bit[14] D3(hot) support PME message Bit[15] D3(cold) support PME message	5'h1F
10	RO	D2 Support	1
9	RO	D1 Support	1
8:6	RO	Aux Current	3'b000
5	RO	Device-Specific Initialization	1
4	Rsvd	Reserved	0
3	RO	PME Clock	0
2:0	RO	PCI PM spec. 1.2	3'b011

Register Name: Power Management Control and Status
Address: OFFSET 7Ch
Size: 32 bits

Bit	Attrib	Description	Default
31:24	Rsvd	Reserved	8'h00
23	RO	BPCC_EN	0
22	RO	B2_B3#	0
21:16	Rsvd	Reserved	5'h00
15	RW1C	PME Status	0
14:13	RO	Data Scale	2'b00
12:9	RW	Data Scale	4'h0
8	RW	PME Enable	0
7:4	Rsvd	Reserved	0

3	RW	No Soft Reset	1
2	Rsvd	Reserved	0
1:0	RW	Power State Bit[1:0] = 2'b00 PMState D0 Bit[1:0] = 2'b01 PMState D1 Bit[1:0] = 2'b10 PMState D2 Bit[1:0] = 2'b11 PMState D3	2'b00

8.2.5 PCI Express Capability Registers

Register Name: Capabilities ID
Address: OFFSET 80h
Size: 8 bits

Bit	Attrib	Description	Default
7:0	RO	Capabilities ID	8'h10

Register Name: Next Pointer
Address: OFFSET 81h
Size: 8 bits

Bit	Attrib	Description	Default
7:0	RO	Next Pointer	8'hC0

Register Name: Capabilities Registers
Address: OFFSET 82h
Size: 16 bits

Bit	Attrib	Description	Default
15:14	Rsvd	Reserved	2'b00
13:9	RO	Interrupt Message Number	5'h00
8	RO	Slot Implemented	0
7:4	RO	Device Port Type	4'h7
3:0	RO	Capability Version	4'h1

Register Name: Capabilities Registers
Address: OFFSET 84h
Size: 32 bits

Bit	Attrib	Description	Default
31:28	Rsvd	Reserved	4'h0
27:26	RO	Captured Slot Power Limit Scale	2'b00
25:18	RO	Captured Slot Power Limit Value	8'h00
16:17	Rsvd	Reserved	2'b00
15	RO	Role-Base Error Reporting	1
14	RO	Power Indicator Present	0
13	RO	Attention Indicator Present	0
12	RO	Attention Button Present	0
11:9	RO	Endpoint L1 Acceptable Latency	3'b000

8:6	RO	Endpoint L0s Acceptable Latency	3'b000
5	RO	Extended Tag Field Supported	0
4:3	RO	Phantom Function Supported	2'b00
2:0	RO	Max Payload Size Supported	3'b000

Register Name: Device Control
Address: OFFSET 88h
Size: 16 bits

Bit	Attrib	Description	Default
15	RW	Bridge Configuration Retry Enable	0
14:12	RW	Max Read Request Size	3'b010
11	RW	Enable No Snoop	1
10	RW	Auxiliary (AUX) Power PM Enable	0
9	RW	Phantom Function Enable	0
8	RW	Extended Tag Field Enable	0
7:5	RW	Max Payload Size	3'b000
4	RW	Enable Relaxed Ordering	1
3	RW	Unsupported Request (UR) Reporting Enable	0
2	RW	Fatal Error Reporting Enable	0
1	RW	Non-Fatal Error Reporting Enable	0
0	RW	Correctable Error Reporting Enable	0

Register Name: Device Status
Address: OFFSET 8Ah
Size: 16 bits

Bit	Attrib	Description	Default
15:6	Rsvd	Reserved	10'h000
5	RO	Transactions Pending	0
4	RO	Aux Power Detected	0
3	RW1C	Unsupported Request (UR) Detected	0
2	RW1C	Fatal Error Detected	0
1	RW1C	Non-Fatal Error Detected	0
0	RW1C	Correctable Error Detected	0

Register Name: Link Capabilities
Address: OFFSET 8Ch
Size: 32 bits

Bit	Attrib	Description	Default
31:24	RO	Port Number	8'h01
23:21	Rsvd	Reserved	3'b000

20	RO	Data Link Layer Link Active Reporting Capable	0
19	RO	Surprise Down Error Reporting capable	0
18	RO	Clock Power Management	0
17:15	RO	L1 Exit Latency	3'b001
14:12	RO	L0s Exit Latency	3'b101
11:10	RO	Active State Power Management (ASPM) Support	2'b11
9:4	RO	Maximum Link Width	6'h01
3:0	RO	Maximum Link Speed	4'h1

Register Name: Link Control
Address: OFFSET 90h
Size: 16 bits

Bit	Attrib	Description	Default
15:9	Rsvd	Reserved	7'h00
8	RW	Enable Clock Power Management	0
7	RW	Extended Sync.	0
6	RW	Common Clock Configuration	0
5	RO	Retrain Link	0
4	RW	Link Disable	0
3	RW	Read Completion Boundary (RCB)	0
2	Rsvd	Reserved	0
1:0	RW	Active State Power Management (ASPM) Control Bit[1:0] = 2'b00 Disable ~~Bit[1:0] = 2'b01 L0s Entry Enable~~ ~~Bit[1:0] = 2'b10 L1 Entry Enable~~ ~~Bit[1:0] = 2'b11 L0s and L1 Entry Enable~~	2'b00

Register Name: Link Status
Address: OFFSET 92h
Size: 16 bits

Bit	Attrib	Description	Default
15:14	Rsvd	Reserved	2'b00
13	RO	Data Link Layer Link Active	0
12	RO	Slot Clock Configuration	0
11	RO	Link Training	0
10	RO	Training Error	0
9:4	RO	Negotiated Link Width	0
3:0	RO	Link Speed	4'h1

Register Name: Slot Capabilities
Address: OFFSET 94h
Size: 32 bits

Bit	Attrib	Description	Default
31:19	Rsvd	Reserved	13'h0000
18	RO	No Command Completed Support	0
17	RO	Electromechanical Interlock Present	0
16:15	RO	Slot Power Limit Scale	2'b00
14:7	RO	Slot Power Limit Value	8'h00
6	RO	Hot Plug Capable	0
5	RO	Hot Plug Surprise	0
4	RO	Power Indicator Present	0
3	RO	Attention Indicator Present	0
2	RO	MRL Sensor Present	0
1	RO	Power Controller Present	0
0	RO	Attention Button Present	0

Register Name: Slot Control
Address: OFFSET 98h
Size: 16 bits

Bit	Attrib	Description	Default
15:13	Rsvd	Reserved	3'b000
12	RW	Data Link Layer State Changed Enable	0
11	RO	Electromechanical Interlock Control	0
10	RW	Power Controller Control	0
9:8	RW	Power indicator Control	2'b11
7:6	RW	Attention Indicator Control	2'b11
5	RW	Hot Plug Interrupt Enable	0
4	RW	Command Completed Interrupt Enable	0
3	RW	Presence Detect Changed Enable	0
2	RW	MRL Sensor Changed Enable	0
1	RW	Power Fault Detected Enable	0
0	RW	Attention Button Pressed Enable	0

Register Name: Slot Status
Address: OFFSET 9Ah
Size: 16 bits

Bit	Attrib	Description	Default
15:9	Rsvd	Reserved	7'h00
8	RW	Data Link Layer State Changed	0
7	RW	Electromechanical Interlock status	0
6	RW	Presence Detect State	0
5	RW	MRL Sensor State	0
4	RW1C	Command Completed	0
3	RW1C	Presence Detect Changed	0
2	RW1C	MRL Sensor Changed	0
1	RW1C	Power Controller Detected	0

0	RW1C	Attention Button Pressed	0

8.2.6 SSID / SSVID Capability Registers

Register Name: Capabilities ID
Address: OFFSET C0h
Size: 8 bits

Bit	Attrib	Description	Default
7:0	RO	Capabilities ID	8'h0D

Register Name: Next Pointer
Address: OFFSET C1h
Size: 8 bits

Bit	Attrib	Description	Default
7:0	RO	Next Pointer	8'h00

Register Name: SSVID
Address: OFFSET C4h
Size: 16 bits

Bit	Attrib	Description	Default
15:0	RO	SubSystem Vender ID	16'h0000

Register Name: SSID
Address: OFFSET C6h
Size: 8 bits

Bit	Attrib	Description	Default
15:0	RO	SubSystem ID	16'h0000

8.2.7 Virtual Channel Capability Registers

Register Name: Extended Capabilities ID
Address: OFFSET 100h
Size: 16 bits

Bit	Attrib	Description	Default
15:0	RO	Extended Capabilities ID	16'h0002

Register Name: Next Pointer and Version
Address: OFFSET 102h
Size: 16 bits

Bit	Attrib	Description	Default
15:4	RO	Next Capability offset	12'h200
3:0	RO	Capability Version	4'h1

Register Name: Port VC Capability Register 1
Address: OFFSET 104h
Size: 16 bits

Bit	Attrib	Description	Default
15:12	Rsvd	Reserved	4'h0
11:10	RO	Port Arbitration Table Entry Size	2'b00
9:8	RO	Reference Clock	2'b00
7	Rsvd	Reserved	0
6:4	RO	Low Priority Extended VC Count	3'b000
3	Rsvd	Reserved	0
2:0	RO	Extended VC Count	8'h00

Register Name: VC Arbitration Capability
Address: OFFSET 108h
Size: 8 bits

Bit	Attrib	Description	Default
7:0	RO	VC Arbitration Capability	8'h00

Register Name: VC Arbitration Table Offset
Address: OFFSET 10Bh
Size: 8 bits

Bit	Attrib	Description	Default
7:0	RO	VC Arbitration Table Offset	8'h00

Register Name: Port VC Control
Address: OFFSET 10Ch
Size: 16 bits

Bit	Attrib	Description	Default

15:4	Rsvd	Reserved	12'h000
3:1	RW	VC Arbitration Select	3'b000
0	RW	Load VC Arbitration Table	0

Register Name: Port VC Status
Address: OFFSET 10Eh
Size: 16 bits

Bit	Attrib	Description	Default
15:1	Rsvd	Reserved	15'h0000
0	RO	VC Arbitration Table Status	0

Register Name: VC Resource Capability Register 0
Address: OFFSET 110h
Size: 24 bits

Bit	Attrib	Description	Default
23	Rsvd	Reserved	0
22:16	RO	Maximum Time Slots	7'h00
15	RO	Reject Snoop Transactions	0
14	RO	Advanced Packet Switching	0
13:8	Rsvd	Reserved	6'h00
7:0	RO	Port Arbitration Capability	8'h00

Register Name: Port Arbitration Table Offset 0
Address: OFFSET 113h
Size: 8 bits

Bit	Attrib	Description	Default
7:0	RO	Port Arbitration Table Offset	8'h00

Register Name: VC Resource Control Register 0
Address: OFFSET 114h
Size: 32 bits

Bit	Attrib	Description	Default
31	RW	VC Enable	1
30:27	Rsvd	Reserved	4'h0
26:24	RW	VC ID	3'b000
23:20	Rsvd	Reserved	4'h0
19:17	RW	Port Arbitration Select	3'b000
16	RW	Load Port Arbitration Table	0
15:8	Rsvd	Reserved	12'h000
7:0	RW	TC/VC Map	8'hFF

Register Name: VC Resource Status Register 0
Address: OFFSET 11Ah
Size: 16 bits

Bit	Attrib	Description	Default
15:2	Rsvd	Reserved	14'h0000
1	RO	VC Negotiation Pending	1
0	RO	Port Arbitration Table Status	0

8.2.8 PCI Express AER Extended Capability Registers

Register Name: Extended Capabilities ID
Address: OFFSET 200h
Size: 16 bits

Bit	Attrib	Description	Default
15:0	RO	Extended Capabilities ID	16'h0001

Register Name: Next Pointer and Version
Address: OFFSET 102h
Size: 16 bits

Bit	Attrib	Description	Default
15:4	RO	Next Capability offset	12'h000
3:0	RO	Capability Version	4'h1

Register Name: Uncorrectable Error Status
Address: OFFSET 204h
Size: 32 bits

Bit	Attrib	Description	Default
31:21	Rsvd	Reserved	11'h000
20	RW1C	Unsupported Request Error Status	0
19	RW1C	ECRC Error Status	0
18	RW1C	Malformed TLP Status	0
17	RW1C	Receiver Overflow Status	0
16	RW1C	Unexpected Completion Status	0
15	RW1C	Completer Abort Status	0
14	RW1C	Completion Timeout Status	0
13	RW1C	Flow Control Protocol Error Status	0
12	RW1C	Poisoned TLP Status	0
11:5	Rsvd	Reserved	7'h00
4	RW1C	Data Link Protocol Error Status	0
3:1	Rsvd	Reserved	4'h0
0	Undef	Undefined	Undefined

Register Name: Uncorrectable Error Mask
Address: OFFSET 208h
Size: 32 bits

Bit	Attrib	Description	Default
31:21	Rsvd	Reserved	11'h000
20	RW	Unsupported Request Error Mask	0
19	RW	ECRC Error Mask	0
18	RW	Malformed TLP Mask	0
17	RW	Receiver Overflow Mask	0
16	RW	Unexpected Completion Mask	0
15	RW	Completer Abort Mask	0
14	RW	Completion Timeout Mask	0
13	RW	Flow Control Protocol Error Mask	0
12	RW	Poisoned TLP Mask	0

11:5	Rsvd	Reserved	7'h00
4	RW	Data Link Protocol Error Mask	0
3:1	Rsvd	Reserved	4'h0
0	Undef	Undefined	Undefined

Register Name: Uncorrectable Error Severity
Address: OFFSET 20Ch
Size: 32 bits

Bit	Attrib	Description	Default
31:21	Rsvd	Reserved	11'h000
20	RW	Unsupported Request Error Severity	0
19	RW	ECRC Error Severity	0
18	RW	Malformed TLP Severity	1
17	RW	Receiver Overflow Severity	1
16	RW	Unexpected Completion Severity	0
15	RW	Completer Abort Severity	0
14	RW	Completion Timeout Severity	0
13	RW	Flow Control Protocol Error Severity	1
12	RW	Poisoned TLP Severity	0
11:5	Rsvd	Reserved	7'h00
4	RW	Data Link Protocol Error Severity	1
3:1	Rsvd	Reserved	4'h0
0	Undef	Undefined	Undefined

Register Name: Correctable Error Status
Address: OFFSET 210h
Size: 32 bits

Bit	Attrib	Description	Default
31:14	Rsvd	Reserved	18'h00000
13	RW1C	Advisory Non-Fatal Error Status	0
12	RW1C	Replay Timer Timeout Status	0
11:9	Rsvd	Reserved	3'b000
8	RW1C	REPLAY_NUM Rollover Status	0
7	RW1C	Bad DLLP Status	0
6	RW1C	Bad TLP Status	0
5:1	Rsvd	Reserved	5'h00
0	RW1C	Receiver Error Status	0

Register Name: Correctable Error Mask
Address: OFFSET 214h
Size: 32 bits

Bit	Attrib	Description	Default
31:14	Rsvd	Reserved	18'h00000
13	RW	Advisory Non-Fatal Error Mask	1
12	RW	Replay Timer Timeout Mask	0
11:9	Rsvd	Reserved	3'b000
8	RW	REPLAY_NUM Rollover Mask	0
7	RW	Bad DLLP Mask	0
6	RW	Bad TLP Mask	0

5:1	Rsvd	Reserved	5'h00
0	RW1C	Receiver Error Mask	0

Register Name: Advanced Error Capabilities and Control
Address: OFFSET 218h
Size: 32 bits

Bit	Attrib	Description	Default
31:9	Rsvd	Reserved	23'b000000
8	RW	ECRC Check Enable	0
7	RO	ECRC Check Capable	0
6	RW	ECRC Generation Enable	0
5	RO	ECRC Generation Capable	0
4:0	RO	First Error Pointer	5'h00

Register Name: Header Log Register
Address: OFFSET 21Ch
Size: 128 bits

Bit	Attrib	Description	Default
127:0	RO	Header of TLP Associated with Error	128'h0

Register Name: Secondary Uncorrectable Error Status
Address: OFFSET 22Ch
Size: 32 bits

Bit	Attrib	Description	Default
31:14	Rsvd	Reserved	18'h00000
13	RW1C	Internal Bridge Error Status	0
12	RW1C	SERR# Assertion Detected	0
11	RW1C	PERR# Assertion Detected	0
10	RW1C	Delayed Transaction Discard Timer Expired Status	0
9	RW1C	Uncorrectable Address Error Status	0
8	RW1C	Uncorrectable Attribute Error Status	0
7	RW1C	Uncorrectable Data Error Status	0
6	RW1C	Uncorrectable Split Completion Message Data Error Status	0
5	RW1C	Unexpected Split Completion Error Status	0
4	Rsvd	Reserved	0
3	RW1C	Received Master-Abort Status	0
2	RW1C	Received Target-Abort Status	0
1	RW1C	Master-Abort on Split Completion Status	0
0	RW1C	Target-Abort on Split Completion Status	0

Register Name: Secondary Uncorrectable Error Mask
Address: OFFSET 230h
Size: 32 bits

Bit	Attrib	Description	Default
31:14	Rsvd	Reserved	18'h00000
13	RW	Internal Bridge Error Mask	0
12	RW	SERR# Assertion Detected Mask	1
11	RW	PERR# Assertion Detected Mask	0
10	RW	Delayed Transaction Discard Timer Expired Mask	1
9	RW	Uncorrectable Address Error Mask	1
8	RW	Uncorrectable Attribute Error Mask	1
7	RW	Uncorrectable Data Error Mask	1
6	RW	Uncorrectable Split Completion Message Data Error Mask	0
5	RW	Unexpected Split Completion Error Mask	1
4	Rsvd	Reserved	0
3	RW	Received Master-Abort Mask	1
2	RW	Received Target-Abort Mask	0
1	RW	Master-Abort on Split Completion Mask	0
0	RW	Target-Abort on Split Completion Mask	0

Register Name: Secondary Uncorrectable Error Severity
Address: OFFSET 234h
Size: 32 bits

Bit	Attrib	Description	Default
31:14	Rsvd	Reserved	18'h00000
13	RW	Internal Bridge Error Severity	0
12	RW	SERR# Assertion Detected Severity	1
11	RW	PERR# Assertion Detected Severity	0
10	RW	Delayed Transaction Discard Timer Expired Severity	0
9	RW	Uncorrectable Address Error Severity	1
8	RW	Uncorrectable Attribute Error Severity	1
7	RW	Uncorrectable Data Error Severity	0
6	RW	Uncorrectable Split Completion Message Data Error Severity	1
5	RW	Unexpected Split Completion Error Severity	0
4	Rsvd	Reserved	0
3	RW	Received Master-Abort Severity	0
2	RW	Received Target-Abort Severity	0
1	RW	Master-Abort on Split Completion Severity	0

0	RW	Target-Abort on Split Completion Severity	0

Register Name: Secondary Advanced Error Capabilities and Control
Address: OFFSET 238h
Size: 32 bits

Bit	Attrib	Description	Default
31:5	Rsvd	Reserved	27'h000000
4:0	RO	Secondary Uncorrectable First Error Pointer	5'h00

Register Name: Secondary Header Log Register
Address: OFFSET 23Ch
Size: 128 bits

Bit	Attrib	Description	Default
127:64	RO	Transaction Address	64'h0
63:44	Rsvd	Reserved	20'h00000
43:40	RO	Transaction Command Upper	4'h0
39:36	RO	Transaction Command Lower	4'h0
35:0	RO	Transaction Attribute	36'h0

8.2.9 MISC Register

Register Name: PCI Interrupt Mapping
Address: OFFSET 264h
Size: 8 bits

Bit	Attrib	Description	Default
7:2	Rsvd	Reserved	6'h0
1:0	RW	Interrupt mapping to INTx Virtual Wires	2'b00

Device Number	Register Option	Interrupt Signals	Mapping to INTx Virtual Wires
i*4; i=0~12	Interrupt mapping=00	INTA#	INTxA
i*4; i=0~12	Interrupt mapping=00	INTB#	INTxB
i*4; i=0~12	Interrupt mapping=00	INTC#	INTxC
i*4; i=0~12	Interrupt mapping=00	INTD#	INTxD
i*4+1; i=0~12	Interrupt mapping=01	INTA#	INTxB
i*4+1; i=0~12	Interrupt mapping=01	INTB#	INTxC
i*4+1; i=0~12	Interrupt mapping=01	INTC#	INTxD
i*4+1; i=0~12	Interrupt mapping=01	INTD#	INTxA
i*4+2; i=0~12	Interrupt mapping=10	INTA#	INTxC
i*4+2; i=0~12	Interrupt mapping=10	INTB#	INTxD
i*4+2; i=0~12	Interrupt mapping=10	INTC#	INTxA
i*4+2; i=0~12	Interrupt mapping=10	INTD#	INTxB
i*4+3; i=0~12	Interrupt mapping=11	INTA#	INTxD
i*4+3; i=0~12	Interrupt mapping=11	INTB#	INTxA
i*4+3; i=0~12	Interrupt mapping=11	INTC#	INTxB
i*4+3; i=0~12	Interrupt mapping=11	INTD#	INTxC

Register Name: TOP Clock control option
Address: OFFSET 265h
Size: 8 bits

Bit	Attrib	Description	Default
7	RW	Dynamic Clock	0
6:0	Rsvd	Reserved	6'h0

9 Electrical Characteristics

9.1 Recommand Operation Condition

Terminals	Operation	Min	Typ	Max	Unit	Remark
VCC33	3.3V	3	3.3	3.6	V	
VCC33P	3.3V	3	3.3	3.6	V	
VCC12	1.2V	1.08		1.32	V	
VCCP	1.2V	1.08		1.32	V	
	Temperature	0	25	70	°C	

9.2 PCI Express Differential Transmitter Output Ranges

Terminals	Parameter	Min	Typ	Max	Unit	Remark
PTXP PTXN	Unit Interval (UI)	399.88	400	400.12	ps	300PPM, no SSC included
PTXP PTXN	VTX-DIFFp-p Differential peak-to-peak output voltage	0.8		1.2	V	
PTXP PTXN	VTX-DE-RATIO De-emphasized differential output voltage (ratio)	-3.0	-3.5	-4.0	dB	This is the ratio of the VTX-DIFFp-p of the second and following bits after a transition divided by the VTX-DIFFp-p of the first bit after a transition.
PTXP PTXN	TTX-RISE, TTX-FALL P/N TX output rise/fall time	0.125			UI	
PTXP PTXN	VTX-CM-ACp RMS ac peak common mode output voltage			20	mV	
PTXP PTXN	VTX-CM-DC-ACTIVE-IDLE DELTA Absolute delta of dc common mode voltage during L0 and electrical idle	0		100	mV	
PTXP PTXN	VTX-CM-DC-LINE-DELTA Absolute delta of dc common mode voltage between P and N	0		25	mV	
PTXP PTXN	VTX-IDLE-DIFFp Electrical idle differential peak output voltage	0		20	mV	
PTXP PTXN	VTX-RCV-DETECT The amount of voltage change allowed during receiver detection			600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present.
PTXP PTXN	VTX-DC-CM The TX dc common mode voltage	0		3.6	V	The allowed dc common mode voltage under any condition
PTXP PTXN	TTX-IDLE-SET-to-IDLE Maximum time to transition to a valid electrical idle after sending an electrical			20	UI	After sending an electrical idle ordered set, the transmitter must meet all electrical idle specifications within this time. This is considered a debounce time for

Terminals	Parameter	Min	Typ	Max	Unit	Remark
	idle ordered set					the transmitter to meet electrical idle after transitioning from L0.
PTXP PTXN	TTX-IDLE-to-DIFF-DATA Maximum time to transition to valid TX specifications after leaving an electrical idle Condition			20	UI	Maximum time to meet all TX specifications when transitioning from electrical idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving electrical idle.
PTXP PTXN	RLTX-DIFF Differential return loss	10			dB	
PTXP PTXN	RLTX-CM Common mode return loss	6			dB	
PTXP PTXN	ZTX-DIFF-DC DC differential TX impedance	80	100	120	Ω	TX dc differential mode low impedance
PTXP PTXN	ZTX-DC Transmitter dc impedance	40			Ω	Required PTXP as well as PTXN dc impedance during all states
PTXP PTXN	CTX AC coupling capacitor	75		200	nF	All transmitters are ac-coupled and are required on the PWB.

9.3 PCI Express Differential Receiver Input Ranges

Terminals	Parameter	Min	Typ	Max	Unit	Remark
PRXP PRXN	Unit Interval (UI)	399.88	400	400.12	ps	300PPM, no SSC included
PRXP PRXN	VTX-DIFFp-p Differential peak-to-peak output voltage	0.175		1.2	V	
PRXP PRXN	VRX-CM-ACp AC peak common mode input voltage			150	mV	
PRXP PRXN	RLRX-DIFF Differential return loss	10			dB	
PRXP PRXN	RLRX-CM Common mode return Loss	6			dB	
PRXP PRXN	ZRX-DIFF-DC DC differential input impedance	80	100	120	Ω	RX dc differential mode impedance
PRXP PRXN	ZRX-DC DC input impedance	40	50	60	Ω	Required PRXP as well as PRXN dc impedance (50 ∧ ±20% tolerance)
PRXP PRXN	ZRX-HIGH-IMP-DC Powered down dc input Impedance	200K			Ω	Required PRXP as well as PRXN dc impedance when the receiver terminations do not have power.
PRXP PRXN	VRX-IDLE-DET-DIFFp-p Electrical idle detect Threshold	65		175	mV	measured at the receiver package terminals
PRXP PRXN	TRX-IDLE-DET-DIFF-ENTER-TIME Unexpected electrical idle enter detect threshold integration time			10	ms	

9.4 PCI Express Differential Reference Clock Input Ranges

Terminals	Parameter	Min	Typ	Max	Unit	Remark

subject to change without notice

Terminals	Parameter	Min	Typ	Max	Unit	Remark
PECLKP **PECLKN**	fIN-DIFF Differential input frequency		100		MHz	The input frequency is 100 MHz + 300 ppm and − 2800 ppm including SSC-dictated variations.
PECLKP **PECLKN**	VRX-DIFFp-p Differential input peak-to-peak voltage	0.175		1.2	V	
PECLKP	VIH-SE	0.7 * VCC33P		VCC33P	V	Single-ended, reference clock mode high-level input voltage
PECLKP	VIL-SE	VCC33P		0.3 * VCC33P	V	Single-ended, reference clock mode low-level input voltage
PECLKP **PECLKN**	VRX-CM-ACp AC peak common mode input voltage			140	mV	
PECLKP **PECLKN**	Duty cycle	40		60	%	Differential and single-ended waveform input duty cycle
PECLKP **PECLKN**	ZRX-DIFF-DC DC differential input impedance		20		kΩ	REFCLK+/− dc differential mode impedance
PECLKP **PECLKN**	ZRX-DC DC input impedance		20		kΩ	REFCLK+ dc single-ended mode impedance

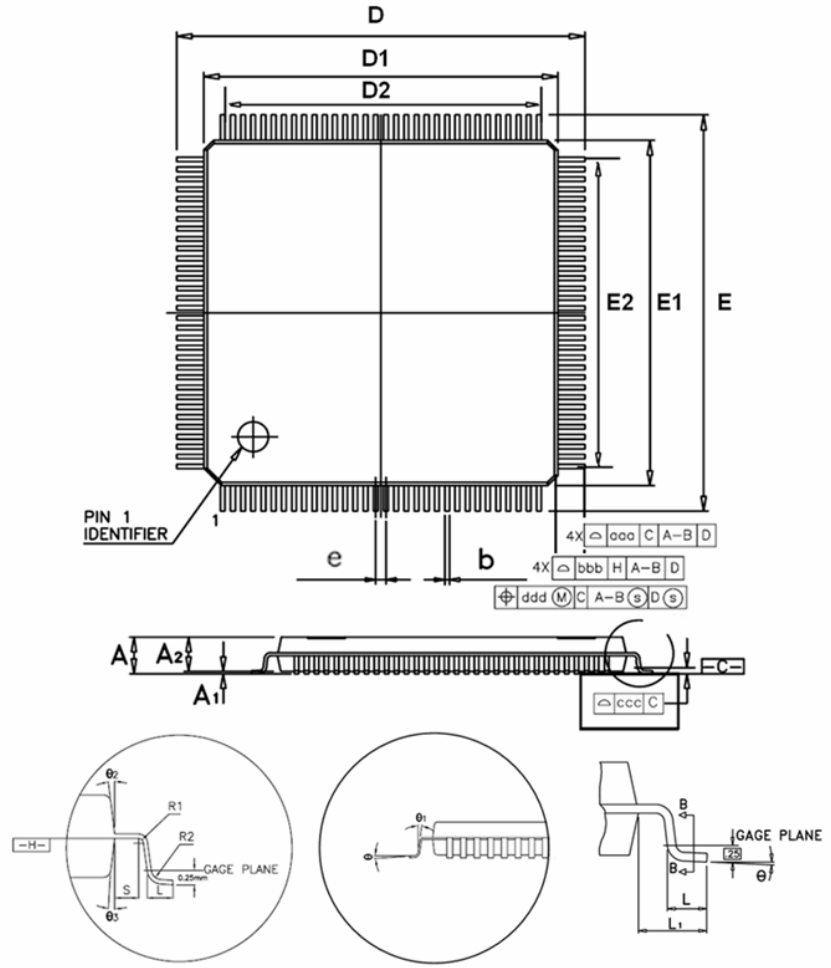
9.5 PCI Bus Electrical Characteristics

Parameter	Min	Max	Unit	Operation
VIH High-level input voltage	0.5 * VCC33	VCC33	V	VCC33
VIL Low-level input voltage	0	0.3 * VCC33	V	VCC33
VI Input voltage	0	VCC33	V	
VO Output voltage	0	VCC33	V	
VOH High-level output voltage	0.7 * VCC33		V	VCC33
VOL Low-level output voltage		0.18 * VCC33	V	VCC33
IOZ High-impedance, output current		10	uA	VCC33
II Input current		10	uA	VCC33

10 Power Consumption

	3.3V	1.2V
Min. Power	70mA	100mA
Max. Power	90mA	115mA

11 Package Information



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

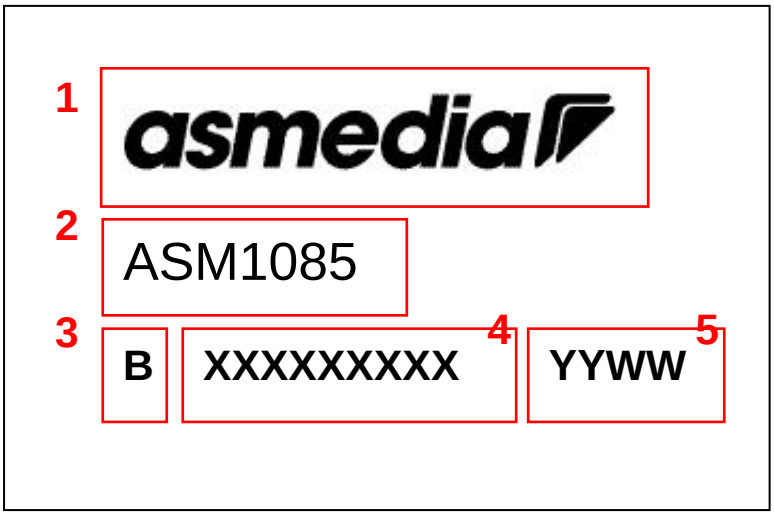
SYMBOL	128L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
D2	12.40			0.488		
E2	12.40			0.488		
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUN PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm and 0.5mm PITCH PACKAGES.
3. ALL DIMENSION OF 128L WERE BASE ON THOSE OF 120L SINCE THEY ARE NOT MENTIONED IN JEDEC SPEC MS-026.

Figure 3: Mechanical Specification – LQFP 128L

Marking Information



1. asmedia: ASMedia Logo
2. ASM1085: Product Name
3. B: Version of ASMedia Logo
4. XXXXXXXXX: Serial No. Reserved for Vendor
5. YYWW: Date Code