

# ASM1061 Data Sheet

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PCI Express 2.0 to SATA 6Gbps Controller

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**Environmentally hazardous materials are not used in this product.**

## Revision History

Rev.	Date	Description
0.1	June 11, 2010	Initial Release
0.2	June 21, 2011	Update the dimension of package
0.3	Nov. 24, 2010	Change internal regulator status to TBD Change 1.2V to 1.25V
0.4	Dec. 22, 2010	Remove TBD description for internal regulator Update XTAL Spec.
1.0	Feb. 9, 2011	Formal Release
1.1	Feb. 11, 2011	Update the Crystal electrical spec.
1.2	Feb. 14, 2011	Add Top Marking information
1.3	March.28, 2011	Update the electrical spec of PCI Express CLK
1.4	Aug. 16, 2011	Add the maximum Tc spec Add the timing spec of power on sequence
1.5	Aug. 22, 2011	Update the timing spec of power on sequence
1.6	Oct. 4, 2011	Update the case temperature and Power Supply specification
1.7	Dec. 12, 2011	Add the electrical spec of internal switching regulator spec
1.8	April 16, 2012	Update the electrical spec of operating case temperature

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## 1. General Description

Engaged in High Speed I/O solution development, Asmedia Technology is committed to enlarging product portfolio with introducing PCI Express Products. The ASM1061, X1 PCI Express Gen2 to two-ports Serial ATA Controller, enables Serial ATA PHY up to 6Gbps high speed interface, following Serial ATA Revision 3.0 Specification.

## 2. Features

### General Features

- Option Rom support through 64K Byte SPI flash
- 20MHz external crystal
- Integrated 3.3V to 1.25V switch regulator
- 3.3V and 1.25V Power Supply
- Industry Specifications Compliance:
  - PCI Express Base Specification Rev. 2.0
  - PCI Express Card Electromechanical Rev. 2.0
  - Serial ATA AHCI Spec. Rev.1.3
  - Serial ATA Revision 3.0
- 7mmx7mm 48-pin QFN package
- Green Package with RoHS Compliance

### PCI Express Features

- One lane PCI Express for 2.5 and 5GHz signaling
- Single virtual channel
- SSC support
- ECRC and Advanced Error Reporting capability
- 100MHz differential PCI Express reference clock in
- Maximum Payload up to 128 bytes

### Serial ATA Features

- 2 ports Serial ATA PHY for 1.5, 3.0 and 6.0GHz signaling
- Support IDE/AHCI mode
- Support Native Command Queue (NCQ)
- Support Gen1m and Gen2m SATA PHY
- Support Port Multiplier

## Package Type

- ◇ QFN 48L

### 3. Functional Diagram

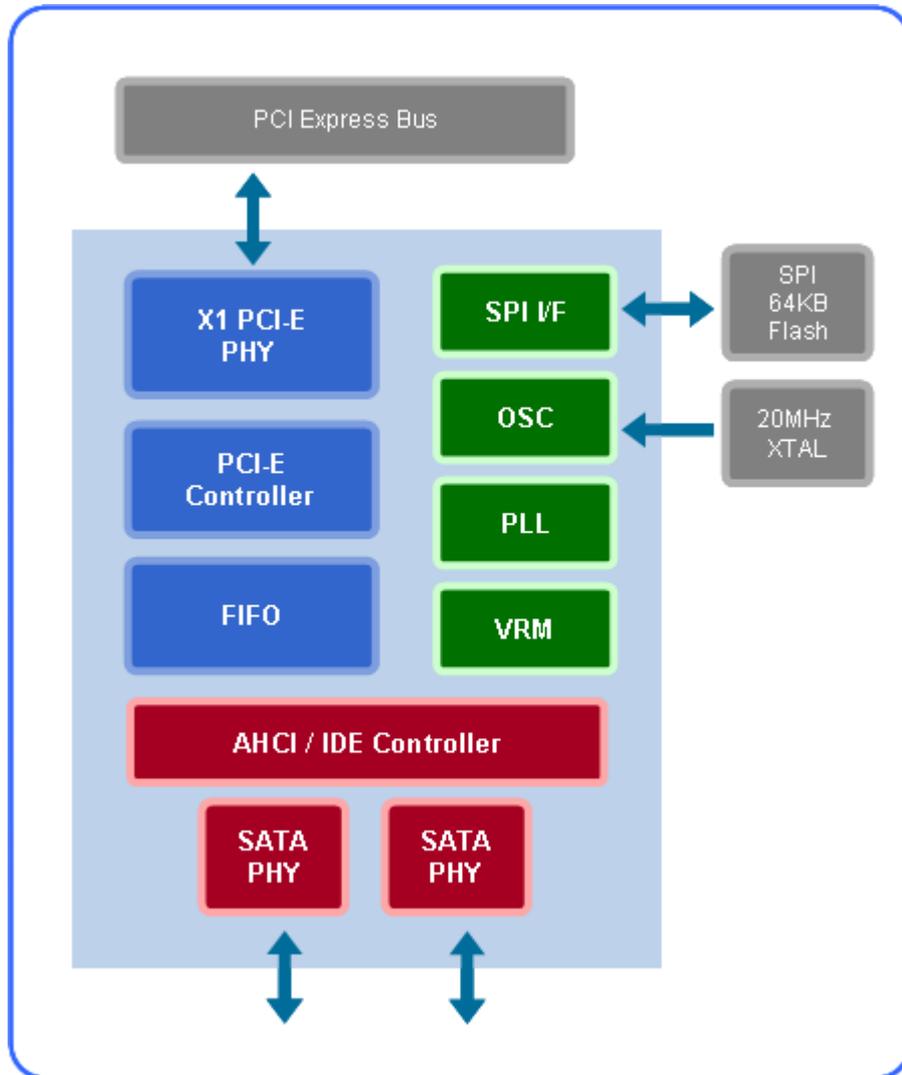


Figure 1: Functional Diagram

## 4. Pinout Diagrams

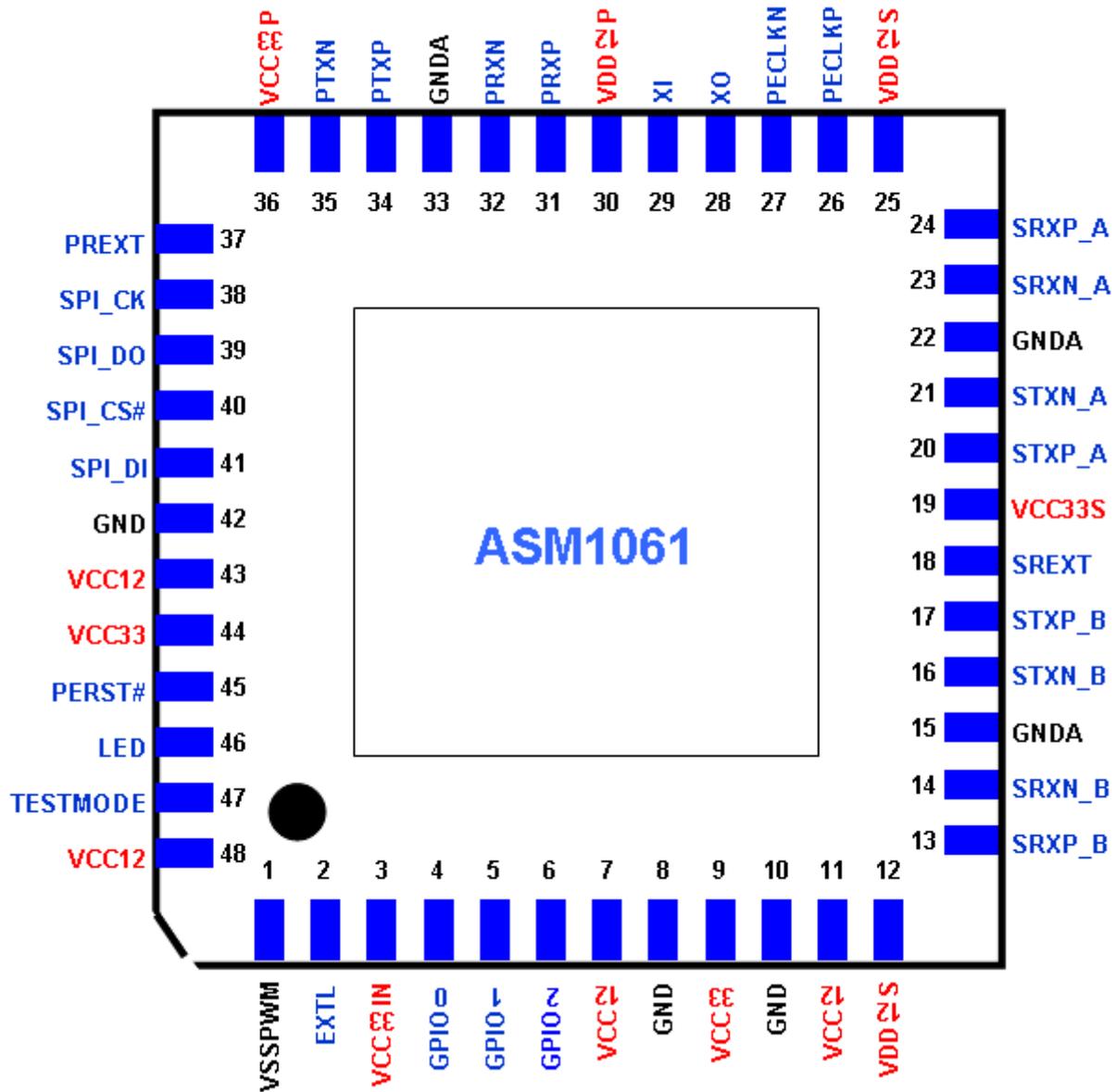


Figure 2: ASM1061 pinout

## 5. Pin Descriptions

This section provides a detailed description of each signal. The following notations are used to describe the signal type.

I/O Type	Definition
I	Input pin
O	Output pin
B	Bi-directional pin
Di	Differential pin
P	Power pin
G	Ground pin
OD	Open Drain
PU	Internal Pull Up
PD	Internal Pull Down

### PCI Express Interface

Pin No.	Name	TYPE	Descriptions
31	PRXP	DiI	PCI Express Differential Receive Signal +
32	PRXN	DiI	PCI Express Differential Receive Signal -
34	PTXP	DiO	PCI Express Differential Transmit Signal +
35	PTXN	DiO	PCI Express Differential Transmit Signal -
37	PREXT	<b>P</b>	External Reference Resistor with 12.1K ohm to GND for PCI Express
26	PECLKP	DiI	PCI Express Differential Clock Signal+
27	PECLKN	DiI	PCI Express Differential Clock Signal-
45	PERST#	I, PU	PCI Express Reset

### SPI Interface

Pin No.	Name	TYPE	Descriptions
38	SPI_CLK	O, PU	Clock of Serial Peripheral Interface
39	SPI_DO	O, PU	Data Output of Serial Peripheral Interface
40	SPI_CS#	O, PU	Chip Select of Serial Peripheral Interface
41	SPI_DI	I, PU	Data Input of Serial Peripheral Interface

### SATA Interface

Pin No.	Name	TYPE	Descriptions
24	SRXP_A	DiI	SATA Receive Signal + for Port A
23	SRXN_A	DiI	SATA Receive Signal - for Port A
21	STXN_A	DiO	SATA Transmit Signal - for Port A
20	STXP_A	DiO	SATA Transmit Signal + for Port A
13	SRXP_B	DiO	SATA Receive Signal + for Port B
14	SRXN_B	DiO	SATA Receive Signal - for Port B
16	STXN_B	DiI	SATA Transmit Signal - for Port B
17	STXP_B	DiI	SATA Transmit Signal + for Port B
18	SREXT	<b>P</b>	External Reference Resistor with 12.1K ohm to GND for SATA
28	XO	O	20MHz Crystal Output
29	XI	I	20MHz Crystal Input

### MISC Interface

Pin No.	Name	TYPE	Descriptions
1	VSSPWM	<b>G</b>	Internal Switching Regulator Ground
2	EXTL	<b>P</b>	Internal Switching Regulator Output. Need to connect a external Inductor. Please reference the

Pin No.	Name	TYPE	Descriptions
			demo circuit for the details.
3	VCC33IN	<b>P</b>	Internal Switching Regulator Power Supply
4	GPIO0	B, PU	General Purpose I/O 0
5	GPIO1	B, PU	General Purpose I/O 1
6	GPIO2	B, PU	General Purpose I/O 2
46	LED	O	SATA/PATA Port Access LED Indicator
47	TESTMODE	I, PD	Test Mode Enable

## Power and Ground

Pin No.	Name	TYPE	Descriptions
8, 10, 42	GND	<b>G</b>	Common Ground
15, 22, 33	GNDA	<b>G</b>	Analog Ground
9, 44	VCC33	<b>P</b>	3.3V IO Power
7, 11, 43, 48	VCC12	<b>P</b>	1.25V Core Power
19	VCC33S	<b>P</b>	3.3V Analog Power for SATA PHY
12, 25	VDD12S	<b>P</b>	1.25V Analog Power for SATA PHY
36	VCC33P	<b>P</b>	3.3V Analog Power for PCI Express
30	VDD12P	<b>P</b>	1.25V Analog Power for PCI Express

## Strapping Table

### Strapping for Spin-up Control of SATA Drives

SPI_DO	Function Description
1	Spinup controlled by register.
0	Spinup immediately

## 6 Electrical Characteristics

### 6.1 Absolute Maximum Ratings

Parameter	Range	Unit
Power Supply for 1.25V	-0.5 ~ +1.6	V
Power Supply for 3.3V	-0.5 ~ +4.5	V
DC Input Voltage	-0.5 ~ +4.5	V
Output Voltage	-0.5 ~ +4.5	V
Storage Temperature	-65 ~ 150	°C

### 6.2 Recommended Operating Conditions

Symbols	Parameter	Min.	Typ.	Max.	Units	Remark
VCC33, VCC33S, VCC33P	3.3V Normal Power Supply	3.0	3.3	3.6	V	
VCC12, VDD12S, VDD12P	1.25V Normal Power Supply	1.20	1.25	1.30	V	
Tj	Operating Junction Temperature	0	25	120	°C	
Tc	Operating Case Temperature		25	85	°C	

### 6.3 AC/DC Characteristics

#### Digital Pin Specification

Symbols	Parameter	Min.	Typ.	Max.	Units	Remark
VIH	Input High Level	2.0			V	
VIL	Input Low Level			0.8	V	
Ileak	Input Leakage Level			10	uA	
VOH	Output High Level	2.4			V	
VOL	Output Low Level			0.5	V	

### PCI Express Electrical Specification

(Refer to PCI Express Base Specification Rev. 2.0)

#### Differential Transmitter Output Ranges

Symbols	Parameter		2.5GT/s	5GT/s	Unit	Remark
UI	Unit Interval	Min	399.88	199.94	ps	300 ppm without SSC
		Max	400.12	200.06		
V <sub>TX-DIFF-PP</sub>	Differential p-p Tx voltage swing	Min	0.8	0.8	V	
		Max	1.2	1.2		
V <sub>TX-DIFF-PP-LOW</sub>	Low Power differential p-p Tx voltage swing	Min	0.4	0.4	V	
		Max	1.2	1.2		
V <sub>TX-DE-RATIO-3.5dB</sub>	Tx de-emphasis level ratio	Min	3.0	3.0	dB	
		Max	4.0	4.0		
V <sub>TX-DE-RATIO-6dB</sub>	Tx de-emphasis level ratio	Min	N/A	5.5	dB	
		Max	N/A	6.5		
V <sub>TX-CM-AC-PP</sub>	Tx AC common mode voltage	Max	20 mV	100 mVPP		
V <sub>TX-DC-CM</sub>	Transmitter DC common mode voltage	Min	0	0	V	
		Max	3.6	3.6		
V <sub>TX-CM-DC-ACTIVE-IDLE-DELTA</sub>	Absolute Delta of DC Common Mode Voltage during L0 and Electrical idle	Min	0	0	mV	
		Max	100	100		
V <sub>TX-CM-DC-LINE-DELTA</sub>	Absolute Delta of DC Common mode voltage between D+ and	Min	0	0	mV	
		Max	25	25		

Symbols	Parameter		2.5GT/s	5GT/s	Unit	Remark
	D-					
$V_{TX-IDLE-DIFF-A}$ C-p	Electrical idle Differential Peak Output Voltage	Min	0	0	mV	
		Max	20	20		
$V_{TX-IDLE-DIFF-D}$ c	DC Electrical Idle Differential Output Voltage	Min	Not Specified	0	mV	
		Max		5		
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection	Max	600	600	mV	
$C_{TX}$	AC Coupling Capacitor	Min	75	75	nF	
		Max	200	200		
$I_{TX-SHORT}$	Transmitter Short-Circuit Current Limit	Max	90	90	mA	
$Z_{TX-DIFF-DC}$	DC Differential Tx impedance	Min	80		$\Omega$	
		Max	120	120		
$T_{MIN-PULSE}$	Instantaneous lone pulse width	Min	Not Specified	0.9	UI	
$T_{TX-EYE}$	Transmitter Eye including all jitter sources	Min	0.75	0.75	UI	
$T_{TX-EYE-MEDIAN}$ -to-MAX-JITTER	Maximum time between the jitter median and max deviation from the median	Max	0.125	Not Specified	UI	
$T_{TX-HF-DJ-DD}$	Tx deterministic jitter >1.5MHz	Max	Not Specified	0.15	UI	
$T_{TX-LF-RMS}$	Tx RMS jitter <1.5MHz		Not Specified	3.0	ps	
$T_{TX-RISE-FALL}$	Transmitter rise and fall time	Min	0.125	0.15	UI	
$T_{RF-MISMATCH}$	Tx rise/fall mismatch	Max	Not Specified	0.1	UI	
$T_{TX-IDLE-MIN}$	Minimum time spent in Electrical Idle	Min	20	20	ns	
$T_{TX-IDLE-SET-TO}$ -IDLE	Maximum time to transition to a valid Electrical Idle after sending an EIOS	Max	8	8	ns	
$T_{TX-IDLE-TO-DIF}$ F-DATA	Maximum time to transition to valid diff signing after leaving Electrical Idle	Max	8	8	ns	
$T_{CROSSLINK}$	Crosslink random timeout	Max	1.0	1.0	ms	
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	Max	500ps + 2UI	500ps + 4UI	ps	
$BW_{TX-PLL}$	Maximum Tx PLL bandwidth	Max	22	16	MHz	
$BW_{TX-PLL-LO-3}$ DB	Minimum Tx PLL BW for 3dB peaking	Min	1.5	8	MHz	
$BW_{TX-PLL-LO-1}$ DB	Minimum Tx PLL BW for 1dB peaking	Min	Not Specified	5	MHz	
$PKG_{TX-PLL1}$	Tx PLL peaking with 8MHz min BW	Max	Not Specified	3.0	dB	
$PKG_{TX-PLL2}$	Tx PLL peaking with 5MHz min BW	Max	Not Specified	1.0	dB	
$RL_{TX-DIFF}$	Tx package plus Si differential return loss	Min	10	10	dB	
$RL_{TX-CM}$	Tx package plus Si common mode return loss	Mn	6	6	dB	

### Differential Receiver Input Ranges

Symbols	Parameter		2.5GT/s	5GT/s	Unit	Remark
UI	Unit Interval	Min	399.88	199.94	ps	300 ppm without SSC
		Max	400.12	200.06		
$V_{RX-DIFF-PP-CC}$	Differential p-p Rx voltage for common Refclk Rx architecture	Min	0.175	0.120	V	
		Max	1.2	1.2		

Symbols	Parameter		2.5GT/s	5GT/s	Unit	Remark
V <sub>RX-DIFF-PP-DC</sub>	Differential p-p Rx voltage for data clocked Rx architecture	Min	0.175	0.100	V	
		Max	1.2	1.2		
V <sub>RX-MAX-MIN-RATIO</sub>	Min/max pulse voltage on consecutive UI	Max	Not Specified	5		
V <sub>RX-CM-AC-P</sub>	Rx AC common mode voltage	Max	150	150	mVP	
V <sub>RX-IDLE-DET-DIFFP</sub>	Electrical Idle Detect Threshold	Min	65	65	mV	
		Max	175	175		
Z <sub>RX-DC</sub>	Receiver DC single ended impedance	Min	40	40	Ω	
		Max	60	60		
Z <sub>RX-DIFF-DC</sub>	DC Differential Rx impedance	Min	80	Not Specified	Ω	
		Max	120			
Z <sub>RX-HIGH-IMP-DC-POS</sub>	DC input CM input impedance for V>0 during Reset or power down	Min	50K	50K	Ω	
Z <sub>RX-HIGH-IMP-DC-NEG</sub>	DC input CM input impedance for V<0 during Reset or power down	Min	1.0K	1.0K	Ω	
T <sub>RX-MIN-PULSE</sub>	Minimum width pulse at Rx	Min	Not Specified	0.6	UI	
T <sub>RX-EYE</sub>	Receiver eye time opening	Min	0.4	N/A	UI	
T <sub>RX-TJ-CC</sub>	Maximum Rx inherent timing error	Max	N/A	0.4	UI	
T <sub>RX-TJ-DC</sub>	Maximum Rx inherent timing error	Max	N/A	0.34	UI	
T <sub>RX-DJ-DD-CC</sub>	Maximum Rx inherent deterministic timing error	Max	N/A	0.3	UI	
T <sub>RX-DJ-DD-DC</sub>	Maximum Rx inherent deterministic timing error	Max	N/A	0.24	UI	
T <sub>RX-EYE-MEDIAN-to-MAX-JITTER</sub>	Maximum time delta between median and deviation from the median	Max	0.3	Not Specified	UI	
T <sub>RX-IDLE-DET-DIFF-ENTERTIME</sub>	Unexpected Electrical Idle Enter Detect Threshold Integration Time	Max	10	10	ns	
L <sub>RX-SKEW</sub>	Lane-to-Lane Skew	Max	20	8	ns	
BW <sub>RX-PLL-HI</sub>	Maximum Rx PLL bandwidth	Max	22	16	MHz	
BW <sub>RX-PLL-LO-3DB</sub>	Minimum Rx PLL BW for 3dB peaking	Min	1.5	8	MHz	
BW <sub>RX-PLL-LO-1DB</sub>	Minimum Rx PLL BW for 1dB peaking	Min	Not Specified	5	MHz	
PKG <sub>RX-PLL1</sub>	Rx PLL peaking with 8MHz min BW	Max	Not Specified	3.0	dB	
PKG <sub>RX-PLL2</sub>	Rx PLL peaking with 5MHz min BW	Max	Not Specified	1.0	dB	
RL <sub>RX-DIFF</sub>	Rx package plus Si differential return loss	Min	10	10	dB	
RL <sub>RX-CM</sub>	Common mode Rx return loss	Mn	6	6	dB	

## PCI Express Differential Reference Clock Input Ranges

Symbols	Parameter	Min	Typ	Max	Unit	Remark
F <sub>IN-DIFF</sub>	The input frequency is 100 MHz + 300 ppm and max. – 5000 including SSC-dictated variations Differential input frequency		100		MHz	
	Rising Edge Rate	0.6		4.0	V/ns	
	Falling Edge Rate	0.6		4.0	V/ns	
V <sub>IH</sub>	Differential Input High Voltage	150			mV	
V <sub>IL</sub>	Differential Input Low Voltage			-150	mV	

Symbols	Parameter	Min	Typ	Max	Unit	Remark
V <sub>CROSS</sub>	Absolute crossing point voltage	250		550	mV	
V <sub>CROSS-DELTA</sub>	Variation of VCROSS over all rising clock edges			140	mV	
V <sub>RB</sub>	Ring-back Voltage Margin	-100		100	mV	
T <sub>STABLE</sub>	Time before V <sub>RB</sub> is allowed	500			ps	
T <sub>PERIOD-AVG</sub>	Average Clock Period Accuracy	-300		2800	ppm	
T <sub>PERIOD-ABS</sub>	Absolute Period (including Jitter and Spread Spectrum)	9.847		10.203	ns	
T <sub>CC-JITTER</sub>	Cycle to Cycle Jitter			150	ps	
V <sub>MAX</sub>	Absolute Max input voltage			1.15	V	
V <sub>MIN</sub>	Absolute Min input voltage			-0.3	V	
	Duty Cycle	40		60	%	
R/F Matching	Rising edge rate (REFCLK+) to Falling edge rate (REFCLK-) matching			20	%	
Z <sub>C-DC</sub>	Clock source DC impedance	40		60	Ω	

### Crystal Electrical Specification

Note: please refer to the figure 3

Symbol	Parameter	Min.	Typ	Max.	Unit
f <sub>XTAL</sub>	Frequency		20		MHz
Δf <sub>XTAL</sub>	Long Term Stability (at 25°C)	-30		30	ppm
T <sub>C</sub>	Temperature Stability	-30		30	ppm
F <sub>A</sub>	Aging	-5		5	ppm
C <sub>L</sub>	Load Capacitance (Single-end mode)		20		pF
C <sub>0</sub>	Shunt Capacitance	1	3	7	pF

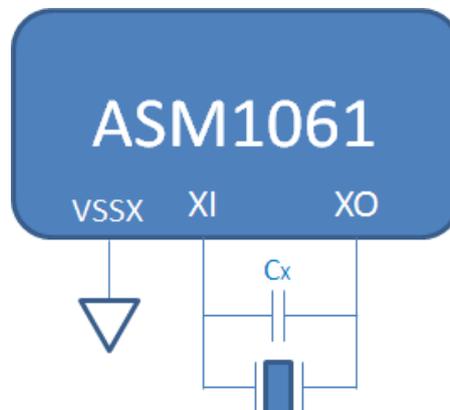


Figure 3: Differential Crystal Design

## Clock Oscillator Electrical Specification

Note: please refer to the figure 3

Symbol	Parameter	Min.	Typ	Max.	Unit
$f_{CLK}$	Frequency		20		MHz
$\Delta f_{CLK}$	Long Term Stability (all condition)	-150		150	ppm
$C_X$	External Load Capacitance (Differential mode)		10		pF
$C_{TOTAL}$	Total External Equivalent Capacitance from XI pin to XO pin (Differential mode)	12	14	20	Pf
$R_{TOTAL}$	Total External Equivalent Series Resistance from XI pin to XO pin			60	$\Omega$

## External Reference Resistor Spec Requirement

Parameter	Min.	Typ.	Max.	Units
PREXT PCIE External Reference Resistor		12.1K		Ohm
SREXT SATA External Reference Resistor		12.1K		Ohm

## Internal Switching Regulator Spec Requirement

Symbol	Parameter	Min.	Typ	Max.	Unit
$V_{IN}$	Input Voltage Range	3.0	3.3	3.6	V
$V_{OUT}$	Output Voltage Range	1.2	1.25	1.3	V
$\Delta V_N$ (p-p)	3.3V input voltage noise/ripple Range	-8		8	%
$F_{OSC}$	OSC frequency		1.5		MHz
$IP_{(LM)}$	P-channel current limiter		1		A

- **Strong recommend to have 10uF decoupling capacitor placed close to pin3 to filter the noise/ripple of 3.3V switching regulator input.**

## 7. Timing Diagram

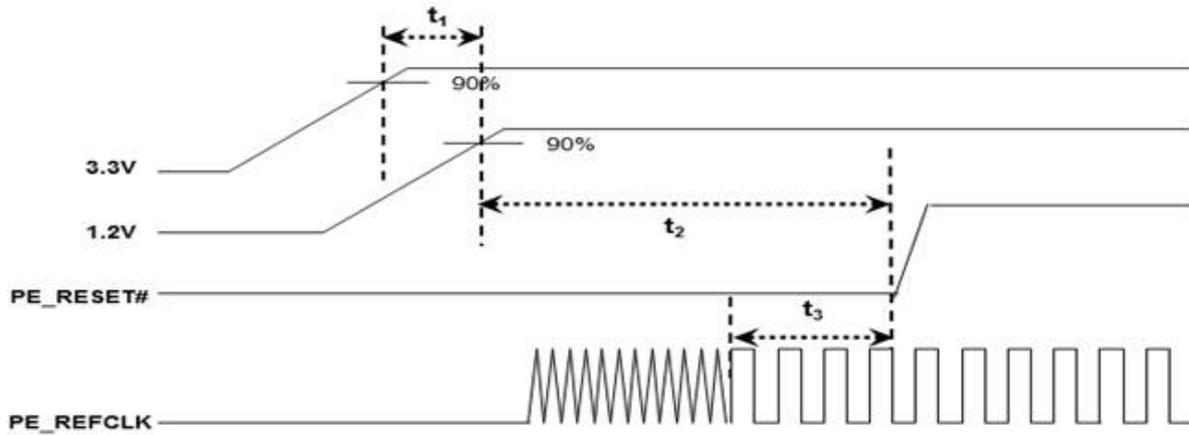


Figure 4: Power On Sequence

### Power On Sequence Timing Specification

Symbols	Parameter	Min	Max	Unit	Remark
$t_2$	Power on 90% ready to PE_RST#	100		ms	
$t_3$	PCI Express Reference stable Clock before PE_RST#	100		us	

## 8. Package Information

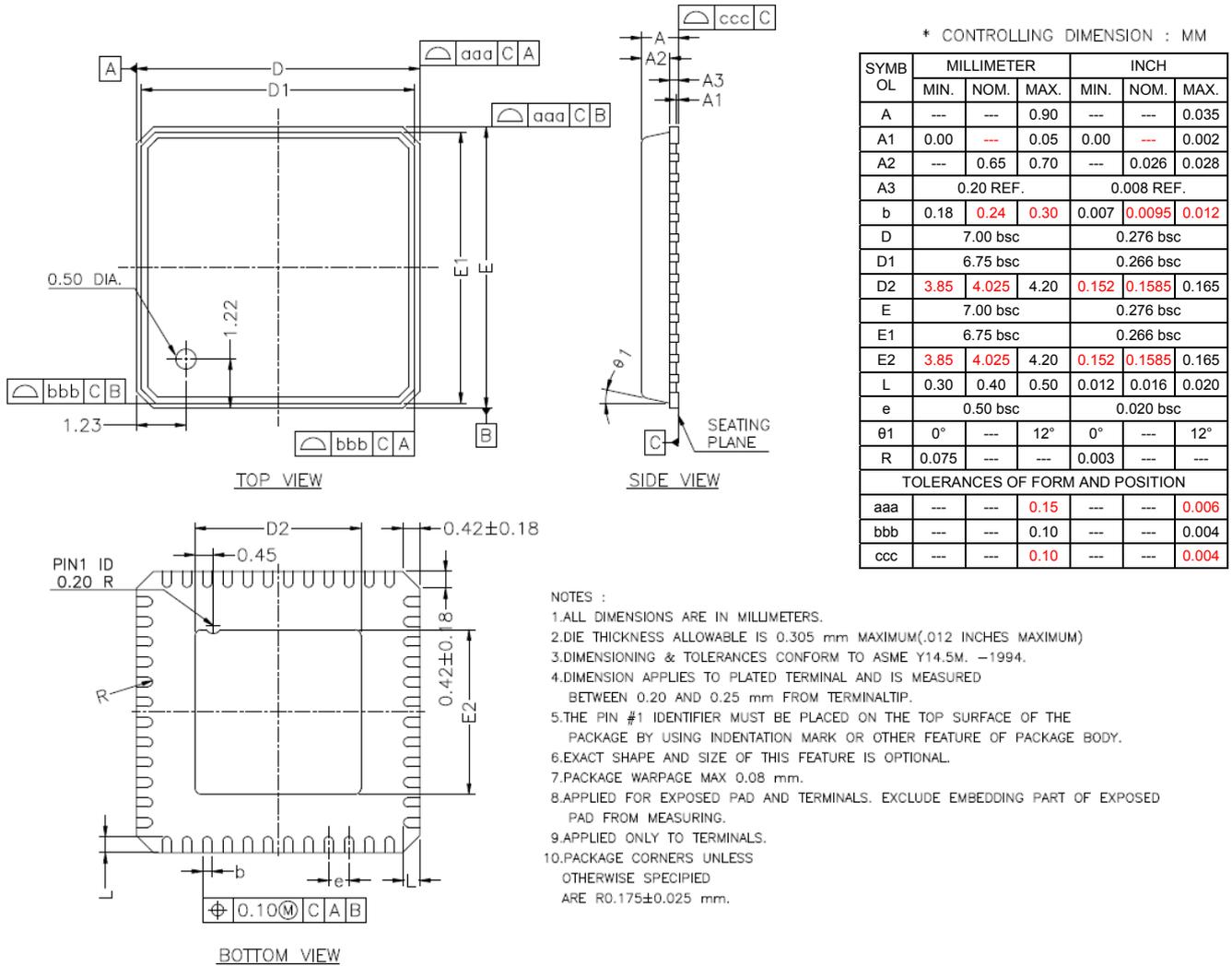
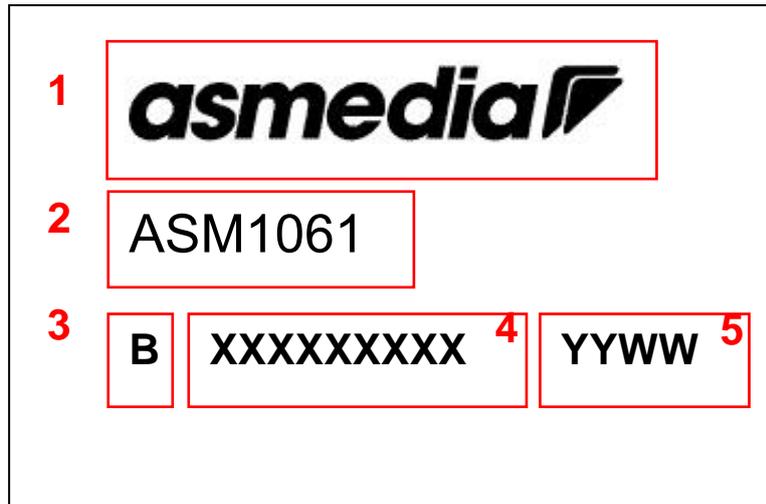


Figure 5: Mechanical Specification – QFN 48L



1. asmedia: ASMedia Logo
2. ASM1061: Product Name
3. B: Version of ASMedia Logo
4. XXXXXXXXXX: Serial No. Reserved for Vendor
5. YYWW: Date Code